PERFORMANCE OF DIFFERENT CMOS LOGIC STYLES FOR LOW POWER AND HIGH SPEED

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ABSTRACT

Designing high-speed low-power circuits with CMOS technology has been a major research problem for many years. Several logic families have been proposed and used to improve circuit performance beyond that of conventional static CMOS family. Fast circuit families are becoming attractive in deep submicron technologies since the performance benefits obtained from process scaling are decreasing as feature size decreases. This paper presents CMOS differential circuit families such as Dual rail domino logic and pseudo Nmos logic their delay and power variations in terms of adder design and logical design. Domino CMOS has become the prevailing logic family for high performance CMOS applications and it is extensively used in most state-of-the-art processors due to its high speed capabilities. The drawback of domino CMOS is that it provides only non-inverting functions because of its monotonic nature. Dual-Rail Domino logic, (also known as clocked Cascade voltage switch logic where both polarities of the output are generated, provides a robust solution to this problem.

KEYWORDS

Static CMOS Logic, Dual rail domino logic, pseudo nmos, Low power.

1. INTRODUCTION

VLSI designers have different options to reduce the power dissipation in the various design stages. For example, the supply voltage may be reduced through fabrication technology, circuit design or dynamically through the system level. Switched load capacitance may be reduced through technology scaling [10], efficient layout, circuit design, gate level optimization, and/or System level. This paper gives emphasis on low power design [2] aspect using some CMOS differential circuit families. In CMOS (*Complementary Metal-Oxide Semiconductor*) technology, both N-type and P-type transistors are used to realize logic functions. The static CMOS style [1] is really an extension of the static CMOS inverter to multiple inputs .Today, CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or bipolar circuits, a CMOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC The main principle behind CMOS circuits that allows them to implement logic gates is the use of p-type and n-type metal–oxide–semiconductor field-effect transistors to create paths to the output from either the voltage source

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or ground. When a path to output is created from the voltage source, the circuit is said to be pulled up. The other circuit state occurs when a path to output is created from ground and the output pulled down to the ground potential.

Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters [1]. The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power still demands high computational speeds. Hence, in recent VLSI systems the power-delay product becomes the most essential metric of performance.

2. STATIC CMOS LOGIC

The most widely used logic style is static complementary CMOS which consists of pull down and pull up networks as shown in Fig 1.

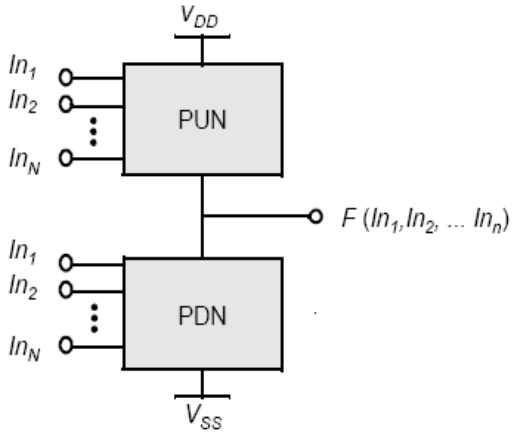

Figure 1. Static cmos logic

The static CMOS style is really an extension of the static CMOS inverter to multiple inputs.[1] In this static CMOS logic for an N-input logic gate, 2N-transistors are required which results in significantly large implementation area. Conventional static CMOS has been a technique of choice in most processor design. Alternatively, static pass transistor circuits have also been suggested for low-power applications [3] ,[12]. Dynamic circuits, when clocked carefully, can also be used in low-power high speed systems [4].

2.1. Static Adder

The Static CMOS logic adder design as shown in Fig 2 which consists of three input bits A, B, CIN, and has two outputs SUM and CARRY.

Sum = a xor b xor cin … A1
Carry=ab + acin+ bcin ….A2

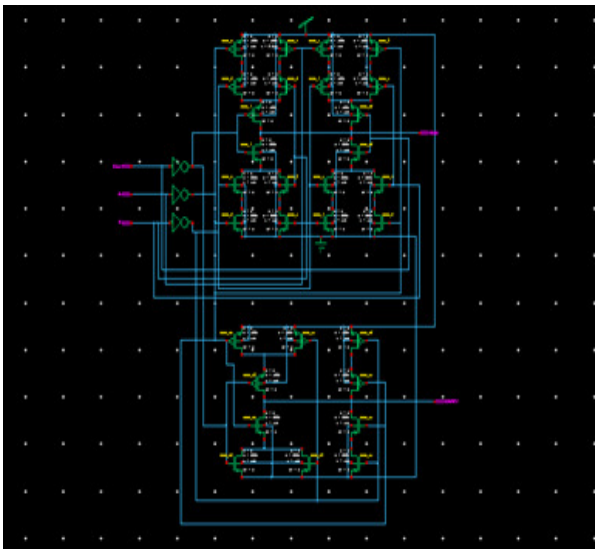

Figure 2. Static cmos adder

2.2. Static Logic

A static logic could be defined as a combinational circuit that performs the logical operations such has AND, NAND, XOR, XNOR. It consists of two inputs A and B and two outputs Fig 3 shows the logic level diagram of a static logic.

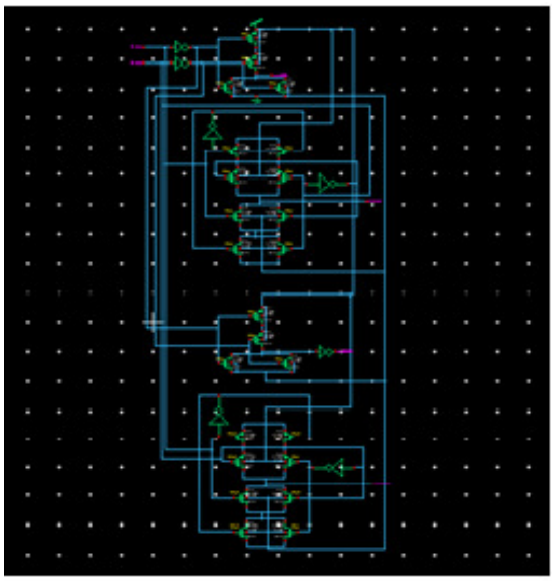

Figure 3. Static logic circuit

3. DUAL RAIL DOMINO ADDER

Domino CMOS has become the prevailing logic family for high performance CMOS applications and it is extensively used in most state-of-the-art processors due to its high speed capabilities [11].

3.1. Dual Rail Adder

Dual-Rail Domino Logic [5], [6], [8] is a pre-charged circuit technique which is used to improve the speed of CMOS circuits. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer. The dynamic circuit consists of a PMOSFET pre-charge transistor and an NMOSFET evaluation transistor with the clock signal (CLK) applied to their gate nodes, and an NMOSFET logic block which implements the required logic function. During the pre-charge phase (CLK = 0) the output node of the dynamic circuit is charged through the pre-charged PMOSFET transistor to the supply voltage level. The output of the static buffer is discharged to ground. During the evaluation phase (CLK = 1) the evaluation NMOSFET transistor is *ON*, and depending on the logic performed by the NMOSFET logic block, the output of the dynamic circuit is either discharged or it will stay pre-charged. Since in dynamic logic every output node must be pre-charged every clock cycle, some nodes are pre-charged only to be immediately discharged again as the node is evaluated, leading to higher switching power dissipation [1] ,[13]. One major advantage of the dynamic, pre-charged design styles over the static styles is that they eliminate the spurious transitions and the corresponding power dissipation. Also, dynamic logic does not suffers from short-circuit currents which in static circuits when a direct path from power supply to ground is caused. However, in dynamic circuits, additional power is dissipated by the distribution network and the drivers of the clock signal.

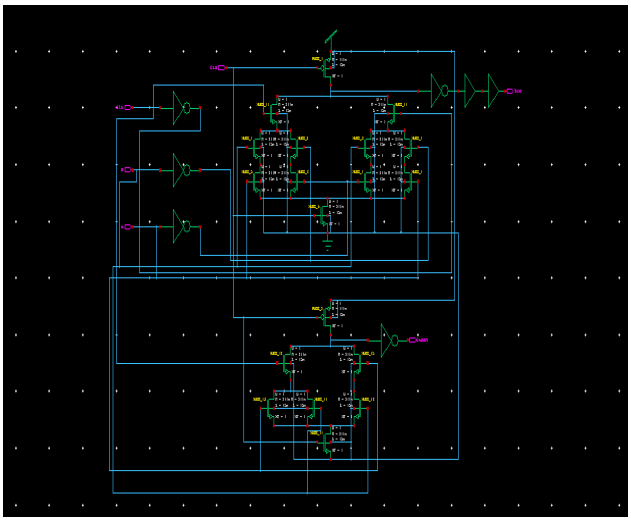

Figure 4. Dual rail adder

The Dual rail adder design as shown in Fig 4 which consists of three input bits A, B, CIN, and has two outputs SUM and CARRY.

3.2. Dual Rail Logic

Dual rail domino logic [6] could be defined as a combinational circuit that performs the logical operations such has AND, NAND, XOR, XNOR. It consists of two inputs A and B and two outputs Fig 5 shows the logic level diagram of dual rail logic.

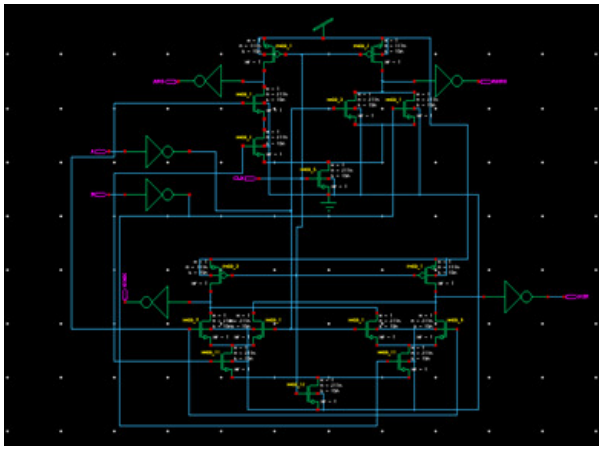

Figure 5. Dual rail logic

4. PSEUDO NMOS

4.1. Pseudo NMOS Adder

The design of a high-speed low-power I-bit full adder cell [7]. The main design objectives for this adder circuit are low power consumption and higher speed at low supply voltage. Using pseudo-NMOS [7], [8] together with two inverters this adder cell has been designed in CMOS process. As shown in fig (6). Considering transistor chaining, grouping, and signal sequencing in our proposed adder layout which all have noticeable impacts on the circuit performance, shows substantial power saving and high speed improvement [9] at no area penalty. Inverters act as drivers. Therefore, each stage will not suffer degradation in its deriving capabilities. This saves power, area, and time.

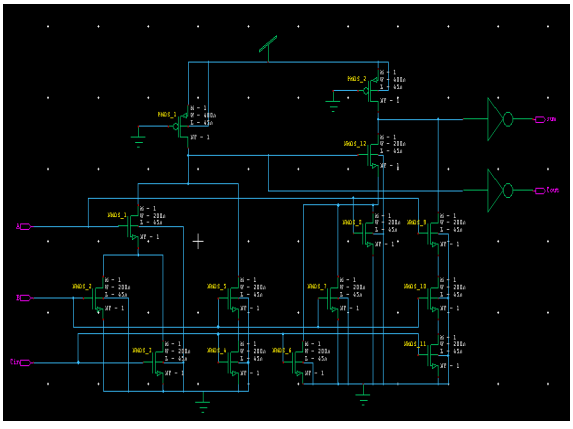

Figure 6. Pseudo NMOS Adder

4.1. Pseudo NMOS Logic

Pseudo nmos logic [7], [8] could be defined as a combinational circuit that performs the logical operations such has AND, NAND, XOR, XNOR.

It consists of two inputs A and B and two outputs Fig 7 shows the logic level diagram of pseudo NMOS logic.

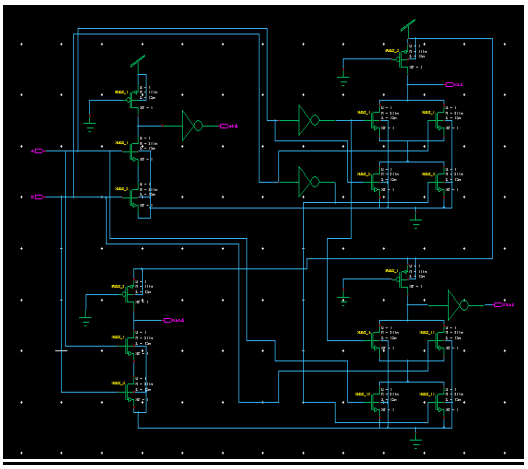

Figure 7. Pseudo NMOS Logic

5. OBSERVATIONS

The following are the observations of delay and power of static CMOS logic in 45 nm process.

Static cmos logic		
	Delay(Ps)	Power(µwatts)
Sum	442.18	0.49
Carry	540.12	0.69
AND	202.23	0.14
NAND	198.23	0.91
XOR	239.34	0.81
XNOR	276.54	0.83

Table 1. Static CMOS Logic Observations

The following are the observations of delay and power of Dual rail domino logic in 45 nm CMOS process

DUAL RAIL DOMINO LOGIC		
	Delay(Ps)	Power(µwatts)
Sum	543.45	0.56
Carry	298.3	0.65
AND	192.3	0.24
NAND	209.5	0.99
XOR	275.6	0.89
XNOR	299.8	0.95

Table 2. Dual Rail Logic Observations

The following are the observations of delay and power of Pseudo NMOS logic in 45 nm CMOS process

PSEUDO NMOS LOGIC		
	Delay(Ps)	Power(µwatts)
Sum	343.14	0.59
Carry	272.32	0.68
AND	182.15	0.27
NAND	175.53	1.01
XOR	225.6	0.92
XNOR	262.8	0.97

Table 3. Pseudo NMOS Logic Observations

5. SIMULATION RESULTS

5.1 The figure 6 shows static full adder sum and carry out puts.

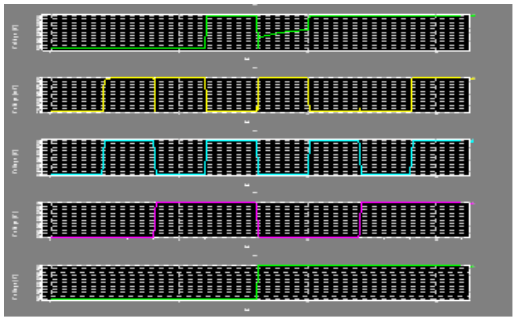

Figure 6. Static sum and carry

5.2 The figure 7 shows static CMOS basic gates like AND, NAND, XOR and XNOR Out puts.

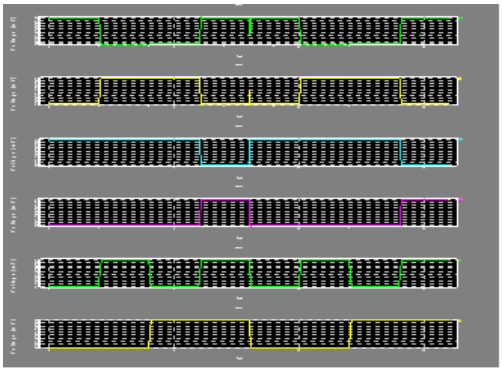

Figure 7. Static AND, NAND, XOR, XNOR

5.3 The figure 8 shows Full adder outputs by using Dual rail Domino Logic.

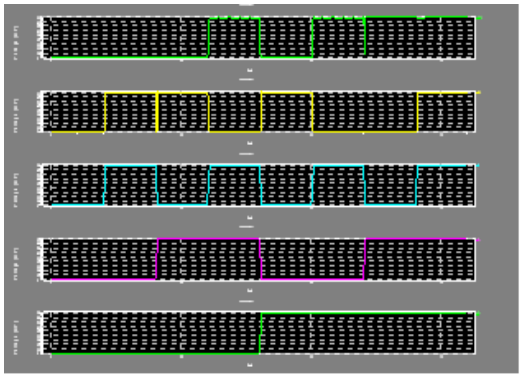

Figure 8. Dual Rail sum and carry

5.4 The figure 9 shows Dual rail Domino Logic basic gates like AND, NAND, XOR and XNOR Out puts

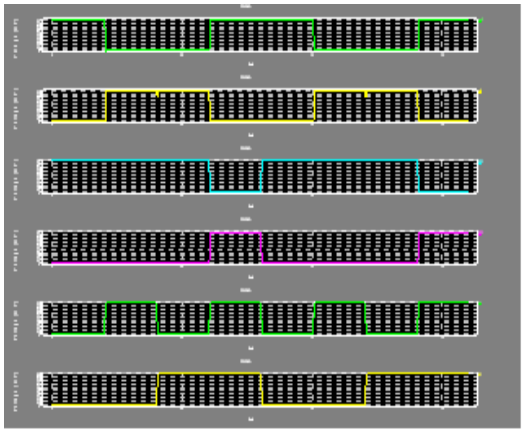

Figure 9. Dual Rail AND, NAND, XOR, XNOR

5.5 The figure 10 shows Full adder outputs by using Pseudo NMOS Logic

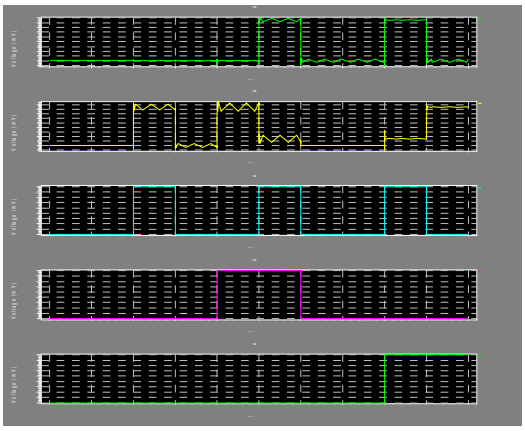

Figure 10. Pseudo NMOS sum and carry

5.6 The figure 11 shows Pseudo NMOS Logic basic gates like AND, NAND, XOR and XNOR Out puts

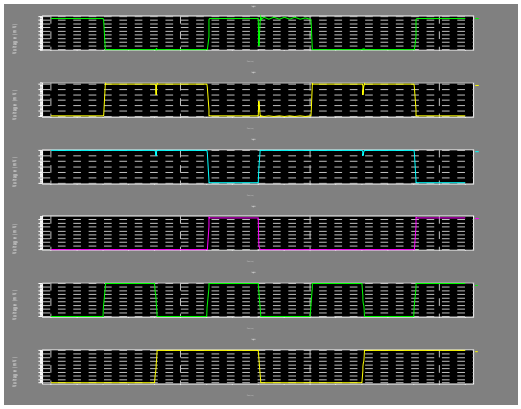

Figure 11. Pseudo NMOS AND, NAND, XOR, XNOR

6. CONCLUSION

In this paper we have implemented CMOS differential circuit families such as static CMOS logic, dual rail logic and pseudo NMOS logic which performs different arithmetic and logical operations. A comparison has been carried out between Static CMOS, Dual Rail Domino Logic and pseudo Nmos. In this thesis we have observed full adder sum and carry and also observed basic logic gates like AND, NAND, XOR & XNOR and also a 32-bit Arithmetic Logic Unit (ALU) has been designed & depending upon the Multiplexer selection the operations like ADDER, AND, NAND, XOR & XNOR has been performed along with this stimulation results were observed. In this paper among three logic the pseudo NMOS is low transistor count and high speed compared to static and dual rail logics.

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