Photonic Integrated Circuit Design in a Foundry+Fabless Ecosystem

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(Invited Paper)

***Abstract*—A foundry-based photonic ecosystem is expected to become necessary with increasing demand and adoption of photonics for commercial products. To make foundry-enabled photonics a real success, the photonic circuit design flow should adopt known concepts from analog and mixed signal electronics. Based on the similarities and differences between the existing photonic and the standardized electronics design flow, we project the needs and evolution of the photonic design flow, such as schematic driven design, accurate behavioral models, and yield prediction in the presence of fabrication variability.**

***Index Terms*—CMOS, photonic integrated circuits(PICs), foundry, fabless design, photonics ecosystem, process design kit (PDK), circuit design, design flow.**

I. Introduction

PHOTONICS has made tremendous progress in the last few years. The application base has broadened to a range of applications from optical communications to sensing. The photonics market today is shared by several material systems such as group IV semiconductors (silicon and germanium) [1], [2], compound III-V semiconductors (indium phosphide and gallium arsenide) [3], [4], silica *planar lightwave circuits* (PLC) [5], silicon nitride (with flavors such as TriPlex) [6], different polymers [7], and more exotic materials [8]. Among these, group IV semiconductor based photonics, often called *silicon photonics*, has become a prominent technology for *photonic integrated circuits* (PIC). This is due to the use of the existing *complementary metal oxide semiconductor* (CMOS) infrastructure and the high material index contrast between the guiding silicon and the cladding which permit sub-micron waveguides and a high integration density.

Silicon photonics itself covers a range of material systems such as *silicon-on-insulator* (SOI), *silicon nitride*-on-insulator (SiN), germanium-on-silicon, germanium-on-silicon nitride and silicon-on-silicon nitride. All these material systems are compatible with CMOS fabrication facilities and processes and support densely integrated circuits, so we can categorize all of them as silicon photonics. Among these silicon photonics material systems, the SOI is by far the most mature and the most widely used platform. It provides the highest possible integration density with the highest potential for high-volume manufacturing. However, the manufacturing volumes for even the most used SOI platform fall still several orders of magnitude short of those in CMOS electronics. To give an idea, few tens of thousands of wafers are required for entire photonics market per year which is in contrast to many tens of thousands of wafers being processed by a typical CMOS electronics fab in only a month [9]. Therefore, it is not feasible to set up a new infrastructure for such small production volumes and makes it compelling to use the existing CMOS fabrication facilities for silicon photonics. This availability of an existing foundry distinguishes silicon photonics from PIC technologies in other material systems based on the compound semiconductors, silica, and polymers.

A foundry provides fabrication services on one or more standardized platforms that can be accessed by third-party (fabless) designers. The third party can access the fabrication services directly or through a broker for *multi project wafer* (MPW), dedicated engineering runs, or for low or high-volume production [10]. As SOI is the most popular platform, so several CMOS foundries offer the open-access fabrication facilities for SOI platform. Some of the prominent foundries providing prototyping, MPW, and large scale production facilities are tabulated below in Table I. A more detailed overview of foundry activities, specific to silicon photonics, can also be found in [10].

To make a foundry model successful, offered technology platform should be sufficiently generic to address a diverse application market. *Silicon nitride* (SiN) being a CMOS compatible material was investigated to target life science applications (requiring visible light) because silicon is not transparent for wavelengths smaller than 1.1 μm. The transparency window for SiN extends to 0.4 μm which makes it very useful for life science applications [28]–[30]. The foundries providing the silicon nitride fabrication facilities are tabulated in Table II. A more detailed overview of foundry activities, specific to silicon nitride, can also be found in [31]. Integration of light sources and detectors makes SiN platform even more attractive for various applications [32]. Still, to make the foundry enabled

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TABLE I
SOME OF THE AVAILABLE OPEN-ACCESS SILICON-ON-INSULATOR FABRICATION FACILITIES

Foundry	Technology	Direct Access	Waveguide Thickness (nm)	Ref
ASP	e-beam	Direct	220	[11]
ANT	e-beam	Direct	220	[12]
CornerStone	e-beam & deep UV	Direct	220, 340, 500	[13]
AMO	e-beam	Direct	220, 340	[14]
AIM	-	MOSIS	-	[15]
CEA-LETI	193	Europractice	310	[16]
IHP	248	Europractice	220	[17]
IMEC	193	Europractice	220	[18]
IMECAS	-	SPP	220	[19]
INPHOTEC	e-beam	Direct	220	[20]
Sandia National Labs	-	Direct	240	[21]
VTT	UV	Direct	3000	[22]
AMF	248/193nm	Direct	220, 340	[23]
CompoundTek	193 immersion	Direct	-	[24]
Global Foundry	193 immersion	Direct	100	[25]
SMIC	-	Direct	340	[26]
TowerJazz	193nm	Direct	-	[27]

TABLE II
SOME OF THE AVAILABLE OPEN-ACCESS SILICON NITRIDE FABRICATION FACILITIES

Foundry	Technology	Access	Wafer Size (inch)	Ref
CNM-CSIC	i-Line	Direct	4,6	[33]
LIGENTEC	-	Direct	4,6	[34]
IMEC	193nm	PIX4life, Direct	8	[35]
AMF	248/193nm	Direct	8	[23]
LioniX	UV	PIX4life, Direct	-	[6]
AIM	-	MOSIS	12	[15]

photonics economically feasible for other material platforms, the margin on the fabrication needs to be sufficient to recover the investments and operations of the platform. This makes the foundry model suitable either for markets with sufficiently high volume (e.g., datacom transceivers) or for high-value, high-complexity products, which can often be found in medical, defense and aerospace markets. The added value of the PIC technology now comes from the integration of very complex functionality on a chip, which requires a reliable design flow that allows both the foundry and the third-party designers to make first-time-right designs.

Because the foundry model separates the designers from the actual technology, the design flow, software tools, and design kits should fill the gap that now separates the designers from physical fabrication. Circuit design already requires a higher level of abstraction, but the fact that in a foundry model the designer is now physically shielded from the actual technology (literally: in many cases the fabs do not disclose all the technological details of the fabrication to the users) requires some formal mechanism that enables the designers to design a working circuit reliably.

So, it is crucial to the success of a real foundry model for photonic integrated circuits to standardize the design flow for the photonic circuits in a similar fashion as it was done for electronics. In this article, we provide an overview of the similarities and differences between the currently used design flow for photonic integrated circuits, and especially larger-scale photonic circuits, to the standardized design flow for electronics. The best comparison is drawn with analog electronics, not digital, as analog electronics is still somewhat rooted in physical layout design as electronics, and photonic functions today are still mostly analog. Based on the differences we project how the design flow for the foundry enabled photonic integrated circuits will evolve and which requirements need to be fulfilled to make it a success, especially in the realm of standardization.

It can be said that the photonic integrated circuits using SOI are really moving towards electronics like circuits where the functionality is designed as a connection of functional building blocks instead of optimizing the component geometries. The number of chips fabricated by electronics is enormous in comparison to the photonic chips. So, in order to reduce the cost of the fabrication and to make the foundry enabled photonics the number of fabricated chips should scale up considerably. The capital expenditure for the foundries fabricating photonic chips is pretty high due to the small number of volumes for the photonic chips. So, either high margin chips with a lot of complexity or a foundry model to spread volumes over many applications are needed.

II. PHOTONICS DESIGN FLOW TODAY

Good design flow is a combination of different tasks organized in a systematic and reproducible manner to achieve the ultimate goal of turning an idea into a working chip. The step in the design flow needs to be backed up by efficient software tools that take the designer all the way to the tape-out of a working chip design, and this with high yield. Present photonics design flow can be divided into four major parts i.e.

- Component design & optimization
- Circuit design & simulation
- Layout generation
- Verification

Here we briefly discuss each of these to find out the missing links in this designs flow. Detailed design flow is discussed in [36].

A. Component Design & Simulations

Even though the common term for photonic chips is *photonic integrated circuits* (PIC), PIC design in the past couple

of decades has focused largely on the design of *building blocks* (also called *devices* or *component*). As the functionality of devices is entirely determined by the geometry and material parameters, good device relies heavily on the simulation of light propagation using electromagnetic modeling techniques such as *finite difference time domain* (FDTD) [37], *eigenmode expansion* (EME) [38], *finite element* (FE) [39], or *beam-propagation method* (BPM) [40].

We can separate devices in *passive* and *active* devices. Passive photonic devices are pure optical and therefore have no electrical function. In a first approximation, their behavior is also linear, but the functionality of passive devices can also be extended to optical nonlinearities. Passive devices range from elementary waveguide-based geometries like directional couplers [41] to complex periodic geometries like photonic crystals [42]. In a passive device design, there is essentially unlimited freedom to design the geometries, as long as it is compatible with the chosen fabrication technology. Optimization of the devices with such a large degree of freedom can be challenging and requires specialized algorithms [43]–[47], but this can often lead to impressive functional performance on a tiny footprint.

Active components also include an electrical function. This can be a tuning of a passive device through thermal and electromechanical effects. Other active devices include electro-optic conversions such as lasers, modulators, and amplifiers, or optoelectric conversion in photodetectors. Modeling such devices usually involves the physics of multiple domains (thermal, mechanical, carrier dynamics) and requires multiphysics simulations.

Given that the geometry entirely determines the propagation of light, photonic devices on a chip will be sensitive to variations in geometrical parameters and environment. This sensitivity depends very much on the material system, and especially the refractive index contrast between the materials used for waveguide cores and the materials used for the surrounding cladding. Higher index contrast allows for tighter confinement of light, but this will also make the device more sensitive to variations. This is particularly prominent in silicon photonics with its submicron waveguides and huge index contrast between the guiding layer and the claddings.

B. Circuit Design & Simulations

In contrast with device design, circuit design does not revolve around geometries. Instead, the focus is on connecting known devices in such a way that some desired, higher level of functionality is achieved. The geometric layout is of secondary importance and relates more to the placement of building blocks than adjusting their geometries. Currently, the complexity of the photonic integrated circuits is generally low, with tens to hundreds of components in a single circuit. This is a somewhat arbitrary metric, as the component count is not standardized (e.g., sometimes individual waveguide bends are counted as a separate component), and even the most complex designed circuits, such as multi-channel transceivers [48] and optical phased arrays [49], are a parallelization of simpler circuits. The circuit size is gradually improving (increasing) with improved technology platforms, especially for Indium Phosphide PICs [50]–[52] and silicon photonics [10], [53]–[55].

An increase in complexity depends very much on the availability of a circuit design flow and software tools that help the designer scale up his circuit design in a reliable way. This is where circuit design today is in full evolution. In order to predict the behavior of a circuit, the design needs to be simulated. Unlike with devices, it is no longer possible to use computationally intensive electromagnetic simulations to calculate the response of an entire circuit. Instead, in circuit simulation, the individual devices are abstracted into a behavioral response which maps the inputs to the outputs. These behavioral responses (compact models) are constructed based on physical simulations, theory, and measurements. There are several circuit simulation tools available in the market [56]–[60], and their use is increasing. However, the usefulness of these circuit simulation tools today is not limited by their engine and algorithms, but by the quality and availability of the compact models for the building blocks offered by the technology platforms. The circuit simulation can only be as accurate as the behavioral models of the components.

Photonic circuit simulations can be broadly divided into two categories, i.e. *frequency domain* and *time domain* simulations. Frequency domain simulations of the circuit calculate the wavelength dependent response (both amplitude and phase) between the input and the output ports of the circuit. As photonic components are wavelength dependent, the used behavioral models need to be accurate for the entire simulated frequency range. Frequency-domain simulations are most useful for passive linear photonic devices. These can be described by a frequency-dependent scatter matrix (S-matrix). As a linear system supports superposition, a scatter matrix describes all possible linear responses of the circuit. Also, as the S-matrix formalism is well known from microwave design, there exist standardized formats (e.g., Touchstone) to exchange S-matrix data [61]. Beyond linearity, the frequency-domain formalism can also be useful to describe certain nonlinearities, or the transmission of passive devices which are actively tuned, with a tuning that is much slower than the optical phenomena. Usually, this requires some iterative strategy to converge to the eventual frequency response.

Time domain simulations, on the other hand, solve the response of the circuit for a time-variant stimulus on the input ports of the circuit. The response of the circuit is solved by time-stepping the signals between all the nodes in the circuit, and updating the models at each step. The individual models should capture the underlying physics, either by incorporating the governing equations or by approximating them using a fitted black-box modeling strategy. Unlike S-matrices, there is little or no standardization in time domain circuit models for photonics. The models can be implemented in a variety of tools and languages, and their implementation can range from a set of ordinary differential equations (ODE) to fully-custom code models.

One particular implementation is a state-space model, where the behavior of a component is described using a set of states, which are related with one another and the input signals through a set of ordinary differential equations [62], [63]. For each time

step, first the states are updated based on the incoming signals, and then the outgoing signals are updated based on the new states. The variables in a state-space model can represent actual physical variables (e.g., the temperature of a thermo-optic phase shifter), or they can be fitted to some measured or simulated response curve, resulting in a black-box model that mimics the behavior of the component but where the internal variables have no relation with the actual physics. For instance, time domain models for the passive linear optical components can be fitted from frequency response by deriving a corresponding linear filter model, either with a finite impulse response (FIR) or infinite impulse response (IIR) [64], [65]. Note that time domain models usually work in a limited bandwidth, and model the signal as a modulation on top of a carrier wavelength. This works well for modeling simple communication systems, and it can be expanded to multiple carrier wavelengths for modeling wavelength division multiplexing (WDM) circuits, but it will not scale to the full optical bandwidth of tens of THz, as this would require either very short time steps or a massive amount of data exchange between components [36].

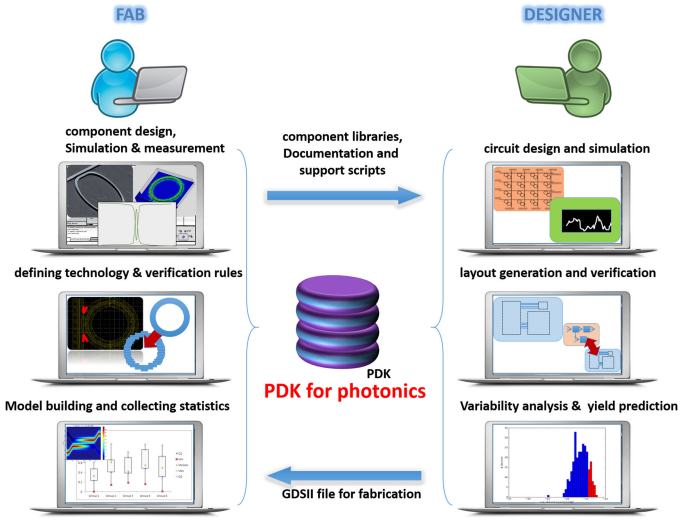

Fig. 1. The process development kit provides the necessary information about the fab to the designer. At present, process information, design requirements, basic building blocks, compact models and the verification decks are usually available in a PDK.

C. Process Design Kits (PDK)

An essential requirement for efficient circuit design is a library of qualified building blocks from which to construct a circuit. These building blocks are the result of the component design process. Historically, photonic component design and circuit design were combined in the same person or group, but with the emergence of foundry-based fabrication, a new communication channel is needed.

The *process design kits* (PDK) is the bridge between the foundry and component designers on the one hand, and the circuit designers on the other, and it has become an essential aspect of today's PIC manufacturing ecosystem. A PDK contains a library of the optimized components for a particular platform along with other practical details like design requirements, basic building blocks, verification deck, etc. It allows a circuit designer (with the right set of software tools) to construct a circuit that can be fabricated by the foundry.

The foundries usually maintain the PDKs for their technology platforms, but it is not uncommon that foundry customers extend the vanilla PDK with their proprietary component and subcircuit designs. The initial PDKs from photonic foundries were limited to information about the fabrication process, sometimes accompanied by a set of layouts of building blocks. The addition of *parametric cells* (PCells) for essential components such as waveguides came next, along with design rule checking (DRC) decks. Today, we see the emergence of PDKs with device models capturing the nominal (ideal) behavior of the devices in the building block libraries.

In a foundry-enabled fabless ecosystem, the *process development kit* (PDK) is playing an increasingly important role, as it serves as the middle man between the designer and the foundry, as shown in Fig. 1. The richness of the component library, the supported software tools and the sophistication of the device models have become a differentiator that is as important as the quality of the fabrication technology. This is understandable: as in electronics, the functionality of circuits is not necessarily determined by the quality of the single transistor, but by the circuit, and the reliability of the circuit design libraries determines the complexity of circuits that can be designed.

PDKs also allow fabs to encapsulate the essential properties of their technology platform without having to reveal the intimate details, which they might consider valuable intellectual property or trade secrets. Library building blocks can be represented as black boxes, and behavioral models can be compiled, so the actual equations and parameters are no longer accessible to the circuit designer. However, this encapsulation comes at a price: it requires some commitment of the fab to guarantee the performance of these black-box components, as the designer cannot second-guess the implementation and could, therefore, hold the fab liable in case their library components do not work according to the original specs.

D. Circuit Layout Generation

When sending design for fabrication in a foundry, it is communicated as a layout for the different mask layers. The layout is exchanged using *graphic data system* (GDSII) or *open artwork system interchange standard* (OASIS) format. GDSII has been the industrial standard for over 30 years, but recently OASIS seems to be gaining some traction because of smaller file sizes. Unlike in component design, where the layout consists of custom geometries, the layout in a circuit design mostly consists of placement of (parametric) cells, connected by optical waveguides and/or electrical wiring. Optical connections of components are more complicated than electrical connections. Waveguides need to maintain a minimum bend radius and separation to prevent excess waveguide losses and parasitic coupling. Most waveguide routing today is done manually, although some software tools support waveguide generation with different curve algorithms [66], [67]. Fully automatic routing of

complex layouts with tens of waveguides is not yet available. One particular obstacle for this is that most PIC technologies only support a single waveguide layer, and therefore need to introduce engineered waveguide crossings to connect nontrivial circuit topologies. [68], [69].

E. Verification

Once the layout has been generated, the layout is checked for potential errors and violations of the design rules provided by the fab. The design rules from the fab usually include the minimal critical dimensions, sharp angles and pattern density requirements. For this, photonics design relies on *Design rule checking* (DRC) software tools from the electronics, such as Calibre by Mentor [70], Cadence's Physical Verification System [71] or Synopsis IC Validator [72]. The foundries usually provide a design rule checking deck for one or more of these tools and require that the designers submit a DRC-clean design. One of the problems with early DRC decks for photonics arose from the fact that DRC software for electronics was not designed to handle the smooth curvilinear shapes that are typical for optical on-chip waveguides, and sometimes generate false errors. However, new DRC rules for the curvilinear structures and all-angle polygons are helping to improve the automated DRC checking process [73].

F. Summary of the Present Design Flow

Even when using standard building blocks from PDKs, photonic circuits today are still mainly designed as a physical layout. The design process does not have a smooth translation from the functional idea to the physical layout over a more abstract schematic, as is the typical workflow in analog electronics design. This lack of flow in this process is making it hard for designers to scale up the functionality and complexity of their photonic circuits.

III. Photonic Versus Electronic Design Flow

It is essential for the success of a real foundry based model for photonic integrated circuits to standardize the design flow similarly as it was done for electronics. In this section, we list the shortcoming in the current photonics design flow presented in the previous section. These shortcomings are marked down based on a comparison to the electronics design flow.

A. Compact Models

It has been mentioned in the previous sections that PDKs play an important role in a foundry enabled fab-less ecosystem as they provide the required information about the fab to the designer. The compact models, parametric cells and sensitivity of the performance parameters to fabrication variability are the most important elements of a PDK for the designer. Accurate compact models of the components are required for reliable circuit simulations, and the accuracy and standardization of compact models have played an important role in the success of a fab-less ecosystem for electronics. Photonic PDKs on the other hand lack in terms of the maturity and accuracy of the compact models. There is no standardization regarding the building of the compact models, so even the available compact models are specific to particular simulation software tools. So, standardization is required to expand the adoption and usability of compact models. In analog electronics design, such standardization has led to the widespread adoption of SPICE and Verilog-A, which in turn have stimulated fabs to invest in good model generation. As a result, electronic designers can trust their simulations, even for rather aggressive circuit designs.

Model standardization can also be done on the level of devices, by agreeing on a set of standard device descriptions for many conventional devices. This could start with passive devices such as waveguides, directional couplers, splitters, etc., but it could well be extended to include modulators and detectors. Amplifiers and lasers are examples of optical devices for which a set of widely accepted standard models have been developed [74].

B. Standardized Design Flow

Most of the electronic designers follow a standardized workflow with circuit hierarchy and reusable parametric cells. On top of the standardized work-flow, modern *electronic design automation* (EDA) tools help them automate the tasks which enable them to achieve the first-time-right design for even very complex circuits. Currently, there is no standardized design flow for the photonics, but with the increasing complexity of the photonic integrated circuits, the design process is evolving towards the standardization of the workflow in line with the electronic design automation.

As we will discuss in Section IV, this involves a more schematic-based approach to capture an idea into a circuit representation, before drilling down to the details of the circuit layout. In electronics, this translation is increasingly supported by software automation, where the layout tool can provide placement guidance and visual feedback on connectivity through fly lines, helping the designer to avoid connectivity mistakes. This *schematic driven design* speeds up the physical layout dramatically and is also emerging for photonics [66], [75].

C. Verification

The generated layout from the schematic is verified before forwarding to the foundry. However, electronic circuits are verified at a much deeper level than just checking the design rules. The more critical verification step involves checking of the functionality of the generated layout actually matches the original circuit design intent; this step is called the *layout versus schematic* (LVS) verification. LVS identifies the connectivity of the circuit by checking the overlaps of all electrical wiring. On top of that, more sophisticated LVS checkers also analyze the geometry of the wires and extract capacitive and inductive parasitic coupling. From this *parasitic extraction*, a more complicated circuit schematic is generated that can be simulated and compared to the original simulations.

In photonics, DRC has become a common practice, but LVS checking has proven to be complicated. First of all, it is not easy to extract the connectivity of photonic components from the layout. The primary connections can be fairly easily identified, as

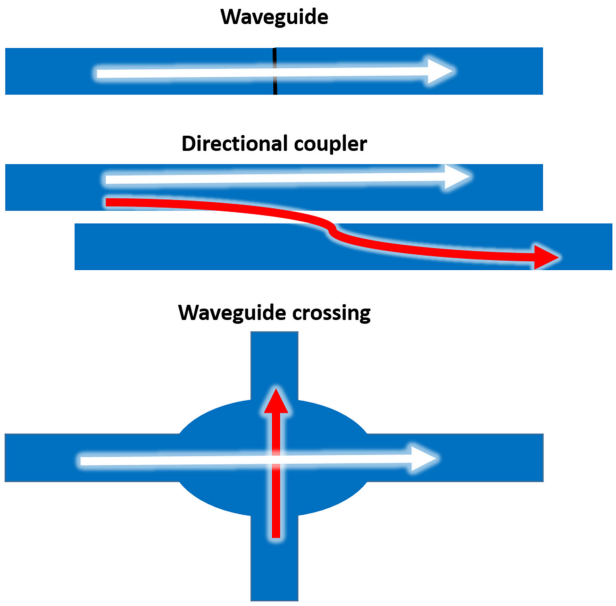

Fig. 2. (a) A waveguide is extended using another waveguide of the same dimensions. The waveguides need to be accurately aligned to get rid of the back-reflections and scattering. (b) Two waveguides do not come in physical contact with each other but light couples from one waveguide to another. (c) Two waveguides physically touch each other in a waveguide crossing, but one mode does not interrupt the other.

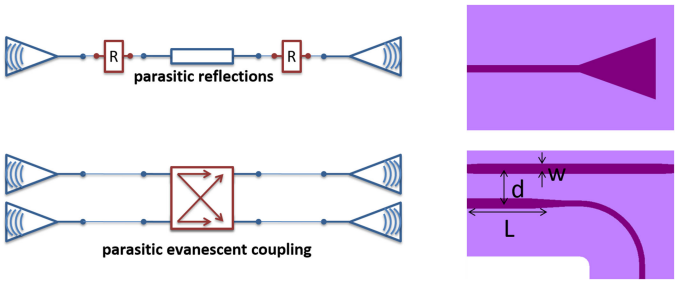

Fig. 3. The parasitics due to the back reflections/scattering in a straight waveguide and due to coupling in closely packed waveguides are depicted.

the waveguide ports of the building blocks and subcircuits can be annotated, and these connections can be checked against the original schematic. But it is much harder to identify unintentional connections and parasitics.

This can be explained using the example of the simplest photonic component, i.e., waveguide. Three different scenarios of waveguide connectivity are shown in Fig. 2 below. In the first scenario, a waveguide is connected to another waveguide of the same type. When the position and orientation match perfectly, they are properly connected. There should be no offset between the waveguides; otherwise, back-reflections and scattering will induce parasitic effects, Fig. 3. In a directional coupler, two waveguides are not physically in contact with each other but light can still couple from one waveguide to another. If such a directional coupler is implemented as a device, then it can be recognized for its function. But if such a coupler is unintentionally implemented by bringing two waveguides too close together, the parasitic coupling will occur, and the devices become connected when they should not be. This connectivity is not so trivial to detect and quantify in a layout. On top of that, such parasitic coupling is wavelength and geometry dependent as the coupling strength changes with the gap, coupling length and wavelength of operation. It should be mentioned here that this problem is not unique to photonics, for RF there is a similar challenge in verification, where usually designer expertise is complemented with full-scale electromagnetic simulation (which is still possible on an RF circuit, but not on a photonics circuit, as the circuit scale is much larger compared to the waveguide). A waveguide crossing is another example where an intentional design suggests coupling, but where it is engineered to let light pass straight on. On top of that, extracting parasitic back-reflections and scattering in waveguides, which can be stochastic in nature is very hard, but these effects can have a significant detrimental effect on the performance of larger circuits.

So, as it stands today, photonic layouts are not that easily verified with the original schematics. One thing that is now becoming more common is that at least the layout parameters of the building blocks are being taken back into the circuit simulation. For instance, the actual waveguide length can play a vital role in balancing interferometric circuits, so post-layout circuit simulations has proven a big step forward in photonic circuit design [66], [76]. Sometimes, electromagnetic simulations are required to find out the connectivity from a photonic layout, which is prohibitively expensive in terms of simulation time.

D. Variability Analysis

Variability analysis and the yield prediction are an essential part of the standardized electronics design flow. Traditionally, this was done through corner analysis, where the circuit is calculated using the best (fast) and the worst (slow) case scenarios for both PMOS and NMOS transistors. Based on this analysis, a circuit could be designed to work even in the worst-case scenario. More recently, corner analysis is gradually being supplemented to more complex statistical approaches, as reliance on corner analysis alone would usually result in overly conservative designs. With such statistical methods, yield can be predicted for different variations of a designed electronic circuit in the presence of a variety of different fabrication parameters.

In photonics corner analysis is not directly applicable, but Monte-Carlo simulations for variability analysis and yield prediction are needed, and slowly finding their way in the design flow [77], [78]. Variability for photonics can be explained with the example of the most basic building blocks, i.e., waveguide. A silicon wire waveguide is very sensitive to change in linewidth and thickness. Therefore, the effective and the group indices change as the geometry of the waveguide changes. This change in propagation constants can lead to phase errors in interferometric circuits with multiple delay lines, even when waveguides are placed close together. This sensitivity depends very much on the choice of technology platform, and especially the refractive index contrast between core and cladding. In silicon, a small variation in the waveguide core dimensions (linewidth, thickness) on the order of 1 nm can lead to shifting in wavelength

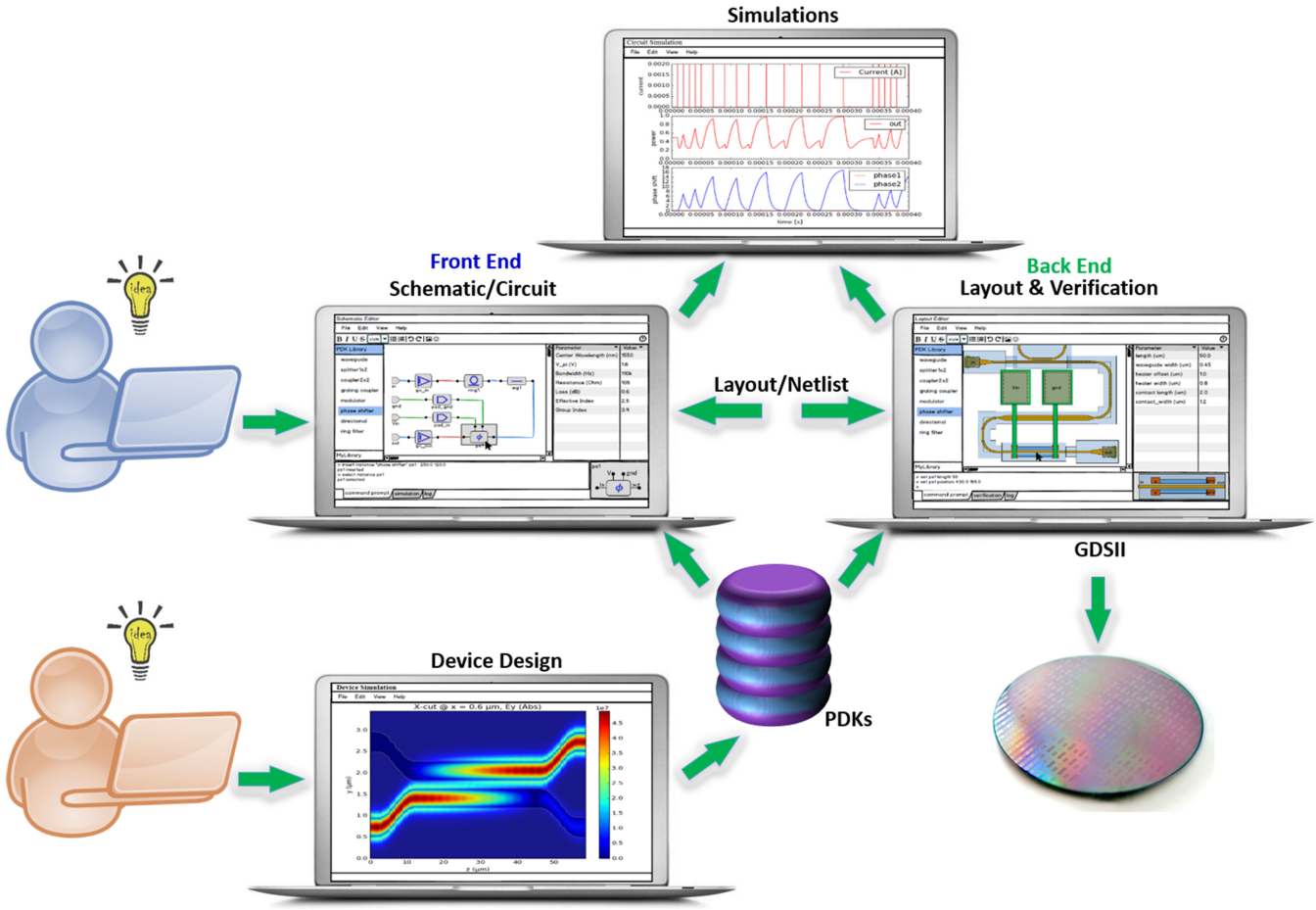

Fig. 4. In schematic driven design, an idea is converted into a logical schematic and then into a circuit. Circuit simulations are performed using the compact models from PDKs. The PDKs (which can be provided by the fab, internal or third party) contain the optimized components and compact models, so front end designers do not need to worry about the underlying physics of the components. The generated circuit by the front end designers is passed to the back end team for layout generation and verification. Fab uses the final mask provided by the back end team for fabrication.

response of a wavelength filter circuit of 1–2 nm, which would be unacceptable for many applications in dense wavelength division multiplexing (DWDM). This degradation in performance propagates to the circuit level, and the overall yield can drop drastically as the complexity increases, ultimately increasing the cost of the final product. Variability and yield prediction are discussed in detail in Section V.

IV. Future Photonic Circuit Design Flow

Now that we have compared the existing photonics design flow to that of the standardized electronics design flow, we are in a position to project how the circuit design flow is going to evolve with the incorporation of the missing links mentioned in the previous section, and we can also identify where some of the key changes in today's workflow are needed.

As in electronics, the emerging design flow will start from an idea and a logical schematic. In the current photonics design flow, it is normal practice to start from the physical component level, but this will gradually be changing from the physical component level to the abstracted schematic level. This is most likely to happen first in a foundry/fabless model, where the designers will be increasingly shielded from the exact fabricated geometry and process details. This *schematic driven design*, depicted in Fig. 4, starts from the more abstract schematic [65], [79].

In schematic driven design, a circuit is composed of the abstracted building blocks in a library, which can be part of the PDK or sourced from internal designs or third-party suppliers. The circuit designer is required only to know the functionality of the building blocks rather than having complete knowledge of the underlying physics. These libraries are hierarchical, so an abstracted building block can itself be a circuit consisting of other building blocks. This enables the designer to partition more complex circuit into tangible subproblems. This way, the circuit designer can cover the design from the building block all the way up to the higher level design, including the system implementation. Note in Fig. 4 that the design flow is restricted to the abstract (circuit design) levels without going into the component design using physical simulations. The component optimization will increasingly become more of a foundry responsibility, and every foundry will provide the PDKs with the optimized building blocks for their offered platforms. In case of building blocks with private intellectual property, the layout of the component can even be abstracted, and the PDK will only have a functional

block showing the logical mapping of the inputs to the output ports.

Schematic driven design can further be divided into the *front end* and the *back end* designs. The *front end* and *back end* design terminologies are being imported from the electronics design flow where these design stages are de-coupled from each other, allowing design teams to work in parallel. The front end comprises the abstract schematic-level circuit design, where the generated circuits are simulated using the circuit models.

In the back-end of the flow, the designed circuit is handed over to the layout designers for the generation of the mask layout. The abstracted components are replaced with the physical layouts of these components and placed on the layout canvas, in a similar hierarchical manner as in the schematic design. Component ports are connected based on the netlist defined in the schematic, using waveguides to complete the layout of the circuit. These waveguides are also optical components, so their properties will affect the performance of the circuit. As long as the waveguides have a mere connectivity function, this is usually not a problem. When the waveguides have a phase-sensitive function, like on interferometric filters, they should be treated as components in the schematic, and not as simple connectors.

The back-end designers will also need to take into account packaging and system integration requirements, adhering to optical, electrical and thermal guidelines [36]. These should be verified as part of the verification procedure, where not only manufacturing verification (DRC) is performed, but also LVS functional verification is carried out. After performing the DRC, post-layout simulations are performed to verify the functionality of the generated layout, preferably incorporating extracted parasitics such as backscattering and parasitic coupling [79].

One of the areas where a lot of work is ongoing is variability analysis and yield prediction for photonic integrated circuits [77], [78], [80]–[83]. We discuss this in more detail in the next section.

Future photonic design flow is meaningless without also incorporating electronics. Increasingly complex photonic circuits will also use complex electronic control, and many application also interface with high-speed RF signals. Therefore, it is a good trend that today there is a strong drive for co-integration of photonic design tools with the well established EDA tools. This integration will lead to co-design and co-simulation of electronics and photonics. This we discuss in more detail in Section VI. To summarize, photonics design flow is moving towards the standardization and *photonics design automation* (PDA) is steadily taking up design methodologies from the *electronic design automation* (EDA).

V. Variability Analysis and Yield Prediction

Depending on the material system, photonic circuits can be susceptible to fabrication imperfections, and variations in the linewidth and thickness of a waveguide can result into significant deviation of effective and group indices from the desired values. Similarly, gap variations between two parallel waveguides (for example in a directional coupler) introduce errors in the device's coupling. This is more pronounced in high-contrast waveguides, and because such waveguides can also scale to larger, more complex circuits, the effect of fabrication variability is most critical for such high contrast waveguides, like in silicon photonics. The deviations in performance of individual components accumulate at the circuit level and will degrade circuit performance severely, especially in phase-sensitive circuits like wavelength filters. Performance degradation in filter metrics such as channel cross-talk and deviation from the designed center wavelength becomes increasingly notable as the circuits become larger (e.g., longer delay lines) and more complex (e.g., more delay lines or filter stages). Since circuit parameters are not purely random, but spatially correlated, large-footprint circuits (e.g., with long delay lines) also increase the variation between components within a circuit, which further deteriorates the circuit performance. When the circuits are held to a given specification, this performance degradation will affect the yield of the circuit, i.e., the fraction of fabricated circuits working within the specification. Ultimately, fabrication variation induced performance variation increases the final product cost and limits the scaling capacity of circuits. Predicting fabrication yield is, therefore, becoming an essential part for a photonic circuit design flow, so it becomes possible to optimize circuits for yield instead of maximum performance [36], [81].

Realistic yield prediction requires a projection of the variations of low-level behavioral parameters (effective index, coupling coefficient) or fabricated geometry parameters (linewidth, thickness) to high-level circuit performance variations. The most straightforward method for this is based on Monte-Carlo simulations, with the statistical distribution of the geometrical variables (linewidth, thickness, ...) or behavioral variables (effective index, coupling coefficients, ...) as inputs. Monte-Carlo simulations can be computationally intensive, even if they can easily be parallelized. More efficient stochastic methods, such as polynomial chaos expansion (PCE) can reduce that simulation time drastically by capturing the statistical moments of the distribution as additional variables in an extended circuit, and solving that circuit only once [84].

A drawback of this approach is that the variables are assumed to be independent, and layout information is not really taken into account to correlate the variability between neighboring components in the circuit. This can be improved by using a layout-aware variability analysis [77], [78], [85]. This procedure consists of three steps: First, a detailed wafer map is generated from the fabrication variation. This map can contain variability contributions at different length scales, as process steps such as lithography, etching, and planarization have different spatial effects. Second, a good mapping between the geometric parameters and the circuit behavioral parameters is needed. This can be a direct mapping, but it is often easier to define a mapping based on sensitivity to deviations from the nominal values. Finally, the wafer map and the parameter mapping are combined to generate a circuit model with location-dependent circuit parameters, and the response is simulated. This last step is then repeated in Monte-Carlo fashion by placing the circuit in different locations on the wafer map or on different generated wafer maps. We discuss these steps in a bit more detail.

A. Fabrication Parameter Extraction Using Circuit Models

Extraction of the variations in fabricated geometry is essential in mapping fabrication variations to circuit performance variations. However, metrology of fabricated chips using a *scanning electron microscope* (SEM) or *atomic force microscope* (AFM) is either expensive, destructive or extremely time-consuming. Therefore, inline monitoring is usually reserved for critical steps, and done on a sampling of wafers and dies, and used to verify whether the fabrication process steps are within specifications. Also, the accuracy of such a measurement is not high enough to serve as an input for variability analysis. As an alternative, optical transmission measurements can be used to get an accurate measure of geometry variations. To find out the fabricated geometry of a waveguide (linewidth and thickness), effective and group indices are extracted and then mapped on to the linewidth and thickness of the waveguide using numerical models. In [77] ring resonators were used first to extract effective and group indices and then the fabricated geometry from the interfering spectrum. Although ring resonators provide very sharp features which provide easy parameter fitting, a ring consists of a combination of straight and bend waveguides, and their contributions cannot be separated based on the spectrum.

Instead, we used a combination of low and high order *Mach-Zehnder interferometers* (MZI), as shown in Fig. 5(a) to extract effective and group indices of the straight waveguide respectively [86]. The effect of bend waveguides in an MZI can be canceled out by using the same bends in both arms of the circuit. The effective and group indices were calculated by fitting the measured optical spectra to the simulations as shown in Fig. 5(c). A numerically developed geometrical model linking the waveguide effective and group indices was then used to estimate waveguide geometry (linewidth w and thickness t) [80]. This approach allows characterizing sub-nanometer precision of geometry extraction for straight waveguides fabricated using a foundry process line, which helps to identify process variations and non-uniformity across the device layer. Even if the mapping model is not perfect, this will mostly affect the absolute precision of the geometry: the relative variation between components is still valid and form a good basis to build a spatial variability model of a wafer.

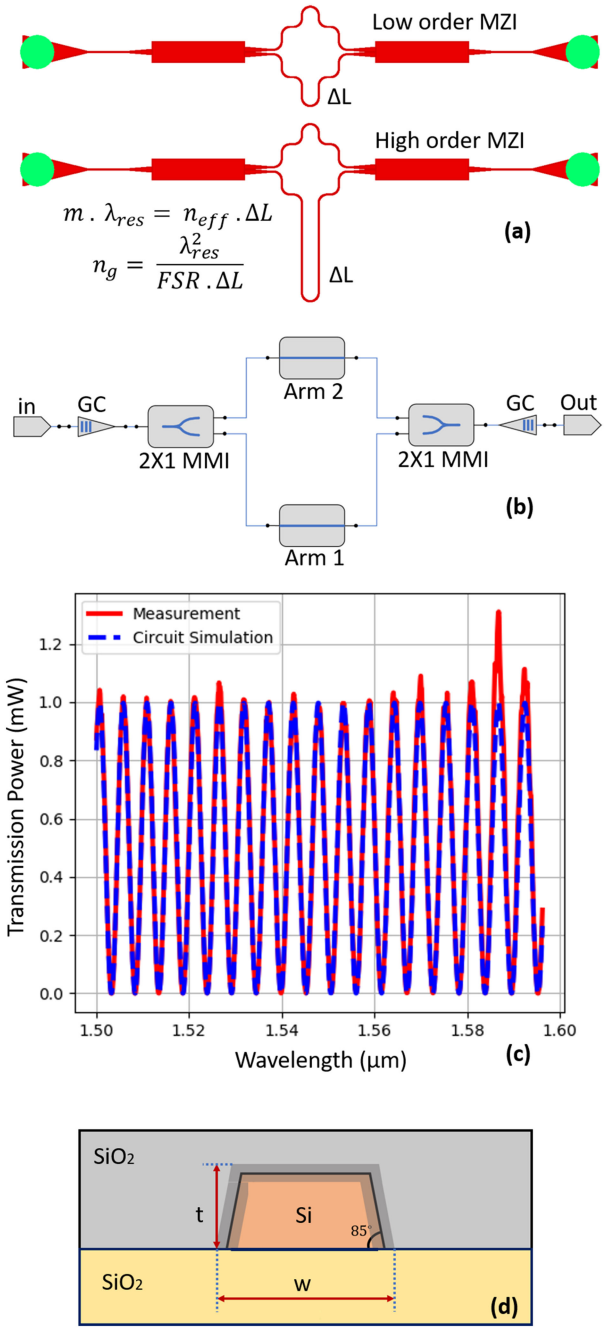

Fig. 5. (a) Two configurations of MZIs (having orders m = 15 and m = 150) for parameter extraction. (b) The circuit model used for fitting of the measured spectrum. (c) Extracting the n_{eff} and n_g using the curve fitting method. (d) Mapping n_{eff} and n_g to width w and thickness t.

B. Spatial Variability Model

To analyze the statistics of the parameters extracted from a fabricated wafer and make use of it in the yield prediction, we require a variation model which we can later use to generate synthetic wafer maps for Monte-Carlo simulations. The process-related parameter variations originate from a multitude of sources during the fabrication process, each with its own distribution over the wafer [87]. For example, wafer-level non-uniformity can come from layer thickness, photoresist spinning effects and plasma distributions, which varies slowly across the wafer and exhibits a symmetric radial pattern. Resources such as low-frequency change in layer thickness, local pattern density, and error in the photomask lead to intra-wafer and intra-die systematic variations. Different effects affect the wafer on shorter length scales. For instance, local pattern densities can affect dry etching plasma composition and thus affect the etch rate. Such layout-dependent variations will be repeated die-to-die over the wafer and superimposed on the longer-scale variations. On top of that, the model should capture random variations, both at die and wafer scale, as well as between wafers. Fluctuation in exposure dose and imaging focus add to the random die-to-die variation. Intrinsic randomness in layer thickness and waveguide sidewalls result in device-to-device random variation.

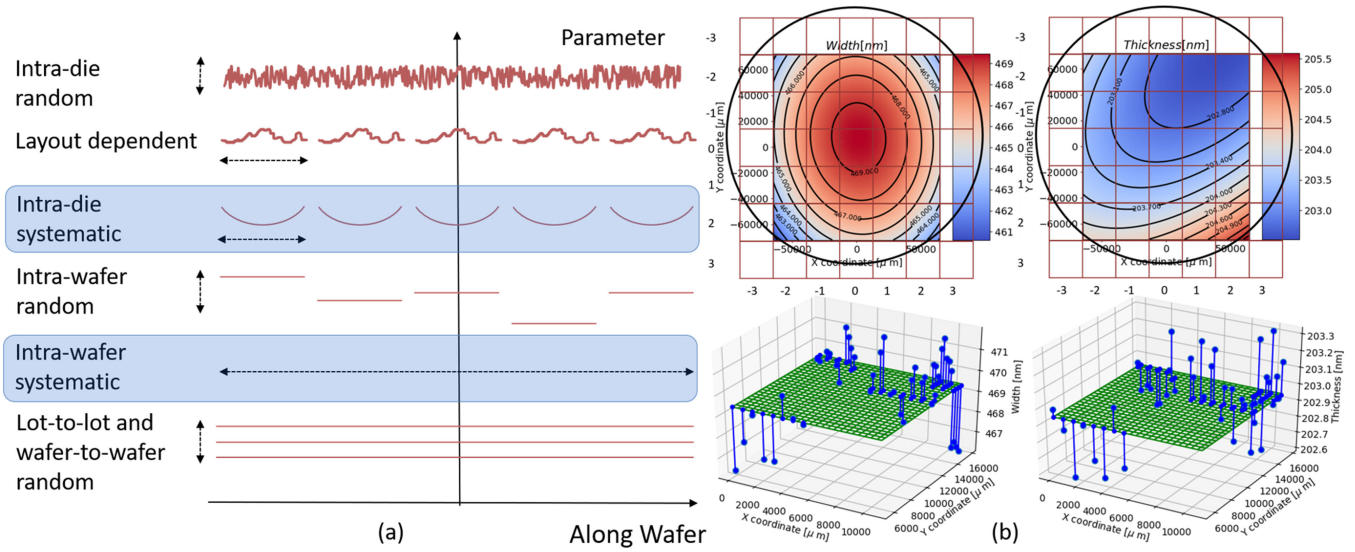

Fig. 6. (a) Illustration of spatial variability of device parameter at different levels. (b) Top wafer maps of linewidth and thickness present the systematic intra-wafer variations under the process variation. Bottom wafer maps represent the systematic intra-die variations of linewidth and thickness.

We can decompose the total spatial variation into lot-to-lot, wafer-to-wafer, die-to-die and device-to-device variations with systematic and random components, which can be combined into a hierarchical model (Fig. 6). This facilitates the characterization of statistical data measured on the wafer. For instance, in [87] we show an example where the waveguide thickness suffers significantly larger intra-wafer systematic variation (3.0 nm) than the intra-die systematic variation (0.7 nm), while linewidth has an intra-wafer systematic variation (8.5 nm) comparable with its intra-die systematic variation (5.0 nm). These separate variability components can be captured in generator models that replicate the essential statistical properties of the original variations, using deterministic functions of stochastic noise functions with a given correlation length. These map generators can then be used to perform location-aware variability analysis and yield prediction at the circuit level. Therefore, it would present a significant added value in the future for fabs to include such map generator functions into the PDK. These can be implemented as black box models, so there is no need to disclose process information that is considered confidential.

C. Location-Aware Yield Prediction

Waveguide-based filters are susceptible to phase variations and coupling variations. Monte-Carlo simulations using simple random distributed parameters already show the sensitivity of the circuit, but for yield prediction, this is not realistic since this method does not consider location-dependency of variations. For example, intra-wafer thickness variations with a radial pattern on the wafer affect devices in the center and near the rim differently, which is not considered by the standard Monte-Carlo method. Also, devices located next to each other should be more correlated than when placed further apart.

To make realistic predictions, we incorporated information about the spatial variations into the Monte-Carlo method. Using a virtual fabrication map (linewidth, thickness) generated by the additive spatial variation model, the local deviations from the nominal values are projected onto the circuit layout and then used to adjust the circuit model parameters of the building blocks

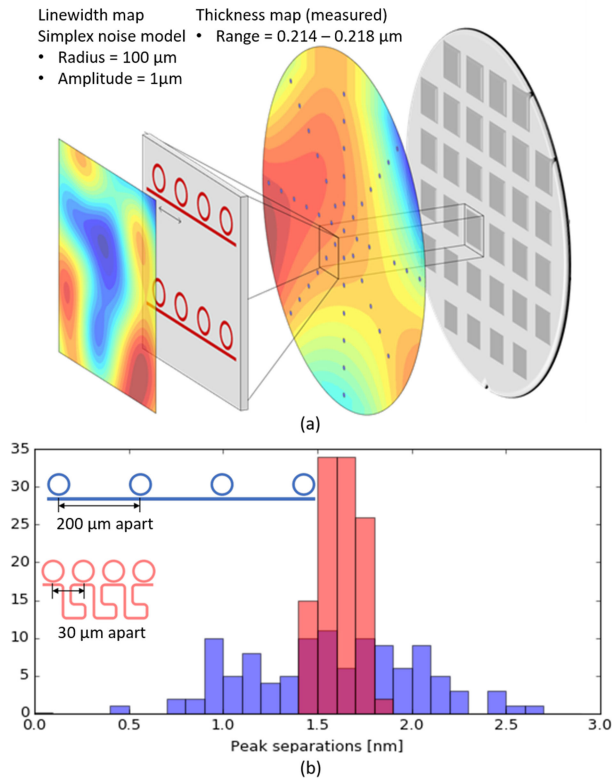

Fig. 7. (a) The generated linewidth and thickness maps used to find out the performance of ring demultiplexers over the virtual wafer. (b) Channel spacing distribution of the demultiplexer with rings spaced 200 μm and 30 μm apart are shown in blue and red respectively.

on the different locations. The circuit is then simulated using a circuit simulator. To analyze the variations, the circuit is then positioned on various wafer sites, or on different wafers [77], [78]. These simulations show that placing components closer together in a circuit does make the circuit less sensitive to local variations, but not to global variations. For instance, a circuit with multiple ring filters will show a much larger spread between the ring resonances when the rings are spaced further apart [77], [81].

For this technique to work, it is essential that all the information needed for this analysis is available to the circuit designer. This means that the foundry should be willing to provide not just compact models of the building blocks, but also wafer map generator functions of the critical fabrication parameters (or synthesized parameters that reflect the variability), as well as the sensitivity of the component model parameters to these parameters. Not only would this enable designers to make yield predictions of their circuits, but it would also allow them to design circuits that are more tolerant of variations [85]. For instance, it is possible to make MZI filter circuits more robust by combining multiple waveguide geometries within the same circuit, using the difference in sensitivity as a degree of freedom to compensate against long-range variations in linewidth or thickness [88].

VI. Models For Time-Domain Circuit Simulation

While passive photonic circuits are often modeled in the frequency domain, integration in a larger circuit or system requires that these same circuits are then evaluated in the time domain. However, frequency domain models are not always easily translated into time domain models, especially when the component or subcircuit has very strong dispersion. Furthermore, photonic circuits which contain nonlinear or electro-optical building blocks can only be modeled in the time domain, where the performance can be assessed through bit error rates (BER), eye diagrams or constellation diagrams [89], especially for telecom and datacom applications.

While the nonlinear of electro-optic components usually have good time-domain models where the behavioral equations are implemented into code, they are usually combined with passive components into the same circuit, and the accuracy of the entire circuit simulation is determined by the combination of models [36]. As the passive devices are usually parametric and combined into larger passive subcircuits, it is not trivial to translate the frequency domain response into a suitable time domain model that can be efficiently evaluated by the circuit simulator. A suitable circuit model should meet three basic requirements: 1) the models should be accurate enough with regard to the behaviors of the actual devices, and eventually generate valuable information to guide circuit designs; 2) the models must be represented in the time domain; 3) the models must be "compact" to make sure that the circuit simulation is efficient. How these criteria are met depends on the model generation strategies and the circuit simulation approach.

Since photonic circuits and electronic circuits closely work together and are integrated, the simulation should be conducted in both domains. There are several simulation approaches to combine these domains discussed and implemented in both academia and industry [36]: simulate photonic circuits and electronic circuits in 1) photonic simulators; 2) electronic simulators; 3) separate electronic and photonic simulators with unidirectional data exchange; 4) separate electronic and photonic simulators with bidirectional data exchange (Co-simulation) [90]. Therefore, before building the model, we should also be aware of where the models will be evaluated: in a photonic simulator or an electronic simulator? This is important because the signals propagating through the photonic and electronic circuits in simulations are quite different, as are the underlying equations. The photonic circuits use bidirectional optical waves as port signals while electronic circuits use voltage and current at each connection node.

Among the four simulation approaches, the second option (adopting electronic simulators for both electronic and photonic circuits) has shown a lot of promise [91], [92]. It is important to note that optoelectronic devices such as detectors, amplifiers, lasers, and modulators can have both electrical and optical behaviors, and therefore must be simulated in both domains, especially if they have electrical control loops [36], [90]–[92], which indicates that it is better to simulate electrical and optical behaviors at the same time.

Bidirectional co-simulation is not trivial to implement and requires two simulators to operate in lockstep [90]. While such techniques are also used in analog-digital mixed-signal (AMS) design, it can raise questions about stability and conservation of energy when exchanging information between the two domain [89]. While it requires that electro-optical components have representation in both simulation engines, the use of co-simulation makes it possible to use an optimized simulator for all parts of the circuit.

The first option (simulating everything in the optical simulator) can work if the optical simulator has some support for electronic components. However, it would require designers to abandon the trusted and mature electronic simulators and models, and rebuild models for electronic devices suitable for photonic simulators. It would also be difficult for a new simulator to match the established and standardized models for a large variety of electronic devices, which are natively supported by most electronic circuit simulators.

The opposite case, namely simulating the photonic part of the circuit in an electronic simulator, has more merits. A lot of effort has been invested in SPICE and/or Verilog-A compatible models for non-linear photonic devices, such as for lasers [93]–[95], modulators [96]–[98], photodiodes [99]–[102]. The linear photonic devices, such as waveguides, couplers, and wavelength filters, are normally characterized in the frequency domain and represented by transfer matrix (without reflection) and scattering matrix (with reflection). To build time-domain models for these devices which take into account higher-order dispersion, wavelength dependent loss, and imperfections in general, requires the fitting of a black-box behavioral model to the frequency response. Possible techniques include FIR based modeling method [64], or state-space model generation based on Vector Fitting [62]. Both techniques are based on scattering parameters and

are widely applicable to linear passive devices. Furthermore, the models built via both techniques have the potentials to be converted to SPICE and/or Verilog-A compatible circuit models, but can also be adapted to most photonic circuit simulators [63].

The main challenge to adopting the electronic simulators for photonic circuits is that they use inherently different signal models. In electronics, signals are represented by voltages and currents on nets, while in photonics they are forward and backward optical waves in optical waveguide modes, which are essentially transmission lines operating at very high (optical) frequencies. Therefore, the optical waves are often represented by their complex amplitude envelope which is a time-dependent complex number, modulated onto a high-frequency carrier wavelength. It is not straightforward to describe the complex-valued waves with voltages and current in electronic simulators. A simple solution is to mathematically interpret the magnitude/phase or real/imaginary parts of the complex envelope to voltage (potential) and current (flow) which is physically not sound but works as a purely mathematically construct [91], [103]. Another possible solution is to semi-physically interpret the optical waves to voltages and current, which essentially map onto the electric and magnetic field components of the guided optical mode(s) in the waveguide. Like for microwave systems, the non-conservative electromagnetic waves can be converted to voltages and currents through characteristic impedance [104], which in the optical domain is related to the effective index.

One of the obstacles for generalizing this approach for photonics is that this only simulates a fairly narrow frequency band around an optical carrier wave. This approximation only holds if there is only one coherent carrier wave. When multiple carriers are used, such as in wavelength division multiplexing (WDM) systems, each carrier should get its own signal line, and this only works well if the modulation bands of the carriers do not overlap at all. When this happens, or when broadband light is used instead of monochromatic carriers, it is no longer possible to represent the optical signal as a simple set of transmission lines.

VII. Summary and Conclusion

To summarize, the design process currently used by the photonic designers is still removed from the perfect process to translate a functional idea to the physical layout, and especially in a foundry/fabless setting where the circuit designer is decoupled from the fab. While the technology for the different PIC platforms is currently very capable of fabricating complex circuits, this scaling in complexity is currently limited on the design side. Photonic designers do not yet enjoy the comfort of a workflow, the software tools and design kits that guarantee them a first-time-right design, which is the expectation today in the electronics design community. It is not surprising that we are seeing today a closer integration between photonic circuit design tools and established EDA software packages.

So, following the footsteps of analog electronics, where designers can focus on circuits by trusting the provided standardized compact models, the introduction of a schematic driven design flow for photonics is a first step in improving this picture. But the success of this design flow depends very much on the availability of circuit models. The current lack of standardization in model building (and their interoperability between circuit simulators) slows down the investments of the foundries in sophisticated compact models. Also, the integration between photonic and electronic design tools raises the question of the best co-simulation strategies for electronics and photonics.

Depending on the PIC technologies, it is also essential that these models capture the effects of variability. Especially with high-contrast waveguide systems such as silicon, variability analysis, and yield prediction techniques are desperately needed to enable scaling in complexity.

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