PHY 351/651 – LABORATORY 6

The Bipolar Junction Transistor (BJT)

Reading Assignment

Horowitz, Hill Chap. 2.01 – 2.12; 2.23 (p50-68, p89-91)

Data sheet

Overview

In today's lab activities, you will utilize LabVIEW to explore the basic properties of the bipolar junction transistor (BJT). As you learned about in your reading, the BJT is one class of semiconductor-based transistors. Speaking most generally, the transistor is one of the building blocks of modern electronics: transistors are used in everything from amplifiers to power supplies to transducer circuits and switches, and they are one of the main components from which integrated circuits (ICs) are built. Thus developing a basic, working knowledge of transistors should be of great utility for anyone involved in experimental research or the development of new technology.

Physically, a transistor is a three-port, non-Ohmic, active device whose operation derives from the characteristics of the doped semiconductor material from which the device is made. For the case of the BJT, it can be understood in terms of the characteristics of the *PN junction*, which we have already studied in the context of the *diode* (Lab 5). In essence, the BJT is made from *two* PN junctions sandwiched together. As shown in Figure 1a, it can come in two different types: the *npn* and the *pnp*. In the *npn* type, as the name suggests, the middle region is composed of *p*-doped silicon; and in the *pnp* type, the middle region is composed of *n*-doped silicon. In either case (*npn or pnp*), there are three distinct regions known as the *emitter*, the *base*, and the c*ollector* (Fig. 1a), each of which is separated from the next by a PN junction (i.e. there is the emitter-base junction and the collector-base junction). In practice, through electrical connections to each of the three regions (Fig. 1b), the emitter-base junction and collector-based junction can be forward or reversed biased independently, allowing for four different modes of operation of the BJT. In today's lab you will use an *npn* type BJT to explore the three most important of these modes (*forward active*, *saturation*, and *cut-off*).

While the BJT is not as commonly used in integrated circuits (ICs) these days as its cousin the *field effect transistor* (FET), it is still employed for many different electronic tasks including the amplification of signals, switching, handling of large current, and the engineering of circuit impedances. You will explore some of these applications today, and in the process you should develop experience that will enable you to appreciate how transistors are used more generally, including in ICs.

Laboratory Goals

The plan for the day is as follows. In Activity 1, you will utilize a VI from a previous activity to measure, store and analyze the characteristic curves of a commercial BJT in a standard

configuration known as the *common-emitter* configuration. In Activity 2, using these characteristic curves, you will then design, build and operate an important circuit known as the *common-emitter amplifier*. In Activity 3, you will build a circuit known as the *emitter follower* (also known as the *common collector* amplifier). Finally in Activity 4, you will investigate switching behavior of a transistor and use it to build a two-transistor logic gate (specifically, a NOR gate).

Today's learning objectives are as follows:

- To gain additional experience in the use of LabVIEW to configure and operate your DAQ for analog input operations.
- To gain additional experience constructing circuits on the 503 proto-typing board.
- To become familiar with the properties and operation of a common type of silicon transistor, the MPS3904 npn bipolar junction transistor.
- To develop an appreciation for the importance of transistors in general.

Equipment

- PB-503 proto-typing board
- BK Precision Function Generator or DG1022 Generator
- A dual channel power supply (model/manufacturer will vary)
- MPS3904 silicon npn transistor
- Various resistors and capacitors
- NI USB-6003
- Hand-held digital multi-meter, banana cables, coaxial cables, and BNC-to-mini-grabber adapters

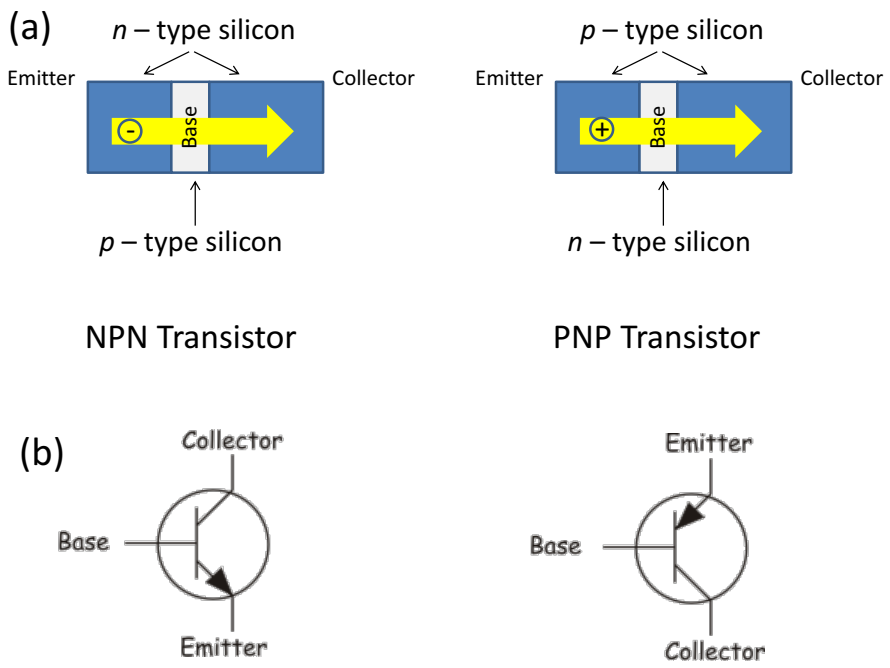


Figure 1: Schematics of the two types of BJTs. (a) The yellow arrow illustrates the majority current when the transistor is biased in the *forward active regime (see text)*. For the NPN transistor, electrons are injected from the emitter through the base to the collector (so conventional current is in the opposite direction). (b) Circuit symbols for the NPN and PNP transistors respectively.

Activity 1 – Measuring the Characteristic Curves of the MPS3904 Silicon npn Transistor in Common Emitter Configuration

Generally speaking, transistors are three-port (or three-terminal) devices. For the case of the BJT, the three terminals are known as the emitter, the collector, and the base (Fig. 1b). For typical operation of a BJT, one port of the transistor serves as an input for signals, another port serves as a signal output, and one port serves as the common for the input and output (Fig. 2a). Correspondingly, for such operation, there are three possible, different BJT configurations; these are known as the common-emitter (CE), common-base (CB), and common-collector (CC) - as the names suggest, each configuration is labeled by the terminal that serves as that configuration's common. Figure 2b illustrates the circuit connections for the CE and CC configurations, the two configurations which you will be working with in today's lab activities.

Because of differences in the level and polarity of doping between the three regions of the transistor (e.g. for the *npn*-type, the emitter is heavily n-doped, the collector lightly n-doped, and the base is lightly p-doped) and differences in geometry between the two (the collector usually occupies greater volume and the emitter the smallest), the three BJT configurations have distinct operating characteristics (i.e. current gain, voltage gain, and input/output impedance) that make them suitable for different applications. For example, the CB configuration has relatively large output impedance, thus making it suitable in some applications as a current source. By contrast, the CC (also known as the emitter-follower configuration) has characteristically low output impedance, making it useful (as you will see later) as a voltage buffer. To round out our

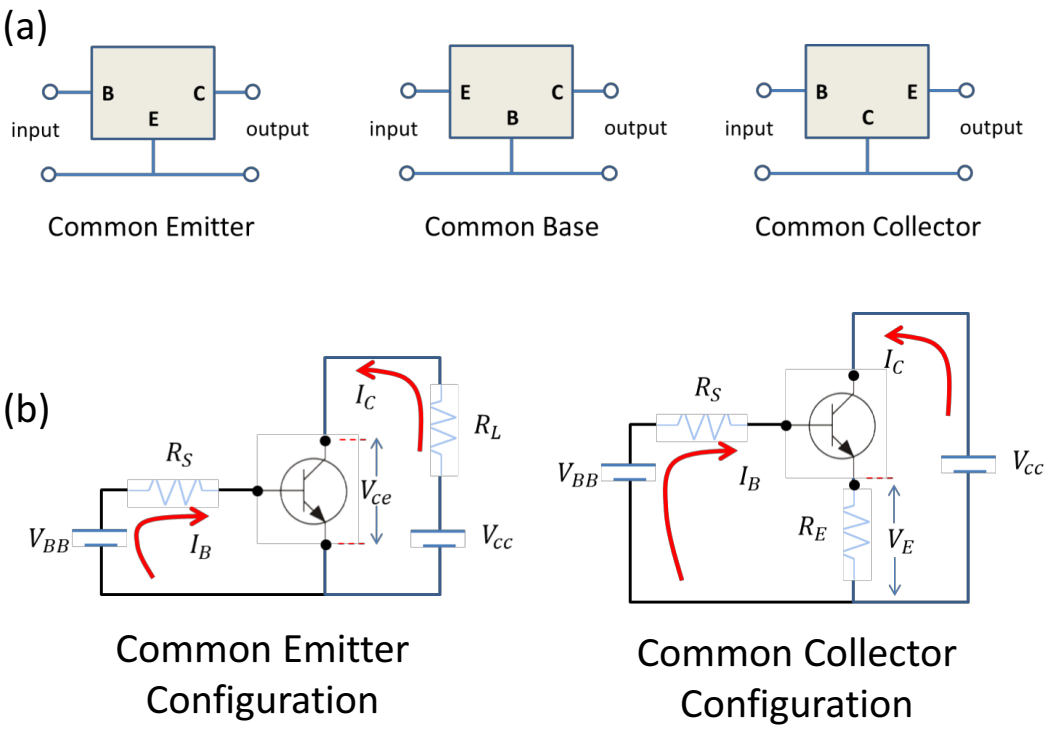


Figure 2: (a) Schematic of the three BJT configurations and their corresponding inputs and outputs. Here B stands for "Base"; E stands for "Emitter"; and C stands for "Collector". (b) Circuit schematics of transistor connections for CE and CC configurations. For CC mode, the output is taken across R_E.

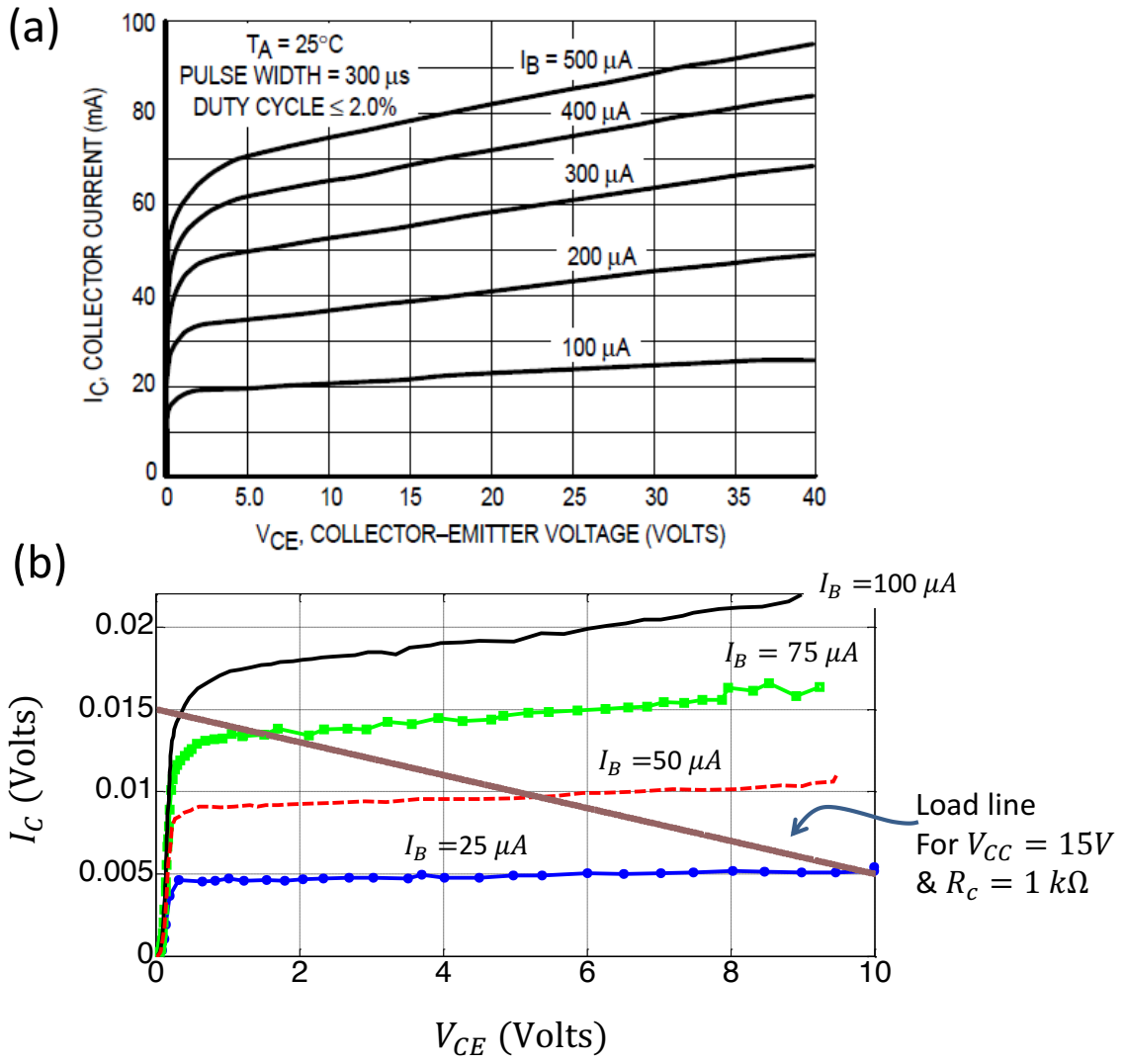


Figure 3: CE output characteristic curves as measured by (a) the manufacturer (Motorola) and (b) the instructor. In (b), the straight line with negative slope is the load line to illustrate proper biasing of the transistor for amplification in Activity 2.

discussion, while the CE configuration has output impedance somewhere in between the CB and CC, it is typically the most desirable of the three configurations for use as an amplifier. In Activity 2, you will design and build such a *common-emitter amplifier*. First, in this activity, you will develop some insight on how such an amplifier works.

To gain insight on how one could use a transistor in CE configuration as an amplifier, it is helpful to first look at the transistor's CE *output characteristic curves* (Fig. 3). Figure 3a displays such curves for the MPS3904 npn transistor ,which you are working with today.

For the CE configuration, the base terminal is used as the signal input and the collector terminal is used as the signal output. Thus, the output characteristics of the CE are generally illustrated by plotting a family of curves consisting of the collector current I_C versus collector-emitter voltage (V_{ce}) for different values of base current I_B. What is clear from such curves (like in Fig. 3a for

the MPS3904 in CE configuration) is that, for large enough V_{ce} (≳2V in Fig. 3a), small changes in the input current I_B produce large, proportional changes in the output current I_C (e.g. changes of ~ 100 μA in base current result in changes of ~20 mA in collector current. The transistor in this configuration and parameter regime is thus acting like a current amplifier (in Activity 2, you will learn how to properly wire up this configuration for use as a voltage amplifier).

The BJT parameter regime used for amplification, which we discussed in the previous paragraph, is known as the *forward-active regime.* It results from the base-emitter junction being forward biased and the base-collector junction being reversed biased; and it gives rise to the following relationship between I_C and I_B, which you read about in your latest reading assignment: $I_C = \beta I_B$, where $\beta \gg 1$ (β depends on v_{ce} as you can infer from Fig. 3; but typical values for the MPS3904 are on the order of β ~100-200). In Activity 1, you will perform measurements to map out the *forward-active regime* for the MPS3904 transistor given to you in lab today.

To perform measurements of the output characteristic curves of your transistor, please follow these guidelines:

1. Use the circuit configuration shown in Figure 2b for the common emitter.
2. To measure and record collector current I_C and collector-emitter voltage V_{ce}, use the LabVIEW VI that you developed in Laboratory 5 to measure diode IV characteristics. In order to do this, you will need to use one AI channel to read V_{ce} directly and one AI channel to measure the voltage across the collector resistor R_L in order to infer I_C. R_L should be chosen so that voltage drop is readily measurable but not so large that at modest I_B the collector voltage drops too close to zero and the base-collector junction becomes forward biased (this would put you in *saturation mode*). If this isn't obvious to you, don't worry… think about it.
3. For the base and collector bias voltages (V_{BB} and V_{CC}respectively), use the dual channel power supply that your work station has or the power supply on the PB-503b.
4. To provide the base current I_B, choose the base resistor R_S to be sufficiently large that V_{BB} and R_S look like a current source to the transistor's input (this will require $R_S \gg R_{in} \approx \beta r_e$, where R_{in} is the input resistance of the transistor looking into its base and r_e is known as the emitter resistance; to be safe, assume that r_e< 25 Ω for your measurements.
5. To take your data, fix I_B and then record I_C versus $V_{ce}$for different values of V_{CC}. Save a different spreadsheet file for each value of I_B. Note: Because of the limitations of the USB-6003 analog input channels' range, you will not be able to measure $V_{ce} > 10\ V$.
6. Be sure that you have correctly identified the collector, emitter and base terminals of your transistor before you put the transistor in the circuit and start turning on voltages. See the technical data sheet that I handed out to identify terminals.

****For your lab report: Please include the values of the resistors that you used for the measurements in this activity and a discussion of why you chose those values. Also, please provide a graph like that in Fig. 3b illustrating the characteristics curves of your transistor (Do not worry about including the load line).**

Activity 2: Designing and Building a Common-Emitter Amplifier

To understand how the CE configuration can be used to amplify a signal, it is helpful to take a look back at Fig. 3b. (By now, you should have constructed similar curves from the data you took in Activity 1.) In addition to displaying the characteristic output curves for MPS3904, the graph also shows a plot of the *load line* for the collector-emitter loop of the CE circuit shown in Fig. 2b. A load line is a current-vs-voltage plot for a circuit element as derived by applying Kirchoff's laws to the branch of the circuit that the element of interest resides in. (You can find more on load lines in Horowitz & Hill, Appendix F, p650.) As an example, the load-line in Fig. 3b reflects the dependence of collector current on current-emitter voltage; it is given mathematically by $I_C = (V_{CC} - V_{CE})/R_L$, where I have used the values $V_{CC} = 15\ V$ and $R_L = 1000\ \Omega$ (Why I chose these values should be come clear when you build your amplifier in a few moments). *Note: If it is not apparent where the expression for the load line derives from, please take some to understand it before proceeding with this activity.

Now, the intersections of the load line curve with the family of I_C vs. V_{CE} curves in Fig. 3b tell us the operating points of the transistor (known as the *quiescent* points) for the circuit parameters $V_{CC} = 15\ V$ and $R_L = 1000\ \Omega$ and for different I_B. Thus, if you apply $I_B = 50\ \mu A$ to the base, you will find that $I_C \sim 10\ mA$ and $V_{CE} \sim 5V$. Alternatively, for $I_B = 75\ \mu A$, you will find $I_C \sim 13\ mA$ and $V_{CE} \sim 1V$. Etc. Imagine then that you apply a sinusoidal current to the base that takes the form: $I_B = 50\ \mu A + (25\mu A)\sin\omega t$. At the output of the transistor (between the collector and emitter terminals), you would observe that $V_{CE} = 5V - (4V)\sin\omega t$! You would be converting a modest size current signal into a fairly large voltage signal. In essence you would have created an amplifier (an inverting transimpedance amplifier to be exact).

There's an important point to make here about the choice of DC bias point in the previous paragraph. By choosing $I_B = 50\ \mu A + (25\mu A)\sin\omega t$, you are selecting an operating point of the transistor where V_{CE} follows I_B linearly. Alternatively, if you had instead chosen the base current DC bias to be $75\ \mu A$ so that $I_B = 75\ \mu A + (25\mu A)\sin\omega t$, then it's clear from Fig. 3b that you would not observe V_{CE} to change linearly with I_B: V_{CE} would oscillate about 1V, but it would oscillate between ~0.5 V and ~5V, which is clearly not symmetric about the quiescent point. As a more extreme example, imagine adjusting the base current bias point to be $25\ \mu A$ and applying a base current modulation of $50\ \mu A$ so that $I_B = 25\ \mu A + (50\mu A)\sin\omega t$. In this case, for positive halves of the current cycle, V_{CE} would decrease linearly with I_B, but for negative halves of the input current cycle, the transistor would enter the *cut-off* regime, where the collector current goes to zero (i.e. $I_C \sim 0$) and the collector-emitter voltage reaches a maximum at $V_{CE} = V_{CC}$; in essence, for this bias point, your signal would be clipped during the negative half cycle.

The proceeding discussion was meant to illustrate the importance of knowing and understanding the characteristic curves of your transistor. **The bottom line is this**: knowing the characteristic curves of your transistor and the magnitude of your input signal will enable you to determine an operating point (aka bias point) that safely allows for linear amplification of your signal.

The next question is: How do we turn the CE configuration into a *voltage amplifier*? Short answer: Use the circuit in Fig. 4. I will not work through the analysis of the voltage gain of this circuit here as it was covered in your most recent reading assignment. (Of course, though, I would be happy to go over it in class if you have questions about its operation.) **Nonetheless, I would like you to use the characteristic curves you measured in Activity 1 and engineer the circuit in Fig. 4 to build a CE voltage amplifier with the following characteristics:**

1. 1 $k\Omega$ output impedance.
2. Voltage gain $= 5$.
3. Powered by a voltage source in the range of 12-20 V.

Some other things that I would like to note:

- Be careful about your choice of input and output capacitors C_1 and C_2 (as labeled in Fig. 4); these will determine the low frequency cut-off of your amplifier (I have left it up to you to determine the frequency at which you would like to operate your amplifier.
- In Fig. 4, the resistors R_1 and R_2 are used to establish the appropriate biasing of the base for linear operation of the transistor. Be careful, however, to make sure that their parallel resistance is less than the input impedance of the transistor (as discussed in the reading assignment). If this point isn't clear, please talk to me.
- Use the oscilloscope VI you created in Lab 5 to record both the signal input to your amplifier and the signal output from your amplifier in order to measure the gain.
- Use your function generator to provide the input signal Δv_B and the TTL signal for the VI's trigger.
- Once you have your amplifier working, explore a range of input signal voltages and frequencies, and try to understand what limits the amplifier's working range. (For example, as you turn up the amplitude of the input signal, does the gain remain constant? If not, why might that be? What happens as you turn up the frequency of the input signal? Does the gain appear constant? If not, why might that be? Etc.)

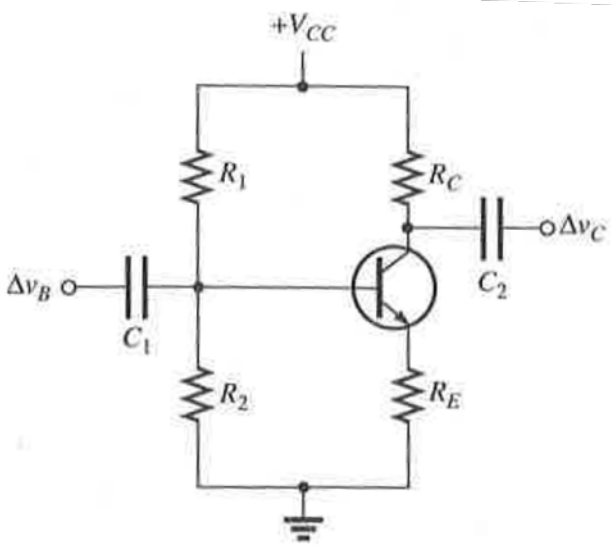


Figure 4: From Diefenderfer, Figure 8.8. The capacitively-coupled, resistor-biased common-emitter amplifier, which you are to build and characterize in Activity 2. Use your digital oscilloscope VI to record Δv_B and Δv_C and analyze the circuit as you make changes to circuit parameter values and input parameter values.

For Your Lab Report

1. Include a screen shot of the front panel of your oscilloscope VI illustrating the gain of 5 achieved by your CE amplifier.
2. Be sure to discuss all the circuit parameter values you chose to realize your CE amplifier. Discuss reasons for using those parameters; talk about parameters that didn't work.
3. Discuss your observations and thoughts on the operating range of your amplifier.
4. Optional. If you have time, try building a CE with a much higher gain. Say, gain=100. Can you get it to work? If not, what do you think could be limiting your design? If so, provide the parameter values.

Activity 3 – Impedance Engineering with the Common-Collector (a.k.a. the Emitter Follower)

Imagine that you have a 9 Volt battery and two 1 $k\Omega$ resistors, and you need to apply 3.8 V across 100 Ω load. Could you do it using the voltage divider circuit in Fig. 5a? Hopefully, you answered "no" (**For your lab report, please include this calculation**). One way to understand this situation is to think about the Thevenin equivalent circuit for the 9 V battery and voltage divider, Fig. 5b (**For your lab report, please work out this equivalent circuit**). From this equivalent circuit, it is clear that the 100 Ω load sees an effective voltage source of 4.5 V with an output impedance of 500 Ω. Such a voltage source could put out a maximum current of 9 mA; yet, the 100 Ω needs 38 mA in order to maintain 3.8 V across it. Thus the voltage source is incapable of functioning as a true voltage source, and the voltage across the load lags (you would find it to be 0.75 V in this case).

What we discussed in the preceding paragraph is known as "loading of the source" and occurs whenever the source impedance is comparable to or larger than impedance of the load (equivalently, whenever the load needs to draw more current than the source can supply in order to maintain the source's potential difference across its terminals). One nice way to rectify this problem is to use the common-collector configuration, or, as it's more widely known, the *emitter follower* (Fig. 2b & Fig. 5c).

As you learned in your latest reading assignment, the change in output voltage (ΔV_E) of an ideal emitter follower is equal to the change in input voltage (ΔV_B). So the transistor in this configuration acts like a unity gain amplifier. Its real utility, though, is its super-low output impedance, which, as your book showed, is generically given by $R_{out} = R_S/\beta$, where R_S is the resistance of the source supplying the base and β is the transistor's current gain. Note, before proceeding, make sure you understand where this relationship derives from.

As a result of these characteristics, the emitter follower is frequently used as a unity-gain voltage buffer; that is, it can be used to follow a poor voltage source (i.e. one with relatively large output impedance) and supply the current necessary to maintain a constant voltage across a lower impedance load. In essence, the emitter follower is used to amplify the current output by the source while maintaining the source's potential difference. You will now implement the emitter follower to solve the problem we started this activity by discussing.

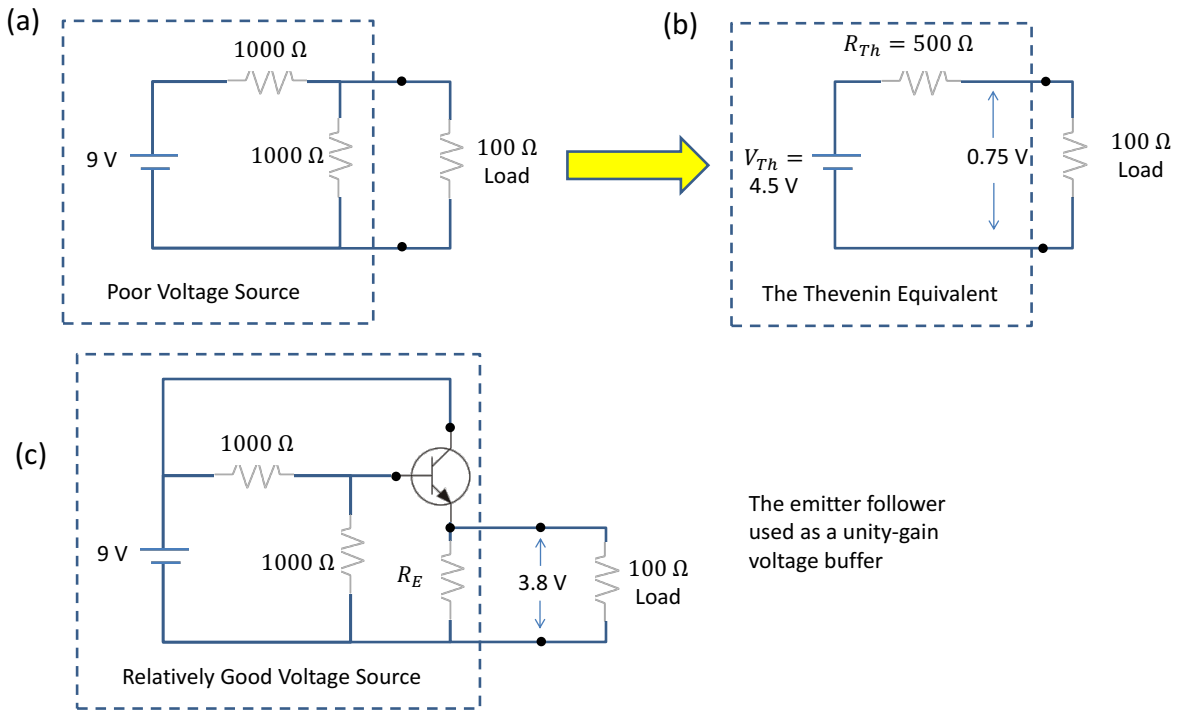


Figure 5: (a-b) Example of a situation when a voltage-divider circuit acts as a poor voltage source; that is, when the Thevenin equivalent impedance (or output impedance) of the voltage divider is comparable to or greater than the load resistance. (c) The situation can be rectified by using an emitter follower to boost the amount of current to the load to maintain the desired potential difference (in this case, the buffered source provides 3.8V) and effectively low output impedance.

Before implementing the emitter follower circuit in Fig. 5c, I would like you first to perform a measurement of the Thevenin impedance (or output impedance) of the voltage divider circuit in Fig. 5a. A simple way to do this is as follows:

1. First, remove the 100 Ω and measure the *open circuit output voltage* of the divider. Record this value.
2. Second, insert a variable resistor in the circuit at the former location of the 100 Ω load. (You could for instance use the potentiometer on the PB-503.)
3. Then, start decreasing the value of the variable resistor until you see the circuit's output voltage decrease to ½ the open circuit voltage. Record this value of the variable resistance; it is the output resistance of your voltage divider circuit. **For your lab report, be sure to show why this is true.**

Next, implement the emitter follower circuit of Fig. 5c. Choose the emitter resistor R_E so that $I_C \sim 10\ mA$ without the 100 Ω load in place. (This will ensure that the emitter's intrinsic resistance r_e does not limit the follower's output impedance; if you are interested, I can explain this in more detail in the class.) And be sure to do the following:

1. Demonstrate that you can supply 3.8 V across the 100 Ω load.

2. Measure the output impedance of the follower using the same technique that you used to measure the output impedance of the voltage divider.

****For your Lab Report:**

1. Show that you cannot use the circuit of Fig. 5a to supply 3.8V to the 100 Ω load.
2. Provide a calculation to justify your output impedance measurement technique (for the case of the voltage divider).
3. Provide the value you measured for the output impedance of the voltage divider in Fig. 5a.
4. Using the MSP3904 data sheet estimate the output impedance of emitter follower in Fig. 5c.
5. Provide the value you measured for the output impedance and discuss how it agrees with/or not the value you estimated in (5).

Activity 4 – The BJT Switch and a Transistor-Transistor NOR Gate

In this activity, you will learn about the *saturation* and *cut-off* modes of the BJT transistor and see how they could be used for operation of the transistor as a switch and for implementation of a basic logic gate.

Figure 6a displays an npn BJT in CE configuration with bias conditions adjusted so that the transistor could readily be used as a switch. To understand how this might work, it's helpful to first take a look at Fig. 6b, which displays a graph of the output characteristic curves measured for the MPS3904. This is the same graph as in Fig. 3b, except the load line is now drawn for the circuit of Fig. 6a. What should be apparent to you from studying the load line is that there is a very small range of parameter space for which the circuit could be operated as a linear amplifier. For example, if $V_{in} \lesssim 0.5\,V$, the base-emitter junction will be reversed biased, and thus $I_B \sim 0$ and hence $I_C \sim 0$. This is known as the *cut-off* regime (both the BE and BC junctions are reversed biased and no current flows). For this case, you should convince yourself that $V_{out} = 5V$ (note the change in terminology here; V_{out} is equivalent to V_{CE}, which I used before). On the other hand, if $V_{in} \gtrsim 0.8\,V$, then $I_B \gtrsim 100\,\mu A$. For this situation, you would expect that $I_C = \beta I_B \gtrsim 100\,mA$. But inspection of the circuit in Fig. 6a shows that this would require > 100 V drop across the collector resistor! Such a voltage, given the source, is clearly not possible. What would happen instead is that the transistor would continue to increase I_C until $V_{CE} \sim 0.5\,V$, around which point β would start to decrease significantly. As one increases V_{in} further, V_{CE} drops toward zero, the BC junction becomes fully forward biased, and I_C is no longer a function of I_B. This is known as *saturation*. At this point, you should convince yourself that $V_{CE} \sim 0.2\,V$ at most. Once you have done so, proceed with verifying this *switching* behavior using your transistor. Record the values of V_{in} for which saturation and cut-off occur. Also record the values of V_{out} for the corresponding regimes of operations.

Now, you can utilize this switching behavior to implement basic logic gates. One such *transistor-transistor* logic gate is shown in Fig. 7.

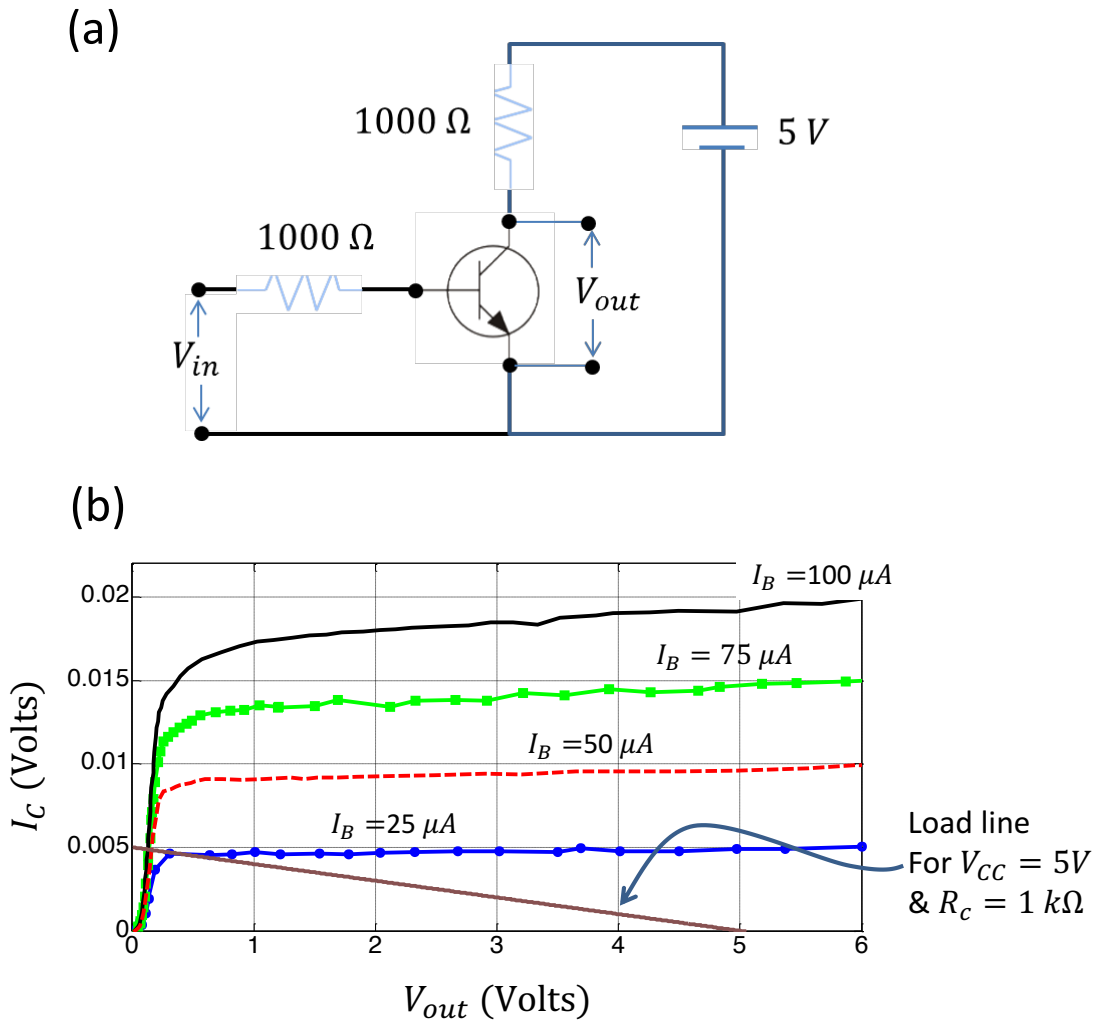


Figure 6: (a) One possible bias configuration for an NPN transistor to implement a transistor switch. (b) From the load line for the circuit in (a), it is clear that for $I_B \gtrsim 25\ \mu A$, the transistor *saturates* and $V_{out} \sim 0\ V$. On the other hand, if $I_B \sim 0\ \mu A$, then $V_{out} \sim 5\ V$, and the transistor is *cut-off.*

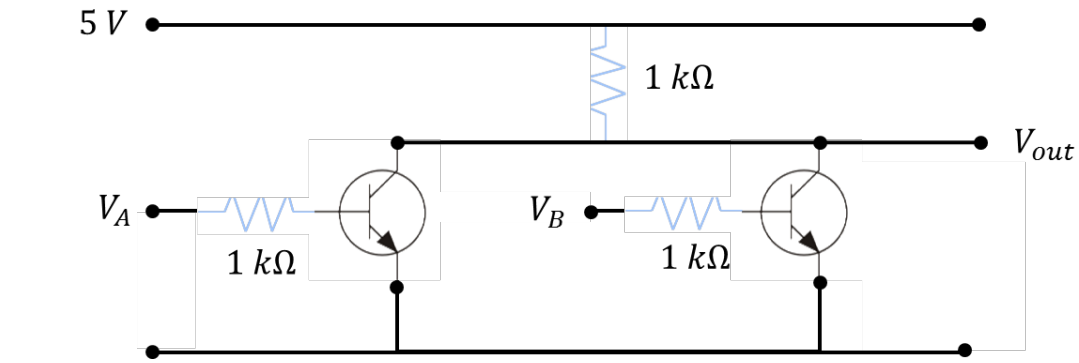
For the circuit shown in Fig. 7a, if we call a "1" any voltage in excess of 0.8 V, and we call a "0" any voltage less than say 0.4 V, then this circuit functions exactly as a *NOR gate.* The truth table for the logic gate is shown in Fig. 7b. For the last activity of this lab, construct the circuit from Fig. 7a, and then verify that it functions as a *NOR gate* for the appropriate designation of *0s* and *1s.* You should use the logic switches on the PB503 board in order to provide the appropriate input signals; and use the logic indicators on the PB503 to indicate logical *0's* and *1's.*

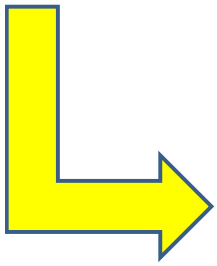
**** For Your Lab Report**

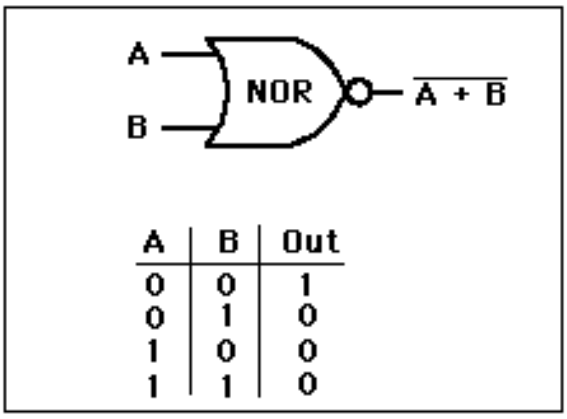
1. Provide the values of V_{in} and V_{out} for saturation and cut-off that you measured. Also provide a plot of I_C vs V_{out} with a load line analysis for the circuit of figure 6a. (For the I_C family of curves, you can just use your data from Activity 1. But you do need to

include a load line in order to discuss whether your observations of V_{in} and V_{out} make sense.

2. Provide a discussion of the transistor-transistor *NOR gate* that you implemented. Were you able to construct the truth table that you expect? What values did you designate for *0's* and *1's*.







A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Figure 7: (Top) Transistor-transistor NOR gate that you are to construct in Activity 4. (Bottom) You should find that the inputs and output follow the dependence shown in the truth table (provided you make the appropriate designation for logical *0*'s and *1*'s).