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PLC S7-300, CPU Specifications CPU 312 IFM to CPU 318-2 DP

Reference Manual

This documentation can **no longer** be ordered under the given number!

This manual is part of the documentation package with the order number
6ES7398-8FA10-8BA0

Edition 10/2001
A5E00111190-01

Safety Guidelines

This manual contains notices intended to ensure personal safety, as well as to protect the products and connected equipment against damage. These notices are highlighted by the symbols shown below and graded according to severity by the following texts:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution

indicates that minor personal injury can result if proper precautions are not taken.

Caution

indicates that property damage can result if proper precautions are not taken.

Notice

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Qualified Personnel

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

Preface

Purpose of the Manual

This manual gives you a brief overview of 312 IFM to 318-2 CPUS in an S7-300. You can look up information on how to operate the system, its functions and technical data of the CPUs.

Essential know-how

General knowledge of automation technology is required for comprehension of this Manual. You should also be acquainted with basic *STEP 7* software as described in your *Programming with STEP 7 V 5.1* Manual.

Scope of the Manual

The manual covers the following CPUs and Hardware/Software versions:

CPU	Order No.	As of Version	
		Firmware	Hardware
CPU 312 IFM	6ES7 312-5AC02-0AB0 6ES7 312-5AC82-0AB0	1.1.0	01
CPU 313	6ES7 313-1AD03-0AB0	1.1.0	01
CPU 314	6ES7 314-1AE04-0AB0 6ES7 314-1AE84-0AB0	1.1.0	01
CPU 314 IFM	6ES7 314-5AE03-0AB0 6ES7 314-5AE83-0AB0	1.1.0	01
CPU 314 IFM	6ES7 314-5AE10-0AB0	1.1.0	01
CPU 315	6ES7 315-1AF03-0AB0	1.1.0	01
CPU 315-2 DP	6ES7 315-2AF03-0AB0 6ES7 315-2AF83-0AB0	1.1.0	01
CPU 316-2 DP	6ES7 316-2AG00-0AB0	1.1.0	01
CPU 318-2	6ES7 318-2AJ00-0AB0	V3.0.0	03

This manual describes all modules that are valid at the time the manual is released. We reserve the right to release product information for new modules or new module versions.

Alterations from Previous Version

The following changes were made in the *Structuring, CPU Data* Manual, Order no. 6ES7398-8AA03-8BA0, Edition 2:

- Now, this manual only contains the CPU description. For information on the S7-300 structure and installation refer to the *Installation Manual*.
- CPU 318-2 DP as of Firmware Version V3.0.0 behaves as DP Master according to PROFIBUS DPV1.

Agreement for CPU 314IFM

The CPU 314IFM is available in 2 versions:

- with slot for Memory Card (6ES7314-5EA**10**-0AB0)
- without slot for Memory Card (6ES7314-5EA**0x**-0AB0)

All details in this chapter apply to both versions of CPU 314IFM, unless explicit reference is made to differences between them.

Approbation, Standards and Approvals

The SIMATIC S7-300 series conforms to:

- Requirements and criteria to IEC 61131, Part 2
- CE labeling
  - EC Guideline 73/23/EEC on Low Voltages
  - EC Guideline 89/336/EEC on electromagnetic compatibility (EMC)
- Canadian Standards Association: CSA C22.2 Number 142, tested (Process Control Equipment)
- Underwriters Laboratories, Inc.: UL 508 registered (Industrial Control Equipment)
- Underwriters Laboratories, Inc.: UL 508 (Industrial Control Equipment)
- Factory Mutual Research: Approval Standard Class Number 3611
- C-Tick Australia

Integration in the Information Technology Environment

This Manual forms part of the S7-300 documentation package:

Reference Manual “CPU Data” → CPU Data of CPU 312 IFM to 318-2 DP CPU Data of CPU 312C to 314C-2 PtP/DP	Description on how to operate, of the functions and of technical data of the CPU
“Technological Functions” Manual Manual Samples	Description of specific technological functions: • Positioning • Counting • Point-to-point connection • Rules The CD contains examples of technological functions
Installation Manual Manual	Description of how to create a project and how to install, wire, network and commission an S7-300
Reference Manual “Module Data” Manual	Description and technological details of signal modules, power supply modules and interface modules
Operations List “CPU 312 IFM, 314 IFM, 313, 315, 315-2 DP, 316-2 DP, 318-2 DP” “CPUs 312C to 314C-2 PtP/DP	List of the CPU’s system resources and their execution times. Listing of all runtime function blocks (OBs/SFCs/SFBs) and their execution times
Getting Started “CPU 31xC:Positioning with Analog Output” “CPU 31xC: Positioning with Digital Outputs” “CPU 31xC: Counting” “CPU 31xC: Point-to-point Communication “CPU 31xC: Controlling” “CPU 31xC: “S7-300”	the various Getting Started manuals offer help for commissioning your applications

You are reading this manual

Figure 1-1 S7-300, information technology environment

Complementary to this documentation package you require the following manuals:

Manual **“Integrated Functions CPU 312 IFM/314 IFM”**  Manual Order no.: 6ES7398-8CA00-8BA0	Description of technological functions of the CPUs 312 IFM/314 IFM.
Reference Manual “System Software for S7-300/400 System and Standard Functions”  Reference manual Part of the STEP 7 documentation package, order no. 6ES7810-4CA05-8BR0	Description of the SFCs, SFBs and OBs of the CPUs. This description is also available in the STEP 7 Online Help.

Figure 1-2 Additional Documentation

Further Support

Please contact your local Siemens representative if you have any queries about the products described in this manual.

http://www.ad.siemens.de/partner

Training Center

Newcomers to SIMATIC S7 PLCs are welcome to take part in our respective training courses. Please contact your local Training Center, or the central Training Center in D-90327 Nuremberg, Germany:

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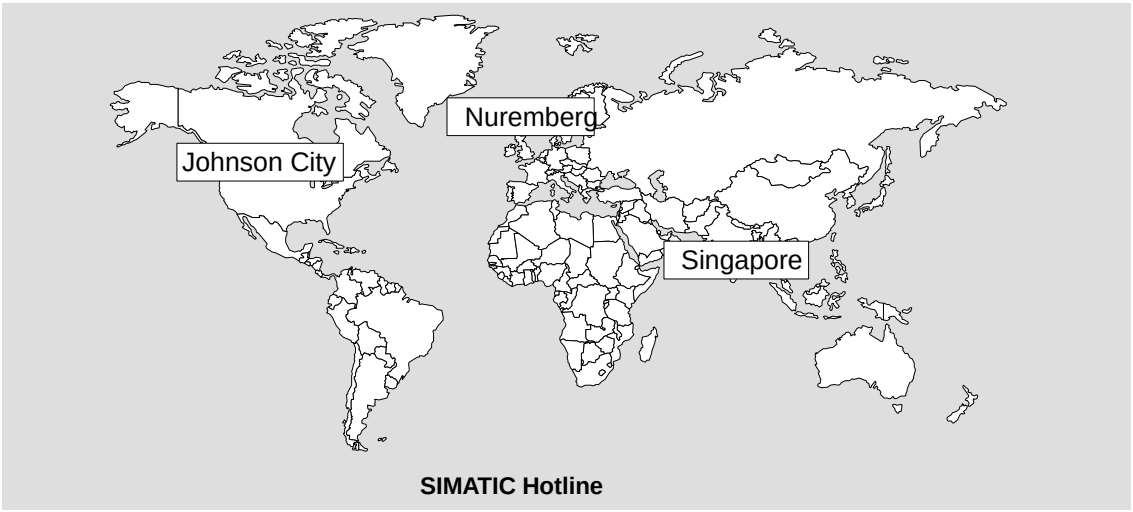

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- The Knowledge Manager finds the right documents for you.
- Users and specialists across the globe share their experiences in our Forum.
- Your local service partner for Automation & Drives is found in our Service Partner Database.
- Information relating to on–site Service, repairs, spare parts and lots more is available to you under the topic “Service”.

Contents

Figures

Tables

CPUs

1

In This Section

Agreement for CPU 314IFM

The CPU 314IFM is available in 2 versions:

- with slot for memory card (6ES7314-5EA**10**-0AB0)
- without slot for memory card (6ES7314-5EA**0x**-0AB0/ 6314ES7314-5EA**8x**-0AB0)

All details in this chapter apply to both versions of the CPU314IFM unless explicit reference is made to differences between them.

1.1 Control and Display Elements

Figure 1-1 shows you the control and display elements of a CPU.
The order of the elements in some CPUs might differ from the order shown in the figure below. The individual CPUs do not always have all the elements shown here. Table 1-1 shows you the differences.

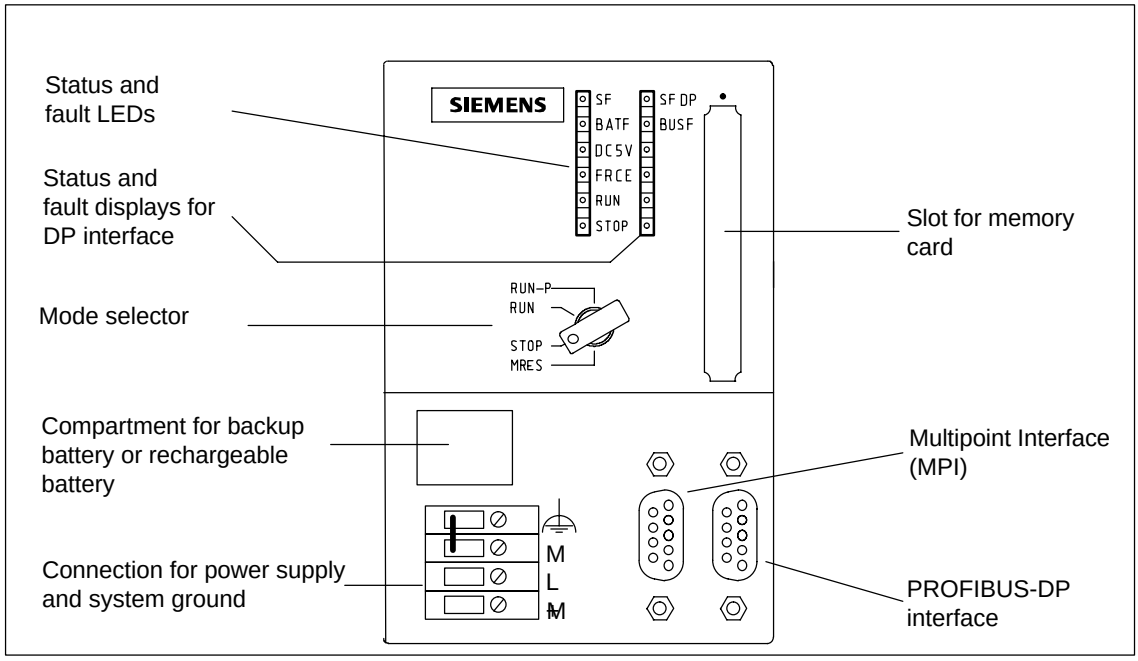


Figure 1-1 Control and Display Elements of the CPUs

Differences Between CPUs

Table 1-1 The Differences in Control and Display Elements Between CPUs

Element	312 IFM	313	314	314 IFM		315	315-2 DP	316-2 DP	318-2
				-5AE0x-	-5AE10-				
LEDs for DP interface	No						Yes		
Backup battery/accumulator	No	No accumulator	Yes						
Connection for power supply	No; via the front connector	Yes							
Memory card	No	Yes		No	Yes	Yes			
PROFIBUS-DP interface	No						Yes		

1.1.1 Status and Fault Displays

Displays for the CPU:

SF ... (red) ...hardware/software error
BATF ... (red) ...battery error (not CPU 312 IFM)
DC5V ... (green) ... 5V DC supply for CPU and S7-300 bus is ok.
FRCE ... (yellow) ...force job is active
RUN ... (green) ... CPU in RUN mode; LED flashes at start-up with 1 Hz; in HALT mode with 0.5 Hz
STOP ... (yellow) ... CPU in STOP/HALT or STARTUP mode;
LED flashes on request to reset memory

Displays for the PROFIBUS:

CPU 315-2 DP/
CPU 316-2 DP

BUSF ... (red) ... hardware or software fault at PROFIBUS interface

CPU 318-2

BUS1F ... (red) ... hardware or software fault at interface 1
BUS2F ... (red) ... hardware or software fault at interface 2

Figure 1-2 Status and Fault Displays of the CPUs

1.1.2 Mode Selector Switch

The mode selector is the same in all CPUs.

Mode Selector Positions

The positions of the mode selector are explained in the order in which they appear on the CPU.

Details on CPU operating modes are found in the *STEP 7* Online Help .

Position	Description	Description
RUN-P	RUN-PROGRAM mode	The CPU scans the user program. The key cannot be taken out in this position.
RUN mode	RUN mode	The CPU scans the user program. The user program cannot be changed without password confirmation. The key can be removed in this position to prevent anyone not authorized to do so from changing the operating mode.
Stop mode	Stop mode	The CPU does not scan user programs. The key can be removed in this position to prevent anyone not authorized to do so from changing the operating mode.
MRES mode	Memory reset	Momentary-contact position of the mode selector for CPU memory reset (or a cold start as well in the case of the 318-2). Memory reset per mode selector switch requires a specific sequence of operation.

1.1.3 Backup battery/accumulator

Exceptions

The CPUs 312IFM and 313 do not have a real time clock so they do not need an accumulator battery.
The CPU 312IFM does not have a buffer which means that you can not insert a battery.

Backup battery or rechargeable battery?

Table 1-2 shows the differences in the backup provided by an accumulator and a backup battery.

Table 1-2 Using a Backup Battery or Accumulator

Backup with...	... Backs up	Remarks	Backup Time
Rechargeable battery	Real-time clock only	The rechargeable battery is charged after CPU POWER ON. **Note** You must create a backup of the user program either on Memory Card or, in the case of CPU314IFM 314 (-5AE**0x**-), on EPROM.	120 h (at 25°C) 60 h (at 60°C) ... after 1 hour of recharging
Backup battery	• User program (if not stored on memory card and protected against loss on power failure) • More data areas in data blocks are to be retained than possible without battery • The real-time clock	**Note** The >CPU can retain part of the data without backup battery. You only need a backup battery if you want to retain more data than this.	1 year

1.1.4 Memory card

Exceptions

You cannot insert a memory card with the CPUs 312 IFM and 314 IFM (-5AE**0x**). These CPUs have an integrated read-only memory.

Purpose of the Memory Card

With the memory card, you can expand the load memory of your CPU.

You can store the user program and the parameters that set the responses of the CPU and modules on the memory card.

You can also back up your CPU operating system to a Memory Card. except CPU 318-2.

If you store the user program on the memory card, it will remain in the CPU when the power is off even without a backup battery.

Available Memory Cards

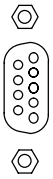
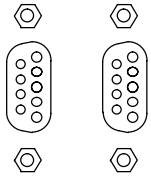
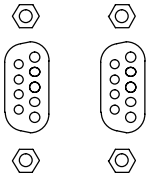
The following memory cards are available:

Table 1-3 Memory Cards

Capacity	Type	Remarks
16 KB	5 V FEPROM	The CPU supports the following functions: • Loading of the user program on the module into the CPU With this function, the memory of the CPU is reset, the user program is downloaded onto the memory card, and then uploaded from the memory card to the CPU's RAM. • Copying RAM data to ROM (not with CPU318-3182)
32 KB		
64 KB		
256 KB		
128 KB		
512 KB		
1 MB		
2 MB		
4 MB		
128 KB	5 V RAM	Only with the CPU 318-2
256 KB		
512 KB		
1 MB		
2 MB		

1.1.5 MPI and PROFIBUS-DP Interface

Table 1-4 CPU Interfaces

CPU 312 IFM CPU 313 CPU 314IFM CPU 314	**CPU 315-2DP CPU 316-2DP**		**CPU 318-2**	
MPI interface	MPI interface	PROFIBUS-DP interface	MPI/DP Interface	PROFIBUS-DP interface
 MPI	 MPI DP		 MPI/ DP DP	
-	-	-	Reconfiguration as a PROFIBUS-DP interface is possible	-

MPI interface

The MPI is the interface of the CPU for the programming device/OP and for communication in an MPI subnet.

Typical (default) transmission speed is 187.5 Kbps (CPU 318-2: adjustable up to 12 Mbps).

Communication with an S7-200 requires 19.2 Kbps.

The CPU automatically broadcasts its set bus parameters (e.g. baud rate) at the MPI interface. This means that a programming device, for example, can automatically ”hook up” to an MPI subnet.

PROFIBUS-DP Interface

CPUs equipped with 2 interfaces provide a PROFIBUS-DP interface connection. Transmission rates up to 12 Mbps are possible.

The CPU automatically broadcasts its set bus parameters (e.g. baud rate) at the PROFIBUS-DP interface. This means that a programming device, for example, can automatically ”hook up” to a PROFIBUS subnet.

In Step 7 you can switch off automatic transfer of bus parameter.

Connectable Devices

MPI	PROFIBUS-DP
• Programming device/PC and OP • S7 programmable controller with MPI interface (S7-300, M7-300, S7-400, M7-400, C7-6xx) • S7-200 (**Note:** 19.2 Kbps only)	• Programming device/PC and OP • S7 programmable controllers with the PROFIBUS-DP interface (S7-200, S7-300, M7-300, S7-400, M7-400, C7-6xx) • Other DP masters and DP slaves

Only 19.2 Kbps for S7-200 in MPI Subnet

Note

At 19.2 Kbps for communicating with S7-200,

- a **maximum of 8 nodes** (CPU, PD/OP, FM/CP with own MPI address) is permitted in a subnet, and
- **no global data communication** can be carried out.

Please consult the *S7200 Manual* for further information!

Removing and Inserting Modules in the MPI Subnet

You must not plug in or remove any modules (SM, FM, CP) of an S7-300 configuration while data is being transmitted over the MPI.

Warning

If you remove or plug in S7-300 modules (SM, FM, CP) during data transmission via the MPI, the data might be corrupted by disturbing pulses.

You must not plug in or remove modules (SM, FM, CP) of an S7-300 configuration during data transmission via the MPI!

Loss of GD packets Following Change in the MPI Subnet During Operation

Warning

Loss of data packets in the MPI subnet:

Connecting an additional CPU to the MPI subnet during operation can lead to loss of GD packets and to an increase in cycle time.

Remedy:

1. Disconnect the node to be connected from the supply.
2. Connect the node to the MPI subnet.
3. Switch the node on.

1.1.6 Clock and Runtime Meter

Table 1-5 shows the characteristics and functions of the clock for the various CPUs.

When you assign parameters to the CPU in *STEP 7*, you can also set functions such as synchronization and the correction factor(see the *STEP 7* online help system).

Table 1-5 Characteristics of the Clock of the CPUs

Characteristics	312 IFM	313	314	314 IFM	315	315-2 DP	316-2DP	318-2
Type	Software clock		Hardware clock (integrated “real-time clock”)					
Manufacturer setting	DT#1994-01-01-00:00:00							
Backup	Not possible		• Backup battery • Accumulator					
Operating hours counter	-	1						8
Number		0						0 to 7
Value range		0 to 32767 hours						0 to 32767 hours
Accuracy • with switched on power supply 0 to 60° C • with switched off power supply 0°C 25°C 40°C 60°C	... max. deviation per day: ± ±9s +2s to -5s ± ±2s +2s to -3s +2s to -7s							

Behavior of Clock in POWER OFF Mode

The following table shows the clock behavior with the power of the CPU off, depending on the backup:

Backup	CPU 314 to 318-2	CPU 312 IFM and 313
With backup battery	The clock continues to operate in power off mode.	At POWER ON, the clock continues to operate using the clock time at which POWER OFF took place. Since the clock does not have a power buffer, it does not continue to run in POWER OFF mode.
With accumulator	The clock continues to operate in power off mode for the backup time of the accumulator. When the power is on, the accumulator is recharged.	
	In the event of backup failure, an error message is **not** generated. When the power comes on again, the clock continues at the clock time at which the power went off.	
None	At POWER ON, the clock continues to operate using the clock time at which POWER OFF took place. Since the CPU is not backed up, the clock does not continue at POWER OFF.	

1.2 Communication Options of the CPU

The CPUs offer you the following communication options:

Table 1-6 CPU Communication Options

Communications	MPI	DP	Description
PG/OP Communication	x	x	A CPU can maintain several on-line connections simultaneously with one or more programming devices or operator panels. For PD/OP communication via the DP interface, you must activate the “Programming, modifying and monitoring via the PROFIBUS” function when configuring and assigning parameters to the CPU.
S7 Basic Communication	x	x	Using the I system functions, you can transfer data over the MPI/DP network within an S7-300 (acknowledged data exchange). Data exchange takes place via non-configured S7 connections.
	x	-	Using the XI system functions, you can transfer data to other communication peers in the MPI subnet (acknowledged data exchange). Data exchange takes place via non-configured S7 connections.
			A listing of I/X SFCs is found in the *Instruction List*. Details are found in the *STEP 7* Online Help or in the *System and Standard Functions* reference manual.
Routing of PG Functions	x	x	With CPUs 31x-2 and *STEP 7* as of V 5/0, you can route your PG/PC to S7 stations of other subnets, e.g. for downloading user programs or hardware configurations, or executing, testing and commissioning functions. Routing with the DP interface requires you to activate the “Programming, Status/Control...” function when configuring and assigning parameters to the CPU. Details on routing are found in the *STEP 7*-Online Help.
S7 Communication	x	-	S7 communication takes place via configured S7 connections. Here, the S7-300-CPUs are servers for S7-400 CPUs. That is, S7-400 CPUs have read/write access to S7-300 CPUs.
Global Data Communication	x	-	The CPUs of the S7-300/400 can exchange global data with one another (unacknowledged data exchange).

Connection Resources

Every communication connection requires a communication resource on the S7 CPU as a management unit for the duration of the communication. Every S7 CPU has a certain number of connection resources available to it according to its technical specifications which can be assigned to various communication services (PD/OP communication, S7 communication or S7 basic communication).

The distribution of connection resources differs between CPUs 312 IFM to 316-2 DP (see the table 3-6) and the CPU 318-2 (see Table 1-8):

Connection Resources for CPUs 312IFM to 316-2 DP

Communication resources are independent of the interface in CPUs 315-2 DP and 316-2 DP. That is, a PG communication occupies a connection resource, regardless of whether the connection was established via MPI or DP interface.

Table 1-7 Connection Resources for CPUs 312 IFM to 316-2 DP

Communication Function	Description
PD communication/ OP communication S7 basic communication	In order to make the allocation of connection resources dependent not only on the chronological sequence in which various communication services are registered, connection resources can be reserved for the following services: • PD communication and OP communication • S7 basic communication For PD/OP communication, at least one connection resource is reserved as the default setting. Lower values are not possible. The technical specifications of the CPUs detail the possible connection resources settings and the default settings in each case. In *STEP 7* you specify a ”redistribution” of communication resources when you configure the CPU.
S7 communication	Other communication services such as S7 communication using PUT/GET functions can not use these communication resources even if they establish their connection at an earlier time. Instead, the remaining available connection resources that have not been specifically reserved for a particular service are used. Example based on CPU 314 which has 12 connection resources available: - You reserve 2 connection resources for PD communication - You reserve 6 connection resources for OP communication - You reserve 1 connection resource for S7 basic communication → In this case, you still have three communication resources available for S7 communication, PG/OP communication and S7 basic communication. **Note** on OP Communication Resources: When using more than three OPs, error messages might occur due to temporary lack of resources in the CPU. Examples of such error messages are “44 Transmission error #13” or “#368 S7 communication error class 131 No. 4”. Remedy: Acknowledge error messages manually or after a time delay configured in PROTOOL (in “System Messages” →→ “Display time”).
Routing of PG functions (CPU 31x-2 DP)	The CPUs provide connection resources for four routed connections. Those connection resources are available in addition.
Communication via a CP 343-1 with data lengths >240 bytes for Send/Receive	The CP requires a free connection resource that is not reserved for PD/OP/S7 basic communication.

Connection Resources for CPU 318-2

Table 1-8 Communication Resources for CPU 318-2

Communication Function	Description
PD/OP communication	The CPU 318-2 provides a total of 32 connection resources (with CPU as connection terminal point) for these communication functions. Those 32 connection resources can be freely allocated to the various communication functions. When allocating connection resources, you should observe the following points: • The number of connection resources differs for each interface as follows: – MPI/DP Interface 32 communication resources – DP-SS: 16 communication resources • In the case of connections that do not have the CPU as their terminal point (e.g. an FM or in the case of routing) you must deduct 2 connection resources from the total resources and 1 connection resource per interface. Figure 1-3 shows the principle of allocation of connection resources. An example of how connection resources are dimensioned is found in Chapter LEERER MERKER.
S7 basic communication	
Routing of PD functions	
S7 communication	

Principle of Connection Resource Allocation for CPU 318-2

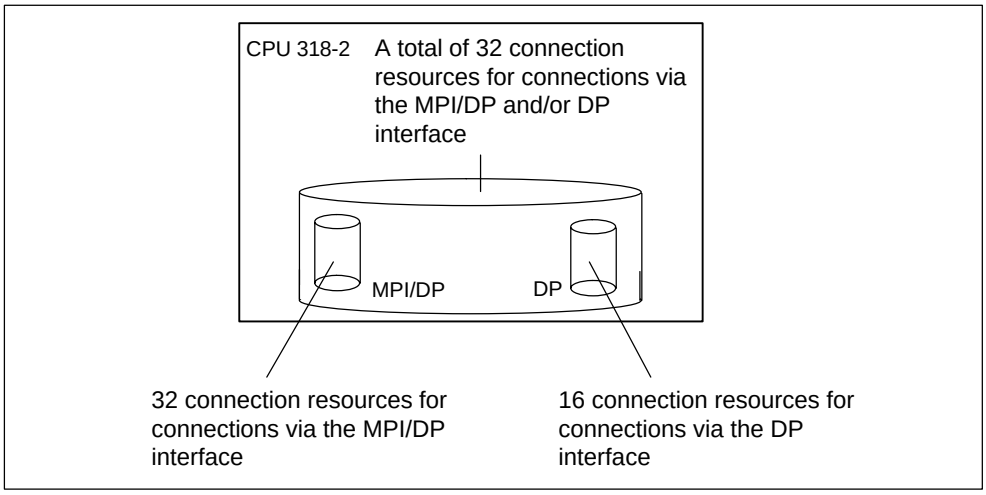


Figure 1-3 Principle of Connection Resource Allocation for CPU 318-2

Interface Resources for CPU 318-2 - Example Calculation

1. Two network transitions by routing on the CPU

Resources used:
- 2 connection resources of the MPI/DP interface are used;
- 2 connection resources of the DP interface are used;
- all 4 connection resources available to both interfaces are used;

2. 4 connections for S7 basic communication and PG/OP communication with the CPU as connection terminal point via MPI/DP interface

Resources used:
- 4 connection resources of the MPI/DP interface are used;
- all 4 connection resources available to both interfaces are used;

Resources still availabe:
- 26 connection resources of the MPI/DP interface;
- 14 connection resources of the DP interface;
- 24 of the connection resources available to both interfaces

Data Consistency for Communication

An essential aspect of the transmission of data between devices is its consistency. The data that is transmitted together should all originate from the same processing cycle and should thus belong together, i.e. be consistent.

If there is a programmed communication function such as X-SEND/ X-RCV which accesses shared data, then access to that data area can be co-ordinated by means of the parameter “BUSY” itself.

However, with S7 communication functions not requiring a block in the user program of the 31x CPU (as server), e.g. PUT/GET or read/write operations via OP communication, the dimension of data consistency must be taken into account during programming. The following differences between CPUs 312IFM to 316-2 DP and CPU 318-2 must be taken into account:

CPU 312 IFM to 316-2 DP	CPU 318-2
PUT/GET functions of S7 communication, or reading/writing variables via OP communication, are processed during the cycle checkpoint of the CPU. A defined process interrupt reaction time is ensured by consistent copying of communication variables in blocks of 32 bytes (CPU Versions lower than described in this manual: Blocks of up to 8 Bytes) into/out of user memory during the cycle checkpoint of the operating system. Data consistency is not guaranteed for any larger data areas. Therefore, communication variables in the user program must not exceed a length of 8 or 32 byte if data consistency is required. If you copy communication variables using SFC 81 “UBLKMOV”, the copying process is not interrupted by higher priority classes.	PUT/GET functions of S7 communication, or reading/writing to variable via OP communication are processed in defined time windows in the CPU 318-2 operating system. For that reason, the user program can be interrupted after every command (Byte/Word/Double Word command) when a communication variable is being accessed. The data consistency of a communication variable is therefore only possible within the limits of the command boundaries used in the user program. If a data consistency size greater than Byte, Word or DWord is required, communication variables in the user program must always be copied using SFC81 “UBLKMOV” that guarantees consistent reading/writing of the complete communication variable area.

Details

... on the communication topic are found in the *STEP 7* Online Help and in the manual *Communication with SIMATIC*.

... on communications SFCs/SFBs are found in the *STEP 7* Online Help and in the *Standard and System functions* reference manual.

Global Data Communication with S7-300 CPUs

Below you will find important features of global data communication in the S7-300.

Send/Receive Conditions

For the communication via GD circuits, you should observe the following conditions:

- Required for the GD packet transmitter is:
  $\text{Reduction}_{\text{ratio Transmitter}} \times \text{Cycle}_{\text{time Transmitter}} \geq 60$ ms (CPU 318-2: ≥ 10 ms
- Required for the GD packet receiver is:
  $\text{Reduction}_{\text{ratio Receiver}} \times \text{Cycle}_{\text{timer eceiver}} < \text{Reduction}_{\text{ratio Transmitter}} \times \text{Cycle}_{\text{time Transmitter}}$

Non-observance of these conditions can lead to the loss of a GD packet. The reasons for this are:

- The performance capability of the smallest CPU in the GD circuit
- Sending and receiving of global data is carried out asynchronously by the sender and receiver.

Loss of global data is displayed in the status field of a GD circuit if you have configured this with *STEP 7*.

Note

Note when communicating via global data: sent global data is not acknowledged by the receiving partner!

The sender therefore receives no information on whether a receiver and which receiver has received the sent global data.

Send Cycles for Global Data

In *STEP 7* (as of Version 3.0), the following situation can arise if you set “Send after every CPU cycle” with a short CPU cycle time (< 60 ms): the operating system overwrites GD packets the CPU has not yet transmitted. **Tip:** Loss of global data is displayed in the status field of a GD circuit if you have configured this with *STEP 7*.

1.3 Test Functions and Diagnostics

The CPUs provide you with:

- Testing functions for commissioning
- Diagnostics via LEDs and *STEP 7*.

1.3.1 Testing Functions

The CPUs offer you the following testing functions:

- Monitor Variables
- Modify Variables
- Forcing (note the differences between CPUs)
- Monitor block
- Set Breakpoint

Details on the testing functions are found in the *STEP 7* Online Help.

Important for the Status FB!

The *STEP 7* function “Status FB” increases CPU cycle time!

In *STEP 7* you can specify a maximum permissible increase in cycle time (not CPU 318-2). In this case, in *STEP 7* you must specify process mode for the CPU parameters.

Different Features of Forcing S7-300

Please note the different features of forcing in the different CPUs:

CPU 318-2	CPU 312IFM to 316-2DP
The variables of a user program with fixed preset values (force values) cannot be changed or overwritten by the user program. It is not permissible to force peripheral or process image areas lying in the range of consistent user data.	The variables of a user program with fixed preset values (force values) can be changed or overwritten in the user program. (See Figure 1-4 on page 1-21)
The following can be variables: Inputs/outputs Peripheral I/Os Memory markers You can force up to 256 variables.	The following can be variables: Inputs/Outputs You can force up to 10 variables.

Forcing with the CPU 312 IFM to 316-2 DP:

Caution

Forced values in the input process image can be overwritten by write instructions (e.g. T EB x, = E x.y, copying with SFC etc.) and peripheral read instructions (e.g. L PEW x) in the user program, as well as by write instructions of PG/OP operations!

Outputs initialized with forced values only return the forced value if the user program does not execute any write accesses to the outputs using peripheral write commands (e.g. TPQB x) and if no PG/OP functions write to these outputs!

Always note that forced values in the I/O process image cannot be overwritten by the user program or PG/OP functions!

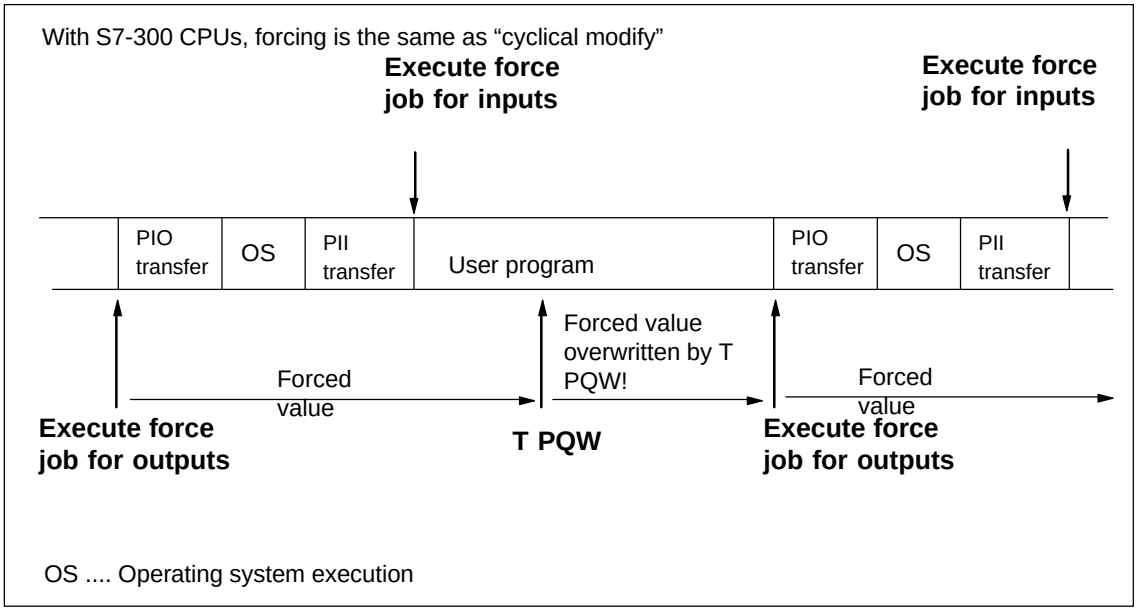


Figure 1-4 The Principle of Forcing with S7-300 CPUs (CPU 312IFM to 316-2DP)

1.3.2 Diagnostics with LED Display

In Table 1-9, only the LEDs relevant to the diagnosis of the CPU and S7-300 are listed. You will find the significance of the PROFIBUS-DP interface LEDs explained in Chapter 2.

Table 1-9 Diagnostic LEDs of the CPU

LED	Description	
SF	**Comes on** in the event of	Hardware faults Programming errors Parameter assignment errors Calculation errors Timing errors Faulty memory card Battery fault or no backup at power on I/O fault/error (external I/O only) Communication error
BATF	**Comes on** when	The backup battery is missing, faulty or not charged. **Note** Also lit if a rechargeable battery is installed. Reason: The user program is not backed up the rechargeable battery.
Stop	**Comes on** when **Flashes** when	The CPU is not processing a user program The CPU requests a memory reset

1.3.3 Diagnostics with *STEP 7*

Note

Please note that this is not a fail-safe or redundant system, regardless of its existing extensive monitoring and error reaction functions.

If an error occurs, the CPU enters the cause of the error in the diagnostic buffer. You can read the diagnostic buffer using the programming device.

The CPU switches to STOP if an error or interrupt event occurs, or your user program reacts accordingly with error or interrupt OBs. Details on *STEP 7* diagnostic functions are found in the *STEP 7* Online Help.

In the *Instruction list* you can find an overview

- of the OBs you can use to react to respective error or interrupt events, as well
- as of the OBs you can program in the respective CPU

CPU Reaction on Missing Error OB

If you have not programmed an error OB, the CPU reacts as follows:

CPU goes into STOP on missing ...	CPU Remains in RUN with Missing ...
OB 80 (Runtime error) OB 85 (Program cycle error) OB 86 (Station failure in the PROFIBUS-DP subnet) OB 87 (Communication error) OB 121 (Programming error) OB 122 (Peripheral direct access error)	OB 81 (Power break)

CPU Behavior When There Is No Interrupt OB

If you have not programmed an interrupt OB, the CPU reacts as follows:

CPU goes into STOP on missing ...	CPU Remains in RUN with Missing ...
OB 10/11 (TOD interrupt) OB 20/21 (Delay interrupt) OB 40/41 (Process interrupt) OB 55 (TOD interrupt) OB 56 (Delay interrupt) OB 57 (for manufacturer-specific interrupts) OB 82 (Diagnostic interrupt) OB 83 (Insertion/Removal interrupt)	OB 32/35 (Watchdog interrupt)

Tip on OB35 (CPU 318-2: also OB32)

For the watchdog interrupt OB 35/32, you can specify times starting from 1 ms.
Note: The smaller the selected watchdog interrupt period, the more likely watchdog interrupt errors will occur. You must take into account the operating system times of the CPU in question, the runtime of the user program and the extension of the cycle by active programming device functions, for example.

1.4 CPUs - Technical Specifications

In This Section

- You will find the technical specifications of the CPU.
- You will find the technical specifications of the integrated inputs/outputs of the CPU 312 IFM and 314 IFM.
- You will **not** find the features of the CPU 31x-2 DP as a DP master/DP slave. Refer to Chapter 2.

1.4.1 CPU 312 IFM

Special Features

- Integrated I/Os (Wiring via 20-pole front connector)
- No backup battery and therefore maintenance-free
- An S7-300 with CPU 312 IFM can be mounted only on one rack

Integrated Functions of the CPU 312 IFM

Integrated Functions	Description
Process interrupt	Interrupt input means: inputs configured with this function trigger a process interrupt at the corresponding signal edge. Interrupt input options for the digital inputs 124.6 to 125.1 must be programmed in *STEP 7*.
Counter	The CPU 312 IFM offers these special functions as an alternative at the digital inputs 124.6 to 125.1. For a description of the special functions “Counter” and “Frequency meter”, please refer to the *Integrated Functions* Manual.
Frequency meter	

“Interrupt Inputs” of the CPU 312 IFM

If you wish to use the digital inputs 124.6 to 125.1 as interrupt inputs, you must program these in *STEP 7* in the CPU parameters.

Note the following points:

- These digital inputs have a very low signal delay. At this interrupt input, the module recognizes pulses with a length as of approx. 10 to 50 µs. Always use shielded cable to connect active interrupt inputs in order to avoid interrupts triggered by line interference.
  Note The minimum pulse width of an interrupt trigger pulse is 50 µs.
- The input status associated with an interrupt in the input process image or with LPIB always changes with ”normal” input delay of approx.3 ms.

Start information for OB40

Table 1-10 shows the temporary (TEMP) variables of OB40 relevant for the “Interrupt inputs” of the CPU 312 IFM. Refer to the*System and Standard functions* reference manual for details on the process interrupt OB.

Table 1-10 Start Information for OB 40 for the Interrupt Inputs of the Integrated I/Os

Byte	Variable	Data Type	Description	
6/7	OB40_MDL_ADDR	WORD	B#16#7C	Address of the interrupt triggering module (in this case, the CPU)
8 on	OB40_POINT_ADDR	DWORD	See Figure 1-5	Signaling of the interrupt triggering integrated inputs

Display of the Interrupt Inputs

In variable OB40_POINT_ADDR, you can view the interrupt inputs which have triggered a process interrupt. Figure 1-5 shows the allocation of the interrupt inputs to the bits of the double word.

Note: Several bits can be set if interrupts are triggered by several inputs within short intervals (< 100 µs). That is, the OB is started once only, even if several interrupts are pending.

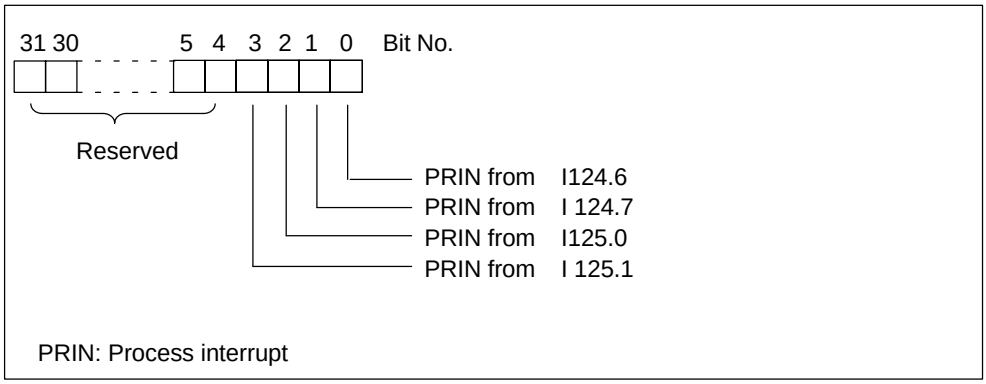


Figure 1-5 Display of the States of the Interrupt Inputs of the CPU 312 IFM

Front View

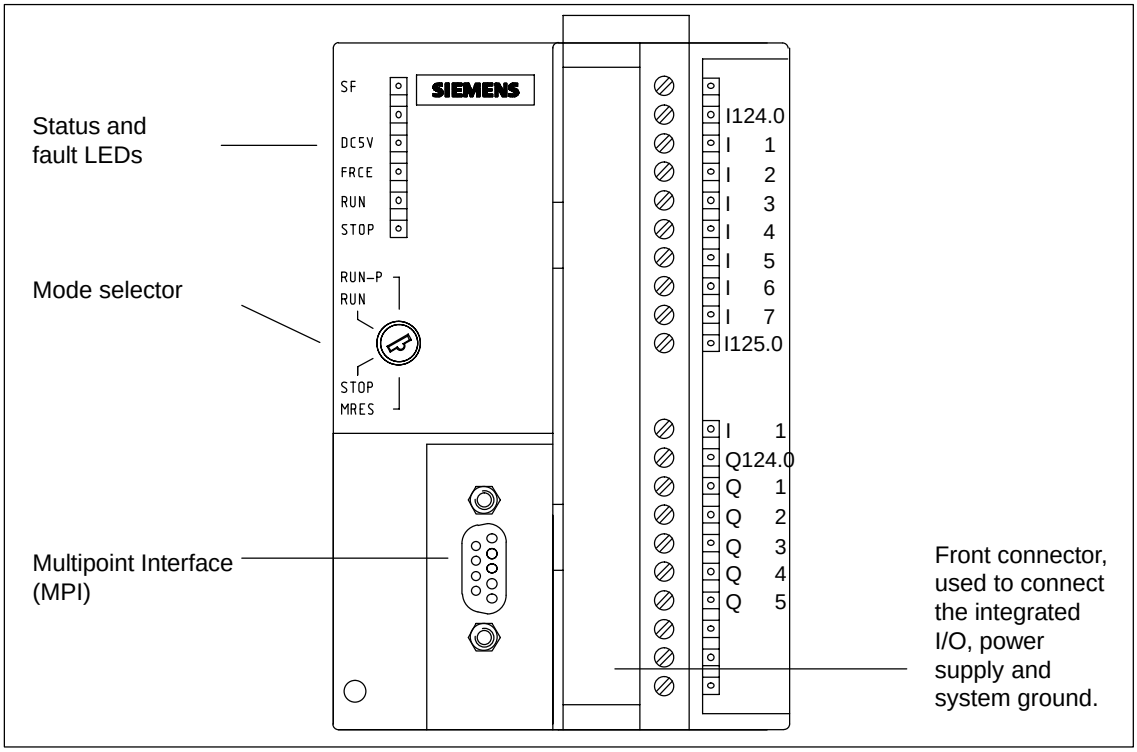


Figure 1-6 Front View of the CPU 312 IFM

Technical Specifications of the CPU 312 IFM

CPU and Product Version	
MLFB	6ES7 312-5AC02-0AB0
• Hardware version	01
• Firmware version	V 1.1.0
• Matching programming package	*STEP 7* V 5.0; Service Pack 03
Memory	
Work memory	
• integral	6 KB
• Expandable	no
Load memory	
• integral	20 KB RAM 20 KB EEPROM
• Expandable FEPROM	no
• Expandable RAM	no
Backup	Yes
• With battery	no
• Without battery	72 bytes retentive Configurable (data, flags, timers)
Processing times	
Processing times for	
• Bit instructions	0.6 μs minimum
• Word instructions	2 μs minimum
• Double integer math	3 μs minimum
• Floating-point math instructions	60 μs minimum
Timers/Counters and their retentive characteristics	
S7 counters	32
• Adjustable retentivity	from C 0 to C 31
• Preset	from C 0 to C 7
• Counting range	1 to 999
IEC Counters	Yes
• Type	SFBs
S7 timers	64
• Adjustable retentivity	No
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFBs

Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	max. 1 DB, 72 data bytes
Bit memories	1024
• Adjustable retentivity	MB 0 to MB 71
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	max. 63 (DB 0 reserved)
• Size	max. 6 KB
• Adjustable retentivity	max. 1 DB, 72 bytes
• Preset	No retentivity
Local data (non-alterable)	max. 512 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 6 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	None
FBs	max. 32;
• Size	max. 6 KB
FCs	max. 32;
• Size	max. 6 KB
Address areas (I/O)	
Peripheral address area	
• Digital	0 to 31/0 to 31
– integrated	124,125 E/124 A
• Analog	256 to 383/256 to 383
Process image (cannot be customized)	32 bytes+4 bytes integrated/ 32 bytes+4 bytes integrated
Digital channels	256+10 integrated/256+6 integrated
Analog channels	64/32

Configuration	
Rack	1
Modules per module rack	max. 8
DP Master	
• integral	None
• via CP	Yes
S7 message functions	
Simultaneously active Alarm-S blocks	None
Time	
Real-time clock	Yes
• Backed-up	No
• Accuracy	See Section 1.1.6
Operating hours counter	No
Clock synchronisation	Yes
• On PLC	Master
• On MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100

Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	No
Standard communication	No
Number of connection resources	6 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 5 from 1 to 5 1
– OP communication User-definable Default	max. 5 from 1 to 5 1
– S7 basic communication User-definable Default	max. 2 from 0 to 2 2
Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No

MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
Dimensions	
Assembly dimension B × H × T (mm)	80 × 125 × 130
Weight	Approx. 0.45 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection

Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 to 28.8 V
Current consumption (idle)	typical 0.7 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 10 A, Type B or C
PG supply on MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 9 W
Battery	No
Accumulator	No
Integrated inputs/outputs	
Addresses of integral	
• Digital inputs	E 124.0 to E 127.7
• Digital outputs	A 124.0 to A 124.7
Integrated Functions	
Counter	1 (see *Integrated Functions* manual)
Frequency meter	up to 10 kHz max. (see *Integrated Functions* manual)

Technical Specifications of the Special Inputs of the CPU 312IFM

Module-Specific Data	
Number of inputs	4 I 124.6 to 125.1
Cable length	
• Shielded	max. 100 m (109yd.)
Voltages, Currents, Potentials	
Number of inputs that can be triggered simultaneously	4
• (horizontal configuration) up to 60°C	4
• (vertical configuration) up to 40°C	4
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	
• Process interrupt	Configurable
Diagnostic functions	None

Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal I 125.0 and I 125.1 I 124.6 and I 124.7	 15 to 30 V 15 to 30 V
• For “0” signal	-3 to 5 V
Input current	
• For “1” signal I 125.0 and I 125.1 I 124.6 and I 124.7	 min. 2 mA min. 6.5 mA
Input delay time	
• For “0” to “1”	max. 50 µs
• For “1” to “0”	max. 50 µs
Input characteristic E 125.0 and E 125.1 E 124.6 and 124.7	 to IEC 1131, Type 1 to IEC 1131, Type 1
Connection of 2-wire BEROs	no
• Permissible idle current I 125.0 and I 125.1 I 124.6 and I 124.7	 max. 0.5 mA max. 2 mA
Time, Frequency	
Internal conditioning time for	
• Interrupt processing	max. 1.5 ms
Input frequency	≤ 10 kHz

Technical Specifications of the Digital Inputs of the CPU 312IFM

Note

Alternatively, you can configure the inputs I 124.6 and I 124.7 as special inputs, in which case the technical specifications listed for the special inputs apply to the inputs I 124.6 and I 124.7.

Module-Specific Data	
Number of inputs	8
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Number of inputs that can be triggered simultaneously	8
• (horizontal configuration) up to 60°C	8
• (vertical configuration) up to 40°C	8
Galvanic isolation	No

Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None
Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal	11 to 30 V
• For “0” signal	-3 to 5 V
Input current	
• For “1” signal	typical 7 mA
Input delay time	
• For “0” to “1”	1.2 to 4.8 ms
• For “1” to “0”	1.2 to 4.8 ms
Input characteristic	to IEC 1131, Type 2
Connection of 2-wire BEROs	Possible
• Permissible quiescent current	max. 2 mA

Technical Specifications of the Digital Outputs of the CPU 312IFM

Module-Specific Data	
Number of outputs	6
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Total current of outputs (per group)	
• (horizontal configuration) up to 40°C	max. 3 A
up to 60°C	max. 3 A
• (vertical configuration) up to 40°C	max. 3 A
Galvanic isolation	No
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None

Actuator Selection Data	
Output voltage	
• For “1” signal	min. L+ (-0.8 V)
Output current	
• For “1” signal	
Rated value	0.5 A
Permissible range	5 mA to 0.6 A
• For “0” signal Residual current	max. 0.5 mA
Load impedance range	48 Ω to 4 kΩ
Lamp load	max. 5 W
Parallel connection of 2 outputs	
• For dual-channel triggering of a load	Possible
• For performance increase	Not possible
Triggering of a digital input	Possible
Switching frequency	
• For resistive load	max. 100 Hz
• For inductive load to IEC947-5-1, DC 13	max. 0.5 Hz
• For lamp load	max. 100 Hz
Inductive breaking voltage limited internally to	typical V 30
Short-circuit protection of the output	yes, electronically timed
• Response threshold	typical 1 A

Wiring diagram of the CPU 312 IFM

Figure 1-7 shows the wiring diagram of the CPU 312 IFM. Use a 20-pole front connector to wire the CPU's integrated I/O.

Caution

The CPU 312 IFM has no reverse polarity protection. Polarity reversal destroys the integrated outputs. Nonetheless, in this case the CPU does not switch to STOP and the status displays are lit. In other words, the fault is not indicated.

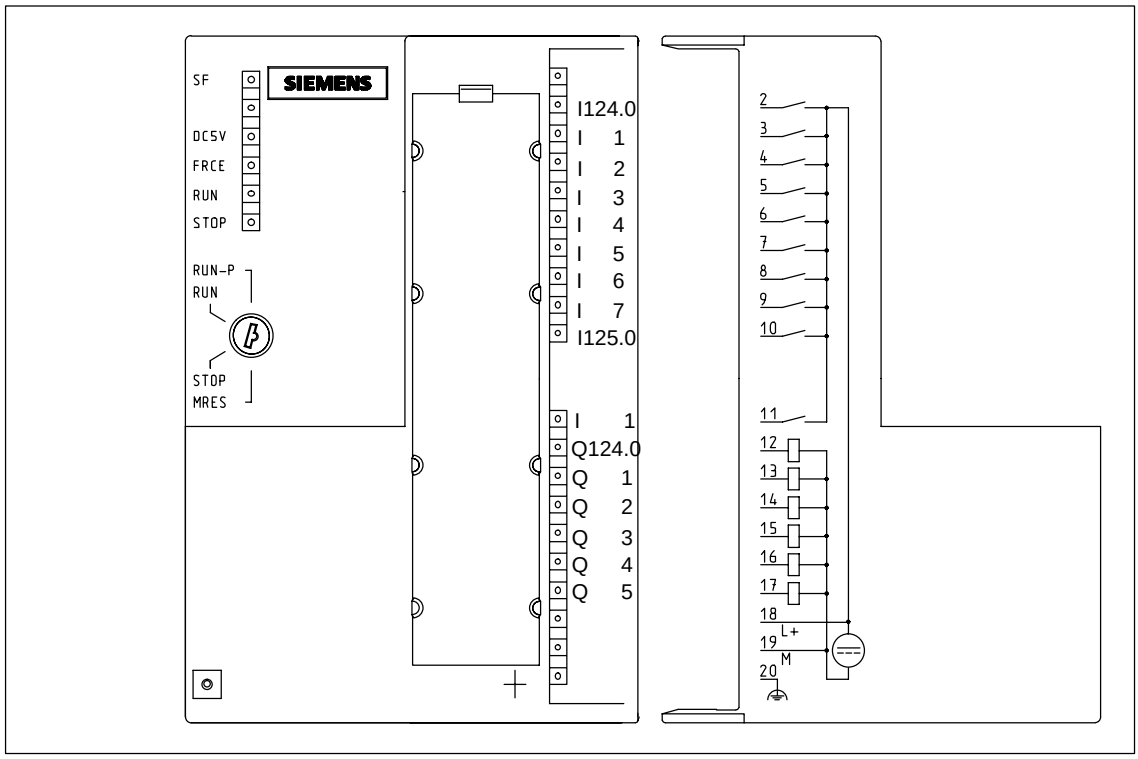


Figure 1-7 Wiring diagram of the CPU 312 IFM

Grounded Configuration Only

You can use the CPU 312 IFM in a grounded configuration only. In the CPU 312 IGFM, system ground is connected internally to chassis ground (M) (see Figure 1-8, page 1-36).

Power Supply Connections

The

- CPU 312 IFM **and**
- the integrated I/Os

are connected to power at the terminals 18 and 19 (see Figure 1-7).

Short-circuit reaction

On short-circuit at one of the integrated outputs of CPU 312 IFM, proceed as follows:

1. Switch the CPU 312 IFM to STOP or switch off the power supply.
2. Eliminate the cause of the short-circuit.
3. Switch the CPU 312 IFM back to RUN or switch the power supply back on.

Basic Circuit Diagram of the CPU 312 IFM

Figure 1-8 shows the block diagram of CPU 312 IFM.

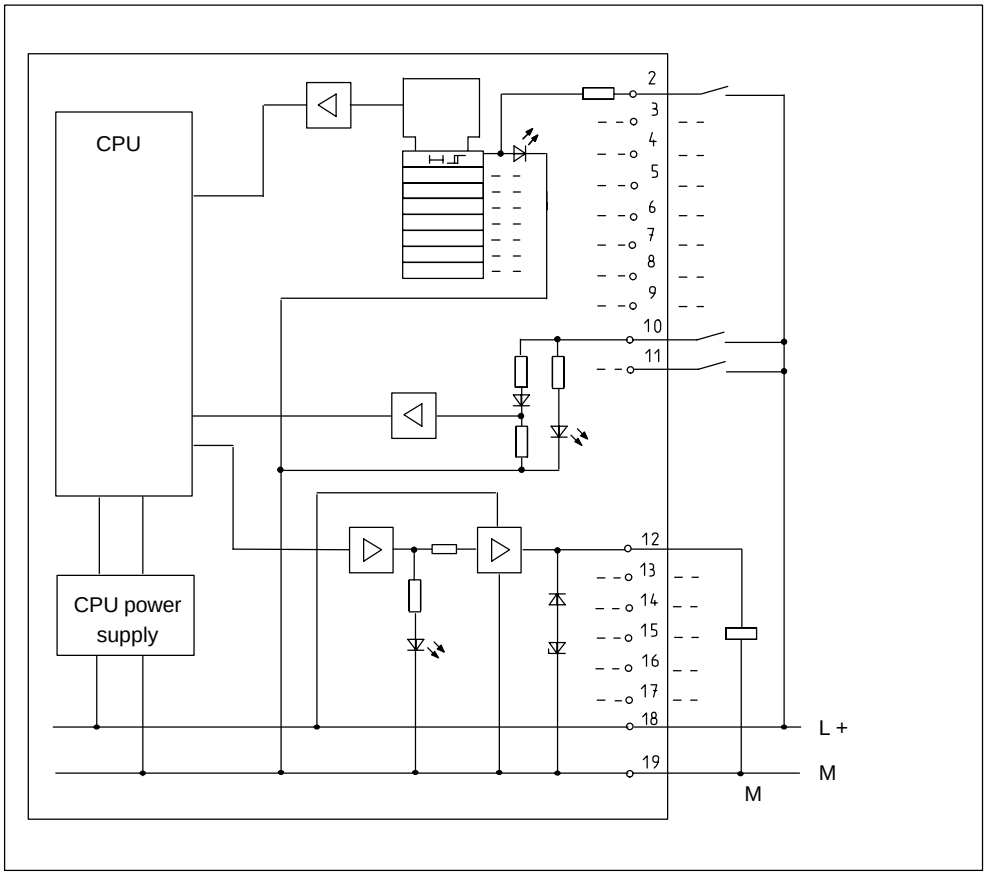


Figure 1-8 Basic Circuit Diagram of the CPU 312 IFM

1.4.2 CPU 313

Technical Specifications of the CPU 313

CPU and Product Version	
MLFB	6ES7 313-1AD03-0AB0
• Hardware version	01
• Firmware version	V 1.1.0
• Matching programming package	*STEP 7* V 5.0; Service Pack 03
Memory	
Work memory	
• integral	12 KB
• Expandable	no
Load memory	
• integral	20 KB RAM
• Expandable FEPROM	Up to 4 MB
• Expandable RAM	no
Backup	Yes
• With battery	All data
• Without battery	72 bytes retentive Configurable (data, flags, timers)
Processing times	
Processing times for	
• Bit instructions	0.6 µs minimum
• Word instructions	2 µs minimum
• Double integer math	2 µs minimum
• Floating-point math instructions	60 µs minimum
Timers/Counters and their retentive characteristics	
S7 counters	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
• Counting range	1 to 999
IEC Counters	Yes
• Type	SFB
S7 timers	128
• Adjustable retentivity	from T 0 to T 31
• Preset	No retentive times
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB

Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	max. 1 DB, 72 data bytes
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 71
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	max. 127 (DB 0 reserved)
• Size	max. 8 KB
• Adjustable retentivity	1 DB, 72 bytes
• Preset	No retentivity
Local data (non-alterable)	max. 1536 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 8 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	4
FBs	128
• Size	max. 8 KB
FCs	128
• Size	max. 8 KB
Address areas (I/O)	
Peripheral address area	
• Digital	0 to 31/0 to 31
• Analog	256 to 383/256 to 383
Process image (cannot be customized)	32 bytes/32 bytes
Digital channels	max. 256/256
Analog channels	max. 64/32

Configuration	
Rack	1
Modules per module rack	max. 8
Number of DP masters	
• integral	No
• via CP	1
S7 message functions	
Simultaneously active Alarm-S blocks	None
Time	
Real-time clock	Yes
• Backed-up	No
• Accuracy	See Section 1.1.6
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master
• On MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100

Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	No
Standard communication	No
Number of connection resources	8 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 7 from 1 to 7 1
– OP communication User-definable Default	max. 7 from 1 to 7 1
– S7 basic communication User-definable Default	max. 4 from 0 to 4 4
Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No

MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
Dimensions	
Assembly dimension B × H × T (mm)	80 × 125 × 130
Weight	Approx. 0.53 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection

Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 to 28.8
Current consumption (idle)	typical 0.7 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A Type B or C
PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 8 W
Battery	
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	No

1.4.3 CPU 314

Technical Specifications of the CPU 314

CPU and Product Version	
MLFB	6ES7 314-1AE04-0AB0
• Hardware version	01
• Firmware version	V 1.1.0
• Matching programming package	*STEP 7* V 5.0; Service Pack 03
Memory	
Work memory	
• integral	24 KB
• Expandable	no
Load memory	
• integral	40 KB RAM
• Expandable FEPROM	Up to 4 MB
• Expandable RAM	no
Backup	Yes
• With battery	All data
• Without battery	4736 bytes, configurable, (data, flags, timers)
Processing times	
Processing times for	
• Bit instructions	0.3 µs minimum
• Word instructions	1 µs minimum
• Double integer math	2 µs minimum
• Floating-point math instructions	50 µs minimum
Timers/Counters and their retentive characteristics	
S7 counters	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
S7 timers	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB

Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	4736 bytes
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	max. 127 (DB 0 reserved)
• Size	max. 8 KB
• Adjustable retentivity	max. 8 DB, 4096 data bytes in all
• Preset	No retentivity
Local data (non-alterable)	max. 1536 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 8 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	4
FBs	max. 128
• Size	max. 8 KB
FCs	max. 128
• Size	max. 8 KB
Address areas (I/O)	
Peripheral address area	
• Digital	0 to 127/0 to 127
• Analog	256 to 767/256 to 767
Process image (cannot be customized)	128 bytes/128 bytes
Digital channels	max. 1024/1024
Analog channels	max. 256/128

Configuration	
Rack	max. 4
Modules per module rack	max. 8
Number of DP masters	
• integral	None
• via CP	1
S7 message functions	
Simultaneously active Alarm-S blocks	max. 40
Time	
Real-time clock	Yes
• Backed-up	Yes
• Accuracy	See Section 1.1.6
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master
• On MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100

Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Standard communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Number of connection resources	12 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 11 from 1 to 11 1
– OP communication User-definable Default	max. 11 from 1 to 11 1
– S7 basic communication User-definable Default	max. 8 from 0 to 8 8
Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No

MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
Dimensions	
Assembly dimension B × H × T (mm)	80 × 125 × 130
Weight	Approx. 0.53 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection

Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 V to 28.8 V
Current consumption (idle)	typical 0.7 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, Type B or C
PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 8 W
Battery	Yes
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	Yes
• Clock back-up period	
– at 0 to 25°C	Approx. 4 weeks
– at 40° C	Approx. 3 weeks
– at 60 ° C	Approx. 1 week
• Battery charging time	Approx. 1 hour

1.4.4 CPU 314IFM

Special Features

- Integrated I/Os (wired with 40-pole front connector)

Details on analog value processing and how to connect measuring transducers, load and actuators to analog I/O is found in the *Module Data* reference manual. Figures 1-14 and 1-15 on page 1-59 show wiring examples.

Memory card

The CPU 314 IFM is available in 2 versions: with and without Memory Card slot.

- With slot for memory card: 6ES7 314-5AE**10**-0AB0
- Without slot for memory card: 6ES7 314-5AE**0x**-0AB0

Integrated Functions of the CPU 314 IFM

Integrated Functions	Description
Process interrupt	Interrupt input means: inputs configured with this function trigger a process interrupt at the corresponding signal edge. If you wish to use the digital inputs 126.0 to 126.3 as interrupt inputs, you must program these using *STEP 7*. **Note:** Your user program should access analog inputs of your CPU individually per L PEW in order to avoid an increase of interrupt response times. Double-word addressing can increase the access times by up to 200 µs!
Counter	The CPU 314 IFM offers these special functions as an alternative at the digital inputs 126.0 to 126.3. For a description of these special functions, please refer to the *Integrated Functions* Manual.
Frequency meter	
Counter A/B	
Positioning	
CONT_C	These functions are not restricted to specific inputs and outputs of the CPU 314 IFM. For a description of these functions, please refer to the *System and Standard Functions* Reference Manual.
CONT_S	
PULSEGEN	

“Interrupt Inputs” of the CPU 314 IFM

If you want to assign interrupt functions to the digital inputs 126.0 to 126.4, configure your CPU parameters in *STEP 7* accordingly.

Note the following points:

These digital inputs have a very low signal delay. At this interrupt input, the module recognizes pulses with a length as of approx. 10 to 50 μs. Always use shielded cable to connect active interrupt inputs in order to avoid interrupts triggered by line interference.

Note The minimum pulse width of an interrupt trigger pulse is 50 μs.

Start information for OB40

Table 1-10 shows the temporary (TEMP) variables of OB40 relevant for the “Interrupt inputs” of the CPU 314 IFM. Refer to the*System and Standard functions* reference manual for details on the process interrupt OB.

Table 1-11 Start Information for OB 40 for the Interrupt Inputs of the Integrated I/Os

Byte	Variable	Data Type	Description	
6/7	OB40_MDL_ADDR	WORD	B#16#7C	Address of the interrupt triggering module (in this case, the CPU)
8 on	OB40_POINT_ADDR	DWORD	See Figure 1-9	Signaling of the interrupt triggering integrated inputs

Display of the Interrupt Inputs

In variable OB40_POINT_ADDR, you can view the interrupt inputs which have triggered a process interrupt. Figure 1-9 shows the allocation of the interrupt inputs to the bits of the double word.

Note: Several bits can be set if interrupts are triggered by several inputs within short intervals (< 100 µs). That is, the OB is started once only, even if several interrupts are pending.

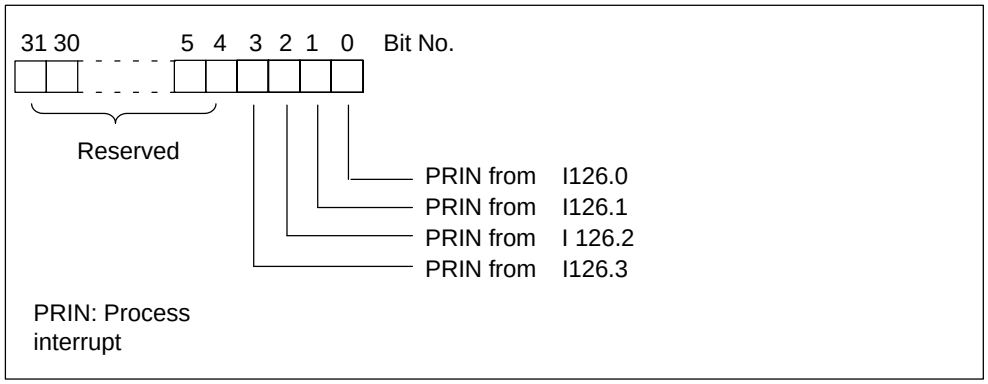
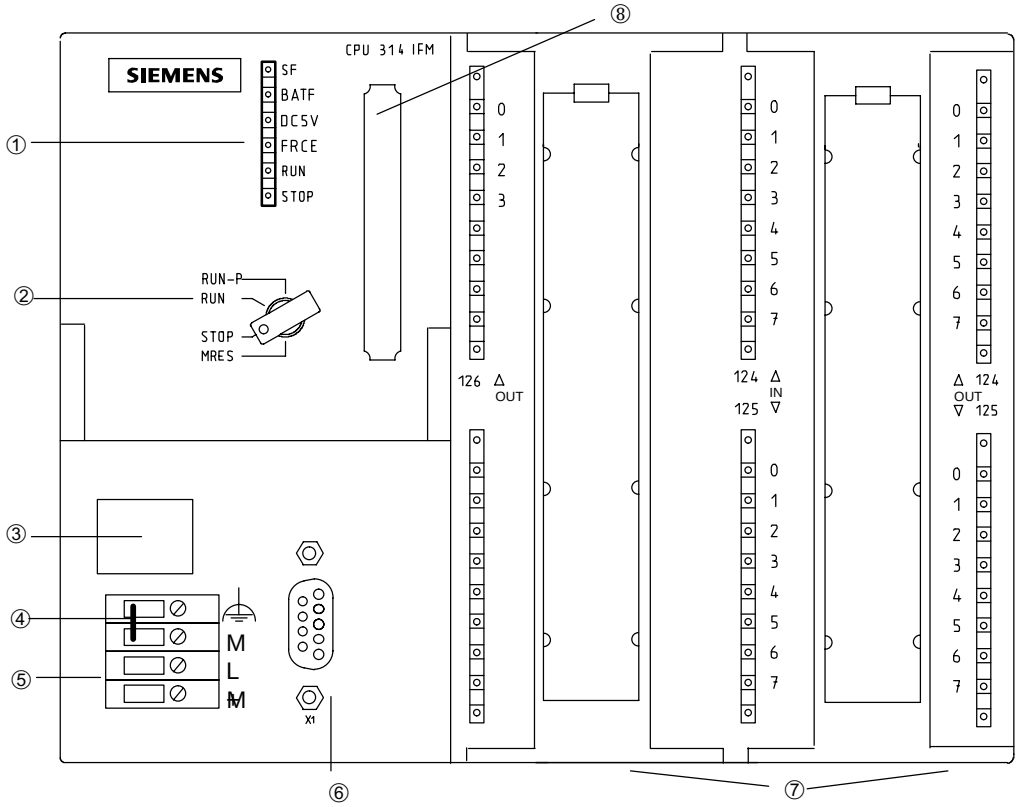


Figure 1-9 Display of the States of the Interrupt Inputs of the CPU 314 IFM

Front View of the CPU 314 IFM



① Status and error LEDs
② Mode selector switch
③ Compartment for backup battery or rechargeable battery
④ Jumper (removable)
⑤ Connection for power supply and system ground
⑥ Multipoint interface MPI
⑦ Integrated I/Os
⑧ Memory Card slot (only -5AE**10**-)

Figure 1-10 Front View of the CPU 314 IFM

Technical Specifications of the CPU 314 IFM

CPU and Product Version		
MLFB 6ES7 314-...-0AB0	-5AE**03**-	-5AE**10**-
• Hardware version	01	01
• Firmware version	V 1.1.0	V 1.1.0
• Matching programming package	*STEP 7* V5.0, Service Pack 3	
Memory		
Work memory		
• integral	32 KB	32 KB
• Expandable	no	No
Load memory		
• integral	48 KB RAM 48 KB FEPROM	48 KB RAM
• Expandable FEPROM	no	Up to 4 MB
• Expandable RAM	no	No
Backup	Yes	
• With battery	All data	
• Without battery	144 bytes	
Processing times		
Processing times for		
• Bit instructions	0.3 µs minimum	
• Word instructions	1 µs minimum	
• Double integer math	2 µs minimum	
• Floating-point math instructions	50 µs minimum	
Timers/Counters and their retentive characteristics		
S7 counters	64	
• Adjustable retentivity	from C 0 to C 63	
• Preset	from C 0 to C 7	
• Counting range	0 to 999	
IEC Counters	Yes	
• Type	SFB	
S7 timers	128	
• Adjustable retentivity	from T 0 to T 7	
• Preset	No retentive times	
• Timing range	10 ms to 9990 s	
IEC Timers	Yes	
• Type	SFB	

Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	max. 2 DB, 144 bytes
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 143
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	max. 127 (DB 0 reserved)
• Size	max. 8 KB
• Adjustable retentivity	max. 2 DB, 144 data bytes
• Preset	No retentivity
Local data (non-alterable)	1536 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 8 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	4
FBs	128
• Size	max. 8 KB
FCs	128
• Size	max. 8 KB
Address areas (I/O)	
Peripheral address area	
• Digital	0 to 123/0 to 123
– integral	124 to 127/124, 125
• Analog	256 to 751/256 to 751
– integral	128 to 135/128, 129
Process image (cannot be customized)	128 bytes/128 bytes
Digital channels	max. 992+20 integral/ max. 992+16 integral
Analog channels	max. 248+4 integral/ max. 124+1 integral

Configuration	
Rack	max. 4
Modules per module rack	max. 8; max. 7 in module rack 3
Number of DP masters	
• integral	None
• via CP	1
S7 message functions	
Simultaneously active Alarm-S blocks	max. 40
Time	
Real-time clock	Yes
• Backed-up	Yes
• Accuracy	See Section 1.1.6
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master
• On MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100

Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Standard communication	Yes (via FC and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Number of connection resources	12 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 11 from 1 to 11 1
– OP communication User-definable Default	max. 11 from 1 to 11 1
– S7 basic communication User-definable Default	max. 8 from 0 to 8 8
Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No

MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
Dimensions	
Assembly dimension B × H × T (mm)	160 × 125 × 130
Weight	Approx. 0.9 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection
Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 to 28.8 V
Current consumption (idle)	typical 1.0 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A Type B or C

PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	Typically 16 W
Battery	Yes
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	Yes
• Clock back-up period	
– at 0 to 25°C	Approx. 4 weeks
– at 40° C	Approx. 3 weeks
– at 60 ° C	Approx. 1 week
• Battery charging time	Approx. 1 hour
Integrated inputs/outputs	
Addresses of integral	
• Digital inputs	E 124.0 to E 127.7
• Digital outputs	A 124.0 to A 127.7
• Analog inputs	PIW 128 to PIW 134
• Analog outputs	PQW 128
Integrated Functions	
Counter	1 or 2, 2 directional comparisons (see *Integrated Functions* manual)
Frequency meter	up to 10 kHz max. (see *Integrated Functions* manual)
Positioning	Channel 1 (see *Integrated Functions* manual)

Characteristic Features of the Integrated Inputs and Outputs of the CPU 314 IFM

Table 1-12 Characteristic Features of the Integrated Inputs and Outputs of the CPU 314 IFM

Inputs/Outputs	Characteristics	
Analog inputs	• Voltage inputs ± ±10 V • Current inputs ± ±20 mA • Resolution 11 bits + sign bit • Galvanically isolated	All information required for • analog value display, as well as for • connecting measuring transducers, loads and actuators to the analog I/Os can be found in the *Module Specifications* Reference Manual.
Analog output	• Voltage output ± ±10 V • Current output ± ±20 mA • Resolution 11 bits + sign bit • Galvanically isolated	
Digital inputs	**Special inputs (E 126.0 to E 126.3)**	**“Standard” Inputs**
	• Input frequency up to 10 kHz • Non-isolated	• Galvanically isolated
	• Rated input voltage 24V DC • Suitable for switch and 2-wire proximity switches (BEROs)	
Digital outputs	• Output current 0.5 A • Rated load voltage 24V DC • Galvanically isolated • Suitable for solenoid valves and DC contactors	

Technical Specifications of the Analog Inputs of the CPU 314IFM

Module-Specific Data	
Number of inputs	4
Cable length	
• Shielded	max. 100 m (109yd.)
Voltages, Currents, Potentials	
Galvanic isolation	
• between channels and backplane bus	Yes
Permissible potential difference	1.0V DC
• between inputs and M_{ANA} (U_{CM})	75V DC
• between M_{ANA} and $M_{internal}$ (U_{ISO})	60V AC
Insulation tested at	500V DC
Analog Value Generation	
Measurement principle	Momentary value encoding (successive approximation)
Conversion time/Resolution (per channel)	
• Basic conversion time	100 µs
• Resolution (inc. overdrive range)	11 bits + sign bit
Interference Suppression, Error Limits	
Interference voltage suppression	> 40 dB
• Common-mode interference (U_{CM}<1.0 V)	
Crosstalk between the inputs	> 60 dB
Operational error limits (throughout temperature range, relative to input range)	± 1.0 %
• Voltage input	± 1.0 %
• Current input	

Interference Suppression, Error Limits, Continued	
Basic error limits (operational limit at 25°C, relative to input range)	
• Voltage input	± 0.9 %
• Current input	± 0.8 %
Temperature error (referred to input range)	± ± 0.01 %/K
Linearity error (referred to input range)	± 0.06 %
Accuracy of reproducibility (in transient state at 25°C, referring to input range)	± 0.06 %
Status, Interrupts, Diagnostics	
Interrupts	None
Diagnostic functions	None
Sensor Selection Data	
Input ranges (rated value)/input resistance	
• Voltage	± ± 10 V/50 kΩ
• Current	± ± 20 mA/105.5 Ω
Permissible input voltage for voltage input (destruction limit)	max. 30 V continuous; 38 V for max. 1 s (pulse duty factor 1:20)
Permissible input current for current input (destruction limit)	34 mA
Connecting signal generators	
• for voltage measurement	Possible
• for current measurement	Not possible
as 2-pole measurement transducer	Possible
as 4-pole measurement transducer	

Technical Specifications of the Analog Output of the CPU 314IFM

Module-Specific Data	
Number of outputs	1
Cable length	
• Shielded	max. 100 m (109yd.)
Voltages, Currents, Potentials	
Galvanic isolation	
• Between channels and backplane bus	Yes
Permissible potential difference	
• between M_{ANA} and $M_{internal}$ (U_{ISO})	75V DC 60V AC
Insulation tested at	500V DC
Analog Value Generation	
Resolution (inc. overdrive range)	11 bits + sign bit
Conversion time	40 µs
Settling time	
• For resistive load	0.6 ms
• For capacitive load	1.0 ms
• For inductive load	0.5 ms
Connection of substitute values	No
Interference Suppression, Error Limits	
Operational error limits (throughout temperature range, relative to output range)	± 1.0 %
• Voltage output	± 1.0 %
• Current output	
Basic error limit (operational limit at 25°C, relative to output range)	
• Voltage output	± 0.8 %
• Current output	± 0.9 %
Temperature error (relative to output range)	± ± 0.01 %/K
Linearity error (relative to output range)	± 0.06 %
Accuracy of reproducibility (in transient state at 25°C, relative to output range)	± 0.05 %
Output ripple; Range of 0 to 50 kHz (referring to output range)	± 0.05 %
Status, Interrupts; Diagnostics	
Interrupts	None
Diagnostic functions	None
Actuator Selection Data	
Output ranges (rated values)	
• Voltage	± ± 10 V
• Current	± ± 20 mA
Load impedance	
• For voltage output	min. 2.0 kΩ
capacitive load	max. 0.1 µF
• For current output	max. 300 Ω
inductive load	max. 0.1 mH
Voltage output	
• Short-circuit protection	Yes
• Short-circuit current	max. 40 mA
Current output	
• Idle voltage	max. 16 V
Destruction limit for externally applied voltages/currents	
• Voltages at the output with ref. to M_{ANA}	max. ± ± 15 V, continuous; ± ± 15 V for max. 1 s (duty factor 1:20)
• Current	max. 30 mA
Connecting actuators	
• for voltage output	
2-wire connection	Possible
4-wire connection	Not possible
• for current output	
2-wire connection	Possible

Technical Specifications of the Special Inputs of the CPU 314IFM

Module-Specific Data	
Number of inputs	4 I 126.0 to 126.3
Cable length	
• Shielded	max. 100 m (109yd.)
Voltages, Currents, Potentials	
Number of inputs that can be triggered simultaneously	4
• (horizontal configuration) up to 60°C	4
• (vertical configuration) up to 40°C	4
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	
• Process interrupt	Configurable
Diagnostic functions	None

Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal	11 V to 30 V 18 to 30 V with angular encoder and integrated ”Positioning” function
• For “0” signal	-3 to 5 V
Input current	
• For “1” signal	typical 6.5 mA
Input delay time	
• For “0” to “1”	< 50 µs (typical 17 µs)
• For “1” to “0”	< 50 µs (typical 20 µs)
Input characteristic	to IEC 1131, Type 2
Connection of 2-wire BEROs	Possible
• Permissible quiescent current	max. 2 mA
Time, Frequency	
Internal conditioning time for	
• Interrupt processing	max. 1.2 ms
Input frequency	≤ 10 kHz

Technical Specifications of the Digital Inputs of the CPU 314IFM

Module-Specific Data	
Number of inputs	16
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Rated load current L+	24V DC
• Polarity reversal protection	Yes
Number of inputs that can be triggered simultaneously	16
• (horizontal configuration) up to 60°C	16
• (vertical configuration) up to 40°C	16
Galvanic isolation	
• between channels and backplane bus	Yes
Permissible potential difference	75V DC
• Between different circuits	60V AC
Insulation tested at	500V DC
Current consumption	
• on power supply L+	max. 40 mA

Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None
Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal	11 to 30 V
• For “0” signal	-3 to 5 V
Input current	
• For “1” signal	typical 7 mA
Input delay time	
• For “0” to “1”	1.2 to 4.8 ms
• For “1” to “0”	1.2 to 4.8 ms
Input characteristic	to IEC 1131, Type 2
Connection of 2-wire BEROs	Possible
• Permissible quiescent current	max. 2 mA

Technical Specifications of the Digital Outputs of the CPU 314IFM

Remarks

When the supply voltage is switched on a pulse occurs on the digital outputs! This can be 50 ms long within the permissible output current range. You must not, therefore, use the digital outputs to trigger high-speed counters.

Module-Specific Data	
Number of outputs	16
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Rated load current L+	24V DC
• Polarity reversal protection	No
Total current of outputs (per group)	
• (horizontal configuration)	max. 4 A
up to 40°C	max. 2 A
up to 60°C	
• (vertical configuration)	max. 2 A
up to 40°C	
Galvanic isolation	
• between channels and backplane bus	Yes
• Between the channels	Yes
in groups of	8
Permissible potential difference	75V DC
• Between different circuits	60V AC
Insulation tested at	500V DC
Current consumption	
• on L+ supply (no load)	max. 100 mA
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None

Actuator Selection Data	
Output voltage	
• For “1” signal	min. L+ (-0.8 V)
Output current	
• For “1” signal	
Rated value	0.5 A
Permissible range	5 mA to 0.6 A
• For “0” signal (residual current)	max. 0.5 mA
Load impedance range	48 Ω to 4 kΩ
Lamp load	max. 5 W
Parallel connection of 2 outputs	
• For dual-channel triggering of a load	Possible, only outputs of the same group
• For performance increase	Not possible
Triggering of a digital input	Possible
Switching frequency	
• For resistive load	max. 100 Hz
• For inductive load to IEC947-5-1, DC 13	max. 0.5 Hz
• For lamp load	max. 100 Hz
Inductive breaking voltage limited internally to	typical L+ (- 48 V)
Short-circuit protection of the output	yes, electronically timed
• Response threshold	typical 1a

Wiring diagram of the CPU 314 IFM

Figure 1-11 shows the wiring diagram of the CPU 314 IFM.

For the connection of integrated I/O you require two 40-pole front connectors (Order no.: 6ES7392-1AM00-0AA0).

Always wire up digital inputs 126.0 to 126.3 with shielded cable due to their low input delay time.

Caution

Wiring errors at the analog outputs can cause the integrated analog I/O of the CPU to be destroyed! (for example, if the interrupt inputs are wired by mistake to the analog output).
The analog output of the CPU is only indestructible up to 15 V (output with respect to M_{ANA}).

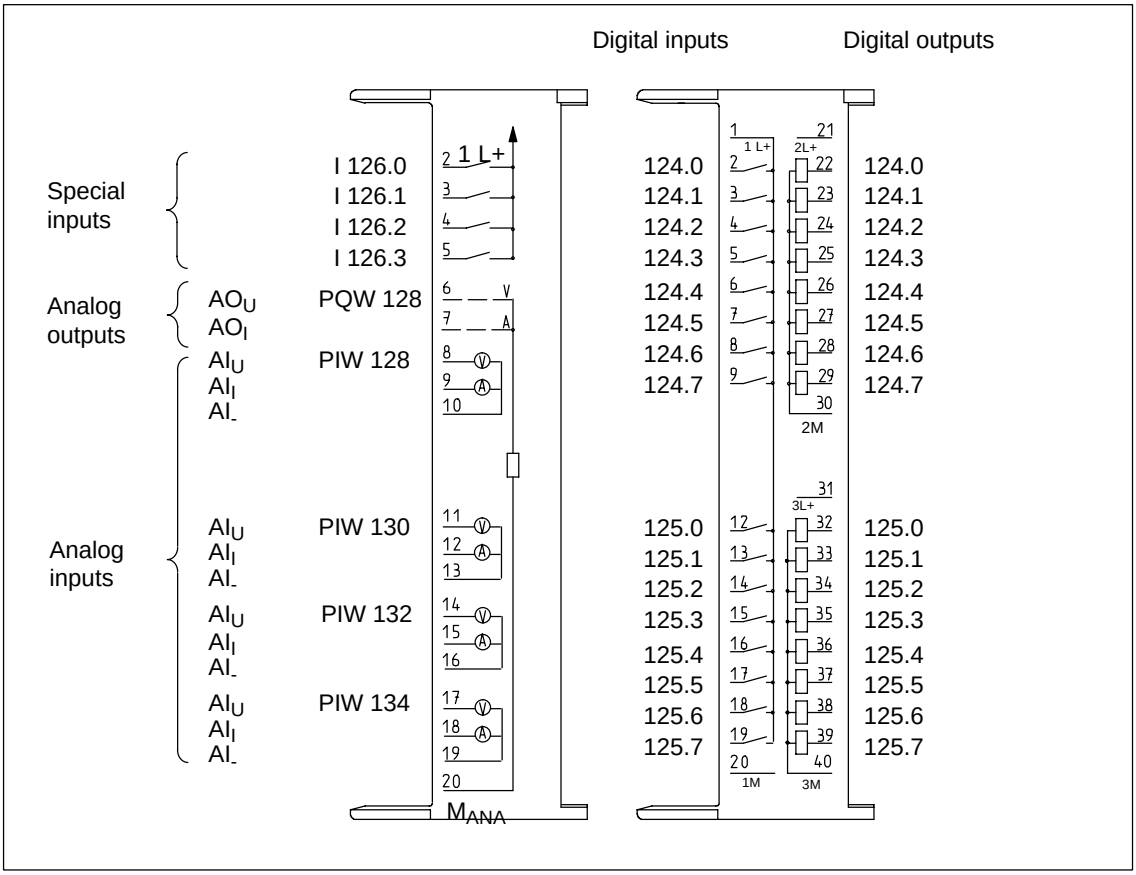


Figure 1-11 Wiring diagram of the CPU 314 IFM

Basic Circuit Diagrams of the CPU 314 IFM

Figures 1-12 and 1-13 show the basic circuit diagrams for the integrated inputs/outputs of the CPU 314 IFM.

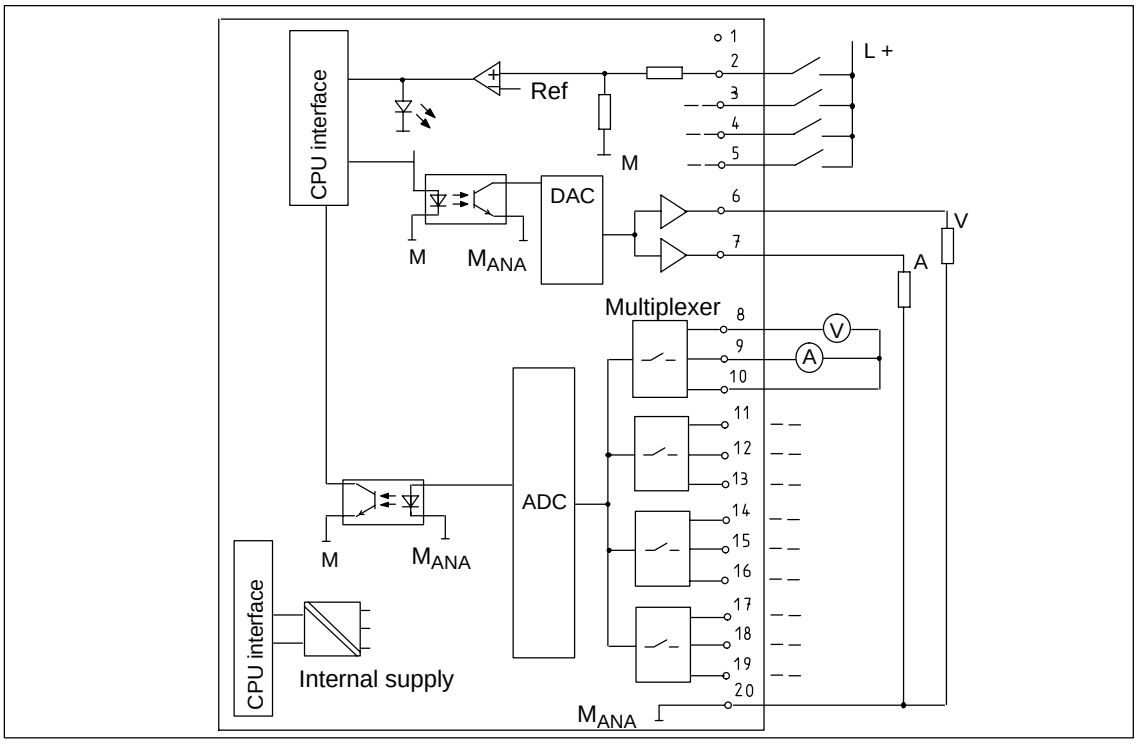


Figure 1-12 Basic Circuit Diagram of the CPU 314 IFM (Special Inputs and Analog Inputs/Outputs)

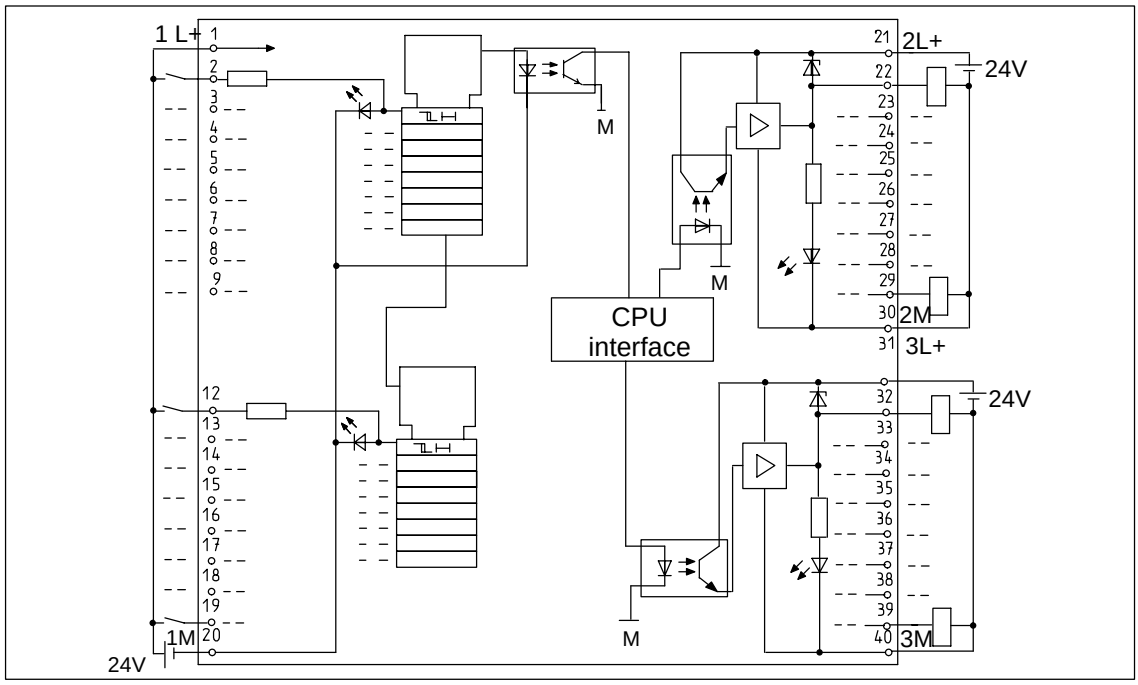


Figure 1-13 Basic Circuit Diagram of the CPU 314 IFM (Digital Inputs/Outputs)

Wiring the Analog Inputs

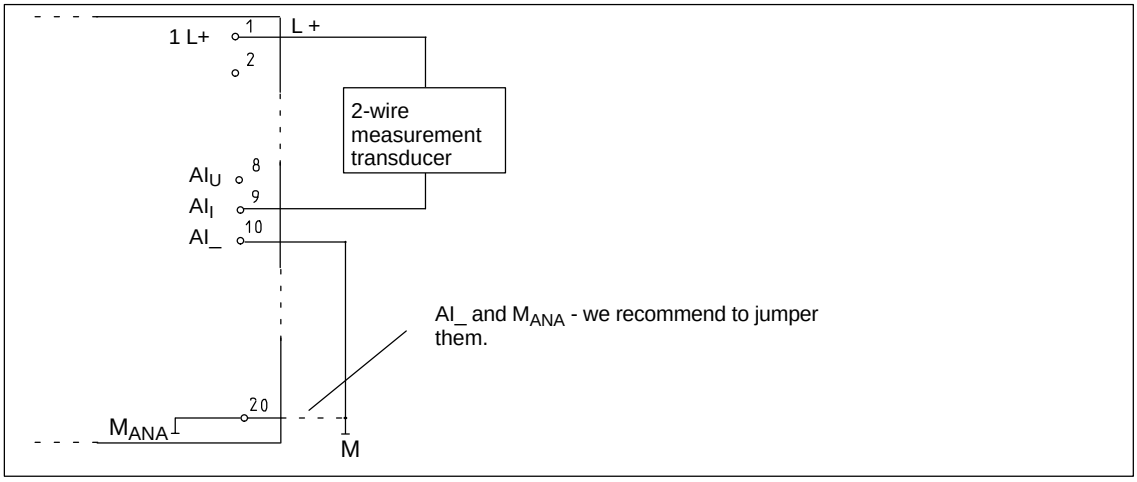


Figure 1-14 Connecting 2-wire measurement transducers to the analog inputs of CPU 314 IFM

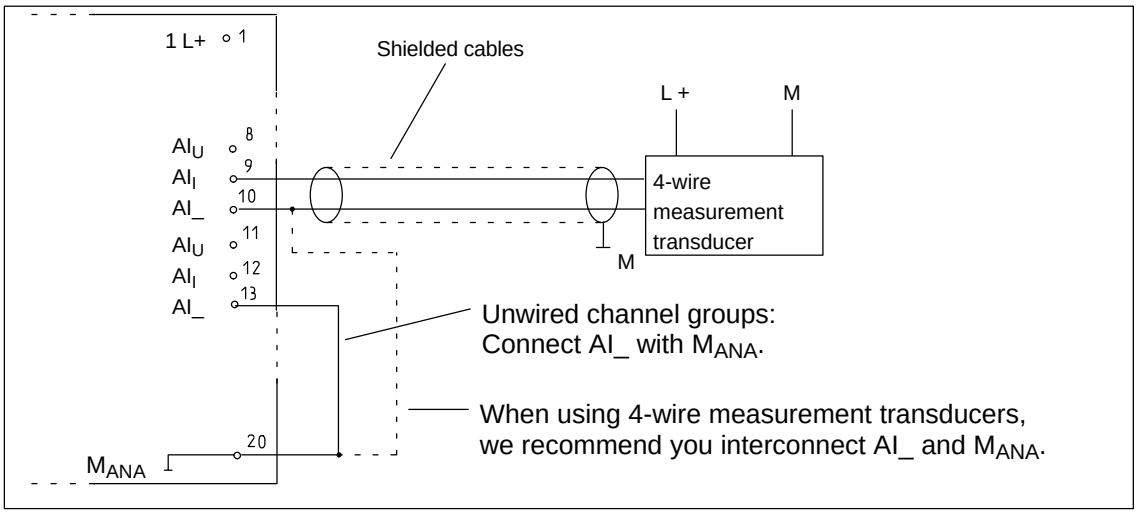


Figure 1-15 Wiring of 4-wire measurement transducers to the analog inputs of CPU 314 IFM

1.4.5 CPU 315

Technical Specifications of the CPU 315

CPU and Product Version	
MLFB	6ES7 315-5AF03-0AB0
• Hardware version	01
• Firmware version	V 1.1.0
• Matching programming package	*STEP 7* V 5.0; Service Pack 03
Memory	
Work memory	
• integral	48 KB
• Expandable	no
Load memory	
• integral	80 KB RAM
• Expandable FEPROM	Up to 4 MB
• Expandable RAM	no
Backup	Yes
• With battery	All data
• Without battery	4736 bytes, configurable, (data, flags, timers)
Processing times	
Processing times for	
• Bit instructions	0.3 µs minimum
• Word instructions	1 µs minimum
• Double integer math	2 µs minimum
• Floating-point math instructions	50 µs minimum
Timers/Counters and their retentive characteristics	
S7 counters	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
S7 timers	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB

Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	4736 bytes
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	max. 255 (DB 0 reserved)
• Size	max. 16 KB
• Adjustable retentivity	max. 8 DB, 4096 data bytes in all
• Preset	No retentivity
Local data (non-alterable)	max. 1536 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 16 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	4
FBs	max. 192
• Size	max. 16 KB
FCs	max. 192
• Size	max. 16 KB
Address areas (I/O)	
Peripheral address area	
Digital/Analog	1 KB/1 KB (freely addressable)
Process image (cannot be customized)	128 bytes/128 bytes
Digital channels	max. 1024/1024
Analog channels	max. 256/128

Configuration	
Rack	max. 4
Modules per module rack	max. 8
Number of DP masters	
• integral	None
• via CP	1
S7 message functions	
Simultaneously active Alarm-S blocks	50
Time	
Real-time clock	Yes
• Backed-up	Yes
• Accuracy	See Section 1.1.6
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master
• On MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DPs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100

Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Standard communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Number of connection resources	12 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 11 from 1 to 11 1
– OP communication User-definable Default	max. 11 from 1 to 11 1
– S7 basic communication User-definable Default	max. 8 from 0 to 8 8
Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No

MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
Dimensions	
Assembly dimension B × H × T (mm)	80 × 125 × 130
Weight	Approx. 0.53 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection

Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 to 28.8 V
Current consumption (idle)	typical 7.0 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A Type B or C
PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 8 W
Battery	Yes
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	Yes
– at 0 to 25°C	Approx. 4 weeks
– at 40° C	Approx. 3 weeks
– at 60 ° C	Approx. 1 week
• Battery charging time	Approx. 1 hour

1.4.6 CPU 315-2 DP

DP master or DP slave

You can operate the CPU 315-2 DP on your 2nd interface (PROFIBUS-DP interface) as DP Master or DP Slave in a PROFIBUS-DP network.

For details on PROFIBUS-DP characteristics of CPU 315-2 DP refer to Chapter 2.

CPU 315-2 DP, Technical Data

CPU and Product Version	
MLFB	6ES7 315-2AF03-0AB0
• Hardware version	01
• Firmware version	V 1.1.0
• Matching programming package	*STEP 7* V 5.0; Service Pack 03
Memory	
Work memory	
• integral	64 KB
• Expandable	no
Load memory	
• integral	96 KB RAM
• Expandable FEPROM	Up to 4 MB
• Expandable RAM	no
Backup	Yes
• With battery	All data
• Without battery	4736 bytes
Processing times	
Processing times for	
• Bit instructions	0.3 µs minimum
• Word instructions	1 µs minimum
• Double integer math	2 µs minimum
• Floating-point math instructions	50 µs minimum
Timers/Counters and their retentive characteristics	
S7 counters	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB

S7 timers	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	4736 bytes
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	max. 255 (DB 0 reserved)
• Size	max. 16 KB
• Adjustable retentivity	8 DB; max. 4096 data bytes
• Preset	No retentivity
Local data (non-alterable)	max. 1536 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 16 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	4
FBs	max. 192
• Size	max. 16 KB
FCs	max. 192
• Size	max. 16 KB

Address areas (I/O)	
Peripheral address area, digital/analog	1 KB/1 KB (freely addressable)of these are
• distributed	1 KB/1 KB
Process image (cannot be customized)	128/128 bytes
Digital channels	max. 8192 (minus 1 byte diagnostic address per DP slave)/8192
• Centralized	max. 1024/1024
Analog channels	max. 512 (minus 1 byte diagnostic address per DP slave)/512
• Centralized	max. 256/128
Configuration	
Rack	max. 4
Modules per module rack	max. 8
Number of DP masters	
• integral	1
• via CP	1
S7 message functions	
Simultaneously active Alarm-S blocks	max. 50
Time	
Real-time clock	Yes
• Backed-up	Yes
• Accuracy	See Section 1.1.6
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master
• CP on MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100
Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes (server)
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Standard communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Number of connection resources	12 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 11 from 1 to 11 1
– OP communication User-definable Default	max. 11 from 1 to 11 1
– S7 basic communication User-definable Default	max. 8 from 0 to 8 8
Routing connections	max. 4

Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No
MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
2. Interface	
Functionality	
• DP Master	Yes
• DP Slave	Yes
– Status/Modify; Program; Routing	Yes, can be activated
• Direct data exchange	Yes
• Point-to-point connection	No
• Default setting	None
• Galvanically isolated	Yes
DP Master	
• Services	
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Activation/deactivation of DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	max. 64
• Address area	max. 1 KB I/1 Kbyte O
• User data per DP slave	max. 244 bytes I and 244 bytes O

DP Slave	
• Services	
– Status/Modify; Program via PROFIBUS Routing	Yes, can be activated
• Device master file	Sie3802f.gsg
• Transmission rate	... up to 12 Mbps
• Transfer memory	244 bytes I/244 bytes O
– Address areas	max. 32 with max. 32 bytes each
Dimensions	
Assembly dimension B × H × T mm (mm)	80 × 125 × 130
Weight	Approx. 0.53 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection
Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 to 28.8 V
Current consumption (idle)	typical 0.9 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, Type B or C
PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 10 W
Battery	Yes
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	Yes
– at 0 to 25°C	Approx. 4 weeks
– at 40° C	Approx. 3 weeks
– at 60 ° C	Approx. 1 week
• Battery charging time	Approx. 1 hour

1.4.7 CPU 316-2 DP

DP master or DP slave

You can operate the CPU 316-2 DP on your 2nd interface (PROFIBUS-DP interface) as DP Master or DP Slave in a PROFIBUS-DP network.

For details on PROFIBUS-DP characteristics of CPU 316-2 DP refer to Chapter 2.

CPU 316-2 DP, Technical Data

CPU and Product Version	
MLFB	6ES57 316-2AG00-0AB0
• Hardware version	01
• Firmware version	V 1.1.0
• Matching programming package	*STEP 7* V 5.0; Service Pack 03
Memory	
Work memory	
• integral	128 KB
• Expandable	no
Load memory	
• integral	192 KB
• Expandable FEPROM	Up to 4 MB
• Expandable RAM	no
Backup	Yes
• With battery	All data
• Without battery	4736 bytes
Processing times	
Processing times for	
• Bit instructions	0.3 µs minimum
• Word instructions	1 µs minimum
• Double integer math	2 µs minimum
• Floating-point math instructions	50 µs minimum
Timers/Counters and their retentive characteristics	
S7 counters	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB

S7 timers	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	4736 bytes
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 17
Clock memories	8 (1 memory byte)
Data blocks	511 (DB 0 reserved)
• Size	max. 16 KB
• Adjustable retentivity	max. 8 DB 4096 data bytes
• Preset	No retentivity
Local data (non-alterable)	max. 1536 bytes
• Per priority class	256 bytes
Blocks	
OBs	See Instruction List
• Size	max. 16 KB
Nesting depth	
• Per priority class	8
• additional levels within an error OB	4
FBs	max. 256
• Size	max. 16 KB
FCs	max. 256
• Size	max. 16 KB

Address areas (I/O)	
Peripheral address area, digital/analog	2 KB/2 KB (freely addressable)
• Distributed	2 KB/2 KB
Process image (cannot be customized)	128/128 bytes
Digital channels	max. 16384 (minus 1 byte diagnostic address per DP slave)/16384
• Centralized	max. 1024/1024
Analog channels	max. 1024 (minus 1 byte diagnostic address per DP slave)/1024
• Centralized	max. 256/128
Configuration	
Rack	max. 4
Modules per Rack	max. 8
Number of DP masters	
• integral	1
• via CP	1
S7 message functions	
Simultaneously active Alarm-S blocks	max. 50
Time	
Real-time clock	Yes
• Backed-up	Yes
• Accuracy	See Section 1.1.6
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master
• On MPI	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	
– Monitor Variables	max. 30
– Modify Variables	max. 14
Force	Yes
• Variable	Inputs, outputs
• Number	max. 10
Monitor block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (non-alterable)	100
Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	1
• Size of GD packets	max. 22 bytes
– Number of which consistent	8 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	32 bytes for X/I_PUT/_GET; 76 bytes for X_SEND/_RCV
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	32 bytes
S7-compatible communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Standard communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Number of connection resources	12 for PD/OP/S7 basic/S7 communication
• Reservation for	
– PD communication User-definable Default	max. 11 from 1 to 11 1
– OP communication User-definable Default	max. 11 from 1 to 11 1
– S7 basic communication User-definable Default	max. 8 from 0 to 8 8
Routing connections	max. 4

Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	No
• DP Slave	No
• Galvanically isolated	No
MPI	**No**
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	19.2; 187.5 Kbps
2. Interface	
Functionality	
• DP Master	Yes
• DP Slave	Yes
– Status/Modify; Program; Routing	Yes, can be activated
• Direct data exchange	Yes
• Point-to-point connection	No
• Default setting	None
• Galvanically isolated	Yes
DP Master	
• Services	
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Activation/deactivation of DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	max. 125
• Address area	max. 2 KB I/2 KB O
• User data per DP slave	max. 244 bytes I and 244 bytes O

DP Slave	
• Services	
– Status/Modify; Program; Routing	Yes, can be activated
• Device master file	Siem806f.gsg
• Transmission rate	Up to 12 Mbps
• Transfer memory	244 bytes I/244 bytes O
– Address areas	max. 32 with max. 32 bytes each
Dimensions	
Assembly dimension B × H × T (mm)	80 × 125 × 130
Weight	Approx. 0.53 kg
Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	8
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection
Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 to 28.8 V
Current consumption (idle)	typical 0.9A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, Type B or C
PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 10 W
Battery	Yes
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	Yes
• Clock back-up period	
– at 0 to 25°C	Approx. 4 weeks
– at 40° C	Approx. 3 weeks
– at 60 ° C	Approx. 1 week
• Battery charging time	Approx. 1 hour

1.4.8 CPU 318-2

Special Features

- 4 accumulators
- The configuration of MPI interfaces can be changed: MPI or PROFIBUS DP (DP Master).
- Configurable data areas (Process image, local data)

Information on differences between CPU 318-2 and other CPUs is found in Chapter 4.1.

DP master or DP slave

You can operate the CPU 318-2 DP as DP Master or DP Slave in a PROFIBUS-DP network. However, note that only one of the interfaces can be a DP Slave. For details on PROFIBUS-DP characteristics of CPU 318-2 DP refer to Chapter 2.

Definable Data Areas and Occupied Working Memory

In your CPU 318-2 configuration, you can change the size of the I/O process image and the local data areas.
Increasing default values for the process image and local data requires additional memory that would otherwise be available for user programs.
Take following dimensions into account:

- Input process image: 1 byte PII occupies 12 Byte in memory
  Output process image: 1 Byte PIO occupies 12 bytes in memory
  Example:
  256 bytes in PII occupy 3072 bytes,
  2047 byte in PIO already occupy 24564 bytes in memory.
- Local data 1 local data byte occupies 1 byte in memory
  256 byte is default, depending on the priority class. With 14 priority classes there are therefore 3584 bytes occupied in the working memory. With a maximum size of 8192 bytes you can still allocate 4608 bytes, which are then no longer available for the user program in the working memory.

Communication

You can transform the first CPU interface from MPI to DP interface operation. You can operate the CPU as DP Master or DP Slave on this DP interface. Routing reduces the maximum possible number of connections for each one of the two interfaces by one connection per active PG/OP communication used by the CPU 318-2 as network node.

FM 353/354, distributed

If you implement the CPU 318-2 as DP Master, you can operate FM 353 as of 6ES7 353-1AH01-0AE0, firmware version 3.4/03 and FM 354 as of 6ES7 354-1AH01-0AE0, firmware version 3.4/03 in distributed mode with an ET 200M.

You cannot operate the following modules in an S7-300 equipped with a 318-2 CPU

FM 357 up to 6ES7 357-4_H02-3AE_, firmware version 2.1;

FM NC up to 6FC5 250-3AX00-7AH0, firmware version 3.7 + Toolbox 6FC5 252-3AX2Z-6AB0, Software Version 3.6;

SM 338 up to 6ES7 338-7UH00-0AC0, version 07;

SIXWAREX M up to 7MH4 553-1AA41, firmware version 0119;

SINAUT ST7 TIM, 6NH7 800-_A__0 (Tip: Use a TIM module as stand alone node)

Peripheral access in CPU 318-2 is not permitted

for T PAW operations on centrally inserted peripheral modules with corresponding address bytes assigned to different peripheral modules.

CPU 318-2, Technical Data

CPU and Product Version	
MLFB	6ES7 318-2AJ00-0AB0
• Hardware version	03
• Firmware version	V 3.0
• Matching programming package	*STEP 7* V 5.1 + Service Pack 02
Memory	
Work memory	
• integral	256 KB data/ 256 KB code
• Expandable	no
Load memory	
• integral	64 KB
• Expandable FEPROM	Up to 4 MB
• Expandable RAM	Up to 2 MB
Backup	Yes
• With battery	All data
• Without battery	max. 11 KB
Processing times	
Processing times for	
• Bit instructions	0.1 µs minimum
• Word instructions	0.1 µs minimum
• Double integer arithmetic	0.1 µs minimum
• Floating-point arithmetic	0.6 µs minimum
Timers/Counters and their retentive characteristics	
S7 counters	512
• Adjustable retentivity	from C 0 to C 511
• Preset	from C 0 to C 7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
S7 timers	512
• Adjustable retentivity	from T 0 to T 511
• Preset	No retentive times
• Timing range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB

Data areas and their retentive characteristics	
Retentive data area as a whole (inc. flags, timers, counters)	max. 11 KB
Bit memories	8192
• Adjustable retentivity	MB 0 to MB 1023
• Preset	MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	2047 (DB 0 reserved)KB
• Size	max. 64 KB
• Adjustable retentivity	max. 8 DB, max. 8192 data bytes
• Preset	No retentivity
Local data (alterable)	max. 8192 bytes
• Preset	3584 bytes
• Per priority class	256 bytes (expandable to 8192 bytes)
Blocks	
OBs	See Instruction List
• Size	max. 64 KB
Nesting depth	
• Per priority class	16
• additional levels within an error OB	3
FBs	max. 1024
• Size	max. 64 KB
FCs	max. 1024
• Size	max. 64 KB
Address areas (I/O)	
Peripheral address area, digital/analog	max. 8 KB/8 KB (freely addressable)
• Distributed	
– MPI/DP Interface	max. 2 KB/2 KB
– DP interface	max. 8 KB/8 KB
Process image (configurable)	2048/2048 bytes
• Preset	256/256 bytes
Digital channels	max. 65536 (minus 1 byte diagnostic address per DP slave)/65536
• Centralized	max. 1024/1024
Analog channels	max. 4096/4096
• Centralized	max. 256/128

Configuration	
Rack	max. 4
Modules per module rack	max. 8
Number of DP masters	
• integral	2
• via CP	2
S7 message functions	
Simultaneously active Interrupt S function blocks and Interrupt D function blocks	max. 100
Time	
Real-time clock	Yes
• Backed-up	Yes
• Accuracy	See Section 1.1.6
Operating hours counter	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Clock synchronisation	Yes
• On PLC	Master/Slave
• via MPI	Master/Slave
• via DP	Master/Slave
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number	max. 70
Force	Yes
• Variable	Inputs, outputs, flags, peripheral inputs, peripheral outputs
• Number	max. 256
Monitor block	Yes
Single sequence	Yes
Breakpoint	4
Diagnostic buffer	
• Number of entries (non-alterable)	100
Communication functions	
PD/OP communication	Yes
Global data communication	Yes
• Number of GD packets	
– Sender	1
– Receiver	2
• Size of GD packets	54 bytes
– Number of which consistent	32 bytes
S7 basic communication	Yes
• User data per job	max. 76 bytes
– Number of which consistent	76 bytes
S7 communication	Yes (server)
• User data per job	max. 160 bytes
– Number of which consistent	Byte, Word, Double word
S7-compatible communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Standard communication	Yes (via CP and loadable FC)
• User data per job	Dependent on CP
– Number of which consistent	Dependent on CP
Interfaces	
1. Interface	
Functionality	
• MPI	Yes
• DP Master	Yes
• DP Slave	Yes
• Direct data exchange	Yes
• Default setting	MPI
• Electrically isolated	Yes
Number of connections	max. 32;
– Of these, the following are reserved:	1 PD connection 1 OP connection
MPI	
• Services	
– PD/OP communication	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes (server)
• Transmission rates	Up to 12 Mbps

DP Master	
• Services	
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Activation/deactivation of DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Address area	max. 2 KB I/2 KB O
• User data per DP slave	max. 244 bytes I and 244 bytes O

DP Slave	
• Services	
– Status/Modify; Program; Routing	Yes, can be activated
• Device master file	siem807f.gsg
• Transmission rate	Up to 12 Mbps
• Transfer memory	244 bytes I/244 bytes O

2. Interface	
Functionality	
• DP Master	Yes
• DP Slave	Yes
– Status/Modify; Program; Routing	Yes, can be activated
• Direct data exchange	Yes
• PtP Connection	No
• Default setting	None
• Galvanically isolated	Yes
Number of connections	max. 16
– Of these, the following are reserved:	1 PD connection 1 OP connection

DP Master	
• Services	
– PD/OP communication	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Activation/deactivation of DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	max. 125
• Address area	max. 8 KB I/8 KB O
• User data per DP slave	max. 244 bytes I and 244 bytes O

DP Slave	
• Services	
– Status/Modify; Program; Routing	Yes, can be activated
• GSD file	siem807f.gsg
• Transmission speed	Up to 12 Mbps
• Transfer memory	244 bytes I/244 bytes O

Dimensions	
Assembly dimension B × H × T (mm)	160 × 125 × 130
Weight	Approx. 0.93 kg

Programming	
Programming language	STEP 7
Stored instructions	See Instruction List
Nesting levels	16
System functions (SFCs)	See Instruction List
System function blocks (SFBs)	See Instruction List
User program security	Password protection

Voltages, Currents	
Power supply	24V DC
• Permissible range	20.4 V to 28.8 V
Current consumption (idle)	typical 1.2 A
Inrush current	typical 8A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, Type B or C
PD supply at MPI (15 to 30V DC)	max. 200 mA
Power losses	typical 12 W
Battery	Yes
• Backup margin at 25° C and continuous CPU buffering	min. 1 year
• Battery shelf life at 25°C	approx. 5 years
Accumulator	Yes
• Clock back-up period	
– at 0 to 25°C	Approx. 4 weeks
– at 40° C	Approx. 3 weeks
– at 60 ° C	Approx. 1 week
• Battery charging time	Approx. 1 hour

CPU 31x-2 as DP Master/DP Slave and Direct Communication

2

Introduction

In this chapter you will find the features and technical specifications of the CPUs 315-2 DP, 316-2DP and 318-2. You will need these in order to use the CPU as a DP master or a DP slave and configure it for direct communication.

Agreement: Since DP Master/Slave behavior is the same for all CPUs, the CPUs described below are referred to as CPU 31x-2.

Note on CPU 318-2: With a CPU 318-2 you can operate the MPI-/DP interface as DP interface. In this case, however, you can only configure it as DP Master and not as DP Slave.

In This Chapter

Additional Literature

Descriptions and notes on system configuration, configuration of a PROFIBUS subnet and on diagnostics in a PROFIBUS subnet is found in the *STEP 7* Online Help.

2.1 Information on DPV1 Functionality

The aim

The EN50170 Standard for Distributed Peripherals was subject to further development. All changes were incorporated in IEC 61158 / EN 50170, Volume 2, PROFIBUS. In order to simplify matters we now refer to DPV1 Mode.

How do I identify a DPV1 Master/Slave?

DP Master CPUs of the S7-400 family and the CPU 318-2, respectively with integrated DP interface, support DPV1 Master functionality as of Firmware Version 3.0.0.

DP Slaves, listed in the STEP 7 hardware catalog under their family name can be identified as DPV1 Slaves with the help of the info text. DP Slaves implemented in STEP 7 via GSD files support V1 functionality as of GSD Revision 3.

As of which STEP 7 version is migration to DPV1 mode possible?

As of STEP 7 V5.1, Servicepack 2.

Which operating modes are available for DPV1 modules?

You are using a DPV1 automation module, but do not want to migrate to DPV1 mode. In this case you use S7 compatible mode. In this mode, the automation module is compatible to EN50170. In this case, however, you cannot utilize full DPV1 functionality. You could, for example, use the new SFBs 52...54. However, default values are written to non-existing data.

You are using a DPV1 compatible automation module and want to migrate to DPV1 mode. In this case, use DPV1 mode for full functionality. In your station you can continue using automation modules not supporting DPV1 as usual.

Can I use all previous slaves after migration to DPV1 mode?

Yes, without restriction. The only difference here is that your previous slaves do not support extended DPV1 functions.

Can I use DPV1 Slaves without this migration?

Yes, without restriction. In this case, DPV1 Slaves behave as conventional Slaves. SIEMENS DPV1 Slaves can also be operated in S7 compatible mode. For DPV1 Slaves of other manufacturers you require a GSD file to EN50170 below Revision 3. DPV1 – station-wide.

You must convert the complete station to DPV1 mode if you migrate to DPV1. In STEP 7 you can configure this mode in the HW Config module (DP Mode).

Details on migration to DPV1 mode are found in our Customer Support under FAQ topic ID: 7027576

2.2 DP Address Areas of the CPUs 31x-2

Address areas of CPUs 31x-2

Address area	315-2 DP	316-2DP	318-2
DP address area for I/Os	1024 bytes	2048 bytes	8192 bytes
of these in the I/O process images	Bytes 0 to 127	Bytes 0 to 127	Bytes 0 to 255 (default) Can be set up to byte 2047

In the input address area, DP diagnostic addresses occupy 1 byte for the DP master and for each DP slave. Under these addresses, for example, you can call DP standard diagnostics for the respective nodes (LADDR parameter of SFC13). The DP diagnostic addresses are specified during configuration. If you do not specify any DP diagnostic addresses, *STEP 7* assigns these addresses, in decrements starting at the highest byte.

Configuring modules with addresses assigned to the peripheral area

Always configure a module address in a peripheral area either completely inside or completely outside of the process image. Otherwise, consistency is not ensured and corrupted data might be generated.

2.3 CPU 31x-2 as DP Master

Introduction

This section covers the features and technical specifications of the CPU when it is used as a DP master.

The features and technical specifications of the CPU 31x-2 as the “standard” CPU are listed in Section 1.

Prerequisite

Should the MPI/DP interface be a DP interface? If so, you must then configure the interface as a DP interface.

Before the CPU can be put into operation, it must be configured as a DP master. This means carrying out the following steps in *STEP 7* :

- Configure the CPU as a DP master.
- Assign a PROFIBUS address.
- Assign a master diagnostic address.
- Integrate DP slaves into the DP master system.

  Is a DP slave a CPU 31x-2?

  If so, you will find that DP slave in the PROFIBUS-DP catalog as “pre-configured station”. This DP slave CPU must be assigned a slave diagnostic address in the DP master. Interconnect the DP master and the DP slave CPU. Specify the address areas for data exchange with the DP slave CPU.

Status/Control, Programming via PROFIBUS

As an alternative to the MPI interface, you can program the CPU via PROFIBUS-DP interface or execute the PG’s status and control functions.

Note

The use of Monitor and Modify via the PROFIBUS-DP interface lengthens the DP cycle.

Equidistance

As of STEP 7 V 5.x you can configure bus cycles of the same length (equidistant) for PROFIBUS subnets. You can find a detailed description of equidistance in the STEP 7 online help system.

Power-Up of the DP Master System

CPU 31x-2DP is DP Master	CPU 318-2 is DP Master
You can also set power-up time monitoring of the DP slaves with the "Transfer of parameters to modules" parameter.	Using the parameters "Transfer of parameters to modules" and "Ready message from modules" you can set power-up time monitoring for the DP slaves.
This means that the DP slaves must be powered up and configured by the CPU (as DP master) in the set time.	

PROFIBUS Address of the DP Master

You cannot set the 126 as the PROFIBUS address for the CPU 31x-2.

2.4 Diagnostics of the CPU 31x-2 as DP Master

Diagnosis with LEDs

Table 2-1 describes the meaning of the BUSF LED.
For display the BUSF LED assigned to the PROFIBUS-DP interface is always it or it flashes.

Table 2-1 Meaning of the BUSF LED of the CPU 31x-2 as DP Master

BUSF	Description	Remedy
LED off	Configuring data OK; all configured slaves are addressable.	–
LED on	• Bus fault (hardware fault). • DP interface fault. • Different transmission rates in multiple DP master mode.	• Check for bus cable breaks or short-circuit. • Evaluate the diagnostic data. Reconfigure or correct the configuring data.
LED flashes	• Station failure. • At least one of the configured slaves cannot be addressed.	• Check the bus cable connection to the CPU31x-312, or check whether the bus is interrupted. • Wait until the CPU 31x-2 has powered up. If the LED does not stop flashing, check the DP slaves or evaluate the diagnostic data for the DP slaves.

Reading Diagnostic Data with STEP 7

Table 2-2 Reading Diagnostic Data with *STEP 7*

DP Master	Modules or registers in *STEP 7*	Application	See...
CPU 31x-2	”DP slave diagnostics” tab	Display slave diagnostic data as plain text on the *STEP 7* user interface	See “Diagnosis of Hardware” in the *STEP 7* Online Help and *STEP 7* User Manual
	SFC 13 “DPNRM_DG”	Reading out slave diagnosis (store in the data area of the user program)	Configuration for the CPU 31x-2, see Section 2.6.4; SFC, see *System and Standard Functions* Reference Manual Configuration for other slaves, see their description
	SFC 59 “RD_REC”	Read out data records of the S7 diagnosis (store in the data area of the user program)	*System and Standard Functions* Reference Manual
	SFC 51 “RDSYSST”	Read out system state sub-lists. In the diagnostics interrupt with the SSL ID W#16#00B4, call SFC51 and read out the SSL (system diagnostic list) of the slave CPU.	
	SFB 52 “RDREC” (only 318-2)	Applicable to DPV1 environment: Read out data records of the S7 diagnosis (store in the data area of the user program)	
	SFB 54 “RALRM” (only 318-2)	Applicable to DPV1 environment: Read out interrupt information within the corresponding interrupt OB	

Evaluating Diagnostics in the User Program

The following figures show you how to evaluate the diagnosis in the user program. Note the order number for the CPU 315-2DP:

CPU 315-2DP **<** 6ES7 315-2AF**03**-0AB0	CPU 315-2DP as of 6ES7315-2AF**03**-0AB0 CPU 316-2DP as of 6ES7316-2AG00-0AB0 CPU 316-2 as of 6ES7318-2AJ00-0AB0
...see Figure 2-1 on page 2-8	...see Figure 2-2 on page 2-9

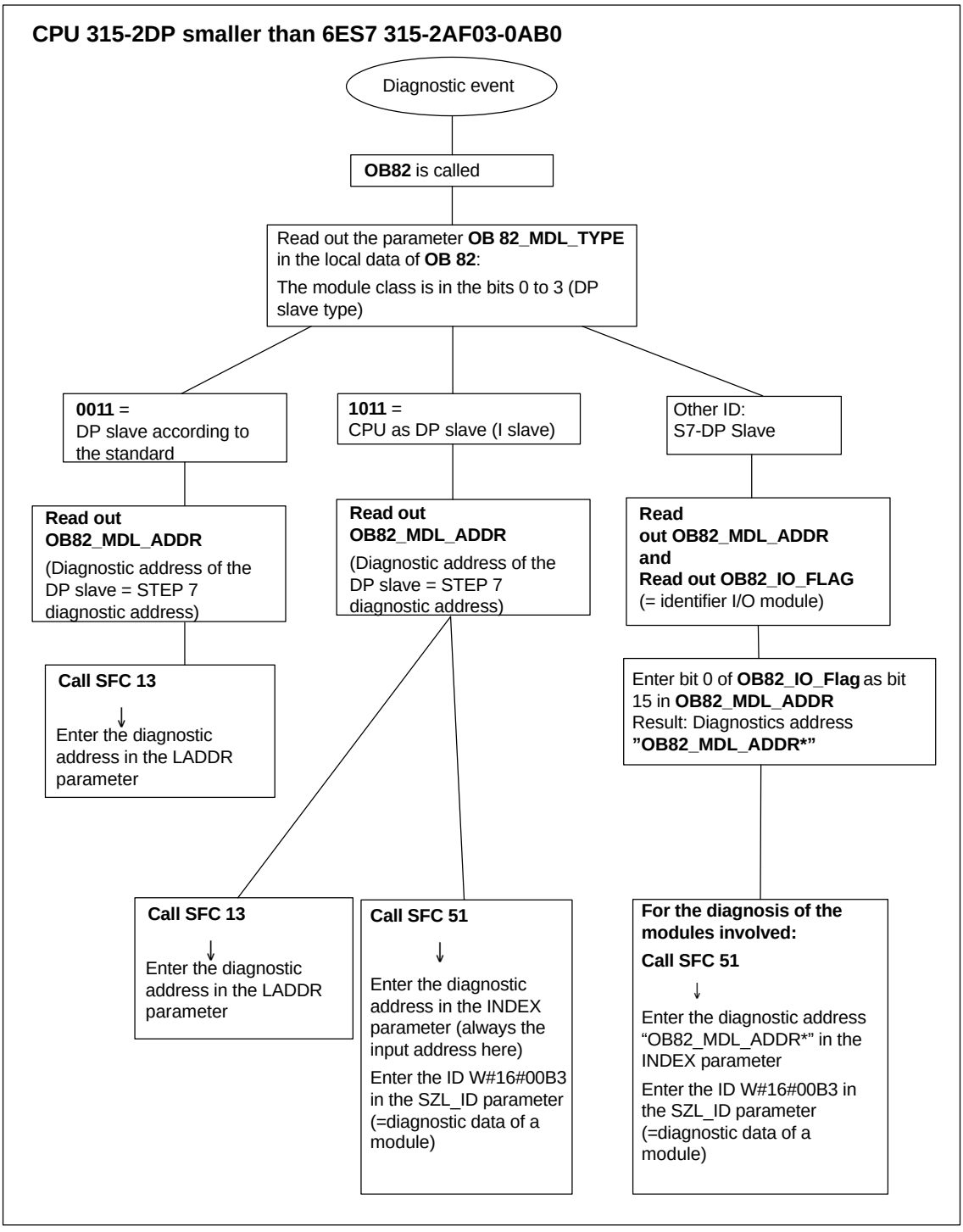


Figure 2-1 Diagnostics with CPU 315-2DP **<** 315-2AF**03**

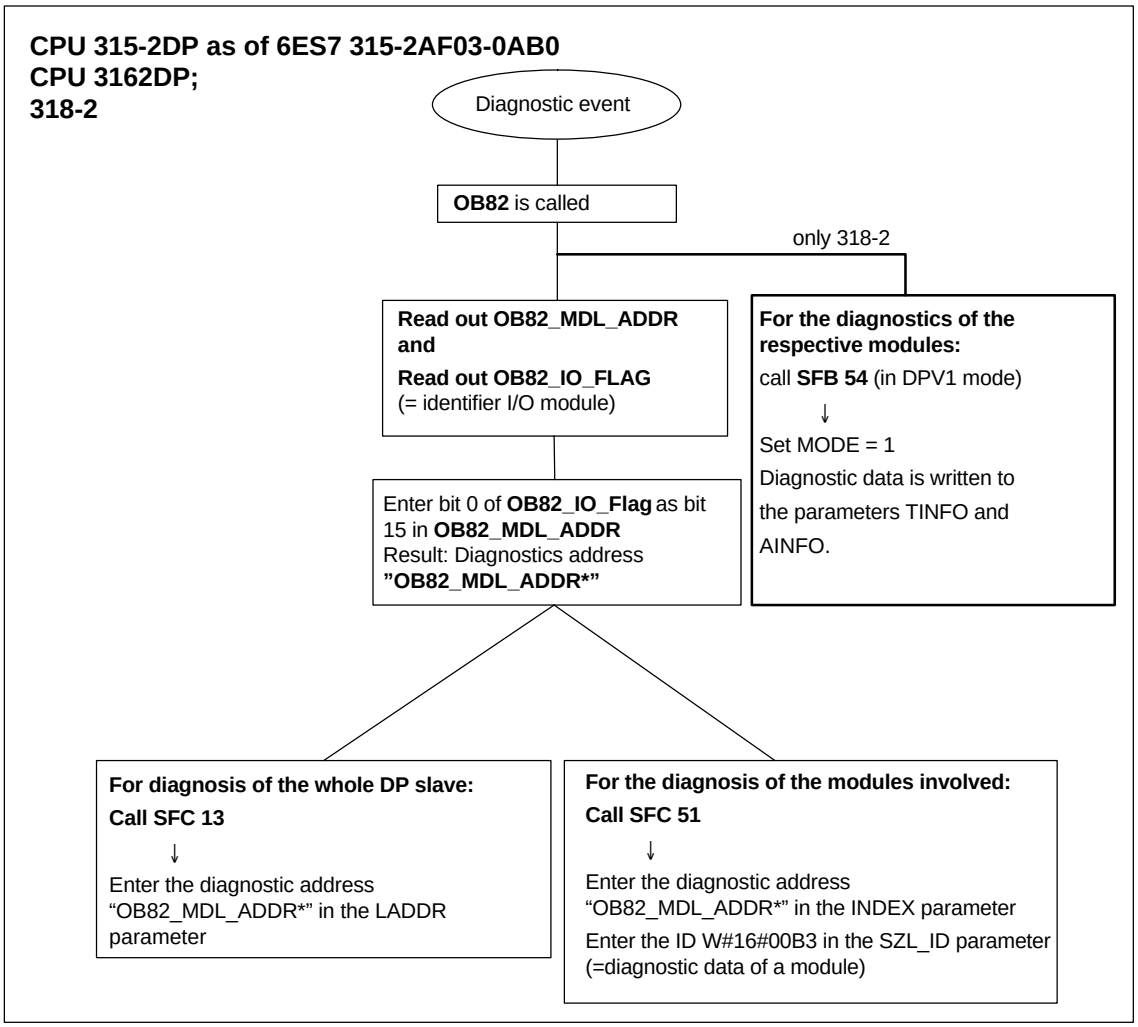


Figure 2-2 Diagnostics with CPU 31x-2 (315-2DP as of 315-2AF**03**)

Diagnostic Addresses

With a CPU 31x-2, you assign the diagnostic addresses for the PROFIBUS-DP. Make sure during configuration that DP diagnostic addresses are assigned to both the DP master and the DP slave.

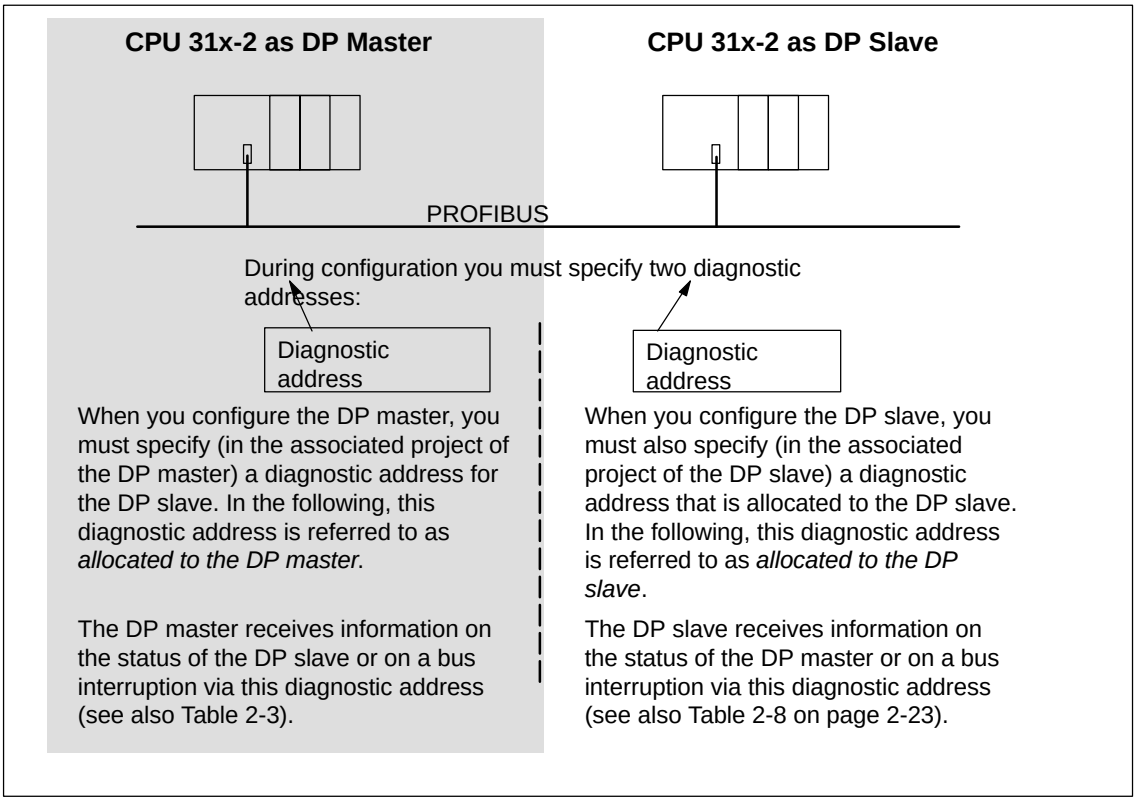


Figure 2-3 Diagnostic Addresses for DP Master and DP Slave

Event Detection

Table 2-3 shows how a DP Master CPU 31x-2 recognizes operating state transitions of a DP Slave CPU or or data transfer interrupts.

Table 2-3 Event Detection of the CPU 31x-2 as DP Master

Event	What Happens in the DP Master
Bus interruption (short-circuit, plug disconnected)	• OB 86 is called and a *station failure* reported (incoming event; Diagnostic address of the DP slave, assigned to the DP master) • on peripheral access: Call of OB 122 (Peripheral access error)
DP Slave RUN → STOP	• OB 82 is called and *Module fault* reported (incoming event; Diagnostic address of the DP slave assigned to the DP master; Variable OB82_MDL_STOP=1)
DP Slave STOP → RUN	• Call of OB82 with the message *Module OK.* (outgoing event; Diagnostic address of the DP slave assigned to the DP master; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

Table 2-4 shows you how you can, for example, evaluate RUN-STOP transitions of the DP slave in the DP master (see Table 2-3).

Table 2-4 Evaluating RUN-STOP Transitions of the DP Slaves in the DP Master

In the DP Master		In the DP Slave (CPU 31x-2DP)
Diagnostic Addresses Example: Master diagnostic address =**1023** Slave diagnostic address in the master system =**1022**		Diagnostic Addresses Example: Slave diagnostic address =**422** Master diagnostic address = not relevant
The CPU calls OB 82 with the following information: • OB 82_MDL_ADDR:=**1022** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=Module fault Tip: The CPU's diagnostic data buffer also contains this information In your user program, you should also program SFC13 "DPNRM_DG" to fetch diagnostic data from the DP Slave. We recommend you use SFB54 when operating in **DPV1 mode**. It outputs complete interrupt information.	←	CPU: RUN → STOP CPU generates a DP slave diagnostic frame (see Section 2.6.4).

2.5 CPU 31x-2 as DP-Slave

Introduction

This section lists the characteristics and technical specifications for the CPU when it is operated as a DP slave.

The characteristics and technical specifications of the CPU as the “standard” CPU can be found in Section 1.

Prerequisite

Should the MPI/DP interface be a DP interface? If so, you must then configure the interface as a DP interface.

Prior to startup, the CPU must be configured as a DP slave. This means carrying out the following steps in *STEP 7*:

- “Switch on” the CPU as DP slave.
- Assign a PROFIBUS address.
- Assign a slave diagnostic address.
- Specify the address areas for data exchange with the DP Master.

Device Master Files

You need a device master file to configure the CPU 31x-2 as a DP slave in a DP master system.
COM PROFIBUS as of V 4.0 includes the GSD file.

If you are working with an older version or another configuration tool, you can get the device master file from the following sources:

- On the Internet at http://www.ad.siemens.de/csi_e/gsd

or

- Via modem from the **SSC** (Interface Center) Fuerth by calling 0911/911/737972.

Configuration and parameter assignment message frame

STEP 7 provides support for the configuration and parameter assignment of 31x-2 CPUs. If you require a description of the configuration and parameter assignment message frame, for example, to carry out a check using a bus monitor, refer to the Internet URL http://www.ad.siemens.de/simatic-cs, article ID 1452338.

Status/Control, Programming via PROFIBUS

As an alternative to the MPI interface, you can program the CPU via PROFIBUS-DP interface or execute the PG's Status and Control functions . To do so, you must enable these functions when configuring the CPU as a DP slave in *STEP 7*.

Note

The use of Monitor and Modify via the PROFIBUS-DP interface lengthens the DP cycle.

Data Transfer Via Transfer Memory

The CPU 31x-2 operating as DP Slave provides a transfer memory for PROFIBUS DP. The data transfer between the CPU as DP slave and the DP master always takes place via this intermediate memory. Here you can configure up to 32 address areas.

That is, the DP Master writes its data to the address areas of the transfer memory while the CPU's user program fetches these data and vie versa.

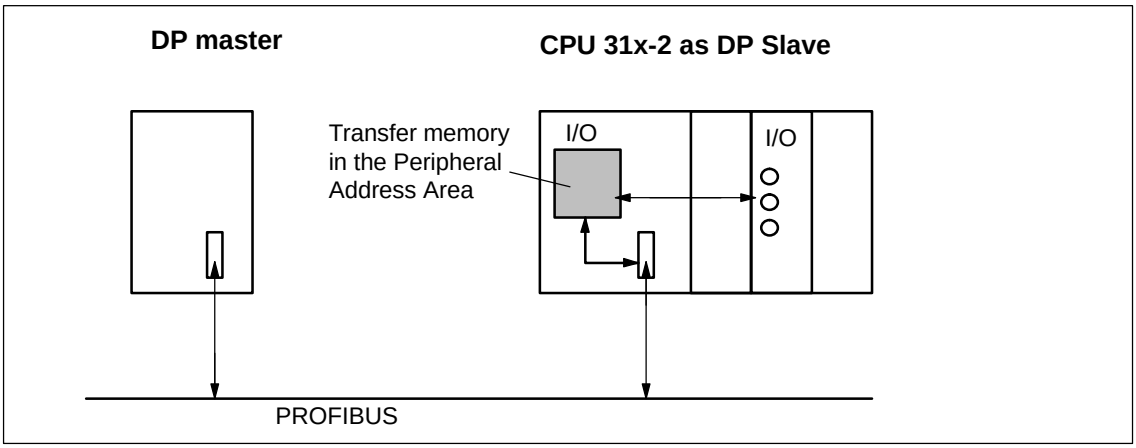


Figure 2-4 Transfer Memory in a CPU 31x-2 operating as DP Slave

Address areas of the transfer memory

Configure the I/O address areas in *STEP 7*:

- you can configure up to 32 I/O address areas
- the maximum length of each one of these address areas is 32 bytes
- You can configure a maximum of 244 bytes for inputs and 244 bytes for outputs.

The table below shows the principle of address areas. You can also find this figure in the *STEP 7* configuration.

Table 2-5 Example of an address area configuration for transfer memory

	Type	Master Address	Type	Slave Address	Length	Unit	Consistency
1	E	222	A	310	2	Byte	Unit
2	A	0	E	13	10	Word	Total length
:							
32							
	Address areas in the DP Master CPU		Address areas in the DP Slave CPU		These address area parameters must be the same for both the DP Master and DP Slave		

Rules

The following rules must be followed when using the intermediate memory:

- Address area assignment:
  - Input data of the DP slave are **always** output data of the DP master
  - Output data of the DP slave are **always** input data of the DP master
- The addresses can be freely allocated. In the user program, access the data with Load/Transfer statements or with SFCs 14 and 15. You can also specify addresses from the I/O process images.

Note

Transfer memory addresses are assigned from the DP address area of the CPU 31x-2.

Do not assign transfer memory addresses to the I/O modules in the CPU 31x-2!

- The lowest address represents the start address of the respective address area.
- Length, unit and consistency of DP Master/Slave address areas related to each other must be identical.

S5 DP Master

If you are using an IM 308 C as a DP master and the CPU 31x-2 as a DP slave, the exchange of consistent data requires the following:

In the IM 308 C, you must program FB 192 to enable the exchange of consistent data between DP master and DP slave. FB192 outputs/fetches all CPU 31x-2 data in a single block!

S5-95 as a DP master

If you are using an AG S5-95 as a DP master, you must also set its bus parameters for the CPU 31x-2 as a DP slave.

Sample Program

Below you will see a small sample program for the exchange of data between DP master and DP slave. The addresses used in the example are those from Table 2-5.

In the DP Slave CPU	In the DP Master CPU

`L 2 Data`
`T MB 6 pre-processing`
`L EB 0 in DP slave`
`T MB 7`
 	
`L MW 6 Forward data to`
`T PAW 310 DP master`	

	`L PEB 222 Further`
	`T MB 50 processing of`
	`L PEB 223 received data in`
	`L B#16#3 the DP master`
	`+ I`
	`T MB 51`

	`L 10 Data Processing`
	`+ 3 in DP master`
	`T MB 60`
	
	`CALL SFC 15 Send data to DP`
	`LADDR:= W#16#0 slave`
	`RECORD:= P#M60.0 Byte 20`
	`RET_VAL:= 22 MW`

`CALL SFC 14 Receive data`
`LADDR:=W#16#D from DP master`
`RET_VAL:=MW 20`
`RECORD:=P#M30.0 Byte 20`	

`L MB 30 Further`
`L MB 7 processing of`
`+ I received data`
`T MW 100`	

Data Transfer in STOP Mode

The DP-Slave CPU goes into STOP: Data in the CPU's transfer memory are overwritten with "0", that is, the DP Master reads "0".

The DP Master goes into STOP: Current data in the CPU's transfer memory are retained and can still be fetched by the CPU.

PROFIBUS address

You cannot set the 126 as the PROFIBUS address for the CPU 31x-2.

2.6 Diagnosis of the CPU 31x-2 operating as DP-Slave

In This Section

2.6.1 Diagnosis with LEDs

Diagnostics with LED displays - CPU 31x-2

Table 2-6 explains the meaning of the BUSF LEDs.
The BUSF LED assigned to the interface configured as the PROFIBUS-DP interface will always come on or flash.

Table 2-6 Meaning of the BUSF LEDs in the CPU 31x-2 as DP Slave

BUSF	Description	Remedy
LED off	Configuring OK.	–
LED flashes	The CPU 31x-2 is incorrectly configured. There is no data interchange between the DP master and the CPU 31x-2. Reasons: • Timeout. • Bus communication via PROFIBUS interrupted. • Incorrect PROFIBUS address.	• Check the CPU 31x-2. • Check whether the bus connector is plugged in properly. • Check for interruptions in the bus cable to the DP master. • Check configuring data and parameters.
LED on	• Bus short-circuit	• Check the bus configuration.

2.6.2 Diagnostics with *STEP 5* or *STEP 7*

Slave Diagnosis

The slave diagnosis complies with EN 50170, Volume 2, PROFIBUS. Depending on the DP master, the diagnosis can be read for all DP slaves that comply with the standard, using *5 STEP5* or *7 STEP 7*.

The following sections describe how the slave diagnosis is read and structured.

S7 Diagnosis

An S7 diagnosis can be requested for all the modules in the SIMATIC S7/M7 range of modules in the user program. The structure of the S7 diagnostic data is the same for both central and distributed modules.

The diagnostic data of a module is in data records 0 and 1 of the system data area of the module. Data record 0 contains 4 bytes of diagnostic data describing the current state of a module. Data record 1 also contains module-specific diagnostic data.

You can find out how to configure the diagnostic data in the *System and Standard Functions* Reference Manual.

2.6.3 Reading Out the Diagnostic Data

Table 2-7 Fetching diagnostic data with *STEP 5* and *STEP 7* in the master system

Programmable Controller with DP Master	Modules or registers in *STEP 7*	Application	See...
SIMATIC S7/M7	"DP Slave Diagnostics" tab	Display slave diagnostic data as plain text on the *STEP 7* user interface	See "Diagnosis of Hardware" in the *STEP 7* Online Help and *STEP 7* User Manual
	SFC 13 "DP NRM_DG"	Reading out slave diagnosis (store in the data area of the user program)	See Section 2.6.4; SFC: see *System and Standard Functions* Reference Manual
	SFC 51 "RDSYSST"	Read out system state sublists. In the diagnostics interrupt with the SSL ID W#16#00B4, call SFC51 and read out the SSL (system diagnostic list) of the Slave CPU.	*System and Standard Functions* Reference Manual
	SFB 54 "RDREC" (only 318-2)	Applicable to DPV1 environment: Read out interrupt information within the corresponding interrupt OB	*System and Standard Functions* Reference Manual
SIMATIC S5 with IM 308-C operating as DP Master	FB 192 "IM308C"	Reading out slave diagnosis (store in the data area of the user program)	See Section 2.6.4; for FBs refer to the *Distributed I/O System ET200* Manual 200
SIMATIC S5 with S5-95U PLC operating as DP Master	FB 230 "S_DIAG"		

Example of fetching Slave diagnostic data with FB192 “IM 308C”

Here you will find an example of how to use FB192 to fetch slave diagnostic data of a DP slave in the 192 *STEP 5* user program.

Assumptions

The following assumptions are made for this *STEP 5* user program:

- IM 308-C, operating as DP Master, occupies frames 0 ... 15 (number 0 of IM 308-C).
- The DP Slave has the PROFIBUS address 3.3
- The slave diagnostic data should be written to DB20. You can also use any data block for this.
- The slave diagnosis consists of 26 bytes.

STEP 5 Use Program

```
STL                                 Description
        :A      DB 30
        :SPA    FB 192
Name    :IM308C
DPAD    :       KH F800             Default address area of IM 308-C
IMST    :       KY 0, 3             IM no. = 0, PROFIBUS address of the DP slave = 3
FCT     :       KC SD               Function: Read Slave diagnostic data
GCGR    :       KM 0                Not evaluated
TYPE    :       KY 0, 20            S5 Data area: DB 20
STAD    :       KF +1               Diagnostic data, starting at Data Word 1
LENG    :       KF 26               Length of diagnostic data = 26 bytes
ERR     :       DW 0                Error code area in DW 0 of DB30
```

Example of reading out S7 diagnostic data with SFC59 “RD_REC”

Here you will find an example of how to use SFC59 to fetch S7 diagnostic data records for a DP Slave in the *STEP 7* user program. Reading out the slave diagnostic data with SFC13 is similar.

Assumptions

The following assumptions are made for this *STEP 7* user program:

- The diagnosis for the input module with the address 200_H is to be read.
- Data record 1 is to be read out.
- Data record 1 is to be stored in DB 10.

STEP 7 User Program

```
STL                                  Description

CALL SFC 59

REQ     :=TRUE                       Request to Read
IOID    :=B#16#54                    Identifier of the Address Area, here the I/O input
LADDR   :=W#16#200                   Logical address of the module
RECNUM  :=B#16#1                     Data record 1 is to be read out
RET_VAL :=                           Errors result in the output of an error code
BUSY    :=TRUE                       Reading process is not finished
RECORD  :=DB 10                      Destination area for the read data record 1 is data
                                     block 10
```

Diagnostic Addresses

With a CPU 31x-2, you assign the diagnostic addresses for the PROFIBUS-DP. Make sure during configuration that DP diagnostic addresses are assigned to both the DP master and the DP slave.

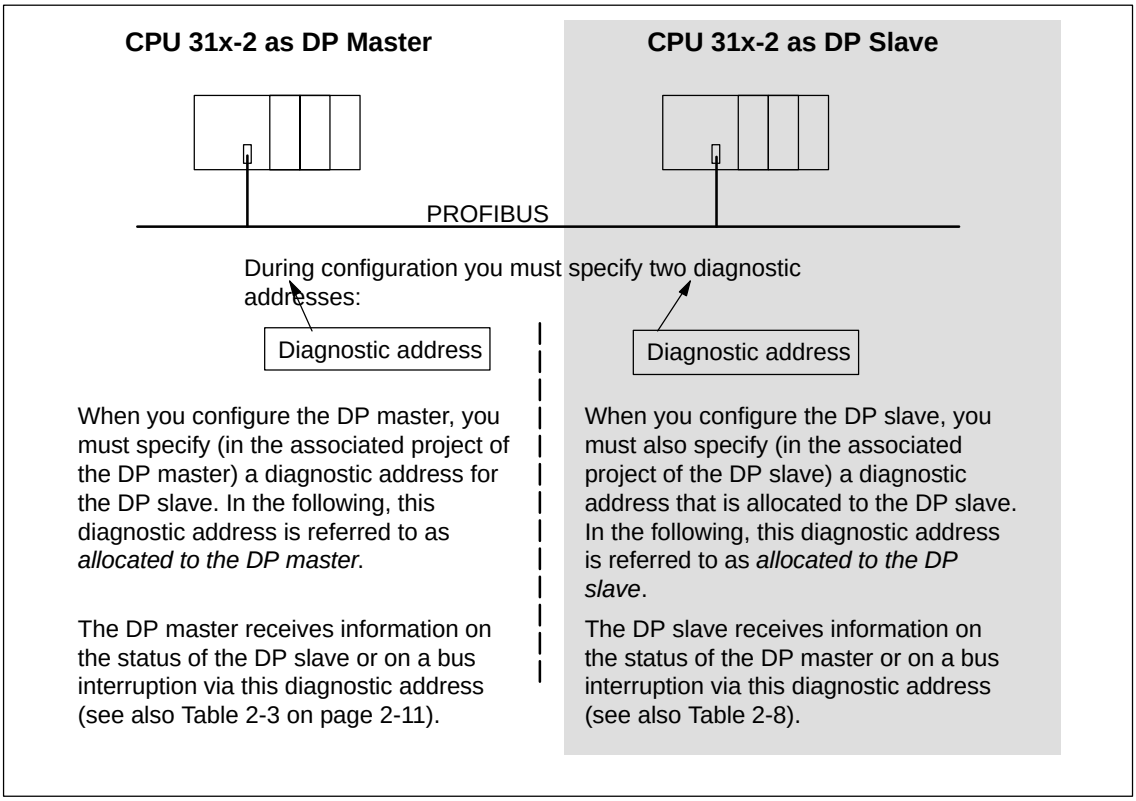


Figure 2-5 Diagnostic Addresses for DP Master and DP Slave

Event Detection

Table 2-8 shows how a DP Master CPU 31x-2 recognizes operating state transitions of a DP Slave CPU or or data transfer interrupts.

Table 2-8 Event Detection of the CPU 31x-2 as DP Slave

Event	What Happens in the DP Slave
Bus interruption (short-circuit, plug disconnected)	• OB 86 is called and a *station failure* reported (incoming event; diagnostic address of the DP slave assigned to the DP slave) • on peripheral access: Call of OB 122 (Peripheral access error)
DP Master: RUN → STOP	• OB 82 is called and *Module fault* reported (incoming event; diagnostic address of the DP slave assigned to the DP slave) Variable OB82_MDL_STOP=1)
DP Master: STOP → RUN	• Call of OB82 with the message *Module OK.* (outgoing event; diagnostic address of the DP slave assigned to the DP slave) Variable OB82_MDL_STOP=0)

Evaluation in the User Program

Table 2-9 shows you how you can, for example, evaluate RUN-STOP transitions of the DP master in the DP slave (see Table 2-8).

Table 2-9 Evaluating RUN-STOP Transitions in the DP Master/DP Slave

In the DP Master	In the DP Slave
Diagnostic Addresses Example: Master diagnostic address =**1023** Slave diagnostic address in the master system =**1022**	Diagnostic Addresses Example: Slave diagnostic address =**422** Master diagnostic address = not relevant
CPU: RUN → STOP →	The CPU calls OB 82 with the following information: • OB 82_MDL_ADDR:=**422** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=Module fault Tip: The CPU's diagnostic data buffer also contains this information

2.6.4 Format of the Slave Diagnostic Data

Structure of Slave Diagnostics

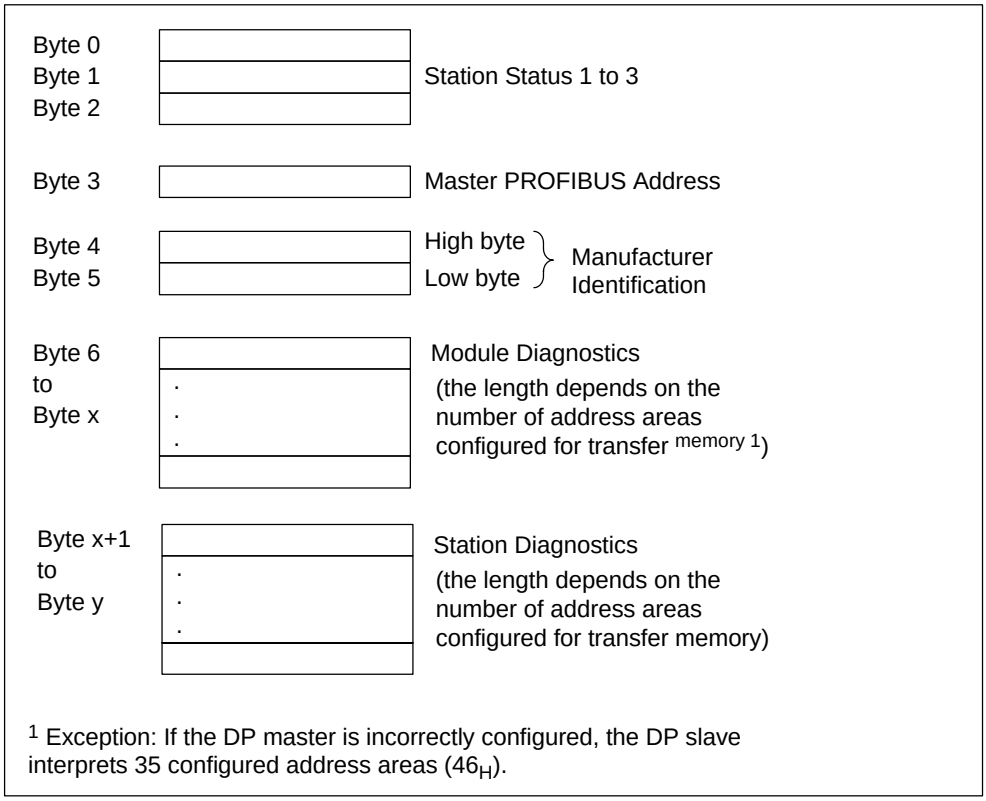


Figure 2-6 Format of the Slave Diagnostic Data

2.6.5 Station Status 1 to 3

Definition

Station status 1 to 3 provides an overview of the status of a DP slave.

Station Status 1

Table 2-10 Structure of Station Status 1 (Byte 0)

Bit	Description	Remedy
0	1: DP slave **cannot** be addressed by DP master.	• Is the correct DP address set on the DP slave? • Bus connector plugged in? • Does the DP slave have power? • RS 485 Repeater setting OK? • Execute a Reset on the DP slave.
1	1: DP slave is not ready for data interchange.	• Wait; the DP slave is still doing its run-up.
2	1: The configuration data which the DP master sent to the DP slave do not correspond with the DP slave's actual configuration.	• Was the software set for the right station type or the right DP slave configuration?
3	1: Diagnostic interrupt, generated by a RUN/STOP transition on the CPU 0: Diagnostic interrupt, generated by a STOP/RUN transition on the CPU	• You can read out the diagnostic data.
4	1: Function is not supported, for instance changing the DP address at the software level.	• Check the configuring data.
5	0: This bit is always "0".	-
6	1: DP slave type does not correspond to the software configuration.	• Was the software set for the right station type? (parameter assignment error)
7	1: DP slave was configured by a different DP master to the one that currently has access to it.	• Bit is always "1" when, for instance, you are currently accessing the DP slave via the PG or a different DP master. The DP address of the master that configured the slave is located in the "Master PROFIBUS address" diagnostic byte.

Station Status 2

Table 2-11 Structure of Station Status 2 (Byte 1)

Bit	Meaning
0	1: New parameter assignment and configuration of the DP Slave is required.
1	1: A diagnostic message has arrived. The DP slave cannot continue operation until the error has been rectified (static diagnostic message).
2	1: This bit is always “1” when there is a DP slave with this DP address.
3	1: The watchdog monitor has been activated for this DP slave.
4	0: This bit is always “0”.
5	0: This bit is always “0”.
6	0: This bit is always “0”.
7	1: DP slave is deactivated, that is to say, it has been removed from the scan cycle.

Station Status 3

Table 2-12 Structure of Station Status 3 (Byte 2)

Bit	Description
0 to 6	0: These bits are always “0”.
7	1: • More diagnostic messages have arrived than the DP slave can buffer. • The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.

2.6.6 Master PROFIBUS Address

Definition

The DP address of the DP Master is written to the diagnostic byte Master PROFIBUS address:

- The master that has configured the DP slave
- The master that has read and write access to the DP slave

Master PROFIBUS Address

Table 2-13 Structure of the Master PROFIBUS Address (Byte 3)

Bit	Description
0 to 7	DP address of the DP master that configured the DP slave and has read/write access to that DP slave.
	FF_H: DP slave was not configured by a DP master.

2.6.7 Manufacturer ID

Definition

The manufacturer identification contains a code specifying the DP slave's type.

Manufacturer Identification

Table 2-14 Structure of the Manufacturer Identification (Bytes 4 and 5)

Byte 4	Byte 5	Manufacturer Identification for
80_H	$2F_H$	CPU 315-2 DP
80_H	$6F_H$	CPU 316-2 DP
80_H	$7F_H$	CPU 318-2

2.6.8 Module Diagnostics

Definition

ID related diagnostics specifies in which one of the configured address areas of transient memory an entry was made.

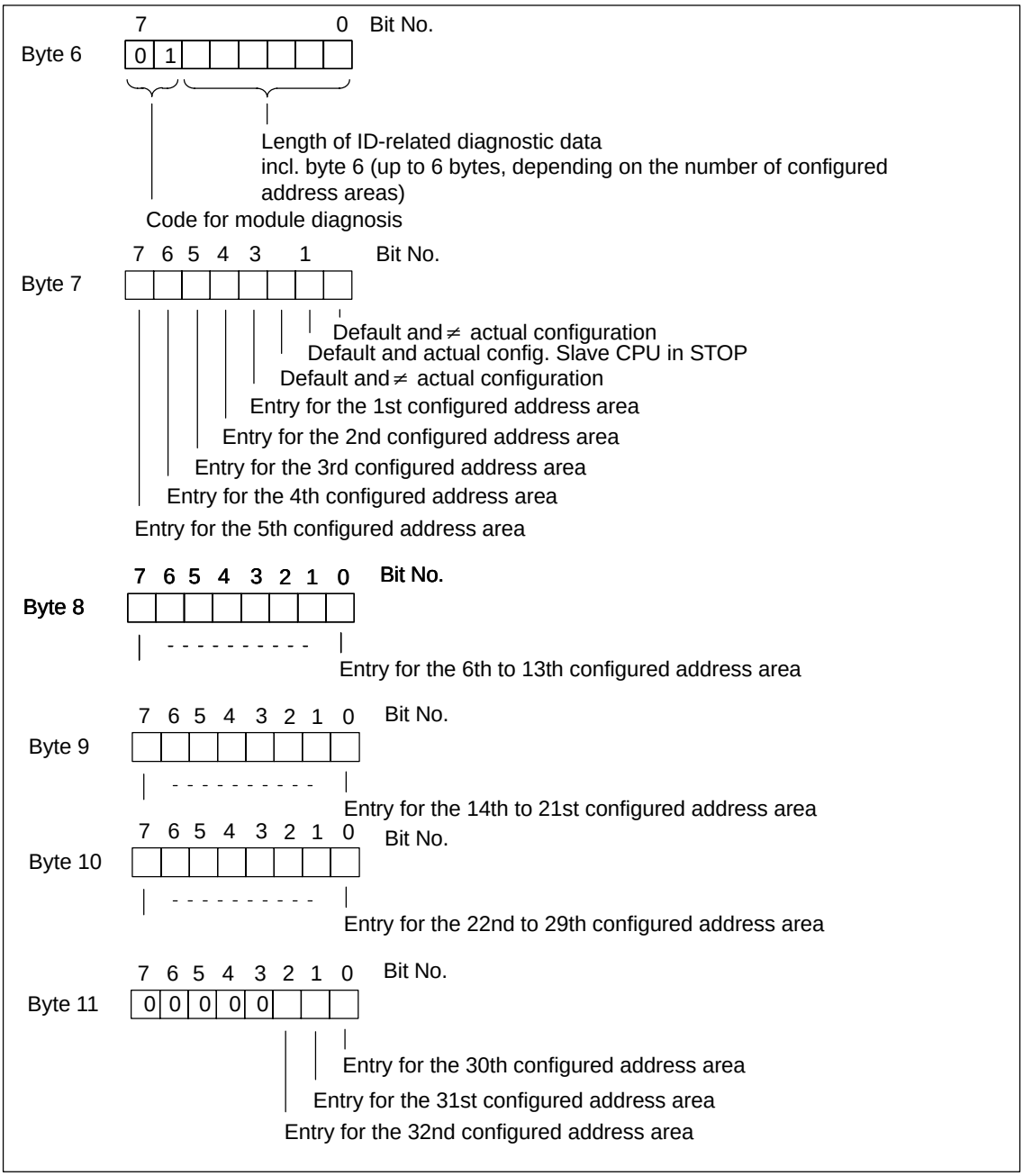


Figure 2-7 Structure of the Module Diagnosis of the CPU 31x-2

2.6.9 Station Diagnostics

Definition

Device diagnostics provides details on a DP Slave. The station diagnosis begins as of byte x and can have a maximum of 20 bytes.

Station Diagnostics

The figure below describes the structure and content of the bytes for a configured address area in transfer memory.

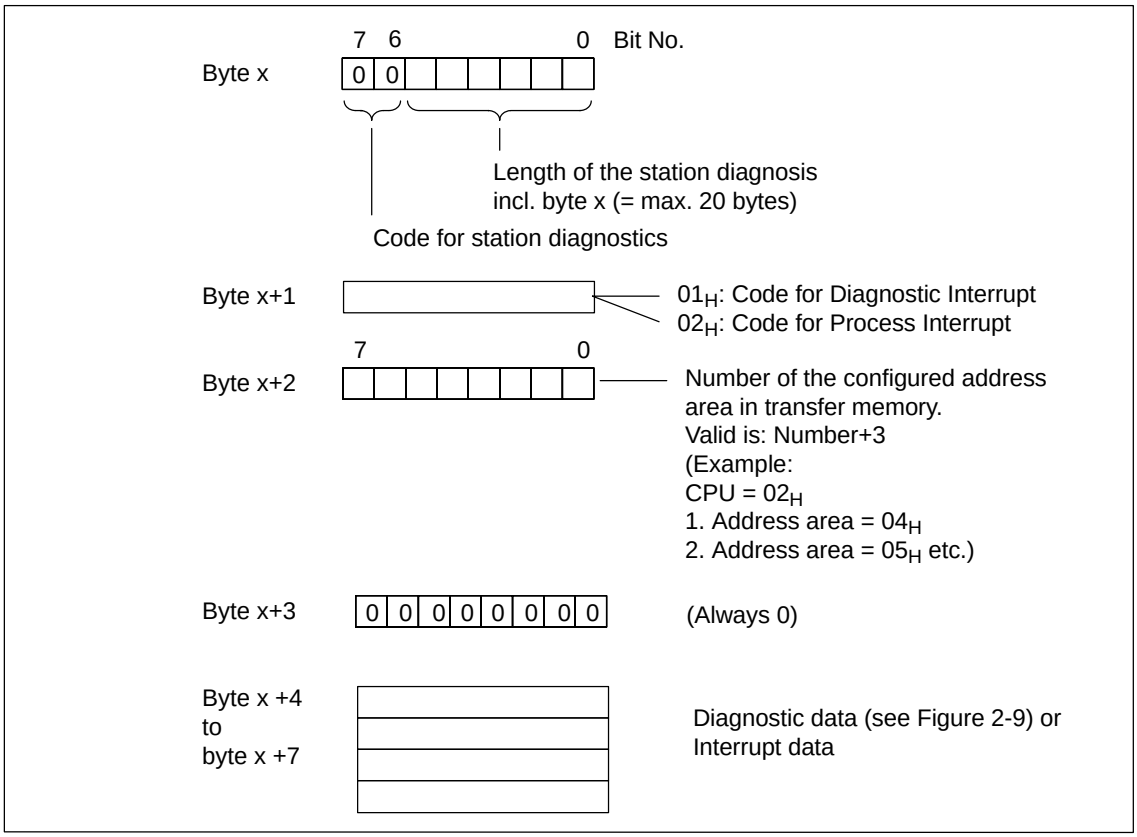


Figure 2-8 Structure of the Station Diagnosis

As of byte x +4

The purpose of the bytes beginning with byte x+4 depends on byte x+1 (see Figure 2-8).

Byte x+1 Contains the Code for...	
Diagnostic Interrupt (01_H)	**Hardware interrupt (02_H)**
The diagnostic data contains the 16 bytes of status information from the CPU. Figure 2-9 shows the contents of the first four bytes of diagnostic data. The next 12 bytes are always 0.	You can freely program 4 interrupt information bytes for the process interrupt. In *STEP 7*, transfer these bytes with SFC 7 “DP_PRAL” to the DP Master (refer to Chapter 2.6.10).

Bytes x+4 to x+7 for Diagnostic Interrupts

Figure 2-9 shows the structure and content of bytes x +4 to x +7 for the diagnostic interrupt. The contents of these bytes correspond to the contents of data record 0 of the diagnostic data in *STEP 7* (in this case, not all bits are assigned).

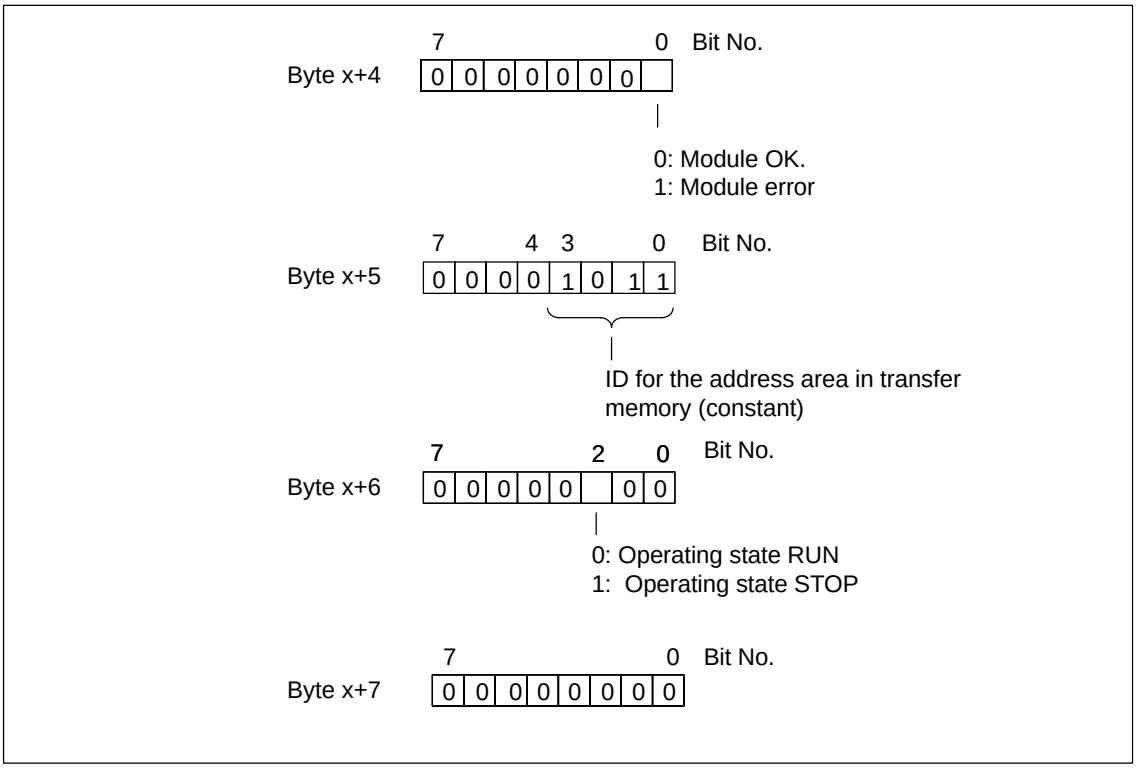


Figure 2-9 Byte x +4 to x +7 for Diagnostic and Hardware interrupt

2.6.10 Interrupts

Interrupts with S7/M7 DP Master

You can trigger a process interrupt at the DP Master in the user program of a CPU 31x-2 operating as DP Slave. A call of SFC 7 “DP_PRAL” triggers an OB40 in the user program of the DP Master. SFC 7 allows you to forward interrupt information in a DWORD to the DP master; this information can then be evaluated in OB 40 in variable OB40_POINT_ADDR. You can program the interrupt information as desired. A detailed description of SFC 7 “DP_PRAL” can be found in the reference manual entitled *System Software S7-300/400 - System and Standard Functions*.

Interrupts with Another DP Master

If you are running the CPU 31x-2 with another DP master, these interrupts are reflected in the station diagnosis of the CPU 31x-2. You must post-process the relevant diagnostic events in the DP master’s user program.

Note

When evaluating diagnostic/process interrupts with another DP Master via device-specific diagnostics, take into consideration:

- The DP master should be able to store the diagnostic messages, that is, the DP master should have a ring buffer in which to place these messages. If the DP master can not store diagnostic messages, only the last diagnostic message would be available for evaluation.
- You must scan the relevant bits in the device-related diagnostic data in your user program at regular intervals. You must also take the PROFIBUS-DP’s bus cycle time into consideration so that you can scan the bits at least once in sync with the bus cycle time, for example.
- With an IM 308-C operating as DP Master, you cannot use process interrupts in a device-specific diagnosis because only incoming interrupts are reported, rather than outgoing interrupts.

2.7 Direct Data Exchange

As of *STEP 7* V 5.x you can configure “Direct Data Exchange” for your PROFIBUS nodes. The CPU 31x-2 can take part in direct communication as the sender or receiver.

“Direct communication” is a special communication relationship between PROFIBUS-DP nodes.

Principle

Direct communication is characterized by the fact that the PROFIBUS-DP nodes “listen in” to find out which data a DP slave is sending back to its DP master. Using this function the eavesdropper (receiver) can directly access changes in the input data of remote DP slaves.

In your configuration with *STEP 7*, specify via respective peripheral input addresses the address area of the receiving station to which requested send data is fetched.

A CPU 31x-2 can be:

Transmitter operating	as DP Slave
Receiver operating	as DP Slave or DP Master, or as CPU that is not tied into a master system (see Figure 2-10).

Example:

Figure 2-10 shows an example of the direct communication “relationships” you can configure. The figure shows all DP Masters and DP Slaves as CPU 31x-2. Note that other DP Slaves (ET 200M, ET 200X, ET 200S) can only operate as transmitters.

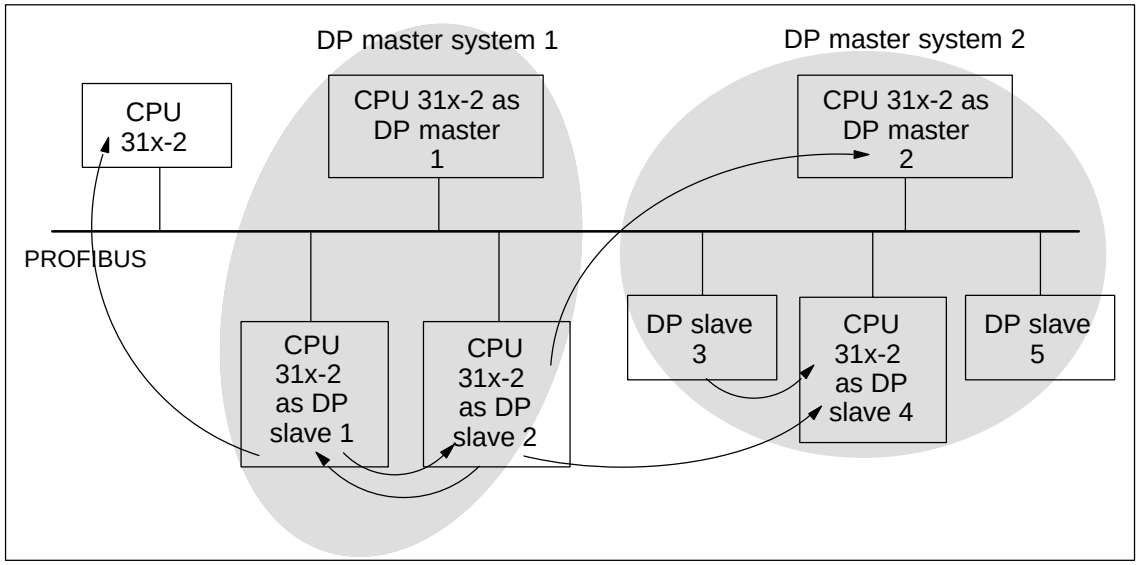


Figure 2-10 Direct Communication using CPU 31x-2

2.8 Diagnosis with Direct Communication

Diagnostic Addresses

With direct communication you allocate a diagnostic address on the receiver:

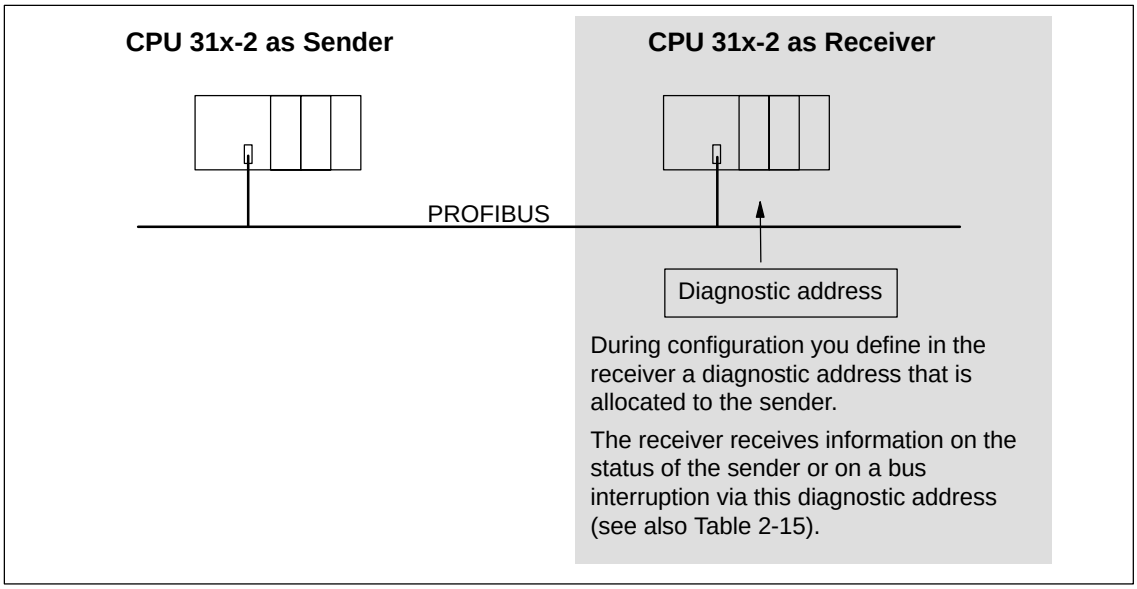


Figure 2-11 Diagnostic address for receiver with direct communication

Event Detection

Table 2-15 shows how a CPU 31x-2 operating as receiver recognizes data transmission errors.

Table 2-15 Event Detection by CPU 31x-2 Acting as Receiver in Direct Communication

Event	What Happens in the Receiver
Bus interruption<FJ>(short-circuit, plug disconnected)	• OB 86 is called and a *station failure* reported (incoming event; diagnostic address of the receiver, assigned to the sender) • on peripheral access: Call of OB 122 <FJ>(Peripheral access error)

Evaluation in the User Program

Table 2-16 shows you how you can, for example, evaluate the station failure of the sender in the receiver (see also Table 2-15).

Table 2-16 Evaluation of the Station Failure of the Sender During Direct Communication

In the Sender	In the Receiver
Diagnostic Addresses Example:<FJ> Master diagnostic address =**1023**<FJ> Slave diagnostic address in the master<FJ> system =**1022**	Diagnostic address: (Example) Diagnostic address =**444**
Station failure →	The CPU calls OB 86 with the following information: • OB 86_MDL_ADDR:=**444** • OB86_EV_CLASS:=B#16#38 (incoming event) • OB86_FLT_ID:=B#16#C4 (failure of a DP station) Tip: The CPU's diagnostic data buffer also contains this information

Cycle and Reaction times

3

Introduction

In this section, we explain what the cycle time and the response time of the S7-300 consist of.

You can use the programming device to read the cycle time of your user program (see the *STEP 7 online help system*).

The example below shows you how to calculate the cycle time.

The response time is more important for the process. In this chapter we will show you in detail how to calculate the response time.

In This Section

Execution times

- for the *STEP 7* instructions processed by the CPU
- for the SFCs/SFBs integrated in the CPUs
- for IEC functions you can call in *STEP 7*

can be found in the *S7300 Instruction List*

3.1 Cycle time

Cycle Time – A Definition

The cycle time is the time that elapses during one program cycle.

Component Parts of the Cycle Time

The cycle time comprises:

Factors	Remarks
Operating system execution time	See Section 3.2
Process image transfer time (PII and PIO)	
User program execution time	Can be calculated on the basis of the execution times of the individual instructions (see the *S7-300 Instruction List*) and a CPU-specific factor (see Table 3-3)
S7 timer (not in the case of the CPU318-2)	See Section 3.2
PROFIBUS DP	
Integrated functions	
Communication via the MPI	You configure the maximum permissible cycle load produced by communication in percent in *STEP 7*
Loading through interrupts	See Sections 3.4 and 3.5

Figure 3-1 shows the component parts of the cycle time

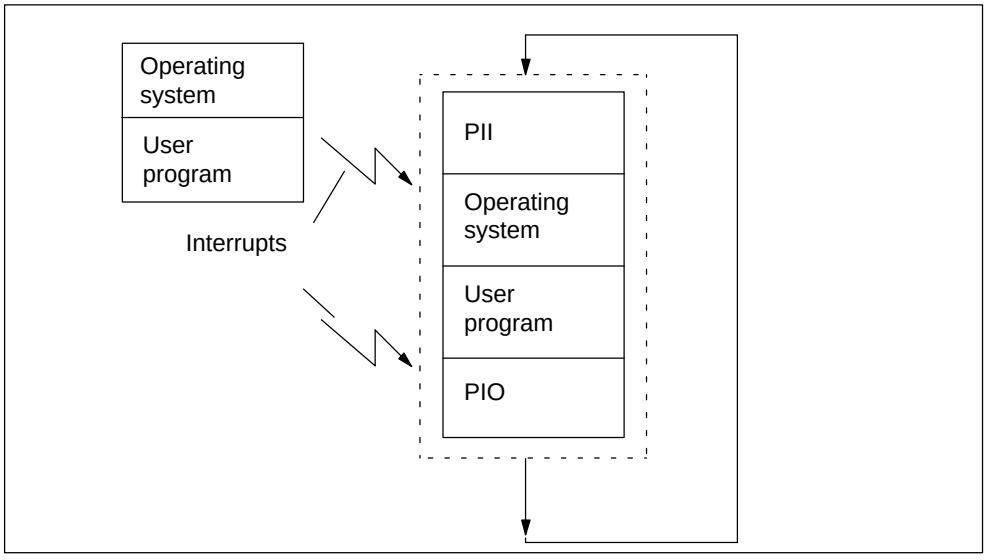


Figure 3-1 Component Parts of the Cycle Time

Extending the Cycle Time

Note that the cycle time of a user program is extended by the following:

- Time-controlled interrupt handling
- process interrupt processing (also refer to Chapter 3.4)
- Diagnostics and error handling (see also Section 3.4)
- Communication via MPI

3.2 Response Time

Response Time – A Definition

The response time is the time between detection of an input signal and modification of an associated output signal.

Factors

The response time depends on the cycle time and the following factors:

Factors	Remarks
Delay of the inputs and outputs	The delay times are given in the technical specifications • In the *Module Specifications* Reference Manual for the signal modules • In Chapter1.4.1 for the integrated I/O of the CPU 312 IFM. • In Chapter1.4.4 for the integrated inputs/outputs of the CPU 314 IFM.
Additional bus runtimes on the PROFIBUS subnet	CPU 31x-2 DP only

Range of Fluctuation

The actual response time lies between a shortest and a longest response time. You must always reckon on the longest response time when configuring your system.

The shortest and longest response times are considered below to let you get an idea of the width of fluctuation of the response time.

Shortest Response Time

Figure 3-2 shows you the conditions under which the shortest response time is reached.

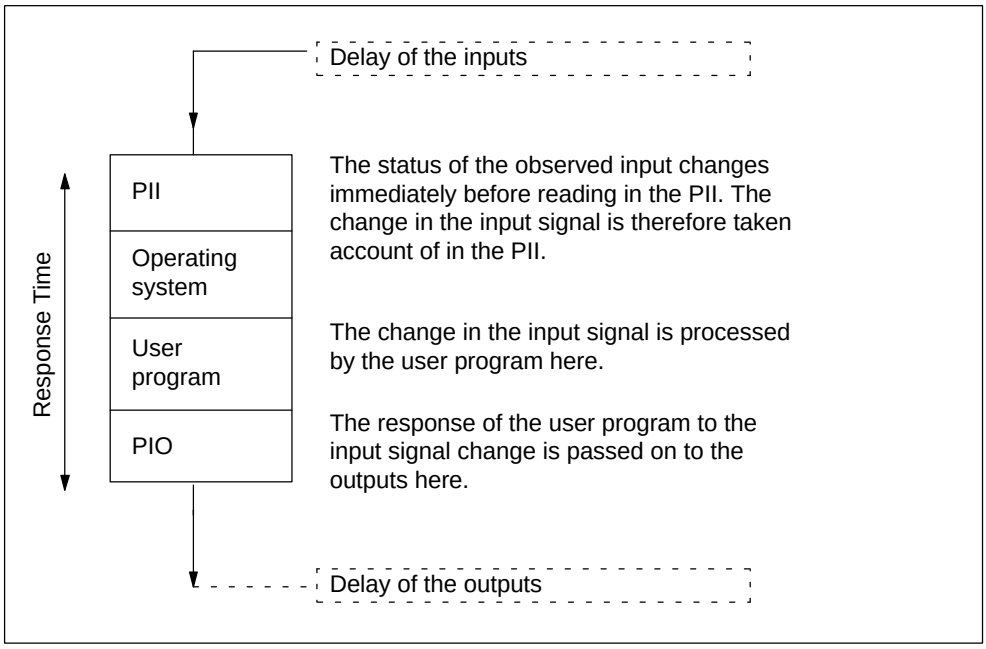


Figure 3-2 Shortest Response Time

Calculation

The (shortest) response time consists of the following:

- 1 × Process image transfer time of the inputs +
- 1 ×operating system execution time +
- 1 × Program execution time +
- 1 ×Process image transfer time of outputs +
- Execution time of S7 timer
- Delay of the inputs and outputs

This corresponds to the sum of the cycle time and the delay of the inputs and outputs.

Longest Response Time

Figure 3-3 shows the conditions that result in the longest response time.

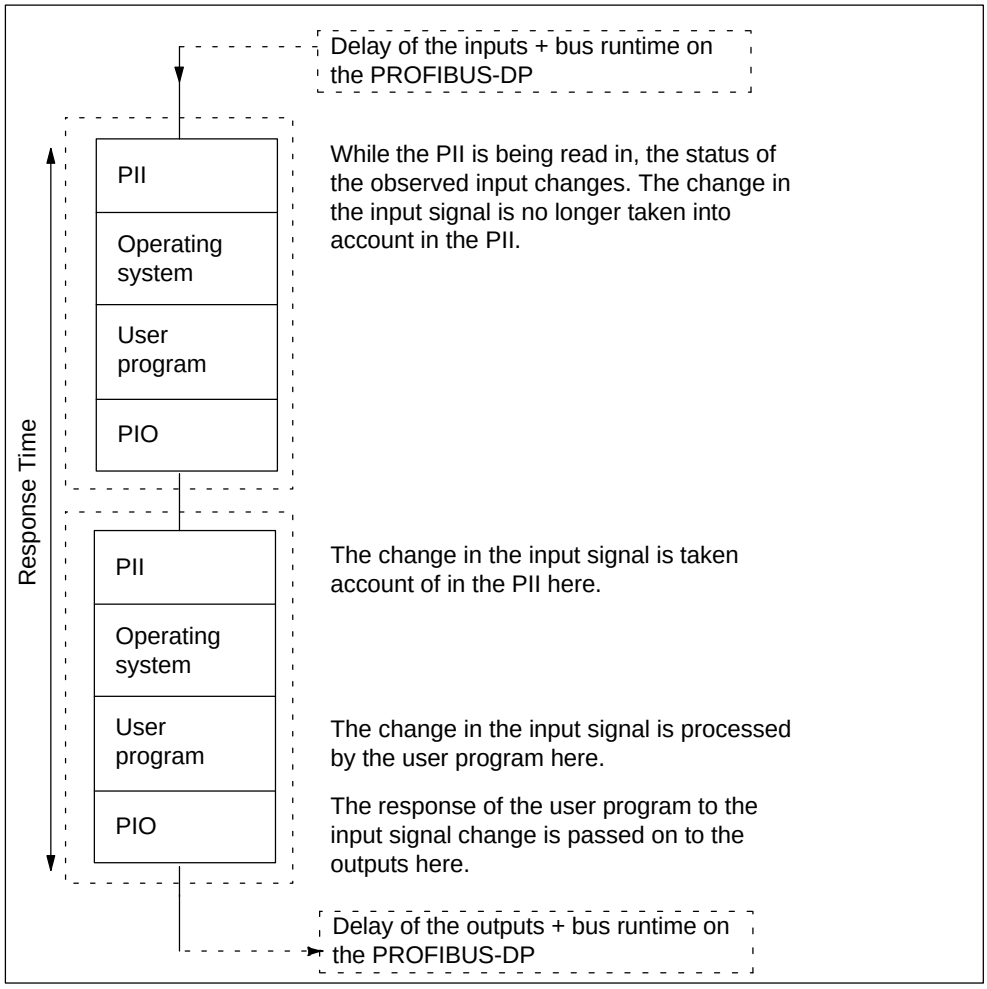


Figure 3-3 Longest Response Time

Calculation

The (longest) response time consists of the following:

- 2 × Process image transfer time of inputs +
- 2 × Process image transfer time of outputs +
- 2 × Operating system execution time+
- 2 × program execution time+
- 2 × Bus runtime on the PROFIBUS-DP bus system (with CPU 31x-2 DP)
- Execution time of the S7 timer+
- Delay of the inputs and outputs

This corresponds to the sum of the double cycle time and the delay of the inputs and outputs plus the double bus runtime.

Operating System Processing Time

Table 3-1 contains all the times needed to calculate the operating system processing times of the CPUs.

The times listed do not take account of

- Test functions, e.g. monitor, modify
- Functions: Load block, delete block, compress block
- Communication

Table 3-1 Operating System Processing Times of the CPUs

Sequence	CPU 312 IFM	CPU 313	CPU 314	CPU 314 IFM	CPU 315	CPU 315-2 DP	CPU 316-2 DP	CPU 318-2
Cycle control	600 to 1200 ms	540 to 1040 ms	540 to 1040 ms	770 to 1340 ms	390 to 820 ms	500 to 1030 ms	500 to 1030 ms	200 µs

Process Image Update

Table 3-2 contains the CPU times for process image updates (Process image transfer time). The times specified are “ideal values” which are prolonged by interrupts or by communication of the CPU.
(Process image = PI)

The time required by the CPU time for a process image update is calculated by

K + number of bytes in the PI of module rack “0” × A
+ number of bytes in the PI of module racks “1 to 3“ × B
+ number of bytes in the PI via DP × D
= Process image transfer time

Table 3-2 Process image update of the CPUs

	Components	CPU 312 IFM	CPU 313	CPU 314	CPU 314 IFM	CPU 315	CPU 315-2 DP	CPU 316-2 DP	CPU 318-2
K	Base load	162µs	142µs	142µs	147µs	109µs	10µs	10µs	20µs
A	For each byte in rack “0”	14.5µs	13.3µs	13.3µs	13.6µs	10.6µs	20µs (per word)	20µs (per word)	6 µs
B	For each byte in racks “1 to 3”	16.5µs	15.3µs	15.3µs	15.6µs	12.6µs	22µs (per word)	22µs (per word)	12.4µs
D	For each byte in DP area for integrated DP interface	–	–	–	–	–	12µs (per word)	12µs (per word)	1µs

User Program Processing Time:

The user program processing time is made up of the sum of the execution times for the instructions and the SFB/SFCs called up. These execution times can be found in the Instruction List. Additionally, you must multiply the user program processing time by a CPU-specific factor. This factor is listed in Table 3-3 for the individual CPUs.

Table 3-3 CPU-specific Factors for the User Program Processing Time

Se-quence	CPU 312 IFM	CPU 313	CPU 314	CPU 314 IFM	CPU 315	CPU 315-2DP	CPU 316-2 DP	CPU 318-2
Factor	1.23	1.19	1.15	1.15	1.15	1.19	1.19	1.0

S7 timers

In the case of the CPU 318-2, the updating of the S7 timers does not extend the cycle time.

The S7 Timer is updated every 10 ms.
You can find out in Section 3.3 how to include the S7 timers in calculations of the cycle and response times.

Table 3-4 Updating the S7 Timers

Sequence	312 IFM	313	314	314 IFM	315	315-2DP	316-2DP
Updating the S7 timers (every 10 ms)	Number of simultaneously active S7 timers × 10 µs	Number of simultaneously active S7 timers × 8 ms					

PROFIBUS-DP interface

In the case of the CPU 315-2 DP/316-2DP, the cycle time is typically extended by 5% when the PROFIBUS-DP interface is used.

In the case of the CPU 318-2, there is no increase in cycle time when the PROFIBUS-DP interface is used.

Integrated Functions

With CPU 312-IFM and 314-IFM operation the cycle time increases by a maximum of 10% when using integrated functions. Also take into consideration a possible instance DB update during the cycle checkpoint.

Table 3-5 shows the update times of the instance DB at the scan cycle checkpoint, together with the corresponding SFB runtimes.

Table 3-5 Update Time and SFB Runtimes

CPU 312 IFM/314 IFM	Update Time of the Instance DB at the Scan Cycle Checkpoint	SFB Runtime
IF Frequency Measurement (SFB 30)	100 µs	220 µs
IF Counting (SFB 29)	150 µs	300 µs
IF Counting (Parallel counter) (SFB 38)	100 µs	230 µs
IF Positioning (SFB 39)	100 µs	150 µs

Delay of the Inputs and Outputs

You must take account of the following delay times, depending on the module:

- For digital inputs: The input delay time
- For digital outputs: Negligible delay times
- For relay outputs: Typical delay times of between 10 ms and 20 ms.

  The delay of the relay outputs depends, among other things, on the temperature and voltage.
- For analog inputs: Cycle time of the analog input
- For analog outputs: Response time of the analog output

Bus Runtimes in the PROFIBUS Subnet

If you have used *STEP 7* to configure your PROFIBUS subnet, *STEP 7* calculates the expected normal bus cycle time. On the PG you can then view the bus cycle time of your configuration (refer to the *STEP 7* User Manual).

An overview of the bus runtime is provided in Figure 3-4. In this example, we assume that each DP slave has an average of 4 bytes of data.

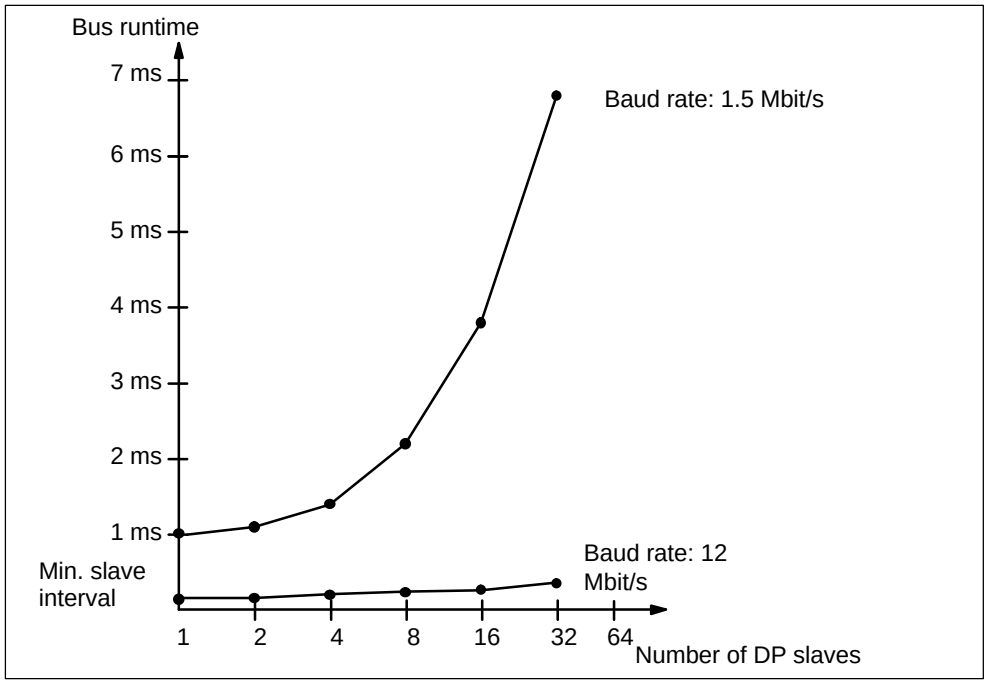


Figure 3-4 Overview of the Bus Runtime on PROFIBUS-DP at 1.5 Mbps and 12Mbps

Take the bus cycle time into consideration for every master when operating a PROFIBUS subnet with more than one master. That is, bus cycle time total = bus cycle time $\times$ number of masters.

Extending the Cycle by Nesting Interrupts

Table 3-6 shows typical extensions of the cycle time through nesting of an interrupt. The program runtime at the interrupt level must be added to these. If several interrupts are nested, the corresponding times need to be added.

Table 3-6 Extending the Cycle by Nesting Interrupts

Interrupts	312 IFM	313	314	314 IFM	315	315-2 DP	316-2DP	318-2
Hardware <FJ>interrupt	approx. 840 µs	approx. 700 µs	approx. 700 µs	approx. 730 µs	approx. 480 µs	approx. 590 µs	approx. 590 µs	approx. 340ms
Diagnostic interrupt	–	approx. 880 µs	approx. 880 µs	approx. 1000 µs	approx. 700 µs	approx. 860 µs	approx. 860 µs	approx. 450 µs
Time–of–day interrupt	–	–	approx. 680 µs	approx. 700 µs	approx. 460 µs	approx. 560 µs	approx. 560 µs	approx. 350 µs
Delay interrupt	–	–	approx. 550 µs	approx. 560 µs	approx. 370 µs	approx. 450 µs	approx. 450 µs	approx. 260 µs
Watchdog interrupt	–	–	approx. 360 µs	approx. 380 µs	approx. 280 µs	approx. 220 µσ	approx. 220 µσ	approx. 260 µs
Programming/ access error/ program execution error	–	approx. 740 µs	approx. 740 µs	approx. 760 µs	approx. 560 µs	approx. 490 µs	approx. 490 µs	approx. 130/ 155/ 285 µs

3.3 Calculation Examples for Cycle Time and Response Time

Component Parts of the Cycle Time

As a reminder: The cycle time comprises:

- process image transfer time +
- operating system processing time +
- user program processing time +
- Processing time of S7 timers

Sample Configuration 1

You have configured an S7-300 with the following modules on one rack:

- 1 CPU 314
- 2 SM 321 DI 32DC 24 V digital input modules (4 bytes each in the PI)
- 2 SM 322 DO 32 × DC 24 V/0.5A (4 bytes each in the PI)

According to the Instruction List, the user program has a runtime of 1.5 ms. There is no communication.

Calculation

In this example, the cycle time is calculated from the following times:

- Process image transfer time

  Input process image: 147 µs + 8 bytes × 13.6 µs = approx. **0.26 ms**

  Output process image: 147 µs + 8 bytes 13.6 µs = approx. **0.26 ms**
- Operating system cycle time

  Cycle control: approx. **1 ms**
- User program processing time:

  approx. 1.5 ms CPU specific factor 1.15 = approx. **1.8 ms**
- Processing time of S7 timers

  Assumption: 30 S7 timers are running.

  For 30 S7 timers, the one-off update takes

  30 × 8 µs = 240 µs.

  Process image transfer time + operating system processing time + user program cycle time results in this time interval:

  0.26 ms + 0.26 ms + 1 ms + 1.8 ms = 3.32 ms.

  Since the S7 timers are called every 10 ms, a maximum of one call can be made in this time interval, i.e. the S7 timers might increase cycle time by a maximum of 240 µs (= 0.24 ms)

The cycle time is calculated from the sum of the listed times:

Cycle time = 0.26 ms + 0.26 ms + 1 ms + 1.8 ms + 0.24 ms **= 3.56 ms.**

Parts of the Response Time

As a reminder, the response time is formed by the sum of:

- 2 × Process image transfer time of inputs +
- 2 × Process image transfer time of outputs +
- 2 × operating system cycle time+
- 2 ×program cycle time+
- Processing time of the S7 timers +
- Delay times of the inputs and outputs

Tip: Simple calculation: calculated cycle time × 2 + delay times.

Thus, for example one applies: 3.34 ms × 2 + timers
the I/O modules.

Sample Configuration 2

You have configured an S7-300 with the following modules on two racks:

- 1 CPU 314
- 4 SM 321 DI 32DC 24 V digital input modules (4 bytes each in the PI)
- 3 SM 322 DO 16 DC 24 V/0.5A (2 bytes each in the PI)
- 2 SM 331 AI 8×12 bits (not in the process image)
- 2 SM 332 AI 4×12 bits (not in the process image)

User program

According to the Instruction List, the user program has a runtime of 2 ms. By taking into account the CPU-specific factor of 1.15, the resulting runtime is approx. 2.3 ms. The user program operates up to 56 S7 timers simultaneously. No activities are required at the scan cycle checkpoint.

Calculation

In this example, the response time is calculated from the following times:

- Process image transfer time

  Input process image: 147 µs + 16 bytes 13.6 µs = approx. **0.36 ms**

  Output process image: 147 µs + 6 bytes 13.6 µs = approx. **0.23 ms**
- Operating system execution time

  Cycle control: approx. **1 ms**
- User program processing time: **2.3 ms**

- **1. Intermediate calculation:** Timebase for the calculation of S7 timer processing time is the sum of all times mentioned above:

2×0.36 ms	(Input process image transfer time)
+ 2×0.23 ms	(Output process image transfer time)
+ 2×1 ms	(Operating system cycle time)
+ 2×2.3 ms	User program cycle time) $\approx$**7.8 ms**.

- Processing time of S7 timers

  Time required for a single update of 56 S7 timers: 56×8 µs = 448 µs $\approx$ 0.45 ms.

  Since the S7 timers are called every 10 ms, a maximum of one call can be made in the cycle time, i.e. the cycle time can be increased through the S7 timers by a maximum of 0.45 ms.

- **2. Intermediate calculation:**The response time **without** I/O delay is formed by the sum of

8.0 ms	(result of the first intermediate calculation)
+ 0.45 ms	(S7 timer processing time)
=8.45 ms.	

- Delay times of the inputs and outputs
  - The SM 321 The maximum delay time of the DI 32DC 24 V digital input module is **4.8ms** per channel.
  - Output delay of the digital output module SM 322; DO 16 $\times$ DC 24 V/0.5A can be ignored.
  - The SM 331; AI 8 12bit analog input module was configured for an interference frequency suppression of 50 Hz. This yields a conversion time of 22 ms per channel. Since 8 channels are active, the cycle time for the analog input module is **176 ms**.
  - Analog output module SM 332 AO 4×12–bit was configured for a measurement range of 0 ...10V. The conversion time is **0.8 ms** per channel. Thus, 4 active channels result in a cycle time of 3.2 ms. To be added is the settling time of 0.1 ms for ohmic loads. Thus, the response time at the analog output is **3.3 ms**.
- Response times with delay times for inputs and outputs:
- **Case 1:** A digital output module channel is set after a digital input signal is received. This results in a response time of:

  Response time = 4.8 ms + 8.45 ms **= 13.25 ms**.
- **Case 2:** An analog value is fetched and an analog value is output. This results in a response time of:

  Response time = 176 ms + 8.45 ms + 3.3 ms **= 187.75 ms**.

3.4 Interrupt response time

Interrupt Response Time – A Definition

The interrupt response time is the time that elapses between the first occurrence of an interrupt signal and the calling of the first instruction in the interrupt OB.

Generally valid is: High-priority interrupts are preferred. This means the interrupt response time is increased by the program processing time of the higher-priority interrupt OBs and the interrupt OBs of equal priority that have not yet been executed.

Calculation

The interrupt response time is calculated as follows:

Shortest interrupt response time =
minimum CPU interrupt response time +
minimum interrupt response time of the signal modules +
PROFIBUS-DPbus cycle time

Longest interrupt response time =
maximum CPU interrupt response time +
maximum interrupt response time of the signal modules +
2 PROFIBUS-DPbus cycle time

Process interrupt response time of the CPUs

Table 3-7 lists the response time of the CPUs to process interrupts (without communication).

Table 3-7 Response time of the CPUs to process interrupts

CPU	Min.	Max.
312 IFM	0.6 ms	1.5 ms
313	0.5 ms	1.1 ms
314	0.5 ms	1.1 ms
314 IFM	0.5 ms	1.1 ms
315	0.3 ms	1.1 ms
315-2 DP	0.4 ms	1.1 ms
316-2DP	0.4 ms	1.1 ms
318-2	0.23 ms	0.27 ms

Diagnostic Interrupt Response Times of the CPUs

Table 3-8 lists the diagnostic interrupt response times of the CPUs (without communication).

Table 3-8 Diagnostic Interrupt Response Times of the CPUs

CPU	Min.	Max.
312 IFM	–	–
313	0.6 ms	1.3 ms
314	0.6 ms	1.3 ms
314 IFM	0.7 ms	1.3 ms
315	0.5 ms	1.3 ms
315-2 DP	0.6 ms	1.3 ms
316-2DP	0.6 ms	1.3 ms
318-2	0.32 ms	0.38 ms

Signal Modules

The response time of signal modules to process interrupts is calculated as follows:

- Digital input modules

  Process interrupt response time = internal interrupt processing time + Input delay

  You will find the times in the data sheet for the individual analog input module.

- Analog input modules

  Process interrupt response time = internal interrupt processing time + Conversion time

  The internal interrupt preparation time for the analog input modules is negligible. The conversion times can be found in the data sheet for the individual digital input modules.

The diagnostic interrupt response time of the signal modules is the time that elapses between the detection of a diagnostic event by the signal module and the triggering of the diagnostics interrupt by the signal module. This time is negligible.

Process interrupt processing

process interrupts are processed at the call of interrupt OB40. Higher-priority interrupts interrupt hardware interrupt processing, the I/O is accessed directly at the time of instruction execution. After the process interrupt has been processed, cyclic program processing continues, or lower-/higher-priority interrupt OBs are called and processed.

3.5 Calculation Example for the Interrupt Response Time

Parts of the Interrupt Response Time

As a reminder: The process interrupt response time is formed by:

- Response time of the CPU to process interrupt and
- the response time of the signal module to process interrupt.

Example: Your S7-300 assembly consists of a CPU 314 and four digital modules. One digital input module is the SM 321; DI 16 × DC 24V; with hardware/diagnostic interrupt configuration. In your CPU and SM configuration you have enabled only process interrupt. You decided not to use time-controlled processing, diagnostics or error handling. You configured an input delay of 0.5 ms for the digital input module. No activities are necessary at the scan cycle checkpoint. There is no communication via the MPI.

Calculation

In this example, the response time to process interrupt is calculated from following times:

- Response time of CPU 314 to process interrupt: approx. 1.1 ms
- Process interrupt response time of SM 321; DI 16 × DC 24V:
  - Internal interrupt preparation time: 0.25 ms
  - Input delay 0.5 ms

The process interrupt response time is formed by the sum of all specified times:

Process interrupt response time = 1.1 ms + 0.25 ms + 0.5 ms = **approx. 1.85 ms**.

This calculated process interrupt response time represents the time expiring between an incoming signal at the digital input and the first instruction in OB40.

3.6 Reproducibility of Delay and Watchdog Interrupts

Definition of Reproducibility

Delay Interrupt:

The interval between the call-up of the first instruction in the OB and the programmed time of the interrupt.

Watchdog Interrupt:

The fluctuation of the time interval between two successive call-ups, measured in each case between the first instruction in the OB.

Reproducibility

Table 3-9 lists reproducibility of the delay and watchdog interrupts of the CPUs (without communication).

Table 3-9 Reproducibility of the Delay and Watchdog Interrupts of the CPUs

CPU	Reproducibility	
	Delay Interrupt	**Watchdog Interrupt**
314	approx. –1/+0.4 ms	approx. ± 0.2 ms
314 IFM	approx. –1/+0.4 ms	approx. ± 0.2 ms
315	approx. –1/+0.4 ms	approx. ± 0.2 ms
315-2 DP	approx. –1/+0.4 ms	approx. ± 0.2 ms
316-2DP	approx. –1/+0.4 ms	approx. ± 0.2 ms
318-2	approx. –0.8/+0.38 ms	approx. ± 0.04 ms

CPU Function, depending on CPU and *STEP 7* Version

4

In this chapter we describe the functional differences between the various CPU versions.

These differences are determined by

- CPU performance characteristics (especially CPU 318-2) compared to other CPUs
- the functionaliy of CPUs described in this manual in comparison to previous versions.

4.1 Differences between CPU 3182 and CPUs 312 IFM to 3162 DP

4 rechargeable batteries for 318-2

CPU 318-2	CPUs 312IFM to 316-2DP
4 accumulators	2 accumulators

The following table shows you what to watch for if you want to use an STL user program of a CPU 312IFM to a CPU 316-2DP for the CPU 318-2.

Instructions	User Program from the CPU 312IFM to 316-2DP for the CPU 318
Double integer math (+I, –I, *I, /I; +D, –D, *D, /D,MOD; +R, –R, *R, /R)	The CPU 318 transfers the contents of accumulators 3 and 4 to accumulators 2 and 3 after these operations. If accumulator 2 is evaluated in the (accepted) user program, you now receive incorrect values with the CPU 318-2 because the value has been overwritten by the contents of accumulator 3.

Configuration

From 312 IFM to 316-2 DP CPUs, the CPU 318-2 “imports” only projects created with *STEP 7* V 5.x.

You cannot operate programs containing FM or CP (SDB 1xxx) configuration data (e.g. FM 353/354) in a CPU 318-2!
In this case, the respective project needs to be edited accordingly or recreated.

Starting a Timer in the User Program

The accumulator register in CPU 318–2 must contain a number in BCD format when starting a timer in your user program (e.g. with SI T).

Force

The differences of force operations are described in Chapter 1.3.1.

Loading the User Program to the Memory Card

CPU 318-2	CPUs 312IFM to 316-2DP
... using the PD function **Load User Program**	... using the PD function **Copy RAM To ROM** or **Load User Program**

System ID (only CPU 318-2)

In the object properties of the ”General” tab, you can assign a system ID when configuring your CPU. This ID can be evaluated in the CPU user program (also refer to the STEP 7 Online Help relating to the “General” tab).

MPI Addressing

CPU 318-2	CPUs 312IFM to 316-2DP
The CPU addresses the MPI nodes within its configuration (FM/CP) via the **module start address**.	The CPUs address the MPI nodes within their configuration via the **MPI address**.
If FM/CP are in the central configuration of an S7–300 with their own MPI address, the CPU forms its own communication bus (via the backplane bus) with the FM/CP, separate from the other subnets. The MPI address of the FM/CP is no longer relevant for the nodes of other subnets. Communication to the FM/CP takes place via the CPU MPI address.	If FM/CP are in the central configuration of an S7–300 with their own MPI address, the FM/CP and CPU MPI nodes are in the same CPU subnet.

Your S7-300 structure includes an FM/CP addressed via MPI. You want to replace the CPU 312 IFM ... 316 with a CPU 318-2. An example is shown in Figure 4-1, Page 4-4.

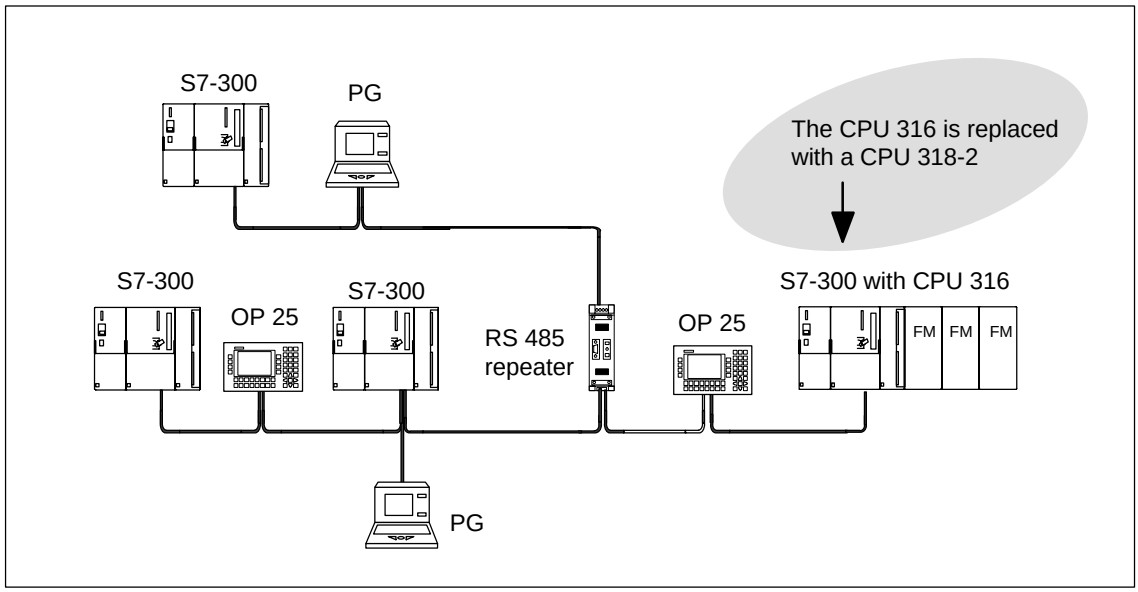


Figure 4-1 Sample Configuration

After the CPUs have been swapped, you must proceed as follows (based on the above example):

- Replace the CPU 316 with the CPU 318-2 in the STEP 7 project.
- Reconfigure the operator panel/programming device. That means: Reassign the controls and start address (= MPI address of CPU 318-2 and the respective FM slot)
- Reconfigure the configuration data for the FM/CP to be loaded onto the CPU.

This is necessary to ensure that the FM/CP in this configuration remain accessible to the operator panel/programming device.

Inserting and Removing a Memory Card (FEPROM)

If you remove a Memory Card and insert a card in with identical content in POWER OFF state (CPU is not buffered), the result after POWER ON is:

CPU 318-2	CPUs 312IFM to 316-2DP
The CPU 318-2 goes into STOP mode and request a memory reset.	The CPU switches to the mode it was in prior to POWER OFF, i.e. RUN or STOP.

Connection resources

CPU 318-2	CPUs 312IFM to 316-2DP
CPU 318-2 provides a total of 32 communication resources, that is, 32 of those via MPI/DP interface or 16 via DP interface. Those connection resources are freely available for • PD/OP communication • S7 basic communication • S7 communication and • Routing of PD communication	The CPUs provide a specific number of connection resources. For • PD communication • OP communication and • S7 basic communication you can reserve connection resources which can then not be used by any other communication function. The remaining connection resources are then available for PD/OP/S7 basic and S7 communication. For routing, the CPUs 315-/316-2 provide additional connection resources for 4 routing connections.

4.2 The Differences Between the CPUs 312 IFM to 318 and Their Previous Versions

Memory Cards and Backing Up Firmware on Memory Card

As of the following CPUs:

CPU	Order No.	As of Version	
		Firmware	Hardware
CPU 313	6ES7 313-1AD**03-**0AB0	1.0.0	01
CPU 314	6ES7 314-1AE**04-**0AB0	1.0.0	01
CPU 315	6ES7 315-1AF**03-**0AB0	1.0.0	01
CPU 315-2	6ES7 315-2AF**03-**0AB0	1.0.0	01
CPU 316-2	6ES7 316-1AG**00-**0AB0	1.0.0	01

You can:

- Insert the 16 bit-wide memory cards:

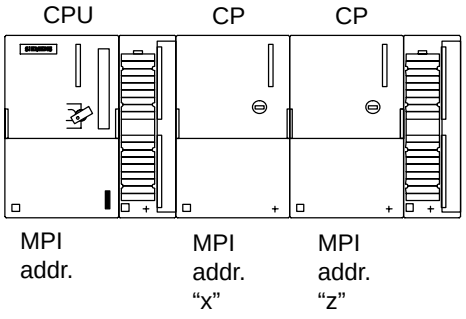
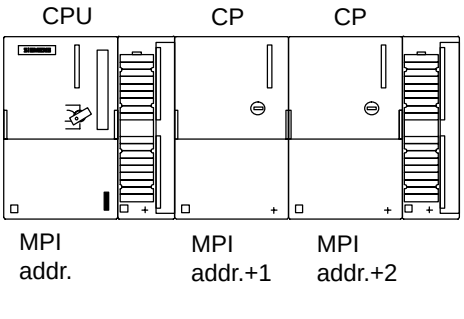
  256 Kbyte FEPROM 6ES7 951-1KH00-0AA0

  1 Mbyte FEPROM 6ES7 951-1KK00-0AA0

  2 Mbyte FEPROM 6ES7 951-1KL00-0AA0

  4 Mbyte FEPROM 6ES7 951-1KM00-0AA0
- Back up the CPU firmware on memory card

MPI Addressing

You Have a CPU as of Order Number and Version:	Your CPU version and order number is lower than the following:
6ES7312-5AC01-0AB0, version 01	
6ES7313-1AD02-0AB0, version 01	
6ES7314-1AE03-0AB0, version 01	
6ES7314-5AE02-0AB0, version 01	
6ES7315-1AF02-0AB0, version 01	
6ES7315-2AF02-0AB0, version 01	
6ES7316-1AG00-0AB0, version 01	–
and STEP 7 V4.02 or later	and STEP 7 < V4.02
The CPU accepts the MPI addresses configured by you in *STEP 7* for the relevant CP/FM in an S7300 or automatically determines the MPI address of the CP/FM in an S7-300 on the pattern MPI addr. CPU; MPI addr.+1 MPI addr.+2 etc.  	The CPU automatically establishes the MPI address of the CP/FM in an S7–300 on the pattern MPI addr. CPU; MPI addr.+1 MPI addr.+2 etc. 

MPI with 19.2 Kbps

With STEP 7 as of V4.02 you can set a transmission rate for the MPI of 19.2 Kbps.

The CPUs support 19.2 Kbps as of the following order numbers:

6ES7312-5AC01-0AB0, version 01
6ES7313-1AD02-0AB0, version 01
6ES7314-1AE03-0AB0, version 01
6ES7314-5AE02-0AB0, version 01
6ES7315-1AF02-0AB0, version 01
6ES7315-2AF02-0AB0, version 01

CPU 315-2 DP

CPU 315-2 DP	≤ 6ES7 315-2AF03-0AB0 and *STEP 7* < V 5.x	as of 6ES7 315-2AF03-0AB0 and *STEP 7* as of V 5.x
Direct communication	No	Yes
Equidistance	No	Yes
Activation/deactivation of DP slaves	No	Yes
Routing	No	Yes
Reading out of slave diagnosis	See Figure 2-1 on page 2-8	See Figure 2-2 on page 2-9

Connection resources

From CPU	Order No.	As of Version	
		Firmware	Hardware
CPU 312 IFM	6ES7 312-5AC02-0AB0	1.1.0	01
CPU 313	6ES7 313-1AD03-0AB0	1.1.0	01
CPU 314	6ES7 314-1AE04-0AB0	1.1.0	01
CPU 314 IFM	6ES7 314-5AE03-0AB0	1.1.0	01
CPU 314 IFM	6ES7 314-5AE10-0AB0	1.1.0	01
CPU 315	6ES7 315-1AF03-0AB0	1.1.0	01
CPU 315-2 DP	6ES7 315-2AF03-0AB0	1.1.0	01
CPU 316-2 DP	6ES7 316-2AG00-0AB0	1.1.0	01

... can be reserved for PD communication, OP communication and S7 basic communication.
In this case, the free communication resources are available for PD/OP/S7 basic or S7 communication (see also Chapter 1.2).

CPU versions earlier than those referred to above provide a fixed number of connection resources for the applicable communication functions.

New SFBs and SFCs in CPU 318-2

Function Block	Application	Execution time in µs		See...
SFB 52	Fetching data records to a DP Slave	Initial call	221	Online help Standard and System functions in STEP 7
		Intermediate call	111	
		Final call	158	
SFB 53	Fetching data records to a DP Slave	Initial call	284	
		Second call	110	
		Final call	110	
SFB 54	Receiving interrupts from a DP Slave (not for I/O-dependent OBs,MODE 1, OB1)		90	
	integrated DP interface, (MODE 1, OB 40, 83, 86)		170	
	(OB 55 to OB 57, OB 82)		176	
	(central peripherals, MODE 1, OB 40, OB 82)		140	

Function Block	Application	Execution time in µs		See...
SFC 100*	Setting TOD and TOD Status	MODE 1 MODE 2 MODE 3	274 84 275	Online help Standard and System-functions in STEP 7
SFC 105*	Reading dynamic system resources	MODE 0 MODE 1 MODE 2 MODE 3	117-1832 138-2098 139-1483 140-2128	
SFC 106	Releasing dynamic system resources	MODE 1 MODE 2 MODE 3	123-1376 126-1334 125-1407	
SFC 107	Creating block related messages including an acknowledgement function	Initial call Empty call	257 101	
SFC 108	Creating block related messages without acknowledgement function	Initial call Empty call	271 115	

* **MODE 0:**
Depending on the size of the target area SYS_INST and the number of system resources still to be fetched.

MODE 1 and 2:
Depends on the number of active messages (occupied system resources).

MODE 3:
Depends on the number of active messages (occupied system resources) and the number of instances used with the CMP_ID to be found.

Description of Diverse SFB Execution Times

The BUSY output parameter indicates the current job status.

Initial call: Job starts with the execution,
d. h. BUSY status is toggled from 0 to 1.

Intermediate call: The job is being executed,
d. h. BUSY retains 1 status.

Final call: The job was executed,
d. h. BUSY status is reset from 1 to 0.

Description of Diverse SFC Execution Times

Configure the desired operating mode in your SFCs modes. The significance of a specific mode depends on the respective function block. For details please refer to the Online Help on Standard and System Functions in STEP 7.

Consistent User Data

If you want to download consistent user data areas (I/O area with full length consistency) to a DP system, note the following:

CPU 315–2 DP **CPU 316–2 DP** **CPU 318–2 DP** (Firmware Version < 3.0)	**CPU 318–2 DP** (Firmware Version > 3.0)
Consistent user data are not updated automatically, even if they exist in the process image. SFC14 and SFC 15 are required for reading/writing consistent user data.	You can select whether or not to update this area, provided the address area of consistent user data exists in the process image. You can also use SFC14 and SFC 15 to read and write consistent data. User data areas can also be accessed directly (e.g. L PEW... T PAW...).

Tips and Tricks

5

Tip on the Parameter “Monitoring time for ...” in STEP 7

Configure the parameters for “Monitoring time

- for parameter download to module”
- ready message by module”

the highest values if you are not certain of the times required on the S7-300.

CPU 31x-2DP is DP Master	CPU 318-2 is DP Master
You can also set power-up time monitoring for the DP slaves with the “Transfer of parameters to modules” parameter.	You can set power-up time monitoring for the DP slaves with **both** of the above parameters.
This means that the DP slaves must be powered up and configured by the CPU (as DP master) in the set time.	

FM in a Distributed Configuration in an ET 200M (CPU 31x-2 is DP Master)

If you operate an FM 353/354/355 in an ET 200M with IM 153-2 and remove and reinsert the FM in ET 200M, you must perform a cold restart (power off/on) in the ET 200M.
Reason: The CPU does not rewrite the parameters to the FM unless the ET200M is initialized with “POWER ON”.

The Retentive Feature of Data Blocks

You must note the following for the retentivity of data areas in data blocks:

<table>
<tr><th rowspan="2">With Backup Battery</th><th colspan="2">Without Backup Battery</th></tr>
<tr><th>CPU program on Memory Card or in the integral EPROM of the 312IFM/314IFM</th><th>Memory card not plugged in</th></tr>
<tr><td rowspan="2">All DBs are retentive, whatever configuration has been performed. The DBs generated using SFC 22 “CREAT_DB” are also retentive.</td><td>All DBs (retentive, non-retentive) are transferred from the memory card or from the integral EPROM into RAM on restart.</td><td>The DBs configured as retentive retain their contents</td></tr>
<tr><td colspan="2">• Data blocks or data areas you have generated with SFC22 ”CREAT_DB” are not retentive.
• After a power failure, the retentive data areas are retained. Note:These data areas are stored in the CPU, not on the memory card. The non-retentive data areas contain whatever has been programmed on EPROM.</td></tr>
</table>

Watchdog Interrupt: Scan period > 5 ms

For the watchdog interrupt, you should set a scan period > 5 ms. With lower values the risk of frequent occurrence of watchdog interrupt errors increases, for example, depending on

- The program cycle time of an OB35
- Frequency and program cycle time of higher priority classes
- Programming device functions.

Hardware Interrupts Generated in I/O Modules

When using applications critical to hardware interrupt, insert the hardware-triggering modules as close to the CPU as possible.
Reason: Interrupts generated in module rack 0, slot 4, are read first. The other slots follow in ascending order.

CPU 312 IFM and 314 IFM: Erasing the integrated EPROM

If you wish to erase the contents of the integrated EPROM, proceed as follows:

1. Open a window with an Online view of the opened project via menu command **View ▸ Online**, or

   open the **Online nodes** window per click on the **Online nodes** in the function bar, or select the menu item **PLC ▸ Show online nodes**.
2. Select the MPI number of the target CPU (double-click).
3. Select the **Function Block** container.
4. Select the menu item **Edit▸ Mark all**.
5. Then select the menu item **File ▸ Delete**, or press the DEL key. This deletes all the selected blocks from the target memory.
6. Select the MPI number of the target CPU.
7. Select the menu item **PLC ▸ Copy RAM to ROM**.

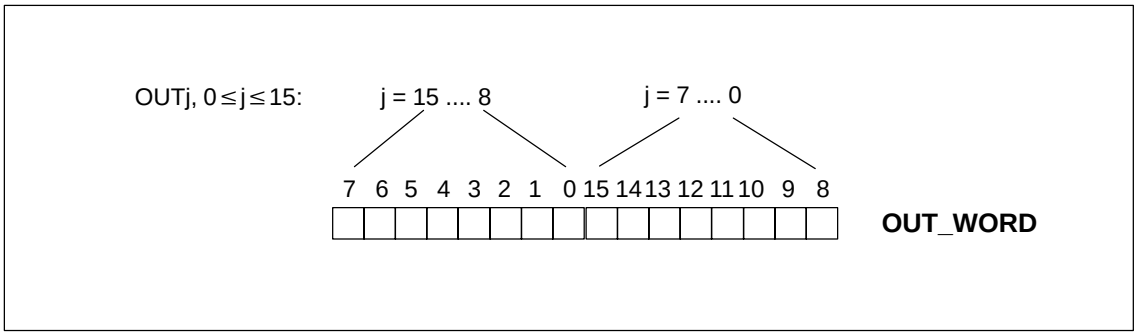
This command deletes all blocks online and overwrites the EPROM with the blank contents of the RAM.

SFB “DRUM” - Reversed Bytes in Output Parameter OUT-WORD

With the SFB “DRUM”, the following CPUs return the value with reversed bytes on the output parameter OUT_WORD.

CPU 312 IFM	up to	6ES7312-5ACx2-0AB0, firmware V 1.0.0
CPU 313	up to	6ES7313-1AD03-0AB0, firmware V 1.0.0
CPU 314	up to	6ES7314-1AEx4-0AB0, firmware V 1.0.0
CPU 314 IFM	up to	6ES7314-5AEx3-0AB0; firmware V 1.0.0
CPU 315	up to	6ES7315-1AF03-0AB0, firmware V 1.0.0
CPU 315-2 DP	up to	6ES7315-2AFx2-0AB0,
CPU 316	up to	6ES7316-1AG00-0AB0

The result is the following assignment, with reference to output parameter OUTj, $0 \leq j \leq 15$:



Standards, Certificates and Approvals

A

Introduction

This Appendix provides the following information on the S7-300 modules and components:

- The most important standards and criteria met by S7-300 and
- Approvals that have been granted for the S7-300.

IEC 1131

The S7-300 programmable controller meets the requirements and criteria to standard IEC 1131, Part 2.

CE Symbol

Our products meet the requirements and protection guidelines of the following EC Directives and comply with the harmonized European standards (EN) issued in the Official Journal of the European Communities with regard to programmable controllers:

- 89/336/EEC “Electromagnetic Compatibility” (EMC Directive)
- 73/23/EEC “Electrical Equipment Designed for Use between Certain Voltage Limits” (Low-Voltage Directive)

The declarations of conformity are held at the address below, where they can be obtained if and when required by the respective authorities:

Siemens Aktiengesellschaft
Automation Group
A&D AS RD 4
P.O. Box 1963
D-92209 Amberg Federal Republic of Germany

EMC Guidelines

SIMATIC products are designed for industrial use.

Area of Application	Requirements:	
	Emitted interference	Immunity
Industry	EN 50081-2 : 1993	EN 50082-2 : 1995

If you use the S7-300 in residential areas, you must ensure emission of radio interference complies with Limit Class B as per EN 55011.

The following measures can be taken to achieve compliance with Limit Class B:

- Install the S7-300 in an earthed control/switch cabinet
- Fit filters to supply lines

UL Recognition

UL Recognition Mark
Underwriters Laboratories (UL) to
UL standard 508, Report 116536

CSA Certification

CSA-Certification-Mark
Canadian Standard Association (CSA) to
Standard C22.2 No. 142, File No. LR 48323

FM Approval

FM Approval to Factory Mutual Approval Standard Class Number 3611, Class I, Division 2, Group A, B, C, D.

Warning

Personal injury or property damage can result.

In hazardous areas, personal injury or property damage can result if you withdraw any connectors while an S7-300 is in operation.

Always isolate the S7-300 in hazardous areas before withdrawing connectors.

PNO

CPU	Certificate No. As ...	
	DP Master	**DP Slave**
315-2 DP	Z00349	Z00258
316-2DP	Yes *	Yes *
318-2	Yes *	Yes *

* Number was not available at time of going to press

Dimensioned Drawings

B

Introduction

This appendix contains the dimensioned drawings of S7-300 CPUs. The specifications in these drawings are required of you for dimensioning your S7-300 assembly. The dimensioned drawings of the other S7-300 modules and components are contained in the *Module Specifications* Reference Manual.

CPU 312 IFM

Figure B-1 shows the dimensioned drawing of CPU 312IFM.

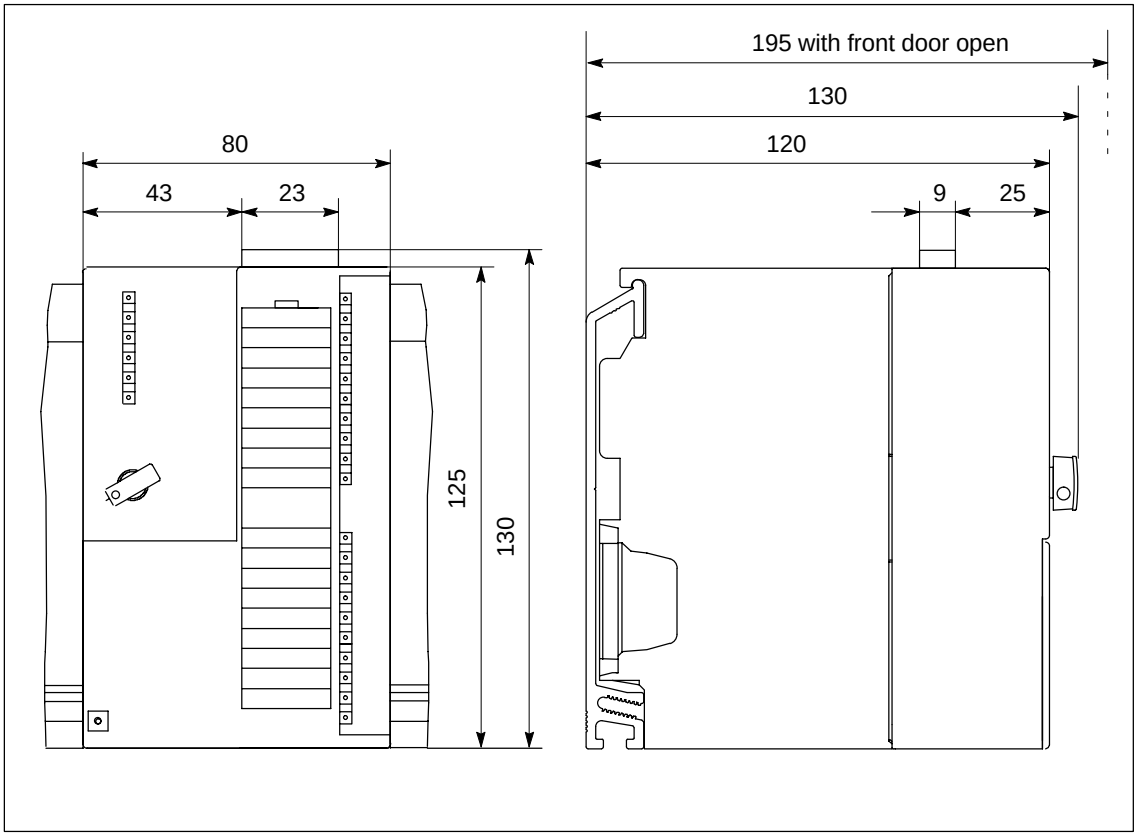


Figure B-1 Dimensioned Drawing of the CPU 312 IFM

CPU 313/314/315/315-2DP/316-2 DP

Figure B-2 shows the dimensioned drawing of the CPU 313/314/315/315-2 DP/316-2 DP. The dimensions are the same for all the CPUs listed. Their appearance can differ (see Chapter 1). For example, the CPU 315-2 DP has two LED strips.

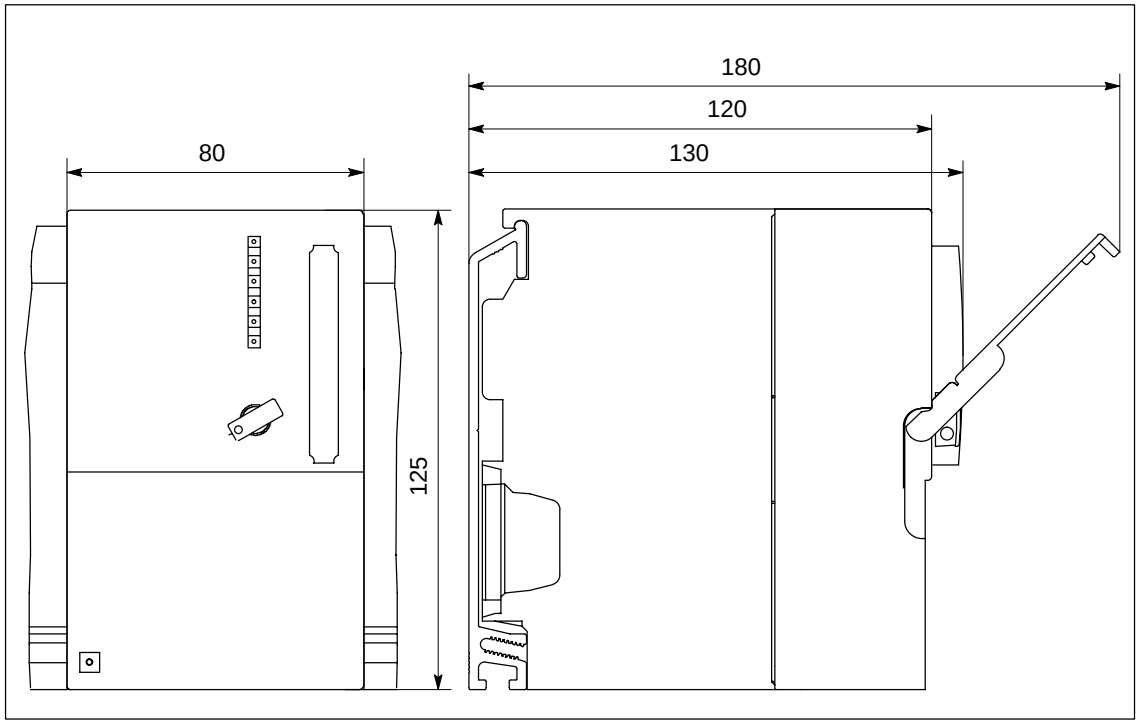


Figure B-2 Dimensioned Drawing of the CPU 313/314/315/315-2 DP/316-2DP

CPU 318-2

Figure B-3 shows the dimensioned drawing of the CPU 318-2, front view. The side view is illustrated in Figure B-2

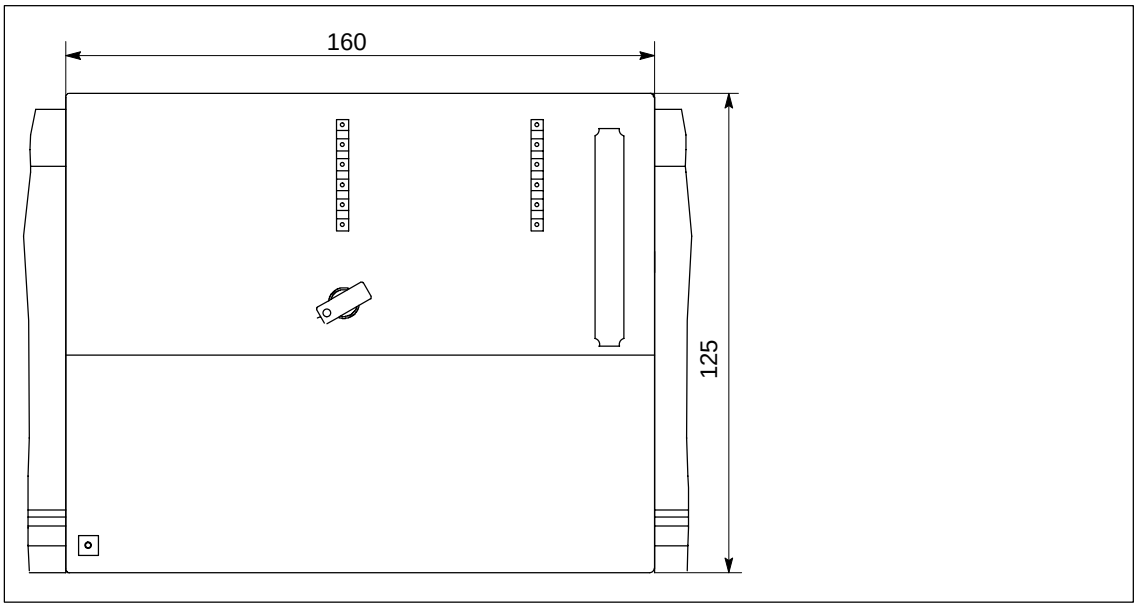


Figure B-3 Dimensioned Drawing of the CPU 318-2

CPU 314 IFM, Front View

Figure B-4 shows the dimensioned drawing of CPU 314IFM, front view. The side view is shown in Figure B-5.

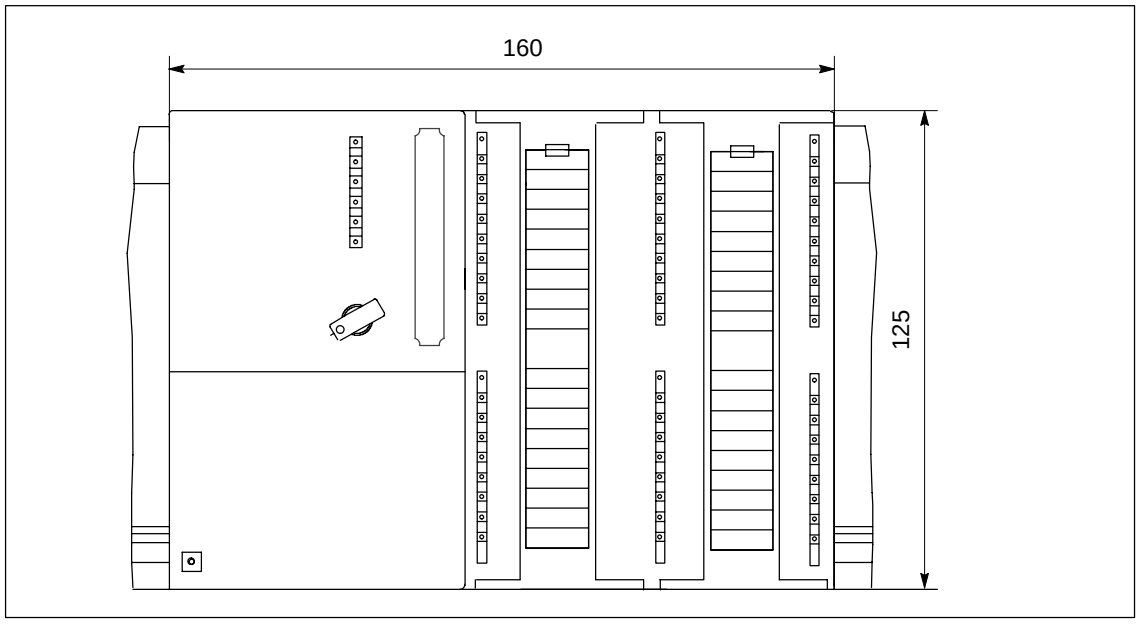


Figure B-4 Dimensioned Drawing of the CPU 314 IFM, Front View

CPU 314 IFM, Side View

Figure B-5 shows the dimensioned drawing of the CPU 314 IFM, side view.

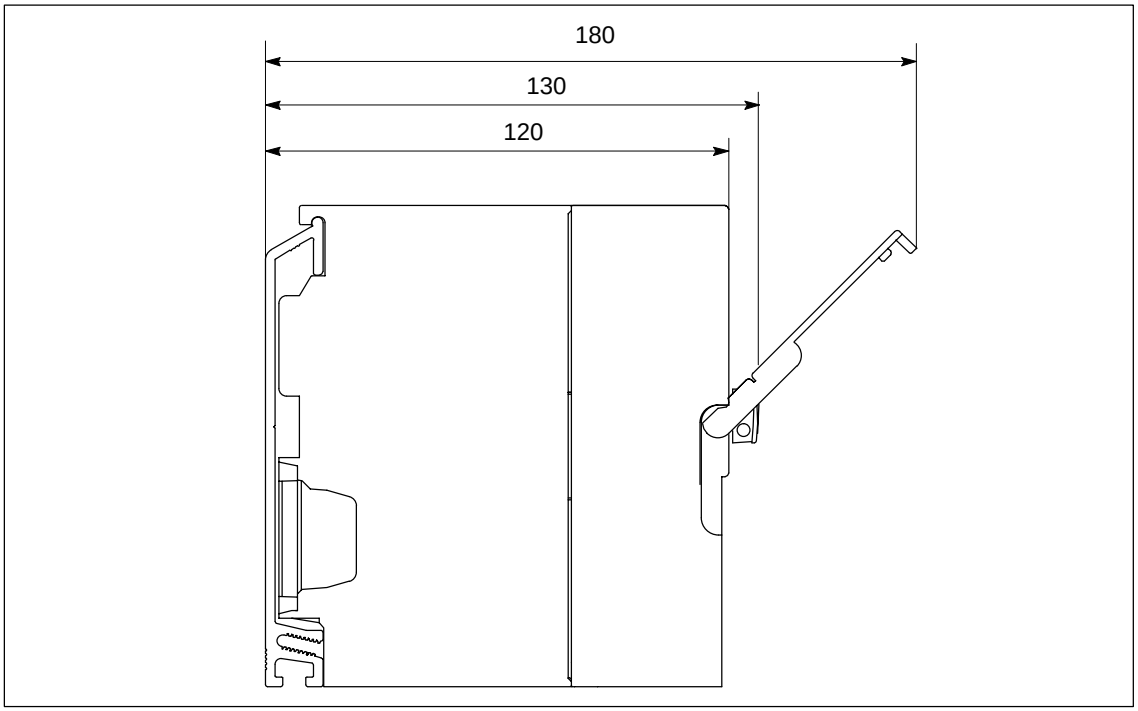


Figure B-5 Dimensioned Drawing of the CPU 314 IFM, Side View

List of Abbreviations

C

Abbrevia-tions	Description
STL	Statement List (programming language representation in STEP 7)
CP	Communication processor
CPU	Central processing unit
DB	Data block
FB	Function block
FC	Function
FM	Function module
GD	Global data communication
IM	Interface module
IP	Intelligent I/O
LAD	Ladder logic (programming language representation in STEP 7)
FO	Fiber-optic cable
M	Chassis ground
MPI	Multipoint Interface
OB	Organization block
OP	Operator panel
PIO	Output process image
PII	Input process image
PG	Programming device
PS	Power supply
SFB	System function block
SFC	System function
SM	Signal module

Glossary

Accumulator

Accumulators are registers in the → CPU. They are an intermediate memory for loading, transfer, compare, calculation and conversion operations.

Address

An address is an ID for a specific operand or operand area, for example: Input I 12.1; memory word MW 25, data block DB 3).

Analog module

Analog modules convert process values (e.g. temperature) into digital values, so that they can be processed by the central processing unit, or convert digital values into analog manipulated variables.

Automation system

An SIMATIC S7 automation system is a → programmable logic controller.

Backplane bus

The backplane bus is a serial data bus over which the modules communicate and over which the necessary power is supplied to the modules. The connection between the modules is established by bus connectors.

Backup battery

The backup battery ensures that the→ user program in the → CPU is saved in the event of a power failure and that defined data areas, memory bits, timers and counters are retentive.

Backup memory

Backup memory ensures buffering of CPU memory areas → CPU, using no battery. A configurable number of timers, counters, memories and data bytes (retentive timers, counters, memories and data bytes) is backed up.

Bit memory

Memory bits are objects of → CPU system memory, used for storing intermediate results. They can be accessed in units of a bit, byte, word or DWORD.

Bus

A bus is a communication medium connecting several nodes. Data transmission can be serial or parallel across electrical conductors or fiber-optic cables.

Bus segment

A bus segment is a self-contained section of a serial bus system. Bus segments are interconnected using repeaters.

Chassis ground

Chassis ground is the totality of all the interconnected inactive parts of a piece of equipment on which a hazardous touch voltage cannot build up even in the event of a fault.

Clock memories

Memories that can be used for clocking purposes in the user program (1 memory byte).

Note

Note in the case of S7-300 CPUs that the clock memory byte is not exceeded in the user program.

Code block

A SIMATIC S7 code block contains part of the *STEP 7* user program. (In contrast: → data block only contains data.)

Compress

The programming device online function “Compress” is used to align all valid blocks contiguously in the RAM of the CPU at the start of the user memory. This eliminates all gaps which arose when blocks were deleted or modified.

Communication processor

Communication processors are modules for point-to-point and bus links.

Configuration

Assignment of modules to racks/slots and (e.g. for signal modules) addresses.

Consistent data

Data whose contents are related and which should not be separated are known as consistent data.

For example, the values of analog modules must always be handled consistently, that is the value of an analog module must not be corrupted by reading it out at two different times.

Counter

Counters are integrated in → CPU system memory. The content of the “counter cells” can by modified by *STEP 7* instructions (e.g. count up/down).

CP

→ Communication processor

CPU

Central processing unit of the S7 programmable controller with open and closed-loop control systems, memory, operating system and interface for programming device.

Cycle time

The cycle time represents the time → a CPU requires for a single → user program execution.

Data block

Data blocks (DB) are data areas in the user program which contain user data. Global data blocks can be accessed by all code blocks while instance data blocks are assigned to a specific FB call.

Data, static

Static data is data which can only be used within a function block. The data is saved in an instance data block belonging to the function block. The data stored in the instance data block is retained until the next function block call.

Data, temporary

Temporary data is local data of a block which is stored in the L stack during execution of a block and which is no longer available after execution.

Delay Interrupt

→ Interrupt, Delay

Device master file

A Device Master File (GSD -file) contains all slave-specific characteristics data. Standard EN 50170,
Volume 2, PROFIBUS, specifies the GSD file format.

Diagnostics

→ System diagnostics

Diagnostic Interrupt

Modules with diagnostic function use diagnostic interrupts to report detected errors to the → CPU.

Diagnostic buffer

The diagnostic buffer is a buffered memory area in the CPU in which diagnostic events are stored in the order of their occurrence.

DP Master

A → master which behaves in accordance with EN 50170, Part 3 is known as a DP master.

DP Slave

A → DP Slave is operated on a PROFIBUS bus system, using the PROFIBUS-DP protocol and behaves in accordance with EN 50170, Part 3.

Equipotential bonding

Electrical connection (equipotential bonding conductor) which gives the bodies of electrical equipment and external conducting bodies the same or approximately the same potential, in order to prevent disturbing or dangerous voltages from being generated between these bodies.

Error display

Error display is one of the possible responses of the operating system to → runtime error. Other possible reactions are: → Error response in the user program, CPU STOP status.

Error handling via OB

If the operating system detects a specific error (e.g. an access error with *STEP 7*), it calls the organization block (error OB) which is provided for this event and which specifies the subsequent behavior of the CPU.

Error response

Reaction to a → runtime error. The operating system can react as follows: Switching the PLC to STOP, call of an OB in which the user can program a specific reaction, or display of the error.

External power supply

Power supply for signal/function modules and the connected hardware I/O.

FB

→ Function block

FC

→ Function

Flash EPROM

FEPROMs are the same as electrically erasable EEPROMS in that they can retain data in the event of a power failure, but they can be erased much more quickly (FEPROM = Flash Erasable Programmable Read Only Memory). They are used on → Memory Cards.

Force

The “Force” function overwrites a variable (e.g. memory marker, output) with a value defined by the S7 user. This variable is then write protected to prevent modification by any other operation (including the STEP 7 user program). The value is retained after the programming device is disconnected. The write protection is not canceled until the “Unforce” function is called and the variable is written again with the value defined by the user program. During commissioning, for example, the “Force” function allows certain outputs to be set to the “ON” state for any length of time even if the logic operations of the user program are not fulfilled (e.g. because inputs are not wired).

Function

A function (FC) according to IEC 1131-3 is a → code block containing no → static data. A function allows parameters to be passed in the user program. Functions are therefore suitable for programming complex functions, e.g. calculations, which are repeated frequently.

Function block

A function block (FB) according to IEC 1131-3 is a → code block containing → static data. An FB allows parameters to be passed in the user program. Function blocks are therefore suitable for programming complex functions, e.g. closed-loop controls, mode selections, which are repeated frequently.

Functional grounding

Grounding which has the sole purpose of safeguarding the intended function of the electrical equipment. Functional grounding short-circuits interference voltage which would otherwise have an impermissible impact on the equipment.

GD circuit

A GD circuit encompasses a number of CPUs which exchange data by means of global data communication. They are used as follows:

- A CPU broadcasts a GD packet to the other CPUs.
- One CPU sends and receives a GD packet from another CPU.

A GD circuit is identified by a GD circuit number.

GD Element

A GD element is generated by assigning shared → global data. It is uniquely identified in the global data table by its GD ID.

GD Packet

A GD packet can consist of one or multiple → GD elements transmitted in a single message frame.

Global data

Global data can be addressed from any → code block (FC, FB, OB). In detail, this refers to memory bits M, inputs I, outputs Q, timers, counters and data blocks (DBs). Absolute or symbolic access can be made to global data.

Global data communication

Global data communication represents a method → for exchanging global data between CPUs (without CFBs).

Ground

The conductive earth whose electrical potential can be set equal to zero at any point.

In the vicinity of grounding electrodes, the earth can have a potential different to zero. The term “reference ground” is frequently used to describe these circumstances.

Ground (to)

To ground means to connect an electrically conducting component to the grounding electrode (one or more conducting components which have a very good contact with the earth) across a grounding system.

Instance data block

A data block, which is generated automatically, is assigned to each function block call in the *STEP 7* user program. The values of the input, output and in/out parameters are stored in the instance data block, together with the local block data.

Interface, multipoint

→ MPI

Interrupt

→ The CPU operating system knows 10 different priority classes that control user program processing. Belonging to these priority classes are, for example, e.g. process interrupts. When an interrupt is triggered, the operating system automatically calls an assigned organization block in which the user can program the desired response (for example in an FB).

Interrupt, Delay

The Delay Interrupt belongs to on of the priority classes for SIMATIC S7 program processing. It is generated on expiration of a time started in the user program. A corresponding organization block is then executed.

Interrupt, diagnostic

→ Diagnostic Interrupt

Interrupt, Process

→Process interrupt

Interrupt, Watchdog

A watchdog interrupt is generated periodically by the CPU in configurable time intervals. A corresponding → OB is then processed.

Interrupt, Time-Of-Day-

The TOD interrupt belongs to on of the priority classes for SIMATIC S7 program processing. It is generated according to a specified date (or daily) and time-of-day (e.g. at 9:50, hourly, or once a minute). A corresponding organization block is then executed.

Isolated

The reference potential of the control and load voltage circuits is isolated galvanically in isolated I/O modules; e.g. with optocouplers, relay contacts or transformers. I/O circuits can be connected to a common potential.alena

Local data

→ Data, temporary

Load memory

The load memory is part of the central processing unit. It contains objects generated by the programming device. It is implemented either as a plug-in memory card or a permanently integrated memory.

Main memory

Main memory is the RAM memory in the → CPU, used by the processor for user program access during program processing.

Master

Masters holding the → Token can send/request data to/from other nodes (= active nodes).

Memory card

Memory cards are card-size memory media for CPUs and CPs, equipped with → RAM or → FEPROM memory modules.

Module parameters

Module parameters are values which can be used to control the response of the module. A distinction is made between static and dynamic module parameters.

MPI

The Multipoint Interface (MPI) represents the SIMATIC S7 programming interface, used to operate multiple nodes (Programming devices, text displays, operator panels) on one or multiple central modules. Each station is identified by a unique address (MPI address).

MPI address

→ MPI

Nesting depth

One block can be called from another by means of block calls. Nesting depth is the number of → code blocks called simultaneously.

Non-isolated

On non-isolated input/output modules, there is an electrical connection between the reference potentials of the control and load circuits.

OB

→Organization block

OB Priority

The CPU → operating system differentiates between different priority classes, e.g. cyclic program processing, process-interrupt controlled program processing. An OB is assigned to each one of the priority classes. → The S7 user can program a reaction in these OBs. The OBs have different standard priorities which determine the order in which they are executed or interrupted in the event that they are activated simultaneously.

Organization block

Organization blocks (OBs) represent the interface between the operating system of the CPU and the user program. The processing sequence of the user program is defined in the organization blocks.

Operating mode

SIMATIC S7 automation systems know the following operating states: STOP, → STARTUP, RUN.

Operating system of the CPU

The operating system of the CPU organizes all functions and processes of the CPU which are not associated with a special control task.

Parameter

1. *STEP 7* code block variable
2. Variable for specifying module behavior (one or several per module). Each module is delivered with a suitable default setting, which can be changed by configuring the parameters in *STEP 7*.
There are → static and → dynamic parameters

Parameters, dynamic

Unlike static parameters, dynamic parameters of modules can be changed during operation by calling an SFC in the user program, for example limit values of an analog signal input module.

Parameters, static

Unlike dynamic parameters, static parameters of modules cannot be changed by the user program, but only by changing the configuration in *STEP 7*, for example the input delay on a digital signal input module.

PG

→Programming device

PLC

→ Programmable controller

Priority class

The S7 CPU operating system offers a maximum of 26 priority classes (or ”program execution levels”), Diverse OBs are assigned to these classes. The priority classes determine which OBs interrupt other OBs. If a priority class includes several OBs, they do not interrupt each other, but are executed sequentially.

Process image

The process image forms part of → CPU system memory. The signal states of the input modules are written to the input process image at the start of the cyclic program. At the end of the cyclic program, the signal states in the output process image are transferred to the output modules.

Process Interrupt

A process interrupt is generated by respective modules, triggered as a result of specific hardware events. The process interrupt is reported to the CPU. An assigned OB is then processed, according to the interrupt priority→.

Product version

The product version differentiates between products which have the same order number. The product version is increased with each upwardly compatible function extension, production-related modification (use of new components) or bug-fix.

PROFIBUS-DP

Digital, analog and intelligent modules and a wide range of field devices to EN 50170, Part 3, e.g. drives or valve blocks, are distributed local to the local process by the PLC - across distances of up to 23 km.

The modules and field devices are connected to the programmable controller via the PROFIBUS-DP fieldbus and addressed in the same way as centralized I/Os.

Programmable controller

Programmable controllers (PLCs) are electronic controllers whose function is saved as a program in the control unit. The configuration and wiring of the unit are therefore independent of the function of the control system. The programmable controller has the structure of a computer; it consists of the → CPU (central module) with its memory, I/O modules and an internal bus system. The I/Os and the programming language are oriented to control engineering needs.

Programming device

Programming devices are essentially personal computers which are compact, portable and suitable for industrial applications. They are equipped with special hardware and software for SIMATIC programmable controllers.

RAM

A RAM (Random Access Memory, read/write) is a semiconductor chip.

Reduction factor

The reduction factor based on CPU cycle time determines the frequency → of GD package exchange.

Reference ground

→ Ground

Reference potential

Potential with reference to which the voltages of participating circuits are observed and/or measured.

Restart

When a central processing unit is started up (e.g. by switching the mode selector from STOP to RUN or by switching the power on), organization block OB 100 (complete restart) is executed before cyclic program execution commences (OB 1). On restart the input process image is read and the *STEP 7*- user program is executed, starting at the first OB1 instruction.

Retentivity

A memory area is retentive if its contents are retained even after a power failure and transition from STOP to RUN. The volatile area of memory markers, timers and counters is reset following a power failure and a transition from the STOP mode to the RUN mode.

The following can be made retentive:

- Bit memories
- S7 timers (**not** for CPU 312 IFM)
- S7 counters
- Data areas (only with memory card or integral EPROM)

Runtime error

Errors occurring during program execution in the PLC (that is, not in the process).

Start-up

RESTART mode is activated on a transition from STOP mode to RUN mode. Can be triggered with the → Mode Selector Switch or after Power On or with a PG operation. With an S7-300 a → complete restart is performed.

Segment

→ Bus segment

SFB

→ System function block (SFB)

SFC

→ System function

Signal module

Signal modules (SM) form the interface between the process and the PLC. There are digital modules digital modules (I/O module, digital) and analog modules (I/O module, analog).

Slave

A Slave can exchange data only on → Master request.

System diagnostics

System diagnostics is a method used to recognize, evaluate and report PLC errors. Examples of such errors: program error or module failure. System errors can be displayed with LED indicators or in *STEP 7*.

System Function

This function (SFC) is
→ integrated in the CPU operating system. It can be called as required in the STEP 7 user program.

System Function Block

The SFB is integrated in the CPU operating system. → This function block can be called as required in the STEP 7 user program.

System memory

System memory is an integrated CPU RAM memory. This system memory contains the operand areas (e.g. timers, counters, memory bits) and data areas → required internally by the operating system (e.g. communication buffer).

System state list

The system status list contains data describing the current status of an S7-300. You can use it to gain an overview of the following at any time:

- S7-300 configuration
- Current CPU configuration and the configurable signal modules
- The current states and sequences in the CPU and the configurable signal modules.

STEP 7

Programming language for developing user programs for SIMATIC S7 PLCs.

Substitute value

Substitute values are configurable values which output modules transmit to the process when the CPU switches to STOP mode.

In the event of an input access error, a substitute value can be written to the accumulator instead of the input value which could not be read (SFC 44).

Terminating resistor

A resistance for terminating a data transmission line. Avoids reflections.

Times

Times are integrated in → CPU system memory. The contents of the “timer cells” are updated automatically by the operating system, asynchronously to the user program. *STEP 7* instructions are used to define the exact function of the timer cells (for example on-delay) and initiate their execution (e.g. start).

Timer

→ Times

Time-of-day interrupt

→ Interrupt, time-of-day

Token

Access right on bus

Transmission rate

Rate of data transfer (bps)

User memory

User memory contains → Code/Data → blocks of the user program. User memory can be integrated in the CPU, on Memory Card or Memory modules. The user program, however, is always processed from → CPU main memory.

User program

SIMATIC differentiates between the → CPU operating system and user programs. The latter are created with the Programming Software → *STEP 7* in the possible Programming languages (FUP, STL) and stored in code blocks. Data are stored in data blocks.

Ungrounded

Having no galvanic connection to ground

Varistor

Voltage-independent resistor

Watchdog Interrupt

→ Interrupt, Watchdog

Index

D

E

F

G

I

L

M

N

O

P

R

S

T

U

V

W