PLL Basics—Loop Filter Design

Introduction

With the rapid expansion of the wireless/RF marketplace, there has been a proliferation of companies entering the fray to design the next winning wireless connectivity product. For many, it is their first attempt to design a PLL synthesized wireless communication transceiver.

The major basic requirements in the design of a PLL frequency synthesizer are to achieve the performance goals of low phase noise, low spurious output and to step, or hop, from one frequency to another in a specified amount of time.

Unfortunately, most of the articles and books written about designing the Loop Filter for PLL synthesizers dwell in the theoretical and try to cover the subject for all cases of PLL synthesizer design. This article will consider the design of a simple passive three-pole Loop Filter typically used in low voltage, low operating bandwidth synthesizer applications. This approach will simplify and demystify the Loop Filter design procedure.

Thanks to current levels of semiconductor integration, the components that make up the total synthesizer solution consist of a PLL IC for the control portion of the synthesizer, a Reference Oscillator and a hybrid VCO. The only external components needed are the DC decoupling elements, RF by-pass elements, and the passive Loop Filter components.

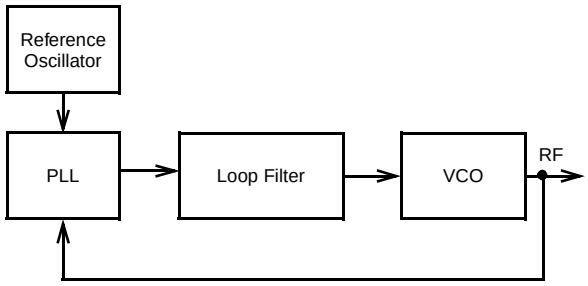

Figure 1. Basic PLL Layout

Presented here are the design calculations that have been used to develop Loop Filter solutions for many PLL applications. These calculations have been found to achieve the expected performance goals.

If the information used in the calculations is accurate, the PLL synthesizer will perform as designed. Experience has shown if the PLL synthesizer does not perform as expected, some component part or device specification is in error.

The simplified Loop Filter design formulas, found in Fujitsu's *Super PLL Application Guide*, are detailed below. The formulas are based upon the use of a basic passive two-pole Loop Filter along with a single-pole spur filter as shown in Figure 2.

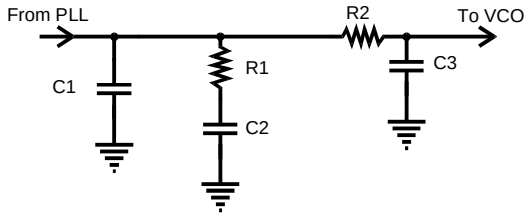

Figure 2. Loop Filter Configuration

Terms

fstep – Maximum frequency change during a step or hop, from one frequency to another.

ts – The desired time for the carrier to step to a new frequency.

fa – The frequency of the carrier, within the desired time (ts), after a step or hop. This is normally 1000 Hz.

ξ – Damping Factor - 0.707 is the typical choice

fn – Natural frequency

Icp – Charge Pump Current

Kvco – VCO sensitivity

ln – Natural LOG

Basic Calculations

1. Determine the maximum dividing ratio, N.

$$N = \frac{Maximum\ VCO\ Frequency}{Channel\ Spacing}$$

2. Calculate fn (natural frequency).

$$fn = \frac{-1}{2\pi \times ts \times \xi} \times ln\left(\frac{fa}{fstep}\right)$$

3. Calculate capacitor C2.

$$C2 = \frac{Icp \times Kvco}{N \times (2\pi \times fn)^2}$$

4. Calculate resistor R1.

$$R1 = 2 \times \xi \times \sqrt{\frac{N}{Icp \times Kvco \times C2}}$$

5. Calculate capacitor C1.

$$C1 = \frac{C2}{10}$$

6. Calculate R2 and C3 – the spur filter.

R2 and C3 are used to reduce any "spurs" caused by the reference frequency. The product of R2 and C3 should be at least 1/10 the product of C2 and R1.

Design Example

First you must define the basic synthesizer requirements for your application. Then define the active component's specifications.

For this example, a hypothetical application with arbitrary low-side injection is specified. It will use the Fujitsu MB15F08SL PLL IC and a VCO with a 25 volt/MHz sensitivity.

Application Requirements

Frequency Range:	1675 to 1735 MHz
Channel Spacing:	200 KHz
Maximum Frequency Hop:	60 MHz
Frequency Hop time:	500 microseconds
Frequency Accuracy after the specified Hop time:	1000 Hz

Identify the Active Component Specifications

VCO sensitivity:	25 MHz/V
PLL IC Charge Pump current:	6 mA

Step by Step Example Calculations

1. Determine N

$$N = \frac{1735\ MHz}{200\ KHz}$$

$$N = 8675$$

2. Determine fn

$$fn = \frac{-1}{6.28 \times 0.5e^{-3} \times 0.707} \times ln\frac{1000}{60e^{6}}$$

$$fn = 4,955.95\ Hz$$

3. Calculate C2

$$C2 = \frac{.006 \times 25e^{6}}{8675 \times (6.28 \times 4955.95)^2}$$

$$C2 = 0.01785\mu F$$

4. Calculate R1

$$R1 = 2 \times 0.707 \times \sqrt{\frac{8675}{.006 \times 25e^{6} \times 0.01785e^{-6}}}$$

$$R1 = 2545\Omega$$

5. Calculate C1

$$C1 = \frac{.01785\mu F}{10}$$

$$C1 = .001785\mu F$$

6. Determine R2 and C3 – the spur filter

The product of R2 and C3 should be about 1/10 the product of R1 and C2.

$$R2 = 2545\Omega$$

$$C3 = \frac{.01785\mu F}{10} = .001785\mu F$$

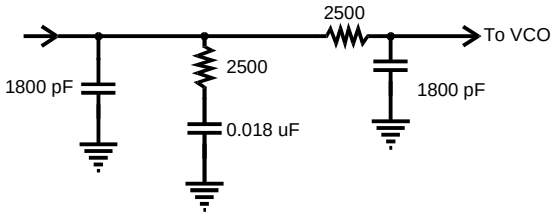

Figure 3. Loop Filter Components to the Nearest Standard Values

After the Loop filter values have been calculated, the Loop Bandwidth can be calculated.

Knowing the Loop Bandwidth will help determine if the PLL is operating correctly when the Phase Noise is displayed on a Spectrum Analyzer.

Loop Bandwidth Calculation

$$Loop\ Bandwidth\ =\ \frac{(2\pi)\times fn}{2}\times\left(\xi+\frac{1}{4\xi}\right)Hz$$

Loop Bandwidth Calculation for this Example

$$Loop\ Bandwidth\ =\ \frac{6.28\times 4955}{2}\times\left(.707+\frac{1}{2.828}\right)$$

$$Loop\ Bandwidth\ =\ 16,500\ Hz$$

The following graphs show the performance of the PLL synthesizer using the calculated values.

The graphs confirm that the calculations work well for designing Loop Filters to be used in many of today's PLL applications.

Figure 4 shows the excellent Phase Noise performance of the RF PLL of Fujitsu's new MB15F08SL dual 2.5/1.1 GHz PLL using the calculated Loop Filter values.

Marker "0" shows the Phase Noise inside the loop is –80.5 dBc/Hz. Marker "1" shows the loop bandwidth is 16000 Hz.

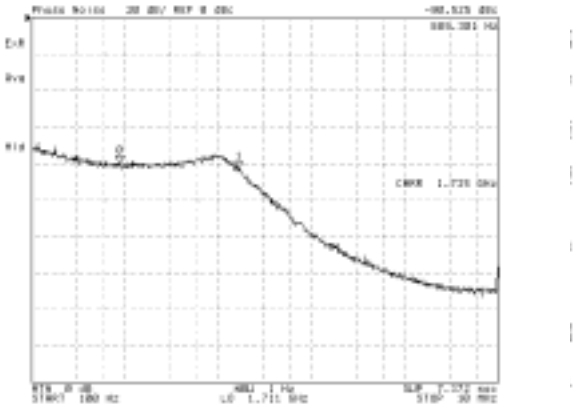

Figure 4. Phase Noise

Figure 5 shows the 200 KHz spurious signals to be an impressive -87.7 dBc, typical of the new Fujitsu SL Series of advanced PLL synthesizers, giving optimum performance for the latest digital wireless communications designs.

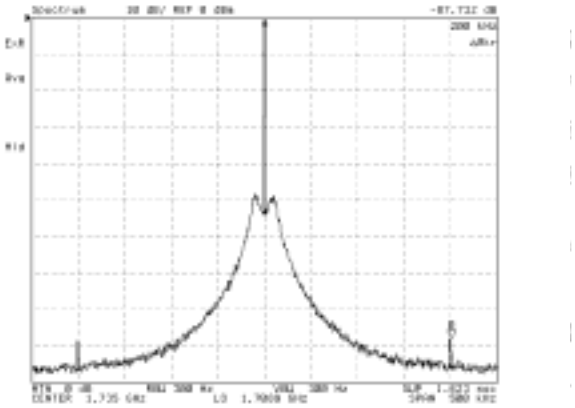

Figure 5. Spurious Response

Figure 6 shows that it takes 514 microseconds to change the frequency from 1675 MHz to 1735 MHz ±1000 Hz.

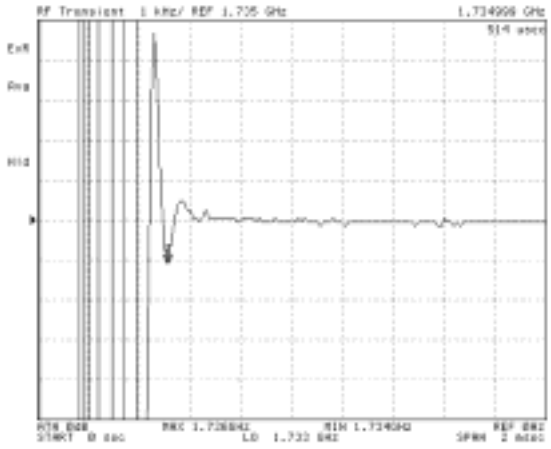

Figure 6. Hop Time

PLL Synthesizer Practical Considerations

Capacitors

An important part of the Loop Filter design is the use of components that will not degrade the performance of the synthesizer. The capacitors must have very low leakage.

Ceramic capacitors should not be used. The piezo-electric effect can cause noise and even microphonics on the VCO tuning line.

Film capacitors are recommended.

Resistors

The resistors should be the Metal or Carbon film type. Carbon composition is not recommended.

PCB Layout

The layout of the PC board can affect the level of VCO spurious signals and noise.

There are two very important things to do when laying out the PC board to reduce noise and spurs.

First, provide the shortest possible ground path between the PLL IC ground pins, Loop Filter ground, and the ground for the VCO Varicap tuning diode. If a packaged VCO is being used, it should be mounted close to the PLL IC and Loop Filter.

Second, bypass the Vcc lines that feed the PLL chip with a small value capacitor (0.1 mfd) and a large value capacitor (10 mfd). These capacitors should be placed as close as possible to the Vcc pins. Bypassing should also be used for the VCO. If the PLL and the VCO use the same Vcc, a 22-ohm resistor should be placed in the Vcc line between them to improve the isolation.

Conclusion

The purpose of this application note is to show that it is not difficult to design a high performance PLL synthesizer using the highly integrated parts available today.

Synthesizers operating well above 2000 MHz can be built with relatively few problems, provided good RF techniques are used for board layout and parts placement.

References:

Super PLL Application Guide
TC-AN-20731-11/98 - Fujitsu Microelectronics, Inc.
Ph. 800-866-8608

MB15FxxSL Series Data booklet
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Ph. 800-866-8608

Microwave and Wireless Synthesizers
Ulrich L. Rohde
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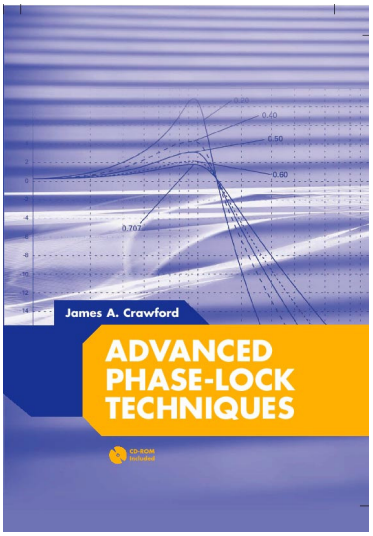

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James A. Crawford

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Chapter	Brief Description	*Pages*
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2	*Design Notes* A compilation of design notes and formulas that are developed in details separately in the text. Includes an exhaustive list of closed-form results for the classic type-2 PLL, many of which have not been published before.	44
3	*Fundamental Limits* A detailed discussion of the many fundamental limits that PLL designers may have to be attentive to or else never achieve their lofty performance objectives, e.g., Paley-Wiener Criterion, Poisson Sum, Time-Bandwidth Product.	38
4	*Noise in PLL-Based Systems* An extensive look at noise, its sources, and its modeling in PLL systems. Includes special attention to 1/*f* noise, and the creation of custom noise sources that exhibit specific power spectral densities.	66
5	*System Performance* A detailed look at phase noise and clock-jitter, and their effects on system performance. Attention given to transmitters, receivers, and specific signaling waveforms like OFDM, M-QAM, M-PSK. Relationships between EVM and image suppression are presented for the first time. The effect of phase noise on channel capacity and channel cutoff rate are also developed.	48
6	*Fundamental Concepts for Continuous-Time Systems* A thorough examination of the classical continuous-time PLL up through 4^{th}-order. The powerful Haggai constant phase-margin architecture is presented along with the type-3 PLL. Pseudo-continuous PLL systems (the most common PLL type in use today) are examined rigorously. Transient response calculation methods, 9 in total, are discussed in detail.	71
7	*Fundamental Concepts for Sampled-Data Control Systems* A thorough discussion of sampling effects in continuous-time systems is developed in terms of the *z*-transform, and closed-form results given through 4^{th}-order.	32
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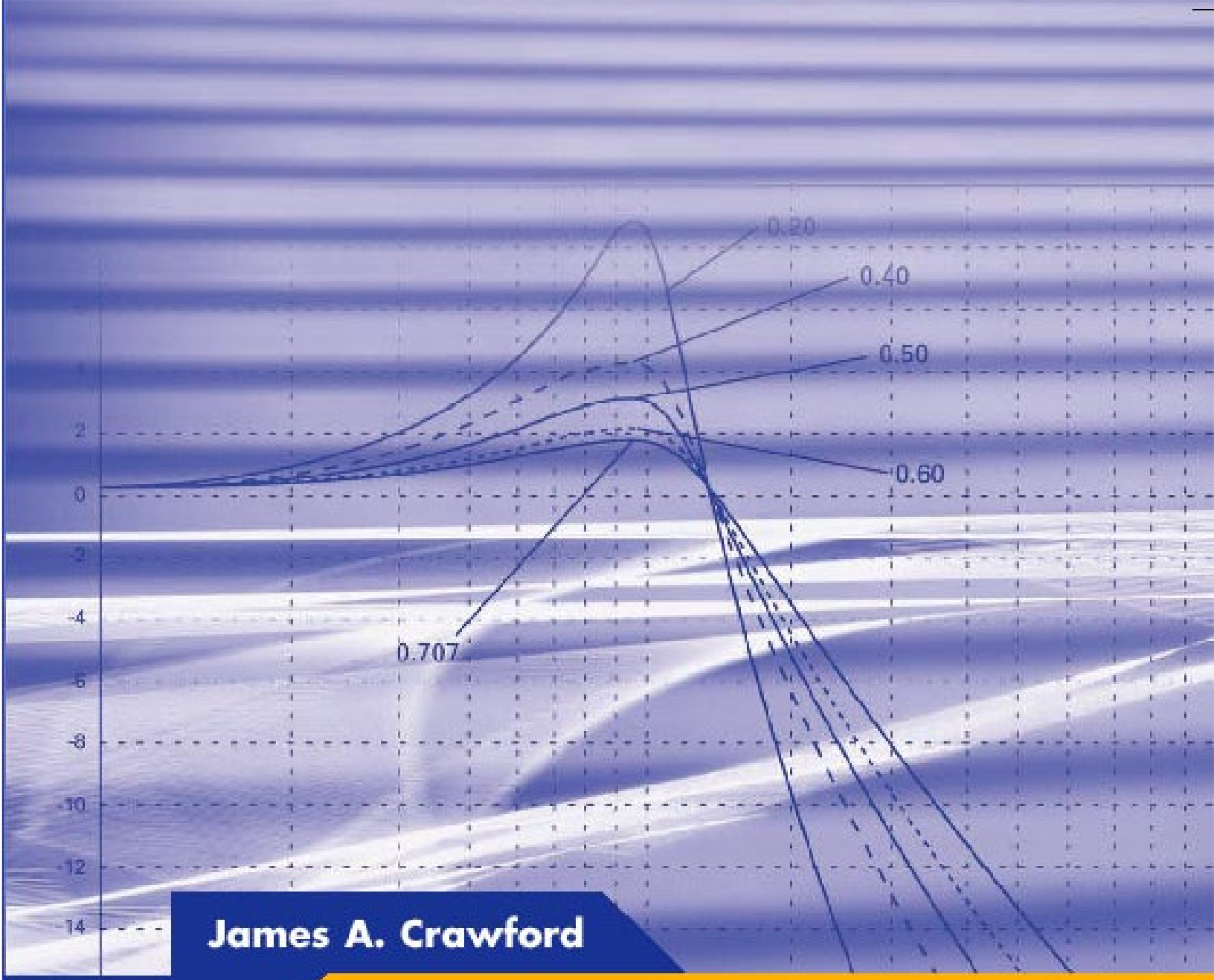

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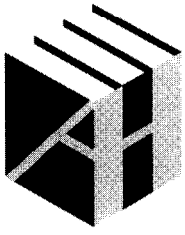

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are described further for the ideal type-2 PLL in Table 1-1. The feedback divider is normally present only in frequency synthesis applications, and is therefore shown as an optional element in this figure.

PLLs are most frequently discussed in the context of continuous-time and Laplace transforms. A clear distinction is made in this text between continuous-time and discrete-time (i.e., sampled) PLLs because the analysis methods are, rigorously speaking, related but different. A brief introduction to continuous-time PLLs is provided in this section with more extensive details provided in Chapter 6.

PLL type and *PLL order* are two technical terms that are frequently used interchangeably even though they represent distinctly different quantities. PLL *type* refers to the number of ideal poles (or integrators) within the linear system. A voltage-controlled oscillator (VCO) is an ideal integrator of phase, for example. PLL *order* refers to the order of the characteristic equation polynomial for the linear system (e.g., denominator portion of (1.4)). The loop-order must always be greater than or equal to the loop-type. Type-2 third- and fourth-order PLLs are discussed in Chapter 6, as well as a type-3 PLL, for example.

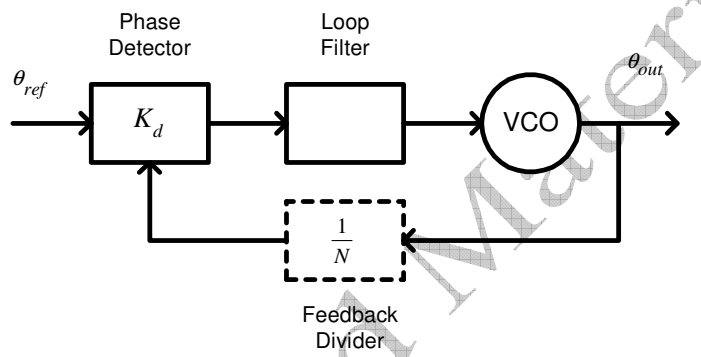

Figure 1-2 Basic PLL structure exhibiting the basic functional ingredients.

Table 1-1
Basic Constitutive Elements for a Type-2 Second-Order PLL

Block Name	Laplace Transfer Function	Description
Phase Detector	K_d, V/rad	Phase error metric that outputs a voltage that is proportional to the phase error existing between its input θ_{ref} and the feedback phase θ_{out}/N. Charge-pump phase detectors output a current rather than a voltage, in which case K_d has units of A/rad.
Loop Filter	$\frac{1+s\tau_2}{s\tau_1}$	Also called the lead-lag network, it contains one ideal pole and one finite zero.
VCO	$\frac{K_v}{s}$	The voltage-controlled oscillator (VCO) is an ideal integrator of phase. K_v normally has units of rad/s/V.
Feedback Divider	$1/N$	A digital divider that is represented by a continuous divider of phase in the continuous-time description.

The type-2 second-order PLL is arguably the workhorse even for modern PLL designs. This PLL is characterized by (i) its natural frequency ω_n (rad/s) and (ii) its damping factor ζ. These terms are used extensively throughout the text, including the examples used in this chapter. These terms are separately discussed later in Sections 6.3.1 and 6.3.2. The role of these parameters in shaping the time- and frequency-domain behavior of this PLL is captured in the extensive list of formula provided in Section 2.1. In the continuous-time-domain, the type-2 second-order PLL[3] open-loop gain function is given by

[3] See Section 6.2.

$$G_{OL}(s) = \left(\frac{\omega_n}{s}\right)^2 \frac{1+s\tau_2}{s\tau_1} \tag{1.1}$$

and the key loop parameters are given by

$$\omega_n = \sqrt{\frac{K_d K_v}{N\tau_1}} \tag{1.2}$$

$$\zeta = \frac{1}{2}\omega_n \tau_2 \tag{1.3}$$

The time constants τ_1 and τ_2 are associated with the loop filter's R and C values as developed in Chapter 6. The closed-loop transfer function associated with this PLL is given by the classical result

$$H_1(s) = \frac{1}{N}\frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{\omega_n^2\left(1+\dfrac{2\zeta}{\omega_n}s\right)}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{1.4}$$

The transfer function between the synthesizer output phase noise and the VCO self-noise is given by $H_2(s)$ where

$$H_2(s) = 1 - H_1(s) \tag{1.5}$$

A convenient frequency-domain description of the open-loop gain function is provided in Figure 1-3. The frequency break-points called out in this figure and the next two appear frequently in PLL work and are worth committing to memory. The unity-gain radian frequency is denoted by ω_u in this figure and is given by

$$\omega_u = \omega_n\sqrt{2\zeta^2+\sqrt{4\zeta^4+1}} \tag{1.6}$$

A convenient approximation for the unity-gain frequency (1.6) is given by $\omega_u \cong 2\zeta\omega_n$. This result is accurate to within 10% for $\zeta \geq 0.704$.

The $H_1(s)$ transfer function determines how phase noise sources appearing at the PLL input are conveyed to the PLL output and a number of other important quantities. Normally, the input phase noise spectrum is assumed to be spectrally flat resulting in the output spectrum due to the reference noise being shaped entirely by $|H_1(s)|^2$. A representative plot of $|H_1|^2$ is shown in Figure 1-4. The key frequencies in the figure are the frequency of maximum gain, the zero dB gain frequency, and the –3 dB gain frequency which are given respectively by

$$F_{Pk} = \frac{1}{2\pi}\frac{\omega_n}{2\zeta}\sqrt{\sqrt{1+8\zeta^2}-1} \text{ Hz} \tag{1.7}$$

$$F_{0dB} = \frac{1}{2\pi}\sqrt{2}\omega_n \text{ Hz} \tag{1.8}$$

$$F_{3dB} = \frac{\omega_n}{2\pi}\sqrt{1+2\zeta^2+2\sqrt{\zeta^4+\zeta^2+\frac{1}{2}}} \text{ Hz} \tag{1.9}$$

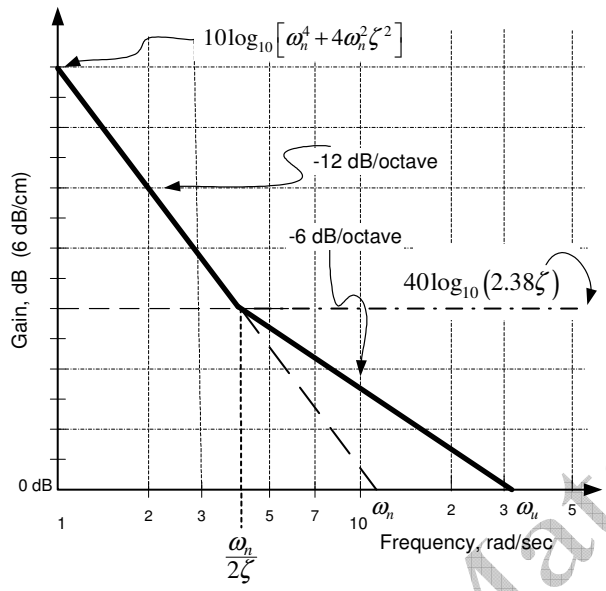

Figure 1-3 Open-loop gain approximations for classic continuous-time type-2 PLL.

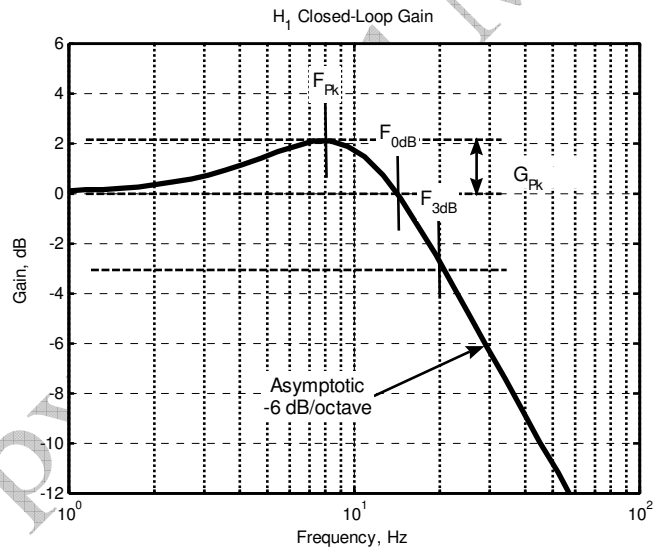

Figure 1-4 Closed-loop gain $H_1(f)$ for type-2 second-order PLL[4] from (1.4).

The amount of *gain-peaking* that occurs at frequency F_{pk} is given by

$$G_{Pk} = 10\log_{10}\left(\frac{8\zeta^4}{8\zeta^4-4\zeta^2-1+\sqrt{1+8\zeta^2}}\right)\text{dB} \tag{1.10}$$

For situations where the close-in phase noise spectrum is dominated by reference-related phase noise, the amount of gain-peaking can be directly used to infer the loop's damping factor from (1.10), and the

[4] Book CD:\Ch1\u14033_figequs.m, $\zeta = 0.707$, $\omega_n = 2\pi 10$ Hz.

loop's natural frequency from (1.7). Normally, the close-in (i.e., radian offset frequencies less than $\omega_n/2\zeta$) phase noise performance of a frequency synthesizer is entirely dominated by reference-related phase noise since the VCO phase noise generally increases 6 dB/octave with decreasing offset frequency[5] whereas the open-loop gain function exhibits a 12 dB/octave increase in this same frequency range.

VCO-related phase noise is attenuated by the $H_2(s)$ transfer function (1.5) at the PLL's output for offset frequencies less than approximately ω_n. At larger offset frequencies, $H_2(s)$ is insufficient to suppress VCO-related phase noise at the PLL's output. Consequently, the PLL's output phase noise spectrum is normally dominated by the VCO self-noise phase noise spectrum for the larger frequency offsets. The key frequency offsets and relevant $H_2(s)$ gains are shown in Figure 1-5 and given in Table 1-2.

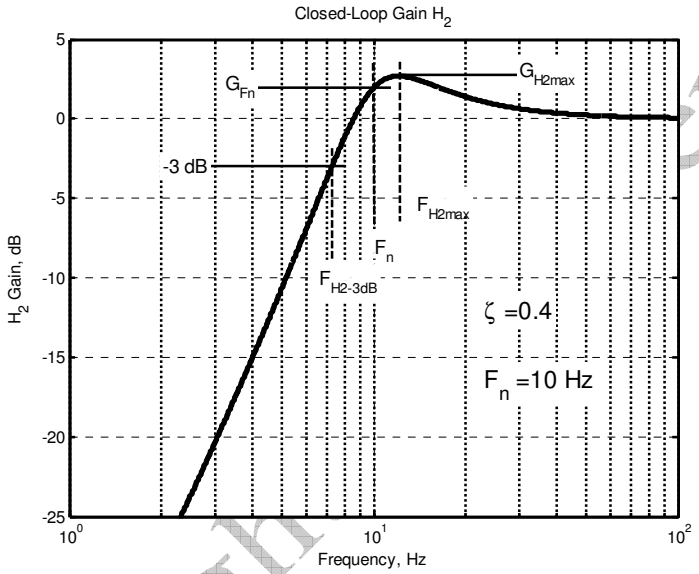

Figure 1-5 Closed-loop gain[6] H_2 and key frequencies for the classic continuous-time type-2 PLL.

Table 1-2
Key Frequencies Associated with $H_2(s)$ for the Ideal Type-2 PLL

Frequency, Hz	**Associated H_2 Gain, dB**	**Constraints on ζ**
$1/2\pi$	$G_{H_2\_1rad/s} = -10\log_{10}\left[\omega_n^4 + \omega_n^2\left(4\zeta^2 - 2\right) + 1\right]$	—
$F_{H_2-3dB} = \frac{\omega_n}{2\pi}\left[2\zeta^2 - 1 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right]^{1/2}$	–3	—
$F_{H_2\_0dB} = \frac{1}{2\pi}\frac{\omega_n}{\sqrt{2-4\zeta^2}}$	0	$\zeta < \frac{\sqrt{2}}{2}$
$F_n = \omega_n / 2\pi$	$G_{H_2\_\omega_n} = -10\log_{10}\left(4\zeta^2\right)$	—
$F_{H_2\_\max} = \frac{1}{2\pi}\frac{\omega_n}{\sqrt{1-2\zeta^2}}$	$G_{H_2\_\max} = -10\log_{10}\left(4\zeta^2 - 4\zeta^4\right)$	$\zeta < \frac{\sqrt{2}}{2}$

[5] Leeson's model in Section 9.5.1; Haggai oscillator model in Section 9.5.2.
[6] Book CD:\Ch1\u14035_h2.m.

Assuming that the noise samples have equal variances and are uncorrelated, $R = \sigma_n^2 I$ where I is the $K \times K$ identity matrix. In order to maximize (1.43) with respect to θ, a necessary condition is that the derivative of (1.43) with respect to θ be zero, or equivalently

$$\begin{aligned}\frac{\partial L}{\partial \theta} &= \frac{\partial}{\partial \theta}\sum_k \left[r_k - A\cos\left(\omega_o t_k + \theta\right)\right]^2 = 0 \\ &= \sum_k 2\left[r_k - A\cos\left(\omega_o t_k + \theta\right)\right] A\sin\left(\omega_o t_k + \theta\right) = 0\end{aligned} \tag{1.44}$$

Simplifying this result further and discarding the double-frequency terms that appear, the maximum-likelihood estimate for θ is that value that satisfies the constraint

$$\overline{\sum_k r_k \sin\left(\omega_o t_k + \hat{\theta}\right)} = 0 \tag{1.45}$$

The top line indicates that double-frequency terms are to be filtered out and discarded. This result is equivalent to the minimum-variance estimator just derived in (1.40).

Under the assumed linear Gaussian conditions, the minimum-variance (MV) and maximum-likelihood (ML) estimators take the same form when implemented with a PLL. Both algorithms seek to reduce any quadrature error between the estimate and the observation data to zero.

1.4.3 PLL as a Maximum A Posteriori (MAP)-Based Estimator

The *MAP estimator* is used for the estimation of random parameters whereas the maximum-likelihood (ML) form is generally associated with the estimation of deterministic parameters. From *Bayes rule* for an observation z, the a posteriori probability density is given by

$$p(\theta|z) = \frac{p(z|\theta)\,p(\theta)}{p(z)} \tag{1.46}$$

and this can be re-written in the logarithmic form as

$$\log_e\left[p(\theta|z)\right] = \log_e\left[p(z|\theta)\right] + \log_e\left[p(\theta)\right] - \log_e\left[p(z)\right] \tag{1.47}$$

This log-probability may be maximized by setting the derivative with respect to θ to zero thereby creating the necessary condition that[27]

$$\frac{d}{d\theta}\left\{\log_e\left[p(z|\theta)\right] + \log_e\left[p(\theta)\right]\right\}_{\theta=\hat{\theta}_{MAP}} = 0 \tag{1.48}$$

If the density $p(\theta)$ is not known, the second term in (1.48) is normally discarded (set to zero) which degenerates naturally to the maximum-likelihood form as

$$\frac{d}{d\theta}\left\{\log_e\left[p(z|\theta)\right]\right\}_{\theta=\hat{\theta}_{ML}} = 0 \tag{1.49}$$

[27] [15] Section 6.2.1, [17] Section 2.4.1, [18] Section 5.4, and [22].

Time of Peak Phase-Error with Frequency-Step Applied

$$T_{fstep} = \frac{1}{\omega_n\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \tag{2.29}$$

Note.[1] See Figure 2-19 and Figure 2-20.

Time of Peak Phase-Error with Phase-Step Applied

$$T_{\theta step} = \frac{1}{\omega_n\sqrt{1-\zeta^2}}\tan^{-1}\left(2\zeta\sqrt{1-\zeta^2}, 2\zeta^2-1\right) = \frac{2}{\omega_n\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \tag{2.30}$$

See Figure 2-19 and Figure 2-20.

Time of Peak Frequency-Error with Phase-Step Applied

$$T_{pk} = \frac{1}{\omega_n\sqrt{1-\zeta^2}}\begin{cases}\zeta \le \frac{1}{2}: & \theta_u \\ \zeta > \frac{1}{2}: & \theta_u + \pi\end{cases} \tag{2.31}$$

$$\text{with } \theta_u = \tan^{-1}\left[\left(1-4\zeta^2\right)\sqrt{1-\zeta^2}, 3\zeta-4\zeta^3\right] \tag{2.32}$$

See Figure 2-21 and Figure 2-22.

T_{pk} corresponds to the *first point* in time where $df_o/dt = 0$.

Maximum Frequency-Error with Phase-Step Applied

Use (2.31) in (2.28). (2.33)

Time of Peak Frequency-Error with Frequency-Step Applied

$$T_{pk} = \frac{2}{\omega_n\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \tag{2.34}$$

% Transient Frequency Overshoot for Frequency-Step Applied

$$OS_{\%} = \left[\cos\left(\sqrt{1-\zeta^2}\,\omega_n T_{pk}\right) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\sqrt{1-\zeta^2}\,\omega_n T_{pk}\right)\right]e^{-\zeta\omega_n T_{pk}} \times 100\% \tag{2.35}$$

$$T_{pk} = \frac{2}{\omega_n\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \tag{2.36}$$

Note.[2] See Figure 2-23 and Figure 2-24.

Linear Hold-In Range with Frequency-Step Applied (Without Cycle-Slip)

$$\Delta F_{\max} = \omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right] \text{ Hz} \tag{2.37}$$

See Figure 2-25.

Linear Settling Time with Frequency-Step Applied (Without Cycle-Slip) (Approx.)

$$T_{Lock} \le \frac{1}{\zeta\omega_n}\log_e\left(\frac{\Delta F}{\delta F}\frac{1}{\sqrt{1-\zeta^2}}\right) \text{ sec} \tag{2.38}$$

for applied frequency-step of ΔF and residual δF remaining at lock

See Figure 2-26.

[1] The peak occurrence time is precisely one-half that given by (2.34).

[2] See Figure 2-24 for time of occurrence T_{pk} for peak overshoot/undershoot with $\omega_n = 2\pi$. Amount of overshoot/undershoot in percent provided in Figure 2-23.

2.3.2.2 Second-Order Gear Result for $H_1(z)$ for Ideal Type-2 PLL

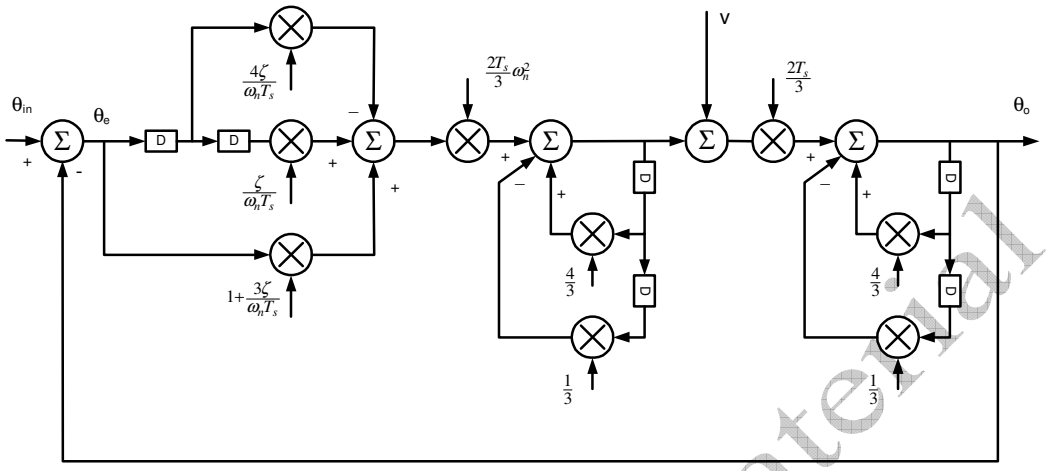

Figure 2-32 Second-order Gear redesign of $H_1(s)$ (2.4).

$$G_{OL}(z)=\left(\frac{2\omega_n T_s}{3}\right)^2 \frac{1+\dfrac{3\zeta}{\omega_n T_s}\left(1-\dfrac{4}{3}z^{-1}+\dfrac{1}{3}z^{-2}\right)}{\left(1-\dfrac{4}{3}z^{-1}+\dfrac{1}{3}z^{-2}\right)^2} \tag{2.52}$$

$$\theta_o(k)=\frac{1}{D}\left[\sum_{n=0}^{2} a_n\theta_{in}(k-n)+\sum_{n=0}^{2} b_n v(k-n)+\sum_{n=1}^{4} c_n\theta_o(k-n)\right] \tag{2.53}$$

$$\begin{aligned} a_0 &= 1+\frac{3\zeta}{\omega_n T_s} \\ a_1 &= -\frac{4\zeta}{\omega_n T_s} \\ a_2 &= \frac{\zeta}{\omega_n T_s} \end{aligned} \tag{2.54}$$

$$\begin{aligned} b_0 &= \frac{3}{2\omega_n^2 T_s} \\ b_1 &= -\frac{2}{\omega_n^2 T_s} \\ b_2 &= \frac{1}{2\omega_n^2 T_s} \end{aligned} \tag{2.55}$$

$$\begin{aligned} c_1 &= \frac{6}{(\omega_n T_s)^2}+\frac{4\zeta}{\omega_n T_s} \\ c_2 &= -\frac{11}{2(\omega_n T_s)^2}-\frac{\zeta}{\omega_n T_s} \\ c_3 &= \frac{2}{(\omega_n T_s)^2} \\ c_4 &= -\frac{1}{(2\omega_n T_s)^2} \end{aligned} \tag{2.56}$$

$$D=1+\frac{3\zeta}{\omega_n T_s}+\left(\frac{3}{2\omega_n T_s}\right)^2 \tag{2.57}$$

2.3.3 Higher-Order Differentiation Formulas

In cases where a precision first-order time-derivative $f(x_{n+1})$ must be computed from an equally spaced sample sequence, higher-order formulas may be helpful.[8] Several of these are provided here in Table 2-2. The uniform time between samples is represented by T_s.

[8] Precisions compared in Book CD:\Ch2\u14028_diff_forms.m.

2.5.5 64-QAM Symbol Error Rate

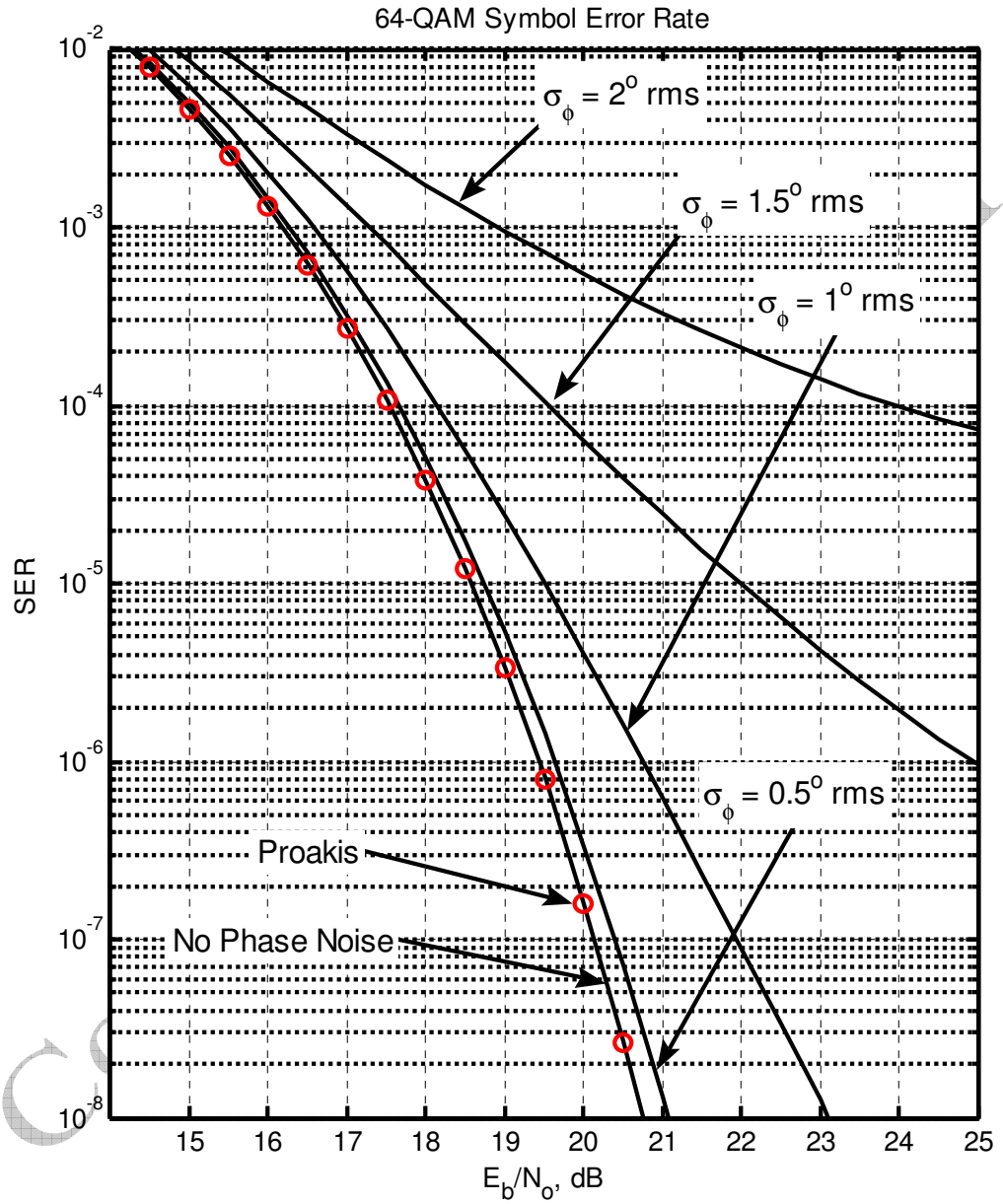

Figure 2-37 64-QAM uncoded symbol error rate with noisy local oscillator.[13] Circled datapoints are from (2.87).

[13] Book CD:\Ch5\u13159_qam_ser.m. See Section 5.5.3 for additional information. Circled datapoints are based on Proakis [3] page 282, equation (4.2.144), included in this text as (2.87).

A more detailed discussion of the Chernoff bound and its applications is available in [9].

Key Point: The Chernoff bound can be used to provide a tight upper-bound for the tail-probability of a one-sided probability density. It is a much tighter bound than the Chebyschev inequality given in Section 3.5. The bound given by (3.43) for the complementary error function can be helpful in bounding other performance measures.

3.7 CRAMER-RAO BOUND

The Cramer-Rao bound[16] (CRB) was first introduced in Section 1.4.4, and frequently appears in phase- and frequency-related estimation work when low SNR conditions prevail. Systems that asymptotically achieve the CRB are called *efficient* in estimation theory terminology. In this text, the CRB is used to quantify system performance limits pertaining to important quantities such as phase and frequency estimation, signal amplitude estimation, bit error rate, etc.

The CRB is used in Chapter 10 to assess the performance of several synchronization algorithms with respect to theory. Owing to the much larger signal SNRs involved with frequency synthesis, however, the CRB is rarely used in PLL-related synthesis work. The CRB is developed in considerable detail in the sections that follow because of its general importance, and its widespread applicability to the analysis of many communication system problems.

The CR bound provides a lower limit for the error covariance of any unbiased estimator of a deterministic parameter θ based on the probability density function of the data observations. The data observations are represented here by z_k for $k = 1, \ldots, N$, and the probability density of the observations is represented by $p(z_1, z_2, \ldots, z_N) = p(\mathbf{z})$. When θ represents a single parameter and θ-hat represents the estimate of the parameter based on the observed data $\mathbf{z}$, the CRB is given by three equivalent forms as

$$\begin{aligned}
\mathrm{var}\left[\left(\hat{\theta}-\theta\right)\right] &= \mathbf{E}\left[\left(\hat{\theta}-\theta\right)^2\right] \\
&\geq \left\{\mathbf{E}\left\{\left[\frac{\partial}{\partial\theta}\log_e p\left(\mathbf{z}\,|\,\theta\right)\right]^2\right\}\right\}^{-1} \\
&\geq -\left\{\mathbf{E}\left[\frac{\partial^2}{\partial\theta^2}\log_e p\left(\mathbf{z}\,|\,\theta\right)\right]\right\}^{-1} \\
&\geq \left\{\int_{-\infty}^{+\infty}\left[\frac{\partial}{\partial\theta}p\left(\mathbf{z}\right)\right]^2\frac{1}{p\left(\mathbf{z}\right)}d\mathbf{z}\right\}^{-1}
\end{aligned} \tag{3.46}$$

The first form of the CR bound in (3.46) can be derived as follows. Since θ-hat is an unbiased (zero-mean) estimator of the deterministic parameter θ, it must be true that

$$\mathbf{E}\left(\tilde{\theta}\right) = \int_{-\infty}^{+\infty}\left[\hat{\theta}-\theta\right]p\left(\mathbf{z}\right)d\mathbf{z} = 0 \tag{3.47}$$

in which $d\mathbf{z} = dz_1 dz_2 \ldots dz_N$. Differentiating (3.47) with respect to θ produces the equality

[16] See [10]–[14].

$$\text{var}\left\{\hat{b}_o\right\} \geq \frac{\sigma^2}{M} \quad \text{for all cases} \tag{3.62}$$

$$\text{var}\left\{\hat{\omega}_o T_s\right\} \geq \begin{cases} \dfrac{\sigma^2}{b_0^2 Q} & \text{Phase known, amplitude known or unknown} \\ \dfrac{12\sigma^2}{b_0^2 M\left(M^2-1\right)} & \text{Phase unknown, amplitude known or unknown} \end{cases} \tag{3.63}$$

$$\text{var}\left\{\hat{\theta}_o\right\} \geq \begin{cases} \dfrac{\sigma^2}{b_0^2 M} & \text{Frequency known, amplitude known or unknown} \\ \dfrac{12\sigma^2 Q}{b_0^2 M^2\left(M^2-1\right)} & \text{Frequency unknown, amplitude known or unknown} \end{cases} \tag{3.64}$$

In the formulation presented by (3.55), the signal-to-noise ratio ρ is given by $\rho = b_0^2 / (2\sigma^2)$.

For the present example, the CR bound is given by the top equation in (3.63) and is as shown in Figure 3-9 when the initial signal phase θ_o is known a priori. Usually, the carrier phase θ_o is not known a priori when estimating the signal frequency, however, and the additional unknown parameter causes the estimation error variance to be increased, making the variance asymptotically 4-times larger than when the phase is known a priori. This CR variance bound for this more typical unknown signal phase situation is shown in Figure 3-10.

Beginning with (3.57), a maximum-likelihood[17] frequency estimator can be formulated as described in Appendix 3A. It is insightful to compare this estimator's performance with its respective CR bound. For simplicity, the initial phase θ_o is assumed to be random but known a priori. The results for $M = 80$ are shown in Figure 3-11 where the onset of thresholding is apparent for $\rho \cong -2$ dB. Similar results are shown in Figure 3-12 for $M = 160$ where the threshold onset has been improved to about $\rho \cong -5$ dB.

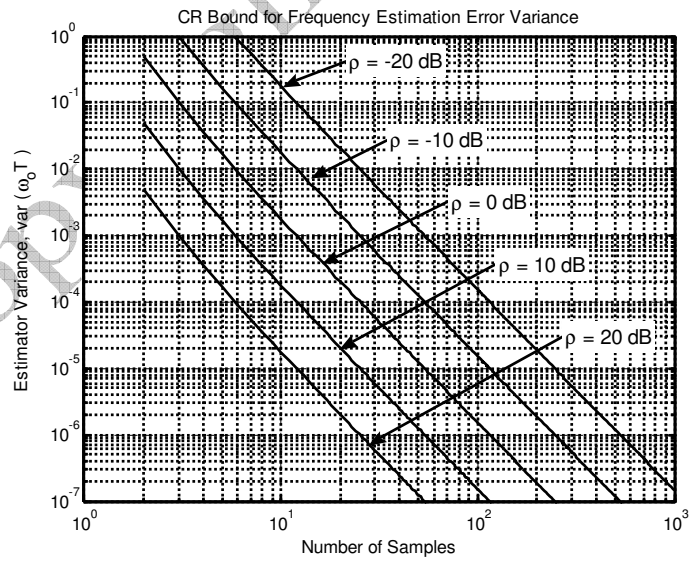

Figure 3-9 CR bound[18] for frequency estimation error with phase θ_o known a priori (3.63).

[17] See Section 1.4.2.

[18] Book CD:\Ch3\u13000_crb.m. Amplitude known or unknown, frequency unknown, initial phase known.

would be measured and displayed on a spectrum analyzer. Having recognized the carrier and continuous spectrum portions within (4.65), it is possible to equate[29]

$$\mathscr{L}(f) \cong P_\theta(f) \quad \text{rad}^2/\text{Hz} \tag{4.66}$$

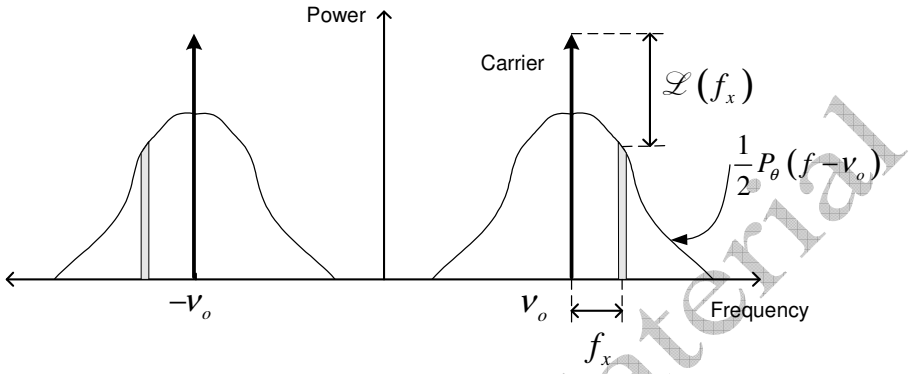

Figure 4-17 Resultant two-sided power spectral density from (4.65), and the single-sideband-to-carrier ratio $\mathscr{L}(f)$.

Both $\mathscr{L}(f)$ and $P_\theta(f)$ are *two-sided power spectral densities*, being defined for positive as well as negative frequencies.

The use of one-sided versus two-sided power spectral densities is a frequent point of confusion in the literature. Some PSDs are formally defined only as a one-sided density. Two-sided power spectral densities are used throughout this text (aside from the formal definitions for some quantities given in Section 4.6.1) because they naturally occur when the Wiener-Khintchine relationship is utilized.

4.6.1 Phase Noise Spectrum Terminology

A minimum amount of standardized terminology has been used thus far in this chapter to characterize phase noise quantities. In this section, several of the more important formal definitions that apply to phase noise are provided.

A number of papers have been published which discuss phase noise characterization fundamentals [34]–[40]. The updated recommendations of the IEEE are provided in [41] and those of the CCIR in [42]. A collection of excellent papers is also available in [43].

In the discussion that follows, the nominal carrier frequency is denoted by ν_o (Hz) and the frequency-offset from the carrier is denoted by f (Hz) which is sometimes also referred to as the *Fourier frequency*.

One of the most prevalent phase noise spectrum measures used within industry is $\mathscr{L}(f)$ which was encountered in the previous section. This important quantity is defined as [44]:

> $\mathscr{L}(f)$: The normalized frequency-domain representation of phase fluctuations. It is the ratio of the power spectral density in one phase modulation sideband, referred to the carrier frequency on a spectral density basis, to the total signal power, at a frequency offset f. The units[30] for this quantity are Hz^{-1}. The frequency range for f ranges from $-\nu_o$ to ∞. $\mathscr{L}(f)$ is therefore a two-sided spectral density and is also called *single-sideband phase noise*.

[29] It implicitly assumed that the units for $\mathscr{L}(f)$, dBc/Hz or rad^2/Hz, can be inferred from context.
[30] Also as rad^2/Hz.

$$z_i = p_i \exp\left(\frac{\alpha}{2}\Delta p\right) \tag{4B.10}$$

A minimum of one filter section per frequency decade is recommended for reasonable accuracy. A sample result using this method across four frequency decades using 3 and 5 filter sections is shown in Figure 4B-3.

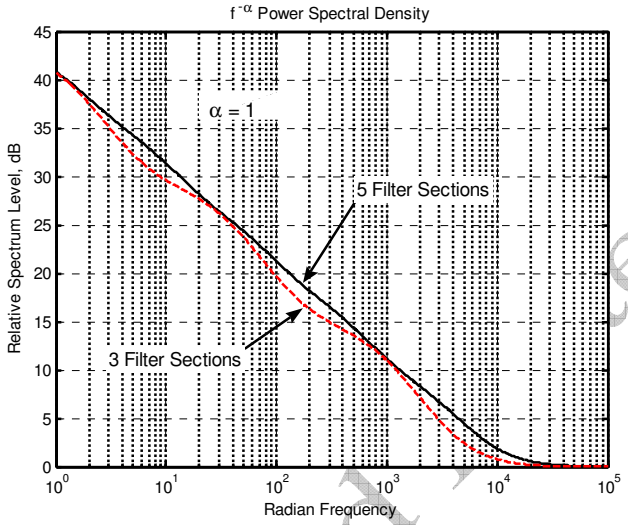

Figure 4B-3 $1/f$ noise creation using recursive $1/f^2$ filtering method[4] with white Gaussian noise.

$1/f^{\alpha}$ Noise Generation Using Fractional-Differencing Methods

Hosking [6] was the first to propose the *fractional differencing* method for generating $1/f^{\alpha}$ noise. As pointed out in [3], this approach resolves many of the problems associated with other generation methods. In the continuous-time-domain, the generation of $1/f^{\alpha}$ noise processes involves the application of a nonrealizable filter to a white Gaussian noise source having $s^{-\alpha/2}$ for its transfer function. Since the z-transform equivalent of $1/s$ is $H(z) = (1 - z^{-1})^{-1}$, the *fractional digital filter* of interest here is given by

$$H_{\alpha}(z) = \frac{1}{\left(1 - z^{-1}\right)^{\alpha/2}} \tag{4B.11}$$

A straightforward power series expansion of the denominator can be used to express the filter as an infinite IIR filter response that uses only integer-powers of z as

$$H_{\alpha}(z) \approx \left[1 - \frac{\alpha}{2}z^{-1} - \frac{\frac{\alpha}{2}\left(1 - \frac{\alpha}{2}\right)}{2!}z^{-2} - \ldots\right]^{-1} \tag{4B.12}$$

in which the general recursion formula for the polynomial coefficients is given by

[4] Book CD:\Ch4\u13070_recursive_flicker_noise.m.

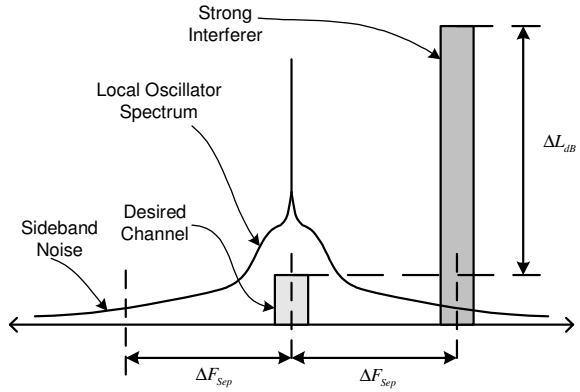

Figure 5-9 Strong interfering channels are heterodyned on top of the desired receive channel by local oscillator sideband noise.

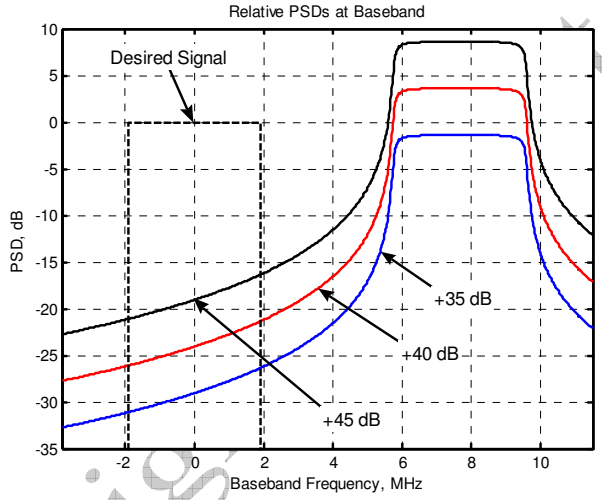

Figure 5-10 Baseband spectra[10] caused by reciprocal mixing between a strong interferer that is offset 4*B* Hz higher in frequency than the desired signal and stronger than the desired signal by the dB amounts shown.

The first term in (5.28) $2BL_{Floor}$ is attributable to the ultimate blocking performance of the receiver as discussed in Section 5.3. The resultant output SNR versus input SNR is given by

$$SNR_{out} = \left[\frac{1}{SNR_{in}} + \frac{\sigma_{MFX}^2}{2BL_{IQ}} \right]^{-1} \tag{5.29}$$

It is worthwhile to note that the interfering spectra in Figure 5-10 are not uniform across the matched-filter frequency region [–*B*, *B*]. Multicarrier modulation like OFDM (see Section 5.6) will potentially be affected differently than single-carrier modulation such as QAM (see Section 5.5.3) when the interference spectrum is not uniform with respect to frequency.

The result given by (5.29) is shown for several interfering levels versus receiver input SNR in Figure 5-11.

[10] Book CD:\Ch5\u13157_rx_desense.m. Lorentzian spectrum parameters: L_o = –90 dBc/Hz, f_c = 75 kHz, L_{Floor} = –160 dBc/Hz, B = 3.84/2 MHz.

of 3° rms phase noise is shown in Figure 5B-8. The tail probability is worse than the exact computations shown in Figure 5-17 but the two results otherwise match very well.

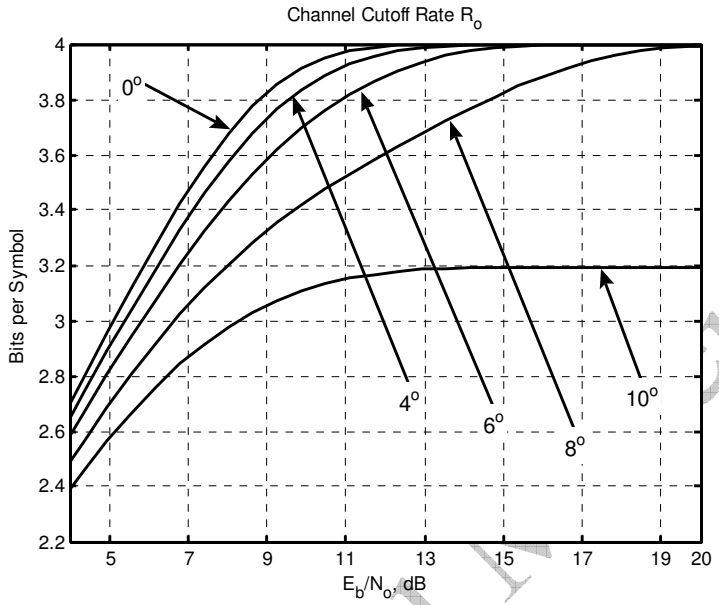

Figure 5B-6 Channel cutoff rate,[7] R_o, for 16-QAM with static phase errors as shown, from (5B.16).

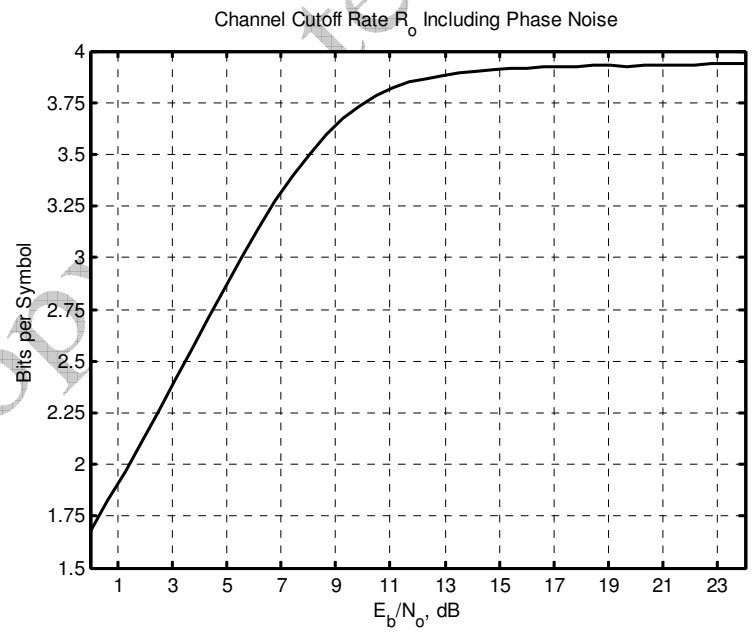

Figure 5B-7 R_o for[8] 16-QAM versus E_b/N_o for 5° rms phase noise from (5B.18) (to accentuate loss in R_o even at high SNR values).

[7] Book CD:\Ch5\u13176_rolo.m.
[8] Ibid.

required, however, because the offset current will introduce its own shot-current noise contribution, and the increased duty-cycle of the charge-pump activity will also introduce additional noise and potentially higher reference spurs. Single-bit Δ-Σ modulators are attractive in this respect because they lead to the minimum-width phase-error distribution possible.

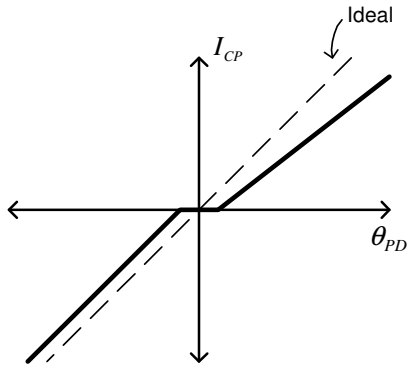

Figure 8-70 Charge-pump (i) dead-zone and (ii) unequal positive versus negative error gain.

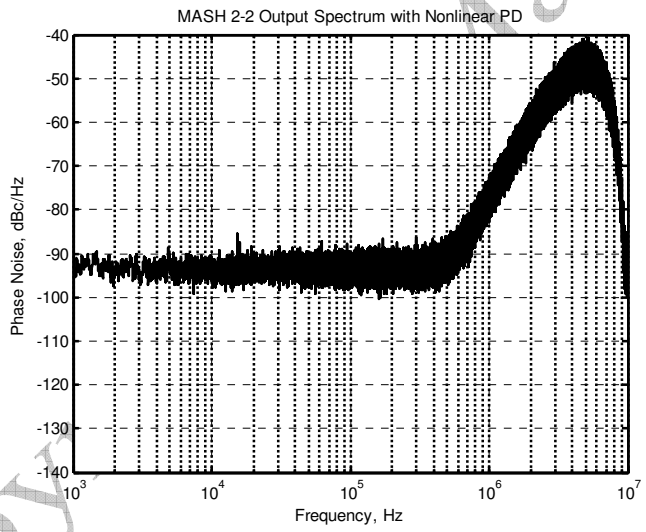

Figure 8-71 Phase error power spectral density[48] for the MASH 2-2 Δ-Σ modulator shown in Figure 8-55 with $M = 2^{22}$, $P = M/2 + 3{,}201$, and 2% charge-pump gain imbalance. Increased noise floor and discrete spurs are clearly apparent compared to Figure 8-56.

Classical random processes theory can be used to provide several useful insights about nonlinear phase detector operation. In the case of unequal positive-error versus negative-error phase detector gain, the memoryless nonlinearity can be modeled as

$$\theta_{pd} = \phi_{in} + \alpha(\phi_{in} > 0)\phi_{in} \tag{8.39}$$

where α represents the additional gain that is present for positive phase errors. The instantaneous phase error due to the modulator's internal quantization creates a random phase error sequence that can be represented by

[48] Book CD:\Ch8\u12735_MASH2_2_nonlinear.m.

the sampling-point within each symbol-period after the datalink signal has been fully acquired. In the example results that follow, the data source is assumed to be operating at 1 bit-per-second, utilizing square-root raised-cosine pulse-shaping with an excess bandwidth parameter $\beta = 0.50$ at the transmitter. The eye-diagram of the signal at the transmit end is shown in Figure 10-15. The ideal matched-filter function in the CDR is closely approximated by an $N = 3$ Butterworth lowpass filter having a –3 dB corner frequency of 0.50 Hz like the filter used in Section 10.4. The resulting eye-diagram at the matched-filter output is shown in Figure 10-16 for $E_b/N_o = 25$ dB.

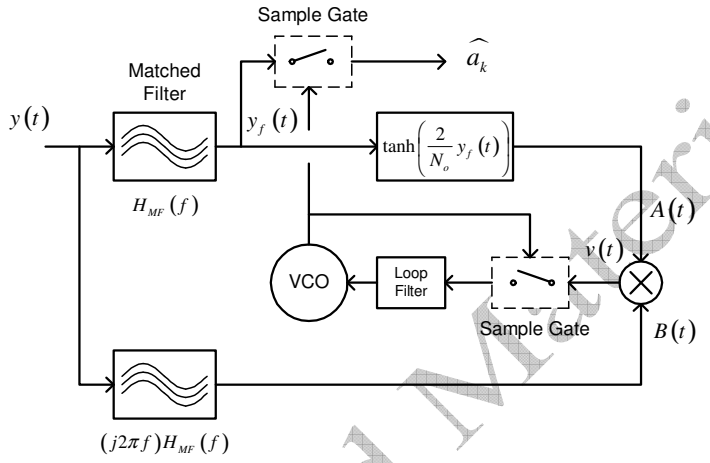

Figure 10-14 ML-CDR implemented with continuous-time filters based on the timing-error metric given by (10.21).

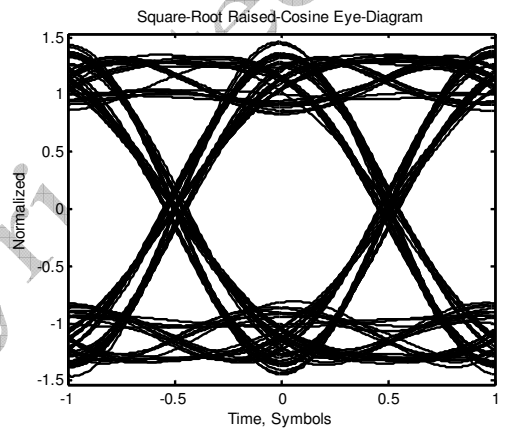

Figure 10-15 Eye diagram[15] at the data source output assuming square-root raised-cosine pulse shaping with an excess bandwidth parameter $\beta = 0.50$.

A clear understanding of the error metric represented by $v(t)$ in Figure 10-14 is vital for understanding how the CDR operates. The metric is best described by its *S-curve* behavior versus input E_b/N_o as shown in Figure 10-17. Each curve is created by setting the noise power spectral density N_o for a specified E_b/N_o value with $E_b = 1$, and computing the average of $v(\, kT_{sym} + \varepsilon\,)$ for $k = [0, K]$ as the timing-error ε is swept across $[0, T_{sym}]$. The slope of each S-curve near the zero-error steady-state tracking value determines the linear gain of the metric that is needed to compute the closed-loop bandwidth, loop stability margin, and other important quantities. For a given input SNR,

[15] Book CD:\Ch10\u14004_ml_cdr.m.

the corresponding S-curve has only one timing-error value ε_o for which the error metric value is zero and the S-curve slope has the correct polarity. As the gain value changes with input E_b/N_o, the closed-loop parameters will also vary. For large gain variations, the Haggai loop concept explored in Section 6.7 may prove advantageous.

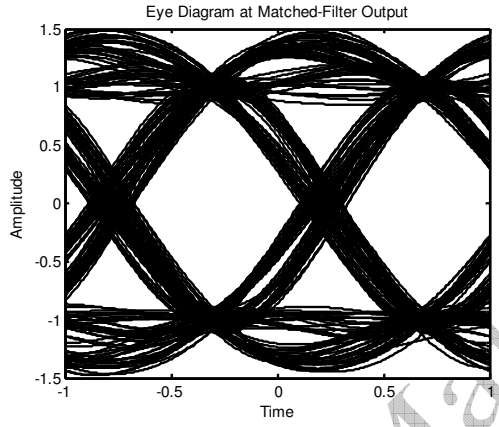

Figure 10-16 Eye diagram[16] at the CDR matched-filter output for E_b/N_o = 25 dB corresponding to the data source shown in Figure 10-15 and using an N = 3 Butterworth lowpass filter with BT = 0.50 for the approximate matched-filter.

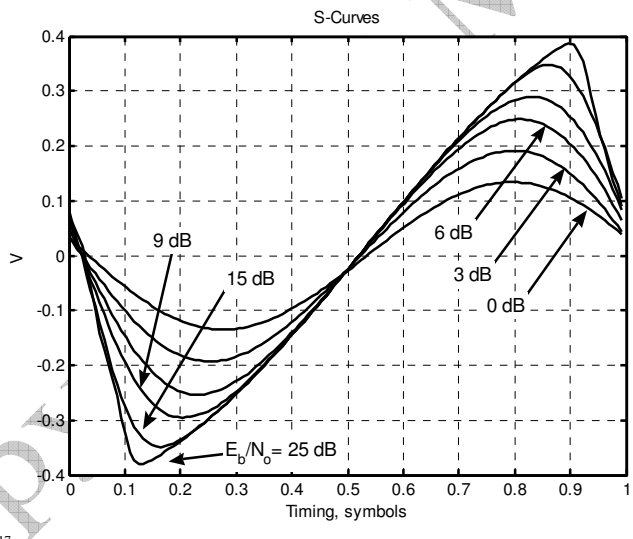

Figure 10-17 S-curves[17] versus E_b/N_o corresponding to Figure 10-16 and ideal ML-CDR shown in Figure 10-14. E_b = 1 is assumed constant.

A second important characteristic of the timing-error metric is its variance versus input E_b/N_o and static timing-error ε. For this present example, this information is shown in Figure 10-18. The variance understandably decreases as the input SNR is increased, and as the optimum time-alignment within each data symbol is approached. The variance of the recovered data clock σ_{clk}^2 can be closely estimated in terms of the tracking-point voltage-error variance from Figure 10-18 denoted by σ_{ve}^2 (V^2), the slope (i.e., gain) of the corresponding S-curve (K_{te}, V/UI) from Figure 10-17, the symbol rate F_{sym} (= $1/T_{sym}$), and the one-sided closed-loop PLL bandwidth B_L (Hz) as

[16] Ibid.
[17] Ibid.