Power Quality Enhancement by Current Controlled Voltage Source Inverter Based DSTATCOM for Load Variations

Hareesh Myneni
PhD scholar, EED
NIT Warangal
Telangana - 506 004, India
Email: hari247.sol@gmail.com

G. Siva Kumar
Member, IEEE
Asst. Professor, EED
NIT Warangal
Telangana – 506 004, India
Email: gsivakumar@nitw.ac.in

D. Sreenivasarao
Asst. Professor, EED
NIT Warangal
Telangana - 506 004, India
Email: srinudee@nitw.ac.in

***Abstract* -- In this paper, Distribution Static Compensator (DSTATCOM) is used for power factor correction, harmonics mitigation, and balancing of source currents in distribution system. In existing DSTATCOM control algorithms, dc-link voltage is maintained constant by dc voltage regulation loop (or PI controller), which give P_{loss} term of Voltage Source Inverter (VSI). In the proposed method, power quality improvement is achieved by DSTATCOM without dc-link voltage regulation loop. For that, the DSTATCOM parameters are designed in new approach. The main advantage of the proposed scheme is that, it will reduce the voltage sensing elements without affecting the compensation capability of DSTATCOM. Its performance is validated through matlab - simulink platform under various load conditions.**

***Index Terms*--DSTATCOM, dc-link voltage, harmonic mitigation, PI controller, voltage source inverter (VSI).**

I. INTRODUCTION

In distribution power system most of the loads are typical loads, such as adjustable speed drives, computer loads, electronic ballasts, refrigerators, air conditioners and other domestic, commercial appliances. Switch Mode Power Supply (SMPS) is used almost in all these appliances, it draws excessive harmonic currents and causing severe power quality problems such as poor voltage regulation, low efficiency, reactive power burden, current harmonics, high %THD and current unbalancing etc. The power quality problems and its mitigation techniques are reported in the literature [1], [2]. There are many standards proposed to control the power quality of supply system in the distribution system [3]. The power quality is improved by using the custom power devices, such as DSTATCOM, Dynamic Voltage Regulator (DVR) and Unified Power Quality Conditioner (UPQC). Among the different custom power devices, DSTATCOM is more generally used to mitigate current related power quality problems in distribution system [4]. Many DSTATCOM topologies are there for power quality improvement, some of them are, three-leg Voltage Source Inverter (VSI) with zig-zag transformer [5], [6], four-leg VSI [7], three single phase VSI and three-leg VSI with split capacitor. The three-leg VSI with split capacitor is having its own advantages such as neutral current compensation, no requirement of transformer, less number of switching devices. In comparison to normal open loop voltage Pulse Width Modulation (PWM) inverter, the current-controlled PWM inverter having more advantages: control of instantaneous current waveform and high accuracy, extremely good dynamics, compensation of dc side and ac side voltage changes, peak current protection [8], [9]. More over the performance of current controlled voltage source inverter system largely depends on quality of applied current control technique.

Different theories are presented in literature for reference compensating current generation. Some of them are *p-q* theory based extraction of fundamental active and reactive components of currents [7], Synchronous Reference Frame (SRF) theory based transformation of *a-b-c* frame to synchronous rotating frame [10], [11], instantaneous symmetrical component theory [12], and neural network theory.

PI controllers or closed loop regulators are used to calculate the power loss term (P_{loss}) of VSI, which is useful in the reference current generation [13], [14], [15]. However the power loss (P_{loss}) of VSI is fraction of average load power, so it will not affect transient response of the system [16].

In this paper, without voltage regulation loop (i.e. without considering P_{loss} term) dc-link voltage maintained constant by designing dc-link capacitor in new approach which also gives capacitor value low compare to existing design value. The main advantage of this proposed method is number of voltage sensing elements are reduced without compromising the DSTATCOM performance. Here the reference currents are generated by using instantaneous symmetrical component theory because of simplicity and good dynamic response. For load variations also the proposed DSTATCOM topology is able to compensate without dc-link voltage regulation.

II. DSTATCOM TOPOLOGY IN DISTRIBUTION SYSTEM

DSTATCOM topology in distribution power system is shown in Fig. 1. It consists of interfacing inductance (L_f), resistance (R_f), two equal dc link capacitor (C_{dc1}, C_{dc2}) and VSI. The three-phase distribution system is connected to non-linear diode rectifier load or controlled bridge rectifier load

and unbalanced *RL*-load. The source neutral point (*N*) is connected to load common point (*n*), in order to provide path for unbalanced current. In Fig. 1, the source connected to the load and DSTATCOM is connected in shunt with the load to mitigate current harmonics and load reactive power compensation. Here, v_{sa}, v_{sb}, v_{sc} are the source voltages, i_{sa}, i_{sb}, i_{sc} are currents drawn from source, i_{la}, i_{lb}, i_{lc} are load currents and i_{fa}, i_{fb}, i_{fc} are filter currents injected by DSTATCOM at the Point of Common Coupling (PCC). The capacitance values of two dc-link capacitors are equal. These two dc-link capacitors are charged to equal value through an anti-parallel diodes of an IGBT switches without applying gate signals. Designing of DSTATCOM parameters like dc-link voltage, interfacing inductor and dc-link capacitors are required for proper tracking of reference filter currents. The design process of DSTATCOM is explained in section-III.

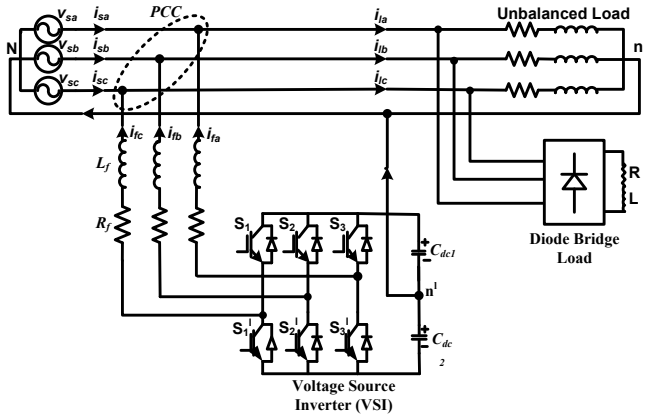

Fig. 1. Topology of DSTATCOM in three-phase four-wire distribution system

III. Design of DSTATCOM Parameters for Proposed Method

Design of DSTATCOM parameters: dc-link voltage, dc-link capacitor, interfacing inductor is discussed below.

A. *Proposed DC-link voltage* (V_{dc})

In literature, dc-link voltage is maintained constant to reference dc voltage with voltage regulation loop. Here reference dc voltage is taken as 2 times of peak of the phase voltage of source [17].

In the proposed method of compensation, dc-link voltage is maintained constant without dc voltage regulation, but it requires a proper design of DSTATCOM parameters. In order to supply compensating filter current, the current controller automatically forces the compensating current in such a way that to maintain the dc-link voltage constant. In general the dc-link capacitors are charged through anti-parallel diodes of IGBT switches of VSI to the voltage V_{dc}. In three-phase four-wire system, each dc-link capacitor is charged to peak of phase voltage, i.e.,

$$V_{dc1} = V_{dc2} = \sqrt{2}V_{ph-rms}, \tag{1}$$

where, V_{dc1} and V_{dc2} are dc-link voltages and $V_{ph\text{-}rms}$ is phase rms voltage.

B. *Proposed DC-link capacitor* (C_{dc})

In existing methods, dc-link capacitor value is calculated from the equation given below.

$$C_{dc} = \frac{2pST}{(1.8V_m)^2 - (1.2V_m)^2} \tag{2}$$

where, C_{dc} is dc link capacitor, *S is kVA* required by load, *p* is number of cycles required to control the dc voltage and *T* is system period. The design of dc capacitor value with this method gives better compensation but, the dc link capacitor value is high, leads to slow transient response [18].

In proposed topology without dc voltage regulation, for proper compensation and to improve transient response, there should be special focus on the designing of dc capacitor value. For that, Unit Capacitor Constant (UCC) is introduced in the design of capacitors, it is similar to the unit inertia constant in synchronous rotary condensers [18].

$$UCC = \frac{1}{2}C_{dc}V_{dc} / Q \tag{3}$$

where, Q = reactive power required by load, C = dc-link capacitor.

C. *Interfacing Inductor* (L_f)

The value of the interfacing inductance is selected on the basis of proper shaping of compensating current. With higher value of inductance, compensating current will not follow the reference currents, with the lower value of inductance there are large ripple in the compensating current. In designing of interface inductance, hysteresis band width and maximum switching frequency of compensator plays an important role. The maximum switching frequency occur when the instantaneous supply voltage is around its peak value [14]. The value of interface inductance (L_f) is obtained from

$$L_f = \frac{mV_{dc}}{4hf_{swmax}}, \tag{4}$$

where, *m* is modulation index, *h* is hysteresis band width and f_{swmax} is maximum switching frequency.

D. *Hysteresis band*

Hysteresis controller is a non-linear current controller [8]. The hysteresis control scheme is based on non-linear feedback loop with two level hysteresis comparators. When error exceeds given tolerance band (*h*), switching pulses are produced. In this paper, variable switching frequency hysteresis current controller is used. The controlling of switching frequency results in complex control of voltage source inverter [19]. The main advantages of hysteresis current controller are simplicity, outstanding robustness, and no tracking errors.

IV. Reference Currents Generation and Control Strategy

The DSTATCOM performance in current control mode mainly depends on generation of reference filter currents.

Many control strategies are there to generate reference filter currents and each having its own advantages and disadvantage [7], [8], [19]. The reference filter currents are generated by using instantaneous symmetrical component theory is used in this paper. The positive sequence currents and voltages are,

$$\begin{bmatrix} i_{a+} \\ i_{a-} \\ i_{a0} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix},$$

$$\begin{bmatrix} v_{sa+} \\ v_{sa-} \\ v_{sa0} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}. \quad (5)$$

The first objective is, in either three-phase three-wire or four-wire unbalanced and nonlinear load system, is to provide balanced supply currents such that zero sequence component in the system becomes zero.

$$i_{sa} + i_{sb} + i_{sc} = 0 \quad (6)$$

where, i_{sa}, i_{sb}, i_{sc} are the source currents.

The second objective is, for a predefined power factor, the relation between instantaneous positive sequence voltage (v_{sa+}) and current (i_{sa+}) is given below.

$$\angle v_{sa+} = \angle i_{sa+} + \theta_{+} \quad (7)$$

where, θ_{+} is angle between fundamental positive sequence source voltage and current and it is consider zero because of unity power factor constraint.

The third objective of compensation is, three-phase source supply only active power P_{lavg} to the load, that means the reactive power required by load is supplied by compensator (DSTATCOM). The VSI also draws real power from the three-phase supply which in termed as losses in the inverter. The power loss in inverter is very less when compare to real power drawn from source so losses are neglected.

$$v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} = P_{lavg} \quad (8)$$

where, v_{sa}, v_{sb}, v_{sc} are source voltages, i_{sa}, i_{sb}, i_{sc} are source currents and P_{lavg} is average active power drawn by load.

From equations (6), (7), (8), the solution for reference currents is

$$\left.\begin{aligned} i_{fa}^{*} &= i_{la} - i_{sa} \\ i_{fb}^{*} &= i_{lb} - i_{sb} \\ i_{fc}^{*} &= i_{lc} - i_{sc} \end{aligned}\right\} \quad (9)$$

$$\left.\begin{aligned} i_{fa}^{*} &= i_{la} - \left(\frac{v_{sa}-v_{s0}}{\Delta}\right)\left(P_{lavg}\right) \\ i_{fb}^{*} &= i_{sb} - \left(\frac{v_{sb}-v_{s0}}{\Delta}\right)\left(P_{lavg}\right) \\ i_{fc}^{*} &= i_{sc} - \left(\frac{v_{sc}-v_{s0}}{\Delta}\right)\left(P_{lavg}\right) \end{aligned}\right\} \quad (10)$$

where, i_{fa}^{*},i_{fb}^{*},i_{fc}^{*} are reference filter currents, i_{la}, i_{lb}, i_{lc} are load currents, v_{s0} is zero sequence voltage and $\Delta = v_{sa}^2 + v_{sb}^2 + v_{sc}^2 - 3v_{s0}^2$.

It is observed from Fig. 2, after getting the reference filter currents from instantaneous symmetrical component theory, error is calculated between reference filter currents and actual filter currents injected at PCC. The error is given to hysteresis controller, having inherent hysteresis band to generate the switching signal. If error is positive, top switch S_1 or S_2 or S_3 of the leg is ON. If error is negative, bottom switch S_1^1 or S_2^1 or S_3^1 of the leg is ON.

The current control forces the filter currents to follow the reference current signals produced by instantaneous symmetrical component theory.

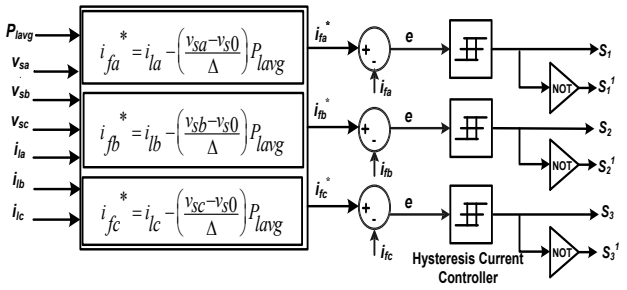

Fig. 2. Switching pulses generation for VSI of DSTATCOM.

V. SIMULATION STUDIES

In order to validate the proposed method, simulation studies are carried out in MATLAB Simulink. The system parameters used for simulation studies are given in Table.1. The simulation results for the proposed method are presented in this section for three cases.

Case A: Performance of DSTATCOM *with Unbalanced and Three-Phase Diode Bridge Load*

The source voltages, source currents, phase-*a* source voltage and source current are shown in Fig. 3 without DSTATCOM. From Fig. 3(b) and 3(c), it is observed that three-phase source currents are non-sinusoidal and unbalanced, and phase-a current lags phase-*a* voltage respectively. The phase-*a* source current %THD is 20.04% and harmonic spectrum are shown in Fig. 4. The load currents, filter currents, source currents and phase-*a* source current and source voltage with DSTATCOM are shown in Fig. 5. It is observed from Fig. 5(c), source currents are balanced and sinusoidal, and from Fig. 5(d) phase-*a* source current is in-phase with source voltage.

The voltages across the dc-link capacitors V_{dc1} and V_{dc2} are charged through anti-parallel diodes of IGBT switches and maintained constant as shown in Fig. 6(a) and Fig. 6(b). It is observed from Fig. 7, the %THD of phase-*a* source current is reduced to 1.76%, which is less than 5% recommended by IEEE 519-1992 standard.

TABLE I
SIMULATION PARAMETERS

System Parameters		Values
System voltage		200 V (Phase)
Supply frequency		50 Hz
Source R_s and L_s		1 Ω, 0.1 mH
Interfacing inductor		16 mH
dc-link capacitor		600 µF
Case:A	Three phase diode bridge rectifier load	120+ j63 Ω,
	Unbalanced load	200+ j103 Ω, 160+ j63 Ω, 100+ j110 Ω.
Case:B	Three phase controlled rectifier load	θ = 45^0, 55+ j62 Ω
	Unbalanced load	84+ j60 Ω, 70+ j121 Ω, 95+ j48 Ω.
Case:C	Load varied at t = 0.6 *sec* of three phase bridge	56+ j23 Ω at t = 0.6 *sec*
	Unbalanced load	200+ j103 Ω, 160+ j63 Ω, 100+ j110 Ω.

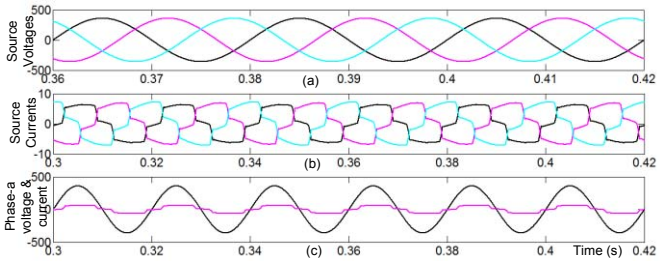

Fig. 3. Simulation results without DSTATCOM (a) source voltages, (b) source/load currents, (c) phase-*a* source voltage & current.

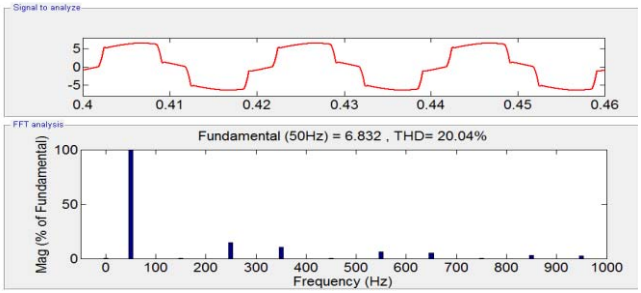

Fig. 4. Phase-*a* source current %THD & harmonic spectrum without DSTATCOM.

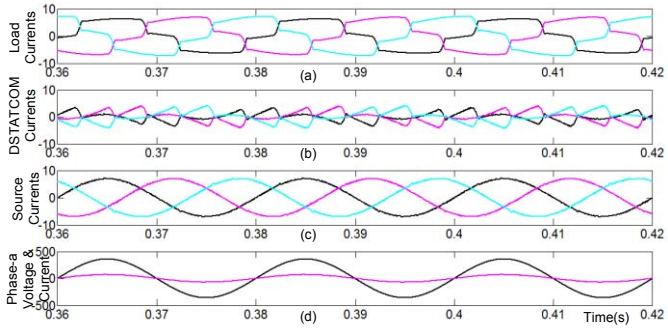

Fig. 5. Simulation results with DSTATCOM (a) 3-ph load currents, (b) 3-ph DSTATCOM currents, (c) 3-ph source currents (d) phase-*a* source voltage and current.

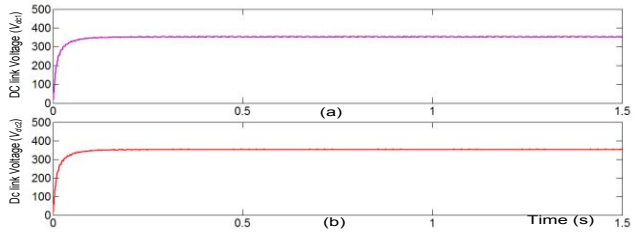

Fig. 6. (a) dc-link voltage V_{dc1}, (b) dc-link voltage V_{dc2}.

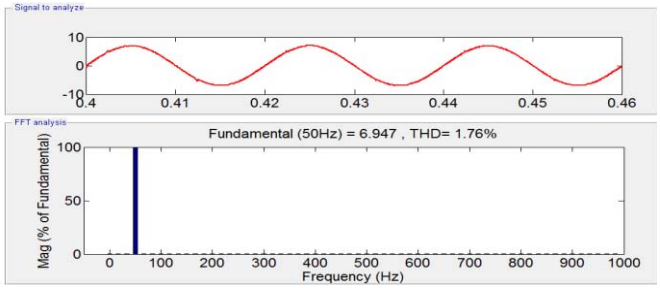

Fig. 7. Phase-*a* source current %THD & harmonic spectrum with DSTATCOM.

Case B: Performance of DSTATCOM *with Unbalanced and Controlled Bridge Load*

The three phase source voltages, source currents, phase-*a* source current and voltage without DSTATCOM are shown in Fig. 8. It is observed from Fig. 8(b) that, the three-phase source currents are unbalanced and distorted, and from Fig. 8(c) phase-*a* source current is lags voltage by some angle, due to reactive load. The phase-*a* source current %THD is 20.53% and harmonic spectrum shown in Fig. 9. In Fig. 10 shows the load current, DSTATCOM currents, source currents and phase-*a* source voltage and current. It is observed from Fig. 10(c), the source currents are perfect sinusoidal and balanced. Fig. 10(d) infers that, the source current of phase-*a* in-phase with source voltage of phase-*a*. The %THD of phase-a source current and harmonic spectrum are shown in Fig. 11, and it is observed that the %THD of phase-a current is reduced to 3.85% from 20.53%. The dc link capacitors are charged through anti-parallel diodes to the voltages V_{dc1} & V_{dc2} shown in Fig. 12(a & b)

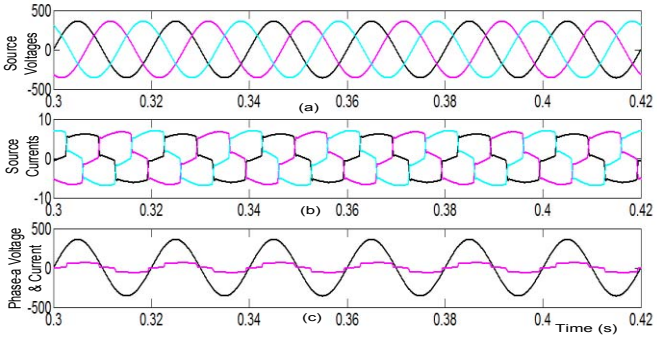

Fig. 8. Simulation results without DSTATCOM (a) 3-ph source voltages, (b) 3-ph source currents, (c) phase-*a* source voltage & current.

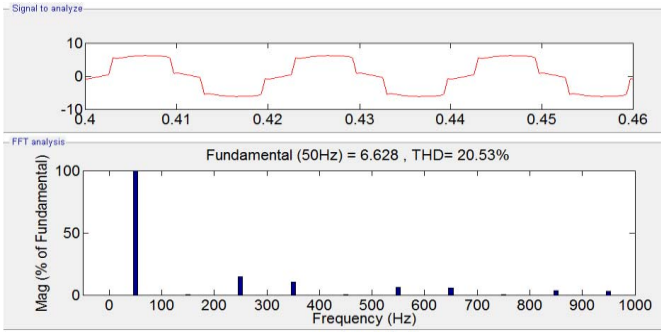

Fig. 9. Phase-*a* source current %THD and harmonic spectrum without DSTATCOM.

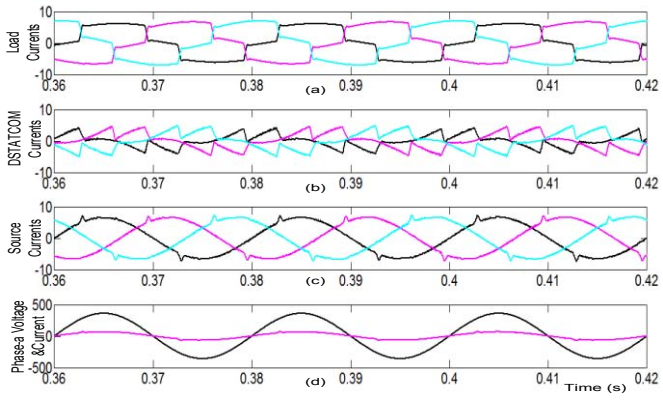

Fig. 10. Simulation results with DSTATCOM (a) 3-ph load currents, (b) 3-ph DSTATCOM currents, (c) 3-ph source currents, (d) phase-*a* source voltage and current.

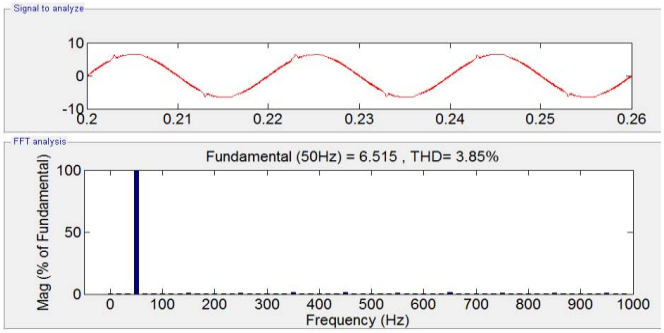

Fig. 11. Phase-*a* source current %THD and harmonic spectrum with DSTATCOM

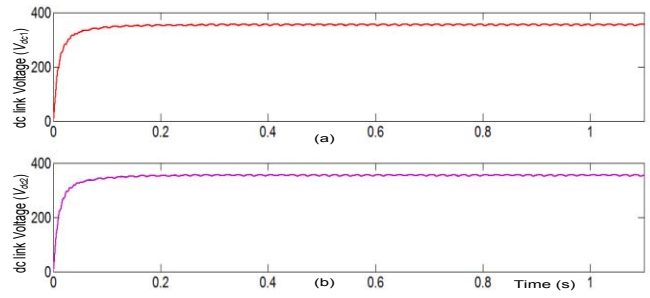

Fig. 12. (a) dc-link voltage V_{dc1}, (b) dc-link voltage V_{dc2}.

Case C: Performance of DSTATCOM *for load variations*

In order to show the effectiveness of the proposed method, the following variations are considered.

(1) At $t = 0.3$ *sec* DSTATCOM connected at PCC point.
(2) At $t = 0.4$ *sec* gate signals applied to DSTATCOM
(3) At $t = 0.7$ *sec* load decreased

In Fig. 13 shows three phase source voltages, source currents and phase-*a* source current lags source voltage without DSTATCOM. It is observed from Fig. 13(b), the source currents are non-sinusoidal and unbalanced, and from Fig. 13(c), the phase-*a* source current lags phase-*a* source voltage. The phase-*a* source current %THD is 22.93% and harmonic spectrum without DSTATCOM are shown in Fig. 14.

It is observed from Fig. 15 that, when DSTATCOM connected at PCC point through circuit breaker at time $t = 0.3$ *sec*, the current drawn from source increases suddenly and comes down to normal current after few cycles shown in Fig. 15(c), because during which the DSTATCOM draws current for charging of dc-link capacitors through anti-parallel diodes shown in Fig. 15(e) and (f). When gate signals are given to IGBT switches of DSTATCOM at time $t = 0.4$ *sec*, DSTATCOM start to send compensating currents towards PCC shown in Fig. 15(b), so that source currents are become balanced, sinusoidal which are shown in Fig. 15(c) and phase-*a* source current becomes in-phase with the phase-*a* source voltage shown in Fig. 15(d). When load decreased at time $t = 0.7$ *sec*, voltage across capacitors increased and comes to constant value near to 350V shown in Fig. 15 (e & f). The %THD of phase-*a* source current is 4.11% with DSTATCOM & harmonic spectrum are shown in Fig. 16.

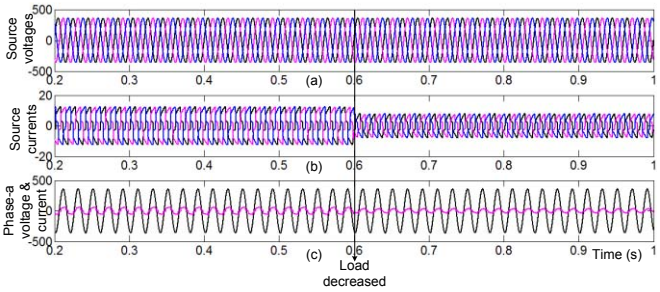

Fig. 13. Simulation results without DSTATCOM (a) 3-ph source voltages, (b) 3-ph source currents (c) phase-*a* source voltage and current.

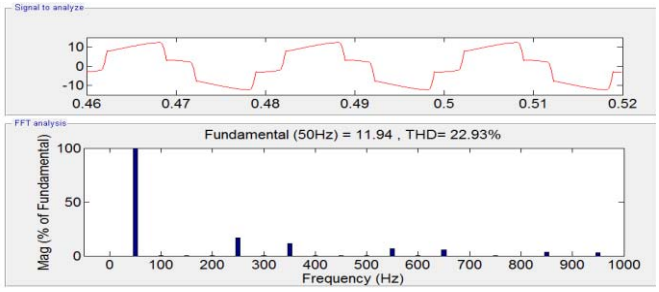

Fig. 14. Phase-*a* source current %THD & harmonic spectrum without DSTATCOM.

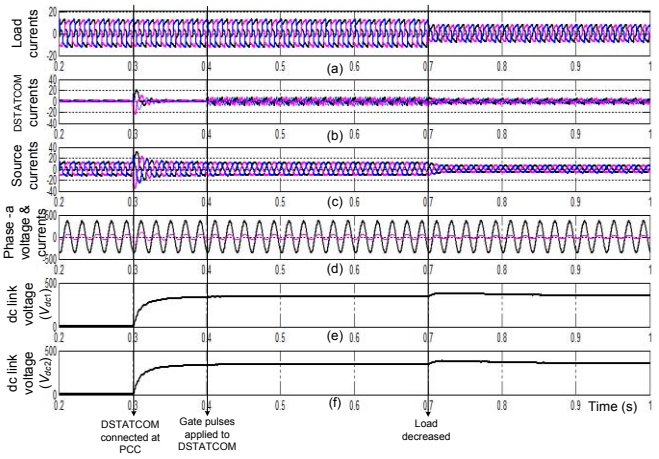

Fig. 15. Simulation results with DSTATCOM (a) 3-ph load currents (b) 3-ph DSTATCOM currents (c) 3-ph source currents (d) phase-*a* source voltage & current (e) dc link voltage V_{dc1} (f) dc link voltage V_{dc2}.

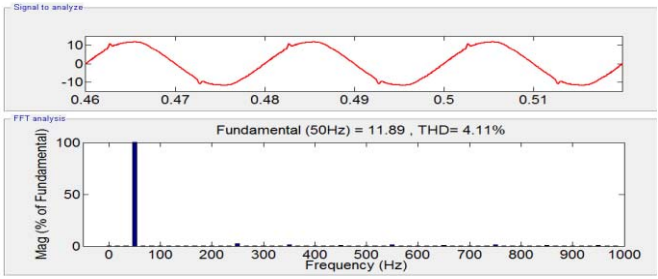

Fig. 16. Phase-*a* source current %THD & harmonic spectrum with DSTATCOM.

TABLE II
%THD OF SOURCE CURRENTS

Cases	Before Compensation %THD			After Compensation %THD		
	Phase-a	Phase-*b*	Phase-*c*	Phase-*a*	Phase-*b*	Phase-*c*
Case A	20.04	18.7	19.79	1.76	1.65	2.06
Case B	20.53	19.05	20.07	3.85	3.92	4.28
*Case C	22.93	23.03	22.31	4.11	3.98	4.86

* after t = 0.7 sec

The comparison of %THD of source currents for different cases: diode bridge load, controlled bridge load and variable load, before and after compensator are shown in Table II. The %THD values in each case are well within the limits specified by IEEE standards 519-1992. This shows the effectiveness of the proposed compensation without dc-link voltage regulation.

VI. CONCLUSION

A DSTATCOM topology without dc-link voltage regulation loop and design parameters has been explained in this paper. The suggested DSTATCOM without dc-link voltage regulation is also validated through simulation for variable loads. It is observed from simulation studies that, the performance of DSTATCOM is not affected, even without the dc-link voltage regulation. The compensation capability in terms of source current %THD, power factor correction and source current balancing is not affected under load variations also. The main advantage is dc-link voltage sensing elements are not required. It has been shown that the DSTSTCOM is able to keep the %THD of supply current within the limits according to IEEE-519-1992 standard (<5%), without dc voltage regulator also.

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