Powering mm-Size Wireless Implants for Brain-Machine Interfaces

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Powering mm-Size Wireless Implants for Brain-Machine Interfaces

by

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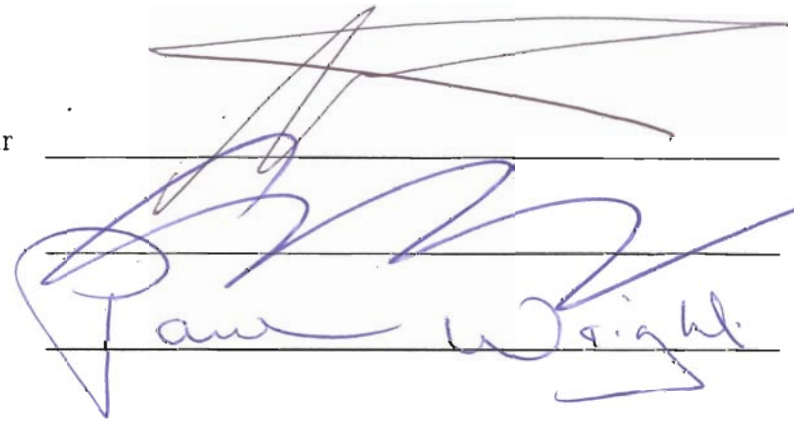

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Abstract

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Over the last couple of years, Brain-Machine Interfaces (BMI) based on microelectrode arrays have been shown to have the potential to substantially improve the quality of life for people suffering from debilitating conditions such as spinal cord injuries or limb loss. One of the most critical parts of a BMI system is the neural sensor. It is ideally implanted underneath the skull, reads out neural signals from the brain and transmits them wirelessly to a receiver outside the skull. The requirements on the electronics of such a sensor are extremely stringent, especially with respect to size and power consumption. Ideally, the overall size of the implanted sensor node is limited by the size of the sensor itself, rather than the electronics and the power source.

This work investigates powering options for implants of sizes ranging from 10 mm by 10 mm down to 1 mm by 1 mm. Wireless power transfer is identified as the most promising option of doing so and is investigated in detail. It is shown, that for a given implant antenna size, an optimum combination of external antenna and frequency of operation exists that minimizes the overall link loss. In combination with limitations on the maximum transmit and received power due to health concerns, the maximum power available to mm-size implants as a function of size is derived. Two different AC-to-DC conversion circuit topologies, covering the expected input power and frequency range, are analyzed in detail and design guidelines for each are given.

Finally, a 1 mm^3 proof-of-concept implementation of a wirelessly powered neural transponder is presented. It was tested in air and in animal and provides enough extra DC power to power a neural sensor front-end while supporting a 2 Mbps radio link. The presented tag is the smallest wireless neural tag reported to date and prooves the feasibility of remotely powered mm-size wireless neural implants.

To Petra, Gloria and Julia

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Nomenclature

AC Alternating Current

ADC Analog-to-Digital Converter

AM Amplitude Modulation

AP Action Potential

BMI Brain-Machine Interface

DBS Deep-Brain Stimulator

DC Direct Current

DIBL Drain Induced Barrier Lowering

DSP Digital Signal Processing

ECoG Electrocorticography

EEG Electroencephalography

FCC Federal Communications Commission

IEEE Institute of Electrical and Electronics Engineers

LDO Low Drop-Out

LFP Local Field Potential

MAG Maximum Achievable Gain

MEA Microelectrode Array

MEMS Micro-Electro-Mechanical Systems

MICS Medical Implant Communication Service

MIM Metal-Insulator-Metal

MOM Metal-Oxide-Metal

NIH National Institute of Health

NSA National Stroke Association

RF Radio Frequency

RFID Radio Frequency Identification

RX Receiver

SAR Specific Absorption Rate

SMT Surface Mount Technology

SNR Signal-to-Noise Ratio

SOI Silicon-on-Insulator

TX Transmitter

UHF Ultra High Frequency

UWB Ultra-Wideband

Acknowledgments

This work marks the end of an incredible journey. The last 6 years changed my life in ways I would have never even imagined. Grad school at Berkeley introduced me to my limits more than once, but it encouraged me to constantly push them and provided me with the tools to do so. It made me accomplish things I never thought I would be able to do. This clearly would not have been possible without the incredible academic and personal communities I had the luck of being part of during my time here.

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Chapter 1

Introduction

For more than 60 years, electronics have been implanted in humans, saving and transforming lives of millions of people. Back in 1958, Arne H. W. Larsson was the first human to receive a fully implanted artificial cardiac pacemaker. Although this first pacemaker lasted for only about 3 hours, Mr. Larsson went on to undergo 24 more surgeries related to various pacemakers he received until his death 43 years later. The stage for a new era in medicine was set [Larsson03]. Today, implanting a pacemaker takes only a couple of hours and can be performed under local anesthesia [NIH09]. After receiving an implant, patients only need to see a doctor for a routine check-up every couple of months. The battery of a pacemaker typically lasts between 6 to 7 years and can be replaced in an outpatient procedure [NIH09]. During the year 2007, between 800 and 1500 people per million received some sort of cardiac implant in Europe [Auricchio10]. Based on these numbers, more than 240,000 people per year are estimated to receive a cardiac implant in the U.S. alone.

Approximately around the same time as the first artificial cardiac pacemaker was implanted, significant breakthroughs in the field of electrically assisted hearing by stimulating the human cochlear were achieved. However, it was not until the late 70s, largely due to a National Institute of Health (NIH) sponsored study, until cochlear implants got enough traction to embark from a research topic towards a widely accepted medical device used by more than 30,000 people worldwide today [Eisen09, ASHA11].

Cardiac pacemakers and cochlear implants are definitely the most established and widespread electronic implants today, but a better understanding of the human physiology, paired with recent advances in micro-electro-mechanical systems (MEMS) and integrated electronics, is leading to a whole set of emerging implantable electronic devices. A number of the more recent applications are centered around the head. Some of them, such as neural stimulators, have already received FDA approval and are used today to treat conditions such as chronic pain, Parkinson's disease, tremor and dystonia [Kringelbach07]. Deep-brain stimulators (DBS) apply electrical impulses to specific parts of the brains to alleviate the symptoms of these conditions. They have also shown remarkable initial results in helping to restore some basic motor, sensory and verbal functions to patients in minimally conscious state for

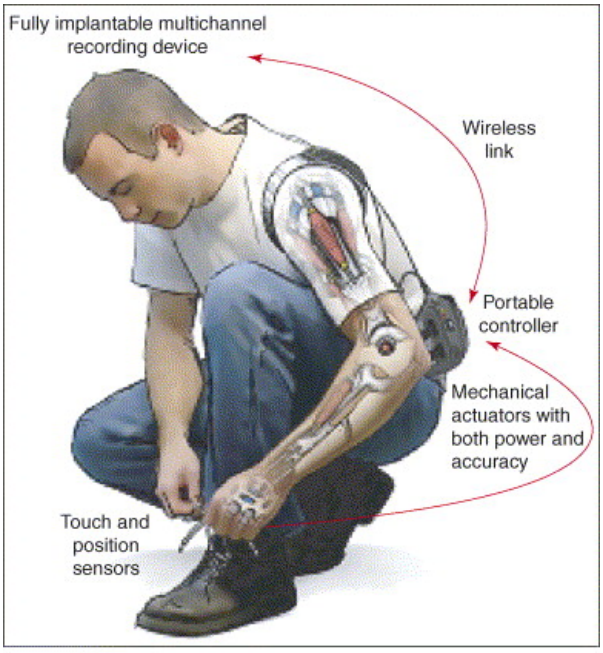


Figure 1.1: Vision of restoring full motor function after limb amputation using brain-machine interfaces [Lebedev06]

more than 12 months [Schiff07]. Other applications of implantable electronics include, for example, artificial retinas aiming to restore sight, or brain-machine interfaces (BMI) enabling direct communication between the human brain and a machine such as a computer. They are at a much earlier stage compared to the previously introduced technologies and topics of a lot of contemporary research in a number of fields, including neurology, signal processing, fabrication and electronics.

One of the ultimate goals of brain-machine interfaces is to restore full motor function for people suffering from conditions such as spinal cord injuries or loss of limbs. Fig. 1.1 shows a cartoon drawing of how such a system could look, indicating the various components that are involved (from [Lebedev06]).

At the University of California at Berkeley, a collaborative effort between the Brain-Machine Interface Systems Laboratory and the Berkeley Wireless Research Center is focusing on building a library of components for miniature, fully implantable, wireless neural recording devices suitable for different applications. Within this framework, one of the main goals is to build a versatile set of tools that enables researchers to conduct experiments that allow them to gain further insight in the way the human brain operates, while building devices that allow long term operation without sacrificing the patient's comfort. To achieve this, research is carried out on virtually all aspects of the implant such as signal acquisition, data-communication, fabrication and assembly issues. One of the aspects that is very often neglected or overlooked, is the power supply of the implants. The main challenge here is

the limited space available as well as the difficulty of getting access to the device once it is implanted. This work is therefore dealing with the question of how to power mm-size implantable devices suitable for brain-machine interfaces.

The remainder of this chapter gives a more detailed overview of the application, the electronics available today and various options for powering implanted electronics. It then summarizes the state-of-the-art for wireless power transfer to implanted electronics and is concluded by an outline of this work.

1.1 Brain-Machine Interfaces

Between 15 to 40 people per million per year suffer from incidents leading to spinal cord injuries [Sekhon01]. In the US alone, 262,000 people are estimated to suffer from spinal cord injuries with approximately 12,000 new cases each year [NSCISC10]. Approximately 795,000 strokes were estimated to occur in the US in 2010 [NSA10]. According to the National Stroke Association (NSA) about 80% of the people suffering from a stroke have some degree of trouble moving one side of their body, or at least experience a weakness of it. On top of that, a lot of stroke survivors have troubles using and comprehending words. Brain-machine interfaces have the potential to help a lot of these people by sensing neural activity and translating it into movement or speech. Beyond that, BMIs may be able to enhance sensorimotor performance of humans or open up new ways of communication.

1.1.1 Neural Signals

When it comes to recording neural signals, different methods, depending on the level of invasiveness and the targeted spatial resolution, exist. Fig. 1.2 depicts the various methods according to their spatial resolution. Electroencephalograms (EEG) are taken by placing sensors on the skin on top of the head and are thus completely non-invasive. BMIs based on this approach are used for fairly simple coarse control, wheelchair operation or communication. However, with a rather low transfer rate of currently 5-25 bits/second they might not be sufficient to support movement of a limb requiring multiple degrees of freedom [Lebedev06]. EEG recordings represent the combination of the electrical activity of a large number of neurons and therefore suffer from low spatial and temporal resolution. On top of that, the tissue consisting of brain, bone and skin acts as a low-pass filter for the signals, further reducing the information content of the recorded signals.

Implanting electrodes subdurally allows recording from a smaller cortical area and up to higher frequencies ($>$ 30 Hz) due to the reduced filtering effect of the tissue. This method is called electrocorticography (ECoG). Owing to the higher resolution and frequency content, ECoG based BMIs are expected to have better accuracy and require shorter training times compared to EEG based ones [Leuthardt04]. However, even with ECoG recordings,

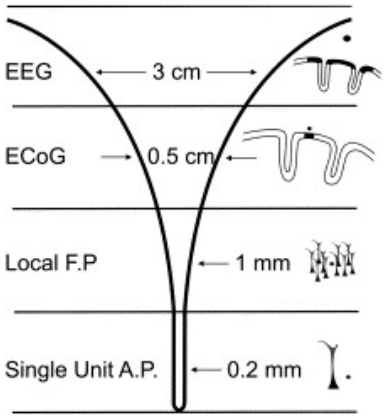


Figure 1.2: Methods for recording neural signals and their spatial resolution [Schwartz06]

restoring full, close to natural, motor control of prosthetic limbs seems unlikely [Lebedev06]. Recordings of even higher resolution signals are necessary to achieve this goal. Electrodes with diameters of only a few 10s of μm, penetrating the brain 100s of μm to a few mm deep are required to get signals with the desired properties. Such microelectrodes allow recording local field potentials (LFP) as well as single unit action potentials (AP), often referred to as spikes. Obviously such an approach is much more invasive than EEG or even ECoG, but the increased signal fidelity outweighs the increased safety risks in many cases. The remainder of this chapter focuses therefore on systems based on LFP and AP recordings.

Fig. 1.3(a) shows a typical signal recorded from the motor cortex of a rat using microelectrodes [Venkatraman07]. The recorded signal is a combination of the local field potential, the action potentials, and a DC offset as large as $\pm$50 mV due to electrochemical processes at the sensor interface. The LFP and the AP signals contain their information in different frequency bands and can therefore be separated in the frequency domain. The action potentials occupy the 300 Hz to 10 kHz band, while the LFP frequencies are typical below 300 Hz. Fig. 1.3(b) and (c) show the AP and LFP extracted from the recording in Fig. 1.3(a), respectively. Typical signal amplitudes of both, the APs and the LFP, range from 10 μV to 1 mV. While the LFP is a summations of signals created in a sphere around the recording site, the action potentials are associated with single neurons [Scherberger05]. Although the LFP and the AP tend to represent different sources, recent research has shown that there is some correlation between the two [Schwartz06]. Most BMIs targeting high fidelity prosthetic control use the AP to derive the control signals for sophisticated movements. The actual information of the APs is encoded in the rate at which the spikes occur, with an active neuron firing more rapidly (up to 100 times per second [Harrison07b]) than an inactive one (up to 10 times per second). The LFP on the other hand, has potential information on the planning and execution state of movements and can therefore be a valuable supplement to AP recordings to enhance the performance of BMIs [Scherberger05].

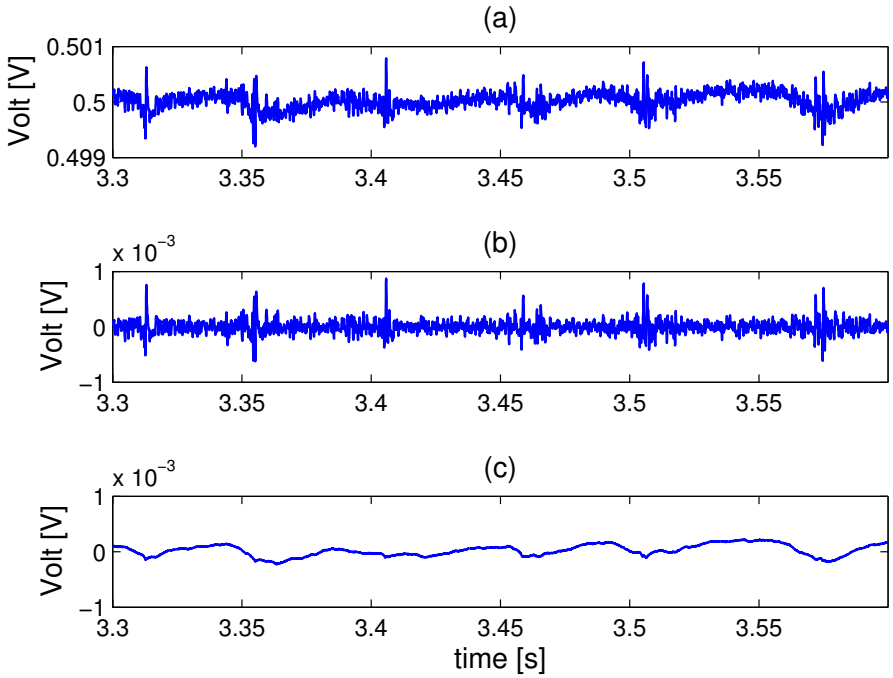


Figure 1.3: Microelectrode recording from motor cortex of rat (based on [Venkatraman07])

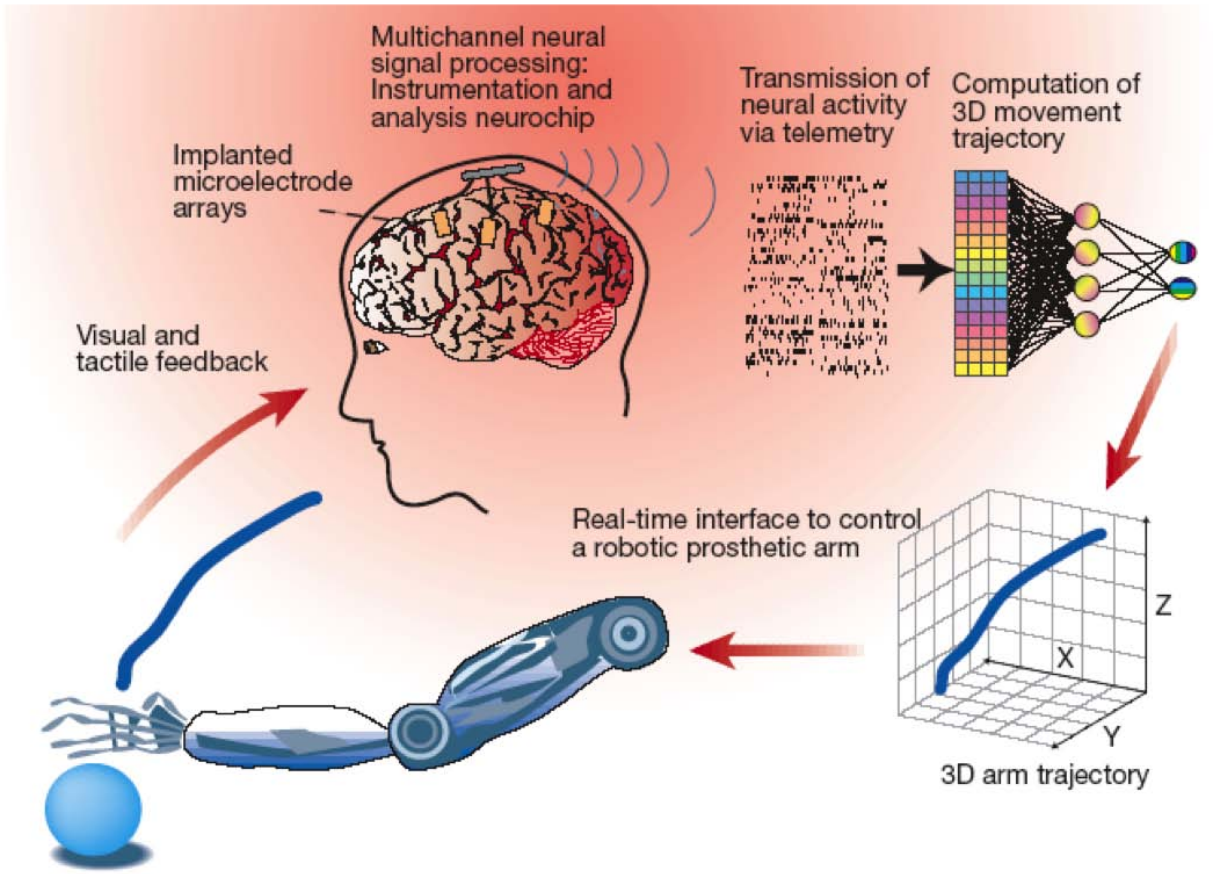


Figure 1.4: Principle of BMI enabled control of prosthetic arm [Nicolelis01]

1.1.2 System Level

The principal components of BMIs controlling prosthetics are outlined in Fig. 1.4. A number of microelectrode arrays are implanted in the brain recording APs and LFPs. All of them are connected to a sensor interface that collects the data, pre-processes it if necessary, and wirelessly transmits it through the skull. Outside the body, signal processing is applied to decode the recorded neural signals and translate them into movement trajectories that can then be used to control the prosthetics. Finally, feedback, both visually and tactile, is used to close the loop [Nicolelis01].

1.1.3 Single Cell Recording

Recordings from single unit neurons are typically obtained using microelectrode arrays (MEA), sometimes also referred to as multielectrode arrays. Some examples of popular electrodes are shown in Fig. 1.5. A single electrode is typically less than 50 μm thick at

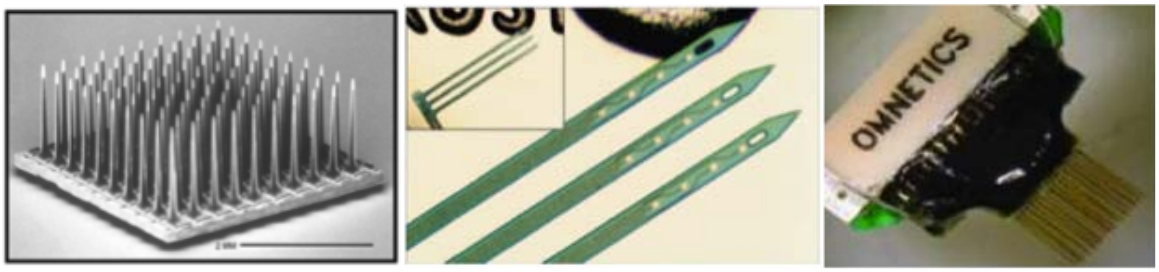


Figure 1.5: Various neural probes (a) Utah Array [Harrison07b], (b) Michigan Probes [Wise04], (c) Plexon Microwires [Nicolelis03]

its tip and at least 1 mm long. The spacing between the probes is on the order of a few 100 μm and the recording sites are either sitting along the shaft or right at the tip of the single electrodes. One single recording site might detect APs from up to 5 neurons, although the average number of neurons within recording range is more in the range of 3 to 4 [Nordhausen96]. A surgical procedure is required to implant the probes in the brain such that the recording sites are on the order of 1 mm deep in the brain.

One of the biggest problems with microelectrode arrays is to get stable, long term recordings once they are implanted. This has to do with the immunoresponse of the brain tissue. After the probes are inserted, the human body starts forming scarring tissue around them. This scarring tissue gets in between the recording site of the electrode and the neurons the electrode is supposed to record from [Polikov05]. As a result of this the signal-to-noise ratio (SNR) of the recorded signals degrades over time and eventually becomes too low to extract reliable information. While this does not happen in 100% of the cases, it typically happens within weeks of the insertion, limiting the overall usefulness of of MEA-based BMIs to acute rather than chronic applications. Fig. 1.6 shows the tissue response to an inserted microprobe over the course of 12 weeks [Turner99]. A number of research projects focus on overcoming this problem, including approaches investigating different materials and/or shapes of electrodes or improving the surgical procedures to implant the electrodes. Other attempts try to limit the micromotion *in-vivo* to enhance the longterm performance of the electrodes, but so far none of them lead to a major breakthrough yet [Polikov05].

1.2 BMI Electronics

Requirements for the electronics interfacing with microelectrodes in order to acquire LFP and AP signals required for high quality motor control are fairly stringent. Ideally, the chip containing all the necessary electronics connects directly to the MEA and is therefore implanted together with the electrodes. As a result of this, it is located on top of the brain, right underneath the skull. Due to the limited available space and in order to minimize friction with the surrounding tissue due to micromotion, the electronics is heavily limited

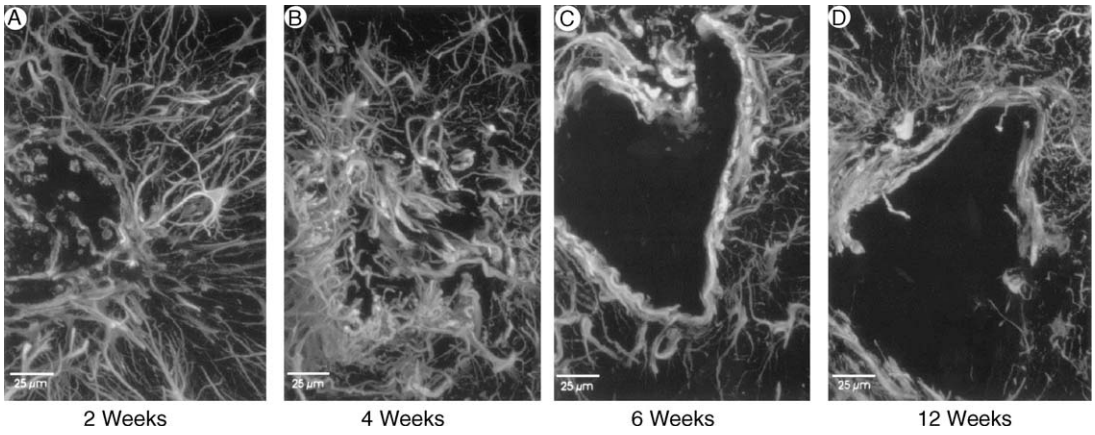


Figure 1.6: Tissue response to microprobes over time [Turner99]

in size and ideally not bigger than the MEA itself. In order to support a range of different electrodes, the systems considered in this work cover a size range of 1 x 1 mm^2 to 10 x 10 mm^2. To minimize the risk of infection associated with transcutaneous wires for communicating with or powering the device, such wires have to be avoided as much as possible. A wireless interface is therefore essential to relay the information recorded by the device through the skin.

Fig. 1.7 shows a system block diagram of a generic BMI circuit. Neural amplifiers are directly interfacing with the electrodes and are typically succeeded by analog-to-digital converters (ADC) digitizing the recorded signals. Digital signals processing (DSP) can be used to perform data reduction to relax the requirements on the wireless interface. Finally a transmitter (TX) transmits the data transcutaneously to the receiving unit. The receiver (RX) included in the system can be used to adapt the DSP unit as needed or receive information for microstimulation. A microstimulator is needed when the system is implementing neural stimulation to provide sensory feedback to the brain to close the control loop. As for any other active electronic circuit, some sort of power supply is needed as well. Due to the wireless operation and the limited space available, providing enough power to support all the building blocks can be very challenging.

In the following sections the various building blocks are discussed in more detail.

1.2.1 Signal Acquisition Front-End

The signal acquisition front-end is the direct interface to the microelectrodes. It records LFP and AP signals as small as a few μV while coping with DC offset voltages up to a few tens of mV, and ideally converts them into the digital domain. Due to the rather large offset compared to the minimum expected signal levels, the offset needs to be removed in order to prevent the electronics from saturating and not being able to amplify the signals of

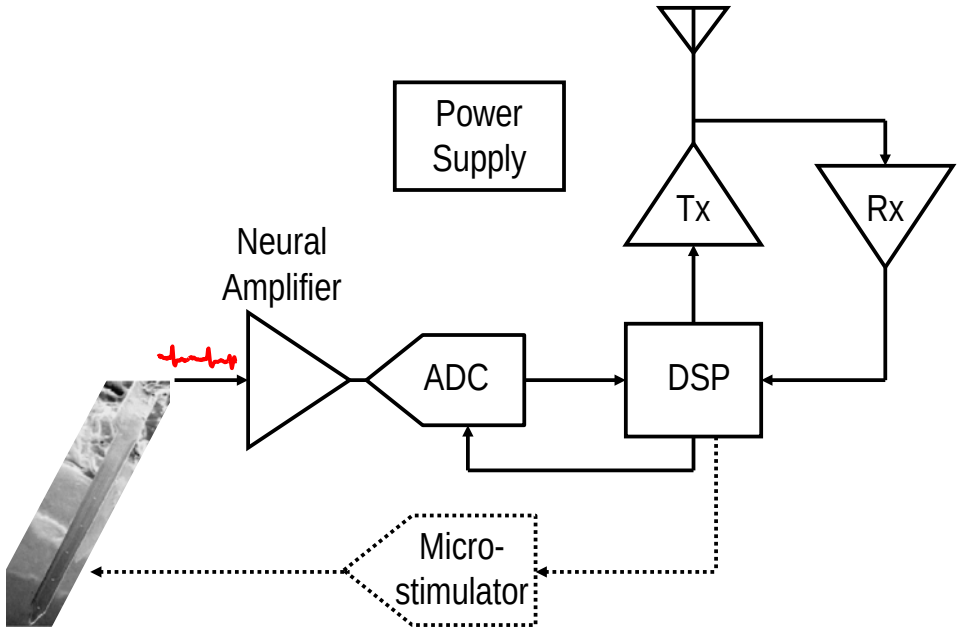


Figure 1.7: Generic BMI system diagram

interest. Since the frequencies of interest in the LFP and AP are in the 10s of Hz to kHz range, separating the offset from the rest of the signal typically requires a large chip area occupied by passives synthesizing large time constants [Harrison06, Wattanapanitch07, Aziz09, Xiao10]. An alternative approach uses digital techniques to cope with the offset and separate the LFP from the AP, leading to a substantial reduction in size as well as minimum supply voltage [Muller11]. State-of-the-art signal acquisition front-ends operate at supply voltages below 1 V, consume as little as 0.64 μW and are as small as 0.013 mm^2 [Xiao10, Muller11]

1.2.2 Data Reduction

With sampling rates of up to 32 kSps, ADC resolutions of around 10 bits and up to 4 neurons captured per recoding site, the raw data rates produced by a single recording site can be larger than 1 Mbps [Rabaey11]. The data rate requirements for the size and power constrained wireless transmitter can therefore become prohibitively high especially when recording from MEAs containing on the order of 100 recording sites, such as the Utah Array. Since a lot of the recorded information might be redundant and good overall system performance could be achieved by using only information on the APs, on-chip digital signal processing can be used to reduce the amount of data significantly. The current belief in neuroscience is that the information at what time a particular neuron spikes is enough to achieve good motor control [Lebedev06]. Due to different distances between the recording sites and the different

neurons they record from, the recorded action potentials typically differ in amplitude and shape from each other. In a lot of cases it is therefore enough to transmit only the recorded signal for a short period of time after a spike is detected. Spike detection can be done by simple thresholding and, due to the limited duration of the action potentials, transmitting data recorded for a few milliseconds combined with a timestamp is sufficient. Approaches based on this so called "spike extraction" principle can reduce the data rate by approximately 95% [Rizk07]. Even more aggressive approaches detect and sort the spikes on chip and only transmit a timestamp and a spike identifier leading to another 90% or more reduction in data rate [Harrison07b]. A factor of 200 between highly compressed and raw AP data is therefore achievable.

1.2.3 Micro Stimulation

Micro-stimulation is the ultimate tool to close the loop of BMI-based control systems by providing feedback directly to the brain. By injecting charge into the brain via microelectrodes, somatosensory feedback can be provided to the patient [Schwartz06]. Typically, bi-phase current pulses with an amplitude of 10s of μA are applied to the microelectrode for around 200 μs to successfully stimulate the neurons [Tehovnik96, Wise04, Venkatraman09]. Combined with a typical electrode impedance of 100 kΩ ([Nordhausen96]) and a maximum rate of 100 stimulations per second, stimulating neurons via a single electrode can be accomplished with less than 1 μW. The data rate to control the stimulation is comparable to the data rates for recordings applying spike sorting, since basically only timing and stimulation site identification information is needed. While most current BMI systems mainly focus on the recording of neural signals, systems capable of both recording and stimulation will most likely be needed to realize the vision of high-fidelity, brain controlled prosthetics.

1.2.4 Data Communication

In order to facilitate a system that is able to record data and stimulate neurons, a two way data link is needed. Complete wireless operation is preferred for medical as well as cosmetic reasons as mentioned before. In most cases, being able to communicate through approximately a centimeter of tissue comprised of mainly bone, fat and skin is sufficient ([Mark10a]), since a more powerful device placed outside the head can take the data from there. While the data rates of the transmitter can be highly reduced by applying the data-reduction techniques described before, access to raw data recordings might still be required for research purposes; be it just for evaluation purposes of existing or new data reduction algorithms or for fundamental investigations like, for example, such as examining the recordings for signal content that has not been discovered yet. Depending on the application, the required data rates might therefore vary between a few kbps and 100s of Mbps [Rabaey11]. The data receiver is needed to control the micro stimulation and might also be needed to tune the data acquisition and/or reduction. Since the latter typically happens only occasionally, the

data rates are mainly determined by the stimulation. Due to the rather simplistic stimulations patterns and the fact that no more than 100 stimulations per neuron per seconds are required, the data rates for stimulating via a single microelectrode are only on the order of a few kbps.

Due to the specifics of the application, highly non-symmetric radio architectures are the most likely candidates to achieve the desired performance while meeting all the constraints. While the implanted device is severely limited in size and power, the external device is, to first order, not limited by these constraints at all. Since recording is the primary application for most integrated BMI systems up to date, most work has been focusing on the data transmitter. Published transmitter systems are based on three different architectures: Low-data rate passive, medium data rate active narrowband, and high data rate active ultra-wideband (UWB) radios. Achieved data rates range from 150 kbps to 90 Mbps while consuming between less than 20 μW and 1.6 mW for the TX only, respectively [Xiao10, Harrison09, Chae09].

Although the required data rates per channel for the implant's receiver are not as high as the ones for raw data recording, they can achieve a few 100 kbps if interfacing to e.g. the Utah Array. Most of today's BMI systems do not support high data rate receivers since they do not include neural stimulation capabilities and therefore do not need the high data rates. Some systems have receivers based on simple modulation schemes such as ASK, supporting data rates of less than 10 kbps to configure the on-chip data reduction hardware [Harrison07b]. Dedicated receiver systems operating in the Medical Implant Communication Service (MICS) band achieve data rates of up to 250 kbps while consuming less than 500 μW [Bohorquez09, Bae09]. A few systems targeted towards retina implants support higher data rates up to 2 Mbps while consuming more than 5 mW [Chen10]. With the increasing need for closed loop BMI control and therefore large scale neural stimulation more systems incorporating medium data rate receivers will almost certainly appear in the near future.

1.2.5 Power Supply

Probably the most commonly used energy source for implantable electronics are batteries. They have been used in cardiac pacemakers for decades and therefore been proven to pose no significant threat to the health of patients. This is achieved by proper encapsulation with some sort of biocompatible material such as steel, which reduces the battery performance when scaled down to mm-size [Heller06]. While the fairly low power density and their limited cycle time is not a problem for applications such as pacemakers, where the device is rather large, the average power consumption of the implant is rather low and the replacement is done during a fairly low-risk outpatient procedure every couple of years, it severely limits the usefulness for applications such as brain-machine interfaces. Miniature batteries consisting of potentially harmless anode and cathode materials and using the subcutaneous interstitial fluid as electrolyte, therefore not needing any encapsulation, have been reported, but their lifetime is currently limited to less than 1 month [Heller06]. Given the small target form

factor combined with the low energy densities or the limited lifetime of implantable batteries, battery replacement, requiring surgery on the open skull, on the timescale of month would be required. This is clearly not a good option for chronical deployment of BMI sensors.

Energy harvesting within the body could potentially eliminate the need for replacing the battery and is thus a very interesting alternative. Areas of research for biomedical applications include bio-fuel cells utilizing glucose from blood [Mano08] or thermoelectric methods to harvest energy from natural temperature gradients within the body [Paradiso05]. While the results emerging from these fields keep on improving, the power densities currently reported, as well as limited longevity, still limit their usefulness for a lot of applications today. Besides that, it remains unclear if, in the case of brain-machine interfaces, enough resources (e.g. in terms of thermal gradient or glucose concentration) are continuously available to guarantee reliable and prolonged operation of the implant.

Vibration-based harvesters might be suitable for certain applications under certain conditions, but the reported power densities for lightweight, mm-size harvesters is even lower than for the harvesting technologies mentioned above [Reilly09].

Another powering technique that is well established in the medical field is powering via electromagnetic power transfer. There, an external transmitter generates an electro- and/or magnetic field that is harvested by the implanted device and converted into a stable DC supply voltage. Depending on the frequency of operation, the separation of the transmitter and the implant, and the antennas used, the energy can be transferred purely via magnetic or electric near fields or through electromagnetic fields. Power coupling via magnetic near fields has been used in a wide variety of applications and it is also the main source of power for cochlear implants. Due to the more than 30 years of history of cochlear implants used in humans, this powering option has proven to be a safe and, with proper design, reliable alternative to batteries. Without any moving parts or the need for chemical processing or temperature gradients, it also seems more robust and durable than the energy harvesting options described before. It still requires a battery, but this time it is located outside the body and can easily be replaced without the help of a doctor. One of the limitations and key concerns are potential adverse health affects associated with high electromagnetic fields in the vicinity of the human body. The maximum transmit power therefore has to be limited to levels that are considered to be safe, as restricted by the Federal Communications Commission (FCC) or recommended by the Institute of Electrical and Electronics Engineers (IEEE) [Cleveland99, IEEE06].

Table 1.1 lists power density levels for the powering options mentioned above. It clearly shows that electromagnetic powering is the most promising in terms of power per area for mm-size devices at this moment. This work therefore focuses on building and optimizing electromagnetic power transfer to mm-size implants.

Principle and Constraints	Power Density
Primary batteries [Roundy04]	0.09 μW/mm^2/year
Glucose bio-fuel cell utilizing glucose from blood (5 mM) [Mano08]	2.8 μW/mm^2
Thermoelectric, ΔT=5°C [Paradiso05]	0.6 μW/mm^2
Piezoelectric microbender, f $\approx$ 800 Hz, 2.25 m/s^2 [Reilly09]	$<$ 0.2 μW/mm^3
Electromagnetic power transfer	10 to 1000 μW/mm^2

Table 1.1: Power densities of various energy source for biomedical implants

1.3 State-of-the-Art

Wireless power transfer to power implantable devices has been around for at more than 50 years [Schuder61]. Historically, most systems operate based on inductive coupling and at low frequencies due to the fear of increased tissue interaction at higher frequencies [Poon10]. Over the years, a lot of effort has been devoted analyzing and optimizing inductive links for implants [Donaldson83, Harrison07a], leading to BMI systems powered by antennas as small as 5 x 5 mm^2 [Harrison09]. While a lot of focus was put on optimizing coil geometries, a holistic investigation of the optimum frequency of operation was excluded from the optimization space, and quite often the frequency of operation was chosen based on regulatory or practical system considerations [Harrison07a, Harrison07b].

It was not until recently, that higher frequencies in the 100s of MHz to low GHz range have been shown to be more optimal for mm-size implants targeted towards brain machine interfaces [Poon07, Poon10, Mark10b, Mark11a, Rabaey11]. Transcutaneous power delivery systems for brain-machine interfaces operating at frequencies around 1 GHz have been published since then, but typically without finding the global optimum based on the main degrees of freedom of the power link (TX antenna, RX antenna, frequency of operation) [O'Driscoll09, Xiao10].

Table 1.2 summarizes representative wireless power transfer systems for implantable, mm-size BMI systems. While it is hard to compare different work due to incomplete information on important parameters such as transmit power, antenna size or tested link conditions, it provides a good overview for what has been achieved and what the challenges are. The missing information on the transmit power makes it especially hard to compare different approaches.

Related to the transmit power is another aspect that is more or less neglected in work published so far: safety concerns related to exposure of humans to electromagnetic fields such as the ones suggested by the IEEE [IEEE06] or mandated by authorities such as the FCC or the European Commission [Cleveland99, CEU99]. These limitations set a limit on

Reference	[Yu03]	[Harrison07b]	[O'Driscoll09]	[Xiao10]
Implanted Antenna Size [mm x mm]	not stated	5 x 5	2 x 2	10 x 15
Frequency [MHz]	4	2.64	915	915
Link Parameters	10 mm air	10 mm air	15 mm bovine muscle	not stated air
Transmit Power [mW]	2100	not explicitly stated	250	not stated
Received Power [μW]	22900	13400	200	160
Minimum Input Amplitude [V]	5.6	3.55	0.7	0.125
Power Available for Electronics [μW]	20700	10800	140	20
Available Power/Area [μW/mm^2]	not stated	432	35	0.13

Table 1.2: Comparison of published wireless power transfer work for BMIs

the maximum transmit power that can be considered safe. While some of these limitations and recommendations are controversial, they are an aspect that cannot be neglected when building systems that are targeted towards long term deployment in humans. Since the maximum allowable transmit power depends on the frequency, it is an important metric when comparing systems operating at different frequencies. Some first order analysis of the system reported by Harrison et al. for example, suggests that the H-field generated by the external antenna exceeds the values stated in the IEEE recommendations ([IEEE06]) by a factor of more than 4. Adjusting the transmit power to be compliant with the IEEE standard would reduce the received power by a factor of more than 16. Due to the proximity of the field source to the body, a more elaborate analysis on whether the basic restrictions on *in-situ* fields are actually violated in this case needs to be carried out, but as the first order analysis shows, the results are very likely to reduce the amount of received power substantially.

When comparing the difference between received power and power available to the implant's electronics another challenge with mm-size implants becomes apparent. The systems that are designed to receive 10s of mW of power consume more than one mW to convert that power into a useful supply for the electronics. With the received power approaching sub-mW levels, be it due to reduced transmit power due to health concerns or reduced implant antenna sizes, spending that much power on the energy conversion is not an option. Novel, more efficient conversion schemes are therefore needed to make powering devices approaching 1 mm by 1 mm feasible.

All of the reported systems, apart from the work by O'Driscoll et al. ([O'Driscoll09]), were tested in air only. While the results for the systems operating at low frequencies might not change too much once implanted, systems operating at higher frequencies are more susceptible to tissue interaction and *in-vivo* testing is crucial to verify functionality. O'Driscoll et al. were using a 15 mm thick layer of bovine muscle tissue to test his system, which is definitely better then just testing it in air, but does not necessarily mimic the fully implanted case realistically enough.

The smallest power delivery system targeting BMI systems reported so far operates at 915 MHz and uses a 2 x 2 cm^2 power transmit (external) loop and a 2 x 2 mm^2 power receive (implanted) loop antenna. It provides 140 μW of power to the implant at an overall efficiency of -33.2 dB [O'Driscoll09]. However, it assumes a fixed external antenna geometry and does not explicitly treat it as a design variable. Further, it does not provide evidence that it adheres to health related regulations.

1.4 Thesis Outline

The main objective of this work is to holistically optimize power transfer links for BMI systems of different sizes, ranging from 1 x 1 mm^2 to 10 x 10 mm^2, and establish how much power can safely be made available to the implant to perform tasks such as data communication, signal acquisition, or stimulation. This systematic approach sheds light

on the power constraints for various sized implants and lays the foundation for further miniaturization of implantable electronics.

In order to obtain global optimums, both the external antenna and the frequency of operation are treated as design variable. Numerical simulation tools are adapted and used to predict and optimize the link performance. Circuit implications of the link parameters are investigated and different circuit architectures tailored to the various use cases are proposed. In order to verify the theories and simulations, a proof-of-concept 1 x 1 mm^2 system, co-designed with a data transmitter, was build in 65 nm CMOS and tested *in-vivo*.

Chapter 2 introduces the concept of holistic optimization of the wireless links for implantable devices. Trends for the optimum frequency as well as the geometry of the external antenna for different implant sizes are derived and the effect of tissue on the link is investigated. The specific absorption rate (SAR) is introduced as a metric to quantify the amount of power being absorbed by the tissue and converted into heat. Based on limitations on the SAR, set by health concerns and the overall link efficiencies, expected input power and voltage levels for different sizes of implants are calculated.

Based on the findings of chapter 2, different architectures and circuits to convert the alternating input signal to a DC voltage that can be used to power the implanted electronics are introduced and analyzed in chapter 3. The conversion efficiencies of the various systems are combined with the amounts of power available to the implant derived in chapter 2 to predict the useful power available to the implant. It also introduces duty-cycled power transmission as a mean to overcome low efficiencies inherent to rectifying low voltage AC signals.

A proof-of-concept 1 mm^3 wireless power delivery supporting a neural transponder while providing excess DC power for additional sensing or actuating capabilities is described in chapter 4. It includes a novel external antenna design that reduces the SAR for a given transmit power and describes the co-design of the power delivery system with the data transmitter in detail. Measurement results of lab bench as well as *in-vivo* system tests are also included in this chapter.

Finally, the results are summarized in chapter 5. Strengths and weaknesses of the proposed solutions are discussed and some directions for future research are suggested.

Chapter 2

Wireless Power Transfer

When it comes to wireless transfer, a good understanding of the wireless channel is crucial, regardless of whether it is information or power that is transferred. In the case of wireless transfer to implants, the channel consists of layers of various kinds of tissues, each having frequency dependent dielectric properties. In order to find the optimum link parameters such as frequency of operation and antenna geometries, full-wave electromagnetic simulations are required, since it is not clear whether the link loss is minimized when operating in the near or the far field, or somewhere in between [Poon10]. Using good models for the tissue parameters is crucial for the accuracy of the simulations.

This chapter describes the specifics of the wireless links associated with implanted BMI systems and investigates the impact the different factors have on the power available at the terminals of the implant's antenna. It starts by outlining the framework under which the link is investigated and continues by describing the process of link optimization under constrained implant sizes. The effects of tissue on the link parameters are investigated and the concept of specific absorption rate as the limiting factor for the created external electromagnetic field is introduced. Finally, the maximum power and expected voltage levels available at the terminal of the implanted antenna are derived by combining SAR and thermal constraints, link loss, and antenna impedance.

2.1 Framework

Due to the challenging size and power constraints, mm-size implanted wireless devices are only capable of operating over distances of a few cm at best. The configuration for the BMI systems this work is focusing on consists therefore of a miniature, implantable wireless sensor sitting on top of the brain, directly underneath the neurocranium, and an external device sitting on the outside of the head, at most a few millimeter away from the skin. This external device is creating the electromagnetic field to power the implanted device and typically also includes a data receiver to receive the neural data transmitted by the implant. Since the

external device is, to first order, not constrained in size and power, larger and more complex devices can be exploited, reducing the complexity and, therefore, the power consumption of the implanted radio and providing more power to the implant to make mm-size implants feasible.

The channel itself consists of various types of tissue and can be modelled as layers of bone, fat and skin [Mark10b]. Depending on the age of the patient and due to variations in anatomy the different layers can add up to a total of between 2.5 and 11 mm [Drossos00]. In the remainder of this chapter the most pessimistic case of 2 mm skin, 2 mm fat and 7 mm of bone is used unless noted otherwise. Additionally, the separation between the external antenna and the skin is fixed to 5 mm to prevent excessive SAR values in the skin. The frequency dependent dielectric properties of the different types of tissue were modeled based on multiple Cole-Cole dispersions as introduced by Gabriel et al. [Gabriel96b] and fed into a commercial finite element based electromagnetic field solver (Ansoft HFSS^{TM}) to simulate the overall link performance [Mark10a].

Since tissue introduces dielectric losses, antennas with low electric near fields are the preferred choice when it comes to implanted antennas [Poon10]. Loop antennas create relatively small electric near fields while providing good coupling through the magnetic field and are therefore the most common choice for wireless implants. This was also the reason for choosing loop antenna structures as antennas throughout this work.

Due to the link not being a traditional far field link, the channel cannot be investigated separately from the antennas. Therefore, 2-port simulations of the entire link, including the antennas, are carried out to characterize the link adequately. Based on the simulated 2-port S-parameters, the maximum achievable power gain (MAG), assuming simultaneously conjugate matched input and output impedances, was calculated as the main figure of merit of the various wireless links [Mark10a]. The MAG can be calculated from the S-parameters by

$$MAG = K - \sqrt{K^2 - 1} \tag{2.1}$$

where K is the stability factor given by

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |s_{11}s_{22} - s_{12}s_{21}|^2}{2\,|s_{12}s_{21}|} \tag{2.2}$$

2.2 Optimum Size - Frequency Pair For Constrained Implant Size

For the given application, typically only the implanted antenna is constrained in size, and the external (transmit) antenna can be made larger to increase the coupling between the antennas. It is therefore advisable to start with the size constrained implant when optimizing the overall link. The receive antenna should maximize the coupling area by exploiting

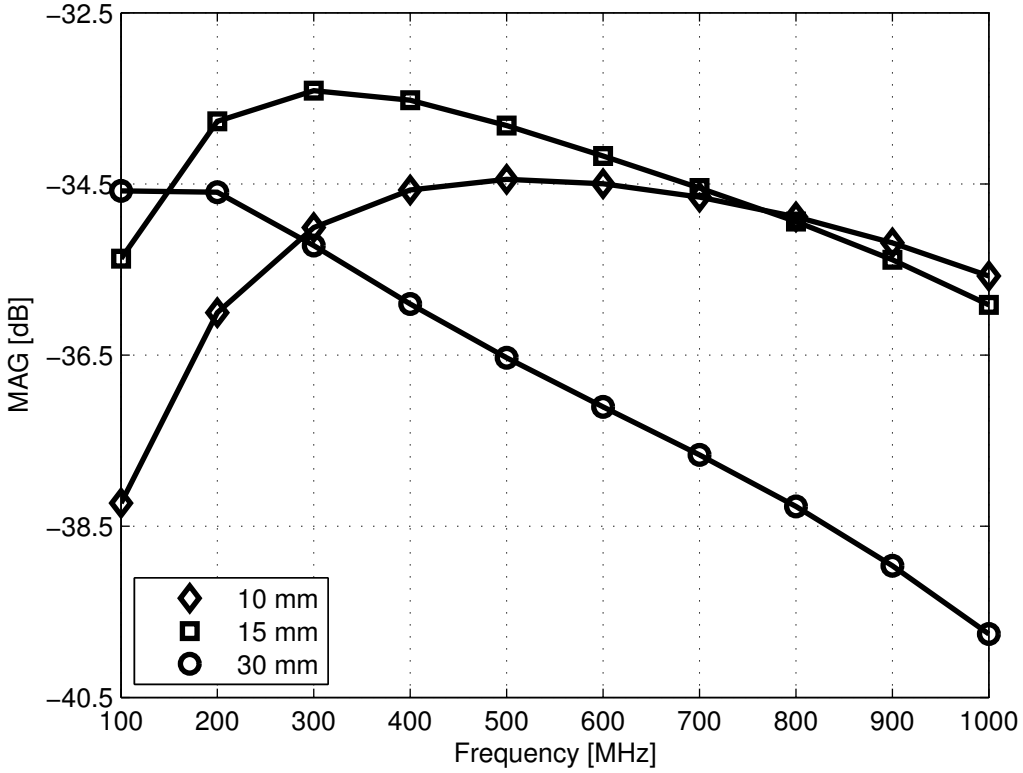


Figure 2.1: Maximum achievable gain for power transfer to a 1 x 1 mm^2 implanted antenna with different external antenna sizes

as much of the available footprint as possible. For the following optimization the implant footprint is constrained to 1 mm by 1 mm. A single square-loop receive antenna of exactly these dimension with a trace width of 50 µm was used to maximize the coupling area [Mark11a]. Poon et al. have reported that the frequency minimizing the link loss shifts down to lower frequencies and the minimum link loss decreases with increasing transmit antenna size [Poon10], but they did not investigate the question of whether there is an optimum external antenna size that minimizes the overall link loss and what the optimum frequency is when using this antenna. Magnetostatics suggests that, for purely inductively linked coils, an optimum diameter of the large coil exists as long as the smaller of the two coils is much smaller than the channel separation [Pichorim04]. Since changing the TX antenna dimension changes the optimum frequency for minimum link loss, the existence of an optimum TX antenna size - frequency combination was hypothesized. In order to investigate whether such a pair really exists, links with hexagonal external coils with varying inner diameters D have been simulated over a frequency range of 100 MHz to 1 GHz. The trace widths of all transmit coils were kept constant at 3 mm to keep the ohmic losses in the transmit coil low.

Fig. 2.1 shows the results for antennas with diameters of 10, 15 and 30 mm. It confirms the

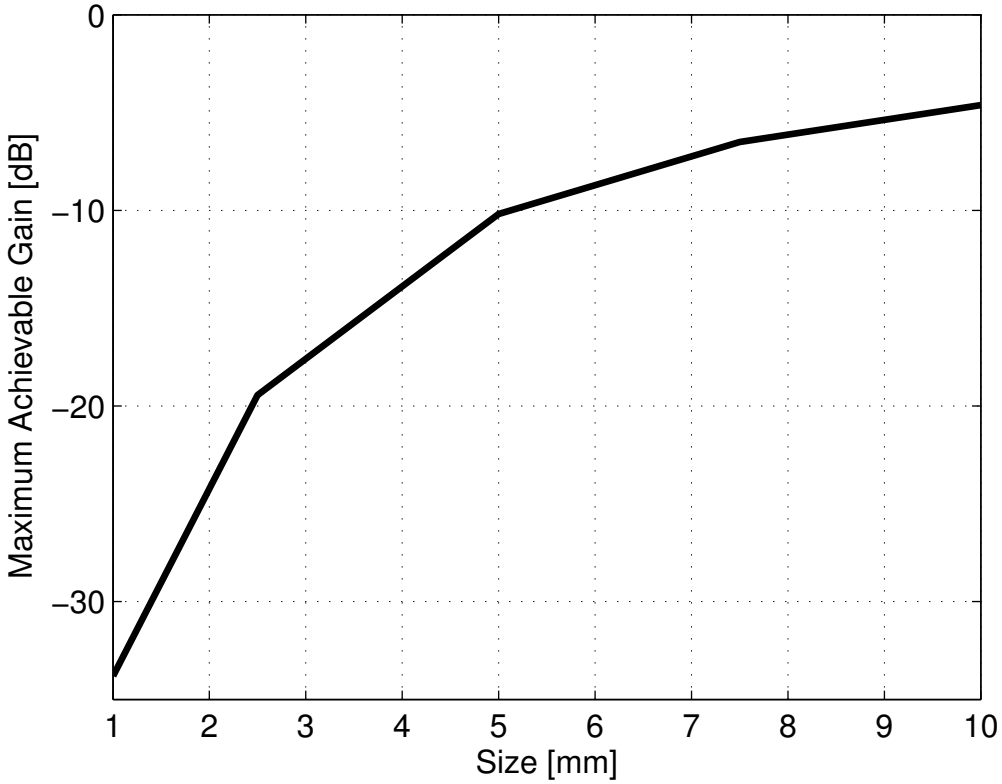


Figure 2.2: Maximum achievable gain for varying implant antenna sizes

existence of an optimum size-frequency pair and shows that, for a 1 mm x 1 mm implant antenna size, the optimum combination is a diameter of around 15 mm and a frequency of approximately 300 MHz. The MAG for this particular configuration has a rather broad optimum and peaks at around -33.5 dB. It is important to note that all these values may vary depending on the actual implementation of the antennas, but there is always one size - frequency pair minimizing the link loss.

For configurations where the separation of the two antennas is on the same order as, or less than, the dimensions of one of the antennas, such as the optimum found above, the smaller antenna is operating in the source region of the larger one [Fuschini10]. This reaffirms the importance of full wave numerical electromagnetic simulations of such links, since none of the common near or far field equations are applicable in this region.

In order to investigate how the optimum values for the link change for different implant sizes, simulations similar to the one leading to fig. 2.1 were carried out. The implanted antenna was modelled as a single square loop antenna with its outer dimensions varying between 1 and 10 mm. Its tracewidth was fixed to be 1/10 of the outer dimension to maintain good coupling while achieving a reasonably high Q factor. A single turn hexagonal loop antenna

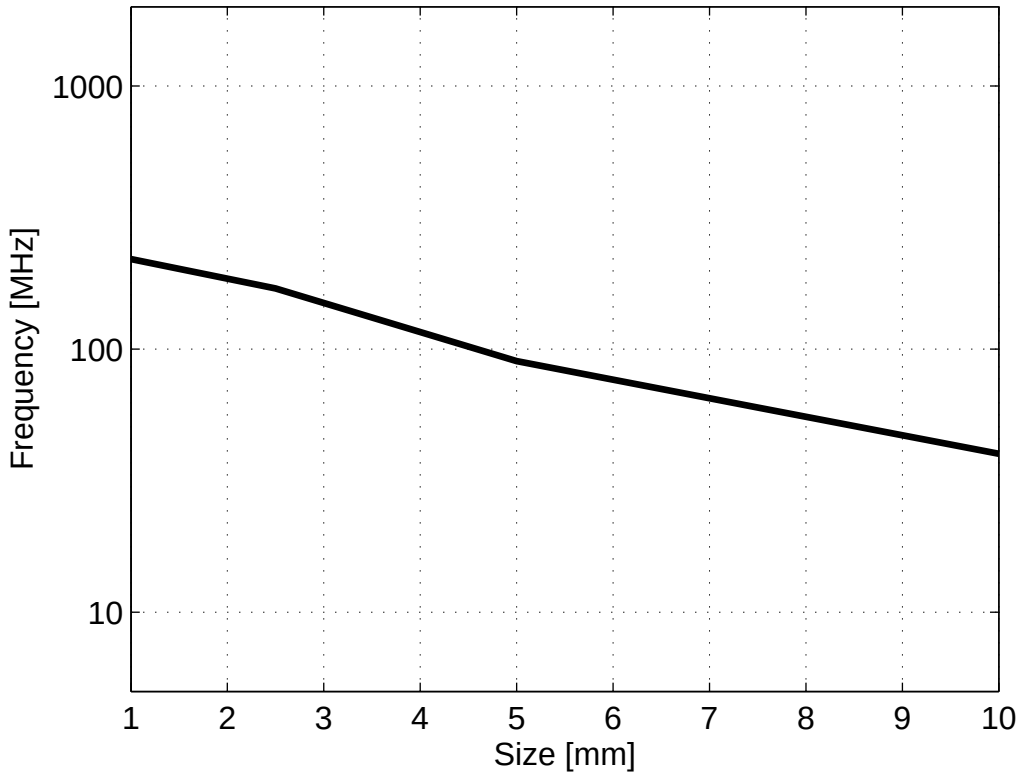


Figure 2.3: Optimum frequency of operation for minimum link loss for varying implant antenna sizes

was again used as external antenna and its dimension was swept to find the optimum size - frequency combination. Both antennas were implemented as 35 µm thick copper traces on standard FR4. Again, the actual values of the results may vary significantly with the actual implementation of the various antennas (especially for the larger size ones, due to the higher flexibility e.g. in terms of number of turns and tracewidth), but the trends described here will still hold [Rabaey11].

Fig. 2.2 shows the maximum coupling achieved between an optimum sized transmit antenna and a receive antenna with a fixed side length (X-axis) at the optimum frequency. It is a strong function of size and degenerates heavily for antennas less then 4 mm by 4 mm. At the same time, the optimum frequency at which the maximum coupling is achieved increases with decreasing size, starting at a few 10s of MHz going all the way up to a few 100s of MHz, as shown in fig. 2.3. When moving to smaller receiver sizes and therefore higher frequencies, the optimum transmit antenna sizes also reduced, although less drastically (from approximately 2.5 cm to 2 cm).

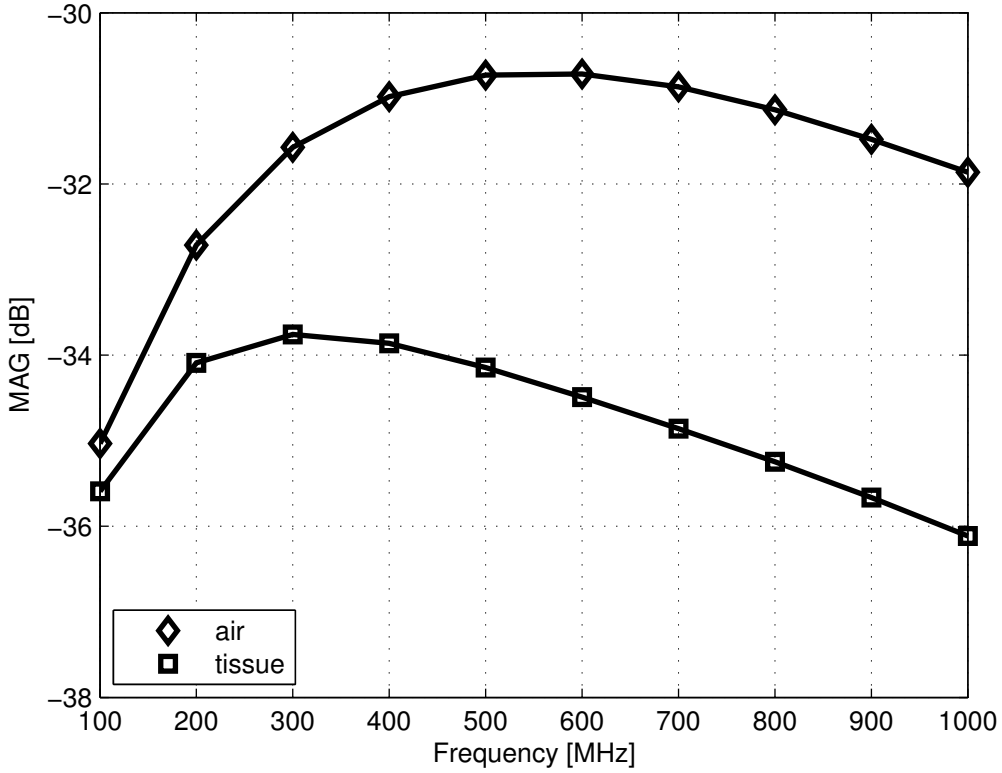


Figure 2.4: Comparison between link in tissue and air

2.3 Effects of Tissue

In order to investigate the effect that tissue has on the link characteristics, the same setup as the one used to generate fig. 2.1 was used. The case with the 15 mm external antenna was simulated with and without tissue, and the results are shown in fig. 2.4. As expected, the link loss when purely operating in air is lower than when operated through tissue across the entire frequency band. At lower frequencies the difference diminishes, while it clearly increases with increasing frequencies. This can be explained by the increased E-field produced by the loop at higher frequencies, leading to higher interaction with the tissue. A shift in the optimum frequency can also be observed. It increases from approximately 300 MHz in tissue to somewhere between 500 and 600 MHz in air.

The observed difference is not primarily caused by the loss in the channel, but more by the effect the channel has on the antennas. Fig. 2.5 and Fig. 2.6 show the comparison between the resistance and reactance of the external and internal antennas, respectively, with air or tissue in between them. While the effect of the tissue on the reactance and hence the inductance of both antennas is almost negligible in the frequency range of interest,

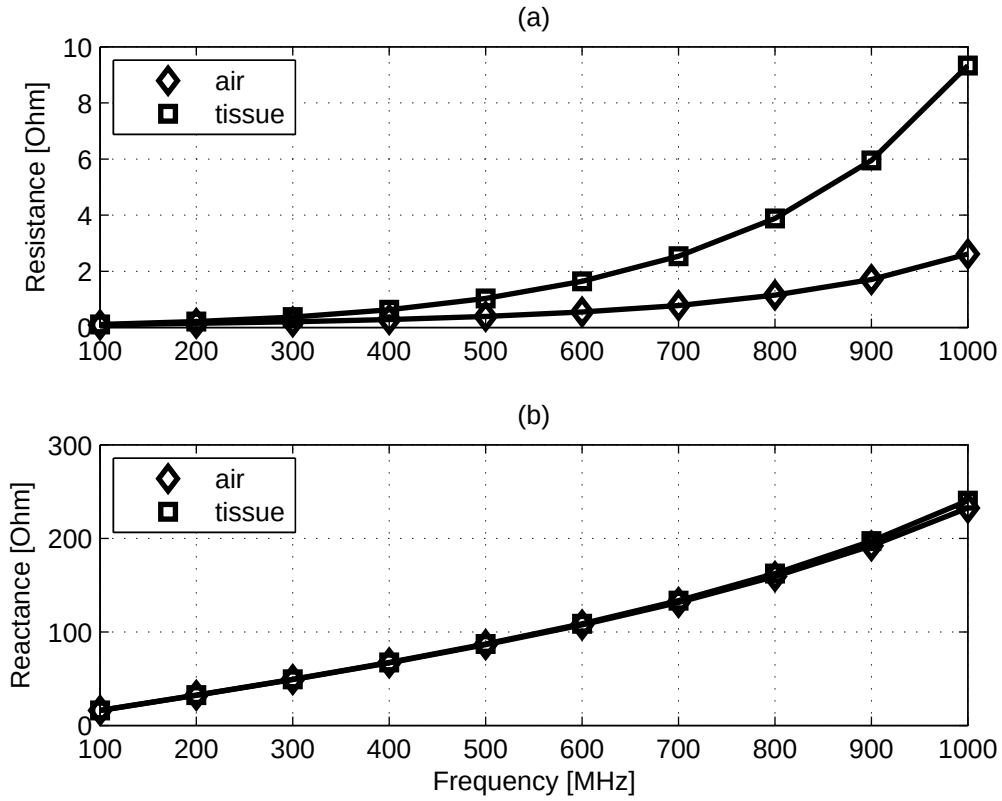


Figure 2.5: Comparison between resistance (a) and reactance (b) of external antenna in tissue and air

the resistive part of the impedance increases significantly, especially for the larger external antenna and at higher frequencies. This can be explained by the effective increase of the electrical size of the loop antennas when placed next to tissue. With relative permittivities between 5 and 80 for the different tissues between 100 MHz and 1 GHz ([Gabriel96a]), the effective wavelength decreases significantly, even for the external antenna placed several millimeters away from the tissue. Electrically, the size of the antennas therefore increases and the antennas produce even larger E-fields leading to an increase in the overall loss due to the enhanced tissue interaction.

2.4 Specific Absorption Rate

The main limiting factor for the power available to the implant is, besides link loss, the limitation on the maximum transmit power imposed by regulations to avoid adverse health effects due to exposure to electric, magnetic and electromagnetic fields. In their standard for safety levels with respect to human exposure to radio frequency (RF) electromagnetic

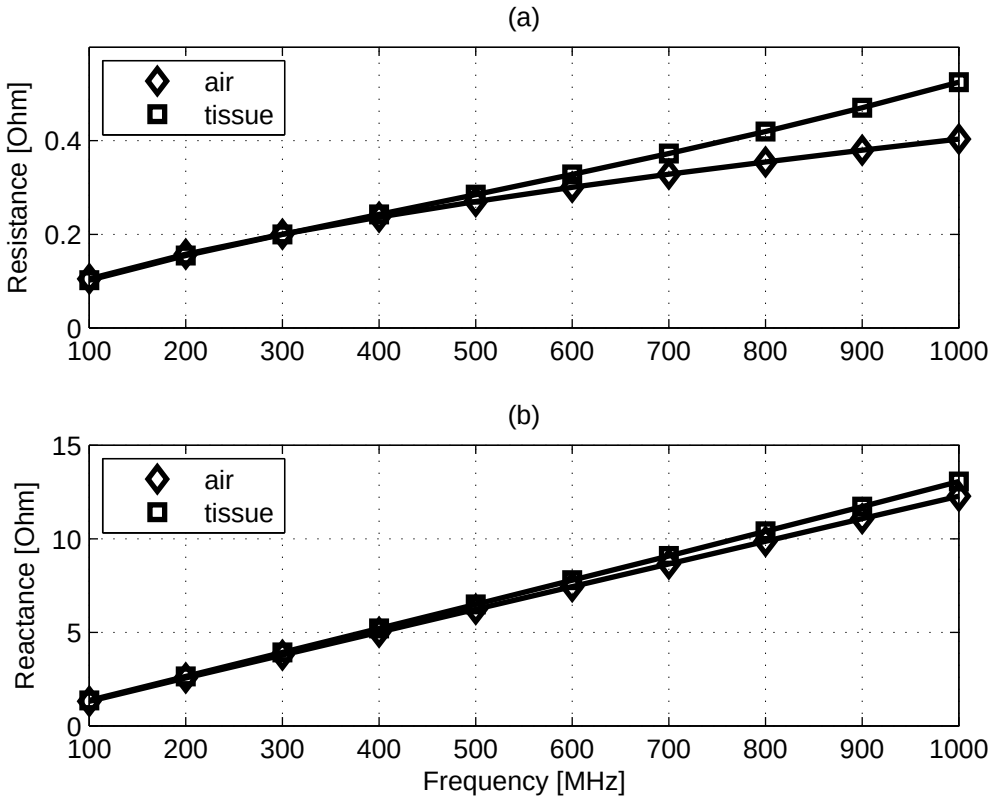


Figure 2.6: Comparison between resistance (a) and reactance (b) of implanted antenna in tissue and air

radiation ([IEEE06]) the IEEE identifies two main classes for established adverse health effects: one class is associated with electrostimulation, the other with tissue heating. The former is caused by fields of frequencies between 3 kHz and 5 MHz, and the latter by frequencies between 100 kHz and 300 GHz. Since the electric field within the biological tissue is causing the electrostimulation, the basic restrictions for the 3 kHz to 5 MHz range are given in terms of *in-situ* electric field. To protect against adverse health effects due to tissue heating, limits in terms of the so called specific absorption rate (SAR) are given for a frequency range from 100 kHz to 300 GHz. In the transition region between 100 kHz and 5 MHz, both restrictions have to be adhered to. Based on the range of optimum frequencies obtained in section 2.2 and shown in fig. 2.3, only the SAR limitations are relevant for the intended applications. If however, a frequency below 5 MHz is used, the E field limitations have to be considered as well.

The SAR is a measure of how much power gets absorbed by a certain amount of tissue and subsequently converted into heat averaged over a certain mass of tissue. Its limit is based on a certain amount of tissue heating (typically 1° C) associated with the electromagnetic radiation it is exposed to, and also governs the maximum transmit power of cellphone handsets. In the U.S., the SAR value for partial body exposure for the general public is limited by the FCC to 1.6 W/kg over 1 gram of tissue [Cleveland99]. The regulations in other parts of the world, like e.g. in Europe, follow the recommendation by the IEEE and limit the maximum SAR to 2 W/kg over 10 gram of tissue, which is less restrictive [CEU99, IEEE06]. The SAR is primarily determined by the E-field and is related to it by

$$SAR = \frac{\sigma \left|E\right|^2}{\rho} \tag{2.3}$$

where σ is conductivity of the tissue, ρ is the mass density of the tissue, and E is the RMS electric field strength in the tissue [IEEE06]. Since the direct determination of the SAR is non-trivial, the IEEE derived limitations on the electric- and magnetic near fields as well as on power density for far field exposure. Due to the fact that the SAR constraint is based on thermal considerations, the derived field and power density levels are time averaged, i. e. the limitations can be temporally exceeded as long as enough time is provided for the tissue to cool down. Typical averaging times are 6 minutes, indicating the slow time constants of the processes involved. On top of the specified averaging time, there is also a limit related to the maximum energy per time slot: During any 100 ms within the averaging interval, the total incident energy density should not exceed one-fifth of the total energy permitted during the averaging time. Another restriction limits the maximum instantaneous levels as well, but it is typically 3 orders of magnitude higher than the time averaged value and hence only rarely a limiting factor when designing wireless power transfer systems. All the values mentioned in this paragraph are taken from the IEEE standard ([IEEE06])

In order to evaluate the maximum power that can be applied to the external antenna without violating the SAR constraints, the built-in SAR function of Ansoft HFSS^{TM} was used to

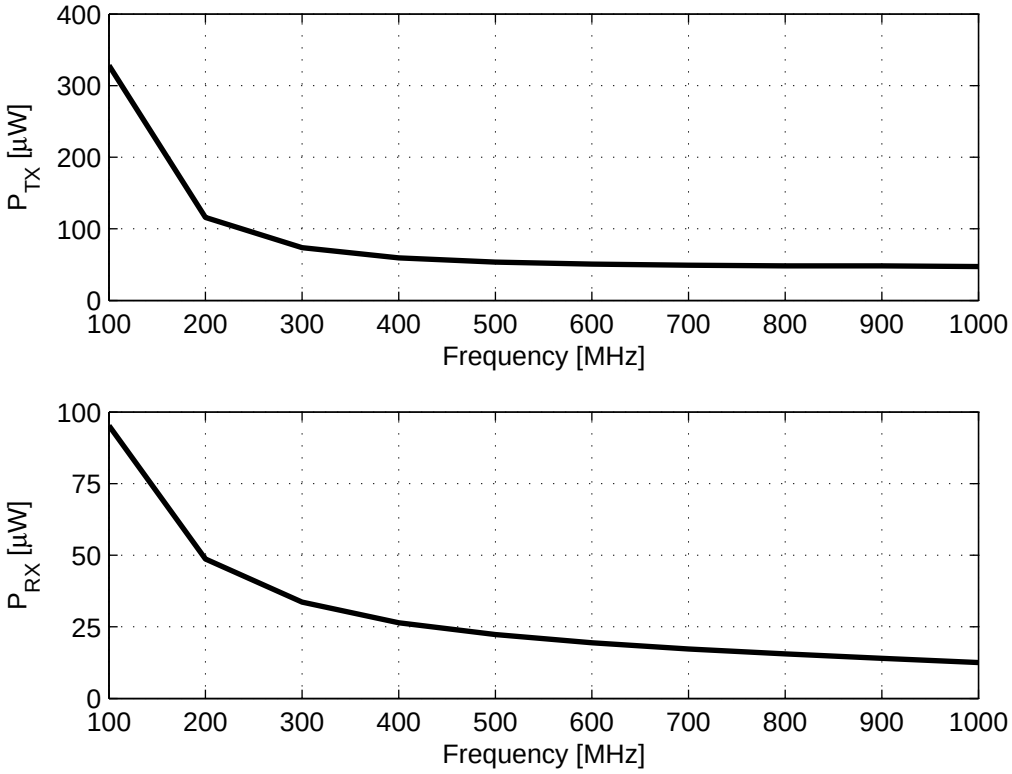


Figure 2.7: Maximum transmit and receive power vs. frequency for an external antenna with a diameter of 15 mm and a 1 mm^2 implant antenna

compute the local SAR values and spatial averaging was performed in Matlab^{TM}. Unless otherwise noted the SAR constraint for the U.S. equal to 1.6 W/kg averaged over 1 gram of tissue was used to derive the maximum allowed transmit power throughout this work.

When it comes to the efficiency of the wireless power transfer, the maximum achievable gain is clearly the most important metric, but very often it is the absolute amount of power available to the implant that matters most. Fig. 2.7 shows the maximum transmit power and the power available at the 1 mm by 1 mm receive antenna for the 15 mm external antenna when transmitting without violating the 1.6 W/kg averaged over 1 g of tissue SAR constraint [Mark11a]. Unlike in the case of the link loss, there is no optimum frequency that maximizes the received power. Purely from a link perspective, this means that the lower the frequency, the higher the received power. The main reason for this is that a fixed size antenna creates lower E-fields at lower frequencies. In general however, the minimum frequency of operation is very often limited by the electronics. For example, resonating out the receive antenna is crucial to increase the input voltage enabling a more efficient AC to DC conversion, however, the antenna inductance and the input capacitance of the implant are limited by the size of the implant and set a lower limit on the frequency of operation.

Additionally, the achievable impedance at resonance and hence the voltage for a fixed power increases with frequency, potentially increasing the AC to DC conversion efficiency, especially when the received power is very low as will be shown in chapter 3. It is therefore crucial to optimize the link and the electronics holistically to maximize the power available to the implant.

On top of that, the maximum achievable gain can be traded-off for available power at a fixed frequency by varying the transmit loop's size. Increasing the external antenna's size spreads out the local SAR more, which reduces the SAR average over a given mass of tissue. Since the spatially averaged SAR is limiting transmit power, reducing it allows to increase the transmit power. The amount by which the transmit power can be increased can, under certain conditions, outweigh the loss in link efficiency and therefore lead to higher receive power levels. A similar trade-off can be made by varying the distance between the transmit antenna and the skin, due to the rapid rate at which the electric field drops off close to the antenna [Mark11a].

2.5 Maximum Available Power

Combining the maximum allowed transmit power and the link loss leads to the power available at the terminals of the implanted antenna. Fig. 2.8 shows this received power (dashed line) for a given receive antenna dimension at the maximum coupling point. It ranges from a few 100 mW for 10 mm by 10 mm to as little as a few 10s of µW for the 1 mm by 1 mm nodes. However, the tissue heating caused by the electromagnetic field produced by the external antenna is not the only health related constraint limiting the received power. The power that gets consumed by the implanted system does heat up the system and as a result the tissue surrounding it. Research has shown that a power density of approximately 500 $\mu W/mm^2$ leads to a 1^{o} C increase in temperature in the surrounding tissue [Kim07]. The solid curve in fig. 2.8 shows the maximum power consumption for implantable integrated circuits of a given size that produces an amount of tissue heating comparable to the one leading to the SAR limitations [Rabaey11]. Comparing this to the achievable power levels received using electromagnetic coupling, shown in the same figure, reveals that the maximum power consumption of implanted electronics larger than approx. 4 mm by 4 mm is not limited by the power transfer, but rather by the heating the integrated circuit causes itself.

As mentioned in section 2.4, several things can be done to trade-off maximum received power for coupling efficiency in the power transfer limited regime. Depending on the exact system requirements one might be able to tolerate a slight loss in efficiency if, at the same time, the received power increases. Since the maximum transmit power is a function of the frequency, the transmit antenna geometry, and the distance of the transmit antenna from the human body, these design variables can be adjusted to increase the received power at the cost of reduced coupling. The fact that coupling with respect to both, the optimum frequency as well as the optimum transmit antenna size, exhibits rather broad optima provides room for

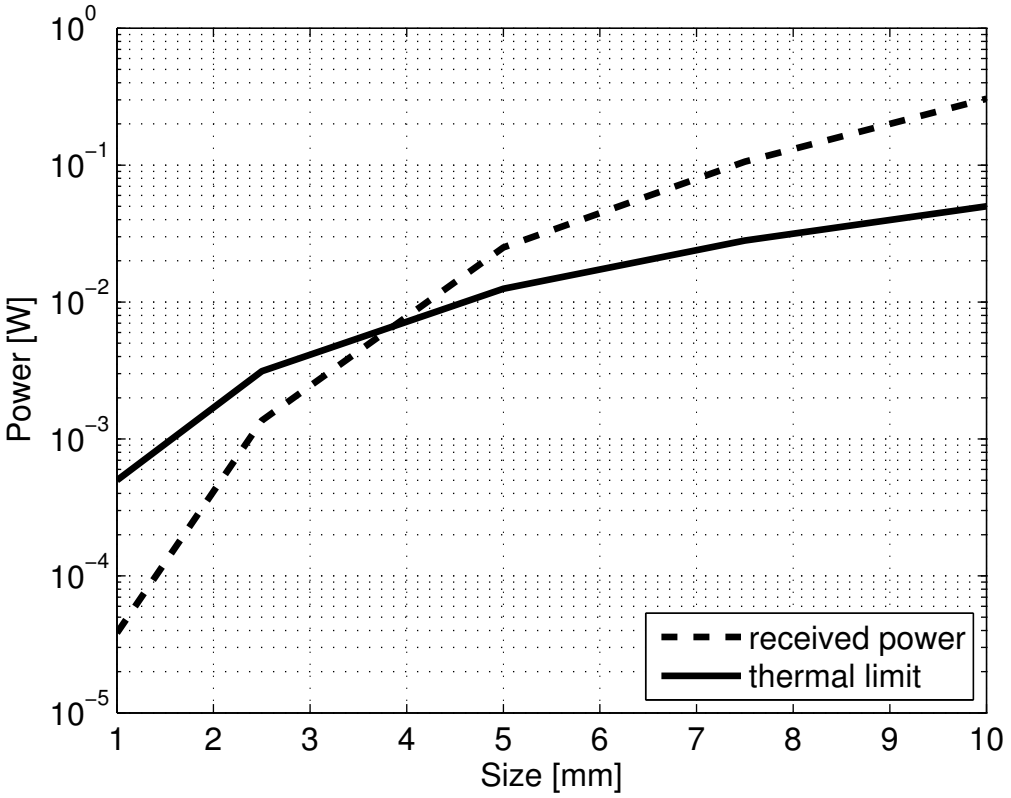


Figure 2.8: Maximum available power at implant antenna terminal for varying implant antenna sizes

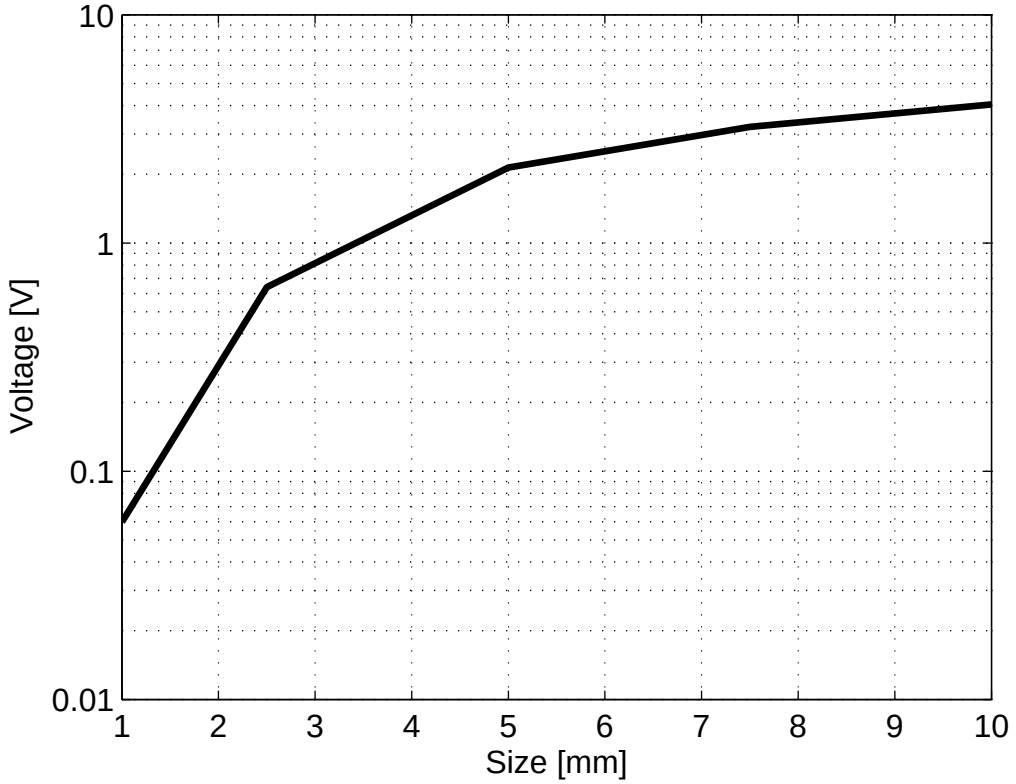


Figure 2.9: Peak input voltage across matched implant antenna terminal for varying implant antenna sizes

such trade-offs. The values plotted in fig. 2.8 are therefore by no means hard limits; they just serve as indicators for the principal trend [Mark11a].

It is important to note that the received signals are AC signals, but the electronics typically requires DC voltages for the supply. Chapter 3 deals with the electronics needed to convert the incoming AC signals to DC signals. Depending on the input voltage levels, different topologies of AC-to-DC converters might be needed, and the efficiency of the conversion process can vary significantly. It is therefore important to get a feeling for what voltage levels can be expected at the input of the converter. Assuming matched conditions between the antenna and the circuit, the input voltage depends on the received power and the input impedance of the antenna. In general the antenna impedance increases with size, and can be very low for mm-size antennas. Fig. 2.9 shows the expected peak input voltage levels based on the single turn implant antennas of varying size and the received power based on the lower of the two limits shown in fig. 2.8. The voltages range from below 100 mV to approximately 3 Volts. Together with the frequency of operation and the input power level, the input voltage is an important parameter when deciding on the AC-to-DC converter architecture, as will be described in the next chapter.

2.6 Summary

Due to the proximity of the antennas and the complexity of the channel, numerical methods are needed to investigate and optimize cm-range wireless links for implants. The maximum achievable gain has been defined as an important metric allowing the comparison of various links. Loop antennas have been identified as good candidates for antennas when operating within, or at least in proximity of, tissue. Assuming size constrained implants, the frequency of operation and the geometry of the external loop are the two main degrees of freedom. Depending on the exact size of the implant, a distinct external antenna size and frequency of operation pair exists that minimizes the link loss. For single loop structures, the optimum frequency increases from 10s of MHz to 100s of MHz when the implant size decreases from 10 mm by 10 mm to 1 mm by 1 mm, while the optimum external antenna diameter decreases from 2.5 to 2 cm. The coupling decreases at a rate that increases with decreasing implant size, dropping to efficiencies below -30 dB for 1 mm by 1 mm implanted antennas.

Tissue decreases the coupling over the entire frequency range, with a more pronounced effect at higher frequencies. It also shifts the optimum frequency to lower frequencies. This is mainly due to the increased tissue interaction with the antennas at higher frequencies.

In the frequency range of interest, adverse health effects based on tissue heating limit the maximum transmit power as well as the maximum power an implant can consume. Wireless power transfer is limiting the power available to the implant for sizes smaller than approximately 4 by 4 mm^2, while tissue heating caused by the power dissipated in the implant, limits the available power for larger implants. Taking the more restrictive limit at a given size into account, the power available ranges from a few 10s of μW for the 1 mm^2 implant to a few 10s of mW for the 10 by 10 mm^2 implant. Combining these levels with the resonant implant antenna impedances leads to peak voltages of less than 0.1 V to more than 3 V, depending on the antenna size. Both, the received power as well as the input voltage are important parameters impacting the choice of the AC-to-DC conversion circuit and architecture as will be shown in the next chapter.

Chapter 3

AC-to-DC Conversion

In order to be able to supply a circuit with the energy available at the antenna terminals, the incoming AC signal needs to be converted to a stable DC voltage. This is typically done by a rectifier (AC-to-DC converter) followed by a regulator to reduce the output ripple of the rectifier and to account for voltage fluctuations due to the the wireless power transfer itself. As shown in chapter 2, the incoming signal can vary by orders of magnitude in amplitude and frequency, imposing different sets of challenges on the AC-to-DC conversion circuit depending on the exact size of the implanted antenna. The AC-to-DC converter is therefore one of the most crucial circuit blocks in a power supply system receiving its power from an AC source. Owing to this, this chapter is devoted to the aspects of AC-to-DC conversion of energy retrieved from AC electro- and/or magnetic fields.

The first part of this chapter provides an overview of state-of-the-art converters and discusses system level considerations, such as choice of frequency and received input voltage amplitudes, impacting the choice of the optimum converter topology. Further, a generic model of AC-to-DC converters is introduced, enabling the abstraction of key characteristics of converters from the circuit level details, simplifying the overall system design. Based on this model, the implications on the circuits interface with the antenna are discussed. Finally, circuit implementation details of two different architectures capable of spanning the entire set of expected input amplitudes and frequencies are presented and the expected performance for various implant sizes is discussed.

3.1 Architectural Considerations

The ultimate task of a rectifier is to convert the input AC signal to a DC voltage of a certain minimum level as efficiently as possible. Factors impacting the choice of architecture and performance are the input power and voltage level, the input frequency and the desired output voltage level. In the BMI space DC voltages on the order of at least 0.5 V are needed to be able to power useful electronics [Muller11]. This means that, depending on the input

P_{IN}	V_{IN} [V_{PK}]	V_{OUT} [V_{DC}]	Frequency	Efficiency	Features	Reference
50.3 mW	2.4	2.08	1.5 MHz	$>$ 85 %	active rectifier	[Guo09]
24.3 mW*	3.8	3.12	13.56 MHz	80.2 %	active rectifier w/ offset controlled comparator	[Lee11]
720 μW	1.2	1.13	1.5 MHz	90 %	active rectifier	[Guo09]
430 μW	2	1.75	125 kHz	85 %*	active rectifier	[Peters08]
30 μW*	2.5*	1.5	350 Hz*	$>$80 %	active rectifier	[Le06]
2.77 μW	0.6	0.5	350 Hz*	88.4 %	active rectifier w/ voltage doubler	[Le06]

* estimated/calculated based on published data

Table 3.1: Comparison between different published AC-to-DC converters with V_{IN} larger than V_{OUT}

voltage and hence the size of the implanted antenna, circuits not only being able to rectify but also to provide DC voltages higher than the input amplitudes might be needed.

Tables 3.1 and 3.2 list representative AC-to-DC converters published over the last couple of years, spanning the expected input power and voltage levels (fig. 2.8 and fig. 2.9) for mm-size receive antennas. Depending on the ratio between the input and output voltage, AC-to-DC converters can be split up in two groups. Work published with the input voltage V_{IN} being larger than the output voltage V_{OUT} is summarized in table 3.1, while table 3.2 summarizes the performance of published systems with the output voltage being larger than the input voltage.

Comparing these two groups, it becomes apparent that the reported efficiencies for rectifiers with V_{IN} larger than V_{OUT} are significantly higher. The predominant underlying principle for achieving these rather high efficiencies between 80 and 90% is the implementation of active rectifiers where a comparator controls a transistor to form a diode with zero forward turn-on voltage and a low on-resistance. Efficiencies above 80% have been reported for input power levels from a few μW up to a few 10s of mW. Since the power needed to switch the transistors and supply the comparators increases with frequency and reduces the overall efficiency of the converter, active rectifiers are typically used at low to medium frequencies up to around 10 MHz.

Looking at converters that provide an output voltage that is higher than the input voltage reveals a more diverse set of approaches to perform rectification while increasing the voltage at the same time. However, most of the converters are either based on some variation of a voltage multiplier first proposed by Greinacher [Greinacher21], sometimes also referred to as Cockcroft-Walton multiplier, or on the self-driven synchronous principle ([Ikeda82]). While their performances are comparable, high performance Greinacher-based converters rely on some sort of threshold voltage cancellation utilizing large passives ([Nakamoto07]) or one-

P_{IN}	V_{IN} [V_{PK}]	V_{OUT} [V_{DC}]	Frequency	Efficiency	Features	Reference
450 μW	0.95	< 3	953 MHz	> 40 %	internal V_{TH} cancellation, ferroelectric C, large R, Greinacher	[Nakamoto07]
225 μW	1.2*	2.6	953 MHz	65 %	self-driven synchronous	[Kotani09]
200 μW	0.75	1.5	915 MHz	65 %	self-driven synchronous	[O'Driscoll09]
160 μW	0.71*	6	900 MHz	60 %	floating gate with one time charge injection, Greinacher	[Le08]
225 μW	1.2*	2.6	953 MHz	65 %	self-driven synchronous	[Kotani09]
28 μW	0.69	1.5	868 MHz	28 %	shottky diodes, Greinacher	[Karthaus03]
11 μW	0.09	1	450 MHz	9 %	low V_{TH} devices, Greinacher	[Kocer06]
8.5 μW	0.36	0.5	950 MHz	23.5 %	self-driven synchronous	[Mandal07]
7.5 μW	0.36	1.5	868 MHz	10 %	shottky diodes, Greinacher	[Karthaus03]
6 μW	0.29	0.4	950 MHz	16.7 %	self-driven synchronous	[Mandal07]
5.5 μW	0.13*	1	900 MHz	10 %	floating gate with one time charge injection, Greinacher	[Le08]
2.7 μW	0.074	0.882	2.4 GHz	37 %	SOI, low V_{TH}, Greinacher	[Curty05a]

* estimated/calculated based on published data

Table 3.2: Comparison between different published AC-to-DC converters with V_{IN} smaller than V_{OUT}

time programming floating gates ([Le08]), or high performance process options such as shottky diodes ([Karthaus03]), low V_{TH} devices ([Kocer06]) or silicon-on-insulator (SOI) CMOS technology ([Curty05a]). Self-driven synchronous based rectifier are reported to achieve at least comparable performance to all but the SOI based converter reported by Curty et al. ([Curty05a]), while implemented in standard CMOS without the additional need for large passives or one-time programming. They are therefore becoming increasingly popular over the last couple of years.

Voltage multiplying rectifiers are typically used at frequencies above 100s of MHz, primarily because of the lower input voltage levels at which ultra-high frequency (UHF) radio frequency identification (RFID) tags are expected to operate. In theory they are expected to achieve at least the same performance at lower frequencies. However, the size of the capacitors needed for the voltage multiplication is to some degree inversely proportional to the frequency, and the circuits would become prohibitively large at low frequencies.

Table 3.2 also indicates another aspect of voltage-multiplying rectifiers: their low efficiencies at low input voltage levels. This can be mainly attributed to the low on-to-off current ratio of the devices involved in the rectification when driven by small voltages. Being able to operate at higher input voltages can therefore increase the efficiency compared to systems with the same input power but lower voltage amplitudes. Higher antenna impedances are one way to obtain higher voltage amplitudes for a fixed input power.

It is also important to note that active rectifiers are not necessarily limited to systems where V_{OUT} is smaller than V_{IN}. However, since the number of comparators and transistors actively being switched increases with the voltage multiplication factor, the auxiliary power consumption increases significantly with each stage of voltage multiplication. Together with the higher frequencies systems with lower input voltages typically operate at, this will most likely cause their efficiencies to drop below what can be achieved by self-driven synchronous rectifiers.

Based on these observations and the expected input voltages and frequencies derived in chapter 2, active rectifiers are identified to be the best candidates for larger implant sizes, whereas self-driven synchronous converters are well suited for smaller size implant antennas. The remainder of this chapter will therefore focus on these two architectures.

3.2 Modelling AC-to-DC Converters

Rectifiers are inherently non-linear, essentially allowing current to flow in one direction but preventing it from flowing into the other. Analyzing the transient start-up behavior of such systems is challenging. However, Curty et al. proposed a modelling approach to model the steady-state behavior of rectifiers [Curty05b]. Since the AC-to-DC converter is operating in steady-state most of the time, such a model is a powerful tool to design systems around rectifiers. This section is based on the model by Curty et al. and extracts its features common to all rectifier circuits.

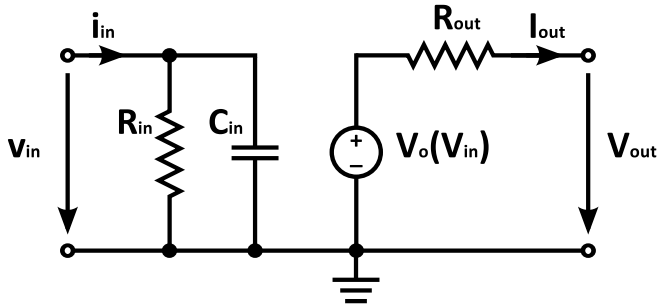


Figure 3.1: Equivalent circuit of a generic rectifier

Fig. 3.1 shows the equivalent circuit of a generic rectifier [Curty05b]. Any rectifier can be modelled as a 2-port with an input impedance, a voltage controlled voltage source at the output, and an output resistance. The input impedance consists of a resistance R_{in} in parallel with C_{in}. Both are only constant for a constant input voltage amplitude V_{in} and output current I_{out}, i.e. they do depend on these two parameters. The same is true for the output resistance R_{out}. V_O on the other hand depends only on the input voltage amplitude V_{in}. In the following paragraphs descriptions of each of the parameters are given. Mathematical expressions are given where applicable, all under the assumption that the circuit operates in steady-state and the output current is constant.

Input Resistance R_{in} The input resistance of a rectifier can be modelled based on the input voltage and the current flowing into the circuit. Although the input current of a rectifier is typically pulsed in nature and the input impedance is therefore not constant in time, it can be modelled as a time constant resistance based on the equivalent mean power that enters the rectifier during one signal period T [Curty05b]. This mean input power can be calculated by

$$\overline{P_{in}} = \frac{1}{T}\int_0^T v_{in}(t)i_{in}(t)dt \tag{3.1}$$

and easily obtained from simulations. Once the input power is known the equivalent constant input resistance can be derived from

$$R_{in} = \frac{V_{in}^2}{2\overline{P_{in}}}. \tag{3.2}$$

Input Capacitance C_{in} Unlike R_{in} which is significantly determined by the power delivered to the load, the input capacitance C_{in} is a parasitic component of the rectifier. Especially at high frequencies, it can reduce the input voltage amplitude and hence the output voltage and overall conversion efficiency. It consists of the capacitances associated with the devices

performing the rectification such as diodes or transistors, the effect the drawn current has on the input waveform, and parasitic capacitances associated with packaging and on-chip wiring. Under certain conditions it can be resonated out by an explicit matching network or absorbed in the antenna design, but its low quality factor Q can still impact the performance significantly. Keeping C_{in} low, especially when converting high frequency signals is therefore crucial.

Its value is best obtained by large-signal simulations, since the parasitic capacitances can significantly change with the operating point of the circuit. The method used throughout this work is based on driving the circuit through a resonant network resembling the antenna. Extra capacitance is added to the circuit to lead to the maximum input voltage (which should be equal to the expected voltage under real operation). C_{in} can then be calculated based on the equation for the resonant frequency of an LC tank (equ. 3.7).

Voltage V_o The voltage V_o is a linear function of the amplitude V_{in} of the input voltage and heavily depends on the architecture of the rectifier as well as on the number of stages in the case of voltage multiplying architectures. It is equal to the output voltage V_{out} for $I_{out} = 0$ and can be expressed by

$$V_o = K \times N \times V_{in} \tag{3.3}$$

where K is a factor specific to the chosen architecture and N represents the number of stages in multi-stage, voltage multiplying converters.

For example, K is equal to 1 for simple half-wave single diode or full-wave bridge rectifiers, 2 for a half-wave Greinacher rectifier, or 4 for a full-wave Greinacher rectifier such as the one used by Curty et al. [Curty05b].

Output Impedance R_{out} R_{out} depends on the input voltage V_{in} as well as on the output current I_{out}, and accounts for the dependency of the output voltage on the output current for a fixed input voltage. It can be determined from simple measurements or simulations of the output voltage for different output currents, by applying equ. 3.4.

$$R_{out} = \frac{V_o - V_{out}}{I_{out}} \tag{3.4}$$

Conversion Efficiency η Although the conversion efficiency is not an explicit part of the equivalent circuit of a generic rectifier as shown in fig. 3.1, it is still one of the most important metrics of an AC-to-DC converter. It is a measure for how much of the input AC power gets converted to useful DC power at the output of the rectifier. Mathematically it is simply given by

$$\eta = \frac{P_{out}}{\overline{P_{in}}} = \frac{V_{out} \times I_{out}}{\frac{1}{T}\int_0^T v_{in}(t) i_{in}(t) dt} \tag{3.5}$$

Plugging equ. 3.5 into equ. 3.2 allows the calculation of R_{in} based on the DC output power and the efficiency as shown below.

$$R_{in} = \frac{V_{in}^2}{2 \times \eta \times P_{out}}. \tag{3.6}$$

The combination of all the metrics described above sufficiently characterizes any rectifier circuit and can therefore be used to optimize overall systems without dealing with implementation details.

3.3 Interfacing with Loop Antennas

Since the AC-to-DC converter directly connects to the antenna, optimizing the interface between these two components has a significant effect on the overall system performance.

A loop antenna below its self-resonance frequency can be modelled by a voltage source in series with a inductor and a resistor. In order to make sure that the maximum amount of energy received by the antenna gets absorbed by the circuit, the input impedance of the circuit has to be conjugately matched to the antenna impedance.

Assuming that C_{in} of the rectifier is small enough, this can easily be achieved by adding extra capacitance C_{add} in parallel to the input of the circuit such that it resonates with the antenna's inductance at the frequency of operation by fulfilling

$$C_{add} + C_{in} = (2 \times \pi \times f)^2 \times L \tag{3.7}$$

and making R_{in} in parallel with the parasitic resistance associated with the input capacitors (R_C) equal to the equivalent antenna resistance at resonance (R_p) given by

$$R_P = R_S \times \left(\left(\frac{2 \times \pi \times f \times L}{R_s} \right)^2 + 1 \right) \tag{3.8}$$

Fig. 3.2 shows the equivalent circuit of this configuration.

In cases where the coupling between the two antennas cannot be considered weak (as can be the case for large receive antennas) the external antenna and the components connected to it have an impact on the impedance seen by the AC-to-DC converter, and its input impedance therefore has to be matched to the antenna impedance modified by the contribution of the

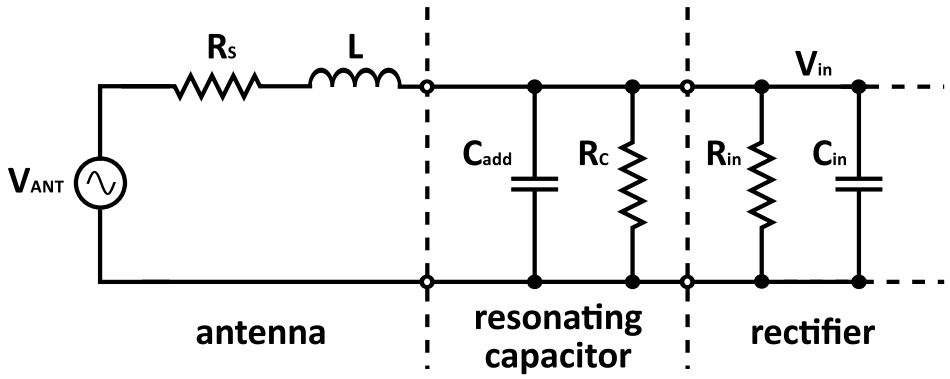


Figure 3.2: Equivalent circuit for antenna - rectifier interface

primary side. At the same time, the matching network on the primary side needs to take into account the effect the implant has on the impedance seen by the primary side. In other words, the 2-port consisting of the two coupled antennas needs to be simultaneously conjugately matched.

Since any power consumed by R_C is wasted, high Q capacitors are essential to keep the losses introduced by the capacitors low. Nevertheless, when using on-chip capacitors the maximum achievable Q is on the order of 100 to 200, which can lead to a loss due to R_C of 10% or more.

For the circuit configuration shown in fig. 3.2, the amplitude of the antenna voltage V_{ANT} can be derived based on the expected power available to the circuit assuming the antenna is resonated with an ideal capacitor as shown in fig. 2.8. V_{ANT} is therefore given by

$$V_{ANT} = 2 \times \sqrt{2 \times P_{avail} \times R_S}. \tag{3.9}$$

Under matched conditions V_{in} can be calculated by

$$V_{in} = \sqrt{2 \times P_{avail} \times R_P}. \tag{3.10}$$

Due to the dependency of the rectifier efficiency on the input voltage V_{in} highlighted in section 3.1, it is advisable to operate at as high impedance levels of R_P as possible to maximize the input voltage [Curty05b]. While more sophisticated matching networks can be used to increase V_{in}, they are not really an option for implants on the lower end of the mm-size range. In order to keep the network losses low, high Q, off-chip components would be required. However, they are unlikely to fit in the constrained area. In case there is extra area available it is better used to increase the antenna sizes, leading to increased coupling, higher antenna impedance and hence higher available power and voltages. Matching the antenna impedance by resonating it with a high Q on-chip capacitor and co-designing the input resistance of the rectifier is therefore the best option for very small implants.

Depending on the intended frequency of operation and the antenna inductance, implementing C_{add} with high Q on-chip metal capacitors might become prohibitively large. In this case, if off-chip components are not an option, lower Q on-chip capacitors with higher capacitance density might have to be considered. Alternatively, a higher frequency of operation might be chosen, trading off available power for a more efficient conversion.

Under certain conditions it might also make sense to, instead of making R_{in} equal to R_P, making it slightly larger. This would reduce the power being absorbed by the circuit, but it also increases V_{in}. Depending on the rectifier characteristics, this might be another way of trading input power for rectification efficiency leading to a net increase in DC power at the output of the rectifier.

The optimum input resistance should thus be designed to be equal to or slightly larger than R_P to maximize the available DC output power. However, since R_{in} depends on the drawn output power, which might not always be constant, the question is under which condition should R_{in} be matched to the antenna. It turns out that the rectifier should be designed such that the input resistance assumes its optimal value under full load condition, because this is when most of the power is needed at the output. When the load demand is lower, the input resistance increases, leading to a reduced amount of power absorbed by the rectifier. This can be tolerated however, since less power is needed at the output. Since the input voltage and hence the output voltage is increasing at the same time, a sufficiently high supply voltage is still guaranteed.

3.4 Circuit Implementations

In section 3.1 active CMOS rectifiers and self-driven synchronous rectifiers were identified as prime candidates for AC-to-DC conversion for large voltage, low frequency and small voltages, high frequency input signals, respectively. This section analyzes both approaches in detail and outlines design procedures for each. Design examples in a 65 nm CMOS process are also given targeting specifications derived in chapter 2.

3.4.1 Active CMOS Rectifier

In CMOS active rectifier circuits, diodes typically used in any rectifier architecture are replaced by a MOS-transistor controlled by a comparator forming an active diode with turn-on voltages much smaller than typical diode turn-on voltages or the threshold voltage of the transistor. The comparator compares the voltages at the anode and cathode of the active diode and turns the transistor on when the voltage at the anode is larger than the one on the cathode and off otherwise. Using this principle, any type of diode based rectifier can be implemented.

A potential problem with such active diode structures is that there is no clear distinction between the source and the drain terminal of the transistor, since the voltage between the

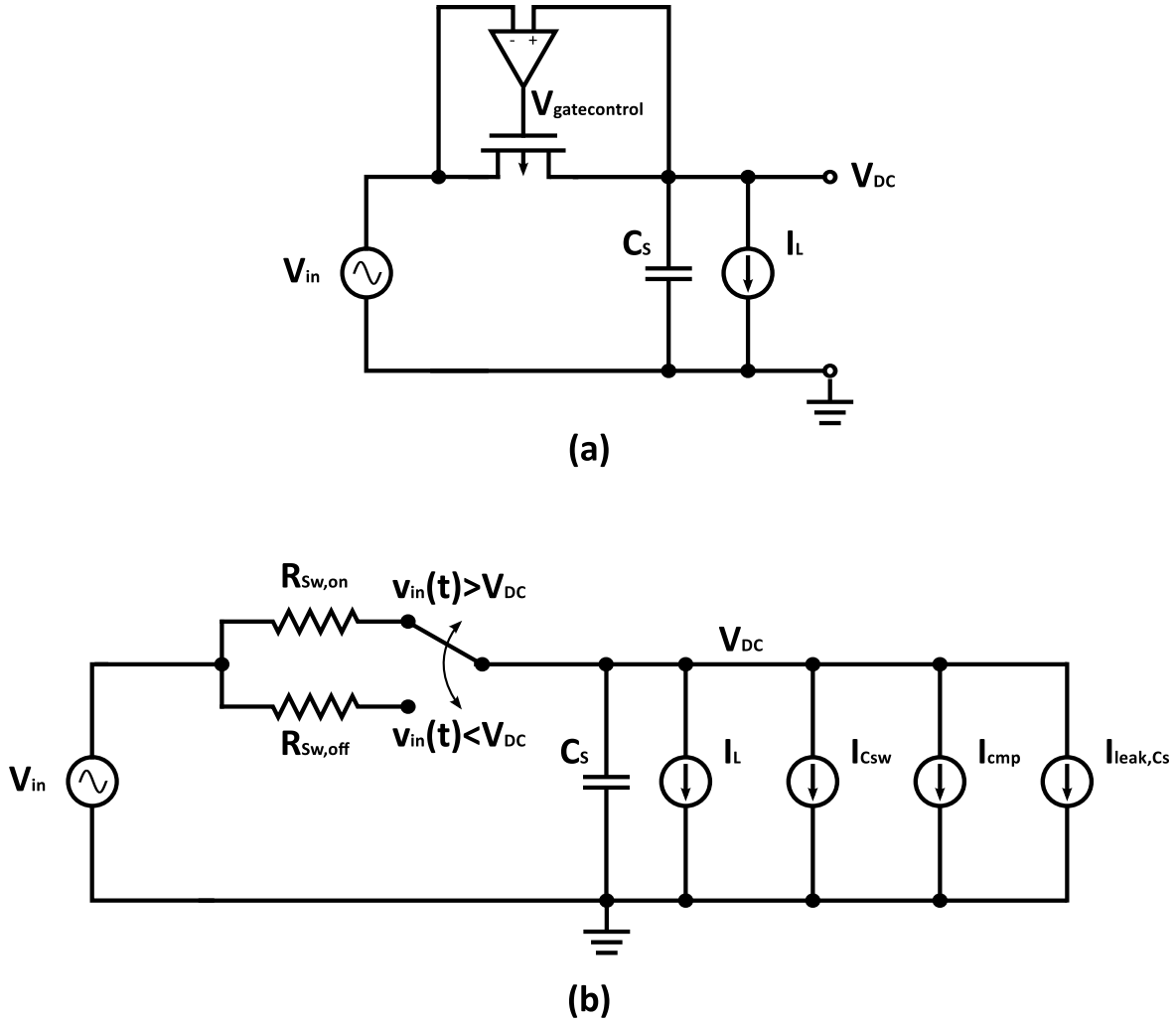


Figure 3.3: A half-wave active CMOS rectifier supplying a constant current (a) and its equivalent circuit to determine V_{DC}

terminals changes its polarity during one signal period. The bulk of the transistor can therefore not be simply hardwired to any of the terminals while guaranteeing that it is the most positive or negative voltage the transistor is seeing. This can lead to potential latch-up and increased substrate leakage. However, dynamically switching the transistor's well to either one of the terminals can be achieved by adding two auxiliary transistors, alleviating this problem substantially [Ghovanloo04].

3.4.1.1 Half-Wave Rectifier

Fig. 3.3(a) shows the implementation of a single diode, half wave rectifier providing a constant load current I_L. In order to analyze the performance of this circuit and optimize

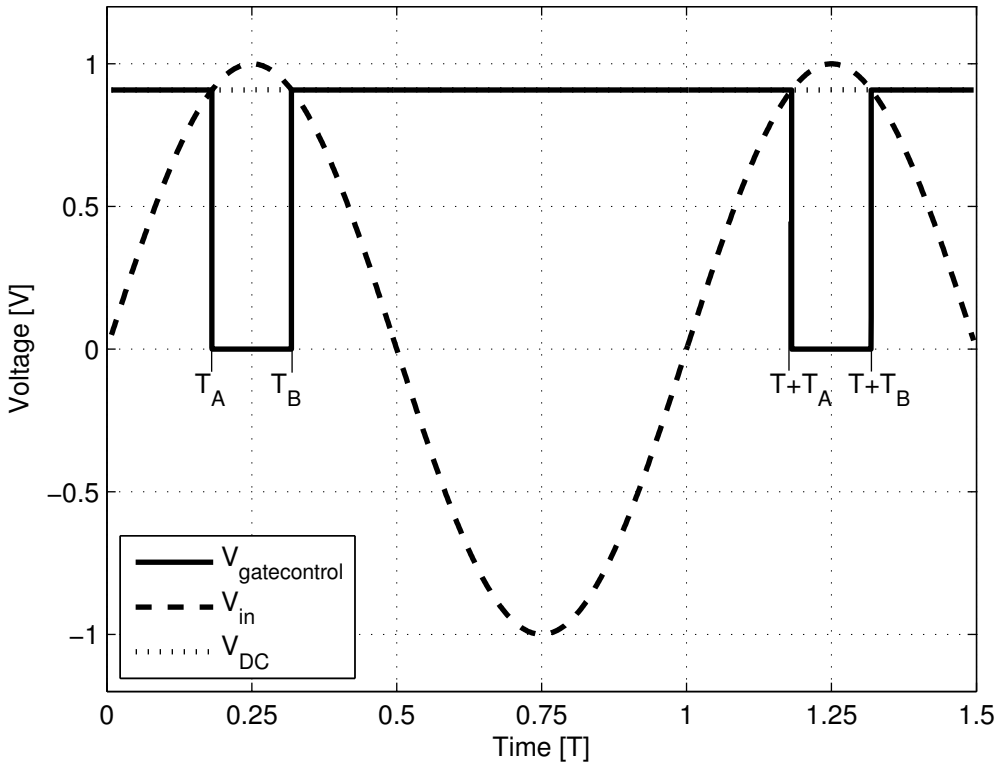


Figure 3.4: Voltage waveforms of idealized active-half wave rectifier over one period

the design, it can be represented by an equivalent circuit as shown in fig. 3.3(b). The operation principle is as follows: Whenever $v_{in}(t)$ is larger than V_{DC} the transistor turns on and can be represented by an equivalent resistor $R_{Sw,on}$, when it is off it is represented by $R_{Sw,off}$. Ideally, $R_{Sw,on}$ is zero and $R_{Sw,off}$ is infinite. C_S is a storage cap that minimizes the ripple during the time the switch is off. The additional current sources represent the losses associated with switching the transistor every cycle (I_{Csw}), the power consumption of the comparator circuit (I_{cmp}) as well as the leakage associated with C_S ($I_{leak,Cs}$).

If C_S is large enough, V_{DC} can be considered constant and the waveforms look like the ones shown in fig. 3.4. This is the case if $C_S \gg T \times {}^{I_L}/_{V_{DC}}$. For example, if it is 100 times larger, the ripple is less than 1% of the input amplitude V_{in}. Simulations show that making C_S big enough to make V_{DC} almost constant maximizes the efficiency of an active rectifier.

Additionally, ideal switching exactly at the time when $v_{in}(t)$ crosses V_{DC} is assumed in fig. 3.4.

In steady-state the charge flowing into the capacitor C_S per period has to be equal to the charge flowing out of it:

$$\int_0^T i_{in}(t)dt = T \times (I_L + I_{C_{Sw}} + I_{cmp} + I_{leak,C_S}) \tag{3.11}$$

Using the parameters from fig. 3.3(b) leads to

$$\begin{aligned} &\frac{1}{R_{Sw,on}} \int_{T_A}^{T_B} [V_{in} \sin(\omega t) - V_{DC}]\, dt \\ &+ \frac{1}{R_{Sw,off}} \int_0^{T_A} [V_{in} \sin(\omega t) - V_{DC}]\, dt \\ &+ \frac{1}{R_{Sw,off}} \int_{T_B}^{T} [V_{in} \sin(\omega t) - V_{DC}]\, dt \\ &= T \times (I_L + I_{C_{Sw}} + I_{cmp} + I_{leak,C_S})\,. \end{aligned} \tag{3.12}$$

Solving the finite integrals gives

$$\begin{aligned} &\frac{V_{in}}{\omega \times R_{Sw,on}} (\cos(\omega T_B) - \cos(\omega T_A)) - \frac{V_{DC}}{R_{Sw,on}} (T_B - T_A) \\ &+ \frac{V_{in}}{\omega \times R_{Sw,off}} (\cos(\omega T_A) - 1) - \frac{V_{DC} \times T_A}{R_{Sw,off}} \\ &+ \frac{V_{in}}{\omega \times R_{Sw,off}} (1 - \cos(\omega T_B)) - \frac{V_{DC}}{R_{Sw,off}} (T - T_B) \\ &= T \times (I_L + I_{C_{Sw}} + I_{cmp} + I_{leak,C_S})\,. \end{aligned} \tag{3.13}$$

T_A and T_B can be calculated by equ. 3.14 and equ. 3.15, where δ_{on} and δ_{off} represent any delay associated with turning the switching transistor on and off, respectively.

$$T_A = \arcsin\left(\frac{V_{DC}}{V_{in}}\right) + \delta_{on} \tag{3.14}$$

$$T_B = \frac{T}{2} - T_A + \delta_{on} + \delta_{off}. \tag{3.15}$$

Based on these equations, the loss associated with each of the non-ideal components in the equivalent circuit (fig. 3.3(b)) can be determined as well. The loss due to the on-resistance $R_{Sw,on}$ can be expressed as

$$\begin{aligned} P_{loss R_{Sw,on}} &= \frac{1}{T} \int_{T_A}^{T_B} i_{Rin}(t)^2 \times R_{Sw,on} dt \\ &= \frac{1}{T} \times \frac{1}{R_{Sw,on}} \int_{T_A}^{T_B} [V_{in} \sin(\omega t) - V_{DC}]^2\, dt \end{aligned} \tag{3.16}$$

leading to

$$P_{lossR_{Sw,on}} = \frac{1}{T} \times \frac{V_{in}^2}{R_{Sw,on}} \left[\frac{T_B - T_A}{2} - \frac{\sin(\omega T_B)\cos(\omega T_B) - \sin(\omega T_A)\cos(\omega T_A)}{2\omega} \right] - \frac{1}{T} \times \frac{2V_{DC}V_{in}}{R_{Sw,on}} \left[\frac{\cos(\omega T_A) - \cos(\omega T_B)}{\omega} \right] + \frac{1}{T} \times \frac{V_{DC}^2}{R_{Sw,on}} (T_B - T_A) \quad (3.17)$$

Assuming ideal switching ($\delta_{on} = \delta_{off} = 0$), this can be simplified by making use of

$$\sin(\omega T_A) = \sin(\omega T_B), \quad (3.18)$$

$$\cos(\omega T_A) = -\cos(\omega T_B), \quad (3.19)$$

$$V_{in} \times \sin(\omega T_A) = V_{DC}, \quad (3.20)$$

and

$$V_{in} \times \cos(\omega T_A) = \sqrt{V_{in}^2 - V_{DC}^2}, \quad (3.21)$$

giving

$$P_{lossR_{Sw,on}} = \frac{T_B - T_A}{T} \times \frac{1}{R_{Sw,on}} \left(\frac{V_{in}^2}{2} + V_{DC}^2 \right) - \frac{3 \times V_{DC} \times \sqrt{V_{in}^2 - V_{DC}^2}}{2\pi \times R_{Sw,on}}. \quad (3.22)$$

While the dependency of $P_{loss,RSw,on}$ on the actual value of $R_{Sw,on}$ is not necessarily apparent from equ. 3.22, numerical solutions of the problem show that the smaller $R_{Sw,on}$, the smaller the loss associated with it. This is mainly due to the fact that a smaller on-resistance leads to a shorter on-time, reducing T_B - T_A. Since the transistor operates in the linear region when switched on, $R_{Sw,on}$ can be assumed to be constant during the on time and approximated by

$$R_{Sw,on} = \frac{L}{W \times \mu \times C_{ox} \times (V_{GS} - V_{TH})}, \quad (3.23)$$

where V_{GS} is equal to V_{DC}.

The loss associated with the off-resistance can be calculated in a similar way by solving

$$P_{lossR_{Sw,off}} = \frac{R_{sw,off}}{T} \times \left(\int_0^{T_A} i_{Rin}(t)^2 dt + \int_{T_B}^{T} i_{Rin}(t)^2 dt \right). \quad (3.24)$$

In this case, a smaller off-resistance increases the loss, since it imposes an additional discharge current on C_S, effectively reducing the current available at the output. Also, $R_{Sw,off}$, as opposed to $R_{Sw,on}$, is not constant over the entire period. This is due to drain-induced barrier lowering (DIBL) which modulates the threshold voltage as the input voltage changes. Due to the large fraction of the period in which the switch is typically off, the input voltage changes significantly and V_{DS} of the switching transistor can become quite large, leading to a varying off-resistance. However, an equivalent $R_{Sw,off}$ leading to the same amount of charge leaking through it per period as through the transistor when it is off can be defined. This can be best done through simulations and the resulting off-resistance can be modelled as

$$R_{Sw,off} = k \times R_{Sw,off}, \tag{3.25}$$

where k can be treated as a constant for a certain transistor flavor and input voltage, since the dependency on the output voltage for the range of interest is only marginal.

So far, all the loss terms have been frequency independent. The losses due to the capacitance associated with the switch however are frequency dependent and can be calculated by

$$P_{LossC_{Sw}} = I_{C_{Sw}} \times V_{DC} = f \times C_{Sw} \times V_{DC,}^2 \tag{3.26}$$

where C_{Sw} can be approximated by

$$C_{Sw} = W \times L \times C_{ox}. \tag{3.27}$$

Combining equ. 3.27 with equ. 3.23 gives a product of $R_{Sw,on}$ and C_{Sw} equal to

$$R_{Sw,on} \times C_{Sw} = \frac{L^2}{\mu \times (V_{GS} - V_{TH})} = \frac{L^2}{\mu \times (V_{DC} - V_{TH})} \tag{3.28}$$

Since both, a larger $R_{Sw,on}$ and a larger C_{Sw} lead to an increased loss, this product should be minimized. This can be most effectively done by choosing the transistor to have minimum L. This fact makes active rectifiers benefit from scaling and the 65nm technology used in this work a very good technology for the application. Equ. 3.28 can be used to calculate C_{Sw} associated with a particular on-resistance $R_{Sw,on}$ and output voltage V_{DC}. Since a smaller $R_{Sw,on}$ decreases the resistive loss but leads to a larger C_{Sw} and therefore an increased switching loss, an optimum transistor size exists which minimizes the overall loss.

In reality the equivalent capacitance that needs to be switched might be higher than indicated by equ. 3.27. Since it is important to switch the transistor as fast as possible after a crossing of $v_{in}(t)$ with V_{DC} is detected, an optimized driver chain interfacing the comparator with the switching transistor might be used. Assuming a fan-out of 4 buffer chain with inverters having a γ ($=C_{out}/C_{in}$) of 1, the actual switching capacitance is increased by 66% compared to the one suggested by equ. 3.27. The advantage of such an approach is that the actual

comparator only needs to drive a very small load, potentially leading to very low power comparator implementations. However, a careful overall optimization weighing delay and power consumption in the comparator and driver chain is needed to maximize the overall efficiency.

The power consumption of the comparator depends heavily on the chosen architecture and is driven by the need for fast switching at fairly low differential input voltages with a common mode around the supply voltage. Depending on the targeted output power of the rectifier and frequency of operation, its effect can be significant and designing a comparator with low enough power consumption can become very challenging.

Related to the amplifier is another source of loss, which is not explicitly shown in fig. 3.3, but can be quite significant: the delay between the ideal switching times and the time when the transistor is actually switched (δ_{on} and δ_{off} in equ. 3.14 and equ. 3.15). These delays impact the loss associated with the on- and the off-resistance of the switch (equ. 3.17 and equ. 3.24) and can easily become the main source of inefficiency in an active rectifier.

Finally, the remaining source of loss is associated with the leakage of C_S, which can be substantial when using large MOS-capacitors, especially in deeply scaled processes. It is modelled by the current source I_{leak,C_S} in parallel with I_L.

Taking all losses into account, the conversion efficiency is given by

$$\eta = \frac{I_L \times V_{DC}}{I_L \times V_{DC} + P_{LossR_{Sw,on}} + P_{LossR_{Sw,on}} + P_{LossC_{Sw}} + P_{cmp} + P_{leak,C_S}} \tag{3.29}$$

The input capacitance of a half-wave rectifier like the one shown in fig. 3.3, consists of the capacitances associated with the drain/source terminal of the switching transistor, the input capacitance of the comparator and a part due to the current drawn during the time the switch is on. Since the current is drawn during the time the input voltage peaks, the extracted charge has only a small effect on the actual phase of the input signal and its effect on the equivalent input capacitance is heavily attenuated [Hajimiri98]. However, it can be on the order of the other capacitances contributing to the total input capacitance and careful simulation of the input capacitance needs to be carried out to account for it when designing the interface with the antenna. It is important to note that C_S itself does not really affect the input capacitance, as long as it is large enough.

3.4.1.2 Full-Wave Rectifier

Unlike half-wave rectifiers, which only use half of the input wave to charge up the output capacitor, full-wave rectifiers use both half-waves of the signal. Although a range of topologies qualify as full-wave rectifiers under this definition, the analysis of this section is restricted to bridge-type full-wave rectifiers such as the one shown in fig. 3.5. The main benefit of these full-wave rectifiers is that they allow for a reduction of the output capacitor C_S by

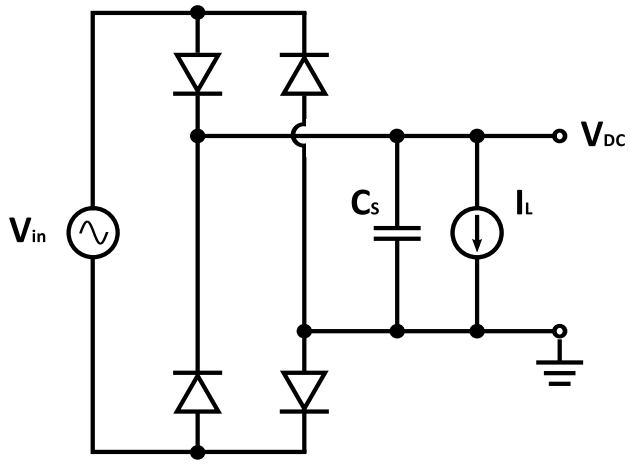


Figure 3.5: Bridge-type full wave rectifier

a factor of approximately two, while keeping the ripple the same. Full-wave rectification is typically achieved by having both output terminals of the equivalent AC source connected to diode-like devices to switch the polarity of the output terminal according to the polarity of the input voltage. This means that there are always two switching devices connected in series with the equivalent AC source's output terminals.

Despite these differences, the overall loss factors are quite similar. Assuming the same transistor sizes, the loss due the on-resistance is equal to the one of a half-wave rectifier. Due to the combination of two switches in series, $R_{Sw,on}$ in equ. 3.16 needs to be multiplied by a factor of 2, but since the switches are on twice as often, the integral needs to be multiplied by 2 as well, and the two effects cancel each other out.

The same is true for the loss due to the off-resistance. During the time when neither of the switches is on ($|v_{in}(t)| < V_{DC}$) , two transistors turned off in parallel are connected to each output terminal, leading to an equivalent loss as in the half-wave rectifier during that time. When one branch is on ($T_A < \mathrm{t} < T_B$ and $T/2+T_A < \mathrm{t} < T/2+T_B$), two transistors turned off are connecting the output terminals to the the input terminal of the "wrong" polarity. Since the two transistors are effectively connected in series, the loss is only half of the loss associated with the off-resistance for half-wave rectifiers during the time $T/2+\mathrm{T}_A < \mathrm{t} < T/2+\mathrm{T}_B$. However, since leakage current is also flowing through the off-transistors during $\mathrm{T}_A < \mathrm{t} < \mathrm{T}_B$, which does not happen in half-wave rectifiers, the overall loss is equivalent to the one of a half-wave rectifier.

When it comes to the switching losses, full-wave rectifiers suffer from the fact that they need more transistors to be switched. Typical state-of-the-art full-wave rectifier implementations use at least 2 active switching transistors ([Guo09, Lee11]), which doubles the losses associated with C_{Sw}. Since each active transistor needs a separate comparator as well, the lost power due to the power consumption of the comparators multiplies as well. There are full-wave rectifiers using only 1 active switching transistor, but they have at least 3 series

connected transistors, increasing the resistive losses [Peters08]. Reducing the number of transistor actively switched by a comparator is typically achieved by connecting the gate of the transistor not actively switched to one of the antenna terminals, effectively increasing the input capacitance of the circuit. This might have an impact on the antenna interface and limit the maximum frequency at which the antenna can be effectively resonated out as discussed in section 3.3.

One loss factor that does get reduced by full-wave rectification is the leakage of C_S, if C_S is scaled to maintain the same ripple compared to a half-wave rectifier.

Considering all these aspects, bridge-based full-wave rectifiers are an option when the overall size is dominated by the output capacitance and size is an issue, but their performance might suffer at higher frequencies due to the increased switching losses.

3.4.1.3 Design Example

The mathematical insights in the loss mechanisms of active rectifiers gained in section 3.4.1.1, allow to relatively quickly estimate the overall performance and optimize the switch size for maximum efficiency. In this section a rectifier for a system with a 2.5 by 2.5 mm^2 receive antenna is designed. The input frequency, power and voltage levels were taken from chapter 2, the equations from section 3.4.1.1 were implemented in Matlab and the constants were calibrated to the available 65 nm CMOS technology. For a given input voltage and frequency and a fixed output DC current, the Matlab script determines the conversion efficiency and the corresponding DC output voltage as a function of the on-resistance of the switches and the delays of the comparator. Since the efficiency of an active rectifier to first order decreases with increasing frequency, decreasing input voltage, and decreasing power, the smallest implant antenna size still achieving a DC voltage larger 0.5 V was chosen to explore the limits of this architecture.

Based on fig. 2.3 the input frequency for the given antenna size is approximately 170 MHz and according to figures 2.8 and 2.9 the input power and voltage amplitude are 1.35 mW and 0.64 V, respectively. Due to the frequency being an order of magnitude higher than the frequencies of the fastest active rectifiers published so far (table 3.1) an active half-wave rectifier was chosen for its smaller frequency dependent losses.

With the parameters of the input signal known, the DC output current I_L still needed to be determined before performing the computations in Matlab. To get a first estimation for the maximum current that can be delivered at the output of the rectifier, a conversion efficiency of approximately 80% and an output voltage of approximately 0.6 V were assumed. This lead to an I_L of 1.8 mA, which was than used as starting point for finding the final value iteratively. The first Matlab simulation using this I_L suggested a slightly higher efficiency of approximately 85% at a slightly lower output voltage of approximately 0.58V. Adjusting I_L to 2 mA for the following optimizations did not change the efficiency or the output voltage significantly and 2 mA was therefore used for the remaining optimization steps.

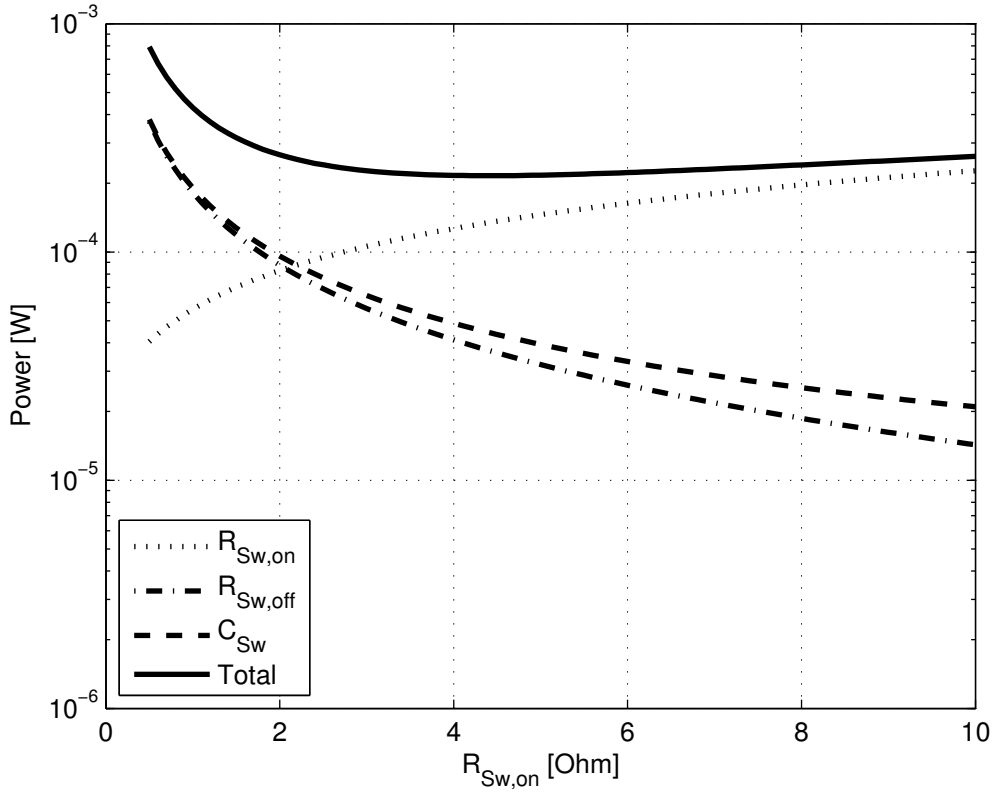


Figure 3.6: Various losses in half-wave rectifier for different $R_{Sw,on}$ using low V_{TH} devices

First, the optimum switch size was determined assuming an ideal comparator (no delay, zero power) and output capacitor (no leakage). While the delay was assumed to be zero, the switched capacitor C_{Sw} was increased by 66% assuming the switch is driven by a fan-out of 4 buffer chain. This approach is justified by the fact that introducing switching hysteresis in the comparator allows, at least in theory, to achieve zero overall switching time. Therefore the impact of the delay on the performance was investigated separately later on. Due to the low input voltage and the high input frequency, the fastest transistor (lowest threshold) available in the technology was the first candidate for the switching transistor.

Fig. 3.6 shows the losses due to the different components associated with the switching transistor for different on-resistances (transistor sizes). As expected, for very small on-resistance (large transistors) the switching losses dominate over the losses due to the on-resistance. What is a little bit less obvious is that the loss due to the finite off-resistance is comparable to the switching losses and therefore has a significant impact on the efficiency of the rectifier.

A transistor with a slightly higher threshold voltage was therefore investigated as well. As shown in fig. 3.7, due to the larger off-to-on resistance ratio of this transistor flavor, the

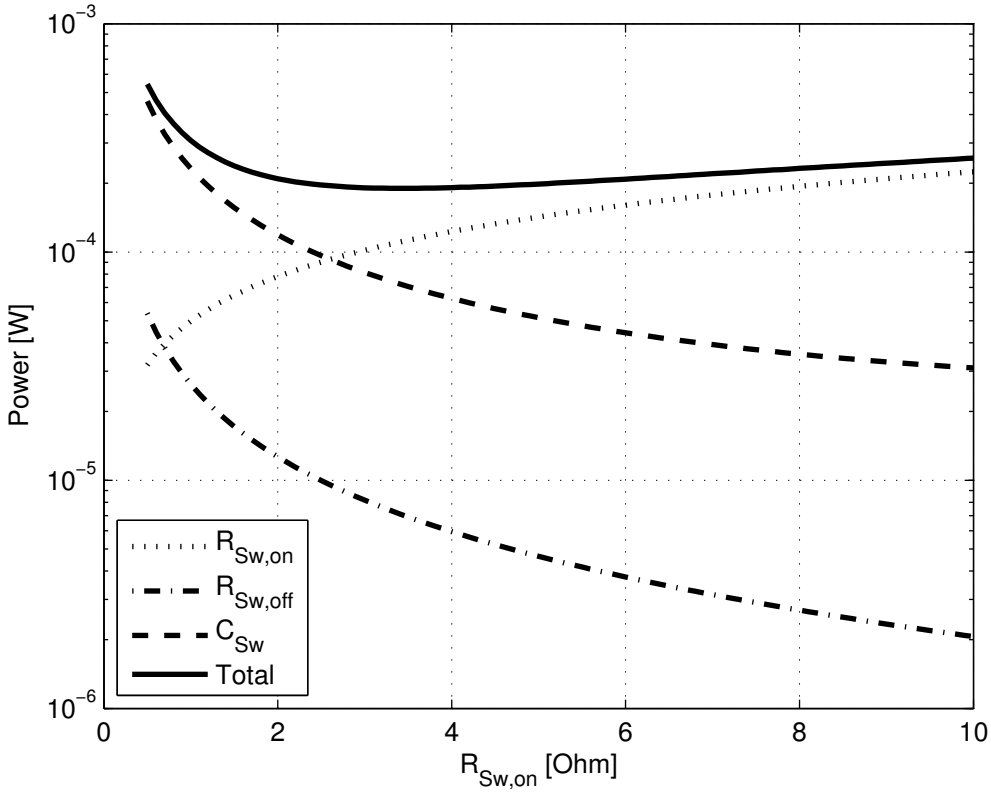


Figure 3.7: Various losses in half-wave rectifier for different $R_{Sw,on}$ using standard V_{TH} devices

losses associated with the off-resistance are now an order of magnitude below the switching losses. Although this comes at the cost of an increased transistor size and hence C_{Sw} for a certain on-resistance, using the standard as opposed to the low V_{TH} device improves the overall maximum efficiency by approximately 2%.

Fig. 3.8 shows the DC output voltage and the overall efficiency as a function of the on-resistance of the transistor. The efficiency exhibits a rather broad optimum and efficiencies above 80% can be achieved for a wide range of transistor sizes. It also shows that making the transistor too large significantly reduces the efficiency. At the same time, the minimum required output voltage puts a limit on the minimum transistor size. If the rectifier is followed by a linear voltage regulator to regulate the actual supply voltage to e.g. 0.5 V it might also make sense to sacrifice rectifier efficiency and operate at lower output voltages to achieve higher combined rectifier and voltage regulator efficiency. Achieving a higher overall efficiency is possible because the efficiency of the linear voltage regulator is, to first order, given by V_{out}/V_{in}, where V_{in} is equal to V_{DC} of the rectifier and V_{out} is equal to the regulated output voltage.

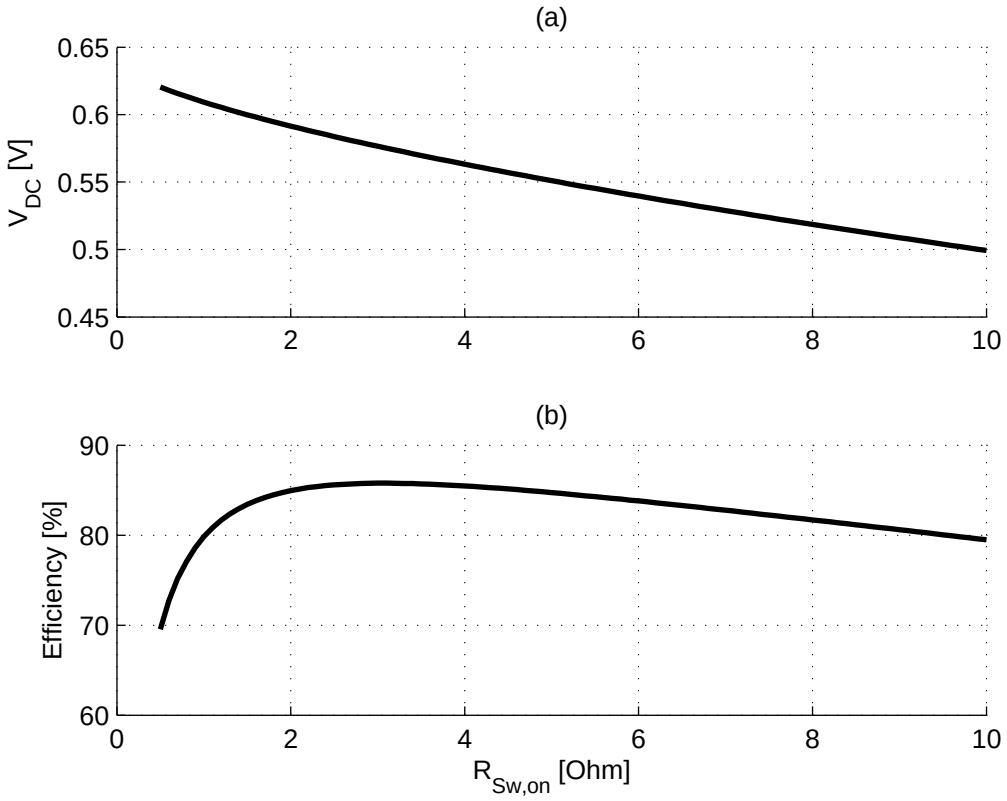


Figure 3.8: Output DC voltage (a) and conversion efficiency (b) for different $R_{Sw,on}$ using standard V_{TH} devices

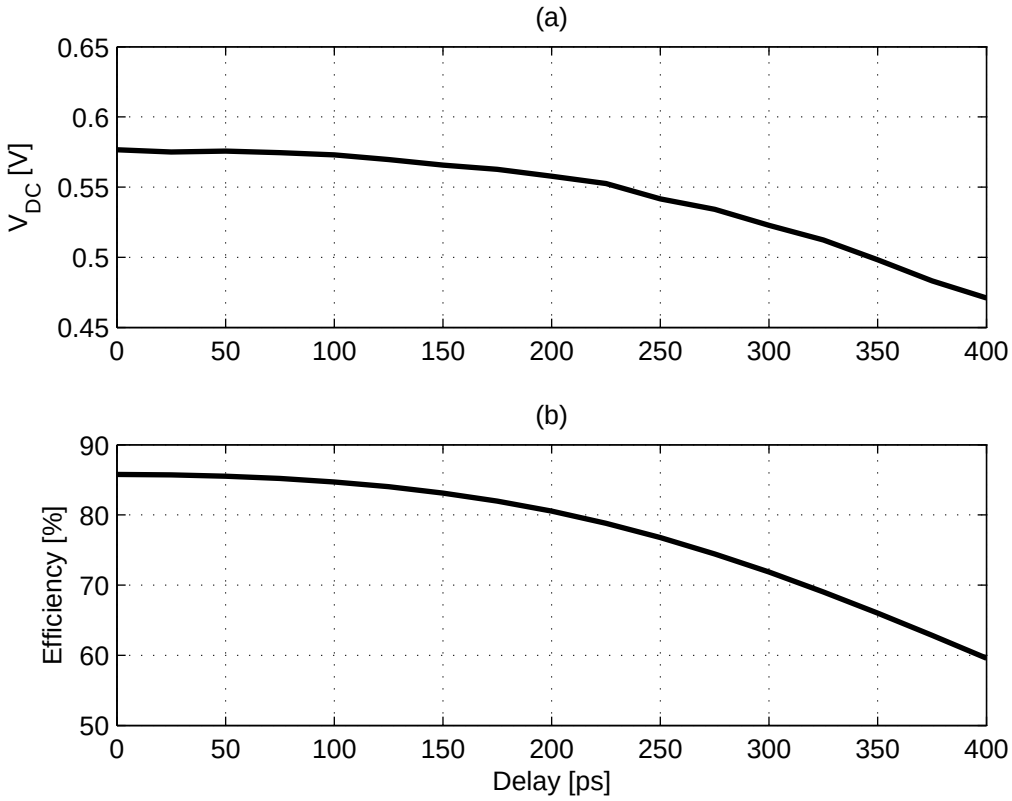


Figure 3.9: Output DC voltage at maximum efficiency (a) and maximum efficiency (b) for different delay ($\delta_{on} = \delta_{off}$) using standard V_{TH} devices

The effect of a delay between the ideal and the actual switching time is illustrated in fig. 3.9. It shows the maximum efficiency for a varying delay and the corresponding output voltages, where the delays for turning the transistor on and off were assumed to be equal (δ_{on}=δ_{off}). Delays of up to 150 ps have only a minor effect on the overall efficiency, but they start reducing the efficiency and the output voltage substantially once they exceed this value. The target delay for the comparator including the buffer chain was therefore set to be below 150 ps.

It turns out that, due to the low supply voltage and the gate capacitance of the optimum sized transistor being around 1 pF, the delay of the optimized buffer chain itself is already on the order of the 150 ps, even when using the fastest transistors available in the technology. To overcome this problem a comparator with adaptive input offset was implemented, effectively moving the actual switching points before $v_{in}(t)$ and V_{DC} cross. A common-gate comparator injecting offset currents depending on its output state adapted from a design first proposed by Lee and Ghovanloo [Lee11] was implemented. The common-gate input stage was chosen for its high speed, very low power capabilities and its suitability to operate at low supply voltages. It is also guaranteed to start-up during initial power ramp-up. This is particularly

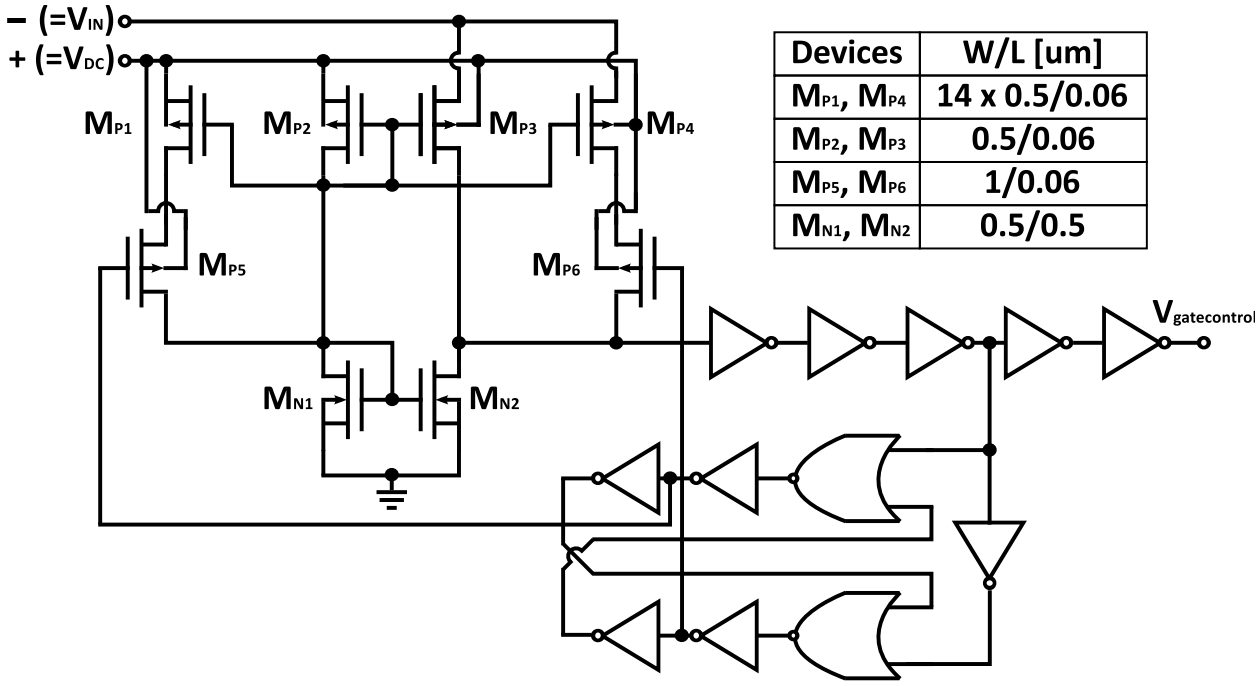


Figure 3.10: Common-gate comparator with adaptive input offset

important for systems that are powered purely by the incoming AC signal, since no stable supply is available at the onset of supplying power to the system.

Fig. 3.10 shows the implementation of the comparator including the buffer chain to drive the switching transistor. Non-overlapping control signals are generated to avoid ringing due to too fast switching between the different switching thresholds. When the output is off (high), the switching threshold for v_{in}(t) with respect to V_{DC} is lowered by injecting an additional current into M_{N2}, causing the voltage at its drain terminal to increase, leading to the output turning on earlier as $v_{in}\,(t)$ increases [Lee11]. The same thing happens when the output is on (low), by injecting a current into M_{N1}. Using this method the overall delays, including the delay of the buffer chain, can be controlled to be well below 150 ps while consuming only around 4.2 μW in the common-gate input stage. This is achieved even when the last inverter of the buffer chain is removed, which reduces the total switched capacitance by more than 15% while only marginally increasing the delay. The final delays achieved are approximately 110 ps and 90 ps for turning the transistor on and off respectively. The simulated timing of the signal controlling the gate of the switching transistor with respect to $v_{in}\,(t)$ and V_{DC} is shown in fig. 3.11.

It is important to note that, although the comparator input stage is guaranteed to start-up, the delay during start-up is much larger due to the supply voltage of the buffers still ramping up. This can cause the output to settle at a voltage much lower than that required. One way to overcome this problem is to increase the input voltage during start-up (for a few microseconds only) until all the inverters work correctly and the timing is in a region where

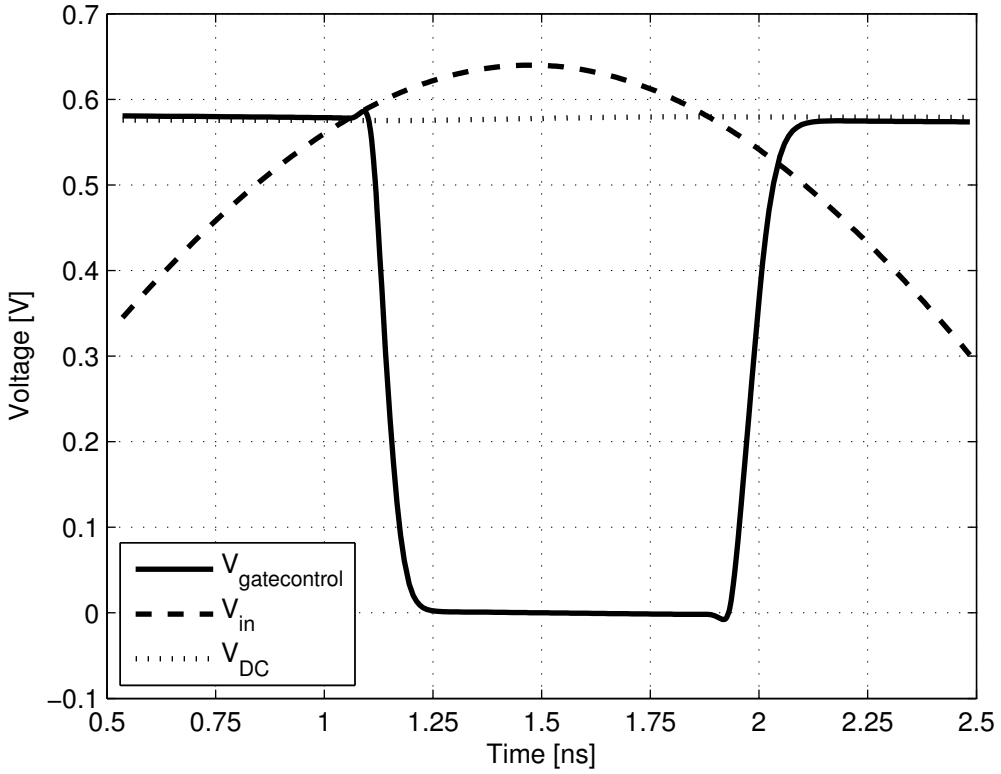


Figure 3.11: Simulated timing of the switching transistor's gate signal with respect to v_{in} and V_{DC}

it can support further increase of the output voltage towards the target value. Since the increased transmit power required to achieve this has to be applied only for a very short period of time, it does not impact the time averaged SAR and hence the transmit power during normal operation.

With a C_S of 2.5 nF, implemented by a MOS cap, the leakage loss stays well below the power of the comparator and the total simulated efficiency is 85.1% at an output voltage of 0.577 mV. This is within 1% of the results obtained by using the equations from section 3.4.1.1 when using simulated delay values. It also falls well within the range of efficiencies reported in table 3.1, although operating at a frequency at least one order of magnitude higher than previously published converters.

The simulated input capacitance is around 2.4 pF making it negligible compared to the more than 170 pF capacitance needed to resonate out the single turn loop antenna used when deriving the input specifications for this circuit, which has an impedance of 0.1917 + j 5.37 Ω at 170 MHz.

All in all this proves that active rectifiers are well suited even for low power, high frequency

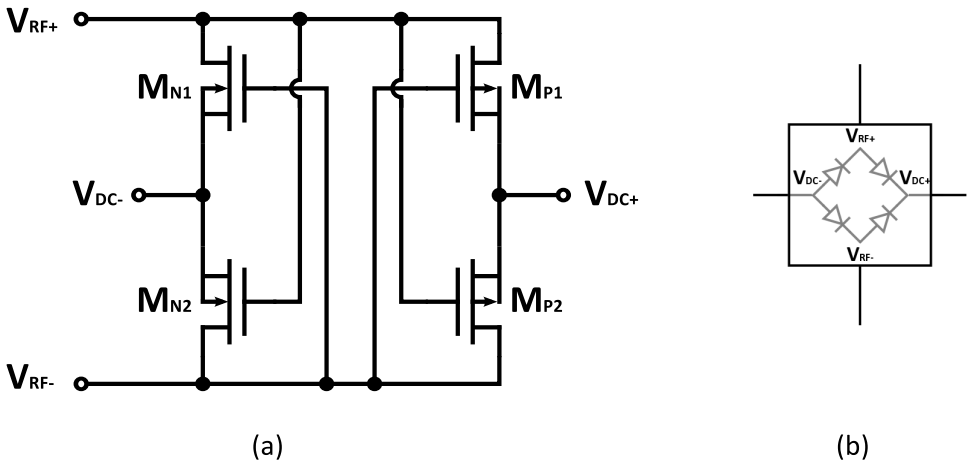


Figure 3.12: Self-driven synchronous rectifier: circuit (a) and symbol (b)

input signals in the context of wireless power transfer to implantable BMI sensors, as long as the input voltage exceeds the minimum required supply.

3.4.2 Self-Driven Synchronous Rectifier

Self-driven synchronous rectifiers are another way of reducing the forward voltage drop associated with the threshold voltage of a transistor used in a diode-like fashion. This is achieved by connecting the gates of the switching transistor to the terminal of the input signal not connected to it, effectively increasing V_{GS} of the transistor, therefore reducing its on resistance. Typically, this principle is applied to bridge-type full wave rectifiers, leading to an implementation like the one shown in fig. 3.12 (a).

The main benefits compared to the active rectifiers described before are the lack of comparators and the fact that the main switched capacitance is connected in parallel to the input and can therefore be absorbed in the resonant tank interfacing with the antenna. This makes the efficiency of these kinds of rectifiers to first order independent of the frequency of the input signal. Another important aspect is that, by steering the currents based on the difference between the on- and off- resistances of the transistors, it also works for input voltages below the threshold voltages of the transistors [O'Driscoll09]. For input voltages larger than the threshold voltage however, the transistors do not turn off immediately after the input voltage drops below the output voltage. The maximum efficiency does therefore not reach the efficiencies of active rectifiers. Combining a self-driven synchronous rectifier with an active rectifier is a possibility to overcome this problem, but the overall behavior resembles that of an active full-wave rectifier analyzed before [Peters08].

The lack of active circuitry and the ability to operate at low voltages make them a good choice for low voltage, high frequency input signals.

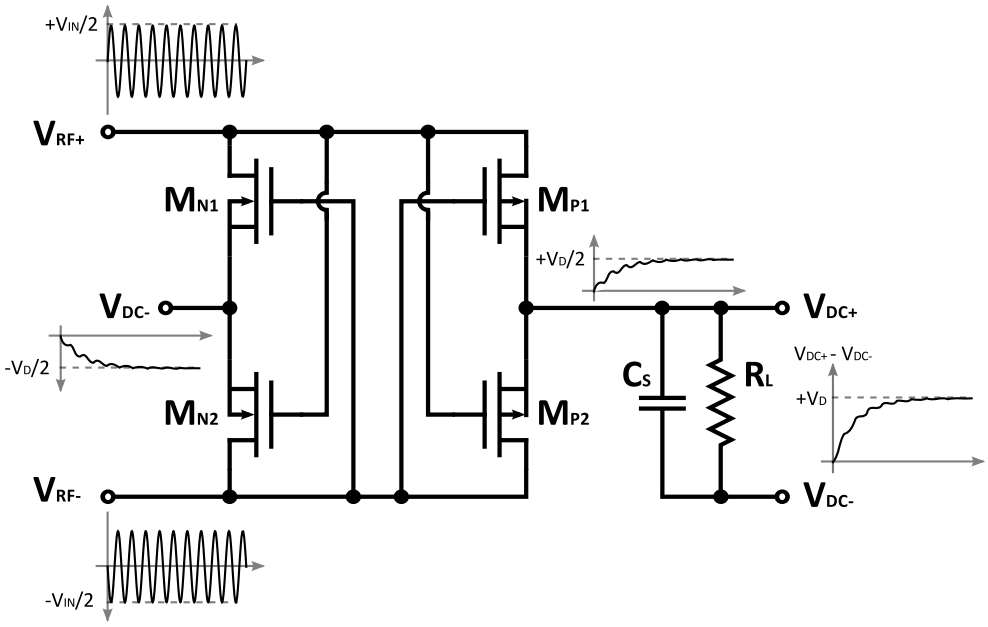


Figure 3.13: Single stage self-driven synchronous rectifier with signals

3.4.2.1 Single Stage Operation

Fig. 3.13 shows a single stage self-driven synchronous rectifier driving a resistive load and including a capacitor C_S to reduce the ripple of the output voltage. Voltage waveforms are also annotated. Although fig. 3.13 shows a fully symmetric input voltage, symmetry is not required for proper operation of the circuit.

The way the circuit works is the following: when V_{RF+} is more positive than V_{RF-} transistor M_{P1} starts turning on and becomes less resistive than M_{N1} (assuming equal transistor sizes and threshold voltages). The current from V_{RF+} gets directed towards V_{DC+} . Similarly, M_{N2} starts turning on and M_{P2} becomes more resistive, steering the current from V_{DC-} towards V_{RF-}. Together with the current through M_{P1} it charges up C_S and provides the current for the load. When the input polarity changes, M_{N1} and M_{P2} carry the main current and preserve the output polarity. Ideally, if the on-resistance of the transistors would be zero and their off-resistance would be infinite, the output voltage would reach $+V_{IN}$. In reality though, the output voltage reaches only V_D, which is always lower than V_{IN}.

In order to analyze the expected performance and come up with design guidelines, the input current averaged over one signal period is again equated with the average output current. Since, depending on the actual input voltage, the region of operation of the transistors might change, an analytical model to analyze the circuit would be overly complicated and provide only limited design guidance. A simulation based analysis and design methodology based on simulating only one transistor over one signal period is therefore introduced. The key to this analysis are the voltage waveforms at the transistor terminals in steady state. Fig. 3.14

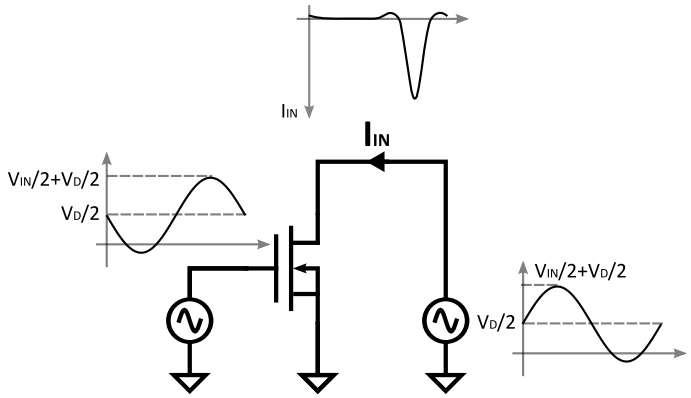


Figure 3.14: Single transistor with signals during one period

shows the equivalent steady-state voltage waveform at a NMOS transistor and the resulting drain current waveform.

A similar setup can be derived for the PMOS and, together, they can be used to quickly simulate the expected overall performance and size the transistors for the design targets. Assuming a fixed input amplitude V_{IN}, the first step is to sweep the output voltage V_D and calculate the average input current I_{IN} over one period of the input signal. Again assuming equally strong NMOS and PMOS devices, two times the averaged input current is equal to the average current that can be supplied to a load, since the average currents of the NMOS and PMOS transistors both contribute to the output current. Fixing the required output current I_L leads to a fixed output voltage V_D and vice versa. The results of the same simulation can also be used to estimate the expected input power by averaging the integral of the instantaneous product of the input current $i_{in}(t)$ and $v_{in}(t)$ and multiplying it again by two. Since the average output power is simply V_D times the average output current, the overall efficiency can be estimated easily. Equations 3.30 to 3.32 summarize the described dependencies.

$$I_L = \frac{2}{T} \int^{T} i_{in}(t)dt \tag{3.30}$$

$$P_{in} = \frac{2}{T} \int^{T} i_{in}(t) \times V_{IN} \times sin(\omega t)dt \tag{3.31}$$

$$P_{out} = I_L \times V_D \tag{3.32}$$

Fig. 3.15 shows the efficiency and the output current for a V_{IN} of 60 mV and different values of V_D, based on the simulation of a single low-threshold voltage NMOS transistor in 65 nm CMOS with a $^{W}/_{L}$ of $^{425.3}/_{0.105}$. For such a small input amplitude, the achievable efficiencies

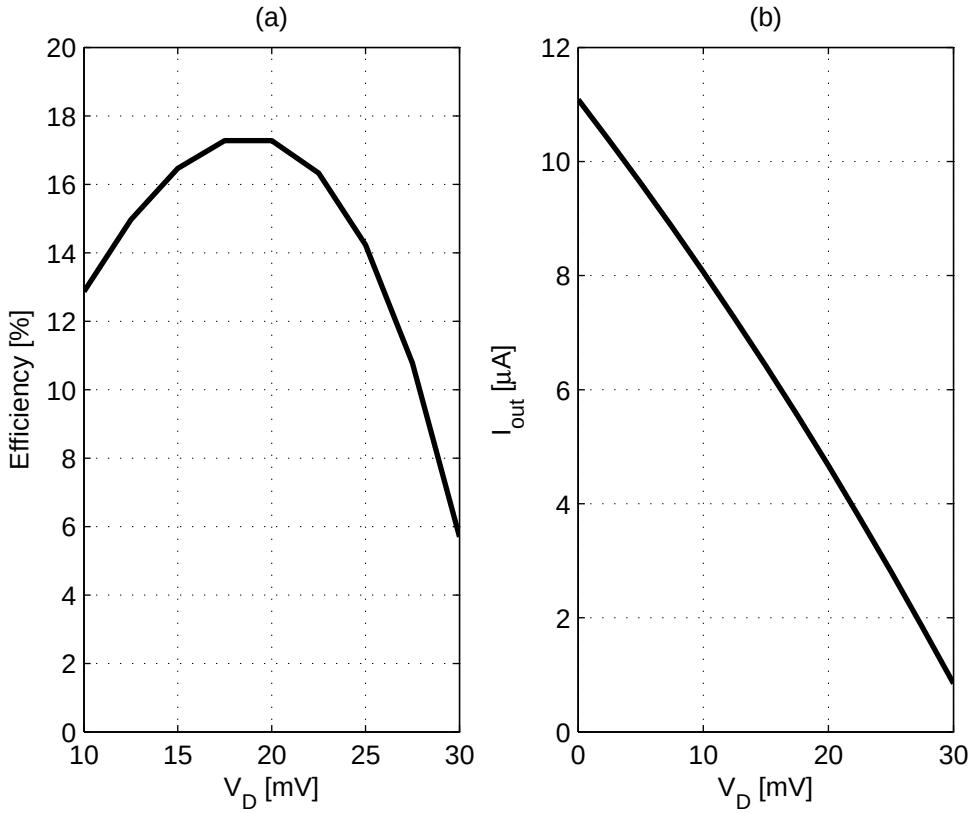


Figure 3.15: Efficiency (a) and average output current (b) over one period for different output voltages per stage

are rather low, as is the DC output voltage at which the peak efficiency is achieved. Since the efficiency is primarily determined by the on-to-off ratio of the transistor currents, it mainly depends on the input amplitude V_{IN} and the output voltage V_D and is largely independent of the actual transistor size, as long as any effects of the transistor's dimension on the device's threshold voltage are neglected. The average output current however, is heavily dependent on the transistor geometries. In other words, while changing the transistors width shifts the current curve in fig. 3.15(b), it does not change the curve in fig. 3.15(a). This means that the rectifier can easily be designed to operate at its peak efficiency point by scaling the transistors until they are able to provide the required current at the voltage leading to the highest efficiency.

The exact value of the input capacitance of the rectifier has to be obtained by simulation as well, but it can be estimated to be on the order of the gate capacitance of one NMOS plus one PMOS transistor.

3.4.2.2 Multi-Stage Operation

Since the output of a single-stage self-driven synchronous rectifier is always below the input amplitude V_{IN}, and DC voltages larger than at least 0.5 V are needed, using a single stage at low input voltages is not an option. Fortunately, this type of rectifier lends itself very well to obtain voltage multiplication by cascading single stages in a charge pump configuration [Mandal07]. Fig. 3.16 shows an example of 3 stages with inputs connected in parallel (at AC) and outputs connected in series to obtain an output voltage V_{DD} equal to 3 times V_D of a single stage.

The coupling capacitors are crucial for the charge pump operation. They need to be large enough to minimize any reduction of the input voltage to the stages due to the capacitive voltage dividers they form with the input capacitance of a single stage. Additionally their equivalent impedance needs to be small compared to the on-resistance of the rectifying transistors. Depending on the frequency of operation one of the two constraints limits the minimum value of C_C. Capacitors with low parasitic bottom plate capacitance are preferred, since the bottom plate capacitance either reduces the input voltage or increases the circuit's input capacitance, depending on which terminal is connected to the input.

In general, with N being the number of stages, the input current, the output voltage and the input capacitance all scale linearly with N, while the input resistance scales with $1/N$ and the output current and overall efficiency remain constant (neglecting higher order effects).

While this approach theoretically allows the design of a system providing a specified output voltage at the peak efficiency by cascading a number of stages, each operating at the optimum V_D, it can take up a prohibitively large die area, especially when operating from low input voltages while driving relatively large currents. In such a case, due to the small V_{GS} of the transistors, very large transistors might be needed to provide the required average current. Large transistors mean large input capacitance, requiring even larger coupling capacitors

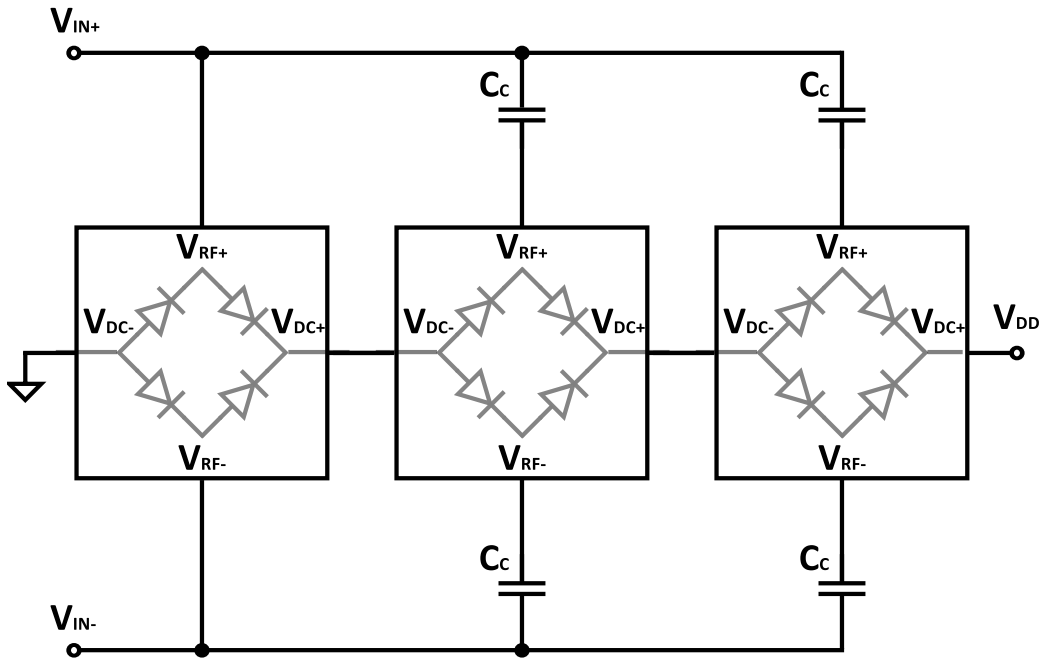


Figure 3.16: Multistage configuration of self-driven synchronous rectifier for voltage multiplication

C_C. Combined with a larger number of stages the area taken up by coupling capacitors might exceed the area budged or the total input capacitance might become so large that it resonates with the antenna at a frequency below the frequency of operation.

One way to increase the drive strength of a transistor of a fixed size is by adding a DC bias to the gate terminals of the transistors, effectively reducing their threshold voltages. By realizing that, in a multi-stage charge pump configuration, the input voltage of a stage up or down the chain is equal to the input voltage of the stage in between shifted up and down by one V_D respectively. Such DC shifted gate control signals can be obtain at the cost of only a little routing overhead. This principle is subsequently referred to as inter-stage gate control.

Fig. 3.17 shows the adapted circuit and symbol of a single rectifier cell that can be used in multi-stages configurations, such as the one shown in fig. 3.18, where signals from the second-next stages are used to obtain a DC shift of 2 times V_D. The reason for placing the cell directly connected to the input without going through a capacitor C_C in the center of the chain is related to start-up performance and will be explained later.

Only simple modifications to the simulation setup need to be made, as shown in fig. 3.19, to use essentially the same design procedure as outlined before for the standard self-driven synchronous design. The factor in front of the first V_D term of the gate voltage corresponds to the number of stages away from which the gate control signal is taken for the current stage. This number is called n, and for the implementation shown in fig. 3.18 n would be

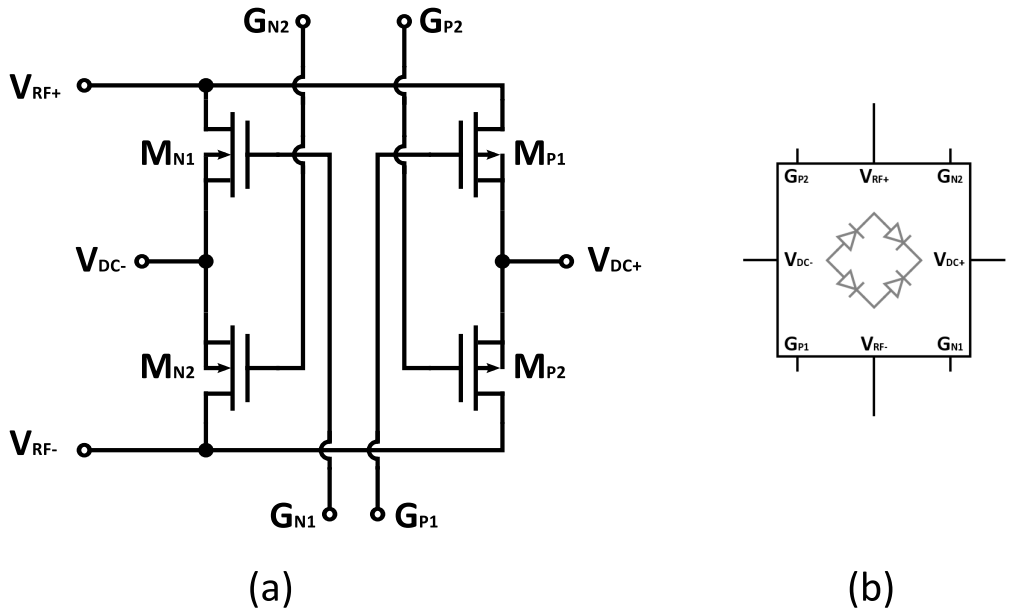


Figure 3.17: Self-driven synchronous rectifier cell for inter-stage gate control: circuit (a) and symbol (b)

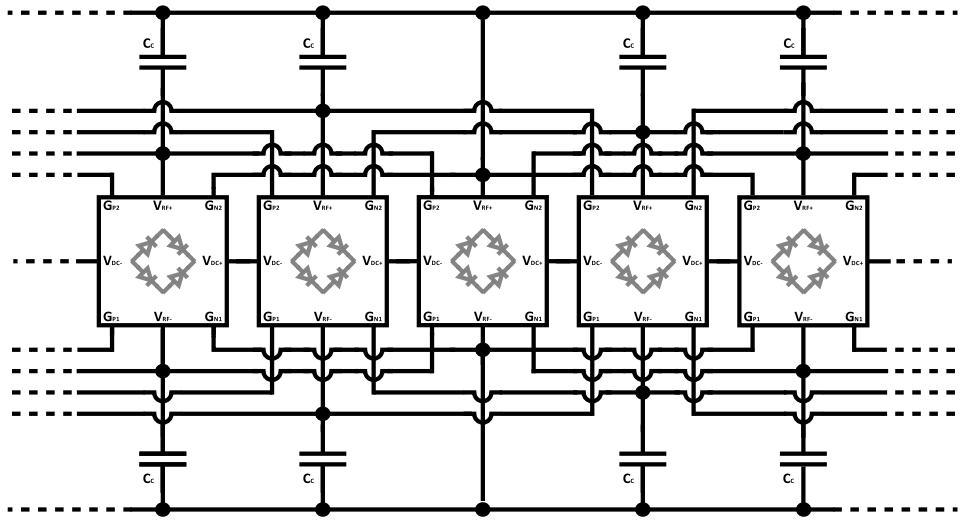


Figure 3.18: Multistage configuration of self-driven synchronous rectifier with inter-stage gate control (n=2)

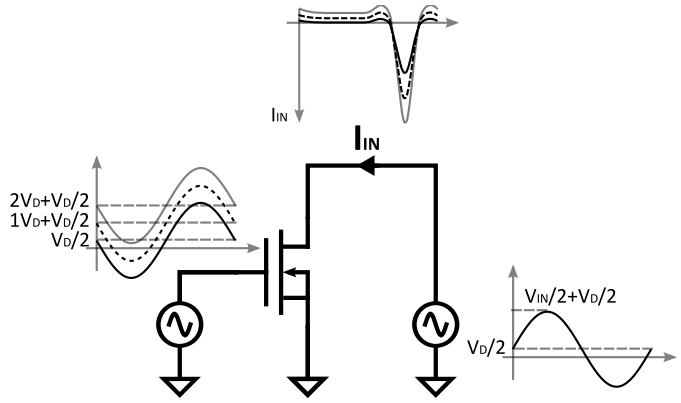


Figure 3.19: Inter-stage gate control: single transistor with signals during one period

equal to 2. A conventional self-driven synchronous design, shown in fig. 3.16, has an n of 0. As indicated by the waveform of I_{IN} sketched in fig. 3.19, adding a DC offset to the gate signal not only increases the on-current, but also the off-current. Inter-stage gate control is therefore only beneficial when operating with input voltage amplitudes well below the threshold voltages of the transistors.

The effect of inter-stage gate control is shown in fig. 3.20. It shows the efficiency and the output current for different orders of inter-stage gate control with the same input voltage and transistor geometry used to derive fig. 3.15. While the peak efficiency and the corresponding voltage increase per stage, V_D, slightly decrease, the output current substantially increases with n. For n of 2, the current at a V_D of 20 mV increases by a factor of more than 2.8, while the efficiency only drops by less than 6%. This means that the active area of the rectifier could be, to first order, reduced by a factor of approximately 2.8, also reducing the equivalent input capacitance C_{in} of the rectifier. In the case where the minimum size of the coupling capacitors C_C is limited by the input capacitance of a single stage this also means the total area can be reduced substantially. It might also reduce the input capacitance enough to be able to resonate out the inductive antenna at the input frequency, in case it is too large to do so for n = 0.

However, there are also some issues with the inter-stage gate control approach. As shown in fig. 3.20 (b), two values of V_D leading to the same output current exists for n larger than 0. Simulations showed that they might be both positive or even have different polarities. It is therefore important that the circuit settles at the desired value of V_D when starting up. One way of ensuring this is to use a hybrid approach, where either some of the cells are used with n=0, or each transistor in a single cell is split up with one gate connecting to that cell's own input and the second gate connecting to a different stage. Additionally, reducing the load current to a minimum during start-up helps the circuit to power up at the highest possible voltage and settle at the optimum point under full load conditions.

Since the current to initially charge the coupling capacitors C_C enters the circuit through the stage directly connected to the input without a coupling capacitor and propagates through

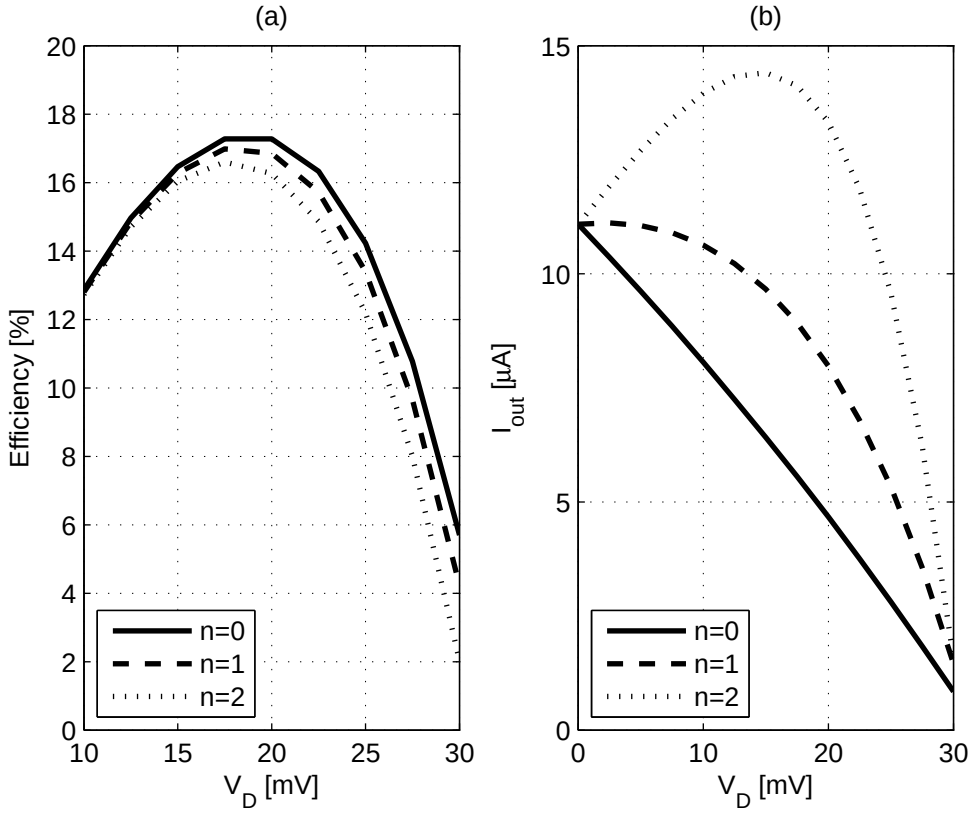


Figure 3.20: Efficiency (a) and average output current (b) for different number of inter-stages

the stages, placing the stage directly connected to the input in the center of the cascaded chain, as indicated in fig. 3.18, speeds up start-up and reduces the chances of a single stage settling in the non-optimum stable operating point.

The approach of using neighboring stages to obtain the DC shifted gate control signals is limited to the stages that are not sitting at either end of the cascaded chain. Scaled down "dummy" stages can be appended at each end to generate the DC shift required for the first and last stages. Another approach is to use standard self-driven synchronous rectifier stages at the ends of the chain. Doing so increases the overall area and input capacitance, but it also provides anchors for start-up, ensuring that neighboring cells see DC shifts with the appropriate polarities even at the onset of start-up.

Overall, start-up is a critical issue when using inter-stage gate control, and careful simulations need to be carried out to ensure reliable start-up.

3.4.2.3 Input Voltage Dependence

Assuming the overall area is not a constraint, meaning any number of stages can be used and the coupling capacitors can always be made large enough to not significantly impact the circuit's performance, the optimum conversion efficiency, to first order, only depends on the input voltage amplitude. Based on the simulation framework introduced in section 3.4.2.1, the maximum efficiencies and the corresponding optimum voltage increase per stage has been simulated for input voltages from 50 mV to 500 mV. The results are shown in fig. 3.21.

They clearly show a strong dependence of the efficiency on the input voltage for input amplitudes of less than 300 mV, which is approximately the threshold voltage of the transistors used. The efficiency saturates around 65% for larger input voltages. Increasing the input voltage from 50 mV to 300 mV increases the conversion efficiency by a factor of more than 5. At the same time, the voltage increase per stage at which the optimum efficiency is achieved increases from less than 15 mV to more than 200 mV, reducing the number of stages needed to achieve a required minimum DC output voltage, and therefore the chip area, by a factor of more than 10. Any method to boost the input voltage of the rectifier, like increasing the antenna impedance at resonance, therefore helps to increase the overall efficiency and should be considered if possible.

3.4.2.4 Design Example

In order to explore the limits of self-driven synchronous rectification for the application space of this work, 3 multi-stage self-synchronous driven rectifier circuits with different degrees of inter-stage gate control have been designed in 65nm CMOS and simulated for the 1 mm by 1 mm node. Again, the specifications for the input signal have been taken from chapter 2. The input amplitude is therefore 60 mV, the frequency is 220 MHz, the input power is 38 μW, and the antenna impedance is 0.1713 + j 2.82 Ω leading to an R_P of 46.7 Ω.

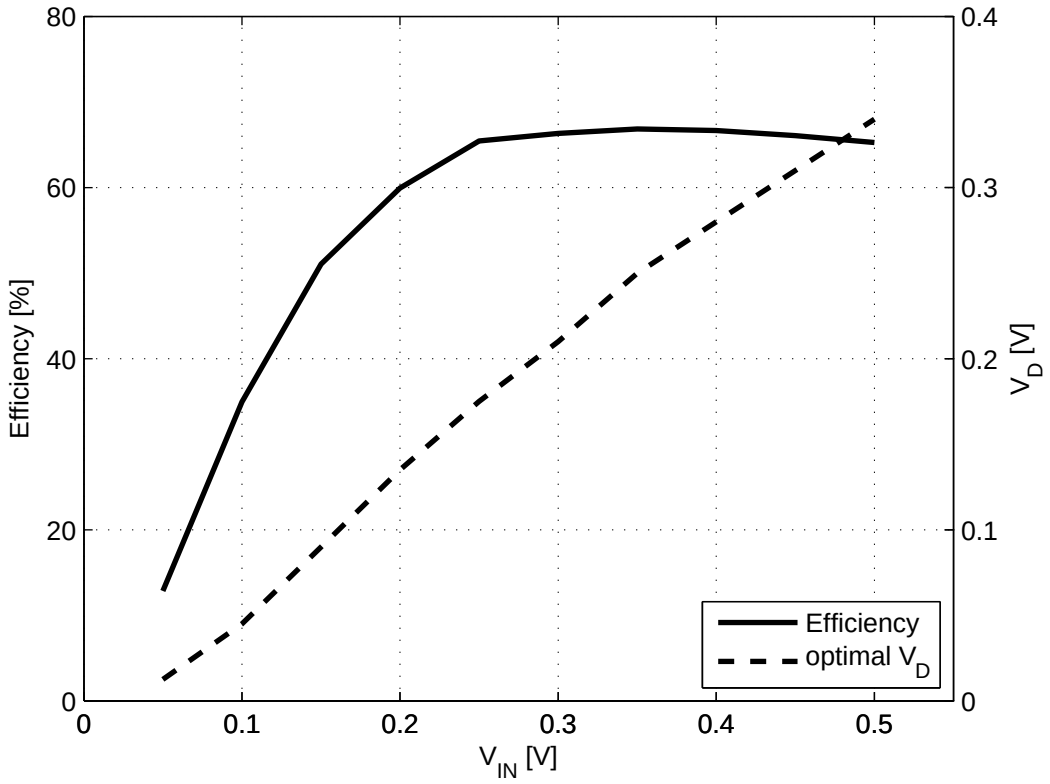


Figure 3.21: Efficiency and optimal voltage increase per stage (V_D) for self-driven synchronous rectifier vs. V_{IN}

n	Size NMOS [μm]	Size PMOS [μm]	C_C [pF]	C_{in} [pF]	Efficiency [%]	P_{out} [μW]
0	2283 / 0.105	4305 / 0.09	57	165	11.23	4.27
1	887.3 / 0.105	1679 / 0.09	53	84	14.88	5.65
2	425.3 / 0.105	804 / 0.09	50	62	15.04	5.72

Table 3.3: Comparison of different multi-stage implementations of self-driven synchronous rectifiers

Exploiting the simulation setup of section 3.19, various transistor flavors and geometries have been investigated with respect to their impact on the overall efficiency. Unlike in the case of the active rectifiers, where devices with slightly higher threshold voltages lead to a better overall performance, minimum V_{TH} devices are the better choice for this design. This has mainly to do with the much lower drive strength at these low input voltages, which would require the transistors with the second lowest V_{TH} to be at least 5 times larger than the ones with minimum V_{TH}. In this case the required size of the coupling capacitors would exceed the available area. Using transistors with non-minimum gate length is beneficial however, largely due to a reverse short-channel length effect on the threshold voltage and reduced leakage.

Simulations leading to fig. 3.20 obtained with the same input specifications as the ones used here, suggest an ideal V_D of 20 mV. This means that, in order to guarantee a minimum supply voltage while leaving some headroom for a low drop-out (LDO) regulator, at least 28 rectifier stages are needed.

While the standard self-driven synchronous rectifier consists of 28 identical stages, the implemented inter-stage gate controlled versions with n=1 and n=2 have 26 and 24 identical stages in the center with 1 and 2 fully self-driven rectifier cells (n=0) at each each end of the chain respectively.

Due to the low input voltage and the output current of approximately 10 μA, the transistors need to be very large, requiring large input coupling capacitors to keep the reduction in input voltage due to the capacitive voltage divider low. Using low parasitic metal-insulator-metal (MIM) capacitors for C_C and the overall size of the node being 1 mm by 1 mm, the total capacitance available on-chip for coupling of the stages is on the order of 3 nF.

The available capacitance is split up evenly between the stages for $n = 0$ and split up such that the capacitors for the corner cells with n=0 are two times larger than the remaining cells with n=1 and n=2 for the higher order inter-stage gate controlled designs.

Table 3.3 summarizes the design parameters for the 3 different designs and compares the simulated performance. The results were obtained at a DC output voltage of 0.55 V and using ideal capacitor models for the coupling capacitors. Due to the very low parasitic bottom plate capacitance of the MIM capacitor, the achievable performance using real devices is expected to be very similar to the one reported in table 3.3. Since the values of C_C are limited by

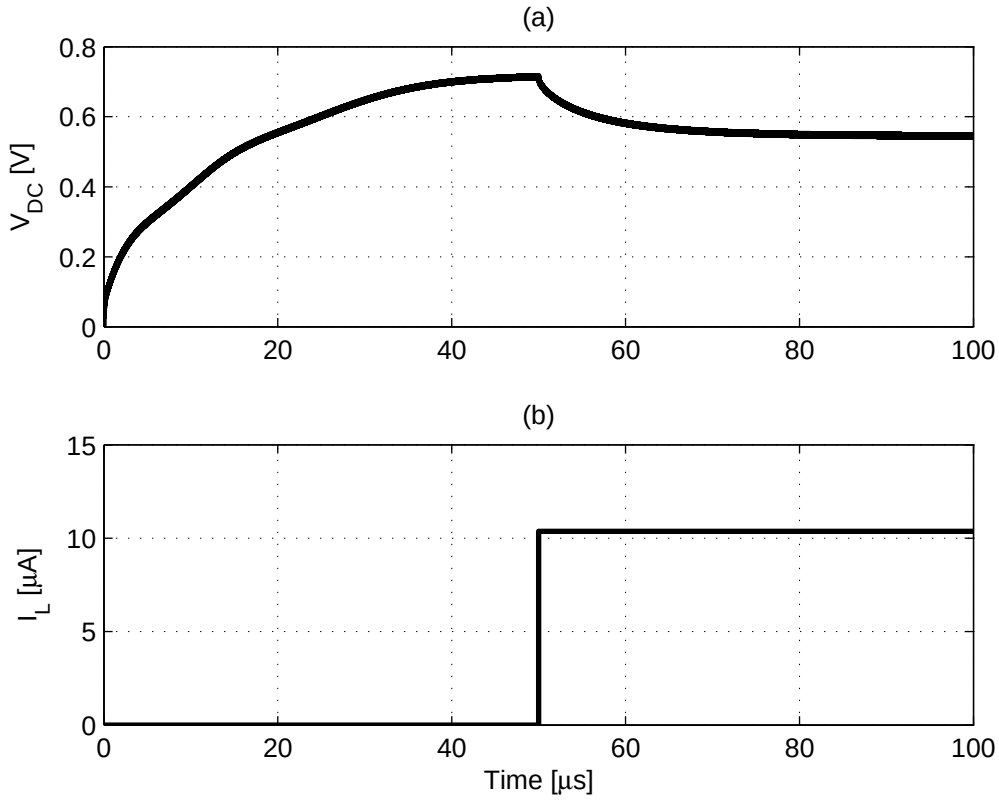


Figure 3.22: Simulated start-up of multi-stage self-driven synchronous rectifier with inter-stage gate control (n=2)

the size constraint of the chip, the effect of the coupling capacitors on the overall efficiency is appreciable, especially when no inter-stage gate control is implemented due to the large transistors. This is the main reason why the simulated efficiencies do not achieve the ones obtained based on the single transistor simulation shown in fig. 3.20. It also explains why the efficiency of the circuits using inter-stage gate control is higher than the one without. Overall, the efficiency is improved by more than 30 % while reducing the active area and therefore the input capacitance of the rectifier by more than 2.6 times when using an inter-stage gate control design with n=2 compared to a standard self-driven design. Although the total area is mainly determined by the coupling capacitors and is essentially the same for all designs, it is the active area that matters most, because due to the usage of MIM capacitors, the remaining circuits needed for the implant can be implemented underneath the capacitors.

Fig. 3.22 (a) shows the output voltage waveform during start-up for the design using n=2. The load current (shown in fig. 3.22 (b)) is initially turned off until the output voltage reaches a level indicating that the circuit reliably started up. This functionality can be achieved using a power-on detector which can be implemented at very low power levels as will be shown

in section 4.3.6. Together with having fully self-driven stages at the beginning and the end of the rectifier chain, this ensures that none of the stages settles at a non-optimum state as described in section 3.4.2.2.

3.5 Summary

AC-to-DC conversion circuits operating in steady-state can be modelled by an equivalent circuit with an input consisting of a capacitor in parallel with a resistor dependent on the input voltage and power, and a voltage dependent voltage source in series with a resistor at the output. This model can be used to analyze and optimize the interface to the antenna. For weakly coupled inductive loop antennas, resonating the antenna inductance with a capacitor in parallel to the circuit's input while matching the input resistance to the real part of the impedance of the resonant tank under maximum load conditions optimizes both input voltage and power absorbed by the rectifier. Non-weakly coupled antennas need to be simultaneously conjugately matched under full load conditions to achieve the maximum power transfer.

Depending on the amplitude of the input voltage and the required DC output voltage, two different AC-to-DC conversion approaches have been identified to provide the highest efficiencies achievable with standard CMOS technologies without extra post manufacturing steps. Active CMOS rectifiers achieve efficiencies of more than 80% for input voltages larger than both the threshold voltages of the MOS transistors and the required DC output voltage at low to medium input frequencies. Self-driven synchronous rectifiers are beneficial when the input voltage is lower than the required output voltage and at higher input frequencies and achieve efficiencies of up to 65%.

Analytical and simulation based analysis and design methodologies have been introduced for active CMOS rectifiers and their self-driven synchronous counterparts, respectively. Sample circuits for 2.5 mm by 2.5 mm and 1 mm by 1 mm implanted antenna size have been designed using these methodologies, pushing the limits of active and self-driven converters.

A strong dependency of conversion efficiency on the amplitude of the input voltage was observed for self-driven synchronous rectifier circuits for voltages below a few 100 mV. Although the concept of inter-stage gate control has been introduced to enhance the efficiency and reduce the size of multi-stage self-driven rectifiers converting very low input voltage levels, operating off of low input voltages remains rather inefficient from both a power and size perspective. Any approach allowing an increase in the input voltage should therefore be considered.

Based on the results of this chapter, conversion efficiencies of more than 80% can be expected for implants larger than approximately 2.5 mm by 2.5 mm, while the efficiencies drop from 65% to around 15% when reducing the size further down to 1 mm by 1 mm. These efficiency numbers do not include any losses due to the matching capacitor at the input, which can be estimated to be on the order of 10%, nor the loss of any regulators following the AC-to-DC

converter. Using linear LDO regulators, the losses can be divided into a part proportional to the voltage ratio between regulated and unregulated voltage and a constant part due to the power consumption of regulator building blocks such as references and amplifiers, with the latter having the potential of being on the same order as the available power for very small implants.

Chapter 4

Proof-of-Concept: A 1 mm^3 Neural Transponder

Combining the results from chapter 2 (fig. 2.8 and fig. 2.9) and chapter 3 (in particularly fig. 3.21) highlights that powering the smallest implant within the considered size range, measuring only 1 mm per side is by far the most challenging task. The low expected receive power, combined with the low antenna impedance and Q, leading to low input voltages, as well as the high optimum frequency, provides slightly less than 6 μW of DC power, not accounting for matching and DC-to-DC converter losses (see table 3.3). Factoring in another 10% loss due to the limited Q of the input capacitor of the circuit, as well as 10 to 20% of loss due to the DC-to-DC conversion, leaves only about 4.5 μW. In case the DC-to-DC converter is implemented by a linear regulator, the power consumption of the auxiliary circuitry, such as operational amplifier and reference voltage generation, needs to be subtracted as well, reducing the power available to the implant to perform signal acquisition and data transmission to around 4 μWor even less. This is already below the lowest power consumption of a neural signal acquisition front-end reported to date [Muller11]. While some of these numbers are based on rather high-level analysis, they indicate the difficulty of building a useful 1 mm by 1 mm neural implant powered wirelessly without violating any health concerns.

This chapter describes the implementation of a fully implanted cubic-millimeter wirelessly powered neural transponder exploring the limits on how much excess DC power can be provided to such a small implant while providing wireless connectivity [Mark11b]. In order to maximize the available DC power, careful link and system level optimizations were carried out, aggressive low-power circuit techniques and implementations were applied, and an optimized co-design between the power delivery block and the data transmitter was conducted. It describes each of these aspects as far as the power delivery is concerned, but only touches on the data transmitter to explain design choices where necessary. The data transmitter uses a passive reflective communication scheme to achieve very low power consumption and was designed by Yuhui Chen. It is described in detail elsewhere [Chen11].

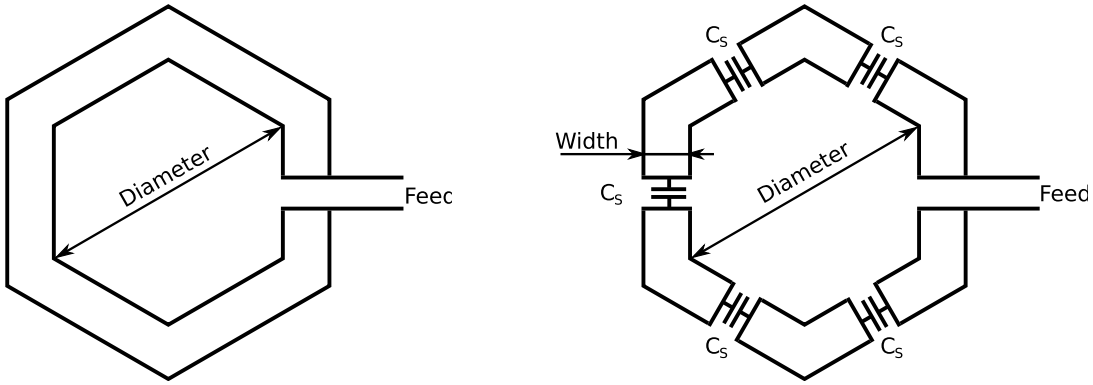


Figure 4.1: Illustration of conventional loop (left) and segmented loop antenna (right)

The first part of this chapter summarizes the various aspects of the link optimization and performance such as design of the external and internal antennas, including a novel approach of designing the external transmit antenna while minimizing the volume averaged SAR it is causing. Section 4.2 deals with the system level design and describes a method to overcome the low AC-to-DC efficiency for small AC voltages. It is followed by a detailed description of the implementation. Measurement results from both, in-air as well as in-animal system tests, are presented and discussed in section 4.4, before a short summary concludes this chapter.

4.1 Link Optimization

Finding the right antenna geometries and frequency of operation to optimize the link for a given application is a somewhat iterative process. Therefore, the first two sub-sections of this section describe the principal approaches used to optimized the external as well as the internal antenna only, while the final optimized link performance is summarized in the last sub-section.

4.1.1 External Antenna

As shown in section 2.2, for a given implant antenna, an optimum external antenna size exists that, if operated at the right frequency, minimizes the overall link loss. Besides link loss, the limitation on the maximum transmit power imposed by regulations to avoid adverse health effects due to the electromagnetic radiation, is the second main factor limiting the power available to the implant. It turns out that an external antenna sized for minimum link loss might in fact severely limit the maximum allowed transmit power and hence the power available to the implant. The following section describes this effect in detail and introduces segmented loop antennas (fig. 4.1) as an approach to mitigate this problem [Mark11a].

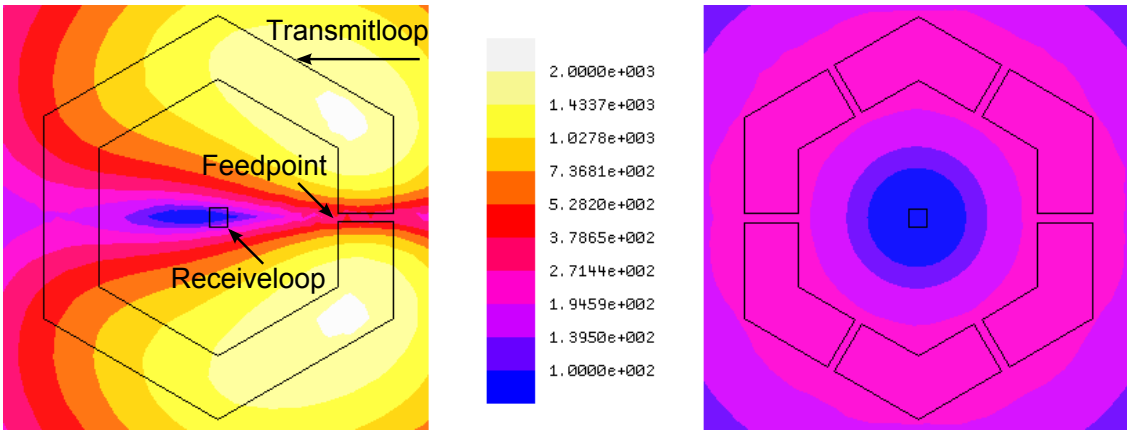


Figure 4.2: E-field distribution in V/m at skin surface for conventional loop (left) and segmented loop antenna (right) for 100 mW input power

In order to maximize the coupling between the antennas, the external antenna has to be significantly larger than the implanted one. For purely inductively coupled coils the optimum diameter of the external coil would be on the order of $2\times\sqrt{2}$ times the distance between the coils, assuming the distance is significantly larger than the radius of the internal coil [Pichorim04]. Although this only holds for electrically small loops, it provides a first order estimate for the optimum size of the transmit antenna. For the given application, with an antenna separation of more than 10 mm and an expected optimum frequency of more than 100 MHz, the perimeter of the optimum transmit coil approaches the effective wavelength λ of the signal and the antenna can no longer be considered electrically small. As a result of this, the current distribution within the loop becomes non-uniform [Cole03], leading to a non-uniform distribution of the E-field parallel to the plane of the loop. The loop starts radiating along its axis. The left part of fig. 4.2 shows the E-field distribution at 400 MHz for a hexagonal loop antenna with a diameter of 15 mm at the surface of the skin. The antenna consists of a 3 mm wide copper trace on a 62 mil thick FR-4 board. These dimensions are the results of a simulation based optimization and are equivalent to the ones used in chapter 2. Even for this loop size, the non-uniform E-field distribution is significant, leading to hotspots close to the feedpoint of the antenna. Since the SAR is directly proportional to $|E|^2$(see equ. 2.3), the SAR averaged over 1 g of tissue peaks exactly around these areas and is limiting the maximum allowable transmit power.

Cole et al. proposed segmenting electrically large coils and inserting capacitors to keep the current distribution along the loop uniform [Cole03]. Fig. 4.1 outlines this approach graphically. The role of the capacitors is to compensate the phase shift along the loop due to its dimension. As a rule of thumb, at the signal frequency each capacitor C_S needs to resonate out the inductance of the closed loop divided by the number of segments, in order to achieve a uniform current distribution along the entire loop. Additionally, each segment must be much shorter than the effective wavelength. Fig. 4.2 compares the E-field distribution

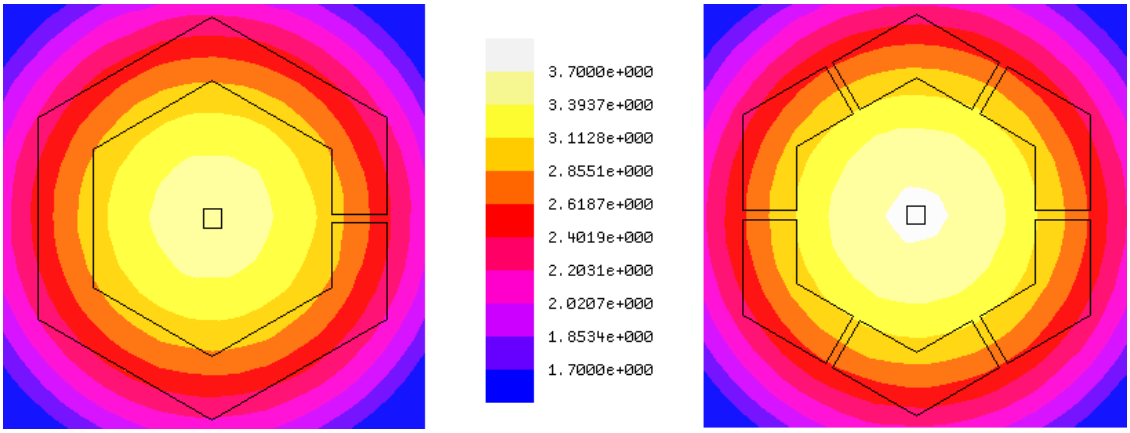


Figure 4.3: H-field distribution in A/m at receiver location for conventional loop (left) and segmented loop antenna (right) for 100 mW input power

at the surface of the skin caused by a conventional loop (left) to the one caused by the same loop, but now split up in 6 segments each connected by a 36.9 pF capacitor (right). As shown in fig. 4.2, segmenting the loop leads to a more uniform E-field distribution and reduces the peak E-field. As a result of this, the maximum SAR averaged over 1 g of tissue is reduced by 30%, allowing the transmit power to be increased by 30% without violating the SAR limitations.

Segmented loop antennas have the potential to not only reduce the electric field, but also to increase the magnetic near field, and therefore the coupling between the antenna pair. Dobkin et al. use segmentation to increase the magnetic field along the axis of the loop and therefore the read range of near-field UHF RFID antennas [Dobkin07]. Fig. 4.3 shows the H-field distribution at the position of the implanted antenna for the antennas used in Fig. 4.2. For these antennas, the shape of the magnetic field distribution does not change significantly, but the value of the H-field increases by approximately 5.7% when segmenting the loop. Comparing the link loss of two links using the two different external antennas described above, the MAG is increased by 10% when using the segmented antenna, which matches well with the observed increase of the H-field at the receiver location. Using a segmented instead of a conventional loop antenna therefore not only allows a higher transmit power, but also potentially increases the coupling between the antenna pair.

In order to investigate the effect of segmentation on the optimum external antenna size and frequency of operation, the same setup as used to arrive at fig. 2.1 was used. This time the external antennas were segmented into six segments. At each frequency point the segmentation capacitor was adapted according to the inductance per segment method outlined above. Figure 4.4 compares the results for the different antenna sizes and types. It indicates that segmenting the external loop slightly increases the optimum frequency, but has only little impact on the optimum antenna diameter. Also shown in fig. 4.4 is how segmentation increases the coupling, especially for electrically larger antennas.

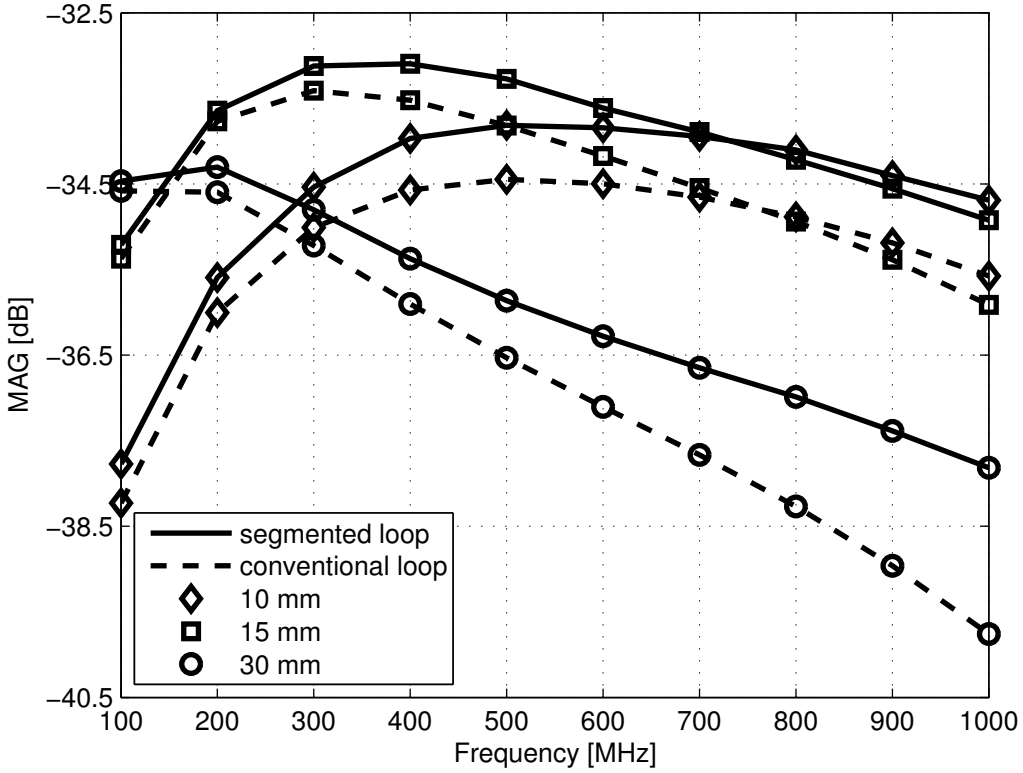


Figure 4.4: Maximum achievable gain vs. frequency for different antennas

The trade-offs between link loss and received power due to operating at lower frequencies, using larger external antennas or moving them further away from skin as described in section 2.4 are, in principle, not altered by using segmented instead of conventional loop antennas [Mark11a].

In summary, segmenting the external loop potentially reduces the SAR by 30% and the link loss by 10% when operating at 400 MHz and coupling to a single turn 1 mm by 1 mm coil. This gives a theoretical increase in power available to the implant of 43%.

It is important to mention that the increase in allowed transmit power due to the use of segmented loops is primarily due to the reduction of the peaking of the E-fields in a small area. Hence the amount by which the power can be increased is larger for SAR limitations based on smaller averaging volumes, such as the one imposed by the FCC, which mandates to average over 1 g of tissue. When bounded to regulations using a larger averaging volume, such as the one recommended by the IEEE and used, for example, in Europe averaging over 10 g of tissue, the possible improvements achievable by segmented loops are much lower. Since segmented loop antennas only improve on the limits imposed on the externally applied power, using them when powering larger implants (e.g. 4 mm by 4 mm) does not necessarily

increase the DC power available to the implant since the power consumption is limited by thermal constraints (fig. 2.8).

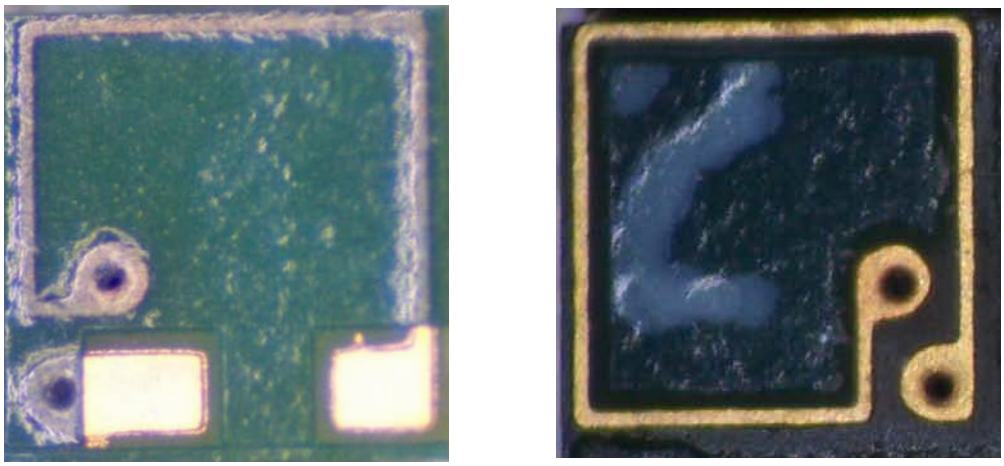
4.1.2 Implanted Antenna

Since the main objective of the external transmit antenna was to produce a large magnetic near field while keeping the electric near field low, the implant antenna should be sensitive to the magnetic rather than the electric near field as well. The obvious choice for the implanted antenna is therefore again a loop structure.

In order to increase the coupling, the loop should maximize the coupling area (area enclosed by the loop) while minimizing the ohmic losses of the loop. Using multiple turns increases the loop's inductance and potentially its Q as well. As a direct result of this, the equivalent impedance of the tank formed by the antenna and the capacitance at the input of the transponder increases, leading to larger input voltages at a fixed input power, which in turn can lead to a more efficient AC-to-DC conversion. At the same time the increased inductance reduces the size of the capacitor needed to resonate out the antenna at the frequency of operation, potentially allowing savings in chip area or operating at a lower frequency.

Due to the low thickness of the metalization of standard CMOS processes and the losses introduced by the silicon substrate, the Q of on-chip inductors at frequencies below 1 GHz is rather low, typically being somewhere in the range of 5. This not only introduces significant loss in the implanted antenna, but also limits the maximum tank impedance and therefore the input voltage of the circuit. To overcome this problem, an off-chip antenna built using micro-PCB technologies with minimum feature sizes of 2 mil (approx. 51 μm) was used. Doing so enabled the use of a significantly thicker metal (approx. 36 μm) to form the loop, leading to a much higher inductor Q. The fact that the loop is now further removed from the lossy substrate increases the Q as well. Going off-chip with the loop does come at a price in the form of a more complex interconnect between the antenna and the circuit. In order to keep the additional losses due to the interconnect low, as well as to stay within the targeted 1 mm by 1 mm, the antenna was flip-chip assembled to the CMOS chip.

Although the minimum feature size of the micro-PCB technology is only around 2 mil, the minimum via size in this technology is limited to more than 8 mil (200 μm). Together with the fact that the vias are through-hole vias, the number of turns achievable without reducing the coupling area is therefore severely limited by the vias. Using blind vias would allow to increase the number of turns by using a board with more layers, but for economical reasons a two-layer board with through whole vias was chosen. Fig. 4.5 shows the top and the bottom layer of the implemented antenna. In the final system the layer shown in fig. 4.5 (a) is facing the chip. The light rectangles seen in the photo are the exposed pads which will be connected to the CMOS chip using a gold stud flip-chip assembly technique using conductive epoxy. Due to the experimental nature of the entire project the assembly process was a manual one, and thus the pad spacing was limited to a minimum of 600 μm. The overall number of turns



(a) (b)

Figure 4.5: 2-layer implanted loop antenna: layer facing CMOS chip (a) and top layer (b)

was chosen to be 2, to avoid reducing the coupling area too much, while keeping losses due to proximity effects low. Standard FR4 material was used as the substrate with a finished thickness of 17 mil, leading to an overall antenna thickness of less than 0.5 mm.

The final trace width of the antennas turned out to be somewhere between 1.3 and 1.6 mil instead of the nominal 2 mil, due to process variations. Fig. 4.6 shows the measured and simulated antenna impedance between 400 and 600 MHz in air, after the simulation model was adjusted to account for the narrower trace width observed. Both the reactance as well as the resistance match very closely over the observed frequency range. An inductance of approximately 5.73 nH with a Q of more than 30 at 500 MHz was achieved.

It is worth mentioning that, while the antenna was designed keeping the heuristic optimization rules mentioned above (maximize coupling area, number of turns & Q etc.) in mind, no exhaustive numerical optimization was carried out to find the globally optimal antenna. Doing so could potentially improve the overall performance, but it is believed that given the tight constraints in area and technology, these improvements would be limited.

4.1.3 Total Link Performance

In this section the total link using a segmented external loop with a diameter of 15 mm, as described in section 4.1.1, and the 2-layer micro-PCB antenna described in section 4.1.2 is investigated. The main focus is on quantifying the expected performance as well as non-ideal effects such as the use of lossy capacitors in the segmented loop and the presence of a CMOS chip next to the implanted antenna. While the model used for the human head still consisted of 2 mm of skin, 2 mm of fat, and 7 mm of bone, the distance between the external antenna and the skin was reduced from 5 mm to 3 mm compared to all of the previously simulated

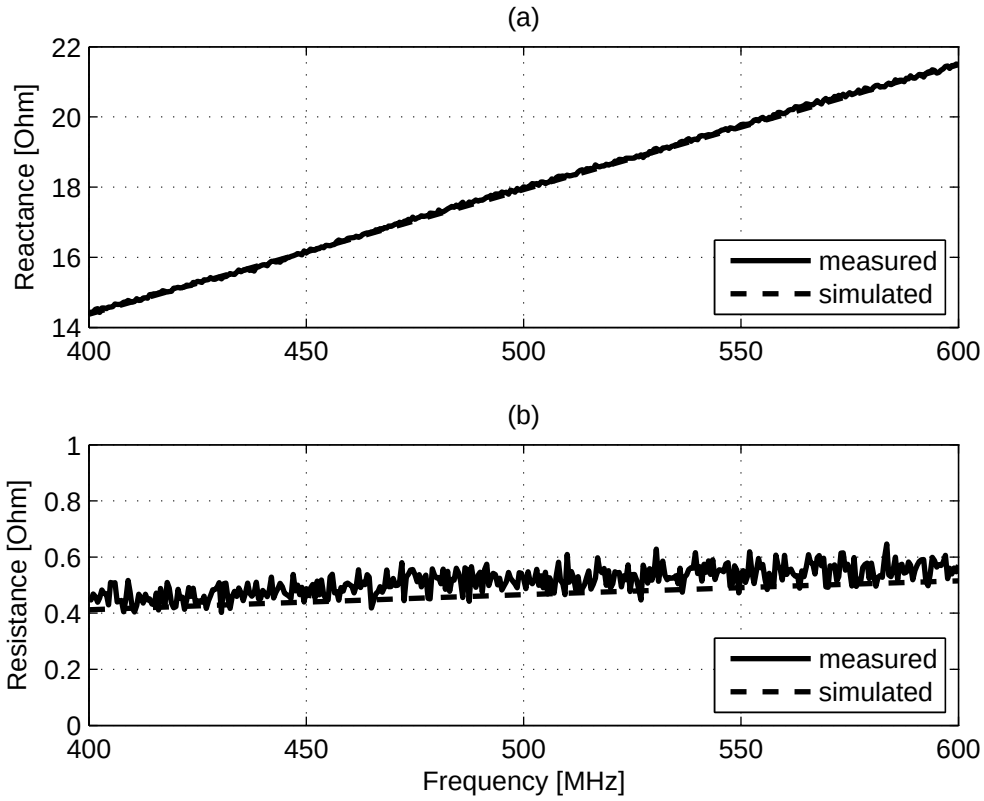


Figure 4.6: Simulated and measured reactance (a) and resistance (b) of 1 mm by 1 mm implanted antenna (in air)

cases. This was done to reduce the overall channel loss, in order to improve the link budget for the data link. Doing so does reduce the maximum allowed externally applied power, however, as discussed in section 2.4.

First, the optimum frequency of operation and the effect of segmenting the external loop is revisited. Figure 4.7 shows the link loss over frequency using a conventional and a segmented external loop with ideal segmentation capacitors. Consistent with the behavior reported in section 4.1.1, segmenting the loop increases the coupling, especially at higher frequencies, although only marginally. Compared to fig. 4.4, the optimum frequency is at a slightly lower frequency, which can be explained by to the use of a multi-turn implanted antenna as opposed to the simple single turn loop assumed in section 4.1.1.

Next, the effect of using real, lossy capacitors to segment the external loop is investigated. In order to keep the losses introduced by the capacitors low, multi-layer, high Q, SMT capacitors with a Q between 60 and 1000 within the frequency range of interest [JohansonTech08] were used. Despite the fairly high Q of the 0603/R14S capacitors, they introduce an extra loss of up to 1.7 dB, as shown in fig. 4.8. They also slightly shift up the optimum frequency.

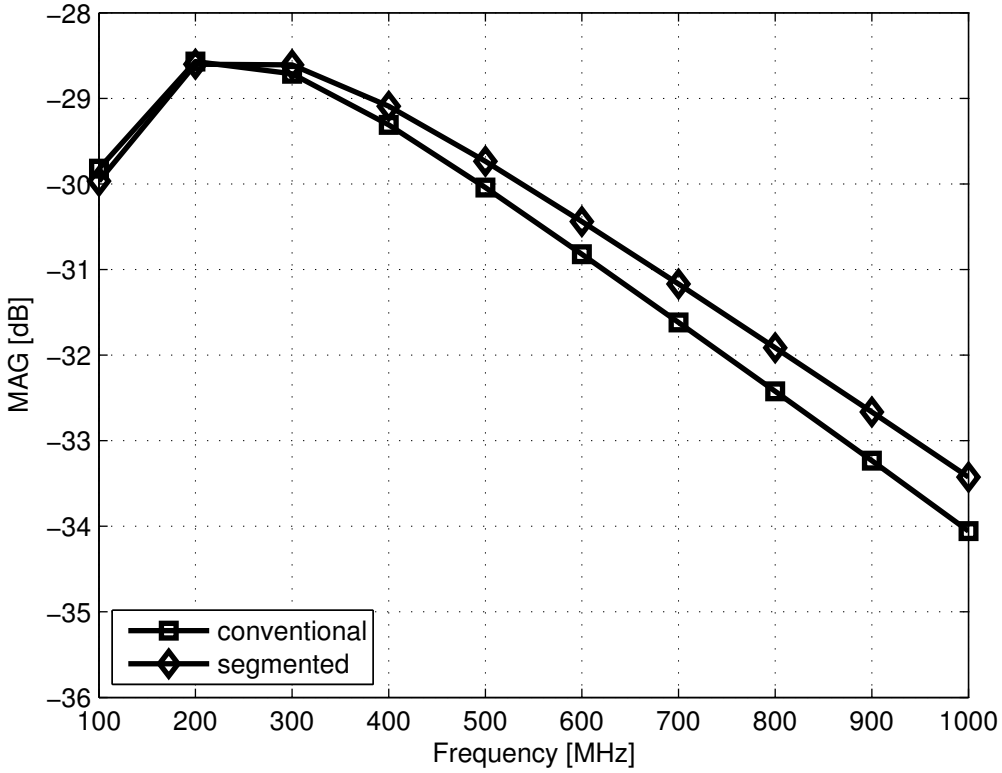


Figure 4.7: MAG over frequency for conventional and segmented loop (ideal segmentation capacitors)

Accounting for the losses due to the segmentation capacitors and looking purely at the link loss, using segmented loop antennas does not seem to be such a good idea after all, since it increases the minimum link loss by about 1.5 dB. However, since the extra loss is due to power lost in the external antenna before the signal is actually leaving it, the lost power can be compensated for by increasing the power going into the antenna without violating SAR limitations. Purely from a received power point of view, the losses in the segmentation capacitors basically do not impact the overall performance of systems utilizing segmented external loops, as shown in table 4.1.

Although the results shown in fig. 4.8 suggest an optimum frequency of approximately 300 MHz to minimize the link loss, 500 MHz was chosen as frequency of operation for the actual implementation. A number of reasons led to this choice of frequency, with the preliminary antenna design of the implant antenna at the time of the chip tape-out pointing to a slightly higher optimum frequency than the one shown above being the most significant one. Other reasons for choosing a higher frequencies included a significantly smaller on-chip capacitor needed to resonate out the antenna and a higher tank impedance at resonance. The last factor increases the input voltage and makes it easier to modulate the reflection of

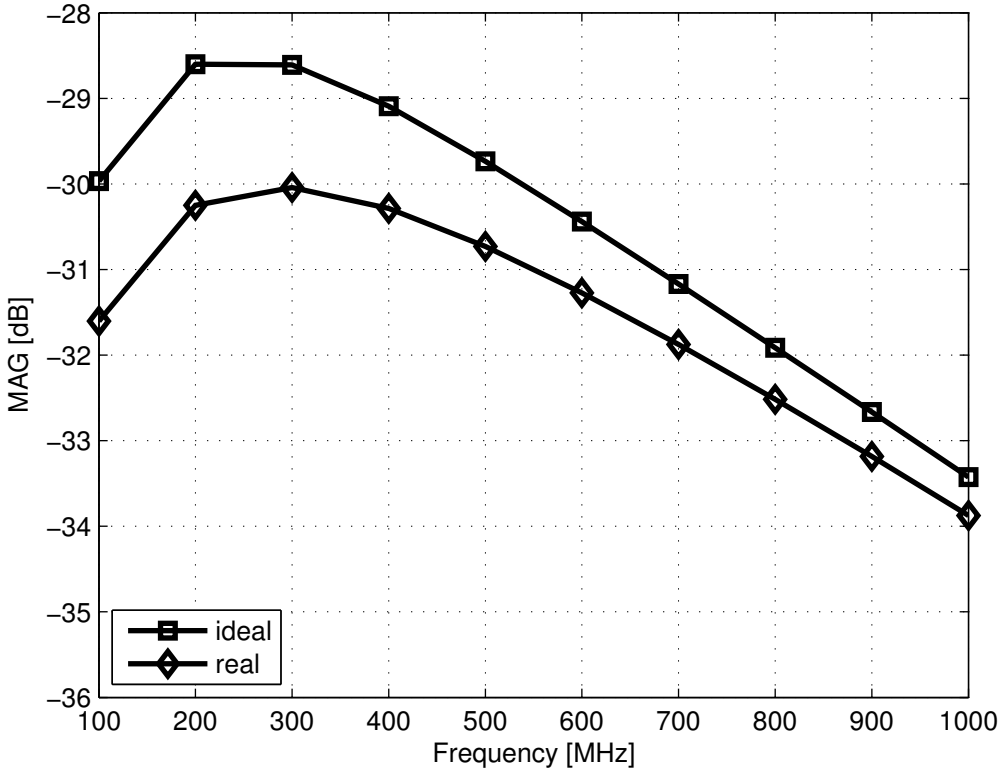


Figure 4.8: MAG over frequency for segmented loop with ideal and real segmentation capacitors

SAR Standard	External Loop Type	P_{TX}[mW]	MAG [dB]	$P_{RX}[\mu W]$
1.6 W/kg over 1 g	conventional	31.6	-30.04	31.3
	segmented (ideal)	44.2	-29.74	46.9
	segmented (real)	54.2	-30.73	45.8
2 W/kg over 10 g	conventional	118.2	-30.04	117.1
	segmented (ideal)	118.7	-29.74	126
	segmented (real)	150.7	-30.73	127.3

Table 4.1: Comparison between different external loop scenarios (at 500 MHz)

the incoming signal when using passive data transmission schemes, such as the one used in the transmitter of the implemented transponder [Mark11b]. Due to the channel loss being rather flat around the optimum frequency, operating at 500 MHz instead of 300 MHz decreases the overall efficiency by only approximately 0.7 dB and is therefore an acceptable trade-off.

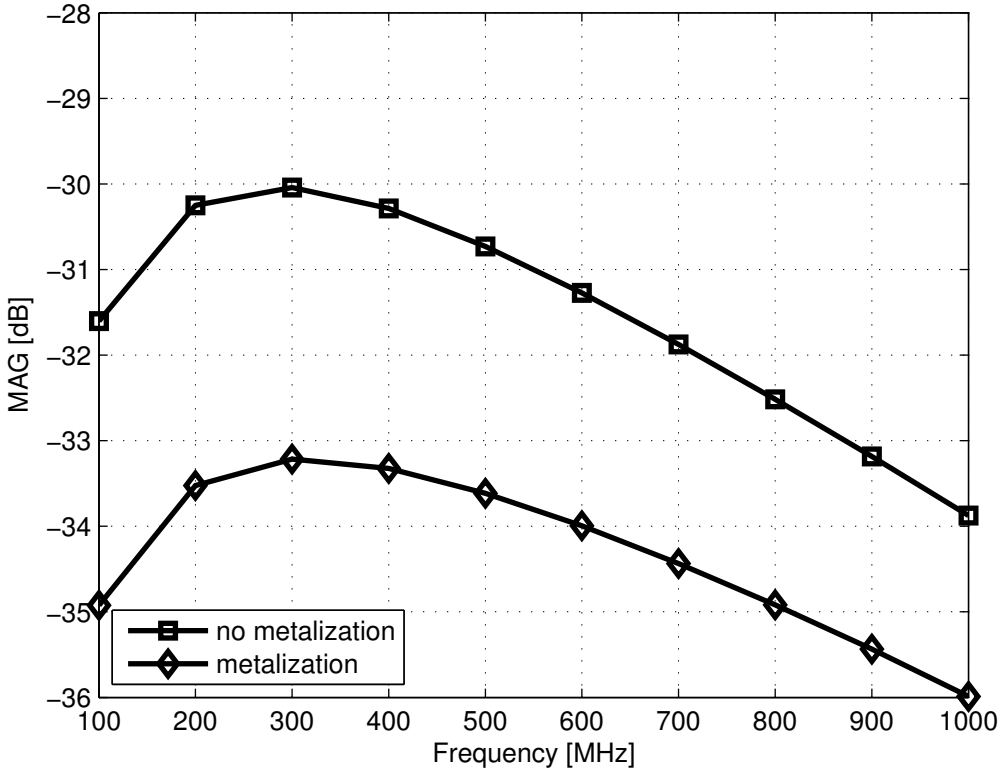


Figure 4.9: Effect of chip metalization on MAG over frequency

Table 4.1 summarizes the power transfer performance for different external loop structures operating at the two SAR restrictions imposed by the FCC and IEEE respectively. It shows the benefits of using segmented loops as far as power received by the implant is concerned. Additionally, it shows that the losses introduced by the segmentation capacitors do not affect the received power. As mentioned in section 4.1.1, it also shows the reduced benefit of using segmented loops when constrained by SAR values that use larger averaging volumes such as the 2 W/kg over 10 g of tissue recommended by the IEEE. Overall, the received power can be increased by more than 45% compared to a conventional external loop by using segmentation when limited by the 1.6 W/kg over 1 g of tissue SAR constraint. The more stringent SAR limitation of 1.6 W/kg average over 1 g of tissue was also chosen as the basis for the remainder of this work.

Figures 4.7 and 4.8 were obtained by simulations, with the implant micro-PCB antenna being placed on top of a cuboid made of pure silicon covered by SiO_2 mimicking the CMOS chip. In reality though, the CMOS chip also contains a significant amount of metal due to routing and fill structures, which are likely to introduce substantial additional loss, primarily due to image currents flowing in the metalization disturbing the inductor's magnetic field [Yue98]. Due to the complexity of modeling the exact metalization of the CMOS chip, a

worst-case scenario with the entire metalization being represented by a solid copper plane was simulated. The difference in link loss between the cases with and without metalization are shown in fig. 4.9. It shows that the additional loss due to the metalization can be larger than 3 dB. Taking this into account, the **power available** at the matched input terminal of the implant at 500 MHz can therefore be anywhere **between 46 and 23.6** μW. Due to the implanted antenna impedance changing from 0.74 + j 18.37 Ω without metalization to 0.71 + j 15.83 Ω with full metalization, the **expected peak input voltage** of the AC-to-DC converter is somewhere **between 205 and 130 mV**.

4.2 System Optimization

In order to be on the safe side, the system was designed based on the worst case link scenario where the effect of the chip metalization is close to the one predicted for the solid metal plane. With an input power of 23.6 μW, assuming a loss due to the finite Q of the on-chip capacitor resonating out the inductance of the antenna of 10%, a maximum rectifier efficiency of 65% (assuming a self-driven synchronous rectifier) and a loss of a bit less than 20% due to the the linear regulator, regulating an average DC voltage of 0.6 V down to a stable 0.5 V required for the transmitter, the expected regulated DC output power is approximately 11 μW.

However, due to the amplitude of the input voltage being only 130 mV, the efficiency of the rectifier based on fig. 3.21 is expected to be less than 45 %, reducing the expected regulated output voltage by more than 30%, leaving only approximately 7.5 μW for the entire electronics of the implant. On top of that 9 stages of rectification would be needed to achieve a high enough output voltage.

The only way to increase the AC-to-DC efficiency to its maximum around 65% is to increase the input voltage. After optimizing the link and increasing the equivalent resistance of the input tank at resonance, which was done by using a 2-turn micro-PCB loop and using high Q on-chip MOM capacitors to resonate out the loop inductance, increasing the transmit power is the only other way to do so. Since the maximum transmit power is limited by the maximum SAR, it is important to understand where the SAR limitations come from to see if there is anything that can be done to, at least temporarily, increase the transmit power. The SAR constraint is based on thermal considerations and derived from an upper limit on the increase of the temperature of tissue when exposed to electromagnetic fields [IEEE06]. However, in order to reach the underlying increase in tissue temperature, the field causing the stated SAR needs to be applied continuously. It seems therefore feasible to temporarily exceed the transmit power associated with the maximum SAR, as long as there is enough time provided for the tissue to cool down or the heat to diffuse before the next high-powered pulse hits the tissue. This hypothesis is supported by the fact that the IEEE specifies time averaged values for their maximum exposure limitations on E- and H-fields as well as power-densities derived from the basic SAR constraint in their recommendations regarding the exposure of humans to RF electromagnetic fields [IEEE06]. Duty-cycling the power signal

leads to an increase in instantaneous received power and therefore voltage without increasing the tissue heating beyond what is considered safe.

Exact thermal simulations of the field - tissue interactions under duty-cycled operation are required to determine the exact extent of duty cycling that can be applied without increasing the tissue temperature too much. Due to the complexity of this problem, doing so was beyond the scope of this work. Instead, the time-averaged transmitted power was limited to be equal to the continues power leading to the maximum SAR while ensuring that the maximum instantaneous transmitted power stayed below the maximum peak values allowed by the IEEE [IEEE06]. While this might not lead to exactly the same temperature increase, it is well suited to prove the concept and build a system that exploits the higher instantaneous input signal. Depending on the exact timing of the duty-cycled power signal, the time-averaged power could actually be even higher than the one used here, without increasing the tissue temperature beyond what is considered safe.

In the case of the 1 mm by 1 mm system, a voltage of approximately 300 mV is needed for the self-driven synchronous rectifier to operate at its peak efficiency (fig. 3.21). This can be achieved by increasing the transmit power temporarily by a factor of approximately 5. In order to not exceed the maximum average transmit power constraint this would require an on-to-off ratio of the power signal of 1 : 4. During the on-phase the implanted system can then more efficiently convert the incoming power to DC and store it on an on-chip energy storage device to allow the implant to continue operating during the off-time. Due to the increased instantaneous input voltage, the size of the transistors in the rectifier can be significantly reduced, allowing to reduce the size of the coupling capacitors C_C substantially without degrading the conversion efficiency. Doing so leaves enough space for an on-chip storage capacitor to power the device during the off-time.

In a real system the minimum on-time is limited by the time constant of the resonant tank formed by the antenna and the input of the chip. Its Q factor limits how fast the voltage across the input can build up. With a Q of approximately 20 and a frequency of 500 MHz, it takes the input voltage approximately 40 ns to reach its final amplitude. Limiting the power loss associated with this transient behavior to less than 10% puts a lower limit on the on-time of approximately 400 ns, requiring at least 1.6 μs of power down phase to allow the tissue to cool down.

At the same time, the off-phase is upper limited by the amount of ripple that can be tolerated on the unregulated DC voltage. Assuming capacitors as energy storage during the off-time, the voltage ripple is given by

$$\Delta V = \frac{I_L \times t_{off}}{C_{stor}} \tag{4.1}$$

where I_L is the average load current, t_{off} is the off-time of the power signal, and C_{stor} is the size of the storage capacitor.

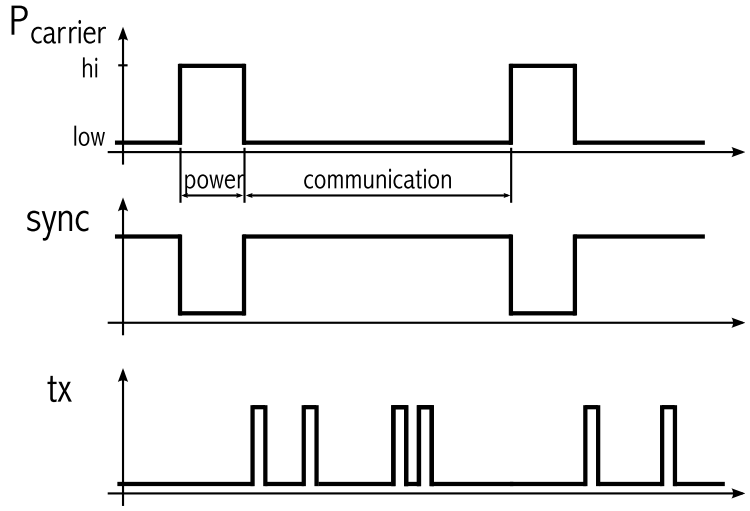


Figure 4.10: Timing diagram for the 1mm^3 transponder

The maximum ripple, together with the maximum amount of storage capacitor that can be integrated on the system and the average load current therefore determines the maximum off-time.

Due to the data transmitter being based on a reflective scheme that changes the input impedance of the tag to modulate the reflection of the incoming signal, the externally applied transmit signal cannot be turned off completely during the off-time. It therefore makes more sense to talk about a power and communication interval (t_{power} and t_{comm}, respectively) instead of on- and off-times of the external signal. Since the power transmitted during the communication phase contributes to the average transmitted power and therefore requires the power during the power phase to be reduced accordingly in order to remain compliant with the SAR constraint, it should be as low as possible, just high enough for the communication link to work.

From an implant point of view, the overall average excess DC power is therefore a function of the power interval, transient losses due to the Q of the resonant tank, the constant power overhead (references, auxiliary amplifiers, etc.), and the power required during the communication interval.

Figure 4.10 shows the actual timing diagram of the system, with $P_{carrier}$ representing the amplitude of the externally applied signal, *sync* being a signal indicating the communication phase, and *tx* being the signal controlling the input impedance modulation of the transponder.

The target data rate for the transponder was 2 Mbps. With the reflective impulse radio transmitting 6 bits of information during each communication phase [Chen11], the sum of power and communication period is limited to 3 μs. This leads to a t_{power} of 600 ns and a t_{comm} of 2.4 μs to achieve the 1 : 4 ratio needed to boost up the instantaneous input voltage

to approximately 300 mV. Transmitting 24.15 dB during t_{power} and 4.15 dB during t_{comm} theoretically leaves sufficient SNR for the data signal at the external receiver [Chen11], while providing an implant input voltage amplitude of more than 280 mV during the power phase. At the same time, it reduces the average power received by the implant during the power phase by less than 5 %. This reduction in received convertible power can be seen as extra power consumption by the transmitter, since it is due to the external signal present during the communication phase for the transmitter to work.

4.3 Implant Implementation

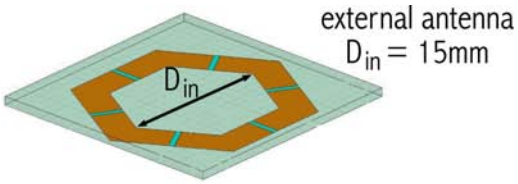
4.3.1 System

Figure 4.11 shows the diagram of the overall system. The external antenna is a 15 mm hexagonal segmented loop antenna with 24 pF segmentation capacitors as described in section 4.1 and placed 3 mm away from the skin of the head. Inside the head, separated by 2 mm of skin, 2 mm of fat and 7 mm of bone, directly on top of the brain, sits the implanted transponder. It consists of the antenna described in section 4.1.2 and a CMOS chip flip-chip mounted to it. The overall footprint of the tag is limited by the antenna's dimension which is 1.1 mm by 1.1 mm, with 0.05 mm on each side being attributed to the required board overlap for dicing. This means that the active area is only 1 mm by 1 mm. The height of the entire transponder is less than 0.8 mm, leading to a total volume of less than 1 mm^3.

The chip itself interfaces to the antenna with a 15 pF, high Q, MOM capacitor to resonate out the inductance of the antenna, and a CMOS switch in parallel to modulate the transponder's input impedance during data communication. An AC-to-DC converter converts the incoming signal to approximately 0.6 V DC during the power phase and stores the energy on C_{stor}. The size of the storage capacitor C_{stor} and the average current drawn determines the large signal ripple and can be calculated based on equ. 4.1. While the system was designed to tolerate a ripple as large as 100 mV, which would have required a C_{stor} of approximately 530 pF assuming a maximum output current of 22 μA, 1 nF of storage capacitor was included on the chip to be able to test a range of communication intervals. To save area, the storage capacitor was implemented using the standard MOS capacitor of the process.

Based on an on-chip generated reference voltage, a low-power linear regulator regulates the voltage across the storage capacitor down to a more stable 0.5 V DC voltage used to supply the chip. The requirements on the supply voltage are based on the needs of the transmitter, leading to a required accuracy of ±10% and a ripple of less than 10 mV.

The synchronizer monitors the input amplitude and detects whether the system is in the power or the communication phase. When transitioning from power to communication phase, it turns off the rectifier and triggers the transmitter. Similarly, it turns on the rectifier as soon as it detects a power signal at the input. The fact that the rectifier gets turned off during the communication phase, changing its input resistance from matched to high impedance, helps



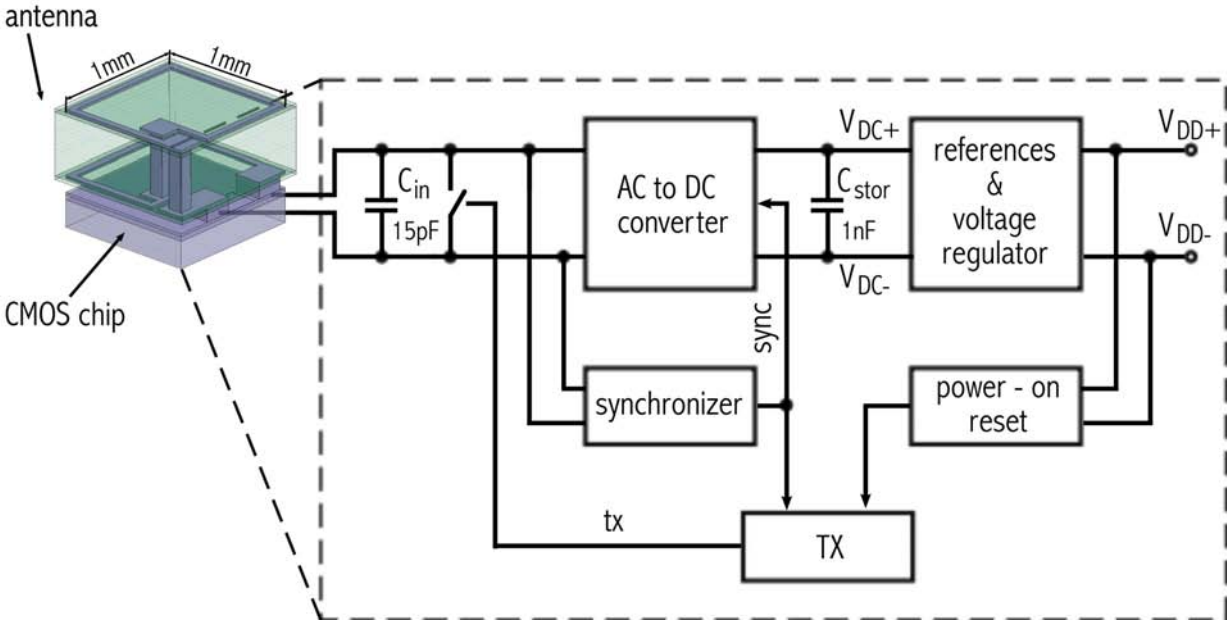


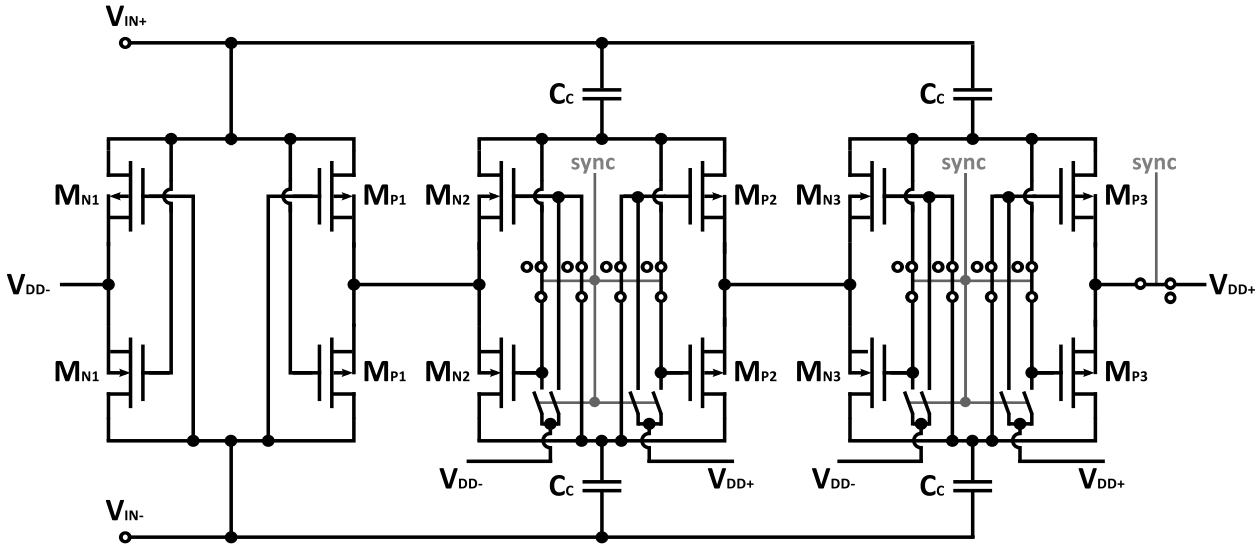
Figure 4.11: System diagram of 1mm^3 transponder

to increase the modulation depth compared to conventional backscattered schemes, This is due to the impedance seen by the antenna being modulated between "open" and "short", as opposed to "matched" and "short" [Chen11].

In order to make sure the transmitter gets initialized correctly during start-up, a power-on reset building block issues a reset signal to the transmitter once a sufficiently high supply voltage is achieved. This reset signal resets the logic in the transmitter to a defined state.

The transmitter is based on a self-terminated delay line and optimized for low power operation. It contains an on-chip shift register generating a pre-defined bit sequence for testing purposes, which would eventually be replaced by the digital output of the sensor acquisition front-end [Chen11].

Since the entire system generates its own power supply, making sure that it reliably starts up during the initial power-on phase is crucial. Architectures guaranteeing reliable start-up had to be chosen, and transient start-up simulation of every single building block, as well as



Device Name	M_{N1}	M_{P1}	M_{N2}, M_{N3}	M_{P2}, M_{P3}
W / L [μm]	35×1.2/ 0.09	95 × 1.4 / 0.09	47×1/ 0.09	127 ×1.2/ 0.09

Figure 4.12: AC-to-DC converter schematic

the complete system were performed to make sure the system does power up correctly.

Except for the transmitter, the circuits of all the building blocks will be described in detail in the following sections.

4.3.2 AC-to-DC Converter

The AC-to-DC converter is a standard 3 – stage self-driven synchronous rectifier without inter-stage gate control. It was designed using the method described in section 3.4.2 to match to the resonant impedance of the input tank under maximum load conditions. Based on an input amplitude of 280 mV, it provides an output voltage of 0.6 V while supplying 100 μA (approximately (t_{power}+t_{comm})/t_{power} times the average current).

Fig. 4.12 shows the schematic of the implemented converter. Stages 2 and 3 are turned off during the communication phase and the storage capacitor is disconnected from the rectifier's output to increase the impedance the circuit presents to the resonant tank during that time. The switches connecting the gates of the transistors to the coupling capacitors C_C in stage 2 are implemented as complementary CMOS switches whereas the corresponding switches in the 3rd stage are PMOS only switches. They were designed to minimize their impact on the conversion efficiency when "on" while still preventing the main transistors from turning on during the "off"-mode. In both cases the switches connecting the gates of the main transistors to V_{DD-} and V_{DD+} when "off" are NMOS and PMOS only, respectively. The first stage is not switched, since it is hard to do so while still guaranteeing reliable start-up, and its effect

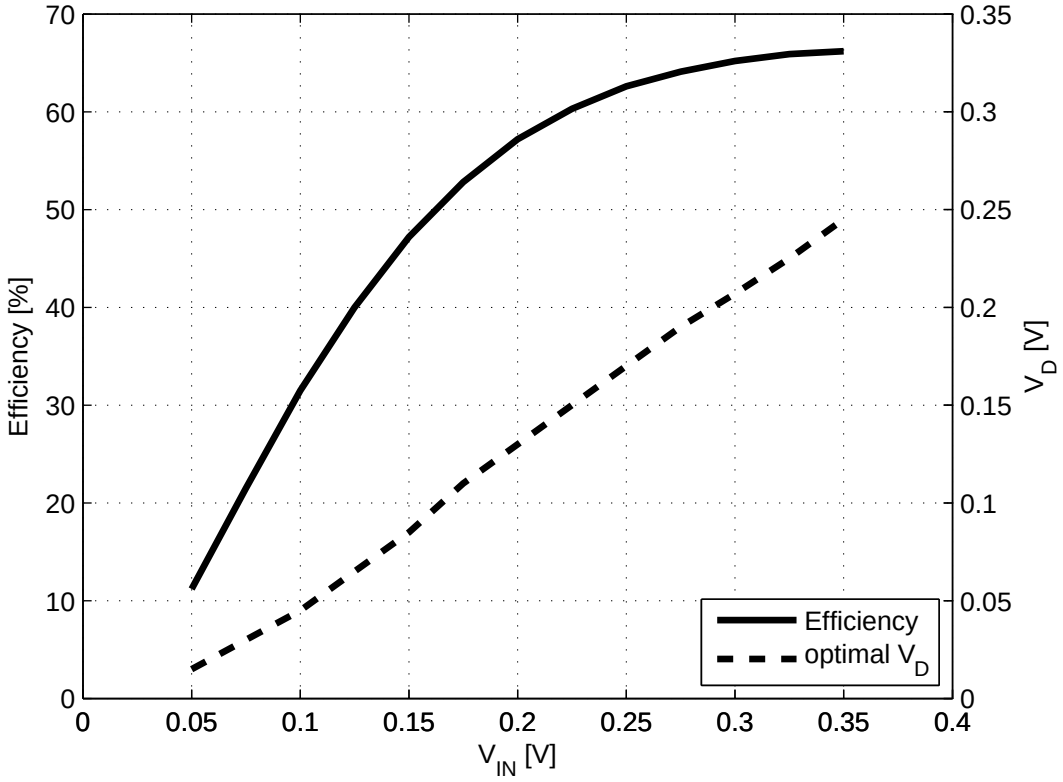


Figure 4.13: Simulated efficiency and optimal voltage increase per stage (V_D) for rectifier

on the overall input impedance is limited. Equipping the converter with such a switching capability does impact the conversion efficiency. In this design, the simulated efficiency for the in- and output specifications described above drops from 64.7% to 61.4%. However, being able to switch into a high resistance mode is crucial for the performance of the transmitter.

The coupling capacitors are 25 pF and implemented using MIM cap for its low parasitic bottom plate capacitance. All transistors are of the lowest threshold voltage flavor available in the process. Due to the reduced gate drive due to the gate-switches and the losses due to the capacitive voltage divider formed by C_C and the input capacitance of the stage, the transistors in the 2nd and 3rd stage are slightly larger than the ones in the first stage.

In fig. 4.13 the maximum achievable conversion efficiency of the implemented converter as well as the voltage gain per stage at which the maximum efficiency is achieved is plotted as a function of the peak input voltage amplitude. Due to the fact that different input voltage levels would require a different number of stages to provide 0.6 V at the output, and the switches would have to be adapted accordingly, the results shown in fig. 4.13 were obtained without any switches present. As a result of this, the shown efficiencies are slightly higher than what would be achievable for switched versions. However, the general trend still holds

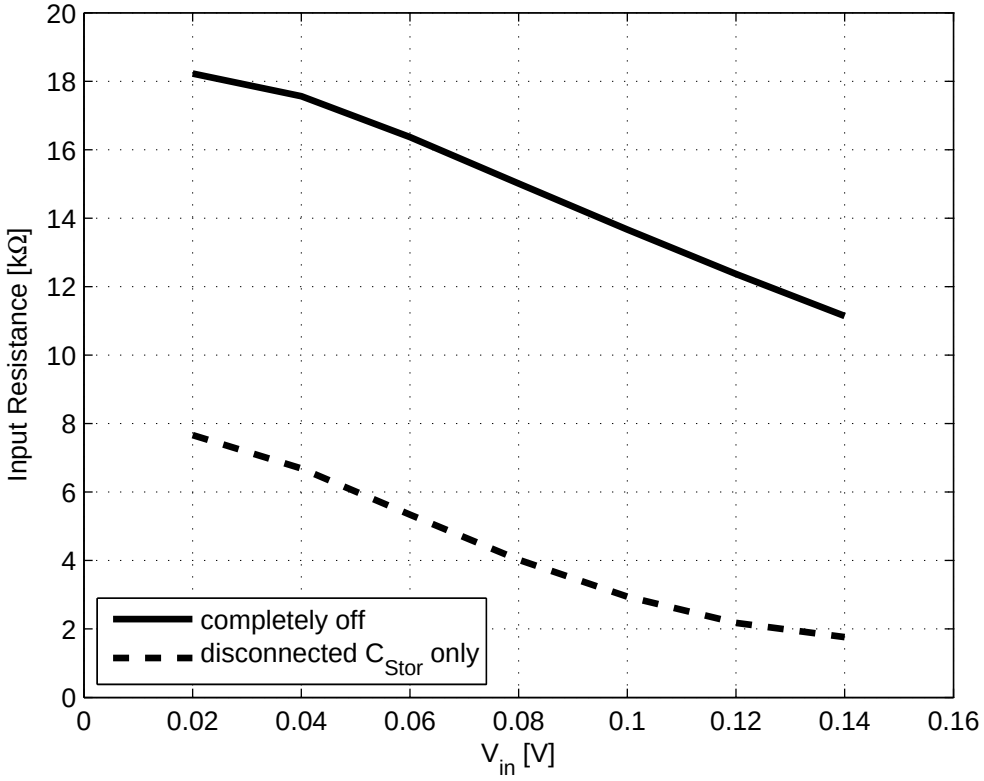


Figure 4.14: Off input resistance of rectifier for different switching schemes

and it shows how the conversion efficiency increases by approximately 60% by operating from 280 mV under duty-cycled operation as compared to 130 mV under continuous powering. At the same time it shows how the number of stages can be reduced from 9 to 3 due to the duty cycling.

Based on system level simulations of the data link, a transponder input resistance of at least 10 kΩ when turned off would be required for it to have no impact on the modulation depth during the communication phase. If the rectifier is not switched at all, charge from the storage capacitor and additional parasitic capacitors would leak back through to the input during the communication phase when the input voltage is significantly lower than during the power phase. This would severely interfere with the modulation of the input impedance performed by the transmitter. Just disconnecting the storage capacitor C_{stor} during the communication phase eliminates this problem almost completely. However, the input resistance stays still well below the required 10 kΩ. Additionally switching off stages 2 and 3 is therefore required to increase the resistance beyond 10 kΩ. Figure 4.14 shows the input resistance over the possible input voltage range during the communication phase. It clearly shows how completely switching the converter off (i.e. stage 2 and 3 as well as disconnecting C_{stor}) keeps the input impedance above 10 kΩ.

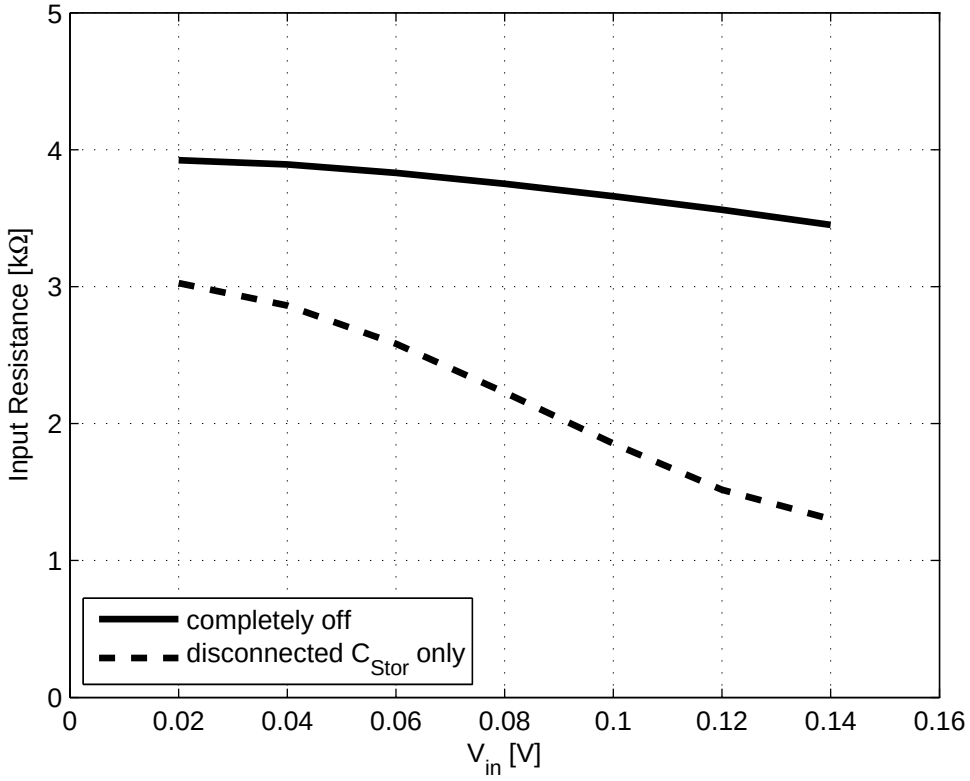


Figure 4.15: Equivalent chip input resistance at resonance for different switching schemes

It turns out that in reality, the tag input impedance is limited by the parasitic resistance of the input capacitors used to resonate with the antenna. Although the Q of the used MOM capacitor's is fairly high (simulated Q is approximately 240), the equivalent resistance at resonance of the capacitor is only about 5 kΩ, putting an upper limit on the maximum achievable input resistance during the communication phase. Figure 4.15 shows the equivalent input resistance of the tag during the communication phase at resonance, which consists of the 5 kΩ in parallel to the rectifier input resistance. The overall input resistance can now be as small as 3.5 kΩ even with stages 2 and 3 switched, leading to a reduced modulation depth. However, complete switching still improves the input resistance by up to a factor of 2.5 compared to the case where just the storage capacitor is disconnected from the rectifier's output.

In order to prevent circuit damage due to accidentally applied overvoltage, back-to-back diodes are connected across the input terminals and a forward biased high turn-on voltage diode is connected between the positive and the negative output terminals.

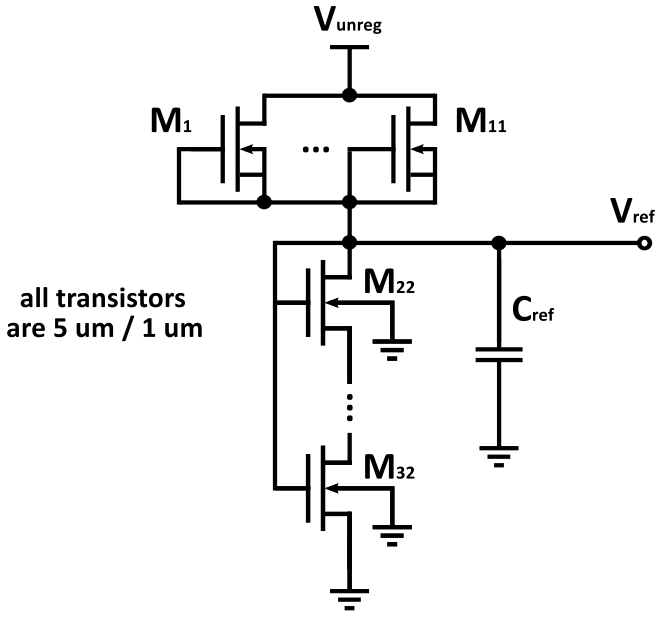


Figure 4.16: Schematic of voltage reference

4.3.3 Voltage Reference

Due to the duty-cycled powering approach and the subsequent ripple of the voltage across C_{stor}, additional voltage regulation is needed to provide a supply voltage with the required accuracy and stability. The base for any regulator is the reference voltage. Based on the low expected available power, low power consumption was the primary design goal. In the current design the main focus was to provide an accurate reference voltage over process. Temperature stability was not a major concern, since the ambient temperature inside the body is expected to stay fairly constant. Therefore there was no need to include a bandgap reference.

The expected range of unregulated DC voltage serving as the supply voltage of the reference was between 0.55 V and 0.8 V. The minimum of 0.55 V is necessary to leave enough headroom for the LDO, while the maximum of 0.8 V is guaranteed due to the on-chip over-voltage protection. Based on constraints on the transmitter the required accuracy of the regulated output voltage was 10%, requiring the reference to be more accurate than this. On top of that the maximum ripple had to stay below 10 mV.

To keep the power consumption low, a fairly simplistic threshold voltage based reference was implemented. Figure 4.16 shows the schematic of the implemented reference voltage generator. It consists of a long, diode-connected NMOS transistor, built out of 10 unit sized devices in series, and a wide NMOS transistor, based on 11 parallel transistor of the same unit size, on top of the diode connected one. The gate of the wide transistor is connected to its source to provide biasing for the diode connected one based on its leakage current. Low-threshold voltages transistors of the low-power process flavor were used. First-order

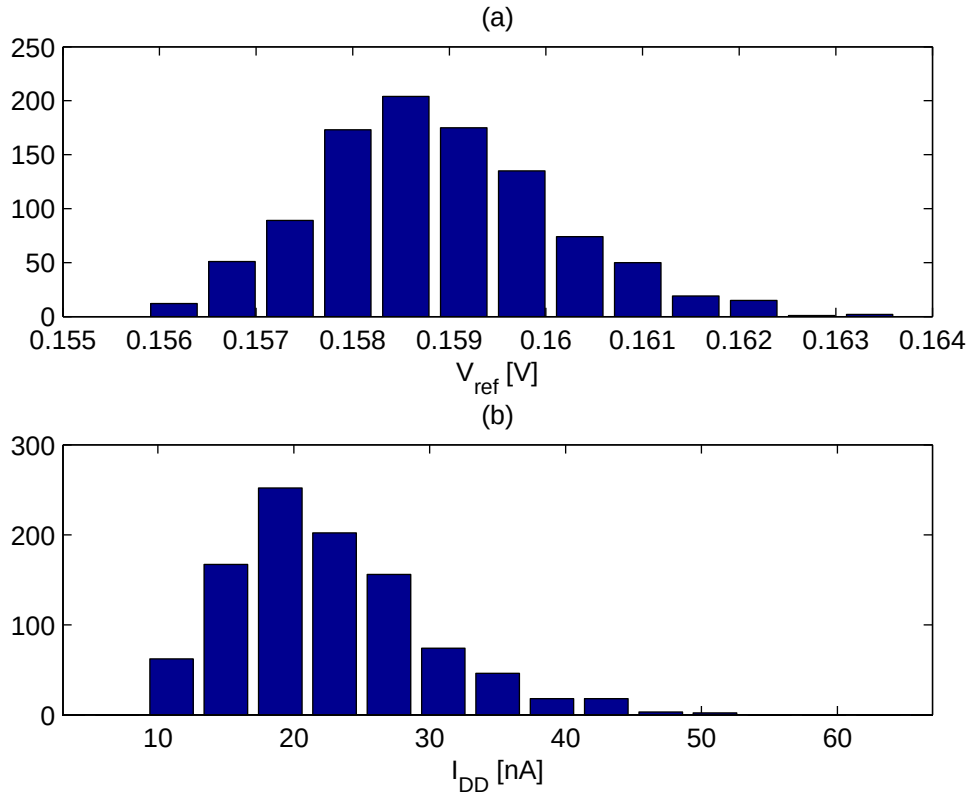


Figure 4.17: Histogram of output voltage and current consumption of voltage reference

stability over process is achieved by making all transistors the same size and matching them as well as possible in layout. A decrease in the threshold voltage of the device, would cause V_{ref} to decrease, assuming a fixed bias current. However, the reduction in threshold voltage also leads to an increased leakage current through the top transistor, bringing the reference voltage back up.

With a required ripple of the regulated supply voltage of less than 10 mV for a 100 mV change in the unregulated supply voltage (section 4.3.1), the supply rejection of the reference voltage when scaled up to 0.5 V needs to be better than 20 dB. The simulated V_{ref} of the implemented circuit under nominal process conditions ranges from 157.7 mV to 163.4 mV, with the unregulated supply voltage changing from 0.55 V to 0.8 V. This translates to a supply voltage rejection of more than 22 dB after multiplying the reference voltage up to 0.5 V, as will be done by the linear regulator. At the same time the current drawn from the unregulated supply changes from 19.6 nA to 23.2 nA.

Simulations over all process corners showed a $\pm 4\%$ change in the reference voltage, making it good enough for the required accuracy. The maximum current consumption over all corners stayed below 77.2 nA when supplied with 0.6 V. The average supply voltage rejection stayed

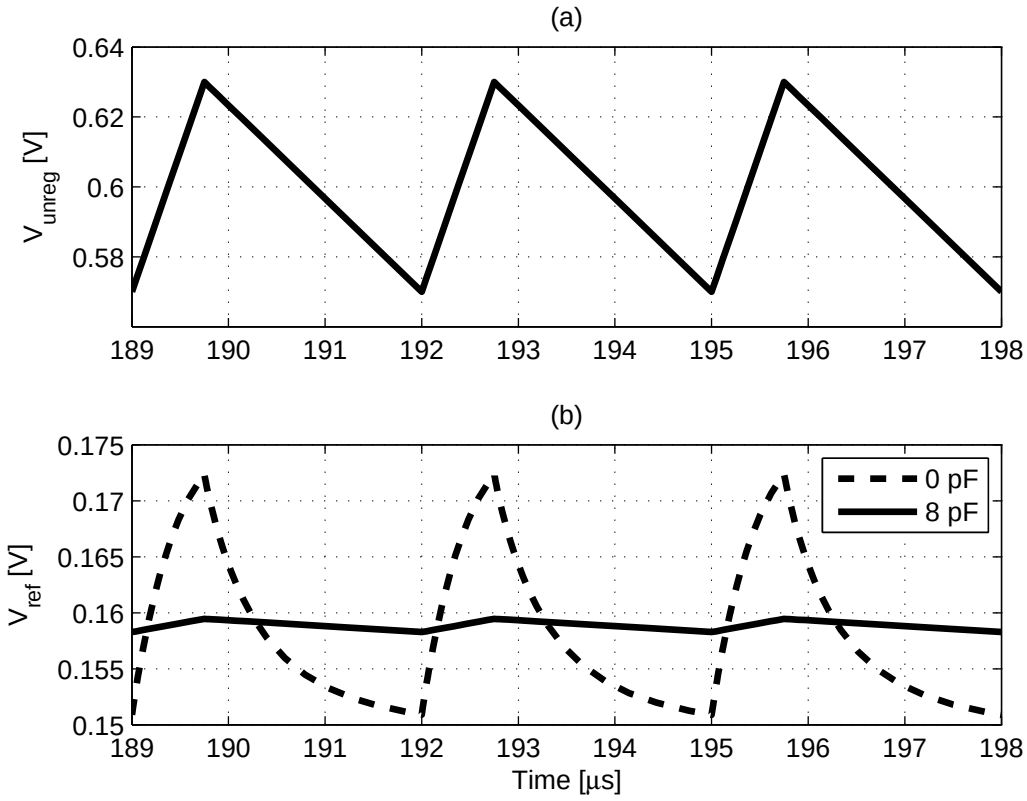


Figure 4.18: Transient unregulated supply voltage (a) and reference voltage for different C_{ref} (b)

above 21.5 dB for all corners. Results of a Monte Carlo simulation over process and mismatch while supplied with 0.6 V are shown in fig. 4.17. The mean of the reference voltage was 159 mV, with a σ of 1.22 mV, giving a σ/μ of less than 1%. At the same time the current consumption averaged to 21.48 nA, with a sigma of 7.13 nA.

All of the previously mentioned simulation results are based on DC simulations. In order to verify the transient behavior of the reference, the unregulated voltage was ramped by $\pm$ 30 mV around 0.6 V based on the expected timing due to the duty cycle. This simulation revealed that due to the large parasitic capacitance of the deep-nwell between V_{unreg} and V_{ref}, and the low current flowing in the reference generator, a ripple of as large as 20 mV on the reference voltage node was observed without the capacitance C_{ref} being present. Adding a C_{ref} of several pF alleviates this problem, as shown in fig. 4.18. A MOS capacitor with a nominal capacitance of 8 pF was therefore added in the final implementation. Adding an even larger capacitor would have improved the supply rejection of the reference voltage even further, at the cost of an increased area. Due to the reference voltage being low and C_{ref} being moderate, the gate leakage of C_{ref} is negligible.

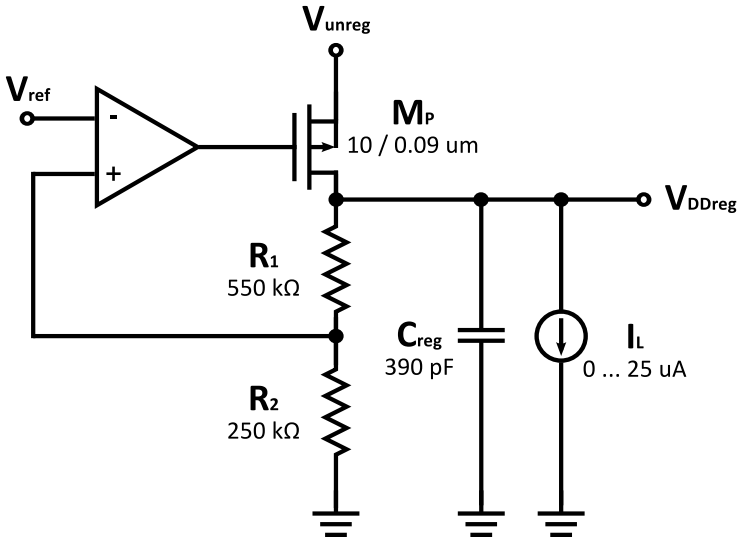


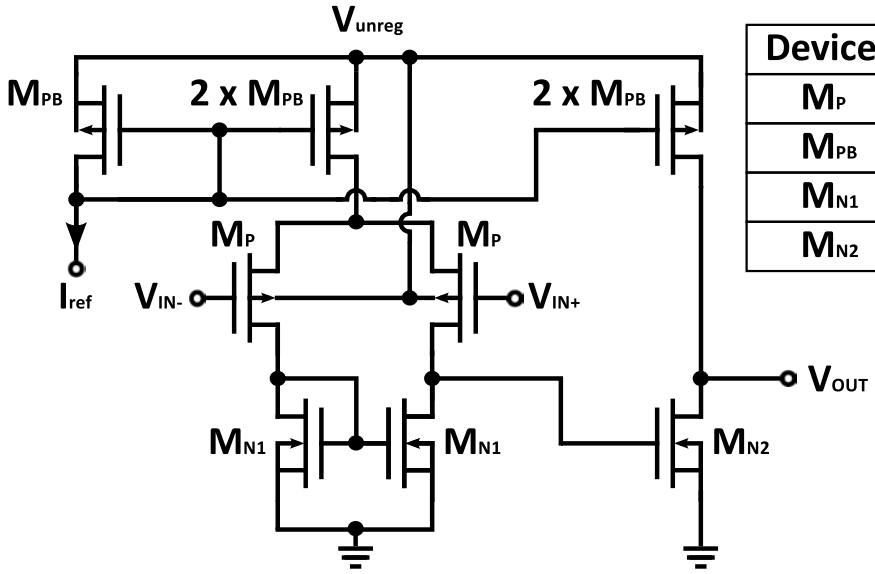
Figure 4.19: Schematic of linear regulator

4.3.4 Low-Drop-Out Linear Regulator

A low-drop-out linear regulator, shown in fig. 4.19 is used to regulate the output voltage to approximately 0.5 V, based on the generated reference voltage. While the unregulated input voltage can range from 0.55 V to 0.8 V, the nominal operating condition for V_{unreg} is 0.6 V with a ripple of less than ± 60 mV. The output current can range from almost 0 up to the maximum supported by the wireless power link. With a worst case minimum DC output power of approximately 11 μW (section 4.2) it needs to support at least 22 μA. In order to provide some margin, the regulator was designed for currents between 0 and 25 μA.

To get an output voltage of 0.5 V with a reference voltage of approximately 160 mV a feedback factor of 0.3125 was implemented using 50 kΩ unit resistors to form R_1 and R_2. The large values of the feedback resistors keep the DC current through them, which directly reduces the current available to the electronics of the implant, low, but also form a non-dominant pole with the input capacitance of the operational amplifier.

The regulator loop consists of two gain elements: the operational amplifier and the transistor M_P. Figure 4.20 shows the implementation of the operational amplifier. It is a conventional two-stage design without any measures to ensure sufficient phase margin. This is justified by the dominant pole being placed at the regulated output and being well below the bandwidth of the amplifier. The amplifier is biased by a current reference shown in fig. 4.21 to provide some power supply independence and achieves a DC gain of more than 40 dB. This gain is high enough to keep the static error of the regulator below 1% across all load conditions. All MOS devices in the linear regulator are of the low threshold voltage, low power flavor of the process. Another important constraint on the amplifier is its offset. The input referred offset of the amplifier has the same effect as an inaccuracy of the reference voltage.



Devices	W/L [um]
M_P	5 x 2 / 0.18
M_{PB}	5 / 2
M_{N1}	1 / 1
M_{N2}	5 / 0.12

Figure 4.20: Schematic of operational amplifier used in LDO

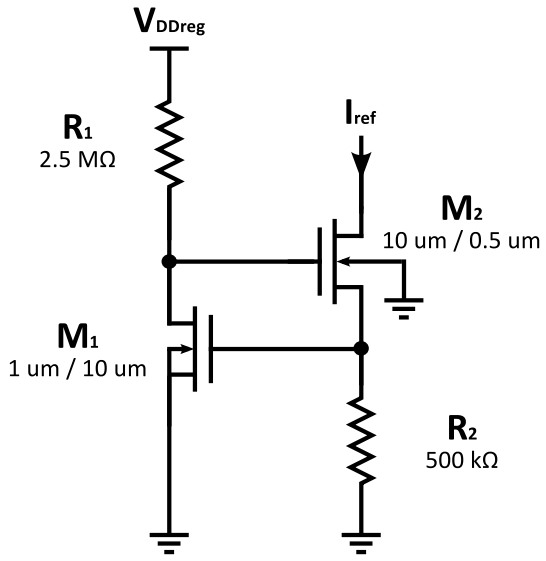


Figure 4.21: Schematic of current reference

Since it is mainly dominated by transistors M_P and to a lesser degree by M_{N1}, the sizes of these transistors where chosen to guarantee 3σ values of the input referred offset of less than 15 mV, corresponding to less than 50 mV at the regulated output, based on given process parameters. While this might not be good enough to guarantee an overall accuracy of $\pm$ 50 mV, due to the additional variability of V_{ref} and the static error of the loop, Monte Carlo simulations suggested that the actual offset might be lower than predicted by the process parameters. Making M_P and M_{N1} larger to further reduce the offset without

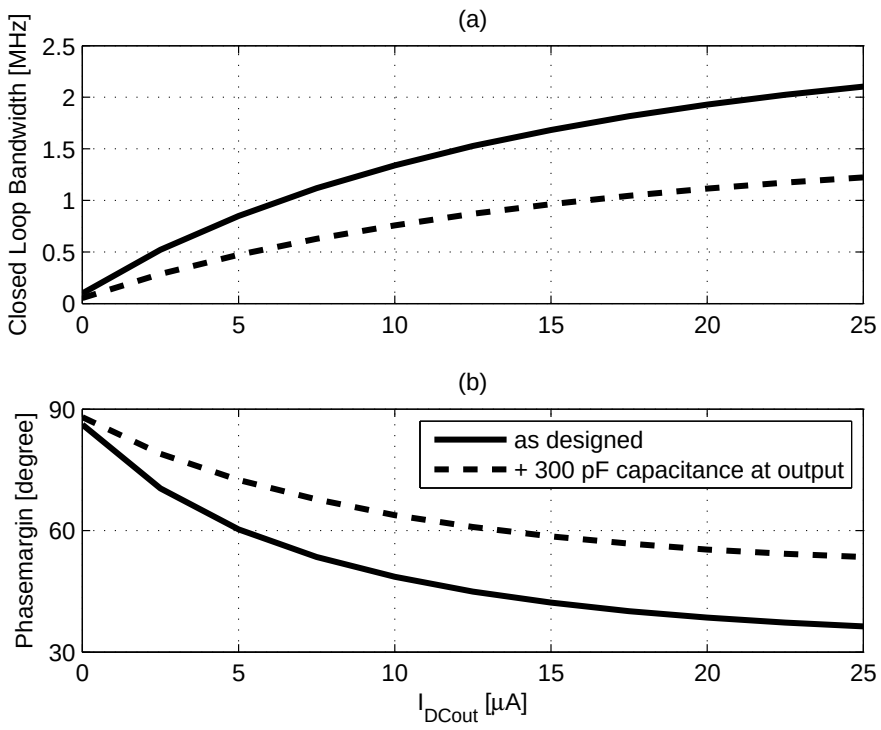


Figure 4.22: Closed loop bandwidth (a) and phase margin (b) of voltage regulator

increasing the power consumption or the area of the circuit could lead to potential instability. Voltage accuracy was therefore traded-off for power consumption.

Due to concerns about the offset modelling, the amplifier implemented on the chip uses an M_P with a L of 0.36 μm and M_{N1} transistors with a W/L of 5 μm / 0.5 μm, reducing the 3σ value of the regulated output voltage based on the hand calculated input-offset of the amplifier down to 30 mV. Unfortunately, simulations after the tape-out revealed insufficient phase margin when drawing close to the maximum load current, leading to oscillations in the transient output voltage. Due to the large input capacitance of the source meters used to measure the regulated output voltage improving the phase margin, this behavior was not observed in measurements. The circuit discussed in detail here uses values that do not show the transient instability, while not increasing the overall power consumption. It might have a higher offset than the implemented one, but power-wise nothing changes.

In order for the regulator to be fast enough, the loop bandwidth needs to be higher than the 330 kHz of the ripple imposed by the 3 μs, coming from the 2 Mbps data rate requirement (section 4.2). At the same time, enough phase margin needs to be provided to ensure stability. Achieving this over a large range of load currents, while maintaining low power consumption and chip area, can be quite challenging. In this design the main focus was on the low load current region, since this was considered to be more important when trying to

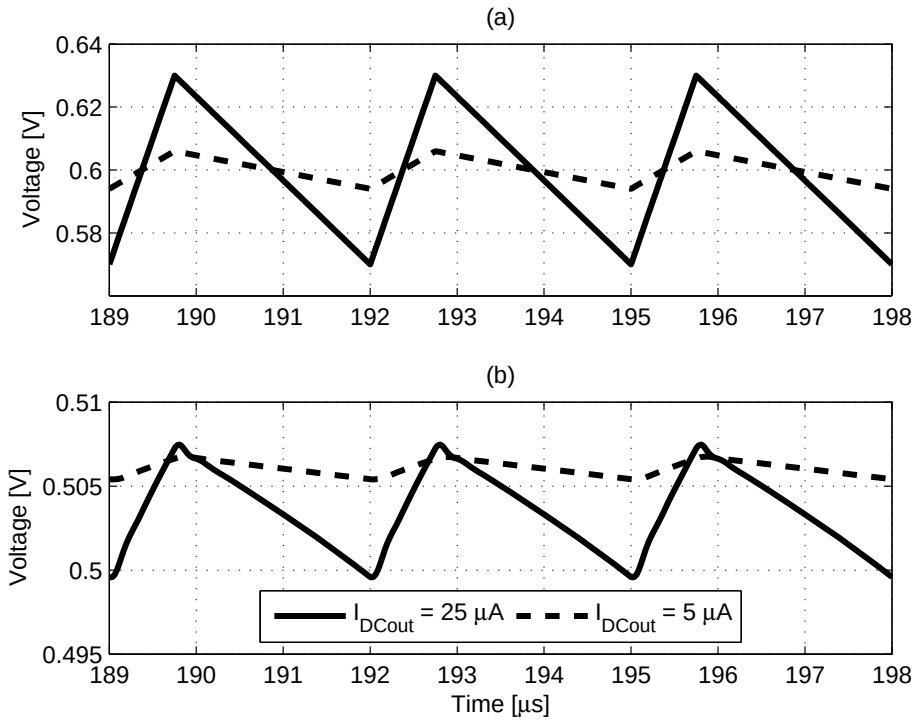


Figure 4.23: Unregulated input voltage (a) and regulated output voltage (b) for different load conditions

show functionality of the fully integrated transponder in animal tests. In this region it is important to keep the power consumption of the operational amplifier very low, and to make sure enough power is available to the transmitter even when the received power is significantly lower than expected. Once the exact available power and load current are established a more optimized regulator should be designed and, in the case of having sufficient power available, spending a little bit more power on the regulator to increase stability would not hurt the overall efficiency too much.

The loop bandwidth and the phase margin over different load conditions of the regulator using the amplifier of fig. 4.20 are shown in figures 4.22 (a) and (b). While the bandwidth is high enough over the entire load range, the phase margin quickly decreases, approaching critical values for larger load currents. Adding additional capacitance in parallel to C_{reg} as indicated in fig. 4.22 would be a simple way to increase the phase margin by decreasing the excess bandwidth. This would however increase the chip area. In the test setup an option for adding additional off-chip C_{reg} if necessary was included.

To investigate the effect of the reduced phase margin under regular operation, additional transient simulations for various load conditions were conducted. As shown in fig. 4.18, the simulations showed that the designed regulator is stable under the normal mode of operation

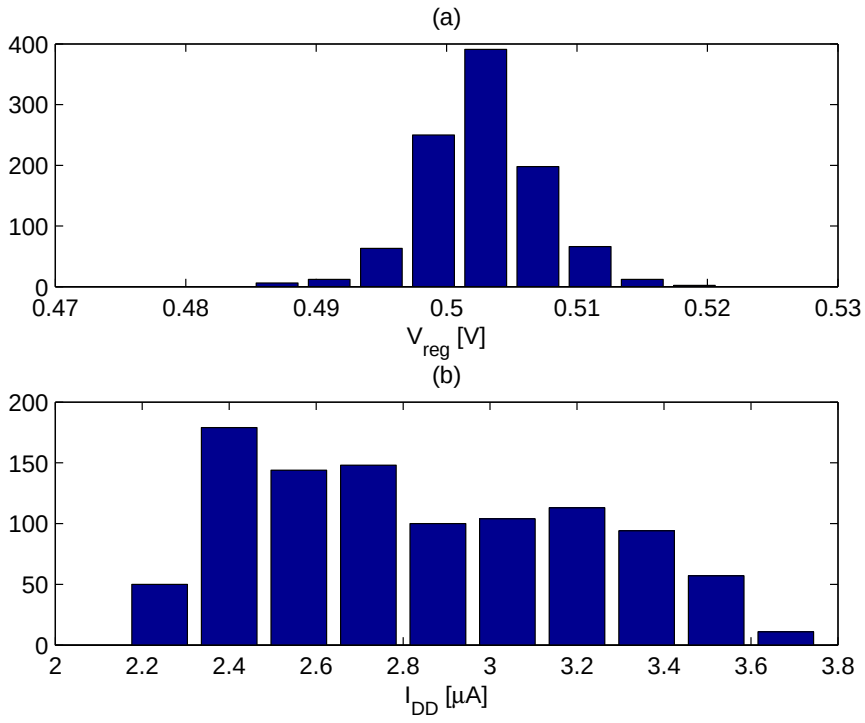


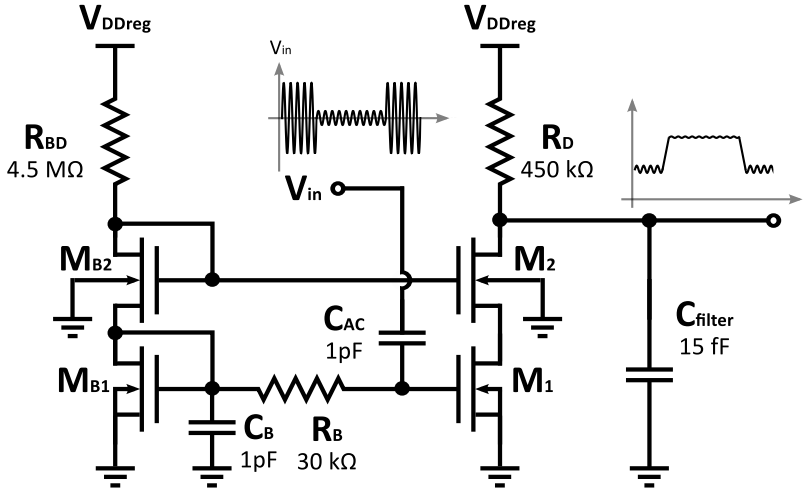
Figure 4.24: Histogram for regulated output voltage (a) and current consumption (b) of LDO

even for high load currents. Since the ripple of the unregulated voltage is a function of the average load current, it has been scaled with the load current as shown in fig. 4.23 (a). Transient simulations were carried out over all corners. When drawing 25 μA, the regulated supply voltage stayed between 485 mV and 530 mV and no ringing was observed. The ripple under typical process conditions was 7.9 mV, with a worst case of 12.6 mV. Although the worst case was slightly higher than the targeted value of 10 mV, it was determined that this was good enough for the targeted system.

Monte Carlo simulations summarized in fig. 4.24 conducted at an unregulated voltage of 0.6 V while drawing 25 μA, lead to an average output voltage of 503 mV and a σ of 4.4 mV. The mean total current consumption was approximately 2.8 μA with a σ of 375 nA.

4.3.5 Synchronizer

The task of the synchronizer is to detect whether the system is in the powering or in the communication phase. It is therefore basically a simple AM demodulator. During the power phase, the input voltage is approximately 280 mV. Assuming at least 12 dB difference in transmitted power between the power and communication phase, the input voltage during



Device Name	M_{B1}, M_{B2}	M_1, M_2
W / L [μm]	$2 \times 2.5/0.13$	$4 \times 2.5/0.13$

Figure 4.25: Schematic of synchronizer

the communication phase is less than 140 mV. The reason for the ratio between the power and communication voltage being only 2 despite the 12 dB difference in power, is due the fact that during the power phase the input impedance of the converter is matched, while during the communication phase it is switched to high impedance (section 4.3.2).

Once a large enough input signal is detected, the output of the synchronizer switches from high to low and turns on the rectifier. The delay with which it turns on is an important design parameter, since the incoming signal is not rectified, and the energy therefore lost, until the synchronizer turns on the rectifier. When the system switches from powering to communication phase, the synchronizer switches from low to high and triggers the transmitter. Too much delay here would have a detrimental effect on the achievable data rate. In both cases delays on the order of 10 ns are acceptable.

As for any of the other building blocks described so far, low power consumption is of utmost importance in order not to consume more power than is gained by increasing the rectifier efficiency by duty-cycling the power signal. For this reason, a common-source AM demodulator based on a transistor biased in weak inversion is used with a cascode transistor connected to its drain to counteract DIBL [Oncu08, Gambini09].

Figure 4.25 shows the input stage of the synchronizer. Together with the output resistance of the amplifier, the capacitor C_{filter} forms a low-pass filter. Its corner frequency was chosen such that it filters out the high frequency (500 MHz) content while it passes the approximately 330 kHz signal representing the input signal envelope. The DC output of the amplifier is designed such that it can be directly connected to a CMOS inverter chain which converts the output signal into a full rail-to-rail signal. The quiescent DC level as well as

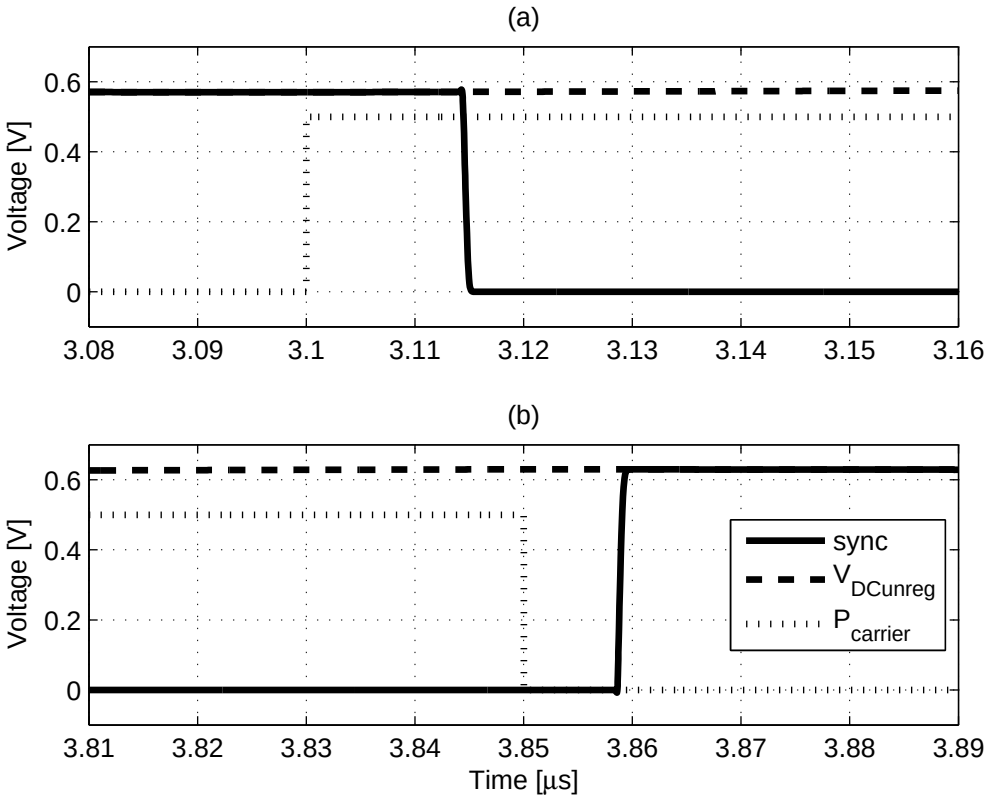


Figure 4.26: Transient results for synchronizer when switching from communication- to power phase (a) and vice versa (b)

the dimensions of the first inverter were chosen such that the crawbar current through the inverter does not get too high, while still making sure that the inverter switches properly when a high enough input signal is available. Biasing is established through R_{BD}, M_{B1}, and M_{B2}. C_B and R_B form a low-pass filter to prevent the AC input signal from modulating the biasing. The lowest threshold voltage devices available in the technology were used for all the transistors in the input stage.

Once the signal is converted to a full swing digital signal, a level-shifter is inserted to shift the high-level from the regulated supply voltage to the higher unregulated DC voltage. This is needed in order to properly switch the rectifier, which operates on the unregulated supply. It is crucial to make sure that the output of the synchronizer stays low during start-up until its input stage is working correctly. Otherwise the rectifier would be turned off, preventing the unregulated and hence the regulated supply voltage from building up. The level shifter was therefore built asymmetrically, so that it always starts-up with the sync-output being low. Extensive transient start-up simulations over process and mismatch were carried out to make sure that this is the case. Higher threshold voltage devices are used in the inverter chain and the level shifter to minimize static power consumption.

Results of a transient simulation of the detection of a typical power and a communication phase are shown in fig. 4.26 (a) and fig. 4.26 (b) respectively. The simulation was carried out assuming 280 mV input voltage during the power phase and 56 mV during the communication phase, representing a 20 dB difference in carrier power between power and communication phase. Detecting the power phase (fig. 4.26 (a)) takes 14.7 ns and switching between power and communication phase (fig. 4.26 (b)) takes 8.8 ns, for typical process parameters. When simulated over process corners, both delays remained below around 25 ns in all but one cases. The single outlier had a delay of 34 ns when detecting the power phase, but only 3.6 ns when detecting the communication phase. It would therefore be possible to reduce the delay for the power detection at the cost of increasing the delay for detecting the communication phase by e.g. increasing R_D.

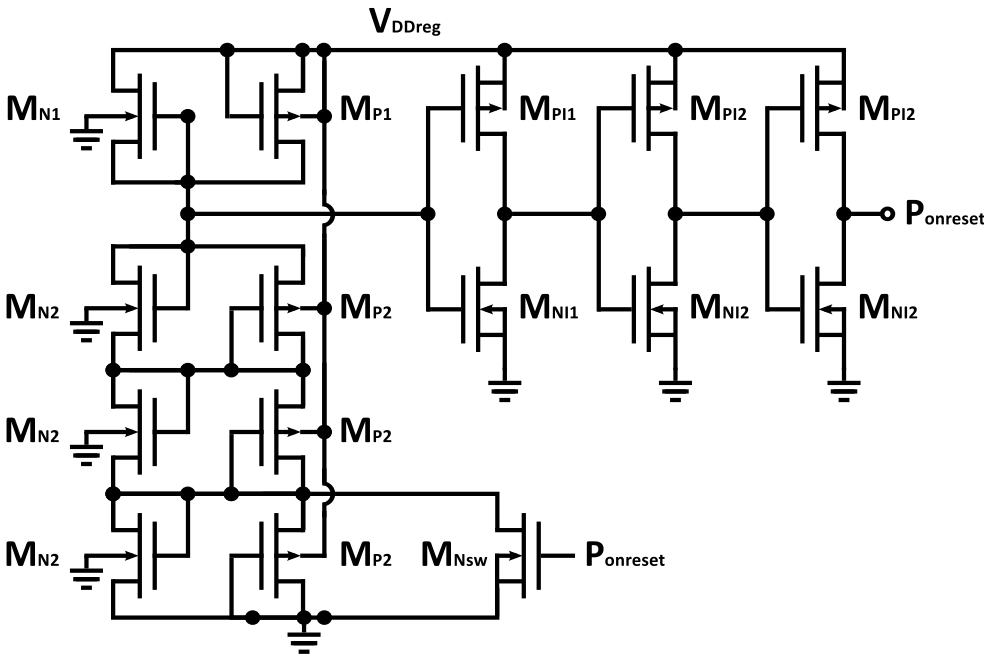
The power consumption of the entire synchronizer does depend on the exact input voltage levels as well as on the exact durations of the power and communication phase. In the typical case simulated above, the circuit draws a total average current of 770 nA and it remains below 2.8 μA even for the worst case process corner.

Simulating the conversion gain from the 500 MHz input signal to the 330 kHz signal at the output of the input amplifier gives a typical value of 1.01, with corner simulations indicating a range over process variations from 0.67 to 1.41.

4.3.6 Power-on-Reset

In order to make sure the digital feedback shift register as well as the state machine controlling the transmitter are properly initialized at start-up, a power-on-reset circuit is needed. It needs to provide a reset signal once a sufficiently high supply voltage is reached and reissue such a signal in case of a temporary drop in power. The key issue besides power consumption is to achieve proper operation over all process corners without trimming. It is important to make sure that a power-on reset gets triggered as long as there is sufficient supply voltage available. At the same time it should not be triggered before the supply voltage is high enough for the digital gates to detect it properly and process it accordingly. Picking the right switching threshold and making sure it stays within a safe window over all process corners is thus the key design challenge here. On top of that, a switching hysteresis was implemented to prevent the reset signal from ringing during start-up due to the ripple on the supply.

Figure 4.27 shows the exact implementation of the circuit. The first stage stage consisting of transistors M_{N1}, M_{N2}, M_{P1}, and M_{P2} is based on the same principle as the voltage reference generation. A pair of M_{N2} and M_{P2} form a forward connected diode. During start-up three of these diodes are connected in series and connected to the regulated supply via M_{N1} in parallel with M_{P1} with their gates connected to their source. The node connecting the leaking transistors to the series connection of diodes is fed into the first stage of a three-stage inverter chain. At the beginning of the power-up process, the input to the inverter



Devices	W/L [um]
M_{N1}	2 x 9 / 0.54
M_{N2}	5 / 1
M_{NI1}	1.2 / 1
M_{NI2}	1.2 / 1
M_{Nsw}	0.9 / 0.18

Devices	W/L [um]
M_{P1}	2 x 49/ 0.18
M_{P2}	6 x 5/ 0.18
M_{PI1}	4 / 2
M_{PI2}	4 / 1

Figure 4.27: Schematic of power-on reset circuit

chain follows the supply voltage and stays above the switching threshold of the first inverter. With the supply voltage increasing further, the diodes start turning on, eventually making the input of the first inverter drop below the switching threshold of the inverter and making the $P_{onreset}$ signal to switch to high. Once $P_{onreset}$ is high, one of the three diodes gets shorted out, reducing the input of the first inverter and hence the level below which the supply voltage must drop for the $P_{onreset}$ to return to zero.

Parallel combinations of NMOS and PMOS devices in the first stage of the circuit were used to achieve a stable operation over all corners (including SF and FS) by at least partially compensating for any shift in the switching threshold of the first inverter. The last two inverters are included to regenerate the signal during the start-up transient to get a full swing output signal with a sharp edge.

All devices in the first stage are low threshold voltage, low power devices. The devices in the inverter stages are still from the low power process flavor but with standard threshold

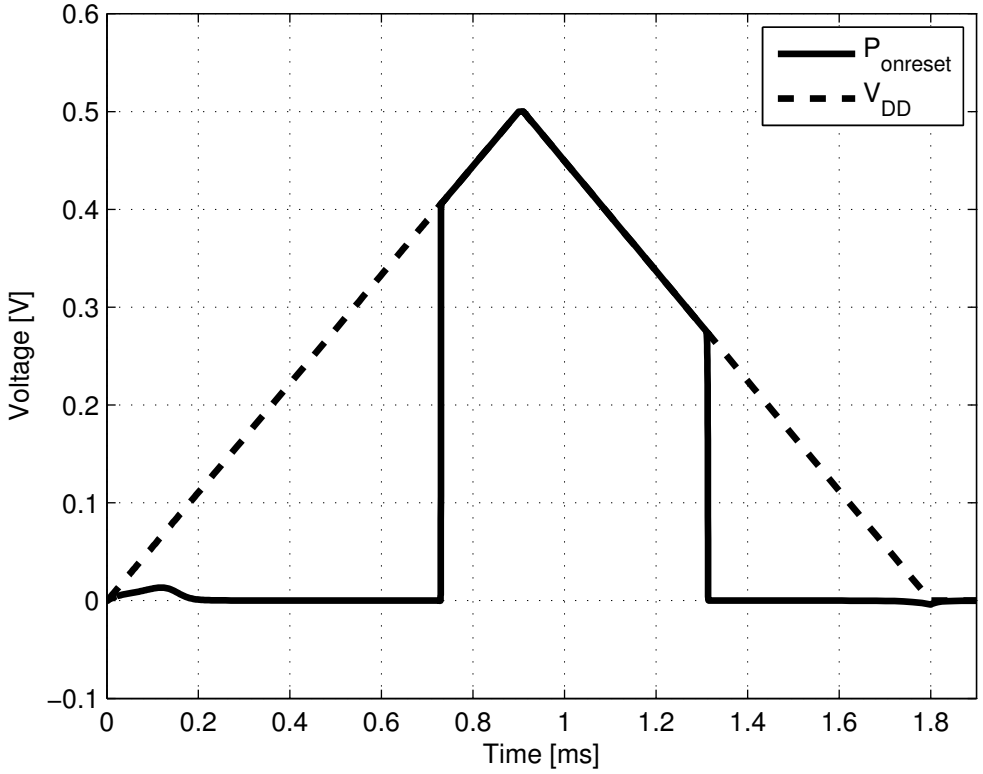


Figure 4.28: Switching hysteresis of power-on reset

voltage to reduce leakage.

A typical simulated power up and down transient is shown in fig. 4.28. Indicating an on- and off-threshold of 0.4 V and 0.27 V, respectively. Due to the slow nature of the circuit, the actual switching thresholds might be quite different from what is obtained by the slow ramp-up shown in fig. 4.28, but this is not a problem as long as it is ensured that the power-on-reset gets issued eventually. In reality it even makes sense to slow down the power-on-reset a bit to make sure the regulated supply voltage reaches its nominal level before "power-on" is indicated.

Once the regulated supply reaches 0.5 V the circuits draws only 12 nA under typical process conditions and never more than 36 nA when simulated over corners. Corner simulations also indicated a minimum and maximum on-threshold of 0.36 V and 0.456 V respectively. Although the maximum threshold is slightly above the minimum specified supply voltage, a power-on-reset can still be guaranteed by slightly increasing the supply power for a short period of time when powering up the system. The off-threshold stayed between 0.25 V and 0.38 V over all corners and the switching hysteresis ranged from 80 mV to 160 mV.

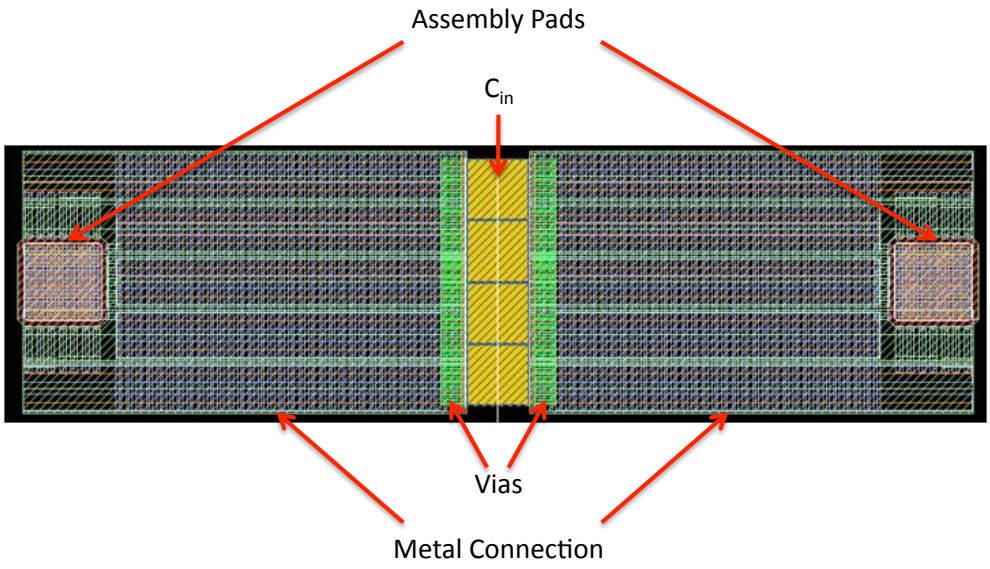


Figure 4.29: Physical connection of bonding pads to input capacitor

4.3.7 Layout and Testchip Implementation

While careful layout is important for every building block, two aspects of the implemented system required extra attention: the connection of the antenna to the on-chip capacitors used to resonate it out and the layout of the core transistors in the AC-to-DC converter.

Due to the experimental nature of the flip-chip assembly, the minimum distance of the two connections between the antenna and the chip was limited to a minimum of approximately 550 μm. The input capacitors, on the other hand, were only about 40 μm wide. Connections between the pads and the capacitor need to have very low resistivity, since any extra resistance de-Qs the resonant tank and manifests itself in additional loss and a lower input impedance. A 170 μm wide trace consisting of the two top metals available in the process, for low resistance and parasitic capacitance, was used to connect the pads to the capacitor. Extensive use of vias between the metal planes was made to achieve good connectivity as well. A patterned shield on the lowest metal layer was added to shield the connections from the substrate. An AC ground was formed by connecting the two shielding layers. The extracted series resistance was 10 mΩ per connection and each of the connections added approximately 800 fF of parasitic capacitance to the shield. These values were low enough with respect to the series resistance of the antenna and C_{in} for them to have only a minor impact on the performance. A screenshot of the layout of the input-connection is shown in fig. 4.29.

When it comes to the layout of the AC-to-DC converter, a number of factors need to be considered. First of all, due to the low input voltage and the comparably large current, the

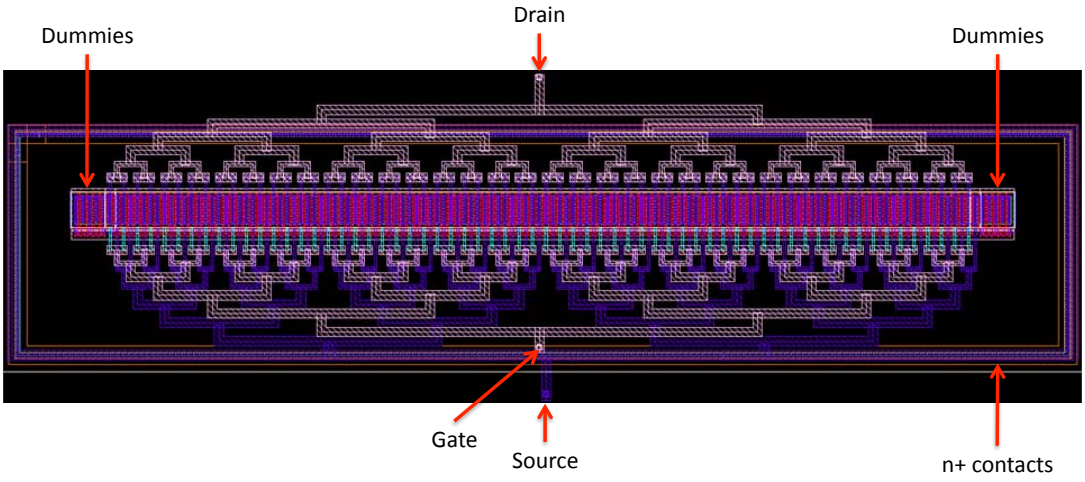


Figure 4.30: Layout of PMOS transistor of stage 2 and 3 of AC-to-DC converter

core transistors are quite large. Fig. 4.30 shows the layout of transistor M_{P2} and M_{P3} from fig. 4.12. The size of the transistor is 152.4 μm / 0.09 μm. In order to reduce the effect of long, narrow gate connections, the transistor was split up into 127 fingers, each 1.2 μm wide. Symmetric, tree-structured metal connections to the terminals were laid out to ensure equal current distribution. Dummy transistors were added on each side of the active device to enhance the uniformity of the single fingers. The well connection was far enough away from the active device to keep any detrimental proximity effects low. The layouts of all the transistors were extracted and used in the actual optimization of the circuit. Doing so allowed to take layout effects into account and either improve the layout iteratively or adjust the circuit accordingly.

Due to the proximity of NMOS and PMOS devices connected between the input terminals, there is a potential risk for latch-up. The use of a deep-Nwell surrounding the NMOS greatly reduces this risk however.

Another concern are currents being injected into the substrate through the parasitic capacitances of the rather large coupling capacitors C_C. To minimize the risks associated with that, patterned metal shields on Metal 1 were included beneath each coupling capacitors and connected to each other to form an AC ground.

The full system, including the transmitter, consumes an active area of approximately 0.45 mm^2, out of which approximately 0.18 mm^2 are occupied by the storage and the regulator capacitor. An additional 0.116 mm^2 are occupied by the connection between the antenna and the input capacitor, and approximately 0.032 mm^2 are due to the coupling MIM capacitors in the AC-to-DC converter. The remaining 0.12 mm^2 are taken up by transistors, resistors, and wiring. By using a more advanced flip-chip technology with a much narrower pitch and moving the MIM capacitors on top of the active area, the overall chip area could be reduced to approximately 0.3 mm^2 without making any changes to the circuits. A die photo of the

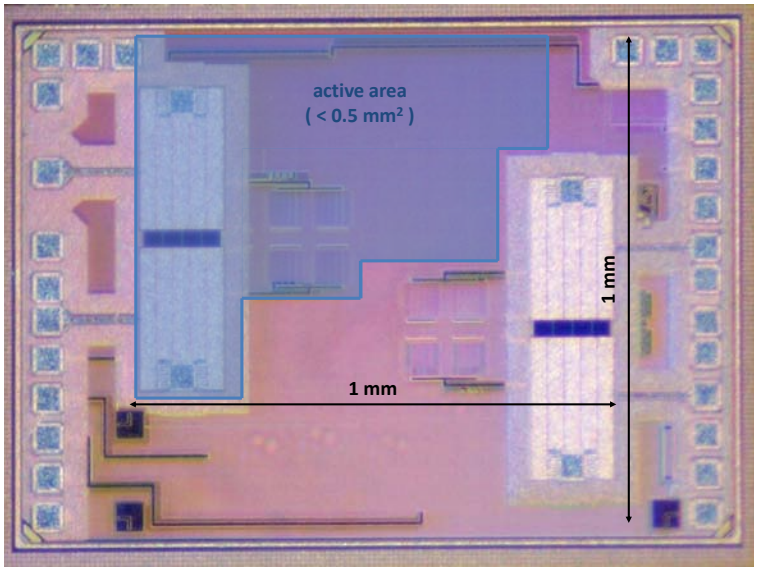


Figure 4.31: Die photo of neural transponder testchip

CMOS chip is shown in fig. 4.31

For testing purposes two almost identical systems were implemented on a single CMOS die. One version was targeted for circuit characterization and lab bench system level tests. It included an SPI interface to tune some of the system characteristics such as reference voltage or switching threshold of the synchronizer and to separate some building blocks from each other for block level testing. This version further included some internal signals from the transmitter routed to pads, such as the signal controlling the input impedance modulation. Since this version required an external supply for the SPI to work properly, it is not very well suited for animal tests. A second version without SPI interface was included on the same die. It included the same tuning capabilities as the SPI version, but this time implemented with laser fuses. The idea was to first try out the settings on the SPI version and then, if necessary, apply the same tuning settings to the second version by programming the fuses, relying on reasonable matching between the two versions. In order to keep any detrimental effects pad connections of certain internal signals might have low, much fewer signals were made available for measurements in the fuse-programmable version. Only the regulated and the unregulated DC voltages, and the power-on-reset signal were connected to bond pads.

The total chip area is about 1.4 mm by 1 mm and therefore slightly bigger than the claimed 1.1 by 1.1 mm^2 footprint of the system. However, as can be seen in fig. 4.31, the additional area is occupied by bond pads which only serve testing purposes. In a final version of the system these pads would not be necessary and the chip would easily fit in the 1 by 1 mm^2 footprint.

A photo of the fully assembled system consisting of the CMOS die and the antenna flip-chip assembled on top of it is shown next to a U.S. cent in fig. 4.32.

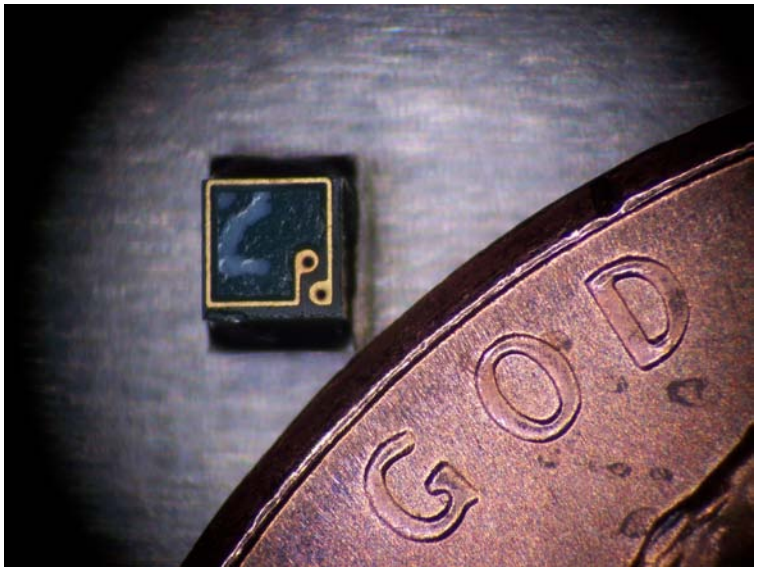


Figure 4.32: Assembled system next to a U.S. cent

4.4 Experimental Results

Several experiments were conducted to verify the chip as well as the overall system functionality and performance. This section summarizes the results from DC chip and AC impedance measurements, transient chip tests, as well as system tests conducted in air and in animal and compares them to simulations.

4.4.1 DC Measurements

DC measurements were done using the SPI version of the system. Doing so allowed to separate the AC-to-DC converter from the regulator and to power down the transmitter.

The regulated output voltage stayed well within the values expected based on Monte Carlo simulations (fig. 4.24) and the measured PSRR of 17.5 dB agreed well with simulations too. Trimming the reference voltage via the SPI interface also worked as expected.

Due to the limited number of pads available, the DC current consumption could only be measured at two points: the output of the AC-to-DC converter and the input of the regulator. This was done while the output of the converter (after the storage cap) was disconnected from the input of the regulator via the SPI. Measurements at the output of the converter therefore included the leakage of C_{stor} and the rectifier, while the current consumption of the regulator (including leakage of C_{reg}), synchronizer, reference voltage generation and power-on-reset was lumped into the current measured at the input of the rectifier. Measurement results were within 4% and 8% of the simulated values at the converter output and the regulator input, respectively.

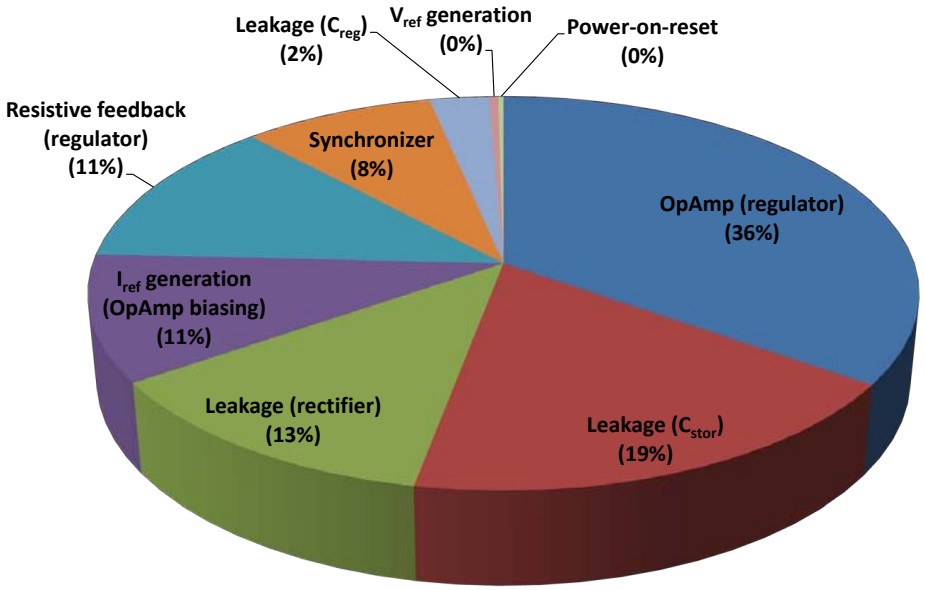


Figure 4.33: Simulated DC power breakdown

Figure 4.33 shows the simulated power breakdown of the complete system for the different building blocks. The total DC power consumption referred to the regulated output was about 2.5 μW. About 60% of the power is consumed by components associated with the voltage regulator. Various types of leakage accounted for 34% of the power, some of which could be easily reduced by using thicker oxide for the storage capacitors (minimum oxide thickness capacitors were used in this design). This comes at the expense of additional chip area however. Alternatively, the amount of storage capacitor could be reduced, but the effect this has on the overall system efficiency due to increased voltage ripple has to be considered. There might also be some room for improvement on the leakage through the rectifier, since this was an area that received less attention during the design of the current system. Finally, the synchronizer consumes about 8% of the static power. However, it is important to note that the synchronizer's power consumption increases by approximately 70% during operation due to the dynamic power consumed by the switching of the rectifier and the changing input levels.

4.4.2 Transient Functionality Tests

In order to verify the chip functionality under transient operating conditions, a pulsed 500 MHz signal was applied to the input of the chip (without antenna attached) via a balun. While doing so, the regulated and unregulated DC voltages, the power-on-reset, and the sync signal were monitored and full functionality could be confirmed.

4.4.3 Input Impedance

To verify the exact resonance frequency of the tank formed by the antenna and the input of the transponder, S_{11} measurements of the input impedance of the fully assembled transponder were performed. This was done using microprobes and a network analyzer. The power at which the measurement was performed was kept low to reduce the impact of the input resistance of the AC-to-DC converter. Three important conclusion could be drawn from these measurements.

First, the resonance frequency was slightly higher than expected, closer to 535 MHz. This was mainly due to pessimistic assumptions made on the parasitic capacitances of the system during design time. However, due to the rather flat behavior of the link efficiency over frequency around its peak point (fig. 4.8) the reduction in link loss compared to 500 MHz is almost negligible, as long as the matching network of the external antenna is adjusted. Second, the impedance at resonance was significantly lower than expected based on simulations. Finally, a rather low yield was observed and even with working chips a significant spread in the resonant impedance was observed.

The last observation specifically suggested some problems with the flip-chip assembly. The applied flip-chip assembly process uses a gold stud bump on the CMOS pad and connects it via conductive epoxy to the pads on the micro-PCB. In this process the gold stud is created by cutting a bond wire that was previously attached to the CMOS pad right above the gold ball typically formed on top of the bond pad during bonding. Conductive epoxy is then applied manually to glue the chip and the antenna together while ensuring good conductivity. Additional underfill materials are used between the two components to provide mechanical stability [Jordan02]. This process has the advantage of being able to be performed on standard CMOS pads since it does not require any special pad post-processing. Further it can be done using standard bonding equipment while capable of providing decent performance. However, it is also known as not very robust and prone to performance degradation over time [Reinert00]. Although resistance values for the flip-chip assembly can be on the order of 100 mΩ, it is a strong function of the way the conductive epoxy is applied and the pressure that is used when connecting the parts so values of up to 0.8 Ω for a single flip-chip contact have been reported [Myung-Jin99].

Adding extra resistance on the order of 0.5 Ω to 0.75 Ω per connection to the simulation setup allowed to reproduce impedance levels similar to the ones observed in measurements. Figure 4.34 shows the magnitude of the input impedance of several measured samples as well as simulated ones. Adding 1 Ω of extra resistance (equivalent to 0.5 Ω per connection) to the system simulated without metalization and 1.5 Ω to the system with a full metal plane representing the chip metalization brings the simulated impedance levels at resonance down to the range of the measured values. However, while the system without metalization required only a capacitance of 15.6 pF, which is reasonably close to the expected input capacitance of the transponder, for its resonance frequency to line up with the measured ones, more than 18.3 pF were needed to achieve the same for the system assuming worst

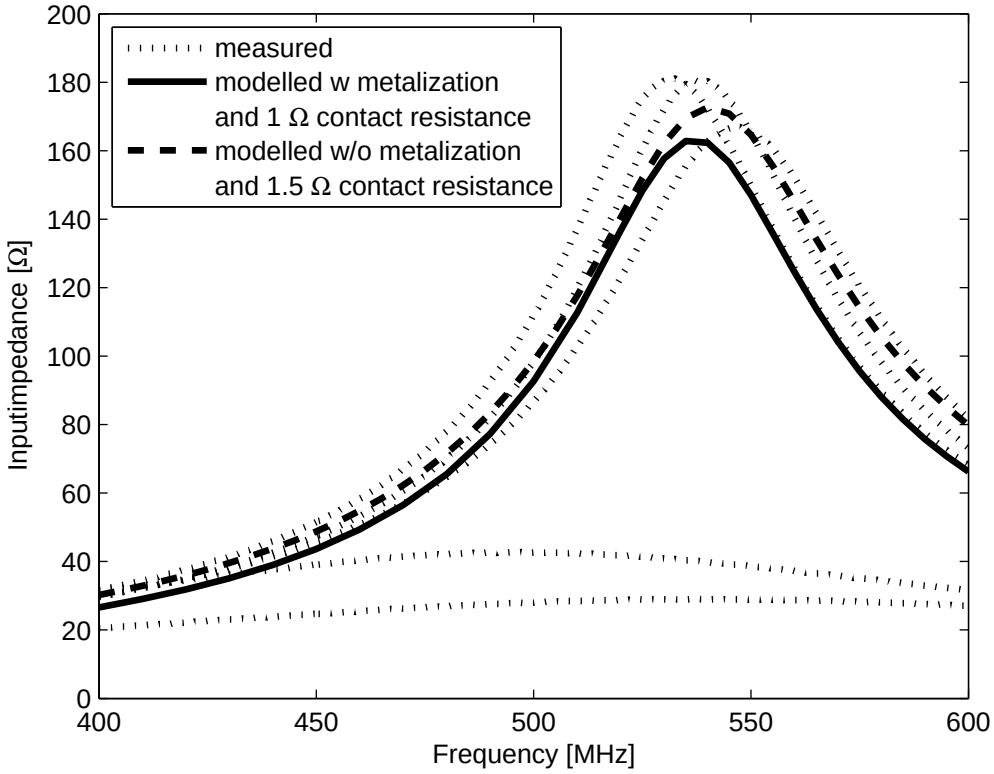


Figure 4.34: Measured input impedance of different samples compared to modelled impedances

case metalization. This suggests that the effect of the metalization is closer to the ideal case without any metal being present than the worst case with a solid metal plane representing the metalization.

Figure 4.34 also shows two measured curves with impedance levels significantly below the others and experiencing a much broader peaking behavior. Such behavior could be explained by assembly resistances on the order of 5 Ω per connection, serving as indicator for a large spread in performance and low robustness of the assembly process.

4.4.4 System Tests

An external transmitter as shown in fig. 4.35 was built to test the system. Two signal paths, one for the power phase the other for the communication phase, are generated by an Agilent E4438 signal source followed by a power splitter. The power path consists of a power amplifier (MPA-450 from RF Bay, Inc.) in series with a programmable attenuator. A SPDT (single pole double throw) switch (ZYSWA from Minicircuits) is controlled by a pattern generator

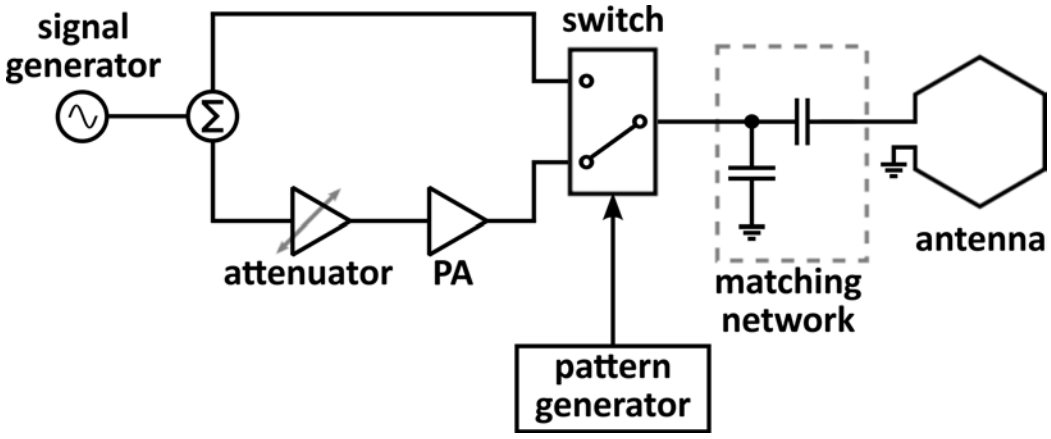


Figure 4.35: External setup for system test

(Agilent 81134A) and connects the power or communication path to the matching network of the antenna as appropriate. The maximum power going into the antenna is limited by the maximum power handling capability of the switch in this setup. Two capacitors form the matching network of the external antenna. One is connected in series with the segmented loop antenna, the other one is connected in parallel to the series combination of the first capacitor and the antenna. The matching network was optimized in Agilent's Advanced Design System (ADS) based on an antenna model obtained from HFSS simulations in the presence of air or tissue, depending on the experiment. A measured S_{11} of better than -10 dB and a bandwidth of 8 MHz was achieved.

Measured results are compared to system simulations carried out in Cadence using two-port S-parameter files obtained from link simulations performed in HFSS. An ideal matching network was used on the primary side and a loss of 0.5 dB due to the matching network obtained from ADS simulations was included in the simulation results.

The following sections summarize the results of various experiments obtained with the non-SPI version of the CMOS chip.

4.4.4.1 Over-the-Air

Non-Duty Cycled Operation

The system was first tested in air. Both, the external antenna as well as the implantable system, were mounted on micropositioners on a probe station to allow precise control of antenna alignment and guarantee repeatability of the experiments. In the test, the external power was varied while a DC current was drawn from the regulated output voltage with a source meter. For each external power level the drawn current was adjusted until a fixed regulated voltage at the output was achieved.

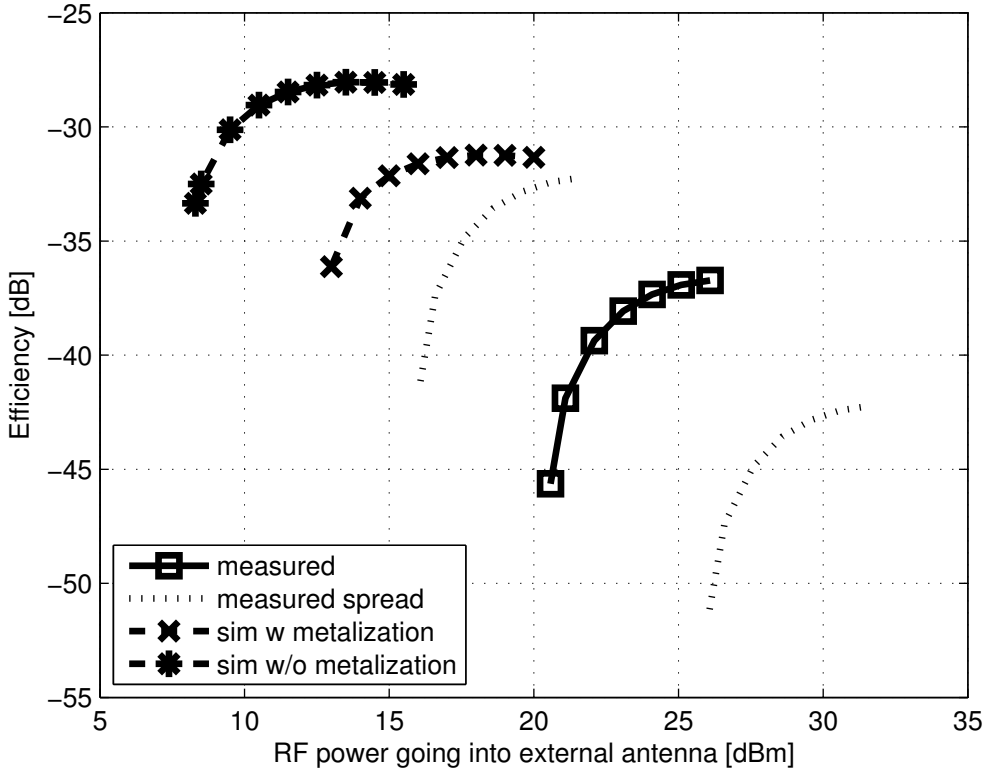


Figure 4.36: External antenna to internal DC efficiency versus power going into external antenna

Spot tests for different antenna separations showed a significant spread in performance between different samples. More than 10 dB difference in external power required to achieve a certain DC output power was observed between the best and the worst performing sample. Additionally, a number of samples did not work at all. Overall the observed yield was less than 50%. Both the spread as well as the low yield are attributed to the flip-chip assembly as discussed in section 4.4.3.

Figure 4.36 compares the measurement results for an antenna separation of 13 mm to simulated values based on the two different cases of metalization used in simulation. Additional capacitance was added to the fully metalized simulation setup to bring the resonance frequency down to 535 MHz for a fair comparison. The dotted lines represent results derived from the actual measured curve based on single point measurements with different samples at different distances and power levels. Due to the low yield and performance degradation over time - some of the devices even stopped working after some time - full characterization of multiple samples at various distances and over the full power range was not possible. The sample used to take the measurements shown in fig. 4.36 performed in general about 4.5 dB worse than the best sample measured, but also about 5.5 dB better than the worst working

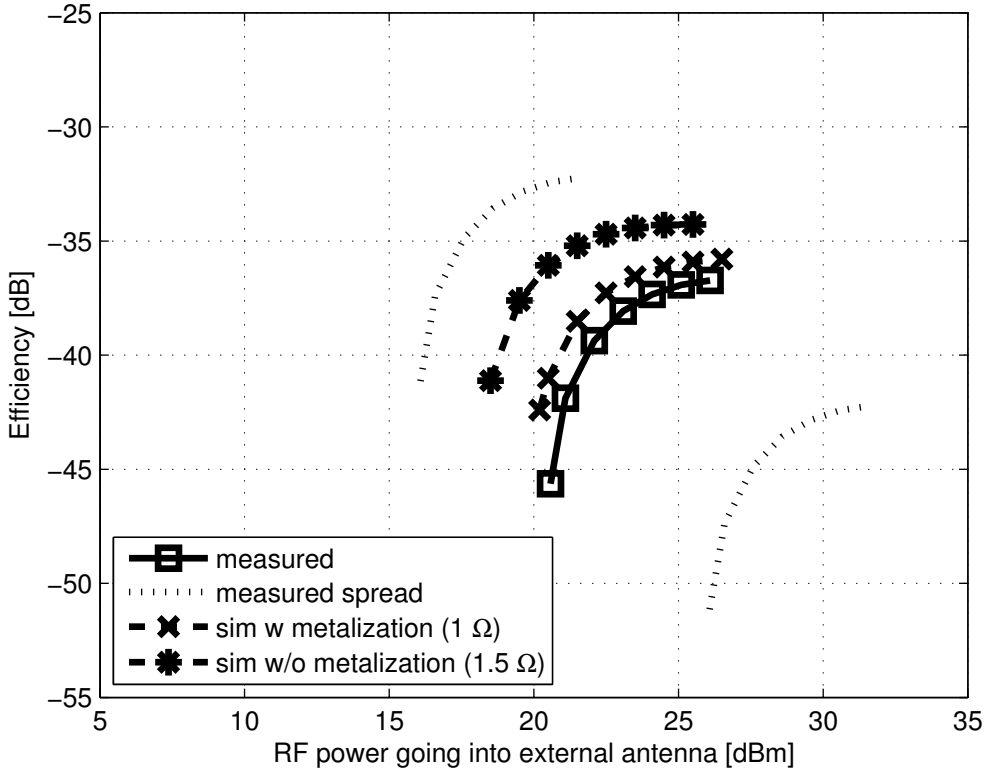


Figure 4.37: External antenna to internal DC efficiency versus power going into external antenna with extra contact resistance

sample. While the actual shape of the dotted curves might be quite different from what is shown, due to the different resonant input impedance these devices are expected to have, they serve as good indicators for what would be possible with a flip-chip process performing more consistently around its best case corner, even if the same flip-chip technology would be used.

However, even when taking the observed spread into account and comparing it to the worst case simulation, simulations predicted an efficiency that was 1 dB better then the one estimated based on the best performing sample. Taking into account the extra resistance that caused the simulated resonant impedance levels in fig. 4.34 to line up with the measurements, brought simulations and measurements much closer together in this case as well. As shown in fig. 4.37, adding in these resistances not only brought the simulation results well within the measured range, it also changed the shape of the simulated curves making them almost identical with the measured curve. After accounting for the extra resistance, the measured results were within 2.5 dB and 1 dB of the simulated values and the best measured sample even outperformed the simulated systems. This provides more evidence that the main limitation of the implanted system is due to the flip-chip assembly. A more advanced

and reliable flip-chip assembly method, using advanced bumping and solder technologies, can provide reliable connection resistances on the order of a few mΩ [Kloeser98] and could therefore significantly improve the systems performance.

Duty Cycled Operation

Next, the effect of duty cycling the power phase on the available power was verified experimentally. At a fixed distance, the external power was adjusted such that the system operates in its most efficient region ($V_{inpk} > 0.28$ V). Then, the DC power at the output of the regulator under continuous powering ($P_{DC,continues}$) was measured. Finally, the DC power under duty-cycled power conditions ($P_{DC,dutycycle}$) was measured under various duty-cycling conditions. The relationship between the power obtained under duty-cycled operation and the power obtained during continuous operation is given by

$$P_{DC,dutycycle} = P_{DC,continues} \times Dutycycle - (1 - Dutycycle) \times P_{diss} \tag{4.2}$$

where

$$Dutycycle = \frac{t_{power} - t_{transient} - t_{dsync}}{T} \tag{4.3}$$

and

$$T = t_{power} + t_{communication}. \tag{4.4}$$

The dissipated power P_{diss} is the total average power consumed by the various blocks of the transponder, such as the regulator, synchronizer, and transmitter. In the measurement setup the transient loss was dominated by the time constant of the external antenna and its matching network, which was determined to be approximately 130 ns. Since this transient loss is related to the external signal building up, the applied signal contributes less to the SAR during that period, and the transmitted power values could be adjusted accordingly. Its impact on the power available to the implant can therefore be heavily attenuated. This was not done for the data presented here, however.

Figure 4.38 (a) compares the actual measured results with the results derived from the measured non-duty-cycled performance using equ. 4.2 for a fixed on-time of 600 ns and varying off-times, with P_{diss} obtained from simulations. The error between the predicted and the actual measured power stayed well within 4% over the entire range. The figure also shows how decreasing the duty cycle decreases the available power.

In the second experiment, shown in fig. 4.38 (b), the duty cycle was kept fixed at 13 : 64 and the on-time was varied. This setup shows the effect of the loss due to the start-up transients. With the start-up transient of the external antenna being 130 ns, almost half of the power

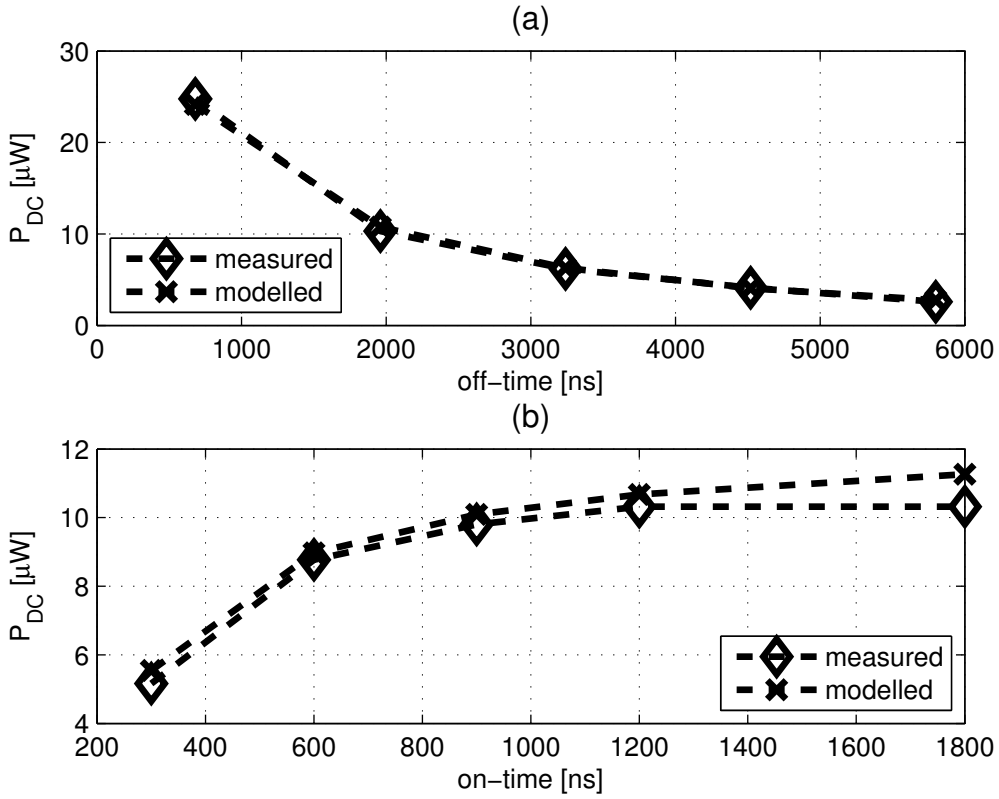


Figure 4.38: DC output power under duty cycled operation for fixed on-time (a) and fixed duty-cycle (b)

gets lost when the on-time is only 300 ns. The longer the on-time the lower the impact of the fixed start-up transient. In this case, the error of the model increases with increasing on-time. For an on-time of 1.8 μs the model predicts an almost 10% higher output current than the actual measured one. This is most likely due to the ripple on the unregulated supply becoming large as the off-time increases, eventually leading to results deviating from the predicted values.

The two experiments described so far all assumed a 20 dB difference in externally applied power between the power and the communication phase. To investigate the effect the power during the communication phase has on the available power, a measurement with a fixed on-time of 600 ns, a fixed duty-cycle of 13 : 64, a fixed power during the power phase, and with varying power during the communication phase was performed. Figure 4.39 shows the results obtained from this measurement. The tested system worked until the power during the communication phase was only 10 dB below the power during the communication phase. Higher power levels during the communication phase do not make much sense, since they would contribute too much to the average SAR for the duty cycled powering approach to still make sense. Until the communication phase power drops below 14 dB below the power phase

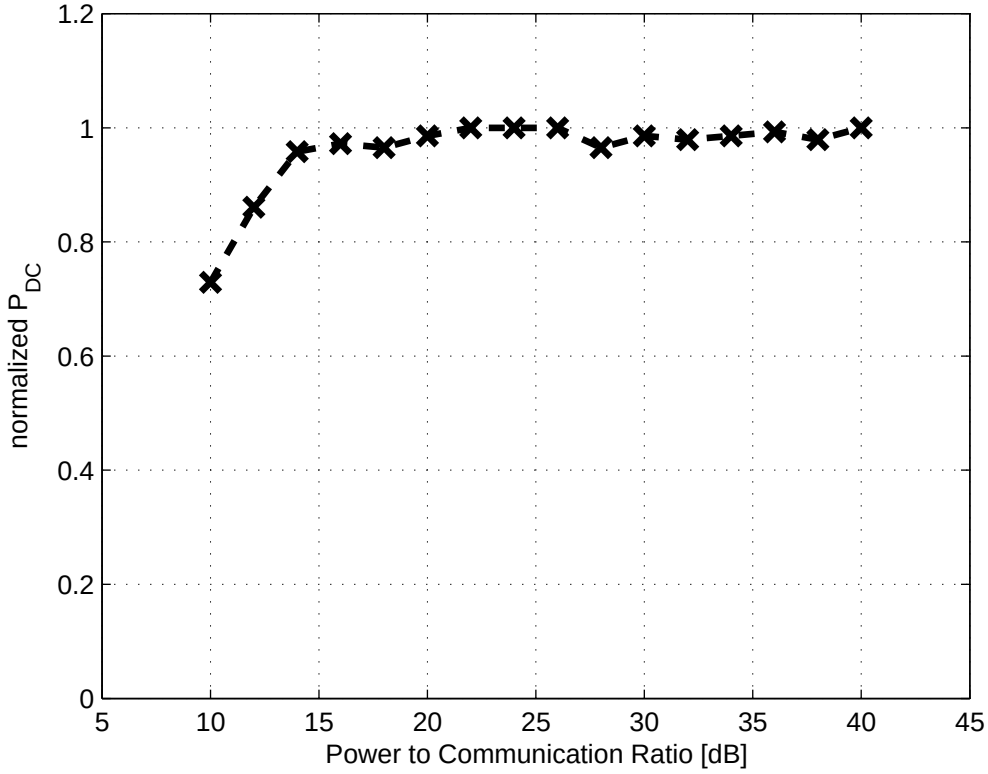


Figure 4.39: Measured DC output power under duty cycled operation for different power-to-communication power ratio

power, the available output power is significantly reduced. While this behavior is expected, only a small portion (approximately 15%) of it can be attributed to increased power in the synchronizer due to the output of its first stage staying closer to the switching point of the first inverter. The remaining loss at lower power-to-communication power ratios can most probably be attributed to the increased time it takes for the input tank voltage to drop below the switching threshold of the synchronizer due to the time constant of the tank. This leads to the rectifier being on when the input voltage is low for an extended period of time, and therefore actively discharging the storage capacitor.

Misalignment

The effect of non-perfect alignment of the antennas in the horizontal plane was investigated by moving the external antenna in the x- and y-plane, while keeping the position of the transponder constant. Non-duty cycled operation was used in this experiment. To compensate for the non-linear effect of the AC-to-DC conversion, the externally applied power was adjusted to provide exactly the same DC power at the implant for each measurement.

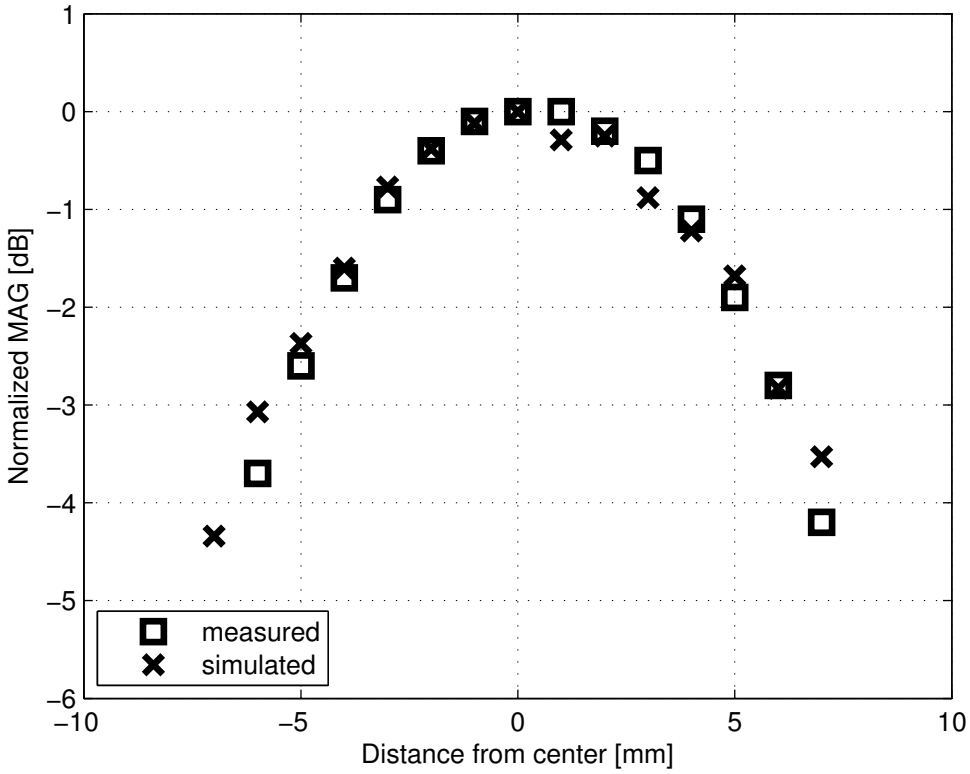


Figure 4.40: Effect of misalignment in xy-plane on coupling

Figure 4.40 compares the measured results with simulations normalized to the maximum measured and simulated values, respectively, for a distance of 13 mm and shows a fairly good agreement between the two. Measurements and simulations with changing only the x- and y- coordinates as well as changing both confirmed nearly perfect symmetrical behavior. For misalignments of less than 3 mm the channel loss only increases by about 1 dB, but it starts to roll off quickly when moving further away from the center.

Distance Variation

Similar to the misalignment measurements, the change in channel loss with varying distance was measured as well. The obtained measurement and simulation results, again normalized to the maximum measured and simulated values respectively, are compared in fig.4.41 again showing good agreement between them.

Especially the last two sets of measurements prove that the simulation setup is able to predict the coupling behavior over a wide set of antenna arrangements, and provides further evidence that the discrepancy in the overall power transfer efficiency reported in fig. 4.36 is

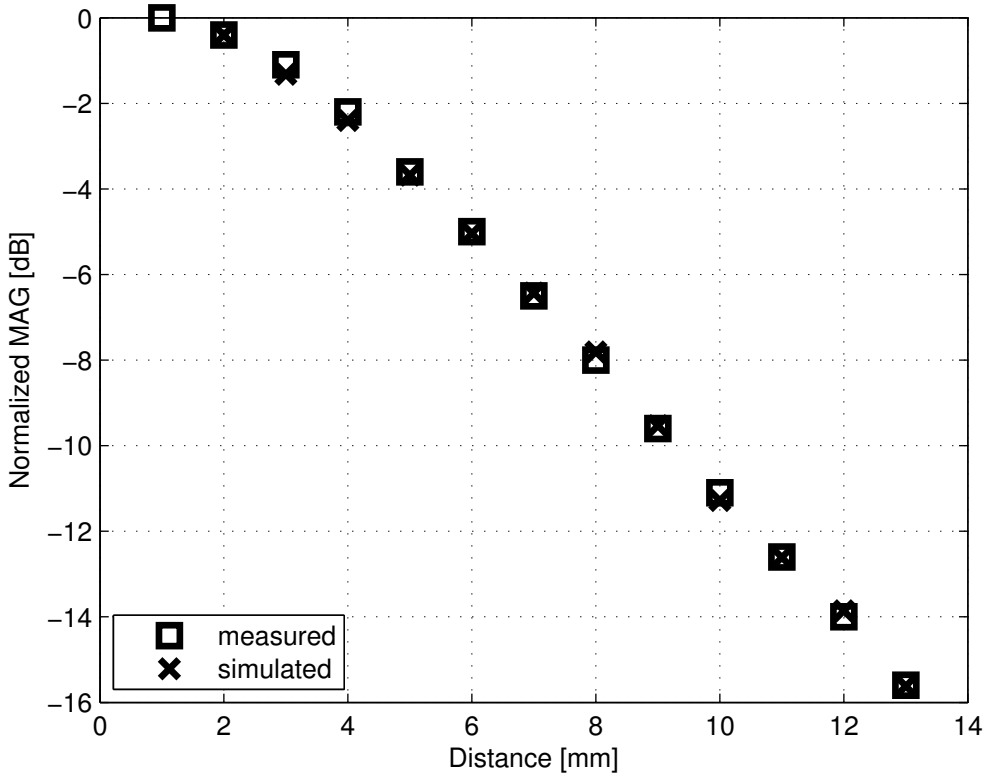


Figure 4.41: Normalized Coupling vs. distance in air

unlikely due to inaccuracies in the link simulation.

4.4.4.2 Animal Test

In order to verify the system functionality in a scenario closer to the actual application, the transponder was implanted in the head of a suckling pig, 3 days postmortem. A pig was used because of the similarity of its anatomy to that of a human. The non-SPI version of the transponder was mounted on a small PCB with the unregulated and regulated DC voltages bonded to the board. It was then placed on top of the pig's brain and two miniature SMA cables were used to access the DC voltages from outside the skull. Finally, the skull and the skin and fat layer was put back onto the pig's head to cover the brain and the transponder. Figure 4.42 shows pictures of the setup. The external segmented loop antenna was then placed on top of the pig's head, 3 mm away from the skin. Overall, the channel consisted of 4 mm of skin and fat, 6 mm of bone, and 3 mm of air, which is very close to the worst case of 2 mm of skin, 2 mm of fat, and 7 mm of bone, used for the human anatomy throughout this work. The simulation model was adapted accordingly, by splitting up the 4 mm of skin and fat in half and assigning 2 mm to each type of tissue.

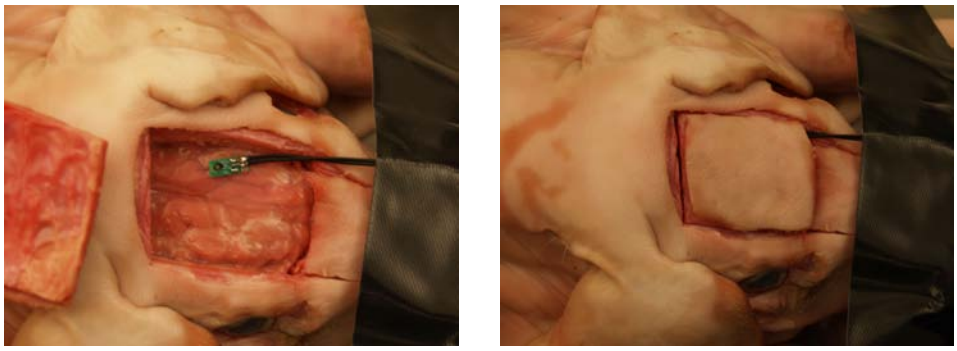


Figure 4.42: Transponder implanted in pig head

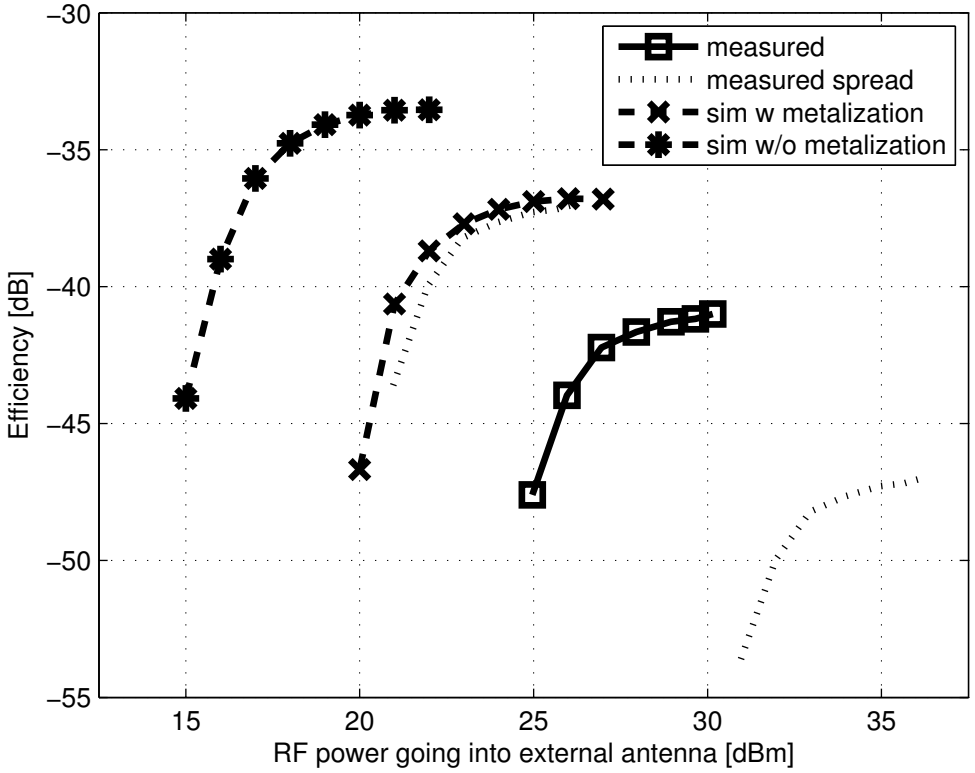


Figure 4.43: External antenna to internal DC efficiency versus power going into external antenna (pig)

Non-duty cycled power measurements were carried out on a sample that performed slightly better than the one used to fully characterize the link in air in section 4.4.4.1, but still about 4 dB worse than the best sample measured in air. The comparison of the measurement results with the simulated ones, not including any extra resistance due to the flip-chip assembly,

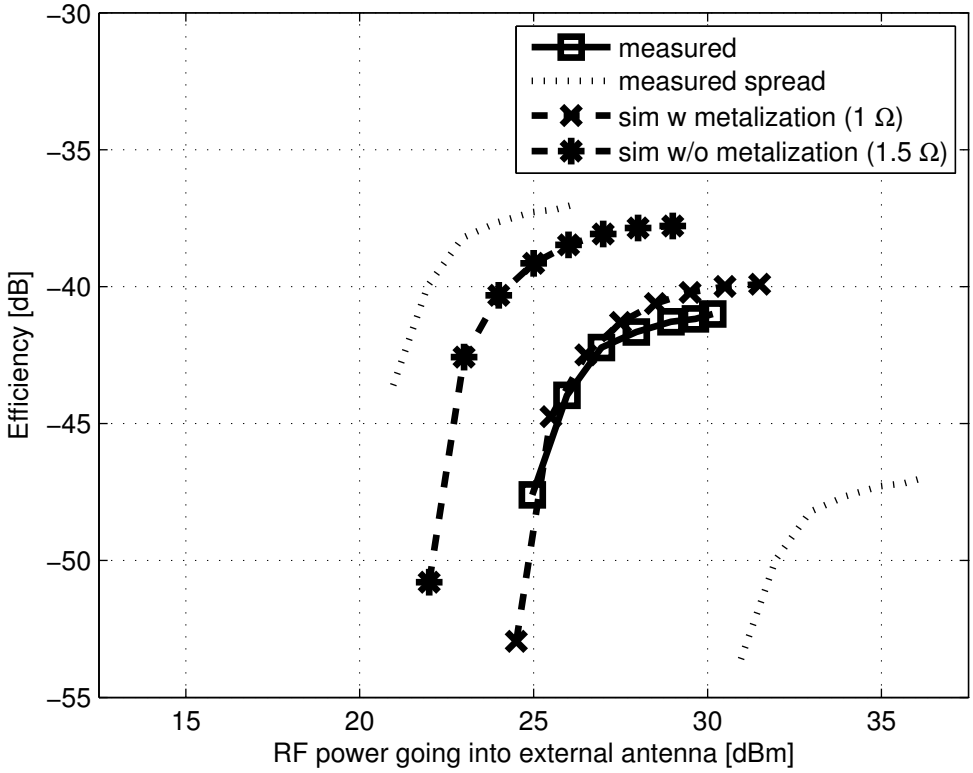


Figure 4.44: External antenna to internal DC efficiency versus power going into external antenna with extra contact resistance (pig)

are shown in fig. 4.43. It shows very similar behavior to that observed in air, with the only major difference being that the shapes of the curves for simulation and measurements are more similar in this case. This can be explained by the lower Q of the implanted antenna when surrounded by tissue reducing the effect of the extra flip-chip assembly resistance has on the shape of the curve.

Introducing the same extra resistance values as before brings the simulated curves well within the range of the measurements as shown in fig. 4.44. The fact that the results in air and animal are again very similar shows that the model of the tissue predicts its effect on the link very accurately.

Based on the efficiencies obtained under continuous operation, the expected power levels under duty-cycled operation, while adhering to SAR regulations (averaged over time), can be predicted. At 535 MHz, 53 mW and 145 mW of average power can be applied to the antenna under the 1.6 W/kg averaged over 1 g and the 2 W/kg averaged over 10 g of tissue SAR constraint, respectively. Table 4.2 summarizes the maximum DC power available at the output of the regulator assuming long enough on-times for the transient losses to become

SAR Standard	Actual Measured	Based on Best Observed Sample	Simulated w/ Metalization 0 Ω	Simulated w/o Metalization 0 Ω
1.6 W/kg over 1 g	1.6 μW	8 μW	8.5 μW	20.9 μW
2 W/kg over 10 g	9 μW	26.4 μW	27.7 μW	61.6 μW

Table 4.2: Derived maximum DC power available to the implant under duty-cycled operation

negligible and zero power during the communication phase. The values are obtained by multiplying the maximum efficiencies from fig. 4.43 with the maximum allowed average transmit power and subtracting 2.5 μW of static power. In table 4.2, "based on best observed sample" refers to the case where data from various measurements in air was taken to estimate how the best sample measured would have performed in the animal test.

The actual values might be up to a few hundred nW lower due to the increased power consumption of the synchronizer when a large input signal is present, but this depends on the actual duty cycle. The absolute error will be larger for low duty cycles. However, low duty cycles are only used when the link loss is low and the received power therefore high. Even when accounting for that and using the more stringent SAR requirement, more than 5 μW of DC power available at the regulated output needed to power a neural signal acquisition front-end are feasible based on the observed spread in performance, without resorting to a different flip-chip assembly method. The same is true when operating to support the 2 Mbps and transmitting a signal in the communication phase which is 20 dB lower than in the power phase.

It is important to note that due to the anatomy of the pig used in this experiment, the channel loss was about 0.8 dB better than the expected worst case channel loss in humans. Nevertheless, even when taken this into account, more than 5 μW of available DC power is feasible for systems implanted in humans.

4.5 Summary

The design and implementation of a 1 mm^3 implantable neural transponder system providing enough power to power a neural acquisition front-end while providing wireless connectivity at 2 Mbps without violating SAR constraints was described. Due to the low expected received power and the low antenna impedance, resulting in a low input voltage potentially severely limiting the AC-to-DC conversion efficiency, every aspect of the system had to be carefully optimized to achieve these goals.

A segmented loop antenna reducing the peak SAR and therefore allowing an increase in the externally applied power was used as the external antenna. This led to an overall increase in receive power of 47% and 8.7% at 500 MHz for the 1.6 W/kg averaged over 1 gram of

tissue and the 2 W/kg averaged over 10 gram of tissue SAR constraint, respectively. While segmenting the external loop potentially increases the link efficiency, losses in segmentation capacitors slightly decreased it. Due to the losses occurring before the signal leaving the external antenna, the applied power can be increased without violating the SAR constraint and the losses in the segmentation capacitors therefore do not reduce the maximum possible received power.

500 MHz was chosen as the optimum frequency of operation based on preliminary link simulations. In retrospect, after refining the modelling and making some changes to the implanted antenna, a slightly lower frequency of operation in the region of 300 to 400 MHz would have provided a slightly lower link loss, while simultaneously allowing to transmit more power.

An off-chip micro-PCB antenna providing significantly thicker metalization was chosen over an on-chip implementation to achieve a higher Q, increased coupling and therefore a higher input voltage. In order to keep the overall footprint of the device low and to minimize parasitics due to the interconnect, the antenna was flip-chip assembled to the CMOS die. Although a well established and mature technology, this additional processing step is an additional price to pay for the increased performance.

Duty-cycled powering was used to increase the instantaneous input voltage amplitude during rectification to overcome the low efficiencies of the AC-to-DC converter at low input voltage levels. Doing so increased the rectifier efficiency by 60% compared to continuous operation. After accounting for transient losses as well as the power consumption of additional circuitry and components needed to support the duty cycled operation, such as the synchronizer and the leakage of the storage capacitor C_{stor} and the rectifier when turned off, the overall improvement is reduced to approximately 30%, which is still significant.

The system was tested and characterized in air and in an animal. Measurements showed a large spread in performance and performance significantly worse than simulated for most of the samples. Simulation based evidence grounded in documented limitations of the assembly method and supported by measurements, suggest that the assembly method is in fact the main reason for degraded performance, the large spread observed, and the low yield experienced. Using a better controlled and more advanced assembly process would allow to bring the actual performance within the range of the simulated one while reducing the variability and enhancing the reliability at the same time.

Despite the absolute difference in overall efficiency, simulations predicted the relative change in performance between air and tissue well. Measurements and simulations for various antenna alignments and distances showed very good agreement of the relative changes in performance further proving the viability of the modelling and simulation method used.

Measurements showed that enough power to power a neural signal acquisition front-end ($> 5\ \mu W$) is definitely within reach, even with the currently used assembly method and the most stringent SAR constraint. The results of this chapter also suggest that excess power levels between 10 and 20 $\mu W$are feasible when using a better assembly process.

Chapter 5

Conclusions and Future Work

5.1 Contributions

This work represents a design framework for wirelessly powering mm-size neural implants. It outlines the link optimization process, provides guidelines for choosing the appropriate AC-to-DC converter topologies, and strategies to design the chosen converter for a given implant size. Further, it discusses implementation and testing issues and presents the design, implementation and experimental verification of a 1 mm^3 neural transponder.

Independent from that, the main contributions of this work are

- the development and verification of a modelling and simulation approach for wireless links through parts of the head
- the establishment of an optimum external antenna size - frequency of operation combination minimizing the link loss for a given implant antenna
- the identification of two families of AC-to-DC converters particularly suitable for wireless power transfer to implants
- the development of analysis and design strategies for these two types of AC-to-DC converters
- the introduction of segmented loop antennas to minimize SAR hotspots and therefore increase the maximum allowed externally applied power
- the utilization of a duty-cycled powering scheme to enhance the AC-to-DC conversion efficiency for very low received power and voltage levels
- the demonstration of the smallest remotely powered, implanted wireless transmitter for neural sensors reported to date, tested in air and in animal

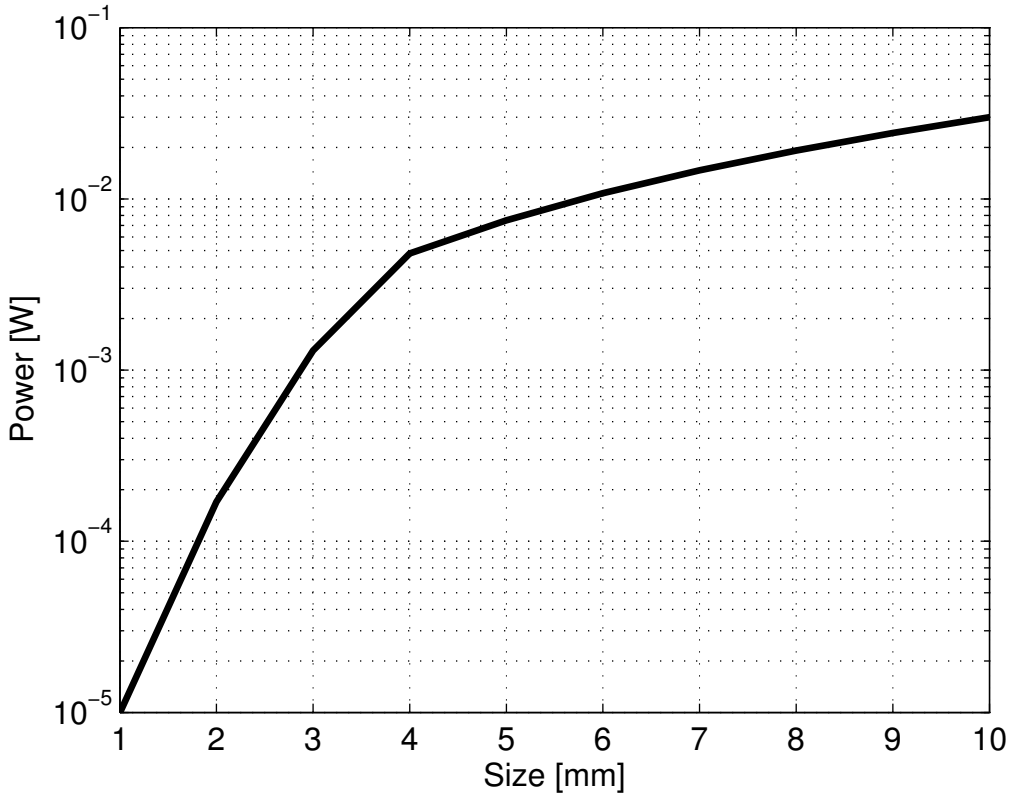


Figure 5.1: Estimated regulated DC power available for different implant sizes

While this work focused heavily on implanted applications, most of the presented work is by no means limited to the biomedical space. Much of it is also applicable to wirelessly power any mm- or below sized piece of electronics and is well suited to facilitate further miniaturization of sensor nodes.

5.2 Achievable Performance

From an electronics point of view the most important question is how much DC power does a device have at its disposal to support its functionality?

Based on the worst case channel model of 2 mm of skin, 2 mm of fat and 7 mm of air, and the observations from chapters 2, 3, and 4, the disposable regulated DC power for various implant sizes can be estimated. Figure 5.1 shows the results of this estimation.

As indicated in chapter 2, fig. 2.8, for implants of size 4 mm by 4 mm or larger, the available power is limited by the temperature increase caused by the chip dissipating that power, rather than the temperature increase caused by the E-field of the external electromagnetic

source. After accounting for losses in the matching network, the AC-to-DC and the DC-to-DC converter as well as in other auxiliary circuits, the estimated available supply power density is approximately 300 $\mu W/mm^2$ for these implants.

Smaller implants are typically limited by the channel loss and the maximum allowed external power governed by SAR restrictions. The most stringent 1.6 W/kg averaged over 1 gram of tissue imposed by the FCC was applied to derive the values shown in fig. 5.1. These values represent estimates of the maximum achievable values when operating at the maximum efficiency point of a link, assuming worst case channel loss and the most stringent SAR restrictions. Trading-off channel loss for increased transmit power as suggested in section 2.4 is one way to increase the available power above the levels shown in fig. 5.1. Another option is to design the system around one of the more relaxed SAR constraints which would provide approximately 3 times more power (table 4.1). Designing systems for average instead of worst case tissue thicknesses potentially decreases the channel loss by about 5 dB [Mark10b], hence leading to increased available power as well. The last two options highlight the need for further research in establishing unified scientifically grounded SAR limitations as well as statistical models of the physical dimensions of the various components of the human head, in order to come up with tighter boundaries on the minimum available disposable power for mm-size implants.

5.3 Room for Improvement

When designing the 1 mm^3 system significant effort has been put into optimizing every single aspect of it. At the same time, building a working proof-of-concept and testing it in a realistic scenario had the highest priority. As a result of this, some aspects of the system would have deserved more attention and, together with the lessons learned from the first prototype, optimizing them could improve the system performance even further.

Two of the most obvious possibilities for improvement are the use of a better assembly method with lower interconnect resistance, and operating the link closer to the optimum frequency of 300 to 400 MHz.

Further, performing numerical optimization of the implant antenna should be carried out to ensure the right choice of antenna. The current design was based on some heuristics such as maximizing the effective coupling area and Q and simulations comparing a few designs only. At the same time some of the design choices in the antenna were the results of working with the PCB manufacturer to end up with a design they were comfortable enough to fabricate, since building such an small antenna was pushing the limits of PCB technology as well.

A better modelling to analyze, understand and potentially optimize the effect the metalization and silicon substrate has on the link would greatly reduce the design uncertainty and allow to design the chip more precisely for the expected power and impedance levels.

Paying more attention to power lost through leakage might be a low hanging fruit. With

leakage accounting for approximately 34% of the DC power consumption of the transponder (fig. 4.33), reducing it would substantially improve the power available to the device.

Improving some of the circuits, especially the voltage reference and regulator to achieve a better PSRR that might be needed for some sensor acquisition front-ends, might be necessary for future applications and might even reduce the power consumption of some of the circuits.

5.4 Future Work

This work is more of a first rather then the final step in building miniature implantable wireless systems. There is still lot of research to be done for this to make it from the experimental stage to a viable technology for the mass market.

Purely focusing on supplying power to implants, building small and efficient external power transmitters is one important area that is crucial for the entire concept to become successful.

The development of magnetic core materials suitable for miniaturization as well as for high frequency operation would help to improve the overall link loss and therefore the power available to the implant substantially.

Beamforming might be a way to reduce SAR while simultaneously increasing the coupling and therefore worthwhile to look at. Ideally, it could increase the allowed maximum external applied power to a point where it is no longer the limiting factor. While this does not increase the power available to implants larger than 4 mm by 4 mm, it potentially increases the power available to a 1 mm by 1 mm implant by more than an order of magnitude.

Encapsulation of the implanted system in a bio-compatible package and its effect on the wireless power transfer is also something that needs to be thought of before these systems can be implanted in humans.

Studying the thermal impact of the duty-cycled operation on the tissue would be necessary to determine the exact parameters of the applied duty-cycle to make sure not to violate any health related constraints.

From a system point of view, integrating the proposed power supply systems with sensors is crucial to perform meaningful tasks and therefore an absolute necessity. While this might come with some unexpected challenges, it might also open up some opportunities such as potentially co-designing the antenna with the sensors.

With neuroscience advancing, the need for implants capable of micro-stimulating the brain will almost certainly arise. While this work focused mainly on building a power supply for sensing and communication applications, designing power supply systems supporting micro-stimulation might have constraints that are quite different from the ones for sensors only. Higher voltages, as well as higher instantaneous currents, might for example be required, and solutions providing them need to be investigated.

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