IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

JANUARY 2020
VOL. 42 NO. 1
ISSN 1077-2999

Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Chris Bailey
University of Greenwich
London, UK

"A new Decade … exciting times ahead for packaging …"

Welcome to a new decade! As I look back at previous decades and what has defined the evolution of electronics packaging, I think of through-hole technology (1960's-80's), surface mount (1990's), area array packaging (2000's) and wafer level and 3D packaging (2010's) to name a few. It makes me wonder how we will define this decade. Clearly, the electronics industry is facing both technical and economic challenges with regards system-on-chip scaling, and packaging is now seen as the key differentiator in future electronics systems. This reminds me of the 1965 paper by Gordon Moore who stated, "*It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected"*. This holds very true today and provides significant opportunities for the electronics packaging community and our society. Exciting times indeed.

As president-elect for our society over the last year, I had the opportunity to work closely with colleagues across our board of governors and those in industry to develop a strategic plan for our society for the next five years. It is a comprehensive plan with twenty-three goals and activities to achieve them. I am also delighted to state that the 2019 edition of the heterogeneous integration roadmap (HIR) recently went live with chapters detailing both challenges and potential solutions for electronics packaging over the next 5, 10 and 15 years. I would like to thank all those who helped develop the strategic plan, and to Bill Chen and Bill Bottoms for their dedication in managing the development of the roadmap across all the technical working groups who wrote each chapter. You can find both the strategic plan and the HIR chapters on our website.

After ten years serving on the board of governors, firstly as student program director, then as VP conferences, I have now reached the lofty position of president. It is a great honor to be in this position. Now every president is expected to provide a list of priorities that will define their term in office. For myself these are:

- Membership: Strengthen the value of EPS membership through new educational material and publications.
- Technical Committees: Expand our technical committee activities and support the next edition of the heterogeneous integration roadmap.
- Conferences & Chapters: Grow participation at our regional conferences and expand our chapters worldwide.
- Student Programs: Reach out to the next generation of electronics packaging engineers.

There is a tremendous amount of activity taking place within our functional teams to achieve the strategic goals set out in the plan. Helping to deliver these are our officers and directors: Jeff Suhling (VP Education), Dave McCann (VP Technology), Pat Thomson (VP Finance), Ravi Mahajan (VP Publications), Sam Karikalan (VP Conferences), Alan Huffman (VP Membership), Kitty Pearsall (PD Chapters), Eric Perfecto (PD Awards), Andew Tay (Student programs), Bill Chen (Industry Programs), Toni Mattila (PD Region 8), Yasumitsu Orii (PD region 10), Adeel Bajwa (Representative for Young Professionals), Tanja Braun (Representative for Women in Engineering), Avi Bar-Cohen (as Junior Past President), and Jean Trewhella (senior past president).

The above will be helped by our members-at-large: For the Americas—Yan Liu, Beth Keser, Xuejun Fan, Patrick McCluskey, Philip Garrou, Eric Perfecto, Pradeep Lall, Kitty Pearsall, Subramanian Iyer, and Rozalia Beica; for Region 8—Grace O'Malley, Tanja Braun and Karlheinz Bock; and for region 10—Yoichi Taira, C. Robert Kao, Chih-Pin Hung, Kishio Yokouchi, and Gu Sung Kim. For those members-at-large newly elected my congratulations and personal welcome to you all. For those returning for their second term welcome back. I look forward to working with you all over the next two years.

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NEWSLETTER SUBMISSION DEADLINES

15 June 2020 for Summer issue 2020

1 December 2020 for Winter issue 2021

Submit all material to d.manning@ieee.org

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Publications

Transactions on Components, Packaging and Manufacturing Technology

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Nominations: Avram Bar-Cohen, avi.bar-cohen@raytheon.com

Distinguished Lecturers

Program Director: Jeff Suhling, jsuhling@auburn.edu

Lecturers: Mudasir Ahmad, Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., William T. Chen, Ph.D., Xuejun Fan, Ph.D., Philip Garrou, Ph.D., Subu Iyer, PhD., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Ravi Mahajan, PhD., James E. Morris, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Jose Schutt-Aine, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Chuan-Seng Tan, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

IEEE Electronics Packaging Society Newsletter is published quarterly by the Electronics Packaging Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Electronics Packaging Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854.

Circulate your printed or PDF copy of this NEWSLETTER to co-workers.

SFI Logo

Mitsumasa Koyanagi and Peter Ramm Receive 2020 IEEE Electronics Packaging Award

Mitsumasa Koyanagi Senior Research Fellow Tohoku University Sendai, Miyagi, Japan

Peter Ramm Head of Strategic Projects Fraunhofer EMFT, Bavaria, Germany

"For pioneering contributions leading to the commercialization of 3D wafer and die level stacking packaging."

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

Mitsumasa Koyanagi's and Peter Ramm's efforts in developing, demonstrating, and commercializing 3D integrated circuit (3DIC) integration processes have played a key role in enabling ever-smaller yet more-powerful devices especially important to mobile communications. 3D integration and packaging involves stacking silicon wafers and interconnecting them vertically so that they behave as a single device, which achieves performance at reduced power and with a smaller footprint than conventional 2D processes. Koyanagi succeeded in fabricating 3D stacked image sensor, 3D stacked memory, and 3D stacked microprocessor test chips using through-silicon vias (TSVs) for the first time. He also demonstrated a four-layer stacked image sensor with quarter video graphics array resolution, a four-layer stacked multicore processor, and a four-layer stacked heterogeneous image sensor with extremely high frame rate. Ramm developed and patented 3D integration approaches with particular focus on die-to-wafer stacking, using low-temperature bonding and vertical integration of IC devices with TSVs, and demonstrated a complete industrial 3DIC integration process. He also published results on key processes such as 3D metallization including robust IMC interconnections and on advanced sensor applications of 3D heterogeneous integration.

An IEEE Life Fellow, Koyanagi is a Senior Research Fellow at Tohoku University, Sendai, Miyagi, Japan.

An IEEE Senior Member, Ramm is the head of Strategic Projects at Fraunhofer EMFT, Munich, Bavaria, Germany.

The 2020 Award will be presented at the 70th Electronic Components and Technology Conference (ECTC), May 2020.

Mitsumasa Koyanagi and Peter Ramm join the following past recipients of this Award.

2019—Ephraim Suhir
"For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems."

2018—William Chen
"For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping."

2017—Paul Ho and King-Ning Tu
"For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration."

2016—Michael Pecht
"For visionary leadership in the development of physics-of-failure-based and prognostics-based approaches to electronic packaging reliability."

2015—Nasser Bozorg-Grayeli
"For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems."

2014—Avram Bar-Cohen
"For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling."

2013—John Lau
"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."

2012—Mauro J Walker
"For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations."

2011—Rao R. Tummala
"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010—Herbert Reichl
"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009—George G. Harman
"For achievements in wire bonding technologies."

2008—Karl Puttlitz Sr. and Paul A. Totta
"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages."

2007—Dimitry Grabbe
"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

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New Appointments for 2020

The Electronics Packaging Society Board of Governors appointed its Officers and Program Directors for the two-year term of 1 January 2020 through 31 December 2021. The following individuals were appointed:.

PRESIDENT

CHRIS BAILEY is Professor of Computational Mechanics and Reliability at the University of Greenwich, London, United Kingdom. I received my PhD in Computational Modelling from Thames Polytechnic in 1988, and an MBA in Technology Management from the Open University in 1996. Before joining Greenwich in 1991, Chris worked for three years at Carnegie Mellon University (USA) as a research fellow in materials engineering.

One of Chris's main achievements with regards to EPS was helping to establish the Region 8 flagship conference ESTC (Electronics System-integration Technology Conference). He was the Programme Chair for the first conference held in Dresden, and was the General Chair for the 2008 conference in London. In 2007 he was the local chair for the IEEE EPS sponsored EuroSime conference held in London, and since 2009 has worked with the EuroSime team as co-editor of the proceedings and track chair for multi-physics modelling.

Since 2010 Chris has served as a member of the EPS Board of Governors. During his first term on the BoG, he also took on the role of Strategic Director for Student Programs with the aim of supporting students involved in EPS activities worldwide. Particular achievements include arranging financial support for student attendees at the International Spring Seminar on Electronics Technology (ISSE) as well as promoting student membership at events such as ECTC, EPTC and ESTC.

Other EPS activities that Chris has been involved with include membership of technical committees for EPTC (Singapore), Eurosime (Europe), ISSE (Europe) and ICEP/HDP (China) where he is a regular attendee and presenter. He has also worked closely with others in Europe to help promote closer co-operation between EPS and IMAPS for the benefit of the whole community.

His research has resulted in over 250 publications. He is currently an Associate Editor for the EPS Transactions and has been a guest editor on the journal of Soldering and Surface Mount Technology. He is also a committee member of the Innovative Electronics Manufacturing Research Centre (IeMRC) in the UK and has participated in a number of UK Government sponsored overseas missions to promote collaboration and review electronic packaging technologies. Recently he became a member of the working group writing a new IEEE standard for Prognostics and Health Management for Electronic Systems.

VICE PRESIDENT, TECHNOLOGY

DAVID MCCANN (M'89) I am supporting the integration of GlobalFoundries ASIC business into Marvell and am based in Malta, New York. In the ASIC business, I was responsible for external supply for wafers through package shipment and for package and test development. Prior to the ASIC business. I was responsible for GlobalFoundries worldwide interconnect and packaging technology development, wafer bump and test factories, and outsourced (OSAT) strategy and operations performance. I have been in GlobalFoundries and Marvell for a combined 8 years. Prior to this, I was VP of the Flip Chip Business Unit at Amkor Technology in Chandler, AZ, where I was responsible for the business and technology development of flip chip and other advanced technologies for high performance product applications. This required significant time spent in Asia in the bump/assembly/test factories and with customers building relationships that enabled the technology development and business to follow. I worked at Amkor for 10 years. Prior to Amkor, I worked at Biotronik in Portland, OR for 10 years in different roles including Technology Development, Process Engineering, Product Engineering, and Production on pacemakers and implanted defibrillators. Prior to Amkor I worked at Bipolar Integrated Technology and American Microsystems. Throughout my career, my focus has been the intersection of technology and business.

Educational background: MS Engineering Management, 1985, Santa Clara University; BS Ceramic Engineering, 1981, University of Illinois.

EPS-related activities include: EPS Technology VP-elect: 2020–2021; EPS BoG ECTC Steering committee: 2018-current; EPS BoG Member at large: 2018–2019; ECTC Sponsorship Chair: 2013–2016; ECTC General Chair: 2012; ECTC ExComm: 2008–2014; ECTC Interconnect Chair: 2005–2006; ECTC Interconnect Committee: 1998–2010, 10 year service recognition; Chair and participant in various ECTC panels and sessions 2002–2015.

Beyond the ECTC ExComm responsibilities, I focused on improving the operating procedures and clarity of roles in executive committee and documenting roles for each ExComm role. The roles enable maintaining the advantages of job rotation while minimizing the risk of gaps, and ensuring we have a path to continue to update "organizational learning" and pass it on. Later, I took on Sponsorships, increasing Sponsorship support from $25k to $200k and from ~7 companies to ~25 companies, increasing the margin of safety on conference finances. More recently I have focused on supporting the ECTC Steering Committee and in helping to improve the EPS Technical Committees and defining the future vision of the TC's.

VICE PRESIDENT, CONFERENCES

SAM KARIKALAN (M: 1995, SM: 2003) has 32 years of experience in the Semiconductor and Electronic Systems Industry. He is currently a Senior Manager of Package Engineering R&D at Broadcom Inc., responsible for Electrical, Thermal and Mechanical design analysis and optimization of IC Packages, Advanced Packaging Technology Pathfinding, and co-design of IPs and Systems. Prior to Broadcom, Sam held technical or managerial positions at STATS ChipPAC, Primarion and Advanced Micro Devices, working on IC Package Design for Signal/Power Integrity and Electromagnetic Compatibility (EMC). Before entering the semiconductor industry in 1998, Sam was a scientist at SAMEER-Centre for Electromagnetics

in India, for over a decade, working on EMI/EMC Research & System Design and Radar technology. His current interests include Heterogeneous Integration Technologies, Design for Performance & Reliability, and Design for Test & Manufacturing.

Sam has 23 issued US patents to his credit, on Interconnect design, 2.5D/3D Packaging and EMI/EMC. He also has authored/co-authored 14 Conference/Journal papers on IC Packaging, Signal Integrity and EMI/EMC and delivered few hundred hours of training lectures on Signal/Power Integrity and EMI/EMC at locations all across the globe, including two PDCs at the IEEE Electronic Components and Technology Conference (ECTC). Sam holds a B.E. degree in Electronics & Communications Engineering from Bharathiar University, Coimbatore, India.

Sam has been a member of the IEEE for over 20 years. He has been very active in local chapters and sections in Singapore, Phoenix and Orange County (California), in various leadership roles, including the founding chairperson of the CPMT Orange County chapter. Sam has received several awards for his contributions to the IEEE, including the 2014 IEEE CPMT Regional Contributions Award—Regions 1-6, 7, 9 (US, Canada, Latin America) and the 2012 Outstanding Leadership Award from the Orange County Section. Sam has been serving on the Technical Program Committee and the Executive Committee of the IEEE ECTC since 2006. Sam was the General Chair of the 2018 IEEE 68th ECTC.

VICE PRESIDENT, PUBLICATIONS

RAVI MAHAJAN is an Intel Fellow and the Co-director of pathfinding and assembly and packaging technologies for 7-nanometer (7 nm) silicon and beyond in the Technology and Manufacturing Group at Intel Corporation. He is responsible for planning and carrying out multi-chip package pathfinding programs for the latest Intel process technologies. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives.

Ravi has led efforts to define and set strategic direction for package architecture, technologies and assembly processes at Intel since joining the company's Assembly and Test Technology Development organization in 2000, spanning 90 nm, 65 nm, 45 nm, 32 nm, 22 nm and 7 nm silicon. Earlier in his Intel career, he spent five years as group manager for thermal mechanical tools and analysis. In that role, Mahajan oversaw a Thermal-Mechanical Lab chartered with delivering detailed thermal and mechanical characterization of Intel's packaging solutions for current and future processors.

A prolific inventor and recognized expert in microelectronics packaging technologies, Mahajan holds more than 30 patents, including the original patent for a silicon bridge that became the foundation for Intel's Embedded Multi-Die Interconnect Bridge technology. His early insights also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation. Ravi has written several book chapters and more than 30 papers on topics related to his area of expertise.

Ravi joined Intel in 1992 after earning a bachelor's degree from Bombay University, a master's degree from the University of Houston, and a Ph.D. from Lehigh University, all in mechanical engineering. His contributions during his Intel career have earned him numerous industry honors, most recently the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI award from SEMITHERM and the 2016 Allan Kraus Thermal Management Medal from the American Society of Mechanical Engineers. He has also been nominated as an IEEE EPS Distinguished Lecturer. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently Co-Editor for Special Topics of IEEE T-CPMT. Additionally he has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was named an Intel Fellow in 2017.

VICE PRESIDENT, EDUCATION

JEFFREY C. SUHLING received a B.S. degree in Applied Mathematics and Physics, and M.S. and Ph.D. degrees in Engineering Mechanics from the University of Wisconsin, Madison, WI. He joined faculty of the Department of Mechanical Engineering at Auburn University in 1985, where he currently holds the rank of Quina Distinguished Professor. Dr. Suhling co-established the NSF Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3) in 1998, and served as Center Director from 2002–2008. CAVE3 is a government and industry sponsored research center involving over 20 member companies, 15 faculty, and 35 graduate students that specializes in reliability of electronic packaging in harsh environments. In 2008, he was appointed Department Chair of the Department of Mechanical Engineering, which is the largest program at the University with over 1000 undergraduate students and 150 graduate students. He was selected "Outstanding Mechanical Engineering Faculty Member" by the undergraduate students during 1990, received the College of Engineering Birdsong Superior Teaching Award in 1994, and received the College of Engineering Senior Research Award in 2001. He has advised 75 graduate students at Auburn University, including 27 Ph.D. students and 48 M.S. students.

Dr. Suhling has been an active researcher in electronic packaging for over 25 years. His general areas of interest are in the mechanics and reliability of packaging. Specializations include silicon sensors for packaging stress and temperature measurements, stress effects in silicon devices, test chips, mechanical characterization of packaging materials including solders and polymers, solder joint reliability and aging effects, and finite element modeling. He has authored or co-authored over 375 technical publications, including 6 books and book chapters, 55 journal articles, and 325 conference proceedings papers. Six of his conference papers have been selected as the Best of Conference. These include Best Session Paper Awards at the 2005 and 2010 ECTC Conferences, as well as Best Paper Awards at the 1998 and 2002 IMAPS Annual Conferences, 2008 SMTA International, and 2013 InterPACK Conference. In addition, he and his co-authors have received Best Poster awards at the InterPACK 2007, InterPACK 2009, and InterPACK 2013 conferences.

Dr. Suhling is a member of IEEE/EPS, ASME, IMAPS, and SMTA. In IEEE, he has served on the ECTC Applied Reliability

program committee for the past 10 years. He was appointed to the ECTC Professional Development Course (PDC) program committee in 2006, and has served as Assistant Chair. He has also been active in the IEEE/EPS ITHERM Conference series, serving on the program committee for over 10 years. In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division (EPPD) during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the InterPACK '07 Conference, and General Chair of the InterPACK '09 Conference. He was elected a Fellow of ASME in 2009, and was recognized with the ASME-EPPD Mechanics Award for outstanding contributions to electronic packaging research. Jeff has served as a member of the EPS Board of Governors since 2014 and as Program Director—Membership Programs from 2016–2018.

VICE PRESIDENT, MEMBERSHIP

ALAN HUFFMAN (M: 2005, SM: 2007) is currently the Director of Engineering for Micross Advanced Interconnect Technology in Research Triangle Park, NC. He received the B.S degree in physics from The University of North Carolina at Chapel Hill in 1994. From 1994 to 2005 he was a Member of the Technical Staff at MCNC Research & Development Institute working on development and implementation of wafer level packaging technologies, reliability and failure mode analysis of flip chip devices, and optoelectronic and MEMS packaging. In 2005, he joined RTI International and was a Senior Research Engineer and Program Manager for WLP technology with RTI's Electronics and Applied Physics Division. His technical interests include wafer level packaging and flip chip process technology and fine pitch bump interconnect, 2.5D and 3D integration technology, characterization and process development for electronic materials used in WLP. He has authored or co-authored numerous papers and presentations on a number of advanced packaging topics, particularly on high density interconnect technologies and characterization of polymer material processes.

Alan is an IEEE Senior Member whose activities include, member of ECTC Interconnects technical sub-committee from 2005–2013, Chaired multiple ECTC technical sessions during this period, member of ECTC Executive Committee 2011-present, 2016–17—Jr. Past General Chair, 2015–16—General Chair, 2014–15—Vice General Chair, 2013–14—Program Chair, 2012–13—Asst. Program Chair, 2011–12—Web Administrator. Alan was appointed to the EPS Board of Governors in 2016 and has been a contributing member of the Board through various adhocs including Branding Change, Membership and Conference Functional Teams.

VICE PRESIDENT, FINANCE

PATRICK THOMPSON (M'87, SM'92) earned his BS, MS and PhD degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 25 years of experience in advanced packaging research, development and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication and packaging, flip chip on board and chip scale packages, to multi-chip packaging, MEMS, optoelectronic packaging, and high performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors , and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads fine pitch Cu pillar interconnect and TSV packaging technology development.

Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Technology Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and continues to serve as Financial Chair. He has served at both the local and Society level of EPS holding positions including Member-at-Large of the Board of Governors, Administrative Vice President, and Vice President of Technology.

PROGRAM DIRECTOR, CHAPTER PROGRAMS

KITTY PEARSALL (AM'84-M'01-SM'02) received the BS degree in Metallurgical Engineering (1971) from the UT El Paso. Kitty received the MS and Ph.D. degree in Mechanical Engineering and Materials from the UT Austin in 1979 and 1983 respectively. Kitty worked for IBM from 1972 to 2013. In 2005 Kitty was appointed an IBM Distinguished Engineer and was elected to the IBM Academy of Technology. Kitty was a process consultant and subject matter expert working on strategic initiatives impacting component qualification and end quality of procured commodities. She engaged with worldwide teams implementing cross-brand, cross commodity processes/products that delivered high quality/high reliability end product.

Kitty received 4 IBM Outstanding Technical Achievement Awards; holds 9 US patents; 2 patents pending; and 8 published disclosures. She has numerous internal publications as well as 22 external publications in her field. Kitty is a licensed Professional Engineer (Texas since 1993). Kitty was the recipient of the UT Austin—Cockrell Engineering Distinguished Engineering Graduate Award in 2007 followed by induction into the UT Mechanical Engineering Dept. Academy of Distinguished Alumni in 2008. Kitty was awarded the Women in Technology Fran E. Allan Mentoring Award (2006) in recognition of her people development both in and outside of IBM. Currently Kitty is President of Boss Precision Inc. and works as an Independent consultant. This has included a one year engagement with Shainin Corporation.

Kitty is an active member in IEEE and CPMT. She is a member of TMS, American Society of Metals, and WIE. Kitty has more than 22 years' experience with ECTC serving as a member of the ECTC Manufacturing Technology Committee (1993–2013) and as the Professional Development Course Chair since 2006. During Kitty's 10 years on the CPMT Board of Governors she has served in many roles: Member at Large, Strategic Awards Director, VP of Education and currently Director of Chapter Programs. In each role Kitty made key contributions.

Kitty introduced the Regional Contribution Awards. She established the baseline for the CPMT Distinguished Lecturer's (DLs) Program. The history of the DLs presentations to Universities, Research Centers, Conferences and CPMT Chapters was charted to determine if the program was meeting its founding principal; i.e., primarily supporting the CPMT chapters. Review of the data noted that this was not the case. Therefore Kitty focused on increasing Chapter usage which did improve over time. DL Budget tracking of planned versus actuals was initiated. Lastly, Kitty documented the roles and responsibilities of the VP Education and passed these on to the new VP. As Director of Chapter Programs Kitty is focusing on worldwide Chapter Communication as well as ensuring Chapters know their benefits and how to access them. First deliverable was a Worldwide Chapter Communication Survey highlighting best practices amongst them.

PROGRAM DIRECTOR, AWARD PROGRAMS

ERIC PERFECTO (M'95, SM'01, F'17) has 37 years of experience working in microelectronics. First at IBM working in the development of multi-level Cu-polyimide advanced packages for high-end systems, followed by the development of the UBM and Pb-free solder processes and yields for flip chip in 2D and 3D packages. As part of the IBM Microelectronics Division divestiture, Eric moved to GLOBALFOUNDRIES where he established a Si Photonics packaging assembly line. He returned to IBM Research at Albany working on heterogeneous integration packaging. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College.

An author of 79 technical papers and three book chapters, Eric received two Best Conference Paper Awards (ESTC and ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards, and an IBM Outstanding Contribution Award for the development of 3D wafer finishing process (2014).

Eric served as the 57th ECTC General Chair, the 55th ECTC Program Chair, the ECTC Materials and Processes Subcommittee Chair ('02–'03). He is the current ECTC Publicity chair. For the last 9 years, Eric's popular Flip Chip Fabrication and Interconnection course has been given at ECTC to great reviews. He is an IEEE Fellow, and has achieved IMAPS and SPE senior membership.

Since 2008, Eric has been elected four times BoG member to the IEEE Electronics Packaging Society (EPS, previously CPMT). For 3 years he served as the EPS Strategic Director of Global Chapters and Membership where he focused on enhancing the EPS membership value. Through his efforts, the CPMT Transactions are now part of the EPS membership. He also highlighted the importance of technical content in the EPS members-only page, where now webinars and presentations can be found. He has served as an Associate Editor for the CPMT Transactions and member of the EPS Technical Committee on Materials and Processes. For the last 6 years, Eric has chaired the EPS Awards Committee responsible for the EPS Mayor Awards, the Regional Awards, the PhD Fellowship, the ECTC Student Travel Awards and the ECTC Volunteer Award. At a local level, Eric is the membership Chair of the Mid-Hudson IEEE Section.

PROGRAM DIRECTOR, STUDENT PROGRAMS

ANDREW TAY (M'91) is currently a Senior Research Fellow at the Singapore University of Technology and Design. Prior to this he was a Professor in the Department of Mechanical Engineering, National University of Singapore (NUS). He obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include thermo-mechanical failures, thermal management of electronics and EV battery systems, reliability of solar photovoltaic modules and fracture mechanics. To date he has published more than 250 technical papers, 4 book chapters, 7 keynote presentations, 11 invited presentations, 3 panel discussions, and co-edited 4 conference proceedings and two special issues of technical journals.

Dr Tay was the inaugural General Chair of the 1st and 2nd Electronics Packaging Technology Conference (EPTC) in 1997 and 1998. Since then, he has been in the organising committee of EPTC. In 2006 he was appointed the inaugural Chairman of the EPTC Board, charged with steering the development of EPTC, and is currently again serving as its Chairman. He has been in the Executive Committee of the Singapore Joint Reliability/CPMT/ED Chapter since 2000 and was its Chairman from 2010–2011. He has been involved in the international advisory boards and program committees of more than 108 electronics packaging conferences worldwide including DTIP, ECTC, EMAP, EPTC, EuroSimE, HDP, ICEPT, IEMT, IMPACT, InterPack, ITHERM and THERMINIC.

Dr. Tay was an Associate Editor of the *ASME Journal of Electronics Packaging*, an editorial board member of several journals including *Microelectronics Journal* and *Finite Elements in Analysis and Design*, and a guest editor of a special issue on *Microelectronics Reliability*.

He has contributed significantly as a member of the IEEE EPS Education Committee from 1998 to 2007 where he helped to evaluate projects on web-based educational modules.

From 1998 to 2005, he coordinated the implementation of the Specialized Manpower Program in Electronics Packaging and Wafer Fabrication which was funded by the Singapore Economic Development Board. He has taught many professional short courses at packaging conferences. He has been awarded competitive research grants exceeding $14 Million for electronics packaging projects.

He has received the following major awards: 2012 IEEE EPS Exceptional Technical Achievement Award, 2012 IEEE EPS Regional Contributions Award, 2004 ASME Electronics & Photonics Packaging Division Engineering Mechanics Award, 2000 IEEE Third Millennium Medal, 2000 Special Presidential Recognition Award.

He has been an IEEE member since 1991, an ASME member since 1993, an ASME Fellow since 2004 and a Fellow of the Institution of Engineers (Singapore) since 2004.

PROGRAM DIRECTOR, INDUSTRY PROGRAMS

WILLIAM T. CHEN (M'92, SM'03, F'06) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Corporation at Endicott New York in 1963.

At IBM he worked in a broad range of IBM microelectronic packaging products. He received IBM Division President Award for his leadership and innovation in Predictive Modelling on IBM products. He was elected to the IBM Academy of Technology for his contributions to IBM Products and Packaging Technologies. He retired from IBM in 1997. He joined the Institute of Materials Research and Engineering (IMRE) in Singapore, to initiate research in microelectronic packaging materials and processes. He was appointed to the position Director of the Institute (IMRE) steering the growth in people, funding and research facilities and research direction for IMRE to become the leading materials science and engineering research center in the ASEAN region. In 2001 he joined ASE Group, where he holds the position of ASE Fellow and Senior Technical Advisor. In this assignment he has responsibilities for guidance to technology strategic directions for ASE Group.

He is Senior Past President of the IEEE/CPMT Society. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap Technical Working Group. He is chair of the Semicon West Packaging Committee. He has been elected to a member of the iNEMI Board. He is a member of the Technology Committee of GSA.

He has been elected to Fellow of IEEE and Fellow of ASME. He has served as an Associate Editor of ASME Journal of Electronic Packaging, and IEEE/CPMT Transactions.

PROGRAM DIRECTOR, REGION 8 PROGRAMS

TONI MATTILA (M'08) is a research scientist and docent at Aalto University in Helsinki, Finland where he leads a research team that focuses on the reliability of electronic devices. He received his Ph.D. degree in electrical engineering in 2005 and an M.Sc. degree in materials science and engineering in 1999 from the Helsinki University of Technology (HUT). Since 1996, he has been working with electronics production technologies and reliability of electronic devices both in industrial and academic settings. Before joining HUT in 1999 he worked in Tellabs and Nokia.

Toni's research has focused on electronics production technologies, soldering in electronics, failure mechanisms of electronic assemblies, MEMS technologies, and the development of improved methods for reliability assessment and lifetime prediction. Within the framework of his research Toni has been working in close co-operation with international electronics industry, research institutions and universities. His research has so far resulted in over fifty publications in scientific and technical journals and conferences. In addition, Toni has authored seven book chapters, held several professional tutorials during conferences and been a frequent speaker at conferences, seminars and technology fairs. He is also a frequent reviewer in several scientific journals, including CPMT Transactions.

Since 2008, Toni has been Chairman of the CPMT Finland Chapter. During this time he has, together with other board members, developed and revitalized local activities. More than 100 people attend seminars and events organized by the CPMT Finland chapter annually. He has also established firm connections between the CPMT chapters in Scandinavia. Toni is currently an elected member of the Board of Governors of the CPMT.

Toni also works actively in the IEEE Finland Section, where he has been a member of the executive committee since 2008, and served in various positions. Other IEEE activities include, for example, a membership of technical committees for all three Electronics System Integration Technology Conferences (ESTC). In the past he has also acted in several other positions of trust. For example, he has been the chairman of a housing association for ten years.

PROGRAM DIRECTOR, REGION 10 PROGRAMS

YASUMITSU ORII (M'12) received the B.S. in Material Science from the Osaka University, Japan and the Ph.D. from the Osaka University, Japan as well.

Dr. Yasumitsu Orii joined IBM Japan in 1986 and is a leading expert on Flip Chip organic packages, which have contributed to the performance improvements and miniaturization of such products as servers, laptop computers, and HDDs. The packaging technology is becoming more important for next generation server products as Moore's Law reaches its limits. His flip chip expertise extends into many related areas. Initially, he was a pioneer of flip chip on FPC (Flexible Printed Circuit) for HDDs, which allowed the read/write amplifier ICs to be mounted on the suspension and much closer to the GMR head. Later, he developed the C2 (Chip Connection) technology that supported low-cost 50-μm-pitch flip chip bonding for the commodity consumer electronics market and it was licensed to a company in Taiwan.

Currently he is a senior manager of IBM Research Tokyo Science & Technology division and a Senior Technical Staff Member as well as IBM Academy member is leading the next generation flip chip organic package, 3D-IC projects and Neuromorphic Computing at IBM Research Tokyo for IBM Servers and creating new technologies under a Joint Development Program involving many leading Japanese materials companies.

Dr.Yasumitsu Orii has served co-chair of IEEE EPS High Density Substrates & Boards and ECTC CPMT Seminar since 2015 and he is the board member of IEEE EPS Japan Chapter. And he has contributed to ICSJ(IEEE EPS Symposium Japan) as an invited speaker since 2012.

He received Best Paper Award at the 2008 ICEPS (International Conference on Electronics Packaging) , Outstanding Paper Award at the IMPACT 2011, JIEPS Annual Best Paper award in 2011, IMAPS Sidney J. Stein International Award in 2012, JIEPS Annual technical award in 2014 and IMAPS Fellow award in 2015. And he had been the chair of Technical Program Committee in ICEPS 2009–2011 responsible for technical program editing and paper selection. He was the general chair of ICEP-IAAC(IMAPS All Asia Conference) 2012 in Tokyo.

Newly-Elected and Appointed Members of the Electronics Packaging Society Board of Governors

In 2019, EPS members elected new Members- at-Large to the EPS Board of Governors for the three-year term of 1 January 2020 through 31 December 2022.

REGIONS 1-6, 7 & 9

ROZALIA BEICA (M'07) is currently Global Director Strategic Marketing with DuPont. In her current role, Rozalia leads strategic marketing activities across Electronics & Imaging Division. She is working with the Business and Senior Leaders to drive strategy planning, investor relations, strategic marketing and thought leadership activities.

She has 27 years of international working experience across various industries, including industrial, electronics and semiconductors. For 20 years, she was involved in the research, applications and strategic marketing of Advanced Packaging technologies, with global leading responsibilities at specialty chemicals (Rohm and Haas Electronic Materials), equipment (Semitool, Applied Materials and Lam Research) and device manufacturing (Maxim IC). Prior to joining DuPont, Rozalia was the CTO of Yole Développement where she led the market research, technology and strategy consulting activities for Advanced Packaging and Semiconductor Manufacturing.

Her passion and hardworking nature, collaboration and commitment have helped her stay at the top of several assignments she has undertaken, either at school, work or industry events, earning her many awards through the years, including:

- 2013 Aphelion Energy Co-founder: project focused on providing renewable energy to rural communities without electricity in Africa. Received "The Entrepreneurship Project of the Year—IE University" and "#1 Entrepreneurship Project" at International Venture Day Fudan University, Shanghai, China
- 2011 & 2012 Applied Materials: "Technical and Customer Excellence Achievement Award" (2011) and "President's Quality Award Honorable Mention for TSV team" (2012) for contribution to the advancements in 3D Interconnect
- 2006 R&D 100 Award for development of lead-free ternary alloy electrodeposition for wafer bumping
- 2006—Congratulatory Letter for Ternary Alloy (SnAgCu) Development from Dr. Paul Totta (IBM Fellow)
- 2002 Dale Carnegie: several awards including 'The Highest Achievement award"

Throughout her career, Rozalia has been actively supporting industry activities worldwide: Program Director of EMC3D Consortia, General Chair of IMAPS Device Packaging and Global Semiconductor and Electronics Forums, Technical Advisory Board Member at SRC, Member of the Executive Committee of ECTC, IMAPS SiP, ISQED, ESTC and member of several committees worldwide (ITRS, IWLPC, EPTC and EPS). Current industry involvements include ECTC Program Chair, HIR WLP Chair, IMAPS VP of Technology, Technical Chair IMAPS Advanced SiP USA, Technical Chair SiP China Symposium, and Advisory Board Member of 3DinCites and IMPACT Taiwan. She has over 150 presentations and publications (including three book chapters on 3D IC technologies), several keynotes, invited presentations and panel participations.

Rozalia has a M.Sc. in Chemical Engineering from Polytechnic University "Traian Vuia" (Romania), a M.Sc. in Management of Technology from KW University (USA), and a Global Executive MBA from Instituto de Empresa Business School (Spain).

SUBRAMANIAN (SUBU) IYER (S'76-M'81-SM'88-F'95) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is Director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45 nm technology node used to make the first generation of truly low power portable devices. He also was among the first to commercialize bonded SOI for CMOS applications through a start-up called SiBond LLC. More recently, he has been exploring new packaging paradigms and architectures that they may enable including in-memory analog compute. He has published over 300 papers and holds over 70 patents. He was a Master Inventor at IBM. He has received several outstanding technical achievements and corporate awards at IBM. He is an IEEE Fellow, an APS Fellow and a Distinguished Lecturer of the IEEE EDS and EPS as well as the treasurer of EDS and a member of the Board of Governors of IEEE EPS. He is also a Fellow of the National Academy of Inventors. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012.

Statement of Interest: I am interested in helping ensure a sound strategy for packaging in general, and IEEE EPS specifically. I am also interested in developing a solid interdisciplinary educational program for our young engineers so they can contribute to Electronics Packaging. I am also interested in good branding approach for EPS and packaging in general. I believe that deep collaboration with our sister societies in IEEE and allied professional societies is crucial for our continued well-being.

KATHERINE (KITTY) PEARSALL (AM '84-M'01-SM'02) received her BS degree in Metallurgical Engineering (1971) from University of Texas at El Paso. Kitty received the MS and PhD degree in Mechanical Engineering and Materials from the University of Texas Austin in 1979 and 1983 respectively. Kitty worked for IBM from 1972 to 2013. In 2005, Kitty was appointed an IBM Distinguished Engineer and was elected to the IBM Academy of Technology. Kitty was a process consultant and subject matter expert working on strategic initiatives impacting component qualification and end quality of procured commodities. She engaged with WW teams implementing cross-brand, cross commodity processes/products that delivered high quality/high reliability end product.

Kitty received many IBM Outstanding Technical Achievement Awards; holds 12 US patents; and 8 published disclosures. She

has numerous internal publications as well as 22 external publications in her field. Kitty is a licensed Professional Engineer (Texas since 1993). Kitty was the recipient of the UT Austin—Cockrell Engineering Distinguished Engineering Graduate Award in 2007 followed by induction into the UT Mechanical Engineering Dept. Academy of Distinguished Alumni in 2008. Kitty was awarded the Women in Technology Fran E. Allan Mentoring Award (2006) in recognition of her people development both in and outside of IBM. Currently Kitty is President of Boss Precision Inc. and works as an Independent consultant. This has included a one year engagement with Shainin Corporation.

Kitty has been an active member in IEEE for 31 years as well as an EPS/CPMT member for 26 years. Kitty just received her 25-year Volunteer award at the 2019 ECTC. She has served as a member of the ECTC Manufacturing Technology Committee (1993–2013); ECTC Professional Development Course Chair since 2006. She just completed her tenure as Chair of the IEEE EPS Field Award Committee and is the past Award Chair for the next 2 years. During Kitty's 14 years on the EPS/CPMT Board of Governors Kitty has served in many roles: Member at Large, Strategic Awards Director, VP of Education, and currently Director of WW Chapter Programs as well as a BoG Member-at-Large. In each role, Kitty has made key contributions. She is also a member of the American Society of Metals, IEEE WIE, and a life member of TMS.

REGION 8

KARLHEINZ BOCK (M'96-SM'17) Since 2014 Karlheinz Bock has served as Professor and chair of Electronics Packaging and director of the Institute of Electronics Packaging (IAVT) at the TU Dresden.

Since 2008, he has served as a Professor of Polytronic Microsystems at the faculty of Communication and Electronics Engineering at the University of Berlin. He earned his Diploma on electrical and communication engineering from the University of Saarbrücken, Germany in 1986 and his Dr.-Ing. (Ph.D.) for RF microelectronics from the University of Darmstadt, Darmstadt, Germany in 1994. From 1996 to 1999, he worked in the materials packaging and reliability department of IMEC vzw. in Leuven Belgium. He received the "Japan Society for Promotion of Science (JSPS) Award" in 1994 for his PhD thesis and worked as post-doc from 1994 to 1995 at the Tohoku University in Sendai, Japan. In 2012, he received the Doctor Honoris causa of the Polytechnical University of Bukarest in Romania for his work on Heterosystem Integration.

He served in the Fraunhofer Gesellschaft, from 2001 until 2014 where he has been employed as head of the Polytronic and Multifunctional Systems department at the Fraunhofer Institute for Reliability and Microintegration (IZM, Munich branch, from 2010 named EMFT) and as deputy director from 2006 until 2010 of IZM and from 2010 until 2012 as acting director of EMFT. Focus of his work is on electronics packaging and reliability, and 3D heterointegration and additive manufacturing of systems; thin silicon and flexible electronics; reliability characterization, failure analysis and condition monitoring; self-assembly and self-alignment; flexible and organic electronics—Polytronics; MEMS packaging; system integration for biosensors and medical electronics, in-particular smart skin and implantable devices.

Karlheinz Bock has contributed to 290 publications and 22 patents. He co-authored more than 16 best paper awards. (see Google Scholar and Research Gate). He is engaged in developing the technological community of 3D systems, heterosystem integration and packaging, organic, and flexible electronics. He served in several IEEE activities i.e. as IEEE EPS vice technical chair from 2016–2018 and as technical chair for emerging technology since 2018, where he proposed and organized the 2019 IEEE EPS future vision contest for young engineers. He served as member of the TPC of IEEE ECTC for emerging technologies (ET) since 2008 and as vice chair ET 2011 and TPC chair ET 2012; as member of IEEE IEDM since 2008 on TPC for display sensors MEMS (DSM) and as chair of DSM TPC in 2010; as the European arrangements co-chair 2011, chair 2012 of IEEE IEDM executive committee; served on the ESTC TPC since 2012, as programm chair of ESTC 2016 in Grenoble and as general chair of ESTC 2018 in Dresden; since 2010 on the TPC of Plastic Electronics and 2012–2017 of FlexTech; since 2013 as session organizer for additive manufacturing and 3D printing at LOPE-C; on Board of Editors of the Micro-and Nanotechnology Journal of Bentham Science Publishers and since 2019 as associate editor for IEEE T-CPMT. Since 2016, he is member of the distinguished lecturer program of the IEEE EPS. Since 2014–2018, he served on the board of governors (BoG) of IEEE EPS in a first term.

TANJA BRAUN (AM'02-M'03-SM'17) studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000, she is working with the group Assembly & Encapsulation Technologies and since 2016, she is head of this group. Her field of research is process development of assembly and encapsulation processes, the qualification of these processes using both non-destructive and destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013, she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins.

Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging. In 2014, she received the Fraunhofer IZM research award.

Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Technical Chapter "Materials & Processing" and the Award Committee as well as the IEEE EPS Women in Engineering (WIE) delegate. Currently she is also ECTC subcommittee chair of "Materials & Processing".

REGION 10

GU-SUNG KIM (M'18) is currently in a faculty position at Kangnam University and a founder of EPRC (Electronic Package

Research Center) and EPMS (Electronic-Package Mission Society). He has 30 years of experience for R&D of Semiconductor Packaging. Prior to joining and establishing lecture/research position, Kim was a 3D IC/TSV/WLP project leader for Samsung Electronics Co., Ltd, IPT team, Memory Division during 17 years. He has more than 130 Patents as an inventor in Korea and USA related 3D IC, TSV, and Interposer. He published 2 semiconductor packaging handbooks and taught more than 3000 engineers in Korea. He received several awards from Korea MOTIE government, Samsung, Alfred Marquis Lifetime, City May, and SEMI etc.

Kim received a Ph.D. degree in materials engineering from Rensselaer Polytechnic Institute, Troy, NY, USA. And a BS degree in ceramic engineering from Yonsei University, Seoul, Korea.

He has served as chair of IEEE EPS Korea Council, SEMI STS ESIP, several National R&D program, vice-chair of KSDT, deputy-chair of EPRC, Kangnam University and Packaging Technology WG at KMEPS. He also has a position of BOD Chair of Electro-Package Mission Society (EPCross).

Congratulations to IEEE EPS Senior Members

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between June and November 2019.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Sitaram Arkalgud, Santa Clara Valley Section
Kenneth Karklin, Buenaventura Section
Anil Lingambudi, Bangalore Section
David Scott, Coastal Los Angeles Section
William Wurst, New Hampshire Section
Ramakrishna Alapati, Hyderabad Section
Amir Sajiad Bahman, Denmark Section
Nataraj Bhadriraju, Phoenix Section
Jai Ramesh Dasari, Hyderabad Section
Wei-Ping Dow, Taipei Section
Kayleen Helms, Phoenix Section
Madhusudan Iyengar, San Francisco Section
Hashem Tabrizi, Washington Section
Peter Thoma, Germany Section
Tim Tilford, United Kingdom and Ireland Section
Rene Zingg, Switzerland Section
En Yun Fei, Guangzhou Section
Thomas DeBoni, Phoenix Section
Somesh Kumar, Madhya Pradesh Subsection
Daniel Lambalot, Santa Clara Valley Section
Hongli Peng, Shanghai Section
Vikram Venkatadri, Boston Section
Jinto George, Kerala Section
Ziaul Karim, Oakland-East Bay Section
Chengkuo Lee, Singapore Section
Cai Liang, Coastal Los Angeles Section
Nicolae Militaru, Romania Section
Srinivas Pietambaram, Phoenix Section

Individuals may apply for Senior Member grade online at: https://www.ieee.org/membership/senior/

President's Column (*Continued from page 1*)

I am particularly pleased that we held our board of governors meeting for first time outside the US at our flagship conference—EPTC—in December 2018. We will continue this with our 2020 fall meeting which will be held at our European flagship conference—ESTC—in Norway in September 2020. In addition to this I plan to attend Eurosime (in April), ECTC (In June), ICEPT (in August), ICSJ (in November) and EPTC (in December). I look forward to meeting you at one of these events if you plan to attend. I am also open to any discussion or ideas you may have with regards the societies activities. Please feel free to contact me.

I would like to take this opportunity to pay particular thanks to Avi Bar-Cohen for his dedication and inspirational leadership as president of EPS over the last two years. I look forward to working with him in his new role as junior president.

Thank you to all those who have placed their confidence in me to provide leadership of our society over the next two years. I look forward to the tasks ahead and to working with all our members to strengthen our society and drive innovation in the electronics packaging community.

Congratulations to the 2020 Newly Elevated IEEE Fellows

Listed below are new IEEE Fellows who are members of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Yifan Guo
for leadership in interconnect technologies for electronics packaging and reliability analysis

Beth Keser
for contributions to electronic packaging technologies

Xiaowu Zhang
for contributions to three-dimensional integrated circuits

Student Chapter Promotion Programs

To promote the formation and continuation of EPS student chapters, EPS has recently initiated a couple of promotion programs. The Student Chapter Promotion Program (SCPP) is aimed at the formation of new student chapters while the Student Chapter Continuation Program (SCCP) is aimed at helping existing student chapters to remain viable.

Student Chapter Promotion Program (SCPP)

Under the SCPP, six students from any university which has an IEEE student branch who are willing to serve as executive committee (exco) members in a new student chapter will be given free IEEE+EPS student memberships. The exco must ensure that their student chapter remains viable for the year. This includes the organization of at least two technical activities per calendar year, holding of annual elections and timely submission of required activity and financial reports every year.

Additionally, faculty members who are willing to serve as Advisors to new student chapters will also be given free IEEE+EPS eMembership where available, otherwise regular memberships will be provided. The Advisor's duties include advising on student chapter activities, endorsing financial statements where necessary, ensuring that annual election of new student exco members are held before end December, and required reports are submitted by the student exco in a timely manner every year.

An evaluation on the performance of subsidized student exco members and Advisors will be conducted in January each year based on reports submitted. Non-performing students and Advisors will not be subsidized for another year. While Advisors may be subsidized every year, student exco members can only be subsidized a maximum of two times in order to encourage a healthy succession of student leaders in the chapter.

The first phase of the SCPP for 5 new student chapters was launched in May 2019 and was over-subscribed by one. All 6 applicants were eventually approved. They are: Michigan State University, University of Florida, University of Maryland, Fudan University, State University of New York at Binghamton and Florida International University.

A second phase of the SCPP to facilitate the formation of 10 more new student chapters in 2020/21 was launched in December 2019. Any student or faculty who are interested to form new EPS student chapters in their universities, *whether they are currently IEEE members or not*, can submit applications to the EPS Director of Student Programs, Dr Andrew Tay by emailing him at andrew_tay@ieee.org listing the names and email addresses of 6 students from the same university who are committed to serve as exco members in the new student chapter, and the name and email address of a faculty who is committed to serve as the chapter Advisor. The deadline for submissions is 28 February 2020. Thereafter the awardees will be decided by a committee according to some criteria and detailed instructions will be provided on the process of forming a new student chapter. It should be noted that not all submissions will be awarded.

Student Chapter Continuation Program (SCCP)

Another program, the Student Chapter Continuation Program (SCCP) has also been initiated to facilitate the continuation of existing EPS student chapters. Similar free IEEE+EPS memberships will be given to six students in a university with an existing EPS student chapter who are willing to serve as executive committee (exco) members in the student chapter, and to a faculty who agrees to serve as the Advisor to the student chapter. For this initial launch, any student or faculty who are interested to continue the existing EPS student chapter in their universities, *whether they are currently IEEE members or not*, can submit applications to the EPS Director of Student Programs, Dr Andrew Tay by emailing him at andrew_tay@ieee.org

listing the names and email addresses of 6 students from the same university who are committed to serve as exco members in the student chapter, and the name and email address of a faculty who is committed to serve as the chapter Advisor. The existing EPS student chapters are at Tsinghua University, Politechnica Univ of Bucharest, Universidade Federal do ABC, Singapore University of Technology & Design, Universidade Estadual Paulista—Guaratingueta, San Jose State University and University of California-Los Angeles.

Annual Subsidy for Student Chapters

To support the organisation of technical activities by student chapters, the exco may apply for subsidies of US$1000 per annum from EPS. For new chapters in their first year, the subsidy is US$1500.

Dr Andrew Tay
EPS Director of Student Programs

Society Membership Grows through Enthusiasm

Since you are receiving this IEEE EPS Newsletter, consider yourself a lucky person. A recent review of membership societies' surveys (regardless of society type) highlight several key opportunities one derives from this.

First and foremost, there is access to peer-reviewed journals, refereed papers from conference proceedings, and conference presentations. Optimally, one can listen to these papers, sit through a professional development course, or participate in a workshop real time. Since this is not always possible, for a variety of reasons, societies like IEEE EPS offer the next best thing: discounted conference registration and fees for the use of IEEE Xplore for paper access, free webinars, online training courses with professional development hours certification granted for one's personal development.

Second, engagement with other members worldwide leads to new and greater networking opportunities, stronger mentoring relationships, and technical expertise sharing regardless of one's location.

When a member feels connected to their community, engaged technically, and interacting socially he/she is most likely to renew their membership. Volunteering on committees/subcommittees for the society and its many technical conferences enhances this connectivity. Enthusiasm garnered through all connections creates a strong atmosphere that spreads to others encouraging them to become a part of the society.

Kitty Pearsall
Chapter Program Director

Technical Committee (TC)—Emerging Technologies

The Emerging Technologies technical committee of the Electronics Packaging Society EPS addresses packaging issues of new and novel technology concepts which target to revolutionize applications in general. This committee places an international focus on the development, characterization, and commercial support for packaging, assembly, and test infrastructure for key applications areas such as, Fluidic Systems, Optical Systems, Automotive Systems, Military Systems, Medical Systems, Remotely Operated Systems, Telecommunications and RF…

At present the EPS TC committee focusses on emerging technology topics like:

- 5G Electro-optical integration
- New assembly methods, self-assembly
- MEMS packaging
- Co design chip to interposer or board
- Additive manufacturing and 3D printing, i.e. nano-pastes nano-interconnect
- RF & power i.e. new challenge in 3D packaging and heterointegration and new reliability methods vibration/lowT
- Bio and medical , flexible and stretchable electronics
- Cyber security on packaging level
- Transformable electronics systems
- new electronics packaging visions in order to prepare for the future

For example one of our actual activities is the organization of the EPS Future Packaging Vision Contest (FPV) at the EPS President's Panel of the ECTC 2020 conference (May 2020).

The IEEE EPS President' Panel explores the path of packaging technologies towards the future. Visions of future packaging technologies are presented by students and discussed with EPS experts in the field. The best student packaging visions will be selected by an expert panel recruited from EPS and ECTC technologists and awarded the EPS FPV Awards at the panel session. In the frame of the EPS packaging technology vision contest, selected students with ECTC 2020 papers will be invited to propose their electronics packaging technologies visions to a review board assembled around the EPS President from IEEE EPS experts. They will prepare a short slide set in advance of the full paper submission. The selected/invited students will present their slide set with the bigger picture of their research work and their visions for the future (about the impact of their research field and work expected) at the panel session. Student ECTC authors are specifically encouraged to apply. The EPS President's Panel provides an enhanced opportunity to dialog with our younger colleagues in order to involve them and their way of thinking as early as possible into the discussion on future packaging technologies within the EPS. The result is to identify significant future packaging technologies in order to best serve IEEE and the electronics community by motivating and involving the very high potential of our students.

Judging Panel: Invited members of the Conference Committee, EPS BoG, TC Chairs and ECTC TPC Committee Chairs.

Timeline: After abstract submission deadline, identify accepted student papers.

Notification/Invitation: Invite up to 6 student authors/teams to participate in the contest and ask to submit a brief slide deck (5-6 slides) by DATE

Criteria for Judging:

- Quality of research done/Originality of the work presented (1-2 slides)
- Bigger picture of the work (1-2 slides)
- Impact to future packaging technologies (1-2 slides)

Presented to: An individual or a team of not more than three.

Prize: Up to three awards will be provided to an individual or team of no more than three

- 1st US$1,000
- 2nd US$600
- 3rd US$300

Presentation of Certificate:

- ECTC 2020, Tuesday evening panel session

For more information, to participate or to join our TC, or to volunteer for a leadership position in the TC and its activities, send an email note or letter to:

Karlheinz Bock, TC Chair for emerging technologies
TU Dresden, Institute for electronics packaging, IAVT
Germany
email: karlheinz.bock@tu-dresden.de

Anyone can be a participating member of one or more of the EPS Society's technical committees TCs without belonging to the IEEE. You may also contact the webmaster concerning the TC emerging technologies web-page https://cmte.ieee.org/eps-mems/.

PUBLICATION NEWS

Electronics Packaging Society Section Within IEEE Access

We invite you to be among the first to have your article peer-reviewed and published in the new Electronics Packaging section within IEEE *Access*. This is an exciting opportunity for your research to benefit from the high visibility of IEEE *Access*. Your work will also be exposed to 5 million unique monthly users of the IEEE *Xplore*® Digital Library.

The Electronics Packaging Section within IEEE *Access* will draw on the expert technical community to continue IEEE's commitment to publishing the most highly-cited content. The Journal peer-review process targets a publication period of 6 weeks for most accepted papers. This journal is fully open and compliant with funder mandates, including Plan S.

Scope

The IEEE Electronics Packaging Society section in IEEE Access covers the scientific, engineering, and production aspects of materials, components, modules, hybrids and micro-electronic systems for all electronic applications, which includes technology, selection, modeling/simulation, characterization, assembly, interconnection, packaging, handling, thermal management, reliability, testing/control of the above as applied in design and manufacturing. Examples include optoelectronics and bioelectronic systems packaging, and adaptation for operation in severe/harsh environments. Emphasis is on research, analysis, development, application and manufacturing technology that advance state-of-the-art within this scope.

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Go to: https://mc.manuscriptcentral.com/ieee-access

Select the Electronics Packaging Society (EPS) Section from the pull-down menu of "Manuscript type" in the first page of the submission process.

Author Information and Instructions

EPS is committed to supporting authors and researchers with IEEE Author Tools including the IEEE Publication Recommender, IEEE Graphics Analyzer, LaTeX Analyzer and more. Discover the tools available at the IEEE Author Center—https://ieeeauthorcenter.ieee.org/ieee-author-tools/.

The EPS is regarded as a trusted and unbiased source of technical information for dialog and collaboration to advance technology within the computing community. EPS is led by researchers and technology professionals who are at the center of respected electronics packaging communities where readers and authors already come together.

The articles in this journal are peer reviewed in accordance with the requirements set forth in the IEEE Publication Services and Products Board Operations. Each published article is reviewed by a minimum of two independent reviewers using a single-blind peer review process, where the identities of the reviewers are not known to the authors, but the reviewers know the identities of the authors. Articles will be screened for plagiarism before acceptance.

Article Processing Charge (APC): US$1,750
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Publication Year: 2011, Page(s): 181–195

Device-Level Thermal Management of Gallium Oxide Field-Effect Transistors
Bikramjit Chatterjee; Ke Zeng; Christopher D. Nordquist; Uttam Singisetti; Sukwon Choi
Publication Year: 2019, Page(s): 2352–2365

A Filtering Dual-Polarized Antenna Subarray Targeting for Base Stations in Millimeter-Wave 5G Wireless Communications
Hui Chu; Yong-Xin Guo
Publication Year: 2017, Page(s): 964–973

EDUCATION/CAREER NEWS

Professional Development Through the EPS CEU (Continuing Education Unit) Program

One of the outstanding benefits of participation in the EPS PDC (professional development courses) offered at EPS sponsored conferences is that it is very easy to participate. An attendee can select a unique packaging topic from the courses.

In 2006 the Electronic Packaging Society introduced professional development courses at the annual ECTC. Today the program has grown; it now consists of 18 unique PDCs; nine held in the morning and nine in the afternoon. As an IEEE EPS member you do receive a discount when you register for these courses at the ECTC. The EPS has issued 1666 Certificates from 2010 to 2019.

In 2018 CEU credit certificates were made available for both the ESTC PDC program and the EPTC PDC program. These conferences are considerably smaller than ECTC yet there is still a desire by attendees to participate in courses and request CEU credit. To date 28 and 120 CEU certificates, respectively, were sent to ESTC and EPTC conference PDC attendees.

This is a great time to consider taking a professional development course in this year's 2020 ECTC held in Orlando, Florida.

EPS Certificate of Achievement

In order to further the education of Electronics Packaging Society (EPS) members, the EPS is now offering a Certificate Program. The goal of the program is to give members new to electronics packaging an opportunity for further packaging education, offer continuous education in electronics packaging to existing members, and also to offer students electronics packaging training if they are in a University program that does not include packaging education.

Criteria: Must be an IEEE Electronics Packaging Society Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of EPS Webinars, Professional Development Courses at select EPS Conferences, author of IEEE T-CPMT paper and/or EPS Conference paper, reviewer for IEEE T-CPMT.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate.

Congratulations to these EPS Members on receiving the IEEE Certificate of Achievement from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Katsuyuki Skuma, IBM Thomas J. Watson Research Center
Tan Yik Yee, ON Semiconductor Sdn. Bhd.
Christopher Breach, KCI UK Holdings Ltd
Stevan Hunter, ON Semiconductor, BYU-Idaho, ASU, UMD CALCE
Venkateswararao Para, Microsystems
Gan Chong Leong, Micron Technology
Venkatesh Avula, Georgia Institute of Technology

Upcoming Webinar

Implantable Electronics: Emerging Packaging Needs, Challenges and Recent Industry Breakthroughs

(February 6, 2020 11:00 AM US Eastern)
Visit https://eps.ieee.org/education/eps-webinars.html to Register

IEEE EPS Nanopackaging TC, Emerging Technologies TC and FIU Miami Student Chapter are happy to sponsor the upcoming webinar on implantable electronics.

Ranu Jung, Professor, BME, FIU; Fellow NAI and Fellow AIMBE

Part I: Packaging Needs and Challenges in Neuroprosthetic technologies
(Ranu Jung, Biomedical Engineering, Florida International University)
Neuroprosthetic technologies aim to continuously interface with the nervous system to restore lost motor or sensory functions from injury and diseases. Such technologies have already been helping patients with hearing and vision loss, amputees, patients with spincal cord injury, and other brain-related disorders. Emerging neuroprosthetic technologies and the needs for advanced packaging solutions for miniaturized functional integration in implantable electronics will be described in the first part. Recent advances in the development of a fully implantable, wirelessly controlled system to directly stimulate nerves and restore sensation with neural-enabled prosthetic hand, develop by the speaker and her team, will be highlighted.

Part II: Glass packaging for long-term implantable electronics
(Ossi Lahtinen, SCHOTT Primoceler Oy, Finland)
For the past 40 years medical implants have been mostly encapsulated inside titanium. However, using glass as a package material

Ossi Lahtinen, Production Director, Schott Primoceler

can offer several benefits. The RF transparency of glass enables recharging, data transfer and reprogramming of implants. Transparency to visible light is an advantage in wide range of optical applications: Hermeticity is one of the key factors when reliability is a concern. Glass micro bonding combined together with hermetic through glass vias (TGVs) helps designing a chronically implantable electronics device. The hermeticity of the designed package can be tested according to Military standards, such as MIL-STD-883 and MIL-STD-750.

Gaurav Mehrotra Principle Packaging Engineer, Renesas (IDT)

Part II: Packaging of Fully-Implantable Photonic Glucose Sensors
(Gaurav Mehrotra, Renesas)
Eversense CGM is the world's first, long-term, fully-implantable (subcutaneous) CGM developed by Senseonics Inc. in collaboration with Integrated Device Technology (a Renesas Company). In this talk, Gaurav will highlight the system integration and packaging challenges associated with Eversense CGM. Type 1 diabetes requires lifelong insulin therapy with doses adjusted based on monitoring of blood glucose levels. 'Self-monitoring' (finger pricking) only provides a few data points per day and does not capture several periods of highs and lows. Continuous Glucose Monitoring (CGM) systems take continuous periodic measurements thereby dramatically increasing the amount of information available to the patient and their healthcare providers. Access to this real-time data can help patients achieve tight glycemic management and do it safely.

EPS News (*Continued from page 3*)

2006—C. P. Wong
"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005—Yutaka Tsukada
"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004—John W. Balde
"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www. ieee.org/awards

3rd Annual Heterogeneous Integration Roadmap (HIR) Meeting & Symposium

Co-hosted by IEEE EPS, EPS Santa Clara Valley Chapter & SEMI

When: February 20–21, 2020
Where: SEMI Headquarters, 673 South Milpitas Blvd, Milpitas, CA USA
Registration Fee: $50 IEEE & ASME members; $35 retired, students, unemployed; $60 non-members. ($20 more after Feb. 14th) (includes 2 lunches, wine-tasting)
Registration fee waived for Invited speakers & HIR Technical Working Group (TWG) members
Register Here: http://www.cpmt.org/scv/?p=999

Thursday, February 20, 2020: HIR Symposium
Time: 8:30 AM – 6:00 PM
Who Should Attend: Open to the General Public
Plenary Speakers and Technical Working Group Representatives (from Intel, Boeing, Fraunhofer, NASA, Infineon, Google, Advantest, ASE, ITRI, SEMI, UI-UC, U-Md, UCLA, more)

Friday, February 21, 2020: HIR Technical Working Meeting and Open House
Time: 8:30 AM – 4:00 PM
Who Should Attend: All HIR Technical Working Group members and anyone interested in participating or learning more about the Heterogeneous Integration Roadmap.

The purpose is to provide a structured forum for interaction, collaboration and feedback.

We are in a period of technology and market disruptions. There is immense need for pre-competitive technology roadmaps addressing future vision, difficult challenges, and potential solutions.

Heterogeneous Integration will be the key technology direction going forward, for device and subsystem integration. It is the "low hanging fruit" for initiating a new era of technological and scientific advances.

The 2019 HIR edition was released October 2019. This Annual Meeting kicks off the revision work for the 2020 HIR Edition. The agenda for the Roadmap Annual Meeting, including Plenary Speakers and Technical Working Group reports, follows:

HIR ROADMAP Symposium Thursday Feb 20, 2020

8:30–9:00 am **REGISTRATION & COFFEE**

9:00–9:05 am **Symposium Opening (HIR IRC)**

9:05–9:10 am **Welcome: Ajit Manocha SEMI CEO**

9:10–9:25 am **HIR Symposium Objective: (HIR IRC)**

9:25 – 9:55 am **1st Plenary Session Moderator: (TBD)**
Plenary Speaker: Dr. Pradeep Dubey, Intel Senior Fellow

Session 1 Chair: Amr Helmy, IEEE Photonics Society and Univ of Toronto
10:05–11:05 am Heterogeneous Integration for Communication
- 5G, RF and Analog Mixed Signal: Tim Lee (Boeing), Herbert Bennett (Alta Tech)
- Mobile: William Chen (ASE), Benson Chen (Binghamton University)
- Aerospace & Defense: Tim Lee (Boeing), Jeff Demmin (Keysight)
- WLP (Fan-in & Fan Out): Rozalia Beica (iNEMI), John Hunt (ASE)
- Simulation: Chris Bailey (University of Greenwich), Xuejun Fan (Lamar University)
- Materials & Emerging Research Materials: Bill Bottoms (3MTS)

11:05–11:15 am **Q&A**

BREAK (15 minutes)

Session 2 Chair: Ravi Mahajan, ASME EPPD & Intel
11:30–12:20 pm Heterogeneous Integration for Consumer & Industrial Applications
- Medical, Health & Wearables: Mark Poliks (Binghamton U), Nancy Stoffel (GE)
- SiP & Module: Rolf Aschenbrenner (Fraunhofer IZM), Klaus Pressel (Infineon)
- Single Chip and Multi Chip Integration: William Chen (ASE), Annette Teng (Promex)
- Emerging Research Devices: Meyya Meyyappan (NASA Ames)
- Co-Design: Jose Schutt-Aine (University of Illinois)

12:20–12:30 pm **Q&A**

12:30–12:35 **Thanks to Organizers and Patrons**

12:35–01:30 pm **LUNCH**

1:30–2:00 pm **2nd PLENARY Session**
Plenary Speaker: Dr Hong Liu, Senior Director Google

Session 3 Chair: Bill Bottoms, IEEE EPS and 3MTS
1:50–2:40 pm Heterogeneous Integration for High Performance Computing
- High Performance Computing & Data Centers: Kanad Ghose (Binghamton University), Dale Becker (IBM), Rockwell Hsu (Cisco)
- 2D-3D & Interconnect: Ravi Mahajan (Intel)
- Thermal Management: Madhu Iyenger (Google), Azmat Malik (Acuventures)
- Integrated Photonics: Amr Helmy (University of Toronto), Bill Bottoms (3MTS)
- Test: David Armstrong (Adventest)

2:40–2:50 pm **Q&A**

BREAK (15 Minutes)

Session 4 Chair: Paul Trio SEMI

3:10–4:10 pm Heterogeneous Integration for Special Applications

- Automotive: Urmi Ray (iNEMI), Rich Rice (ASE)
- MEMS & Sensors Integration: Shafi Saiyed (ADI)
- Integrated Power Packaging: Patrick McCluskey (U-Md), Doug Hopkins (NCSU)
- Cyber Security: Sohrab Aftabjahani (Intel)
- Supply Chain: Paul Trio (SEMI)
- IoT: Robert Lo (ITRI)

4:10 – 4:20 pm **Q&A**

4:20–5:20 pm **HIR Open Forum: Feedback & Comments**

5:20–5:35 pm **Next Day TWG Workshop Preparation**

5:35–5:45 pm **WRAP UP: IRC**
SYMPOSIUM CLOSING

5:45–6:45 pm **California Wine Tasting**

HIR Technical Working Group Workshop Friday February 21st, 2020 8:30 am to 4:00 pm.
Download the 2019 Edition of the Heterogeneous Integration Roadmap at https://eps.ieee.org/hir-2019.

Travel Funding for Outstanding/Best Papers from Flagship Conferences

To highlight the best/outstanding papers selected from each of the EPS flagship conferences (ECTC, ESTC and EPTC), travel funding will be provided to attend another EPS flagship conference. One author will be invited to present their best/outstanding paper (up to US$2,125 for intercontinental travel and up to US$1,375 for intracontinental travel). Only one trip per paper will be allowed (one co-author can be invited; preference for original presenter) and can only be taken within 12 months of award.

For a Limited Time

The following best/outstanding papers from ECTC 2019 will be available on Xplore as Open Access until June 1, 2020.

- Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures
- Low Temperature and Pressureless Microfluidic Electroless Bonding Process for Vertical Interconnection
- A MEMS Microphone in a FOWLP
- An Assessment of Electromigration in 2.5D Packaging

2019 EPTC Highlights

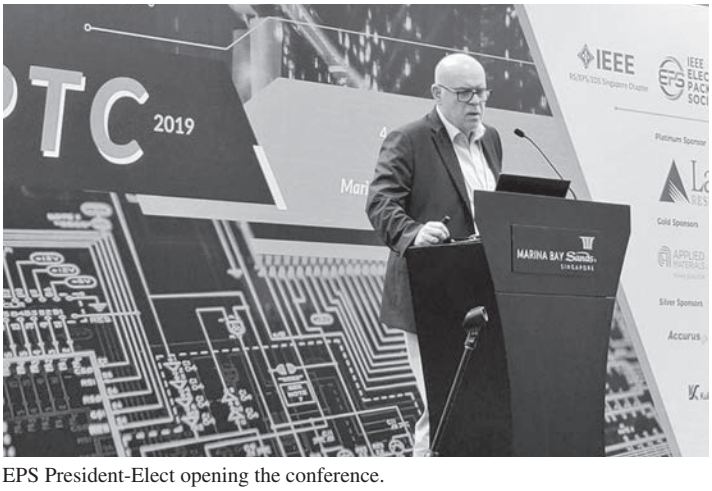
Report on EPTC 2019

The 21st Electronics Packaging Technology Conference (EPTC) was held on 4-6 December 2019 at Marina Bay Sands, Singapore. This international conference is our Society's flagship conference in the Asia-Pacific (Region 10). It is organized by the IEEE Singapore RS/EPS/EDS Chapter and co-sponsored by EPS. It aims to bring together engineers and researchers from the international microelectronics packaging community, especially those from Region 10, under one roof to share knowledge, expertise and network. Attendees include those from semiconductor companies, foundries, OSAT service providers, equipment manufacturers, materials suppliers, research institutions and universities. 158 technical papers and 20 invited presentations were presented in 20 oral sessions and an interactive poster session. Altogether, 356 participants from 21 countries attended the conference.

Starting on the morning of December 4th, the following 5 professional development courses were conducted:

- Prof. Mervi Paulasto-Kröckel; Aalto University, "Power Electronics Packaging for Automotive Application"
- Dr. John H Lau; Unimicron Technology Corporation, "Fan-Out Wafer/Panel-Level Packaging and Heterogeneous Integrations"
- Prof. Xuejun Fan; Lamar University, "Reliability Mechanics and Modeling for IC Packaging—Theory, Implementation and Practices"
- Prof. Y. P. Zhang; Nanyang Technological University, "Antenna-in-Package (AiP) Technology for Millimeter Wave Systems"
- Prof. Chris Bailey, University of Greenwich, "Co-Design/ Modeling and Additive Manufacturing for Electronics Packaging"

The conference was officially opened in the afternoon of December 4th by then EPS President-elect, Prof Chris Bailey.



EPS President-Elect opening the conference.

Keynote speaker Dr Ram Viswanath, VP, Intel.

Keynote speaker Mr Glen Mori, MD, Applied Materials.

That was followed by two keynotes. The first was delivered Dr. Ram Viswanath, VP, Intel, who spoke on "Innovations in electronic packaging for compute and communication". The second was delivered by Mr. Glen Mori, Managing Director, Advanced Packaging, Applied Materials who spoke on "Enabling the building blocks for next generation of electronics packaging".

After a coffee break, in collaboration with iNEMI, a panel session on "Packaging Challenges and Opportunities for 5G Applications" was held which was moderated by Dr. Haley Fu from iNEMI. The panel members were:

- Dr. Daniel Rhee Min Woo, Program Manager, Samsung Electronics.
- Prof. Y. P. Zhang; Nanyang Technological University.
- Mr. Kikuchi, Shunichi; CVP, Fujitsu Advanced Technologies Limited.
- Dr. Toshihisa Nonaka; Director, Hitachi Chemical Co. Ltd.
- Mr. Erkko Helminen; Snr. Manager, TTM Technologies.
- Dr. Gokul Kumar, Snr Manager, Packaging design and development, Micron.

Altogether 20 technical sessions were held on December 5th and 6th. The technical sessions featured selected papers on key topics which included 2.5D, 3D and TSV Processes, Advanced FA and Reliability for IC Packages, Advanced Materials and Processing, Advances in Solder Joint and Reliability, Die Attach and Sintering Technologies, Electrical Simulation and Characterization for Advanced Packaging, Hybrid Bonding, LED and Photonic Packaging, Liquid Cooling and Micro-Fluid Technology, Materials Challenges for Power Module Packaging, MEMS Sensors and IoT Packaging and Processes, Mold Compound Characterization and Processing, New Interconnects for 3D and Heterogeneous Integration, Next Generation Wire bonding & Characterization, Power Module Assembly and Technologies, Printed Electronics, RF, 5G and mmWave Packaging, Silicon and Glass Interposer Processing, Thermal Characterization and Cooling Solutions for IC and Emerging Packaging, Thermal and Thermo-mechanical Simulation and Characterization of Advanced Packages, and Wafer Fan-Out Processes and Characterization.

An invited presentation was given by an expert at the beginning of each technical session. The following is a list of the invited presentations given over December 5th and 6th:

- Dr Curry Chen, ASE Global, "Development of multi-chip integration non-molded 2.5D IC Packaging Technology"
- Prof Jeffrey Suhling, Auburn University, "Reduction of Aging Induced Reliability Degradations Using SAC+X Lead Free Solders"
- Dr Gokul Kumar, Micron, "Memory-Centric Design Challenges for Flash products"
- Prof Yogendra Joshi, Georgia Institute of Technology, "Cooling of high power microelectronic components using flow boiling"
- Mr. Murayama Kei, Shinko Electric Industries, "Effects of trace element on electro-migration of flip chip interconnect between Cu pillar and Sn-Bi alloy system"

Panel session on "Packaging Challenges and Opportunities for 5G Applications".

Platinum Sponsor Lam Research.

EPS booth at the conference.

- Prof SB Park, State University of New York, "Importance of Warpage Engineering in the era of Heterogeneous Integration"
- Dr Szu Huat Goh, Global Foundries, "Evolution of Fault Isolation Techniques for Product Failure Analysis"
- Dr Sia Choon Beng, Formfactor, "Highly Accurate, Efficient and Reliable Silicon Photonics Wafer-Level Test and Characterization"
- Dr Takenori Fujiwara, Toray Industries, Inc. "Development of Novel Polymer Materials for Advance Packaging"
- Dr Murali Sarangapani, Heraeus Singapore, "Micro-Interconnects: Signal Integrity in 5G applications."
- Mr. Shunichi Kikuchi, Fujitsu Advanced Technologies Limited, "System Packaging Solutions for High Performance Computing in the Era of 5G/IoT"
- Dr. Luan Jing-En, STMicroelectronics, "Virtual prototyping for electronic packaging development, dream or reality?"
- Mr. Favier Shoo, Yole Development, "Market and Technology Trends of Advanced Packaging, Fan-Out Packaging"
- Mr. Xue Ming, Infineon, "What is new for the fast learning of IC Reliability—Advanced Defect Learning, Package Structural Testing, & Reliability modelling by HPC"
- Mr. Premachandran CS, Globalfoundries, "A comprehensive Reliability assessment on 2.5D and 3D Integration"

Workshop on Heterogeneous Integration Roadmap.


Meeting of EPS Officers and EPS Region 10 Chapter Chairs.


The conference banquet was held on the 55th floor of the iconic Marina Bay Sands Hotel.


Panel session on future of young professionals in electronics packaging.

EPTC2019 Organizing Committee.

- Dr Dongshun Bai, Brewer Science, "Material Advancement for Heterogenous Integration"
- Prof Sarah Kim, Seoul National University of Science and Technology, "Plasma process optimization for Cu bonding integration using the design of experiment technique"
- Dr Yasuhiro Morikawa, Ulvac, "Manufacturing Technology Solution of Small Via for Heterogeneous Integration"
- Dr Daniel Rhee Min Woo, "Novel MEMS based Lateral Contact Probing Method for Fine Pitch Micro-bumps for High Bandwidth Memory (HBM) Testing", Samsung.
- Dr. Yu-Po Wang, "Innovative Package for 5G Era", SPIL.

In conjunction with the conference, there was an exhibition corner and exhibitors' presentations during tea breaks from leading semiconductor companies showcasing their latest technologies and solutions.

A Workshop on Heterogeneous Integration Roadmap (HIR) was conducted by Dr William Chen and Dr Bill Bottoms in the late afternoon of December 5th featuring the following experts who updated the conferees on on-going efforts within their respective working groups:

- Prof. Mervi Paulasto-Krockel (Aalto University)
- Dr. Gamal Refai-Ahmed (Xilinx)
- Dr. Loh, Wei-Keat (Intel)
- Prof. Christopher Bailey (Greenwich University)
- Prof. Tan, Chuan Seng (Nanyang Technological University)

One of the highlights of EPTC was the banquet which was held high up on the 55th floor of Marin Bay Sands hotel where conferees had a sumptuous buffet dinner with a panoramic view of the bay area and city skyline below.

On the sidelines of the conference, a meeting between EPS Officers and EPS Chapter Chairs and representatives was held.

A panel session on "The Future of Young Professionals in the Field of Electronics Packaging" was also held on the sidelines of the conference.

Last but not least, the organizing committee would like to thank all sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, committee members, EPTC Board members, EPS BoG members, conference secretary, website support team, media partners, partnering associations, conference partners, souvenir sponsors, publicity team, suppliers and vendors as well as all the conference assistants and volunteers for their support and hard work. We also thank all conference delegates for making this event a great success. More information about EPTC is available at https://eptc-ieee.net/.

Andrew Tay and WW Wong

IEEE ESTC EPS VESTFOLD 2020

Electronics System-Integration Technology Conference

15th-18th September 2020
Vestfold, Norway

Call for papers

The Electronics System-Integration Technology Conference (ESTC) is the premier international event in the field of electronics packaging and system integration. The conference is organized every two years in Europe and is supported by IEEE-EPS in association with IMAPS-Europe.

This international event brings together both academics and industry leaders to present and discuss the state-of-the-art as well as the future trends in electronics packaging and integration technologies. ESTC offers excellent opportunities for knowledge exchange and networking with international experts in the field.

The ESTC 2020 will take place from 15th to 18th September 2020 in Vestfold, Norway, where the "Norwegian Centre of Expertise" in Micro- and Nanotechnologies is established. The industry cluster in Vestfold, together with the University of South-Eastern Norway (USN), represents a major portion of Norway's activities in the field. High-end devices for aerospace, medical, maritime and industrial applications are quality products from the region, with a strong focus on packaging, system integration and reliability.

Vestfold, Norway, welcomes you with its proud maritime traditions, as the centre of Viking cultural heritage, and with a pleasant climate. The conference venue will be at the beautiful Tønsberg Pier. Communication to Vestfold is easy, with direct train from Oslo Airport (OSL), as well as the local airport (Sandefjord Torp – TRF) with direct connections to several major European destinations.

University of South-Eastern Norway · IEEE · IMAPS Europe · IEEE Electronics Packaging Society · Norwegian Centres of Expertise NCE Micro- and Nanotechnology

estc-conference.net

Conference topics

The ESTC 2020 seeks original, non-commercial papers describing research and innovations in all areas of electronics packaging and system integration. You are invited to submit abstract(s) presenting new developments and knowledge in areas such as:

Design tools and modelling:
electrical, mechanical, thermal and thermomechanical simulations, preferably presented with supporting experimental test results.

Materials for interconnects and packaging:
advances in soldering, intermetallic bonding, adhesive bonding, Cu pillars, low-k wafers, substrates, printed circuit boards for advanced packaging, die attach, underfill, encapsulants, moulding compounds.

Assembly and manufacturing technologies:
flip-chip bonding, wire bonding, dispensing, printing, deposition techniques, process development, new equipment & improvements, clean room technologies, yield improvement, cost and cycle time reduction, green manufacturing.

Advanced packaging:
2.5D & 3D integration, package-on-package, system in package, panel level packaging, system-integration, embedded parts and components, rugged electronics packaging, wafer level packaging (fan in / fan out), through silicon vias, silicon & glass interposer, re-distribution layer, bumping technologies.

Optoelectronics:
advanced photonics components and systems, power LED assembly, packaging and light guiding, packaging of optoelectronic modules suitable for Gb/s, fibre optic communication, photovoltaic.

MEMS/NEMS and sensor packaging:
MEMS and/or NEMS -based sensors and actuators, RF-MEMS, optical MEMS, bio-MEMS, MEMS-based WiFi modules.

Power electronics:
power embedding, wide bandgap power semiconductor devices, fuel cells, battery technologies.

Flexible printed and hybrid electronics:
wearable electronics, printed electronics.

Advanced technologies for emerging systems:
internet of things, autonomous systems, robotics, telecommunications, radio frequency systems, artificial intelligence, quantum computing.

Reliability and quality of electronic devices and systems:
component-, board-, system- and product-level reliability assessment, interfacial adhesion, accelerated testing, inspection and test, failure characterization.

Topics of special interests:
technologies and solutions for applications such as automotive, maritime, aerospace & space, energy, bio-medical, smart farming.

Practical information

ABSTRACT SUBMISSION
You are invited to submit a 300 - 500 word abstract that describes the scope, content and key points of your proposed paper. Abstracts must include results and graphics. The official language of all presentations is English. Please visit **www.estc-conference.net** to find more information and how to upload your abstract.

Submission of abstracts is opened from 1st December 2019 and is closed by 16th February 2020. All abstracts must be submitted electronically on the conference website. The ESTC committee will review all submitted abstracts and notify authors of paper acceptance with instructions for publication by 31st March 2020.

If you have any questions, please contact us via email **estc@estc-conference.net**

PUBLICATION OF PAPERS
All oral and poster presentation papers will be included in the conference proceedings. Additionally, all papers that are original, not previously published, and without commercial content will be made available in the IEEE Xplore Digital Library (https://ieeexplore.ieee.org/Xplore/home.jsp).

BEST PAPER AWARDS
The ESTC Technical Committee will select the best oral paper as well as the best poster paper. The author(s) of each paper will receive an ESTC award of 1.000 €.

PROFESSIONAL DEVELOPMENT COURSES
The ESTC committee calls for proposals from individuals interested in teaching professional development courses (duration 4 hours) within the topics described in the call for papers.

Up to four professional development courses will be selected from the received proposals. Each selected course is given an honorarium of 750 € if a minimum number of participants signs up for the course. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. A 300 - 500 word proposal containing description of course objectives, course outline and target audience, should be submitted to the Professional Development Courses Chair via email **pdc@estc-conference.net** by **16th February2020.**

Important dates

Website open for abstract submission:
1st December 2019

Abstract submission deadline:
16th February 2020

Notification of acceptance:
31st March 2020

General Chair: Knut E. Aasmundtveit
University of South-Eastern Norway

Executive Chair: Kristin Imenes
University of South-Eastern Norway

Technical Program Chair: Paul M. Svasta
CETTI, Romania

estc-conference.net

2020 21st International Conference on Electronic Packaging Technology (ICEPT) will be held in Guangzhou, China, from *August 12 to 15, 2020*. ICEPT 2020 is hosted by Institute of Microelectronics of Chinese Academy of Sciences (IMECAS), technically sponsored by IEEE Electronics Packaging Society (IEEE-EPS), Electronic Manufacturing and Packaging Technology Society of Chinese Institute of Electronics (CIE-EMPT), organized by Guangdong University of Technology, and co-organized by National Center for Advanced Packaging Co., Ltd. (NCAP China). As one of the most famous international conferences on electronic packaging technology, the conference has received strong support from IEEE- EPS and high praise from Chinese Institute of Electronics (CIE) and China Association for Science and Technology (CAST). At present, Moore's Law has reached an inflection point, semiconductor manufacturing technology is facing challenges, and new technologies are constantly emerging. This conference will provide an academic communication platform for new progresses and new ideas in electronic packaging and manufacturing technology for experts, scholars and researchers from academia and industry worldwide.

During the four-day event, participants from nearly 20 countries and region will share the latest technological developments of electronic packaging technologies via special lectures, invited talks, theme forums, technical sessions, exhibitions, poster presentations and other forms. We sincerely invite you to join in this event!

CONFERENCE TOPICS

- **Advanced Packaging**: 2.5D and 3D packaging, wafer-level and panel-level packaging, flip chip, advanced packaging substrate technologies, system integration, heterogeneous/hybrid integration, packaging design and process.
- **Packaging Materials & Processes**: New packaging materials, green materials, nano-materials, and related packaging materials for packaging/assembly processes.
- **Packaging Design & Modeling**: Design, modeling, methodology, and simulation for system integration and packaging; methodology and simulation for electrical/thermal/optical/mechanical models, multi-scale and multi-physics modeling, process simulation.
- **Interconnection Technologies**: TSV, bumping and micro copper pillar technologies, high density inter-connection technologies, nano-materials bonding technologies, interposer, redistribution layer technologies for fan-in and fan-out packaging, chip-to-wafer/panel and wafer-to-wafer interconnect technologies, thermocompression bonding, non-conventional inter-connection technologies.
- **Advanced Manufacturing & Packaging Equipment**: Assembly, testing, manufacturing, automation technologies and equipment for Packaging manufacturing.
- **Quality & Reliability**: Test technologies for packaging, quality monitoring and evaluation, methodologies for reliability data collection and analysis, reliability modeling, life prediction, failure analysis and non-destructive diagnose.
- **Power Electronics**: Thermal management, interconnection and substrate technologies for power electronics, switch module, isolated/non-isolated power converter, inverter module, IPM, POL, PwrSoC, PSiP, open frame, electrical design, magnetic integration, control algorithm, firmware development, EMI modeling & optimization.
- **Optoelectronics and New Display**: Optoelectronics and solid state lighting design, simulation, interconnection, packaging & integration, display module encapsulation & assembly, new display device and module encapsulation & assembly, mass Transfer of MicroLED, wearable, bendable, foldable and flexible electronics and display.
- **MEMS & Fan-out Packaging**: MEMS, NEMS, sensor, sensor packaging, implantable device packaging, microfluidics, nano-battery. 3D printing, self-alignment and assembly, wafer-level and panel-level packaging, redistribution layer, reliability, new structure and technologies for fan-out packaging.
- **Emerging Technologies**: Electrical modeling, analysis, design, integration, fabrication and characterization of novel devices, packages, and systems for RF/microwave and high-speed I/O, component optimization and power management of computing/communication systems, 5G mobile networking, wearable/flexible electronics and bio-electronics, etc.

IMPORTANT DATES

❑ March 20, 2020	Deadline for Submission of Abstract
❑ April 10, 2020	Notification of Abstract Acceptance
❑ May 20, 2020	Deadline for Submission of Full Paper
❑ June 10, 2020	Notification of Full Paper Acceptance
❑ June 20, 2020	Deadline of Final Paper Submission

SUBMISSION OF ABSTRACT

Abstracts are solicited to describe original and unpublished work. The abstract should be approx. 500 words and contains a clear statement of the background, methodology, results, and conclusions. All abstracts and manuscripts must be in English and should be submitted through online submission system**.** The instructions for abstract submission can be found at the conference website **http://www.icept.org**. All accepted manuscripts will be submitted for inclusion into IEEE Xplore. Selected papers will be recommended for publication in related IEEE/EPS journals.

BEST PAPER AWARD

Best Papers and Posters will be selected and awarded at the conference.

CALL FOR EXHIBITION/SPONSORSHIP

A tabletop exhibition featuring suppliers of materials, equipment, components, software, manufacturers, and service providers of the electronics packaging and related industries will be held during the conference. Potential exhibitors and sponsors may e-mail to **icept2020@gdut.edu.cn** for details.

General Chairs:	**Tianchun YE**	**Xin CHEN**
Technical Chair:	**Chengqiang CUI**	**Liqiang CAO**
Organizing Chair:	**Qiang LIU**	**Wen YIN**

Conference Website: **http://www.icept.org** E-mail: **icept2020@gdut.edu.cn**

ABOUT Guangzhou

As the capital of Guangdong Province, Guangzhou locates at the center of Guangdong-Hong Kong-Macao Greater Bay Area, which is one of the largest urban agglomerations in the world. Since the 3rd century AD, Guangzhou has become the main port of the Maritime Silk Road and a political, military, economic, cultural, scientific and educational center in South China. Today's Guangzhou has attracted a large number of businessmen and high-tech enterprises, brought together 80% of colleges and universities and 70% of scientists and technologists in the province. The city has become an energetic international trade center and comprehensive transportation hub, and is hailed as China's southern gate to the world.

Hosted by IMECAS | Technically Sponsored By IEEE EPS ELECTRONICS PACKAGING SOCIETY, EMPT | Organized by 廣東工業大學 Guangdong University of Technology

IEEE EPS Malaysia: 2019 Semiconductor Advanced Packaging Workshop

(Compiled by Eng Hoo Leow)

The 2019 Semiconductor Advanced Packaging Workshop organized by IEEE EPS Malaysia Chapter is back! The bi-annual one-day technical workshop took place at Eastin Hotel, Penang and New World Hotel, Petaling Jaya scheduled on September 24th and 25th respectively. It featured contemporary packaging trends and development of emerging technologies from two distinguished speakers in the field of semiconductor: (1) *Prof. Dr. Madhavan Swaminathan (Georgia Tech, USA) on "Intelligent Digital Convergence for AI and 5G"* (2) *Dr. John Lau Hon Shing (UMTC, Taiwan) on "Fan-Out Wafer/Panel-Level Packaging & Heterogeneous Integrations (SiPs)".*

Honorable speakers: Prof. Dr. Swaminathan, Georgia Tech, USA & Dr. John Lau, UMTC, Taiwan.

Approximately 180 attendees - a diverse group of industry professionals, researchers and undergraduates from 30+ companies and local universities Malaysia wide participated in this informative and quality knowledge sharing session. In 2019, EPS Malaysia Chapter and Anton-Paar Sdn. Bhd. have exceptionally extended sponsorship to academia, primarily aimed at providing industrial exposure to potential graduates. What's next from IEEE EPS Malaysia Chapter to constantly motivating regional engineering community on technical excellence? –it's the 39th International Electronics Manufacturing Technology (IEMT) 2020 Conference. We are looking forward to seeing you next year in Putrajaya!!

Image: Attendees at Eastin Hotel, Penang

Image: Attendees at New World Hotel, Petaling Jaya.


Images: Souvenir presentation to speakers as token of appreciation


Images: Workshop-In-Progress and Networking hour

Top Conference Papers Based on 2019 Usage

2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

(May 28–May 31, 2019)

System on Integrated Chips (SoIC(TM) for 3D Heterogeneous Integration
Ming-Fa Chen; Fang-Cheng Chen; Wen-Chih Chiou; Doug C.H. Yu

3D-MiM (MUST-in-MUST) Technology for Advanced System Integration
An-Jhih Su; Terry Ku; Chung-Hao Tsai; Kuo-Chung Yee; Douglas Yu

Signal Integrity of Submicron InFO Heterogeneous Integration for High Performance Computing Applications
Chuei-Tang Wang; Jeng-Shien Hsieh; Victor C. Y. Chang; Shih-Ya Huang; T. Ko; Han-Ping Pu; Douglas Yu

Low Temperature Cu Interconnect with Chip to Wafer Hybrid Bonding
Guilian Gao; Laura Mirkarimi; Thomas Workman; Gill Fountain; Jeremy Theil; Gabe Guevara; Ping Liu; Bongsub Lee; Pawel Mrozek; Michael Huynh; Catharina Rudolph; Thomas Werner; Anke Hanisch

OpenCAPI Memory Interface Signal Integrity Study for High-Speed DDR5 Differential DIMM Channel with Standard Loss FR-4 Material and SNIA SFF-TA-1002 Connector
Biao Cai; Jose Hejase; Kyle Giesen; Junyan Tang; Brian Connolly; KyuHyoun Kim; Daniel Dreps; Zhineng Fan; Rocky Huang; Luyun Yi; Qiaoli Chen; Yifan Huang; Stephen Smith

2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(May 28–May 31, 2019)

Electro-Thermal Simulation of Delta-Doped β-Ga2O3 Field Effect Transistors
Nitish Kumar; Chandan Joishi; Zhanbo Xia; Sidhharth Rajan; Satish Kumar

Enhancement of the Electrical and Thermal Performance of AlGaN/GaN HEMTs Using a Novel Resistive Field Plate Structure
Bikramjit Chatterjee; Tae Kyoung Kim; Yiwen Song; James Spencer Lundh; Sang-Woo Han; Daniel Shoemaker; Jae Min Lee; Moon Uk Cho; Rongming Chu; Joon Seop Kwak; Sukwon Choi

Cell Tab Cooling System for Battery Life Extension
Heiner Heimes; Achim Kampker; Ahmad Mohsseni; Francesco Maltoni; Jan Biederbeck

Pool Boiling Experiment of Dielectric Liquids and Numerical Study for Cooling a Microprocessor
Omidreza Ghaffari; Francis Grenier; Jean-François Morissette; Martin Bolduc; Simon Jasmin; Julien Sylvestre

Near Field Radiative Emissivity Enhancement with Application in Electronics Cooling
Mine Kaya; Shima Hajimirza; Aliakbar Merrikh; Mehdi Saeidi

2018 7th Electronic System-Integration Technology Conference (ESTC)

(September 18–21, 2018)

Silver Sintering in Power Electronics: The State of the Art in Material Characterization and Reliability Testing
Marco Schaal; Markus Klingler; Bernhard Wunderle

Board Level Reliability Assessment of Wafer Level Chip Scale Packages for SACQ, a Lead-Free Solder with a Novel Life Prediction Model
Balaji Nandhivaram Muthuraman; Baltazar Canete

Thermomechanical Reliability of Large Wafer Level Chip Scale Packages (LWLCSP) Under Thermal Cycling Qualification Test
Balaji Nandhivaram Muthuraman; Baltazar Canete

Intelligent Power Module Featuring Optimised Active Gate Driver and IGBT Module Integration for Electric Vehicle Application
Mingliang Jiao; Yun Li; Jun Yu; Jia Xie; Pin Zeng; Zhenlong Zhao

Chip-Package-Board Reliability of System-In-Package Using Laminate Chip Embedding Technology Based on Cu Leadframe
Peter Fruehauf; Andreas Munding; Klaus Pressel; Michael Vogt; Patrick Schwarz

2018 IEEE 20th Electronics Packaging Technology Conference (EPTC)

(December 4–7, 2018)

Innovative Packaging Solutions of 3D System in Package with Antenna Integration for IoT and 5G Application
Mike Tsai; Ryan Chiu; Eric He; J. Y. Chen; Royal Chen; Jensen Tsai; Yu-Po Wang

Solder Resist Crack Resistance Process Characterization in BGA Package for Automotive Grade Reliability
Kesvakumar V.C. Muniandy; Chan Kheng Jin; J.L Peter

Package Integrity and Reliability Effects of Mold Compound Chemistry for Power Device Application
April Joy H. Garete; Matthew M. Fernandez; Reinald John S. Roscain

Millimeter Wave Resonator and Cavity-Back Slot Antenna in Fan-Out Wafer Level Packaging
Chen Zihao; Lim Teck Guan

Study on Bottom-Up Cu Filling Process for Through Silicon Via (TSV) metallization
Gilho Hwang; Hsiao Hsiang-Yao; David Ho Soon Wee

Upcoming EPS Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other techical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

Name: 2020 Pan Pacific Microelectronics Symposium (Pan Pacific)
Location: Waimea, HI USA
Dates: Feb 10, 2020–Feb 13, 2020

Name: 2020 21st International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Location: Kraków, Poland
Dates: Apr 26, 2020–Apr 29, 2020

Name: 2020 31st Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Location: Saratoga Springs, NY USA
Dates: May 4, 2020–May 7, 2020

Name: 2020 43rd International Spring Seminar on Electronics Technology (ISSE)
Location: Liptovský Mikuláš, Slovakia
Abstract Submission Date: Jan 20, 2020
Dates: May 13, 2020–May 17, 2020

Name: 2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)
Location: Lake Buena Vista, FL USA
Dates: May 26, 2020–May 29, 2020

Name: 2020 IEEE 70th Electronic Components and Technology Conference (ECTC)
Location: Lake Buena Vista, FL USA
Dates: May 26, 2020–May 29, 2020

Name: 2020 Third International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)
Location: Osaka, Japan
Dates: Jun 22, 2020–Jun 24, 2020

Name: 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC)
Location: Tønsberg, Norway
Abstract Submission Date: Feb 16, 2020
Dates: Sep 15, 2020–Sep 18, 2020

Name: 2020 26th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)
Location: Berlin, Germany
Abstract Submission Date: Apr 10, 2020
Dates: Sep 23, 2020–Sep 25, 2020

Name: 2020 66th IEEE Holm Conference on Electrical Contacts and Intensive Course (HLM)
Location: San Antonio, TX USA
Abstract Submission Date: Feb 8, 2020
Dates: Sep 30, 2020–Oct 7, 2020

Name: 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Location: San Jose, CA USA
Dates: Oct 4, 2020–Oct 7, 2020

MISCELLANEOUS

Benefits of IEEE EPS Student Membership

EPS Webinars—Exclusive free access to informative, current webinars resented by experts.
IEEE Spectrum Magazine—the flagship publication of IEEE, explores the development, applications and implications of new technologies.
myIEEE—an interactive web portal exclusive to IEEE Members which allows for the customization of the member experience using gadgets, RSS feeds, et. al.
IEEE.tv™—Internet television offering exclusive programming about technology and engineering.
IEEE memberNET—an online search and networking tool that enables members to connect with technical and engineering experts worldwide.
IEEE Potentials Magazine—the only student-focused magazine within all of IEEE!
What's New for Students—electronic newsletter for students and graduate student members highlighting resources and new benefits within IEEE.
IEEEXplore—discounted access to more than 3 million documents.
IEEE ResumeLab—an online service that allows IEEE members to develop a resume.
IEEE email alias—free for members with virus protection and spam filtering.
IEEE Discounts—membership pays for itself with as much as 50% off IEEE products.
Career Alerts—a weekly email containing career advice plus the job of the week from IEEE Job Site.
Job Site—helps to locate career opportunities easily and confidentially.
Mentorship—Approach senior professionals to become your career mentors.
Networking—Opportunities to network with professionals in electronics packaging.
Leadership Development—Opportunities for leadership development through special IEEE programs and organisation of student chapter activities.
(For details, please visit: www.ieee.org/benefits and www.eps.ieee.org).

It's Time to Renew Your IEEE Electronics Packaging Society (EPS) Membership!

EPS promotes close cooperation and exchange of technical information among its members and others through its technical conferences and workshops worldwide, peer-reviewed publications, technology webinars and online educational materials, and local networking via Chapter activities and collaboration with other organizations.

Visit our website (eps.ieee.org) for details on how EPS can help support your technical and professional growth. You'll find educational opportunities, conference listings, technical presentations, Chapter locations and contacts, opportunities for professional recognition through EPS and the IEEE Awards Program, including IEEE Senior member and Fellow grades, and much more.

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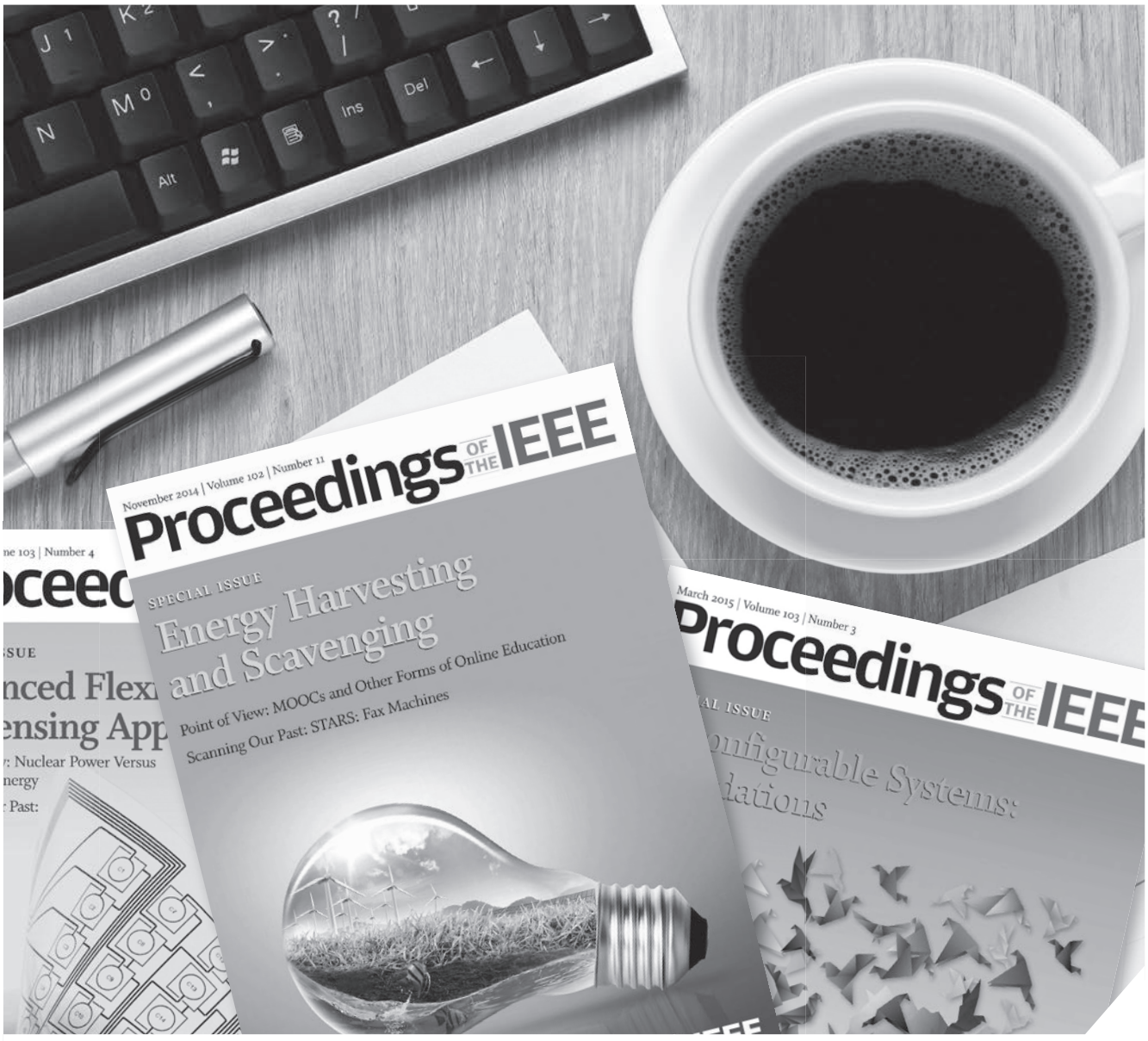

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1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

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