CHAPTER III

PROCESSING AND CHARACTERIZATION OF SOLDERABLE INTERCONNECTION OF POWER DEVICES

3.1 INTRODUCTION

The most critical challenge in today's power electronics packaging is the interconnection technology. Inside the state-of-the-art power modules, interconnection of power devices is accomplished with wire bonds, which are prone to noise, parasitic oscillations, fatigue and eventual failure. Bond wires are the major contributors to the package's resistance; approximately half of the total resistance for the power devices resides in the package components rather than the silicon. The objective of this research is to design direct copper interconnection technique for power electronics modules by eliminating the use of wire bonds. When compared to the wire-bonds, solder interconnects provide larger effective contact areas between power semiconductor devices and overlying power metallization. The larger contact area greatly reduces the current crowding and distributes the mechanical and thermo-mechanical forces over a larger area, thus reducing equivalent mechanical stresses at the device connections. Our thermal and electrical modeling work have suggested that direct solder interconnects will provide the highest packaging density, greatest number of I/Os, shortest possible leads, lowest inductance, highest frequency, best noise control, smallest device footprints, and lowest packaging profile - all of which are fundamental towards the implementation of a three-dimensional power module structure.

An advanced packaging technology must offer the following features:

- compact integration,
- minimized inductance, and
- improved reliability and ruggedness at a lower cost.

To eliminate wire bonds by using soldered post interconnects on the power devices (diodes and IGBTs) for enhanced electrical and thermal performances, we need to make the device contact pads solderable. However, circuits assembly and packaging technologies for power electronics have not kept pace with those of low-power electronics, like the packaging of integrated circuits (ICs). Currently, the IGBT manufacturers use aluminum contact pads, which are not solderable, and these manufacturers are making slow progress in fabricating devices with solderable contacts for commercial use. As a result, we investigated the available deposition techniques of solderable films on the aluminum contact pads of the power devices.

3.1.1 Significance of the Under-Bump-Metallurgy for Solderable Interconnection

Solder bump interconnect includes a under bump metallurgy and a solder bump. Underbump metallization is required to provide varied functionality for the packaging structures as discussed in the following paragraphs[1].

- **Adhesion to wafer passivation:** In most cases, the deposited metal layer should adhere to dielectrics such as nitride, oxi-nitride, oxide and a variety of polyimides. The UBM process requires that the dielectric layer is pin-hole free so that it can maintain the device functionality during the deposition and etching process.
- **Low resistance contact:** Low contact resistance is the most critical feature of a solder contact. A low resistant contact is achieved by the removal of the aluminum oxide layer from the device contact pads with a plasma or chemical etching process. The deposition and the etching process must be controlled to

eliminate the possibility of reformation of aluminum oxide, contamination on the device pads, and oxidation of the deposited layers.

- **Solder diffusion layer:** In a UBM process, there need to be a barrier layer for solder diffusion into the final metallization. Researchers have shown that a solderable diffusion barrier layer such as Ni, provides a more robust and flexible solder joint[1]. Some of the old bumping processes includes a solder with a very high Pb content and only 3-5% Sn content. As a result, the formation of a Sn intermetallic was not a critical issue in those schemes. However, in today's bumping technology, the most commonly selected solder is the Pb-Sn eutectic and as a result, the UBM diffusion layer must be robust enough for the Sn content of the solder. A solderable diffusion layer would prevent the possibility of de-wetting of the solder bump from the UBM structure, which is evident in a UBM structure without a solderable diffusion layer such as TiW and Cr. In a process with a TiW-Cu structure, it is extremely difficult to control film stress and barrier integrity. Since TiW is not solderable, if the copper layer is too thin, it is possible that all of the copper will react with the solder and create a Cu-Sn intermetallic. During multiple reflow of the joint, the solder bump will lose adhesion and eventually cause failure. On the other hand, if a thick copper layer is deposited, solder joints will contain excessive copper, which will require a high temperature reflow and may cause reliability problem due to the formation of excessive Cu-Sn intermetallics.
- **Final solderable metal layer:** The final layer of the UBM must be solderable. The challenge in the final layer deposition is its interaction with the underlying diffusion layer. In the cases, where the diffusion barrier is not solderable, a thick final metal layer is required. For example, in most plating oriented UBM processes, a minimum 20 micron thick copper layer is deposited since the barrier layer underneath copper is not solderable. This thick copper layer creates an excessive Sn-Cu intermetallic upon reflow of a Pb-Sn eutectic solder. Typically, the Sn-Cu intermetallics are brittle, which causes delamination at the UBM-dielectric interface and solder fatigue and failure under power and thermal cycling operations. As a result, the intermetallic thickness should be reduced to improve solder joint reliability.
- **Protection of IC metal from the environment:** An important function of the UBM is the protection of underlying final metal from environmental degradation. This protection feature is sometimes achieved in conjunction with other packaging steps such as underfilling and silicone encapsulation.
- **Minimize stress on silicon:** The underbump metallization should not exert excessive stress on the underlying device. In some cases, the stress caused by a thick UBM structure can be excessive enough to create a fracture or cratering of the silicon, as shown in Figure 3.1.1. Researchers have noted this phenomena as an indication of excellent adhesion of the UBM to the contact pad metal. However, just as in the case of wire-bonding, the cratering of silicon is mostly considered as a reliability issue of solder interconnection. The silicon cratering phenomenon is more pronounced in an electroplated thick copper UBM scheme, where the residual stress of the thick copper layer along with the CTE mismatch induced stress during solder joining causes the silicon cratering.

Figure 3.1.1. Cratering in silicon[1]

A crater created by a high-stress electroless Ni UBM structure is shown in Figure 3.1.2, as a result of a bump-shear test. According to bump-shear test specification, the only acceptable failure mode for solder bump is a failure within the solder layer; a delamination for the solder from the UBM or the cratering of silicon is not an acceptable failure from a reliability point of view.

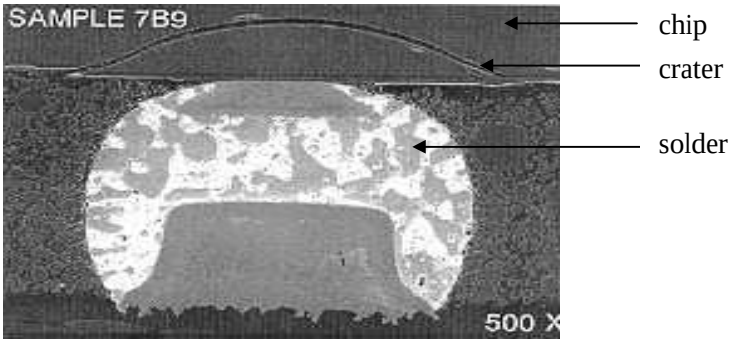


Figure 3.1.2. Si cratering due to thick plated copper bump[1]

- **Ability to bump probed device:** In a standard device fabrication scheme, fabricated devices are immediately probed after their production for their functionality. IGBT dice that we received from the manufacturer also contained probe test marks on every single die. Figure 3.1.3 shows a UBM structure in combination with a solder paste bumping process, which is capable of bumping probed devices. A UBM scheme that allows bumping after probing maintains the standard flow of metallization scheme. However, bumping over probed device pads can produce irregularities such as voids in solder bumps. If the probe damage is severe, a thin film UBM deposited via sputtering or evaporation process would not be able to cover the cavities in most cases.

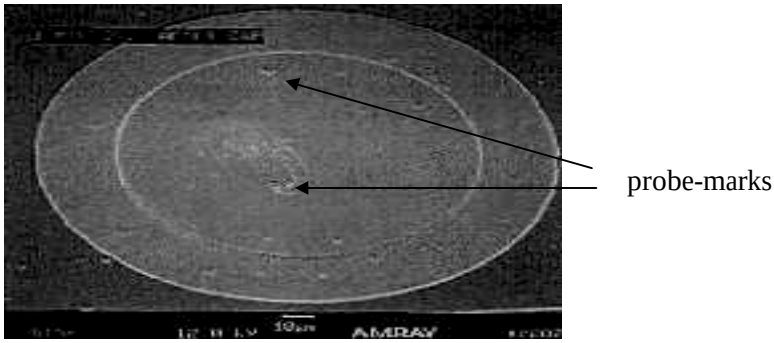


Figure 3.1.3. UBM on over-travelled probe marks on the device pad[1]

3.1.2 Available UBM Schemes for Solder Interconnection of Devices

In the following paragraphs a few common metallurgy used in forming bumps by different researchers are discussed. IBM invented the first metallization scheme for alternative device interconnection in the early 1960s. IBM recognized wire-bonding as a manual intensive, unreliable and expensive technique for device interconnection, which would become a limiting factor in high density packaging[2]. As an alternative interconnection, they designed a scheme called C4 (controlled collapse chip connection), which is a silicon chip to substrate attachment technology. Since then, the C4 infrastructure has evolved and fully developed in becoming the state-of-the-art device interconnection scheme. The actual C4 process has not changed significantly since its inception to IC packaging. However, depending on the surface chemistry and application, the original scheme can be used with minor modifications. Figure 3.1.4 depicts the process steps in fabricating a C4 metallization and its subsequent attachment to a multilayer ceramic carrier.

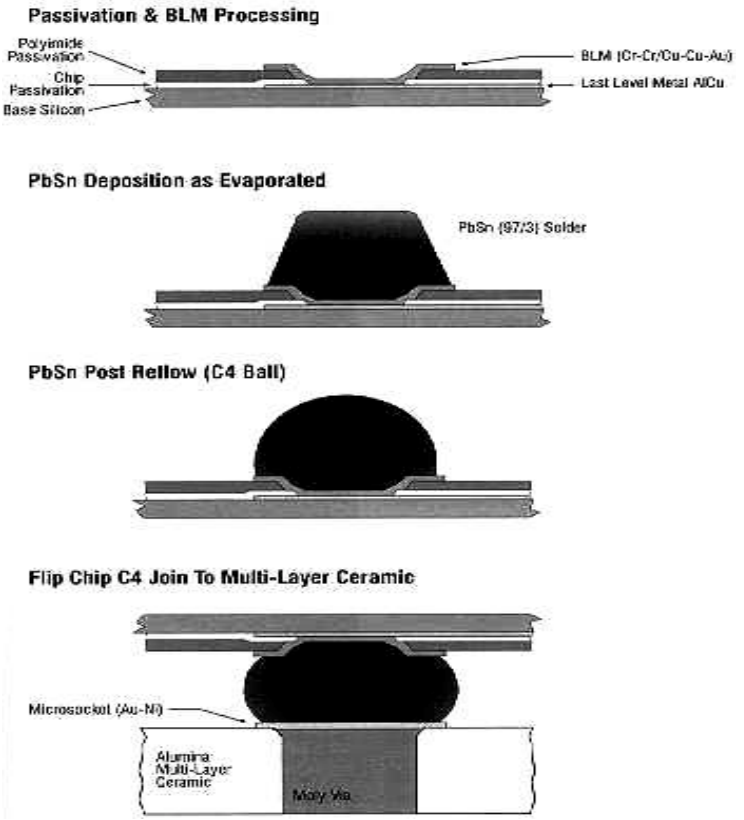


Figure 3.1.4. Process flow of IBM C4 technology[2]

The C4 bonding scheme is employed at the wafer level with an under-bump metallization (UBM) of a chromium-chrome/copper-copper/gold multilayer structure. Cr layer is deposited as an adhesion layer to the contact pad, while the Cr-Cu phased metallurgy is deposited to enhance intermetallic adhesion. As a final step, Cu is deposited as the conductor layer followed by a flash coating of Au to prevent oxidation and corrosion of Cu conductor. Next, the solder bumps are deposited via evaporation or plating technique. The wafer is then placed in a hydrogen furnace and reflowed to create the spherical balls.

Delco Corporation and Flipchip Technologies have implemented an Al-NiV-Cu underbump metallurgy in their *Ultra*CSP package, which is shown in Figure 3.1.5[3,4]. The first Al layer has excellent adhesion to the original Al bonding pad on the device. This layer is also used to relieve some stresses caused by the probe marks on the bond pads. The nickel-vanadium layer serves as the barrier layer for solder diffusion. At the same time, this second layer provides a solder wettable layer. Finally, a copper layer is sputtered for the final solderable metal. The top copper layer protects the underlying Ni-V layer and gets consumed entirely during the soldering process. Once the entire scheme of underbump metallization is sputtered, the layers are patterned with photoresist and etched to leave metal only on the bonding pads of the devices. The adhesion of the underbump metallization is extremely crucial to the reliability of this solder-bumping protocol. Shear tests have shown excellent adhesion of this metallization to the device pad while the only mode of failure has been found in the shear of bulk solder, indicating that the bulk solder is the weakest part of the entire package. Most of the failure modes are lifting of the metal and silicon cratering. Similar defects are observed in conjunction with TiW and electroless Ni-based UBMs, which suggests a weakening of the system by the bump structure and process. Flipchip Corporation has reported typical bump resistance with the entire UBM (Al-NiV-Cu) in the range of five to ten milliohms. In their UBM system, the thin copper layer is used only to promote wettability and protect the underlying Ni-V layer prior to bump formation, and hence, the solder directly wets the Ni-V layer. When a eutectic solder is used for bump-formation, a very thin Cu_5Sn_6, Cu_3Sn

and Sn_3Ni_4 intermetallic layer is formed; however, as the reflow numbers are increased, only Cu_5Sn_6 and Sn_3Ni_4 intermetallics are observed, thus maintaining the integrity of the Ni-V layer.

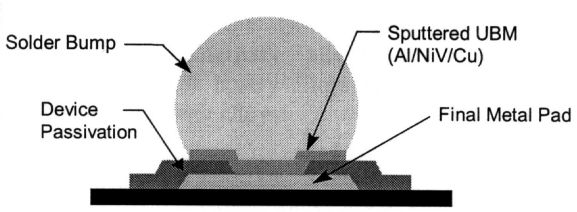


Figure 3.1.5. Delco Electronics and Flipchip Technologies' *Ultra*CSP package[3]

Motorola, Texas Instruments, National Semiconductor and United Microelectronics Corporation (UMC) have employed an underbump metallurgy of TiW (0.1-0.2μm) and Cu (0.5-0.8μm) via sputtering[5]. The sputtered copper is thickened with an additional 8-10μm of electro-plated copper. As a final process step, eutectic Pb-Sn solder is plated on copper, which is then reflowed to form solder bump (as shown in Figure 3.1.6).

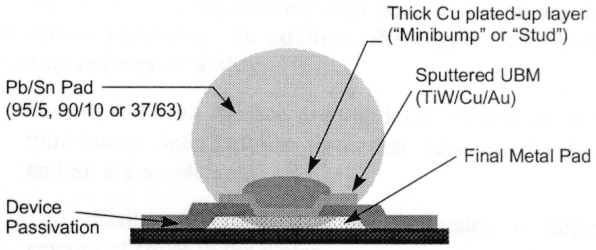


Figure 3.1.6. Thick plated Cu bump used in Motorola, TI, National Semiconductor and UMC[4]

Fujitsu's *Super*CSP (SCSP) is a molded wafer-level chip scale package, which is shown in Figure 3.1.7. On the nitride passivation of dice, a thin layer of polyimide is coated for adhesion and protection. Copper traces are plated and patterned on top of polyimide layer to distribute the I/Os. The first level interconnection between the Al pads on the dice and the copper traces are made by sputtered Ti-Ni. The UBM of the bonding lands on the other end of the copper traces is plated Ni and Pb-Sn solder. As a result, on the bonding pads of the second level interconnects, thicker metal posts (which consist of plated Cu and plated second level UBM) are formed. Eutectic solder balls are mounted to the UBM as package terminals and then reflowed by the conventional SMT method.

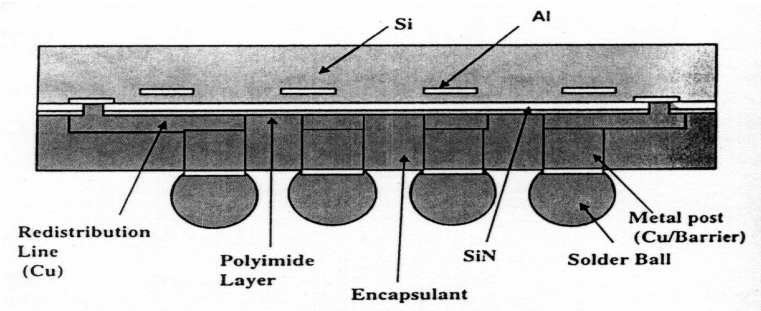


Figure 3.1.7. Fujitsu's *Super*CSP package[5]

Mitsubishi's CSP is flipchip die with a molding encapsulation. The first level interconnects are sputtered TiN on the bond pads. A Ni-Au layer is deposited on top of TiN layer to form the UBM. Package terminals consisting of inner high-lead content solder, transferred copper trace, and external eutectic solder bumps are placed on the UBM.

In NuCSP package (as shown in Figure 3.1.8), introduced by EPS, a thick copper layer is deposited by electro-plating as the final layer. However, the layer underneath copper is a non-wettable solder diffusion layer, and as a result, if a eutectic Pb-Sn solder is used, the thick copper layer forms an excessive Cu-Sn intermetallics, which are brittle and would reduce the solder fatigue life of the solder joint.

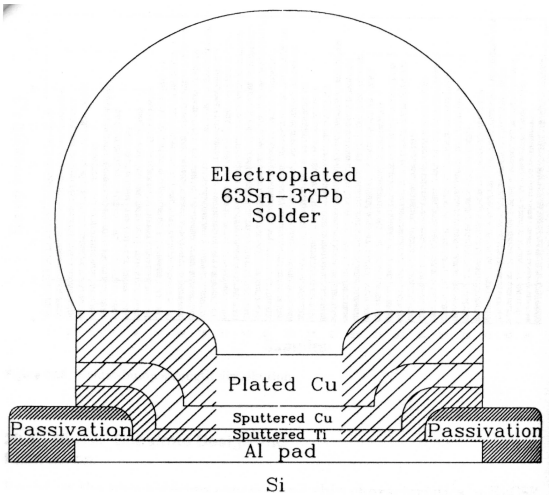


Figure 3.1.8. Electroplated solder in a NuCSP package from EPS[5]

Recently, Epoxy technology has patented a chip assembly process, known as Polymer Flip Chip (PFC), which uses electrically conductive adhesive interconnects for assembling a flipped device[6]. In this technique, the conductive adhesives are printed on the device pads as opposed to sputtering or evaporation in a C4 technique, thus resulting in high productivity, low temperature processing, materials savings, reduction of process steps and cleanliness to the environment. However, the conductive epoxy cannot be dispensed or printed directly on top of the aluminum pad without a pre-treatment. The native aluminum oxide on top of an aluminum pad is highly insulating and results in very unpredictable and unreliable electrical performance of the device if assembled as is[7]. In order to remove the detrimental effects of the oxide layer, Epoxy Technology uses a chemical UBM process to metallize the aluminum pads with a 10μm Ni-Au layer.

In recent years, to bring down the cost of metallization, wafer bumping by electroplating has been employed by Texas Instruments, Motorola, National Semiconductor and Fujitsu[5]. The plating technique is typically based on the same metallurgical system as in the case of C4 technique; however, it has been slightly modified for Pb-Sn eutectic solder. Electroplating is typically less expensive than the evaporation technique; however, excessive variations in the alloy control and bump height can exist. Also, in a plated bump technique, solder voids are more pronounced.

In an electroless Ni deposition scheme, batch processing can be achieved since masking is not necessary to define the metal contacts. Electroless plated nickel covers the entire pad and thus, increases the corrosion resistance. Moreover, nickel provides excellent solder wettability. The process involves a partial etch of the Al pad, followed by an activation treatment in an alkaline zincate solution. Once the nickel is deposited, a layer of gold is flash coated on nickel to prevent oxidation and promote solder wettability. However, the biggest concern of this process is the compatibility of the device with the plating solutions. During the electroless and immersion plating, the device is exposed to foreign materials, which can significantly affect the yield on an entire batch.

The following table summarizes the advantages and disadvantages of the common metallization schemes used in today's industry[8].

Table 3.1.1. A few common UBM schemes used in flipchip applications[8]

	Cr/Cu/Au	**Cr/Au**	**TiW/Pd/Au**	**TiW/Ni/Au**	**Cr/Cu/Ni/Au**	**TiW/Au**
Application	Low temp where PbSn soldering is required	Low temp	Medium temperature Good solderability	Medium temperature Good solderability	Medium temperature Good solderability	High temperature AuGe eutectic bonding
Advantage	Excellent electrical conductivity Solderability to PbSn and AuSn Non-magnetic film	Good electrical conductivity	Good electrical conductivity Solderability to PbSn and AuSn Non-magnetic film	Good electrical conductivity Solderability to PbSn and AuSn	Excellent electrical conductivity Solderability to PbSn and AuSn	Good electrical conductivity AuGe eutectic bonding
Disadvantage	Cu diffusion at AuGe Eutectic bonding temperature Low processing temperature	Not suitable for PbSn or AuSn soldering Cr diffusion at AuGe Eutectic bonding temperature Low processing temperature	Pd diffusion at AuGe Eutectic bonding temperature	Ni diffusion at AuGe Eutectic bonding temperature	Ni diffusion at AuGe Eutectic bonding temperature	Not suitable for PbSn or AuSn soldering
Temperature Limit	280°C for up to 0.5 hour	300°C for 1 hour	300°C for 1 hour	325°C for 1 hour	250°C for 1 hour	425°C for 1 hour
Solderability (PbSn)	Good	Poor	Good	Good	Good	Poor
Die Attach Method	PbSn, AuSn PbSn eutectic Epoxy	PbSn eutectic Epoxy	PbSn, AuSn PbSn eutectic Epoxy	PbSn, AuSn PbSn eutectic Epoxy	PbSn, AuSn PbSn eutectic Epoxy	PbIn eutectic AuSi eutectic AuGe eutectic Epoxy
Thickness	Cr 200-300Å Cu 500-2000μ" Au 20-100μ"	Cr 200-300Å Au 50-300μ"	TiW 200-300Å Pd 1000-2500Å Au 50-300μ"	TiW 200-300Å Pd 1000-2500Å Au 50-300μ"	Cr 200-300Å Cu 50-2000μ" Ni 35-75μ" Au 20-100μ"	TiW 200-300Å Au 20-300μ"

Based on the requirements and reliability considerations, we have employed three different metallization schemes with two different deposition techniques. The first UBM scheme involves physical vapor deposition of Ti-Ni-Cu and Cr-Cu via sputtering. The second UBM scheme includes an electroless process of Zn-Ni-Au metallization. Sputtered Ti-Ni-Cu and Cr-Cu and electroless Ni-Au layers provide low film stress with the following features:

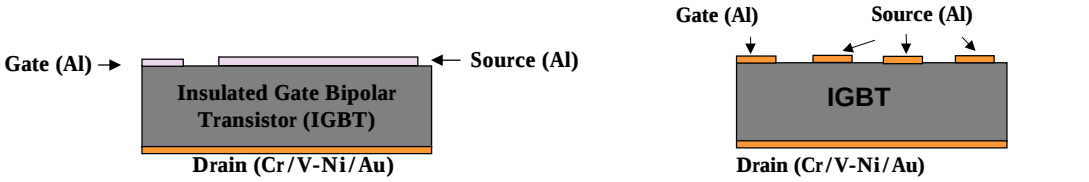
- CTEs of the low stress UBMs match the CTE of Al;
- ductility of copper is similar to the die pad material;
- precise deposition thickness control contributes to lower stress film; and
- UBM schemes allow for device probing before the metallization scheme.

As mentioned before, although the UBM metallizations are common for IC packaging, their implementation to power devices are still under-researched and therefore, optimization of the deposition processes plays a crucial role. In the following sections, process details of sputtering and the electroless plating schemes are presented.

3.2 EXPERIMENTAL WORK

3.2.1 Metallization of Device Contact Pads by a Sputtering Process

As mentioned before, our first choice for metallizing power devices was thin film deposition of Ti-Ni-Cu and Cr-Cu UBM systems by a sputtering process, which has been an industry practice since the invention of the C4 (controlled collapse chip connection) bonding technique at IBM. Figure 3.2.1 shows the cross-section view of the IGBTs; we notice that the gate and the source contact pads are not solderable; however, the drain contact for both the devices are solderable.



(a) Si_3N_4 passivated IXGD40N60A (b) Polyimide passivated IXSD35N120A

Figure 3.2.1. Cross-section schematic of IXYS IGBTs

Due to the differences of the pad geometries of the source, we needed to make different contact masks for the metallization process. The die-maps for both IGBTs are given below. IXGD40N60A IGBT has a Si_3N_4 passivation and contain one rectangular source pad and a small gate pad at the edge of the device, as shown in Figure 3.2.2 (a). On the other hand, IXSD35N120A device is coated with a polyimide passivation layer and the topside of the device contains six square source pads as well as a square gate pad.

(a) Si_3N_4 passivated IXGD40N60A (b) Polyimide passivated IXSD35N120A

Figure 3.2.2. Die-maps of IXYS IGBTs[9]

The metallization scheme by physical vapor deposition is divided in two parts - plasma cleaning and sputtering. In the following paragraphs, these processes are described.

3.2.1.1 Plasma cleaning

Cleaning processes designed to remove contaminants from surfaces of materials play a crucial role in many electronic manufacturing processes. If the contaminants are not removed, they can adversely impact assembly operations such as wire-bonding, soldering, bonding with adhesives and most importantly, the end use of the devices themselves. Therefore, surface pre-treatments are used to develop an adherend surface to optimize the bonding at the interface. This is implemented by the removal of a weak boundary, resulting in enhanced bond strength[10]. Weak boundary layers typically include weak oxide layers of metals, low molecular

weight species, release agents, and organic contaminants. Surface treatment may also modify the physical structure of the adherend surface, which plays a crucial role in mechanical interlocking mechanism in the adhesion process. Furthermore, preparation of the adherend surface can generate specific changes in the chemical nature of the surface to optimize absorption interactions at the interface. Chemical treatments, abrasion, solvent cleaning, vapor degreasing, grit-blasting, corona discharge and plasma treatments are some of the pretreatments commonly used.

Metallization process on the device contact pads will depend heavily on the quality of the surface. Typically, a surface preparation scheme is employed to achieve the desired surface quality. In general, these surface treatment processes are determined by the surface chemical composition. For aluminum contact pads (as in the case of IGBTs), oxygen, carbon and hydrogen contents govern the selection of a suitable chemical treatment since these elements have strong influences on adhesion, epitaxial growth and oxidation[11].

CFC based cleaning methods have been commonly used to remove hydrocarbon oils, greases and other contaminants from material substrates without leaving potentially damaging residues. However, the Montreal Protocol on ozone depleting chemicals has mandated the replacement of chlorofluorocarbon (CFC) based cleaning solutions[11]. Although several alternatives are available to replace the CFC based solutions, the effectiveness of these methods at removing organic contaminants is less than optimal. Additionally, many of these alternatives pose environmental, health and safety risks as well as increased costs. An effective alternative to chemical cleaning process is plasma cleaning, which allows the removal of surface contamination from material substrates while producing no undesirable health and safety hazards. With the continued shrinkage of package size, plasma gas has become the most effective cleaning method for electronic components. Advantages of plasma cleaning and etching over a wet chemical etching can be summarized as below.

- Plasma etching process leaves minimized residue left on the surface compared to wet cleaning.
- Plasma cleaning is more effective in removing organic contaminants than wet etching process.
- Plasma cleaning can penetrate small areas within a surface while the wet cleaning is dependent on surface tension to get to cavities.

With short processing time, hazard-less operation, and no waste disposal, plasma etching is more efficient and cost effective alternative to wet cleaning. Consequently, plasma etching is widely used in the electronics industry in the areas of semiconductor etching, photoresist stripping, hybrid, CSP, BGA, lead frames, hard disks and flat panel displays.

In our plasma cleaning process, we initiate the ionization of the gas by applying an energy field. Plasma systems typically use three source frequencies -- low frequency (<100 kHz), RF frequency (13.56 MHz) and microwave frequency (2.45 GHz). We used RF frequency since they exhibit significantly higher levels vacuum ultraviolet radiation and higher concentrations of electronically charged particles. RF plasma also produces more homogeneous process, which is critical in treating irregularly shaped and small dimension parts. Low temperature plasma works within a vacuum chamber where atmospheric gases have been evacuated typically below 0.1 torr. A low pressure allows a relatively long free path of accelerated electrons and ions. The ions and the neutral particles are near ambient temperatures, and the long free path of the electrons, which are at high temperature or electron-volt levels, have few collisions with molecules at this pressure.

Plasma Reactions can be classified into two categories – chemical and mechanical. Chemical reaction involves a chemical interaction of the plasma with the surface of the product or the contaminants on the surface. These reactions include oxidation and ablation of the surface with gases such as oxygen, fluorine and chlorine. On the other hand, mechanical reactions involve plasmas from noble gases such as argon and helium. These inert gases exist in their monatomic state, which makes the reaction a kinetic energy transfer resulting in a molecular scale sand blasting. The removed contaminants are typically swept away in the vacuum stream without being re-deposited. Polyimide passivated devices contain a polyimide coating;

therefore, to prevent oxidation of the polymer, we have selected an inert atmosphere plasma cleaning with oxygen free argon gas.

3.2.1.2 Sputtering

Once the pad surfaces are plasma cleaned, they are ready for sputtering. Figure 3.2.3 shows a schematic of the sputtering process inside the chamber, which allowed three different targets to be sputtered sequentially. This is particularly helpful since the chamber needs to be pumped down only once during the entire metallization process, thus minimizing the processing time. As mentioned before, we machined stainless steel/ceramic contact masks for sputtering, matching the pad openings on top of the IGBTs. These contact masks are placed on top of the device pads (as shown in Figure 3.2.4), thereby allowing only the opened area i.e. the contact pads to be sputtered.

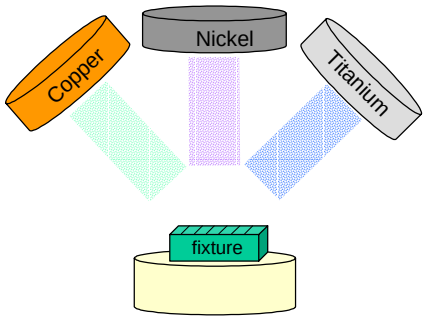


Figure 3.2.3. Sputtering process inside the chamber

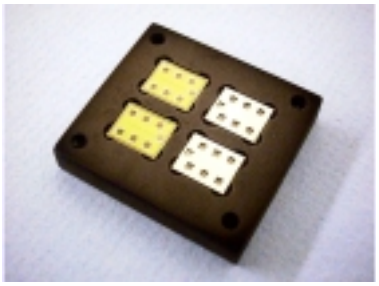


Figure 3.2.4. Sputtering fixture

We have implemented two under-bump metallization systems via sputtering – Ti-Ni-Cu and Cr-Cu. In each case, deposition parameters for sputtering individual metals were selected using the following calibration curves as shown in Figure 3.2.5. Typically, we sputtered 0.2-0.5μm of Ti/Cr as the adhesion layer, 0.5μm of Ni as a solder diffusion barrier layer and 1.5-2.0μm of copper as the final solderable layer.

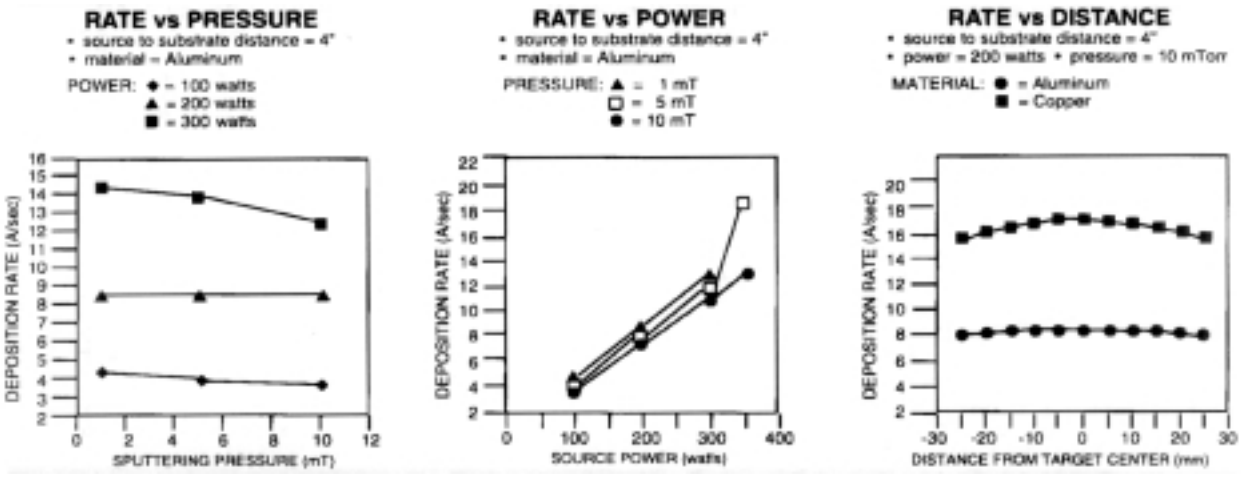


Figure 3.2.5. Calibration curves for the sputtering parameters[12]

3.2.2 Metallization of Device Contact Pads by Electroless Chemical Process

In addition to sputtering, we investigated the feasibility of electroless chemical deposition of under bump metallization (UBM) for subsequent solder interconnection. In the IC packaging arena, the UBM technique via eletroless Ni-Au deposition is well established and numerous metallization services are available for

making the IC devices solderable; however, in the power electronics packaging, only preliminary research work on the electroless plating process has initiated recently. In this research, our specific objectives are listed below:

- Investigate solder bump packaging techniques on power electronic devices
- Design plating procedure for low-cost consistent results
- Investigate UBM interaction and feasibility on bare aluminum bond pads

Once again, we have employed a cleaning process before the actual metallization process for the electroless deposition scheme.

3.2.2.1 Chemical Cleaning

Wet chemical techniques employ solvents designed to dissolve the organic and inorganic components or acids to lightly etch the surfaces where bonding is to take place. A typical wet chemical process uses inexpensive equipment, which makes it well suited for high production volumes. However, some of the major drawbacks of wet chemical etching include environmental and process hazards associated with the large volume of volatile chemicals. Moreover, the cleaning solutions tend to leave residues behind as well. Aqueous cleaning process is very useful in removing inorganic contaminants such as sodium and potassium; however, they also introduce microbial organisms, which causes metallization corrosion, organic surface interface problems and leakage currents. Considering the above-mentioned issues, we employed the following scheme of cleaning on the devices before metallization.

- Prepare bond pads with non-etch silicate free cleaner to remove oils, buffing compounds and inks,
- Mildly etch surface to produce bright, smooth surface with minimal dimensional change,
- Use light HNO_3 (nitric acid) solution to desmut surface,

3.2.2.2 Zincate Plating

Although the zincate plating process for subsequent Ni deposition on aluminum is a standard process in IC packaging, the applicability of this process to power device metallization was critical since the aluminum layer on the device contact pad is only ~3μm thick. The overall plating process is summarized below:

- Apply zincate solution to remove aluminum oxide and apply thick zinc film on bond,
- Immerse in low temperature nickel plating bath, and
- Protective Au flash coating on top of the Ni layer.

Figure 3.2.6 shows the process flow chart of the cleaning and the subsequent electroless Ni-Au deposition process on the power device pads. Zincating and the desmutting processes can be applied more than once depending on the desired thickness of the Zn and surface roughness of the Al pads.

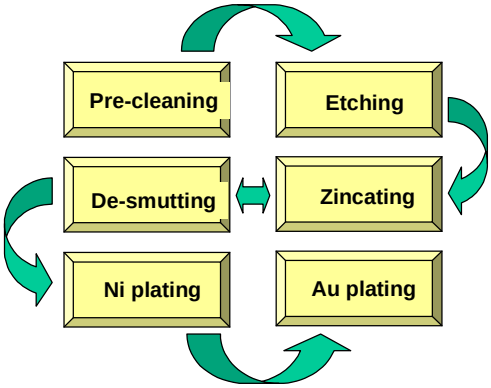


Figure 3.2.6. Electroless plating process flow

We employed manufacturer's specified chemical concentrations and plating times at different stages of the deposition process, which are listed in table 3.3.1. During the metalization process, on top of the Al metal, a thin layer of zinc is plated, which gets replaced by Ni ions during the nickel plating step. Consequently, Ni acts as an adhesion layer as well as solder diffusion barrier layer. The nickel layer also provides adequate adhesion strength for soldering, but typical lead-tin and copper-tin solders do not sufficiently wet the surface during the quick reflow times required for soldering to the thin metallization. As a result, a thin layer of gold is deposited on top of the nickel layer to prevent oxidation and to promote solder-wetting.

In an electroless deposition process, the major advantage comes in batch processing, as many devices can be successfully processed in a very short processing time. The electroless deposition process:

- provides an excellent adhesion base for solder bump joint,
- do not require a mask,
- provides low resistance between IC bond pad and solder bump,
- acts as a solder "wettable" material of appropriate thickness, and
- produces stronger and cheaper interconnects than the conventional wire bonds.

Table 3.3.1. Process parameters of the electroless deposition scheme

Process	Chemical Brand	Concentration	Temperature	Duration
Cleaning	ENPREP 35	15-45 gm/L	49-66^{o}C	1-5 min
Etching	ACTANE E-10	150 ml/L	71^{o}C	1-3 min
Desmutting	HNO_3 acid	50% by vol.	25^{o}C	2-3 min
Zincating	ALUMON EN	200 ml/L	25^{o}C	15 sec – 1 min.
Ni plating	ENPLATE NI-429M	200 ml/L	82^{o}C	20 min
Au plating	OROMERSE MN RTU	100% by vol.	60-70^{o}C	20 min

3.2.3 Solder Bumping Process for Post Attachment

With an optimized UBM scheme, it is essential to select an optimized solder reflow process for subsequent post attachment. The solder should:

- provide all deposited or printed solder on the chip,
- self center during the reflow, and
- collapse during the reflow process.

Selection of a Solder Deposition Process: The variety of solder flipchip approaches in use today spans a broad range of materials deposition techniques. Solder can be deposited via vapor-phase, liquid-phase, solid-phase and electrochemical techniques. The method of solder deposition depends on the selected solder alloy.

Evaporation of solder is the most successful bump formation method to date as it has been used by companies such as IBM, Motorola, Mitsubishi, Fujitsu and NTT[13]. In spite of the wide acceptance of solder evaporation technique, it has certain limitations involving fine pitch resolution through metal mask evaporation. Also, as the size of wafers are increasing, they would require large vacuum chambers which may not be economically feasible. Moreover, an evaporation process can be relatively slow and quality problems may result from damage to the solder bumps in the metal mask removal process with the plugged holes.

In an electrochemical deposition process, solders are deposited using an electrolyte containing ionized metal atoms. Electrolytic and electroless plating are the common methods, which have gained much popularity in recent years for their suitability toward volume production. However, device structures can be extremely sensitive to the electro-chemical baths and as a result, these processes require extreme control to

maintain the desired chemical state of the chemical solutions[14]. The electroplating process involves a blanket deposition method, which demands an etching process to remove the shorts between pads.

Stencil or screen printing of solder paste is a well proven process for surface mount components. Delco Electronics has pioneered the use of this deposition technique for flipchip applications. Figure 3.2.7 shows the solder deposition process using a stencil printing. Stencil thickness needs to be less than the aperture diameter, which sets a practical limit on the bump diameter. However, the stencil can not be too thin either since the squeegee motion may damage or even break the stencil. In this deposition process, stencil needs to be aligned with the pads on the device, which assures printing accuracy.

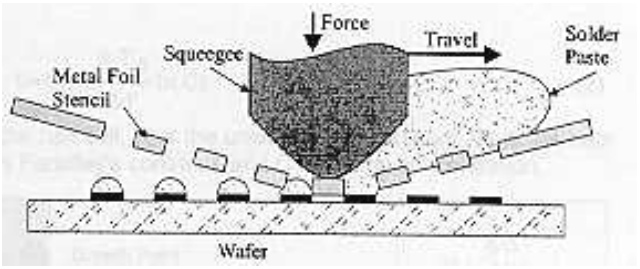


Figure 3.2.7. Stencil printing process for solder deposition[4]

Selection of Solder: Researchers have shown that UBM systems compatible with eutectic Pb-Sn solder are also compatible with high-lead content solders, but not the other way around[15]. The industry standard Cr-Cu UBM was primarily designed for high Pb content solder, which does not provide sufficient reflow cycles. However, in recent applications with UBM, Pb-Sn eutectic solders are primarily used. Tin diffuses readily into copper, as a result, either a thick copper layer or a solder diffusion barrier layer is essential in the UBM structure[16]. Nickel has been selected by researchers in many UBM applications as a barrier layer. The ability to deposit nickel selectively by electroless plating process is considered as a major cost-saving approach for UBM formation[17].

Selection of an alloy is not quite obvious from the literature. Many groups have researched into the topic of alloy selection with a reliability cost consideration. References could be cited to support virtually any solder alloy as superior to other. This is due to the fact that microstructures of most solders are thermodynamically unstable and are continuously changing as a function of thermal and power cycling stresses. In most practical applications, thermal history and geometry of a solder joint play a more significant role in the reliability determination than the alloy composition[18]. Moreover, from an overall reliability point of view, it is widely accepted that the deposited UBM governs the reliability factors to the greater extent than any of the solder process parameters[19,20,21,22,23]. In this research, for the solder-reflow process, a paste form of solder is preferred since the alloy composition of a solder can be precisely controlled to ± 1%. Improper alloy composition can change the liquidus temperature of the solder and result in incomplete wetting to the solder to the device pad metallization. Solder paste allows a repeatable, controllable and high-yielding process for achieving electrical contacts.

Accordingly, we have selected a Pb-Sn eutectic solder paste with no-clean flux to form the interconnect along with the UBM; at the same time, a low cost stencil printing of solder is selected as a deposition method. Placing the bumps in the center of the pads and increasing the joint height by attaching posts will further improve the solder fatigue properties[24]. Figure 3.2.8 shows a soldering fixture where multiple devices can be reflowed in a controlled environment for the post attachment process; while Figure 3.2.9 shows actual photographs of a few posted polyimide passivated IGBTs.

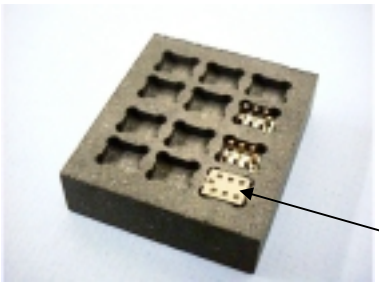


Figure 3.2.8. Soldering fixture for post attachment

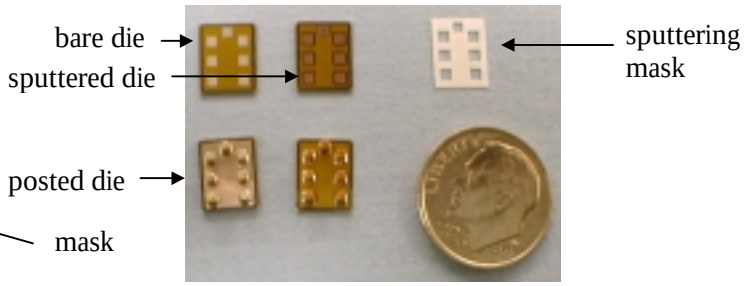


Figure 3.2.9. Post-attached IGBTs

Finally, in Figure 3.2.10, a cross-section schematic of a soldered device pad (without post attachment) is shown.

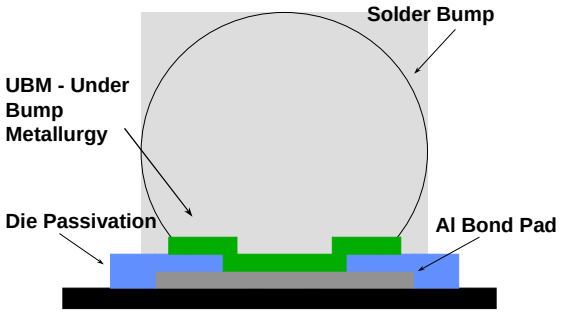


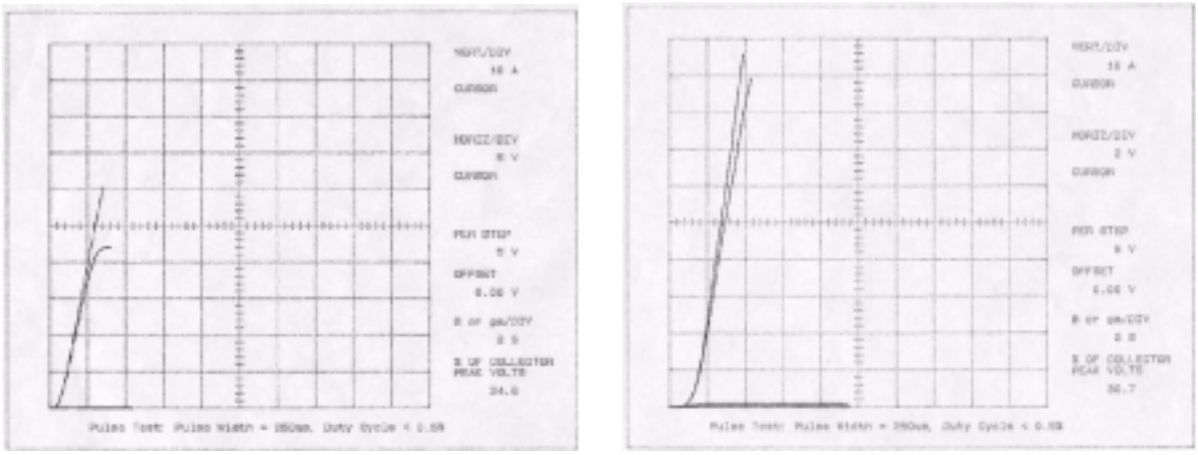
Figure 3.2.10. Cross-section view of a solder-bump on a device pad[3]

3.3 ELECTRICAL CONTACT RESISTANCE TEST RESULTS

Developing a process of metallization for power devices is one part of the solution for three-dimensional packaging; the performance of the new technology will eventually determine the breadth of its application. As time progresses, reliability data will be collected based on the performance shown on the structure under thermal and power cycling. As a result, this research is limited to establish the design rules of the solder interconnect technology. Preliminary test results look promising for the Si_3N_4 passivated devices; however, polyimide passivated devices yielded inconsistent test results. Test results for both types of devices are discussed below.

As mentioned in chapter 2, in the 1st phase of module fabrication with Si_3N_4 passivated IGBTs, we had successfully fabricated packaged devices and modules using the MPIPPS technique. These modules were tested and operated at pulse-switch and high power stages up to 6kW. However, in the 2nd phase of module fabrication with polyimide passivated devices, we experienced significant yield problems due to metallization difficulties of these devices. Only a few packaged devices and modules passed the pulse-switch test while none passed the high-power stage test. In this section we present contact resistance test data on packaged Si_3N_4 passivated and polyimide passivated devices under the exact same metallization schemes.

Curve tracer test results of the metallized (sputtered as well as electroless deposited) and post attached Si_3N_4 passivated devices are shown in Figure 3.3.1. Comparing these data with the specification of a bare Si_3N_4 passivated die, we notice that there was no effective differences induced by any of the metallization processes.



(a) Ti-Ni-Cu sputtered IXGD40N60A (b) Ni-Au plated IXGD40N60A

Figure 3.3.1. Comparison of forward bias characteristics of a sputtered and a plated IXGD40N60A IGBTs

On the other hand, metallization proved to be significantly problematic for the polyimide passivated devices. First of all, the sputtered devices showed sporadic electrical contact resistance after metallization. Of the six source pads on the top of the devices, few pads would show low resistance while the others would exhibit extremely high resistance. Results were even worse for the electroless deposition scheme. After the plating process, the breakdown voltages of these devices lowered significantly, in some cases, the breakdown voltage dropped from 1200V to as low as 400V. On the plated polyimide passivated devices, we noticed that the plating solutions had created small holes through the polyimide coating around the pad area, thus degrading the device characteristics and making them unusable. Figure 3.3.2 shows the schematic of the contact resistance measurement scheme with a probe station and a curve tracer for the polyimide passivated devices while the test results of a few packaged devices are listed in Table 3.3.1.

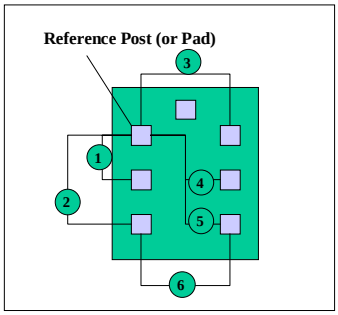


Figure 3.3.2. Contact resistance measurement scheme for polyimide passivated IGBTs

Table 3.2.2. Measured contact resistance results of a few polyimide passivated IGBTs

Device	Measured Resistance Data (ohm)					
	Pad 1	*Pad 2*	*Pad 3*	*Pad 4*	*Pad 5*	*Pad 6*
1	0.2	0.3	0.3	0.3	0.4	0.4
2	3.0	4.0	2.0	3.0	2.9	1.4
3	346	1928	2293	1700	47	72
4	8.5	800000	800000	8.1	79	77
5	27	28	0.6	12	8.8	8.7
6	0.3	0.3	0.3	0.2	0.3	0.3
7	0.2	0.2	0.2	0.2	0.2	0.2
8	0.2	0.2	0.2	0.2	0.2	0.2

3.4 CHARACTERIZATION RESULTS

3.4.1. SEM Characterization Results

Inconsistent and high contact resistance results of the polyimide passivated devices required systematic investigation of the surface characteristics – before and after the metallzation and soldering process. First, SEM characterization was performed on the high and low contact resistance devices to obtain a comparison between the two types of devices.

3.4.1.1 SEM of High and Low Contact Resistance Devices

In the case of sputtered and packaged polyimide passivated devices, we have noticed high contact resistance with probe-station measurement. However, silicon nitride passivated devices with the same UBM do not show higher resistance. One of the sputtered-soldered polyimide passivated IGBTs was placed in an epoxy matrix and then polished to image the cross-section interfaces. Figures 3.4.1 and 3.4.2 show porous delaminated interface between the UBM and the aluminum film on the device pad. The finite gaps between these two layers result in high contact resistance, eventually leading to device failure during electrical and thermal stress test. The observed delaminations are not seen in the sputtered device cross-section (as it will be shown later in section 3.4.2.3); the delaminations occur during the soldering process due to poor adhesion of UBM to the Al metallization on the device pad. During the reflow of Pb-Sn solder on UBM, the solder tends to pull out the UBM from the Al pad. Consequently, if the adhesion of UBM (specifically Ti on Al) is insufficient to withstand the induced stresses during the solder reflow process, UBMs would detach from the Al (as in the cases of polyimide passivated devices).

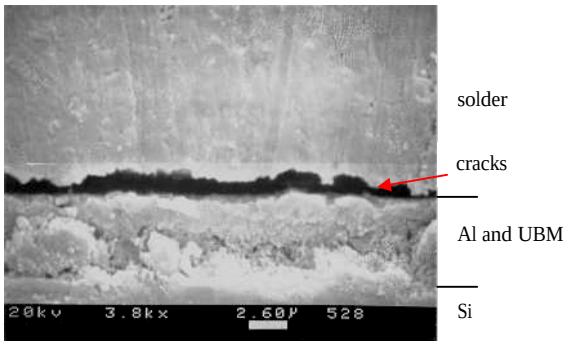


Figure 3.4.1. SEM image of a delaminated interface

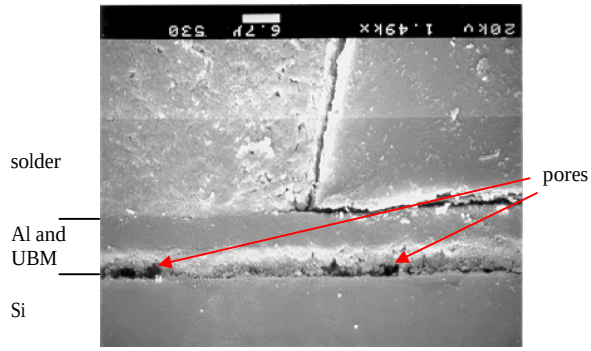


Figure 3.4.2. SEM cross-section of an soldered interface

Another sputtered (Ti-Ni-Cu) and Pb-Sn solder bumped polyimide passivated IGBT, which showed low contact resistance, was prepared for cross-section imaging. Figure 3.4.3 illustrates a cross-section of such an interface; the film layers are continuous and distinct. We noticed that the underbump metallurgy has produced Cu-Sn intermetallic when reflowed with solder.

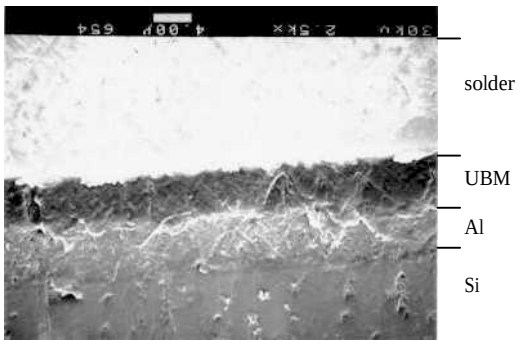
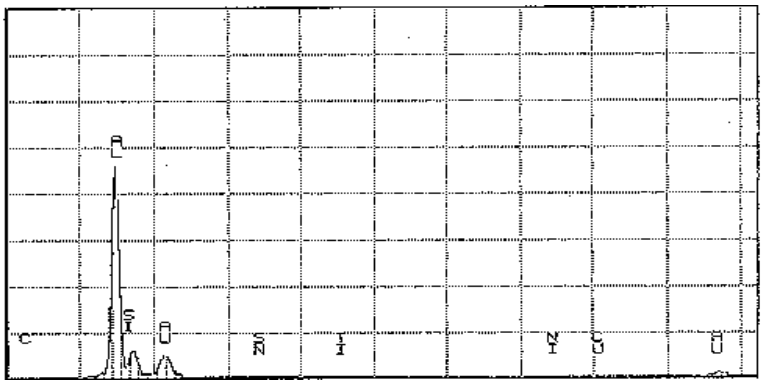
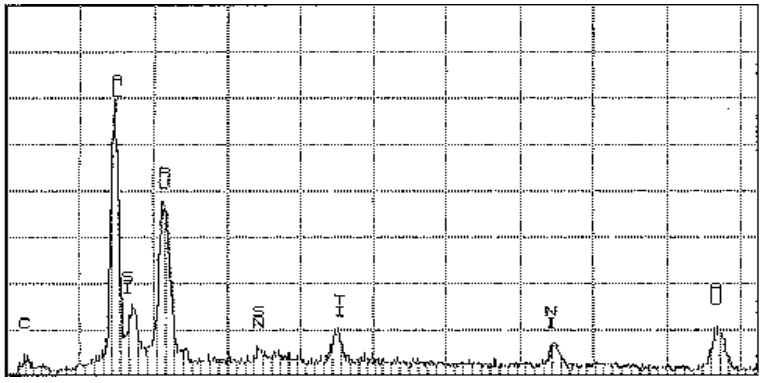


Figure 3.4.3. SEM cross-section of a Ti-Ni-Cu sputtered and eutectic Pb-Sn soldered polyimide passivated IGBT

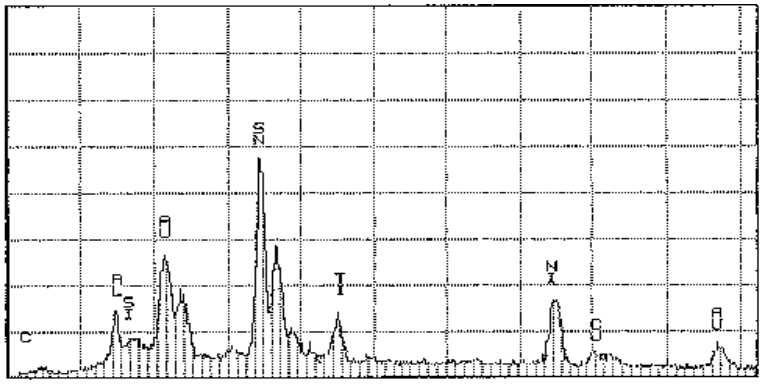
Scanning across the fractured interfaces (from the top aluminum layer to the base Si material) for the same sample (Ti-Ni-Cu sputtered and Pb-Sn solder bumped polyimide passivated IGBT) with EDX revealed the following plots as shown in Figure 3.4.4: plot (a) shows the materials close to the area of the device to Al interface. Within that area, only Si and Al are detected. In plot (b), we observe strong peaks of Al as well as peaks of Ti, Ni and Sn. Copper peak is not pronounced in the UBM-Al interface since all of the sputtered copper gets dissolved with the reflow of Pb-Sn solder. Moving further away from Si, in plot (c), we notice strong peaks of Sn. Small traces of Ti, Ni and Cu are visible. In all three regions, traces of Au are detected since the EDX specimen was coated with a very thin layer of sputtered Au layer.



(a) Si-Al area



(b) Al-UBM area



(c) UBM-Solder area

Figure 3.4.4. EDX scans at different locations of a sputtered-soldered polyimide passivated IGBT

As mentioned before, silicon nitride passivated IGBT devices consistently showed low contact resistance (same as a bare die) when tested at the probe station. Hence, samples were prepared for comparison with the polyimide passivated devices. Figure 3.4.5 presents an optical microscope image of a soldered post on an silicon nitride passivated IGBT; excellent wetting of the solder with the UBM as well as to the post interconnect is observed. Figure 3.4.6 shows a cross-section SEM image of solder-UBM-Si interfaces of an silicon nitride passivated device with a soldered post on top of the contact pad. We notice that the layers are uniform and contain no discontinuities as observed in the case of polyimide passivated devices.

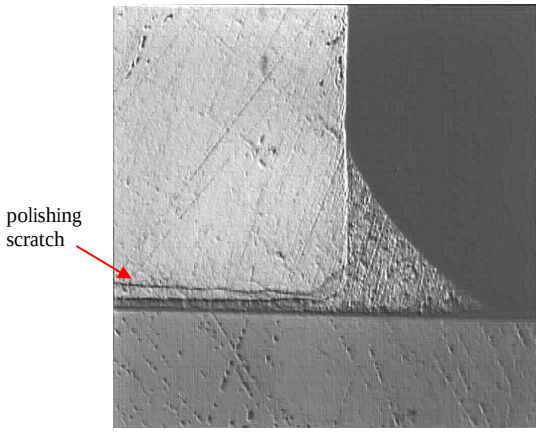


Figure 3.4.5. Microscope image of a soldered post

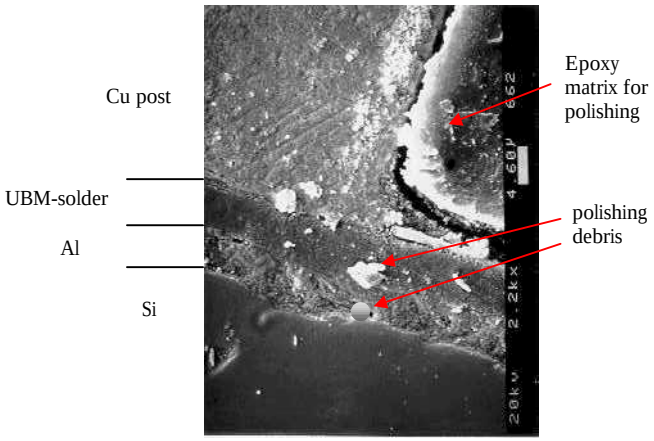


Figure 3.4.6. SEM image of a soldered post

From the above SEM investigations, silicon nitride passivated devices consistently showed smooth and continuous interface while the polyimide passivated devices exhibit porous and weak interfaces. At this point, we initiated a SEM investigation on the fractured bare dice of silicon nitride passivated and polyimide passivated IGBTs.

3.4.1.2 Results on Fractured Bare Devices

To identify the failure mechanism of adhesion and subsequent higher contact resistance, we employed SEM and EDX micrography of fractured device samples. In the following sections, selected images of bare and sputtered IGBTS are presented for establishing comparison between IXGD40N60A (Si_3N_4-passivated) and IXSD35N120A (polyimide-passivated) devices from IXYS.

First, we fractured as-received silicon nitride passivated and polyimide passivated devices from the manufacturer. Both devices are fractured through the source pad to provide metallization layer information. The SEM image (Figure 3.4.7) shows a delamination of Al layer from the Si surface due to the fracture bending.

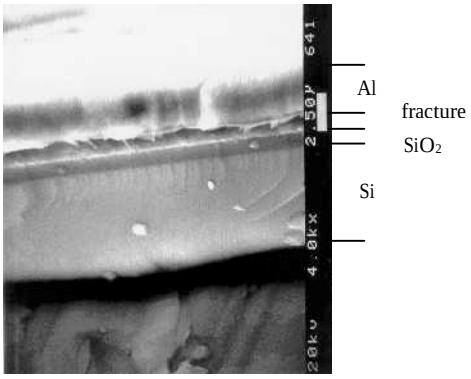


Figure 3.4.7. SEM of a polyimide passivated IGBT

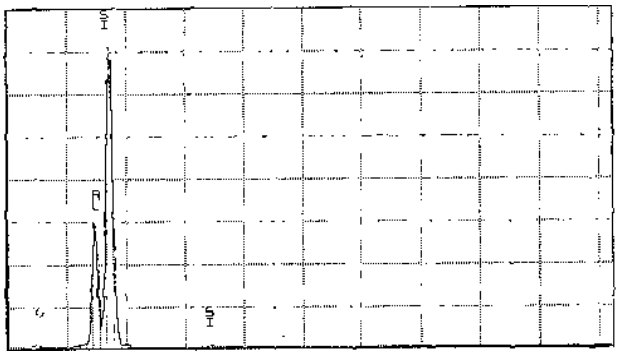


Figure 3.4.8. EDX plot of a polyimide passivated IGBT

The three distinct successive layers of Si, SiO_2, and Al are present in the cross-section, which is also verified with the EDX plot (Figure 3.4.8) of materials identification. The aluminum layer is measured to be 3 micron thick, which corresponds well to the manufacturer's specification. On a silicon nitride passivated IGBT, we see a similar structure as in the case of polyimide passivated IGBTs (as shown in Figure 3.4.9). EDX materials identifier is scanned across the fractured interface and the identified materials are plotted in Figure 3.4.10. Once again, we notice a tri-layer structure of Si, SiO_2, and Al at the cross-sectioned device interface. The Al layer is measured to be 2.5 micron thick.

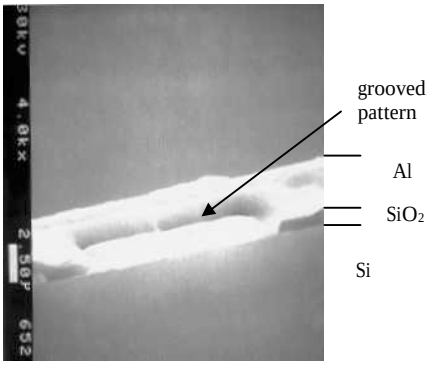


Figure 3.4.9. SEM of silicon nitride passivated IGBT

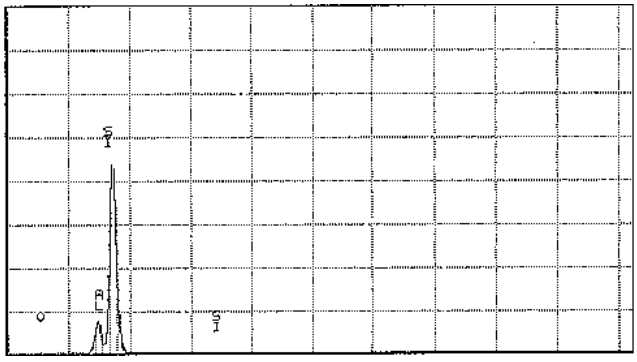


Figure 3.4.10. EDX plot of a silicon nitride passivated IGBT

In Figure 3.4.9, we observed a grooved pattern on the Al metallization. Therefore, we further investigated the surface patterns on the metal pads of the device. In Figure 3.4.11, we notice that the metal and the oxide layers form an inter-leaved pattern throughout the fracture line.

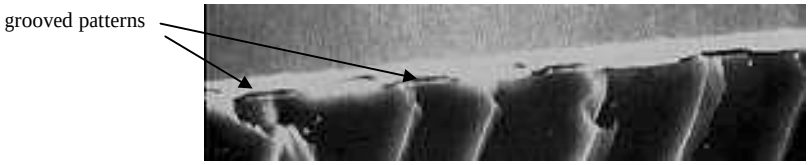
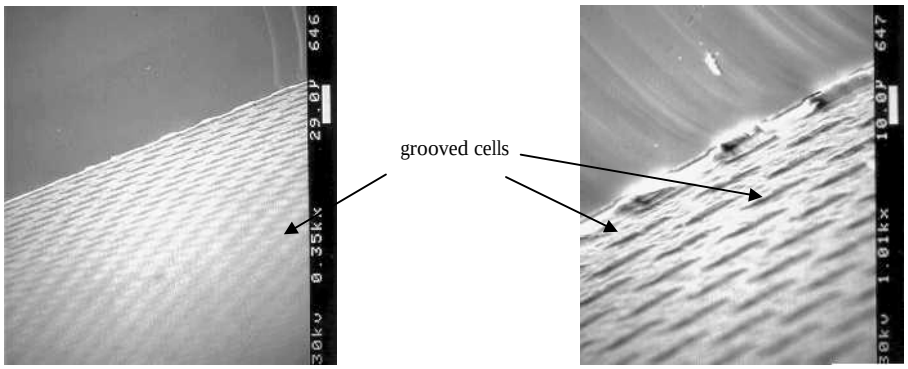


Figure 3.4.11. Grooved patterns on the Al metallization

We further examined the surface texture of the aluminum contact pad as well as the passivation layer for the silicon nitride passivated device. Figure 3.4.12 indicates that the groove patterns are all over the surface area of the metallization and the passivation layer.



(a) aluminum pad (b) Si_3N_4 passivation area

Figure 3.4.12. SEM image of the surface contour of a silicon nitride passivated device

On the polyimide passivated IGBT, we observe similar cell patterns across the metal pads and along the polyimide passivation layer. In this case, the cells or the grooves are much larger than those of silicon nitride passivated device (as shown in Figures 3.4.13 and 3.4.14).

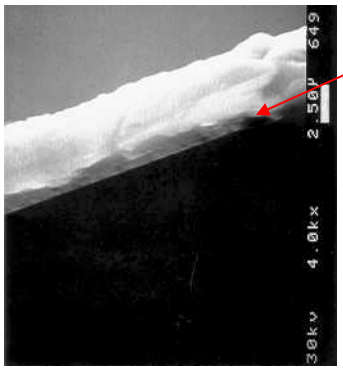


Figure 3.4.13. Cell patterns on an polyimide passivated IGBT

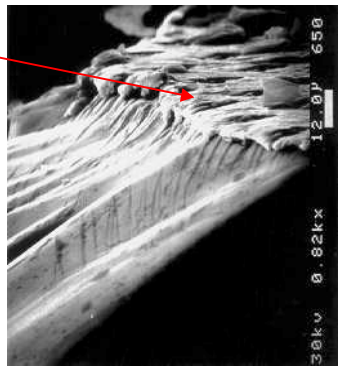


Figure 3.4.14. SEM of run-off cell surfaces

However, one feature is noticeably different in a polyimide passivated device; the aluminum metal pad is continuous underneath the polyimide passivation. When the EDX scanner is moved away from the aluminum pad to an area with passivation, we still detect traces of Si, SiO_2, Al, and polyimide at the fractured interface cross-section. Therefore, from a device point of view, the actual source pad on top of the device is quite large; polyimide passivation is deposited on top of the large Al pad and then patterned to open the smaller pads for bonding. On the other hand, in a silicon nitride passivated device, the aluminum metallization is only at the contact pad opening area and it does not continue under the Si_3N_4 layer. Figure 3.1.15 illustrates a Si-Si_3N_4 interface (area away from the contact pad); Al layer is not present under the passivation layer, which is also verified by the EDX scan plot where no peaks for Al is observed.

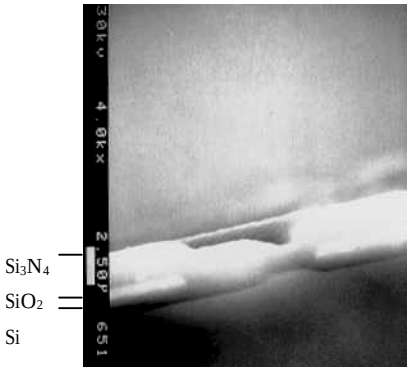


Figure 3.4.15. Si-Si_3N_4 interface of a IXGD40N60A device

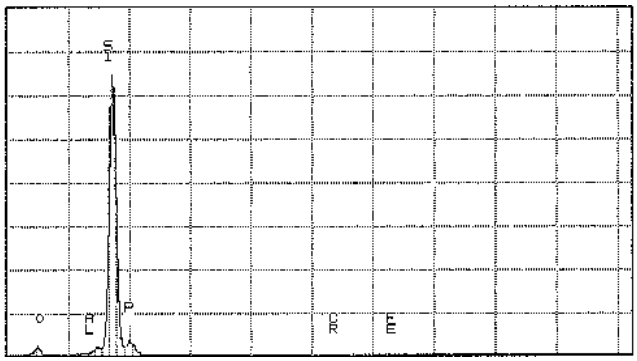


Figure 3.4.16. EDX scan at the Si-Si_3N_4 interface

3.4.1.3 Results of the Metallized Devices

Calibration Samples: Before we investigated the metallized devices, we inspected sputtered layers on calibration samples. The following Figures 3.4.17 and 3.4.18 show SEM and EDX scanning for Ti-Ni-Cu and Ag sputtered films on a Si sample respectively. The film thickness and deposition times are recorded for proper calibration of the sputter deposition. In this case, the sputtering duration for Ti, Ni, Cu and Ag were 45 min, 45 min, 90 min and 20 min respectively. Figure shows the layer mappings, from which we measure the following film thicknesses: Ti~0.8µm, Ni~1µm, Cu~2µm, and Ag~1µm.

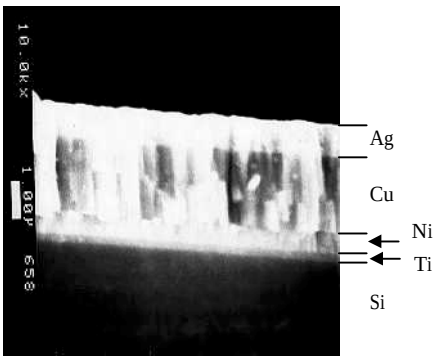


Figure 3.4.17. Ti-Ni-Cu-Ag sputtered films on Si

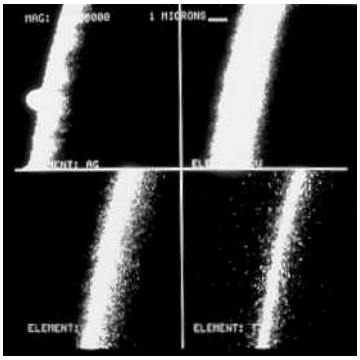


Figure 3.4.18. EDX scan for determining layer thicknesses

SEM cross-section image of a copper sputtered and fractured alumina sample is presented below. On a 96% pure alumina substrate, copper was sputtered for 90 minutes. The image reveals the rough structure of the alumina surface; consequently, the sputtered copper layer also maps the roughness of the alumina surface. Using EDX, the Cu thickness is measured to be ~2μm, which is consistent with the previously sputtered samples.

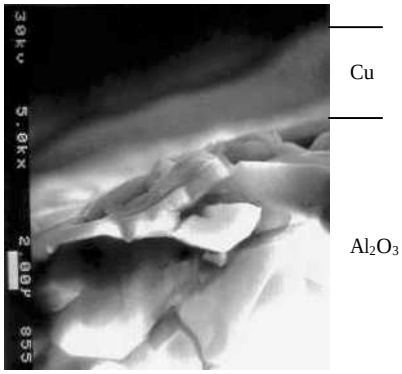


Figure 3.4.19. SEM cross-section of a Cu sputtered Al_2O_3 substrate

Electroless Plated Device: Next, a zincate processed, Ni-Au plated polyimide passivated device is fractured for SEM inspection. Figure 3.4.20 shows different layers of the underbump metallurgy. From the cross-section image, we notice that the traces of Zn are not very prominent. Moreover, compared to sputtered UBMs, the electroless plated UBMs are not distinguishable. Consequently, an EDX mapping of the layers (Al-Zn-Ni-Au) is performed, which is shown in Figure 3.4.21. Thin trace of Zn can be correlated to two facts; first, during the desmutting process, plated Zn layer is purposely thinned with a mild acid etch and secondly, during the Ni plating process, Ni ions replace the Zn ions from the Al surface. For an optimum plating process, very little or no trace of zinc is preferred on the aluminum surface. EDX image also reveals smudged traces of Zn and Al. Compared to sputtered devices where the aluminum layer on the device contact pad is intact, we notice a significant reduction of the Al layer after the entire plating process. The thinning of Al layer is due to the fact that, during the EN-PREP alkaline etching process of the native oxide removal, the aluminum layer may have been slightly etched. Ni layer is measured to be ~1.2μm thick, while the Au thickness is ~0.5μm.

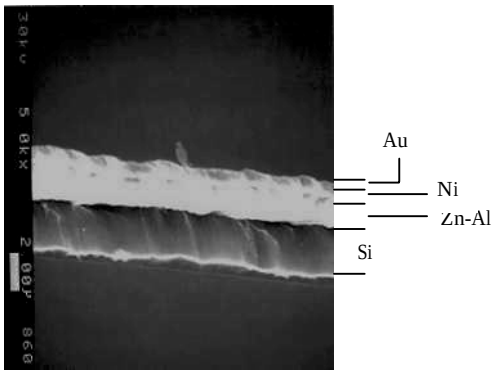


Figure 3.4.20. Zn-Ni-Au plated polyimide passivated

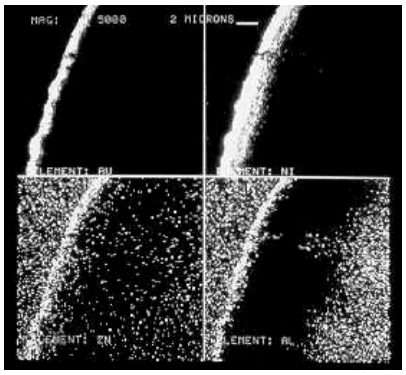


Figure 3.4.21. EDX mapping of Al-Zn-Ni-Au

Sputtered Device: A SEM cross-section image of a Cr-Cu sputtered polyimide passivated device is shown in Figure 3.4.22. Continuous layers of sputtered chromium and copper layers on an aluminum pad are shown. An EDX mapping for layer thicknesses for the same sample shows the continuous layers of Si, Al, Cr and Cu in Figure 3.4.23. Thickness measurements for the underbump metallurgy indicate a ~0.5µm thick chromium on top of the Al layer, while a ~1.5µm thick copper layer follows the chromium layer.

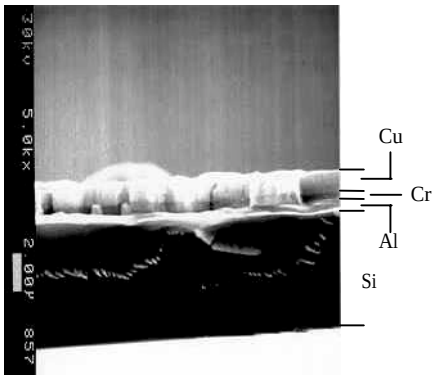


Figure 3.4.22. Sputtered Cr-Cu on polyimide passivated device

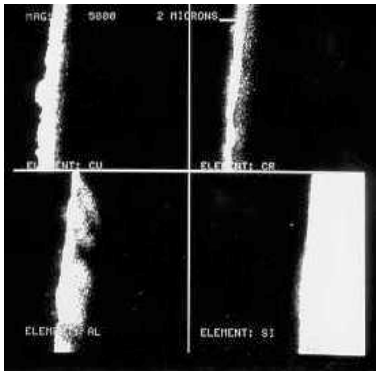


Figure 3.4.23. EDX mapping of Cr-Cu-Al-Si

Comparison between Electroless and Sputter Deposited Devices: We further examined the structure of UBMs to compare the quality of deposited films via the electroless process and the sputtering process. EDX mapping of UBM layers are shown below. Figure 3.4.24 shows electroless plated Zn-Ni layer on an IGBT while Figure 3.4.25 illustrates sputtered Ti-Ni-Cu films on two different IGBTs.

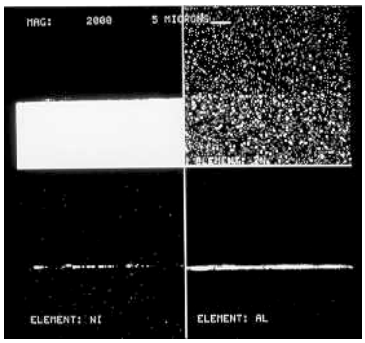
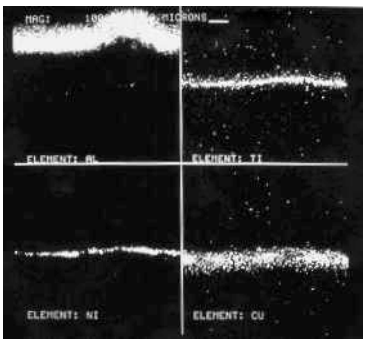


Figure 3.4.24. EDX mapping of plated Zn-Ni



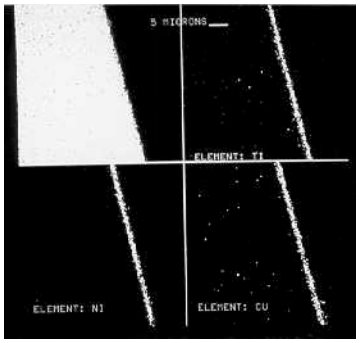


Figure 3.4.25. Sample EDX images of sputtered Ti-Ni-Cu on IGBTs

On the electroless plated device, we notice a very thin and discontinuous trace of Ni; furthermore, the Zn layer is also identifiable at a specific interface. On the other hand, as shown in Figure 3.4.25, the sputtered films of Ti, Ni and Cu are continuous and have solid traces and thicknesses. Consequently, considering the consistency of sputtered film samples, we can conclude that in selecting an UBM deposition process to make power devices solderable, the sputtering technique should be chosen over the electroless chemical deposition process.

From the above discussions, we can conclude that SEM investigations revealed significant processing issues with the electroless plating process. Sputtered layers were consistently identifiable, which proves the integrity of the sputtered metallizations; whereas the plated layers did not show continuous interfaces. SEM results also revealed the different qualities of interfaces between silicon nitride passivated and polyimide passivated devices before and after metallization scheme. However, SEM results do not identify the causes of weak adhesion as observed in the polyimide passivated devices. Consequently, we initiated a systematic XPS analysis for surface characterization of the bare devices.

3.4.2 XPS Characterization Results

XPS data provides elemental and chemical information from the outermost 40-80Å of a surface. XPS uses incident X-rays, typically A1K_α, to cause the photoemission of electrons from the material. The kinetic energy of the electrons emitted from the surface identifies the elements present on the surface. By measuring the exact binding energy and peak shape of a spectrum, the elemental and chemical composition of a surface can be determined. One other advantage of using XPS is that we can detect both organic and inorganic contaminants with this analytical tool.

In this research, XPS analyses are made to investigate the atomic composition of the aluminum bonding pads of the devices. XPS is based on the theory that when monoenergetic X-rays are incident on a surface, they interact with the surface atoms by the photoelectric effect and thereby, emit electrons from the surface. In the process, the energy of these emitted electrons is analyzed. Kinetic energy of the emitted electrons is expressed as follows:

$$\mathbf{K.E. = h\nu - B.E. - \phi_s}$$

Here, hν is the photon energy, B.E. is the binding energy of the emitted electron with the atomic orbital involved in the emission of an electron and ϕ_s spectrometer work function. A typical XPS spectrum shows a plot of number of electrons with respect to electron binding energies. Binding energies can be thought of as ionization energies of atoms for a particular shell. Emitted electrons have a variety of kinetic energies since there is a variety also in the shell types for atom's ionization.

All surface characterizations with XPS were performed at the surface chemistry lab at Virginia Tech with a Perkin-Elmer model 5400 XPS spectrometer, which operates with a 400W, 15kV Mg K_α X-ray source. Energy of the photoelectron is analyzed using a spherical capacitor operated at a constant value of pass energy of 17.9eV. Throughout the XPS analysis process, base pressure of the spectrometer is kept below $5x10^{-7}$ torr. XPS data are measured with a 45^o angle between the sample and the entrance to the analyzer. For all compositional analyses, C 1s, Al 2s, O 1s... are measured and the spectral binding energies are calibrated with respect to hydrocarbon peak (C 1s peak at 285eV). Percent concentration values are measured with the analyzed volume and sensitivity factors. Furthermore, all in-situ sputtering processes are performed with the XPS spectrometer operating with an emission current of 25mA, a beam voltage of 3kV and sputter rate of 5Å/min (as per ion gun setup control).

The depth of penetration for the XPS detector is 50Å, which will reveal sufficient information for surface oxides and contaminants. Bare dice of IXGD40N60A and IXSD35N120A are used for the XPS characterization. In both cases, the following scanning sequences are followed.

- First, we scanned the surface with a wide scan, which gives a quick glimpse of elemental information. Traces of the surface elements are identified using this scan. However, the wide scan does not indicate the volume percentage of each element.

- Based on the element information from the wide scan, we employed a multiplex scan on a few elements such as C1s, O1s, N1s, P2p, Al2p, F1s, and Si2p peaks. In a multiplex scan, the scan windows are narrowed to receive more intense peaks while the randomly generated noise peaks get cancelled out. Individual peaks for selected elements are acquired and their volume percentages are measured.

- An individual element peak should be Gaussian in an ideal case. However, in most cases, the detected elements on the surface form compounds, which causes a deviation from the ideal Gaussian shape of an element peak. Consequently, on a few elements of interest, we perform a curve fit function to identify these compounds, which are also verified with the XPS handbooks[25,26].

First, we scanned the surface of a Si_3N_4 passivated die. Figure 3.4.26 shows the wide scan on the Al pad of the device. As with any XPS scan, we see traces of carbon and oxygen, which are also present on the surface of the Al metallization. We notice traces of aluminum, fluorine and phosphor on the scan. Furthermore, this scan shows a few peaks of silicon, which may have come from the Si_3N_4 passivation surrounding the Al pad area. As a result, we employed an XPS scan outside the Al pad and on the Si_3N_4 passivation area, to isolate some of the elements in the previous scan of the Al pad.

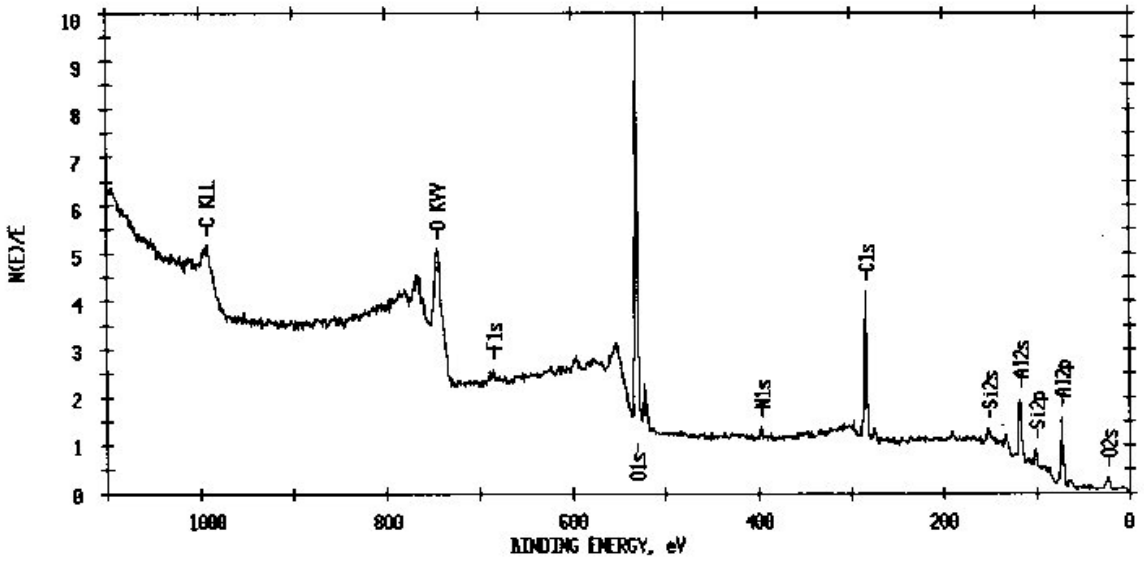


Figure 3.4.26. XPS wide-scan on the Al pad of an IXGD40N60A IGBT

Figure 3.4.27 shows an XPS wide-scan image of the Si_3N_4 area of an IXGD40N60A IGBT. Evidently, there are no traces of Al metallization in this case, which confirms the accuracy of the scanning window setup. We notice a huge peak of nitrogen and silicon, which are the binding elements of the Si_3N_4 passivation layer. Compared to the Al pad scan, fluorine contents are significantly smaller in the passivation area scan, which indicates that the fluorine contaminants are mostly confined near the device pad region.

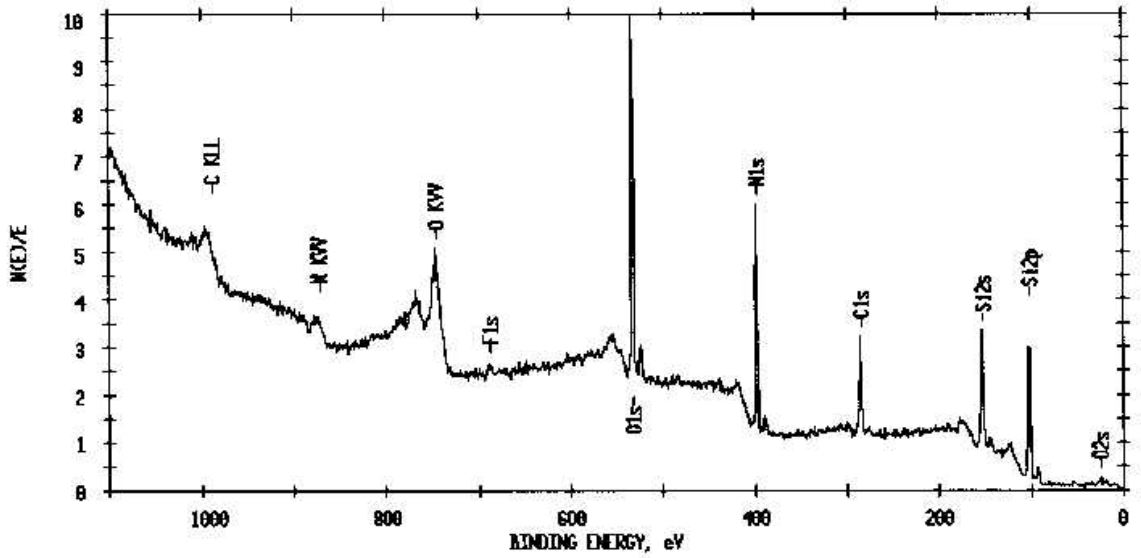


Figure 3.4.27. XPS wide-scan on the Si_3N_4 passivation of an IXGD40N60A IGBT

Next, we examined the contact pad surface of polyimide passivated IGBT. We narrowed down the window of the scan to fit the device contact pad area of the IGBT. Figure 3.4.28 shows the wide-scan of elements on one of the source pads of the device.

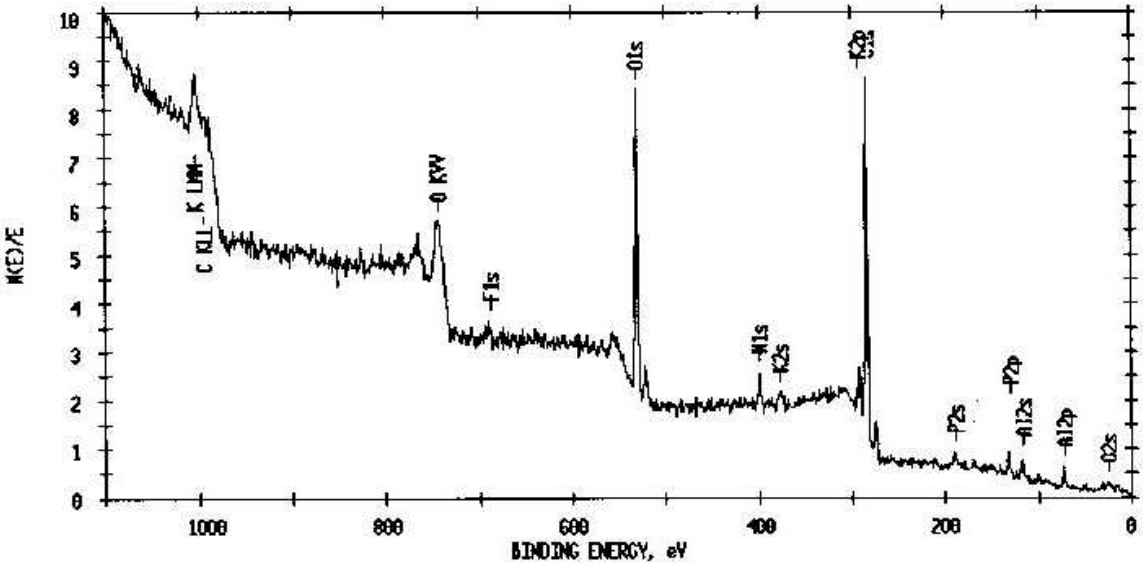


Figure 3.4.28. XPS wide-scan on the Al pad of an IXSD35N120A IGBT

Comparing the scanning results of the two IGBTs in Figures 3.4.27 and 3.4.28, we can clearly detect that in the case of a polyimide passivated device:

- carbon traces are significantly higher
- aluminum peaks are about three times smaller, and
- some traces of potassium and phosphorus are also evident.

Once again, we scanned the passivation area near the Al pad to distinguish the elements between the scanned areas. Figure 3.4.29 shows the wide-scan results on the polyimide passivated area of a polyimide passivated IGBT.

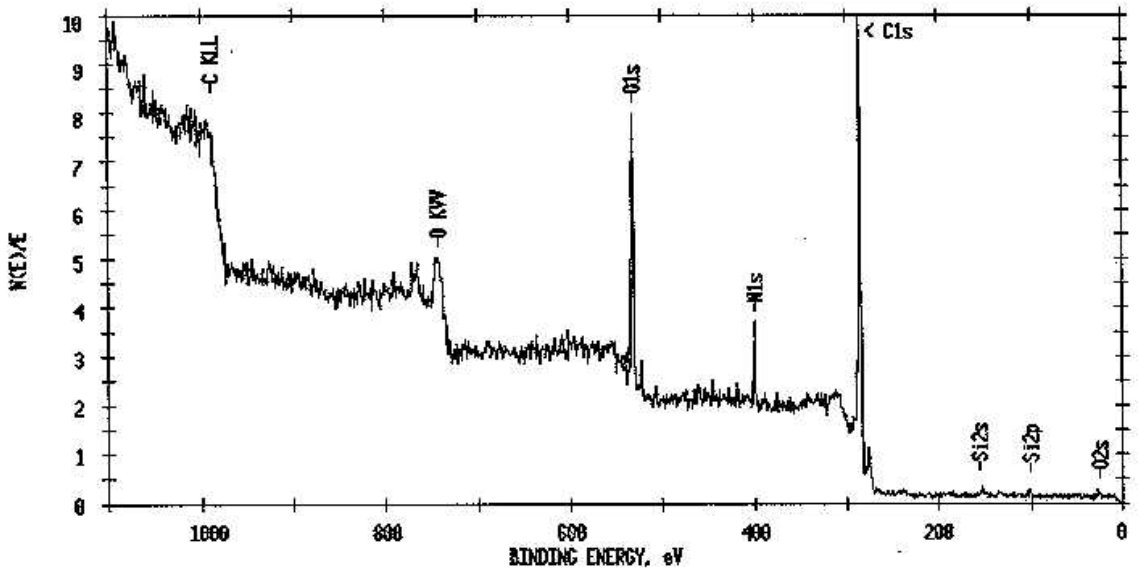


Figure 3.4.29. XPS wide-scan on the polyimide passivation of an IXSD35N120A IGBT

We verified the above scan on the polyimide with a standard XPS scan of polyimide in the handbook[26]. Aluminum, potassium and phosphorus traces are absent from the scan, which indicates the accuracy of the scan focus as well as the fact that potassium contaminant is only present in the device pad area. Carbon and nitrogen peaks are more pronounced in the polyimide passivation area compared to the Al pad region.

In the following table, volume percentages of elemental compositions for both types of devices are presented.

Table 3.4.1. Volume percentage of elemental compositions of IGBT surfaces

	Si_3N_4 passivated IXGD40N60A		**Polyimide passivated IXSD35N120A**	
Elements	Al pad area	Si_3N_4 area	Al pad area	Polyimide area
C1s	29.35	18.41	61.96	74.50
O1s	38.77	30.53	24.86	17.29
N1s	1.17	21.59	3.51	5.75
P2p	2.74	0.79	1.94	0.50
Al2p	22.46	0.08	4.22	0.00
F1s	1.11	0.08	0.25	0.68
Si2p	4.39	28.52	1.18	1.29
K2p	na	na	2.08	0.00

As we can see, the major differences between two IGBTS are the aluminum and carbon concentrations on the pad. As mentioned before, in the case of a polyimide-passivated device, the aluminum concentration is significantly lower (4.22%) and the carbon concentration (61.96%) is significantly higher than those of the silicon nitride passivated devices. At this point, we employed a curve-fitting function to the individual element peaks to identify the differences between the two IGBT surfaces.

Figures 3.4.30 and 3.4.31 show aluminum peaks for IXGD40N60A and IXSD35N120A contact pads respectively.

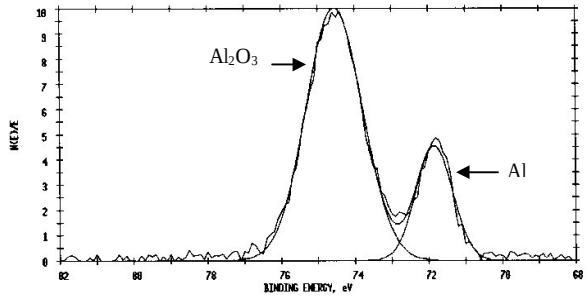


Figure 3.4.30. Multiplex scan on Al (IXGD40N60A)

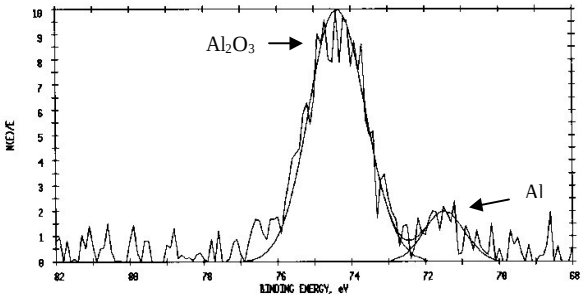


Figure 3.4.31. Multiplex scan on Al (IXSD35N120A)

The peaks of aluminum are very noisy in the polyimide passivated device, which indicates that the XPS detector has not reached enough depth to receive sufficient signals from the aluminum metal and the aluminum native oxide. However, in the silicon nitride passivated device, we notice smooth gaussian peaks of aluminum and its native oxide. As a result, we can conclude that the observed difference between the two IGBTs must reside in the surface of the aluminum contact pads. In a polyimide-passivated device, there must be an additional layer (on top of the Al and Al_2O_3 layer), which results in noisy peaks and significantly lower concentrations of aluminum.

Figures 3.4.32 and 3.4.33 show carbon peaks for IXGD40N60A and IXSD35N120A contact pads respectively. The peaks are not gaussian and consequently, they are curve-fitted to identify the different single bond and double bond compounds of carbon. We observe noisy peaks of carbon and its compounds on a silicon nitride passivated device compared to a polyimide passivated device. Compared to a polyimide passivated device, single bond carbon compounds are higher in concentration while double-bond carbon compounds are in lower concentration in a Si_3N_4 passivated device. The presence of the excess hydrocarbon elements on the Al pad of the IXSD35N120A device prevents the detector to reach Al layer, which may have contributed to the poor adhesion of the UBM system to the Al pad. However, in the UBM deposition technique via sputtering, we have used an argon plasma etching to remove Al surface oxide and contaminants before the actual sputtering of metal. As a result, it is crucial to find out how the Al surface changes with an argon plasma etching and whether the etching process results in different Al surfaces in two different IGBTs. If the Al contact pad surfaces are different for the two types of IGBTs under test, we will be able to probe into the probable causes of insufficient adhesion of UBM and the resulting high contact resistance values.

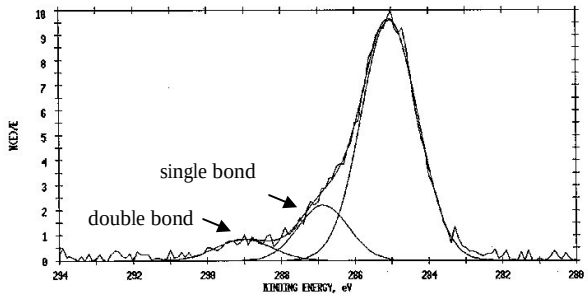


Figure 3.4.32. Multiplex scan on carbon (IXGD40N60A)

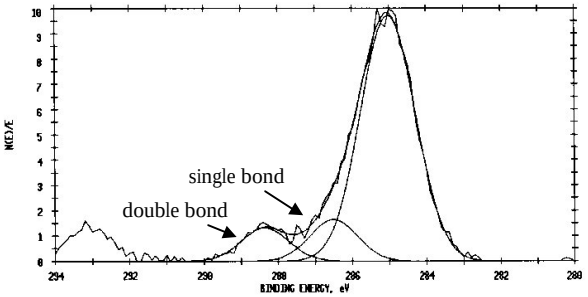


Figure 3.4.33. Multiplex scan on carbon (IXSD35N120A)

Accordingly, we employed an in-situ argon plasma etching to remove the first 50Å of the surface film and to detect the condition of the Al pad surface just before a sputter deposition process. Hence, a ten-minute argon plasma etching (at a rate of 5Å/min) is performed on the IGBT surfaces to remove 50Å from the surface. Figure 3.4.34 shows the XPS wide-scan results for a 50Å etched silicon nitride passivated IGBT. We notice a significant reduction of the carbon peak and a significant increase in the signals of Al peaks, when compared to the non-etched condition (Figure 3.4.26). Once again, peaks of nitrogen and silicon have appeared from the passivation composition of Si_3N_4 around the aluminum source pad.

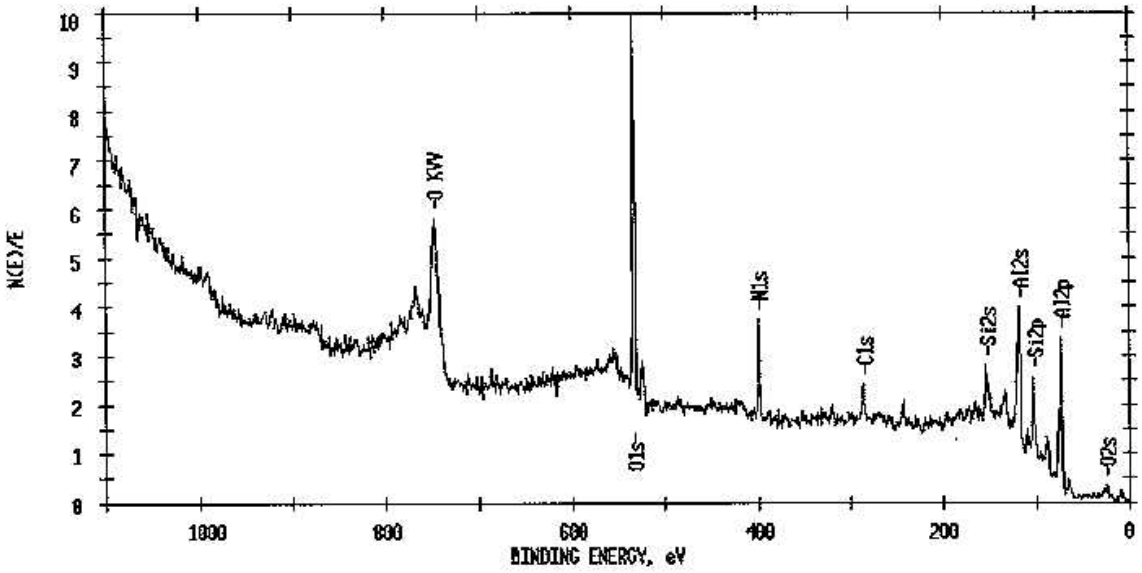


Figure 3.4.34. XPS wide-scan on a 50Å etched Al pad of an IXGD40N60A IGBT

Figure 3.4.35 shows the XPS wide scan results for a 50Å etched IXSD35N120A IGBT. We notice that the oxygen peak is somewhat reduced, however, the carbon peak is still very high compared to an IXGD40N60A device. Fluorine and aluminum signals have increased compared to the non-etched condition (Figure); however, the aluminum peaks are still not strong enough when compared to the Al peaks of an IXGD40N60A device for both etched and non-etched conditions.

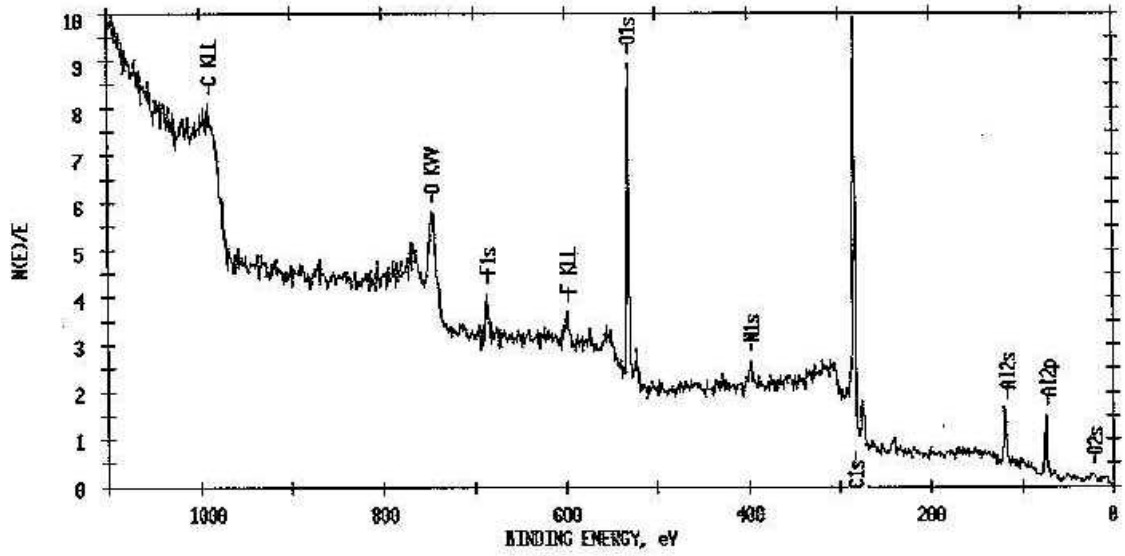


Figure 3.4.35. XPS wide-scan on a 50Å etched Al pad of an IXSD35N120A IGBT

At this point, we employed a multiplex scan for both device surfaces to gather data on elemental volume percentage. In the following table, volume percentages of elemental compositions for both types of etched devices are presented along with the data from the non-etched scans.

Table 3.4.2. Volume percentage of elemental compositions of non-etched and 50Å etched IGBT surfaces

Elements	**Si_3N_4 passivated IXGD40N60A**		**Polyimide passivated IXSD35N120A**	
(vol %)	Before etching	After 50Å etching	Before etching	After 50Å etching
C1s	**29.35**	**7.99**	**61.96**	**57.24**
O1s	38.77	29.08	24.86	22.04
N1s	1.17	11.00	3.51	1.59
P2p	2.74	4.57	1.94	0.00
Al2p	**22.46**	**32.57**	**4.22**	**15.05**
F1s	**1.11**	**0.91**	**0.25**	**4.03**
Si2p	4.39	13.83	1.18	0.00
K2p	na	0.00	2.08	0.00

We observe the most significant differences between the two IGBTs in the case of carbon, aluminum and fluorine concentrations. With a 50Å etch, carbon concentration on the aluminum contact pad of an IXGD40N60A has lowered to a very minimal 7.99%, while the carbon concentration on the IXSD35N120A device is at 57.24%. With an etch, the aluminum concentration has increased from 4.22% to 15.05% in the polyimide passivated device; however, even with the etch, the Al concentration is still not comparable to the case of silicon nitride passivated device. Comparing Figures, we can clearly notice that the Al peaks are more pronounced in the Si_3N_4 passivated devices than those of the polyimide-passivated device. Evidently, in the case of IXSD35N120A IGBTs, there is a thin layer of hydrocarbon elements with a finite thickness of at least 50Å on top of the Al and its native oxide layer. As a whole, presence of this hydrocarbon contamination layer has caused a significant detection of carbon compounds, an insufficient removal of the Al-oxide, as well as a detected weak peak of Al -- all of which may have lead to a poor adherent interface between the Al and the Ti layer of the UBM system. Also noticeable is the fluorine concentration in the case of etched devices. However, on a positive side, plasma etching has reduced contaminants such as potassium and phosphorus in the case of polyimide passivated device.

Comparing the individual peaks of aluminum for the both devices with a 50Å etch in Figures 3.4.36 and 3.4.37, we observe that the Al peak has significantly increased in the case of IXGD40N60A device as a result of the native oxide etch and a subsequent reduction of the Al_2O_3 concentration. However, we notice a completely different picture in the case of the polyimide passivated devices, where the Al_2O_3 peak is still higher than the Al metal peak. Moreover, the peaks of aluminum are very noisy in the polyimide passivated device even after the 50Å etch, which indicates that the XPS detector has not reached enough depth to receive sufficient signals from the aluminum metal and the aluminum native oxide. This clearly indicates that the observed difference between the two IGBTs does indeed reside on the surface of the aluminum contact pads. The additional layer (on top of the Al and Al_2O_3 layer) on top of a polyimide-passivated device results in noisy peaks and significantly lower concentrations of aluminum.

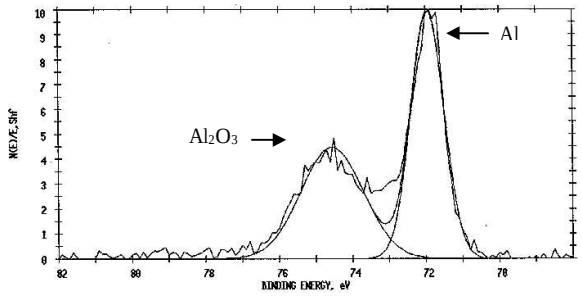


Figure 3.4.36. Narrow scan on 50Å Al-IXGD40N60A

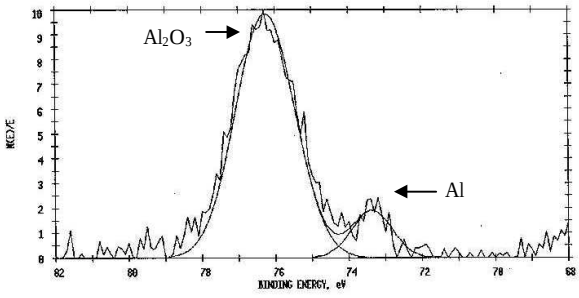


Figure 3.4.37. Narrow scan on 50Å etched Al-IXSD35N120A

The following table compares the concentration of the Al compounds before and after the argon plasma etching for both types of devices.

Table 3.4.3. Volume percentage of aluminum compositions of non-etched and 50Å etched IGBT surfaces

Elements	Si_3N_4 passivated IXGD40N60A		Polyimide passivated IXSD35N120A	
(vol %)	Before etching	After 50Å etching	Before etching	After 50Å etching
Al	22.76	54.06	12.76	19.49
Al_2O_3	77.24	45.94	87.24	80.51

Figures 3.4.38 and 3.4.39 show carbon multiplex scans for the etched devices respectively. Once again, the peaks are not gaussian and consequently, they are curve-fitted to identify the different single bond and double bond compounds of carbon. We observe noisy peaks of carbon and its compounds on an IXGD40N60A device compared to an IXSD35N120A device. With an argon plasma etch, single-bond carbon compounds have slightly increased in concentration in a Si_3N_4 passivated device, while the double-bond compounds are virtually eliminated from the Al surface. However, in the polyimide coated devices, double-bond compounds are still present.

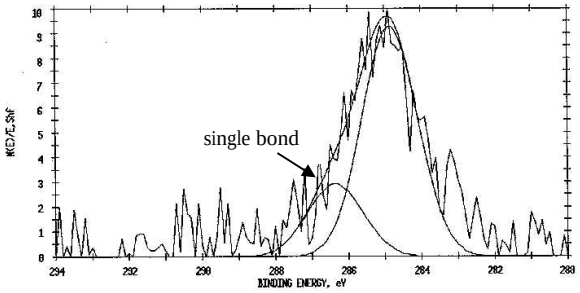


Figure 3.4.38. Narrow scan on 50Å C-IXGD40N60A

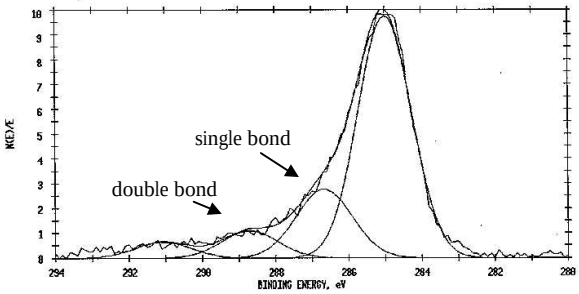


Figure 3.4.39. Narrow scan on 50Å etched C-IXSD35N120A

In the following table, carbon compounds of pure polyimide and the non-etched and the etched devices are presented. Compared to a polyimide passivated device, even after the plasma etching, single bond carbon compounds are higher in concentration in a Si_3N_4 passivated device, while the double-bond compounds are removed from the surface. However, we notice a strong presence of double-bond compounds in the polyimide passivated devices. In IXSD35N120A devices, hydrocarbon contaminants, specifically the double-bond compounds may have re-deposited on the Al contact pad from the surrounding polyimide passivation layer, which also gets etched during the argon plasma cleaning. On the other hand, in IXGD40N60A devices, carbon compound concentrations are significantly lower after the plasma etch since there is no possibility of carbon re-deposition from the Si_3N_4 passivation layer.

Table 3.4.4. Volume percentage of carbon compositions of pure polyimide, non-etched and 50Å etched Al surfaces

Elements	Si_3N_4 passivated IXGD40N60A		Polyimide passivated IXSD35N120A		Pure Polyimide
(vol %)	Before etching	After 50Å etching	Before etching	After 50Å etching	Before Etching
Pure carbon	77.39	76.06	79.19	72.23	78.37
Single-bond	15.82	23.94	11.54	19.30	7.97
Double-bond	6.80	na	9.27	8.47	13.66

In the pure polyimide layer on top of the device, we also notice a significant volume content of the double-bond compound (as shown in Figure 3.4.40), which is higher than the volume content of the single-bond carbon compounds. Moreover, we observe a similar distribution of carbon compounds between pure polyimide and etched IXSD35N120A devices, which leads us to isolate the polyimide passivation as the source of double-bond compounds as seen on the etched devices.

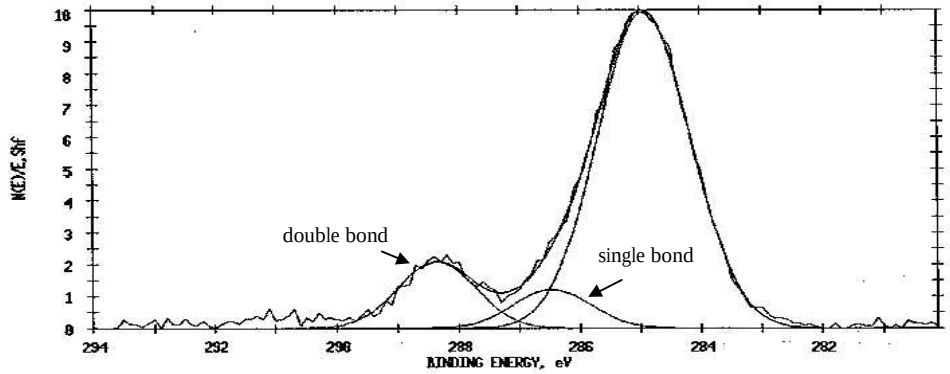


Figure 3.4.40. Multiplex scan on carbon of the polyimide passivation (IXSD35N120A)

The double-bond carbon compounds are extremely hydrophobic in nature (as in the case of IXSD35N120A devices), which resists adhesion of any subsequent layer on top[29]. On the other hand, single-bond carbon compounds leave the surface hydrophilic (as in the case of IXGD40N60A devices), which promotes subsequent adhesion of deposited layer. As a result, deposited UBMs have exhibited strong adhesion on a Si_3N_4 passivated device, resulting in low contact resistance, while the UBMs on polyimide passivated devices have weak adhesion to Al, resulting in high contact resistance and eventual thermal and electrical failure of the device.

In order to further investigate the source of carbon contaminants on the Al pads and estimate the thickness of the contamination layer, we scanned for carbon compositions on the IXSD35N120A devices with 100Å etching. Figure 3.4.41 shows the wide-scan results on the Al pad of an IXSD35N120A device.

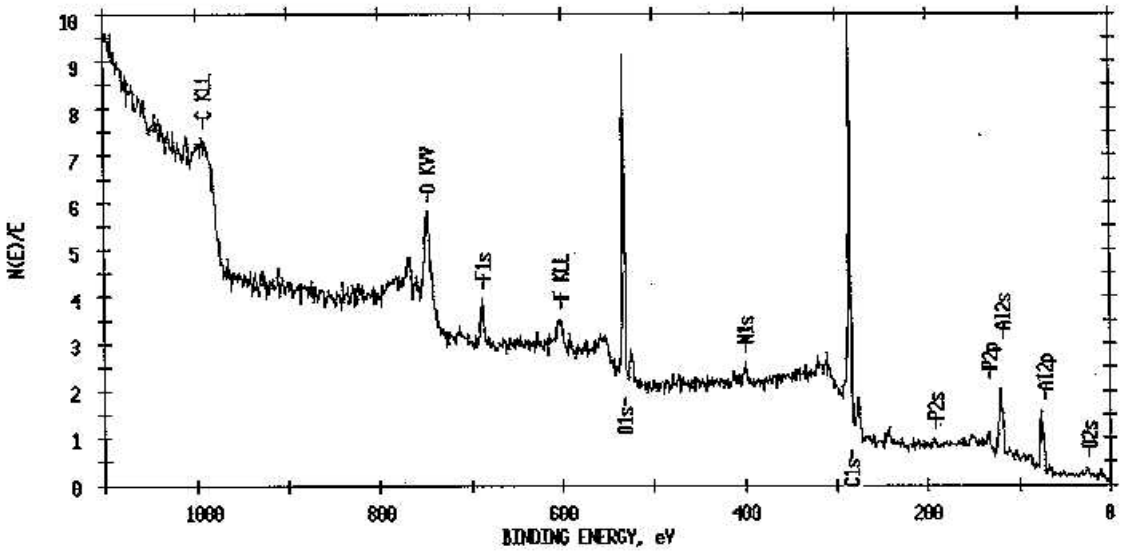


Figure 3.4.41. XPS wide-scan on the Al pad of a 100Å etched IXSD35N120A IGBT

With a 100Å etch, we expect to see further decrease in oxygen and carbon concentration with a significant increase in the Al concentration. However, similar to the 50Å etch case, we observe a significant carbon concentration as well as traces of fluorine with the 100Å etch. Al peaks do not show any significant improvement either. These observations are verified with the multiplex scan results of volumetric compositions, which are listed in the table below. The reduction in oxygen concentration is due to the oxide etch during the argon plasma cleaning. Moreover, a combination of high carbon concentration and a low

aluminum concentration suggests that the hydrocarbon contaminants are still on the surface of the device contact pad, even after a 100Å etch.

Table 3.4.5. Volume percentage of elemental compositions of 100Å etched IGBT surfaces

Elements	**Polyimide passivated IXSD35N120A**		
(vol %)	*Before etching*	*After 50Å etching*	*After 100Å etching*
C1s	61.96	57.24	64.10
O1s	24.86	22.04	16.82
N1s	3.51	1.59	1.63
P2p	1.94	0.00	0.89
Al2p	4.22	15.05	13.32
F1s	0.25	4.03	3.03
Si2p	1.18	0.00	0.00
K2p	2.08	0.00	0.00

Figure 3.4.42 shows the aluminum compositions, where finally an observable Al peak is seen. The argon plasma has etched the native oxide, resulting in an increase in the Al peak without an increase in the total Al metal concentration in the surface film as shown in the table above. However, within the detected Al compounds, metal concentrations have increased while oxide concentrations have decreased, as seen from Table 3.4.6. In any case, the oxide etching is not sufficient enough, when compared to the 50Å etched IXGD40N60A devices. On the other hand, in the case of carbon compounds (as shown in Figure 3.4.43), there is no significant change in concentration for pure carbon as well as its compounds. Consequently, we can conclude that any further etching would not allow us to reduce the carbon concentrations since the Al pad surface is being replenished with carbon contaminants from the nearby polyimide passivation.

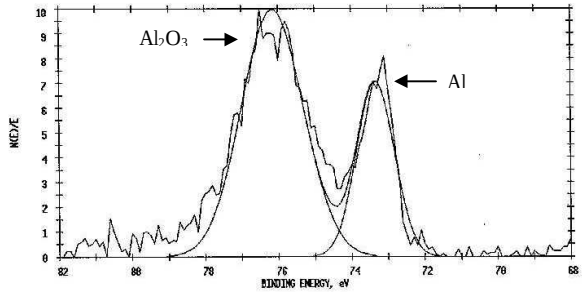


Figure 3.4.42. Al scan with 100Å etched pad (IXSD35N120A)

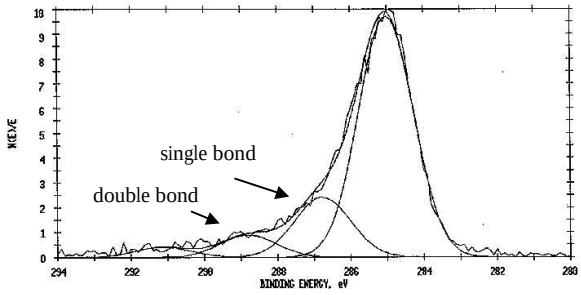


Figure 3.4.43. Carbon scan with 100Å etched pad (IXSD35N120A)

Table 3.4.6. Volume % of aluminum and carbon compositions of pure polyimide, non-etched, 50Å etched, and 100Å etched Al surface

Elements	**Polyimide passivated IXSD35N120A**		
(vol %)	Before etching	After 50Å etching	After 100Å etching
Al	12.76	19.49	30.23
Al_2O_3	87.24	80.51	69.77
Pure carbon	79.19	72.23	71.93
Single-bond	11.54	19.30	18.21
Double-bond	9.27	8.47	6.74

One significant observation during the XPS analysis should be noted here. While scanning after an etching process, we noticed that the carbon peak had shifted to the right (i.e. to a lower binding energy). For example, the carbon peak has moved to 283eV, which is later forced back to the carbon peak reference of 285eV in order to maintain the same reference point for the subsequent peaks of Al, O and other detected elements. This curve-shifting phenomenon indicates that the surface of the Al pad has become more

conductive as a result of plasma etching, thus charging less during the detection of elements and appearing at a lower binding energy in the XPS scan. This is perhaps due to the deposition of conductive carbon contaminants (such as double-bond carbon compounds or graphite) during the plasma etching. In every case of plasma etching on the contact pads of the IXSD35N120A devices, we have detected a strong presence of double-bond carbon compounds. However, in the case of Si_3N_4 passivated devices, we do not observe the curve-shifting phenomenon, rather, we notice that the double bond carbon compounds are removed.

We can summarize the findings of the XPS scanning results as follows:

- IXSD35N120A devices contain a thin layer (at least 50Å thick) of contaminants on top of the Al pad. The contaminants are mostly organic hydrocarbons, while a few inorganic contaminants such as potassium and phosphorus are also evident.
- With an argon plasma etch, we detected traces of fluorine in both IGBT contact pad surface, which are remnants of the passivation etching process via a mixed O_2-CF_4 gas, which is described later in the section 3.5.
- In the case of polyimide passivated devices (IXSD35N120A IGBTs), a 50Å argon plasma etch is sufficient to remove the inorganic contaminants such as potassium and phosphorus. Moreover, with an argon plasma etching, we were able to etch the native Al oxide; however, polyimide particles from the passivation layer get re-deposited on the surface of the pad. Even with a 100Å etch, the hydrocarbon deposits (specifically the double bond carbon compounds) from the passivation layer keeps the Al contact pad sufficiently hydrophobic. As a result, the graphite-like contaminants leave the surface of the Al pad resistant to subsequent adhesion of any thinfilm deposition.
- With a 50Å argon plasma etch, carbon compositions are significantly reduced on the contact pads of the IXGD40N60A devices. Aluminum oxide also gets etched substantially with the argon plasma etching. Hydrocarbon compounds are totally removed in the argon plasma etching process. Consequently, the Al surface is contaminant free, which allows excellent adhesion of subsequent thinfilm deposition.

3.5 DISCUSSION

In this section, we analyze the observations of the SEM and XPS interface characterizations. We concluded that the difference of passivation coating of the two different IGBTs and more importantly, these passivation layers' surface conditions during the plasma cleaning process, have resulted in significantly different electrical characteristics of the packaged devices. Therefore, first, we will explore the inherent differences of silicon nitride and polyimide passivation as used in the device fabrication. Then we will correlate the observations with the processing in which the problems incurred.

3.5.1 Passivation Layer of the IGBTs

Similar to the intermetallic dielectric, the top or passivation layer of an IC is also a dielectric material, which serves as a protective coating[27]. This coating is masked and etched by photolithographic processes to create the openings through which the exposed metal can be attached to the chip package. The passivation layer protects the chip against mechanical damage, as well as against moisture and ionic contaminants, which can gain access to the circuit metallization through pad openings or defect sites, leading to corrosion of internal metallizations[28,29,30]. In the device fabrication industry, a variety of inorganic thin films such as SiO_2, quartz, and Si_3N_4 are commonly used as passivation overcoats.

Inorganic dielectric materials, which are deposited conformally often have a few inherent problems. The sources are these problems include both deposition and photolithography scheme. Inorganic dielectrics can be deposited only to a thickness of 1 to 3 micron. These films tend to reproduce the topography of the underlying substrate since these dielectric lacks planarizing properties. Typical problems include poor step coverage and thinning of the coating over the sharp surface structures. Moreover, thicker inorganic films

often tend to crack while poor step coverage leads to poor line width resolution and long-term reliability problems associated with the cracks and discontinuities in the metallization and dielectric layers[31].

As a result, the ability to planarize topographical features has become one of the most crucial criteria in selecting an intermetallic dielectric. In the last few decades, organic polymers have been used as a permanent, embedded dielectric layer within the IC structure because of the superior planarity characteristics over the inorganic dielectrics. However, the organic materials must meet the same requirements as imposed on the inorganic materials. Moreover, the organic materials must maintain[32]:

- minimal outgassing of residual solvent and moisture,
- stability up to 400^{o}C for subsequent sintering process of metals, and
- higher T_g than the packaging steps (such as soldering) to prevent structural deformation.

Based on the desired properties of the intermetallic dielectrics, polyimides have gained popularity as an organic dielectric. Polyimides have been used in the electronic industry for quite some time as polymer insulation because of their excellent electrical and mechanical properties at elevated temperatures. DuPont marketed one of the first commercially available resins for electrical insulation in the early 60's. Since 1970, the semiconductor industry started an evaluation of polyimide as a spin-coated thinfilm dielectric, which has generated an entire line of semiconductor grade polyimide materials with varied viscosity, percent solids and chemical structures for a wide range of applications. In the following table, material properties of a few intermetallic dielectrics (inorganic and organic such as PIQ polyimide marketed by Hitachi), that are typically used in IC manufacturing, are presented. As can be seen, the dielectric constant of the polyimide is comparable to SiO_2 but significantly lower than Si_3N_4. The dielectric breakdown strength and volume resistivity also closely resemble those of SiO_2 and other inorganic dielectrics. Even though the polyimides are not as thermally stable as the inorganic materials, it is sufficient to allow them to be used for device passivation. However, the less desirable features of polyimides are the high CTE and low thermal conductivity. Regardless of the high CTE and low k, polyimides have exhibited lower residual stresses than the inorganic dielectrics[33]. Good mechanical strength of the polyimide is indicated by a high Young's modulus, elongation at break, and high tensile strength. However, the single most important feature of polyimide is its ability to planarize underlying topography, while the second most important feature is its thermal stability up to ~400^{o}C. Despite the advantages of using polyimide as a protective coating, one biggest disadvantage of polyimide includes its instability and surface modification in a plasma environment, which does not occur in the case of Si_3N_4 passivation.

Table 3.5.1. Properties of PIQ Polyimide and a some inorganic materials[34]

Material	CTE	Young's Modulus	Tensile Strength	Thermal Conductivity	Melting Point	Dielectric Constant	Dielectric Breakdown	Volume Resistivity
	x10^{6} (^{o}C^{-2})	x 10^{4} (gf cm^{-2})	x10^{6} (gf cm^{-2})	(mcal cm^{-1}s^{-1}^{o}C^{-1})	(^{o}C)		(V-cm^{-1})	(ohm-cm)
PIQ Polyimide	20-70	300	1.7	0.4	450-500	3.5-3,8	10^{6}	10^{16}
Si	2.3	1.6	120	72-340	1420	11.7-12	10^{5}	
SiO_2	0.3-0.5	0.7	1.4	5	1710	3.5-4.0	10^{6}-10^{7}	10^{16}
Si_3N_4	2.5-3	1.6	6.4	28	1900	7-10	10^{6}-10^{7}	10^{12}
Al_2O_3	9	3.7	28	78	2050	7-9	10^{5}	10^{14}
Al	25	70	0.7-1.4	570	660	-	-	2.5x10^{-6}

In this research, we have used both types of passivation (inorganic and organic) on top of the IGBTs; IXGD40N60A devices have a Si_3N_4 passivation, while the IXSD35N120A devices have a PIX1400 brand polyimide[35]. In both cases, the thickness of the passivation layer is about 3μm. Polyimide is deposited via spin coating and then lightly cured and patterned with photoresist and then plasma etched in pad areas. Finally, the coating is cured at 400^{o}C for four hours.

3.5.2 Traces of Fluorine

During our XPS characterization of the surfaces on the as-received devices from IXYS, we detected traces of fluorine, which indicates that these contaminants may have originated at one of the steps in the device fabrication process. Moreover, fluorine contaminants increased on the pad surface, as they were plasma cleaned. In the following paragraph, we try to identify the process, which may have contributed the observed fluorine contamination.

In the IC manufacturing industry, polyimide etching by plasma is more preferred due to its resulting superior resolution and uniformity. Oxygen and oxygen mixed with small amount of fluorine containing gases such as CF_4 and SF_6 are used in plasma etching of polyimides[36,37]. The etch rate of the plasma is dependent on a variety of parameters such as plasma reactor type, power, pressure, temperature, time and gas composition. Polyimides and photoresists etch at different rates depending on their chemical compositions. However, assuming a one-to-one etch ratio of resist to polyimide, resist material is deposited with a thickness of twice that of the polyimide.

During the plasma treatment process, fluorine migrates from the plasma to the surface of the polymer where it extracts a hydrogen, leaving behind a radical, which may be attacked by the species in the near vicinity. Oxygen can also extract a hydrogen, however, it is less effective than the fluorine. Etchant attachment to the radical leaves the site either fluorinated or oxygenated as shown in Figure 3.5.1[38]. Oxygenation of the site makes it susceptible to degradation, while fluorination of the site leaves it passive to further etching processes. As a result, introducing fluorine onto the surface increases the etch rate via enhanced radical generation while excessive amount of fluorine inhibit etching by competing against oxygen for radical sites.

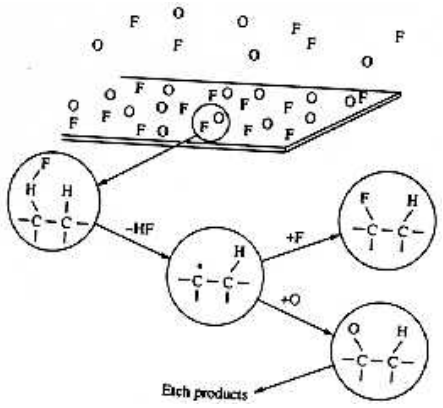


Figure 3.5.1. Reactions at the polymer surface during an oxygen-CF_4 plasma[38]

Oxygen plasma etching degrades the polyimide both by oxidative attack and UV degradation. In plasmas where oxygen and CF_4 gases are mixed, XPS has shown that polyimides first incorporate fluorine into the polymer matrix as a mixture of CF_x-type compounds and then undergo enhanced oxidation degradation[39]. Moreover, the presence of fluorine atoms inhibits plasma etching[40]. Consequently, we can conclude that at the polyimide etching process at IXYS, perhaps all the fluorine contaminants were not removed effectively and the residual contaminants resurfaced during the plasma cleaning since the plasma removed the surface films and exposed the buries fluorine contaminants.

3.5.3 Effects of Plasma on the Polyimide Passivation Layer

In most deposition schemes, surface preparation is extremely crucial. For metal surfaces, plasma cleaning will remove the surface contaminants leaving the surface cleaned down to the base material. In the case of metal surfaces, a thorough cleaning is achievable since metals are mostly quite resistant to the plasma. However, in the case of polymers, plasma environment directly attacks the polymer and alters the chemistry and

topography of the surface as well as the base polymer. For example, in the production of high-strength composites, surfaces of the fiber and plastic parts need to be stripped off. Gas plasma scrubs down the surfaces of the contaminants by a combination of sputtering and UV photolysis of covalent bonds of the contaminants' surface structure[41]. The contaminants degrade into volatile compounds quicker than the base polymer structure. In most cases, a noble gas such as argon is used with a short treatment time since argon plasma tends to initiate cleavage without grafting to the surface.

In our metallization scheme, we have used argon to clean up the pads before sputtering. High energy from the activated atom physically sputter the material to break down carbon compound in the contaminant. With higher vapor pressure, these species would be evacuated from the chamber during processing, leaving a clean surface. XPS data and surface tension measurements have shown the effectiveness of using a plasma cleaning in reducing surface carbon levels on metal surfaces[42] (as we have seen in the case of IXGD40N60A Si_3N_4 passivated devices). However, the same plasma cleaning process has not been able to clean the pad surfaces in the polyimide passivated devices. Despite the use of an inert plasma, we have noticed a significance presence of hydrocarbon contaminants on the device pads. In the following paragraphs, we investigate the possible reasons for this polyimide contamination during plasma cleaning.

- With the plasma cleaning, along with the device metal pad, the polyimide passivation layer also gets etched. Although in a vacuum stream, the etched polyimide particles should be pumped away, a certain percentage of these contaminants may have re-deposited on the device pads immediately after the plasma process. Significant percentage of polyimide-type contaminants on the IXSD35N120A device pads after plasma etching provides sufficient evidence for the re-deposition of hydrocarbon contaminants.

- Plasma process involves surface modification via CASING (crosslinking via activated species of inert gases) and polymer deposition[43]. The ionized gas creates energetic species in gas plasma. Surfaces in contact with gas plasma react with these energetic species and their energy is transferred from the plasma to the solid. These energy transfers are dissipated within the solid by a variety of chemical and physical processes (such as bombardment, oxidation, grafting, cross-linking or polymerization of the gas) to form new compounds and modify the surface of the material. The unique surface modification is achieved to depths from several hundred angstroms to ten microns without changing the bulk properties of the surface. A variety of processing parameters such as gas types, treatment time and operating pressure can directly affect the chemical and physical characteristics of the plasma and subsequently affect the surface chemistry.

- For a proper plasma cleaning scheme, sufficient RF energy must be applied. Lower power densities remove contaminants at a slower rate and can in fact, impede the removal process. During a plasma process, while the top layers of organic contaminants are being removed, underlying layers may crosslink in three dimensions, creating a stable but unremoved new structure:

  $$-CH_2\text{-}CH\text{-}CH_2\text{-}CH_2 \rightarrow CH_2\text{-}CH\text{-}CH_2\text{-}CH_2\text{-}CH_2\text{-}CH_2 \rightarrow -CH_2\text{-}CH_2$$

  Perhaps the plasma cleaning process needs to be optimized for polyimide passivated devices so that only the organic contaminants are removed without regeneration of hydrocarbon contaminants.

3.5.4 Effects of Alkaline Liquid on Polyimide

As mentioned in section 3.3, metallization for the electroless deposition scheme on the IXSD35N120A polyimide passivated devices did not yield promising results. After the plating process, the breakdown voltages of these devices lowered significantly, in some cases, the breakdown voltage dropped from 1200V to as low as 400V. On the plated IXSD35N120A devices, we noticed that the plating solutions had created small holes through the polyimide coating, thus degrading the device characteristics and making them unusable. During the developmental stage of a suitable wet-etching chemical for polyimide, researchers have found that even a cured polyimide can react with strong bases[44]. A few plating solutions in our electroless deposition scheme contain tetralkyl ammonium hydroxide, sodium hydroxide, and potassium hydroxide,

which can attack and remove unprotected polyimide areas. The damages to the passivation are mostly concentrated around the edges of the contact pads. In most cases, the etch rate may be as high as approximately five microns per second, which is too rapid to control. In the process of baking and curing of the polyimide, careful control of the temperature and time must be ensured to achieve the desired degree of imidization and etch rate[45]. Consequently, we can conclude that although the polyimide on the IXSD35N120A IGBT was cured for four hours at the final processing step, the required resistance to alkaline solution did not occur due to improper curing process of this specific type of polyimide.

3.5.5 Possible Solutions to Remove Hydrocarbon Contaminants

We identify a few possible solutions to mitigate the problem of hydrocarbon contamination on the contact pads of the polyimide-passivated devices. Future work will be required to verify these possibilities.

- One possible way to remove organic contaminants is to use oxygen plasma. When oxygen plasma is used, atomic oxygen in the gas plasma combines with carbon material in the organic contaminant to form water and carbon dioxide. These species would be evacuated from the chamber during processing, leaving a clean surface. In the following table, applications of oxygen and argon gas plasmas are listed[46].

Table 3.5.2. Applications of common gases used for plasma etching

Gas	Mixture	Application
O_2	100%	Removal of organic contaminants, stripping of photoresist, activation of polymers. Degreasing of metals and polymers, hydrophilation, oxidation
Ar	100%	Activation and degreasing of metals, hydrophilation, removing epoxy bleed out from hybrid circuits, oxide removal

  Consequently, oxygen plasma could be effectively used to remove organic contaminants. Oxygen plasma creates a chemical reaction and with surface contamination, resulting in their volatilization and removal from the chamber. When exposed to RF field, oxygen gets broken down into monatomic oxygen, O, O^+ and O^-. At pressure level above 0.1 torr, O is the most reactive element in the plasma and will readily combine with any organic hydrocarbon. The resultant combination is water vapor, CO and CO_2, which are carried away in the vacuum stream. This reaction removes organic contaminants, leaving no residual surface products; however, removal of non-organic salts are not so easily achieved in some cases.

  However, selection of the process parameters would be extremely crucial since plasma can modify the contamination instead of removing it. Critical parameters include sufficient power density to remove the contaminants rather than polymerizing them and addition of other gases to facilitate the prevention of polymerization. Moreover, oxygen plasma etching has been found to degrade the polyimide both by oxidative attack and UV degradation[46]. Therefore, process optimization must be ensured for a proper use of the oxygen plasma to remove contaminants. Furthermore, in oxygen plasma, improperly cured polyimide may get oxidized, thus reducing the breakdown voltage significantly, which may cause catastrophic failure of the device.

- Numerous studies have demonstrated that since polar groups are always incorporated onto polymer surfaces, even in the presence of an inert gas, wettability of the polymers are improved. The polymer radicals formed during the treatments are long-lived and can react with molecules in the air upon exposure after treatments. Therefore, even when an inert gas is used in the plasma treatment, introduction of a polar group such as oxygen can be incorporated into polymer surfaces[47,48]. Plasma activation involves altercation process of surface characteristics by the substitution or addition of new chemical groups from active species in the gas plasma. For example, hydroxyl and carboxylic acid groups can be grafted on to a polymer surface to make a hydrophobic surface hydrophilic. Specific profile for etching need to be developed for an application with a specific combination of gas, pressure, power and flow to achieve different etching objectives. However, the extent of improvement will depend on process gas, exposure time to the plasma, energy and power densities, and original composition of the surface specimen position, discharge power and frequency, treatment time, gas pressure and type[41,49,50].

3.6 SUMMARY AND CONCLUSIONS

With all the processing and characterization work on the device interconnection schemes, we can summarize our findings as follows.

- A primary concern with achieving adhesion is the presence of organic contamination on the surface. Contamination can reside in any of the following forms – residues, anti-oxidants, carbon residues and other organic compounds.
- Organic contaminants such as hydrocarbons remain in the form of thin monolayers on the surface, even in the case of as-received devices from the manufacturer. Absorbed monolayers of hydrophobic and hydrophilic surfaces consist of different chemical compositions and accordingly, the attraction forces of these absorbed layers are also different, which affects the bonding properties of the resulting surfaces.
- In the case of polyimide passivated devices, plasma etching may have introduced a few carbon constituents on the surface. Spectra shows clear evidence of possible carbon contaminants, such as carbide (~282.9eV) and graphite (~284.3eV) on the surface at binding energies below the binding energy of the hydrocarbon peak (C 1s at 285eV). Whereas above the hydrocarbon peak energy level, presence of carbon-nitrogen compounds, single bond carbon compounds (~285.9eV) and double bond carbon compounds (~288.5eV) are present. However, a majority of the carbon is associated with hydrocarbons, which are hydrophobic in nature, thus making the device contact pad less wettable.
- Plasma cleaning process may be modified with an elaborate optimization of the process parameters. However, alternative solutions to remove hydrocarbon contaminants do not look promising due to their possible interaction with polyimide.
- Fluorine contaminants were evident on the device contact pads. These contaminants were originated during the etching process of the polyimide to open contact pad areas. Clearly, at the fabrication step, these contaminants were not properly removed.
- Electroless deposition process is not suitable for metallizing polyimide passivated devices due to polyimide degradation with alkaline exposure. The curing of the polyimide passivation needs to provide sufficient chemical resistance, which is not achieved by the device manufacturer at the present time.

This work has enabled IXYS to replace polyimide passivation on the IXSD35N120A devices with silicon nitride. More importantly, the advantages of solderable contact and subsequent packaging possibilities have prompted them to fabricate IGBTs with solderable source and gate contacts.

3.7 REFERENCES

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