PROCESSING OF INTEGRATED CIRCUITS

- Overview of IC Processing (Part I)
- Silicon Processing
- Lithography
- Layer Processes Use in IC Fabrication (Part II)
- Integrating the Fabrication Steps
- IC Packaging (Part III)
- Yields in IC Processing

Integrated circuit (IC)

A collection of electronic devices such as transistors, diodes, and resistors that have been fabricated and electrically intraconnected onto a small flat chip of semiconductor material

- Silicon (Si) - most widely used semiconductor material for ICs, due to its combination of properties and low cost
- Less common semiconductor materials: germanium (Ge) and gallium arsenide (GaAs)
- Since circuits are fabricated into one solid piece of material, the term *solid state* electronics is used for these devices

Levels of Integration in Microelectronics

Integration level	Number devices	Approx. year
Small scale integration (SSI)	10 - 50	1959
Medium scale integration (MSI)	50 - 10^3	1960s
Large scale integration (LSI)	10^3 - 10^4	1970s
Very large scale integration (VLSI)	10^4 - 10^6	1980s
Ultra large scale integration (ULSI)	10^6 - 10^8	1990s
Giga scale integration	10^9 - 10^{10}	2000s

Overview of IC Technology

- An integrated circuit consists of hundreds, thousands, or millions of microscopic electronic devices that have been fabricated and electrically intraconnected on the surface of a silicon chip
- A *chip* is a square or rectangular flat plate that is about 0.5 mm (0.020 in) thick and typically 5 to 25 mm (0.2 to 1.0 in) on a side
- Each electronic device (e.g., transistor) on the chip surface consists of separate layers and regions with different electrical properties combined to perform the particular electronic function of the device

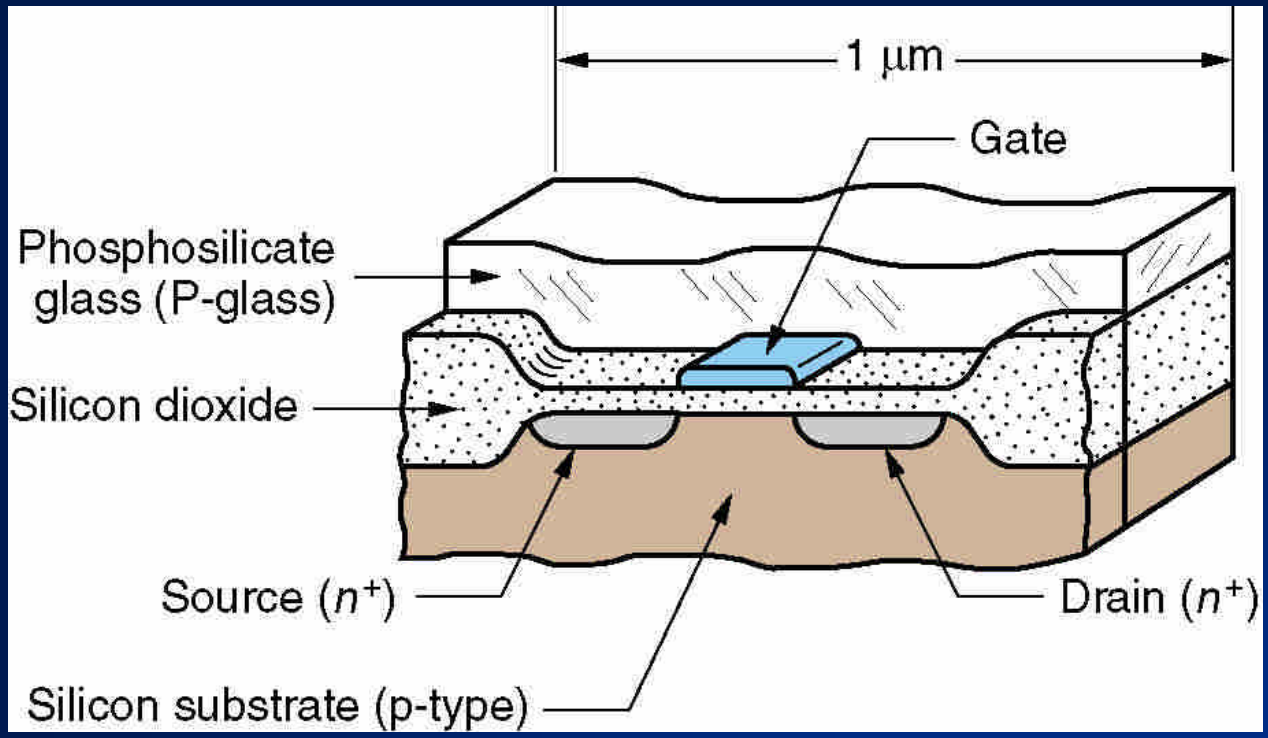

Figure 35.1 - Cross-section of a transistor (specifically, a MOSFET) in an integrated circuit. Approximate size of the device is shown; feature sizes within the device can be less than 1 μm with current technology.

Packaging of ICs

- To connect the IC to the outside world, and to protect it from damage, the chip is attached to a lead frame and encapsulated inside a suitable package
  - The package is an enclosure, usually made of plastic or ceramic, that provides mechanical and environmental protection for the chip
  - It includes leads by which the IC can be electrically connected to external circuits

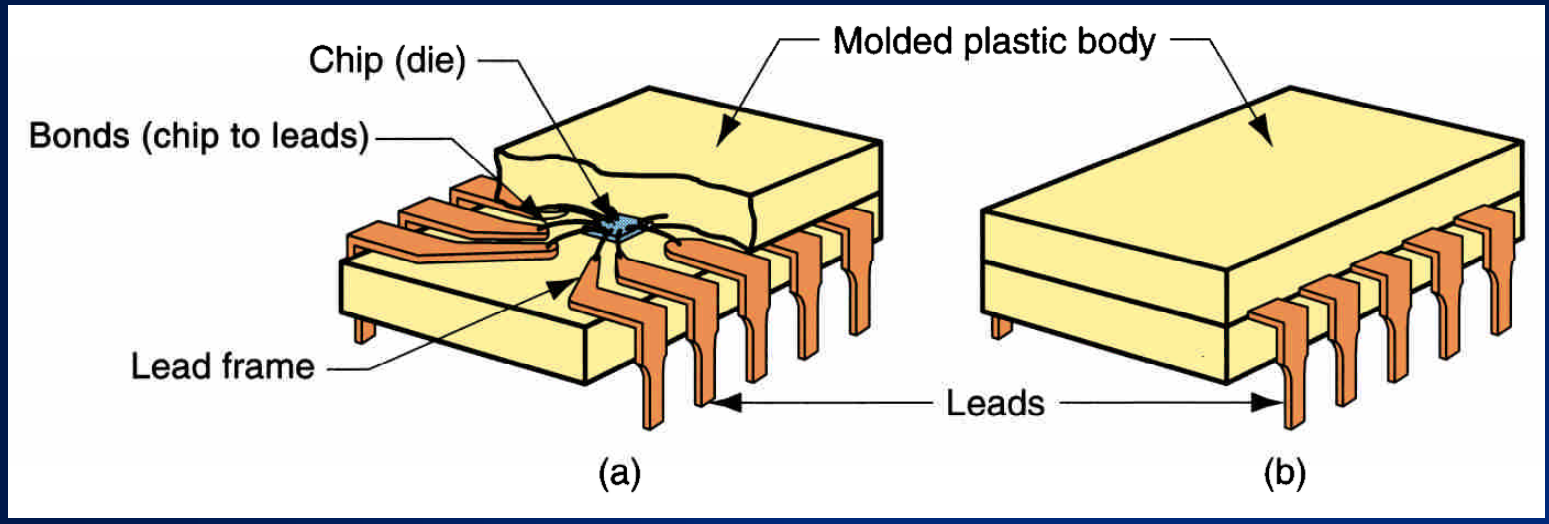

Figure 35.2 - Packaging of an integrated circuit chip: (a) cutaway view showing the chip attached to a lead frame and encapsulated in a plastic enclosure, and (b) the package as it would appear to a user. This type of package is called a dual in-line package (DIP).

Processing Sequence for Silicon-based ICs

- *Silicon processing* - sand is reduced to very pure silicon and then shaped into wafers
- *IC fabrication* - processing steps that add, alter, and remove thin layers in selected regions to form electronic devices
  - Lithography is used to define the regions to be processed on wafer surface
- *IC packaging* - wafer is tested, cut into individual chips, and the chips are encapsulated in an appropriate package

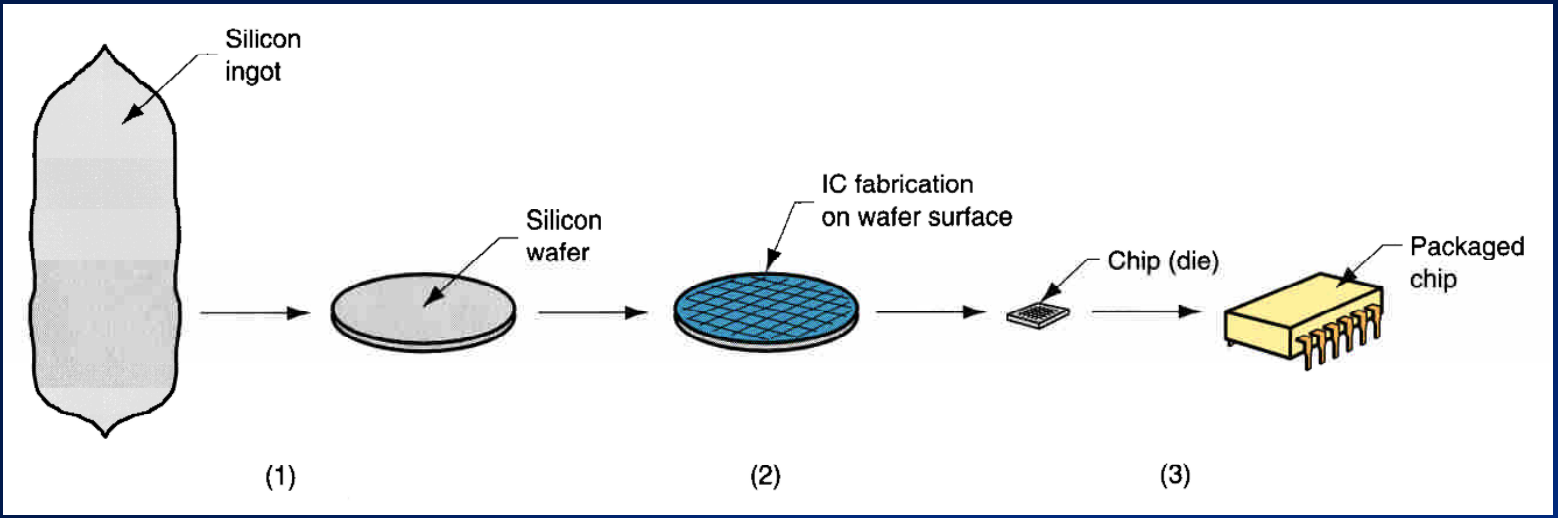

Figure 35.3 - Sequence of processing steps in the production of integrated circuits: (1) pure silicon is formed from the molten state into an ingot and then sliced into wafers; (2) fabrication of integrated circuits on the wafer surface; and (3) wafer is cut into chips and packaged

Clean Rooms

- Much of the processing of ICs must be carried out in a clean room, the ambiance of which is more like a hospital operating room than a production factory
- Cleanliness is dictated by the microscopic feature sizes in an IC, the scale of which continues to decrease with each passing year

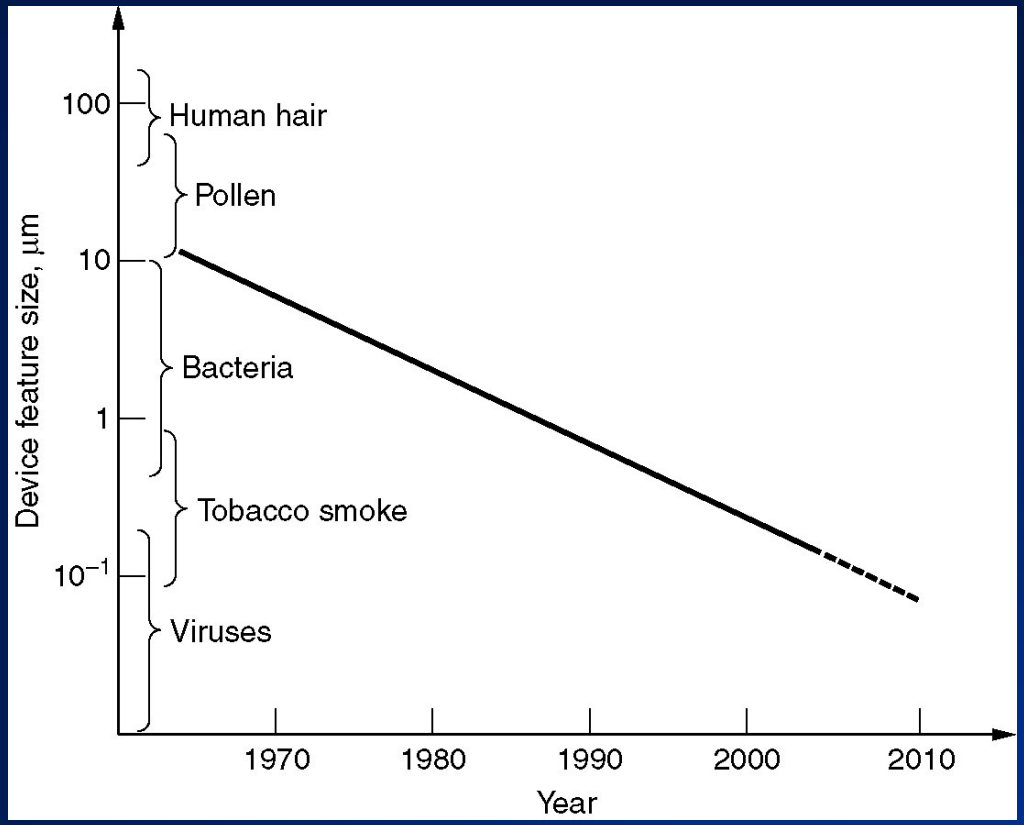

Figure 35.4 - Trend in device feature size in IC fabrication; also shown is the size of common airborne particles that can contaminate the processing environment

Clean Room Classification System

A number (in increments of ten) used to indicate the quantity of particles of size 0.5 μm or greater in one cubic foot of air

- A *class 100* clean room must maintain a count of particles of size 0.5 μm or greater at less than 100/ft^3
- A *class 10* clean room must maintain a count of particles of size 0.5 μm or greater at less than 10/ft^3
- The clean room is air conditioned to 21°C (70°F) and 45% relative humidity

Silicon Processing

- Microelectronic chips are fabricated on a substrate of semiconductor material
- Silicon is the leading semiconductor material today, constituting more than 95% of all semiconductor devices produced in the world
- Preparation of silicon substrate can be divided into three steps:
  1. Production of electronic grade silicon
  2. Crystal growing
  3. Shaping of Si into wafers

Electronic Grade Silicon

- Silicon is one of the most abundant materials in the earth's crust, occurring naturally as silica (e.g., sand) and silicates (e.g., clay)
- Principal raw material for silicon is *quartzite*, which is very pure SiO_2
- Electronic grade silicon (EGS) is polycrystalline silicon of ultra high purity - so pure that impurities are measured in parts per billion (ppb)

Crystal Growing

- The silicon substrate for microelectronic chips must be made of a single crystal whose unit cell is oriented in a certain direction
  - The silicon used in semiconductor device fabrication must be of ultra high purity
  - The substrate wafers must be cut in a direction that achieves the desired planar orientation
- Most widely used crystal growing method is the *Czochralski process*, in which a single crystal *boule* is pulled upward from a pool of molten silicon

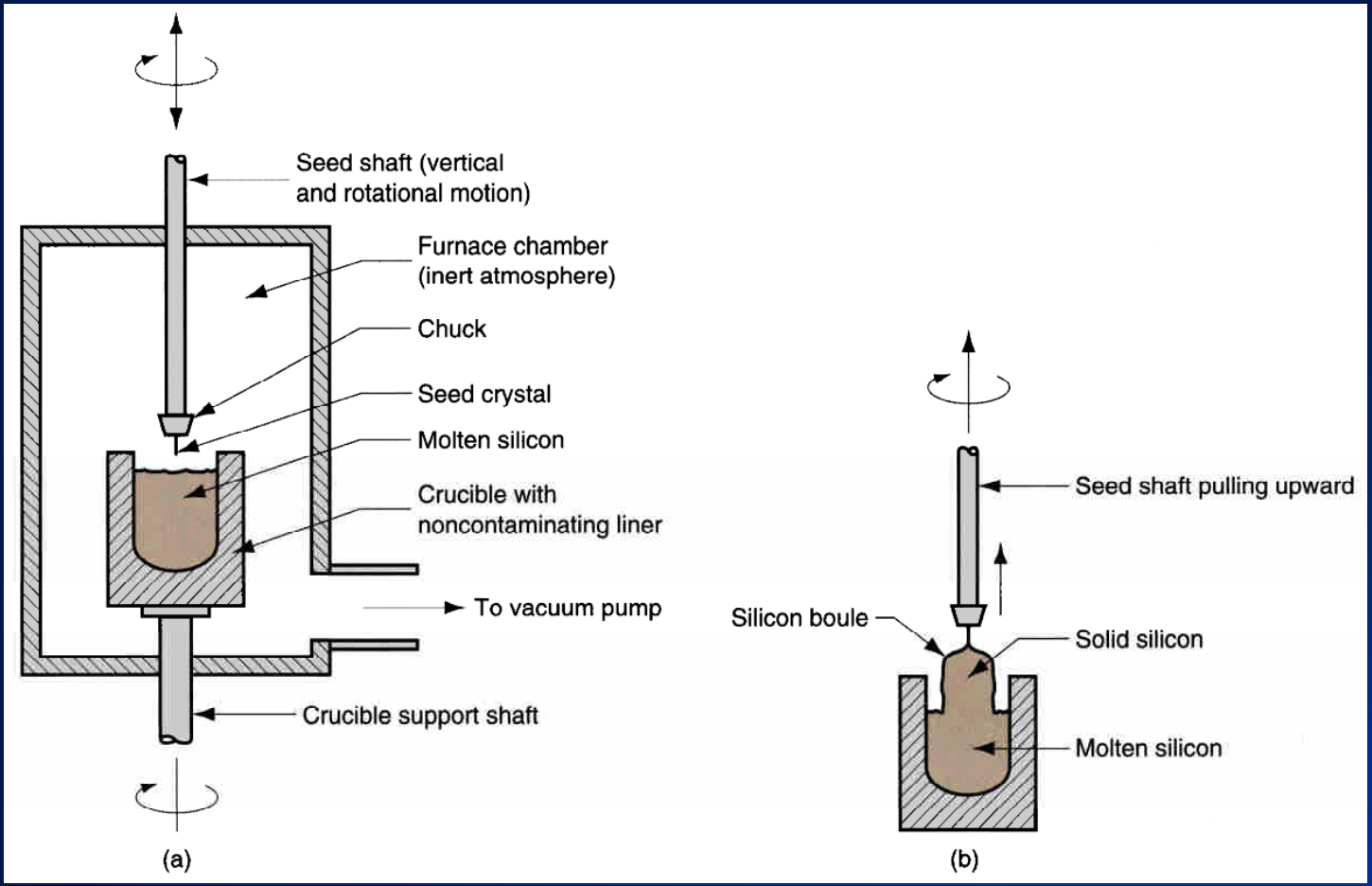

Figure 35.5 - Czochralski process for growing single crystal ingots of silicon: (a) initial setup prior to start of crystal pulling, and (b) during crystal pulling to form the boule

Shaping of Silicon into Wafers

- Processing steps to reduce the boule into thin, disc-shaped wafers
  1. Ingot (boule) preparation
  2. Wafer slicing
  3. Wafer preparation

Preparation of the Boule

- The ends of the boule are cut off
- Cylindrical grinding is used to shape the boule into a more perfect cylinder
- One or more flats are ground along the length of the boule, whose functions, after the boule is cut into wafers, are the following:
  - Identification
  - Orientation of ICs relative to crystal structure
  - Mechanical location during processing

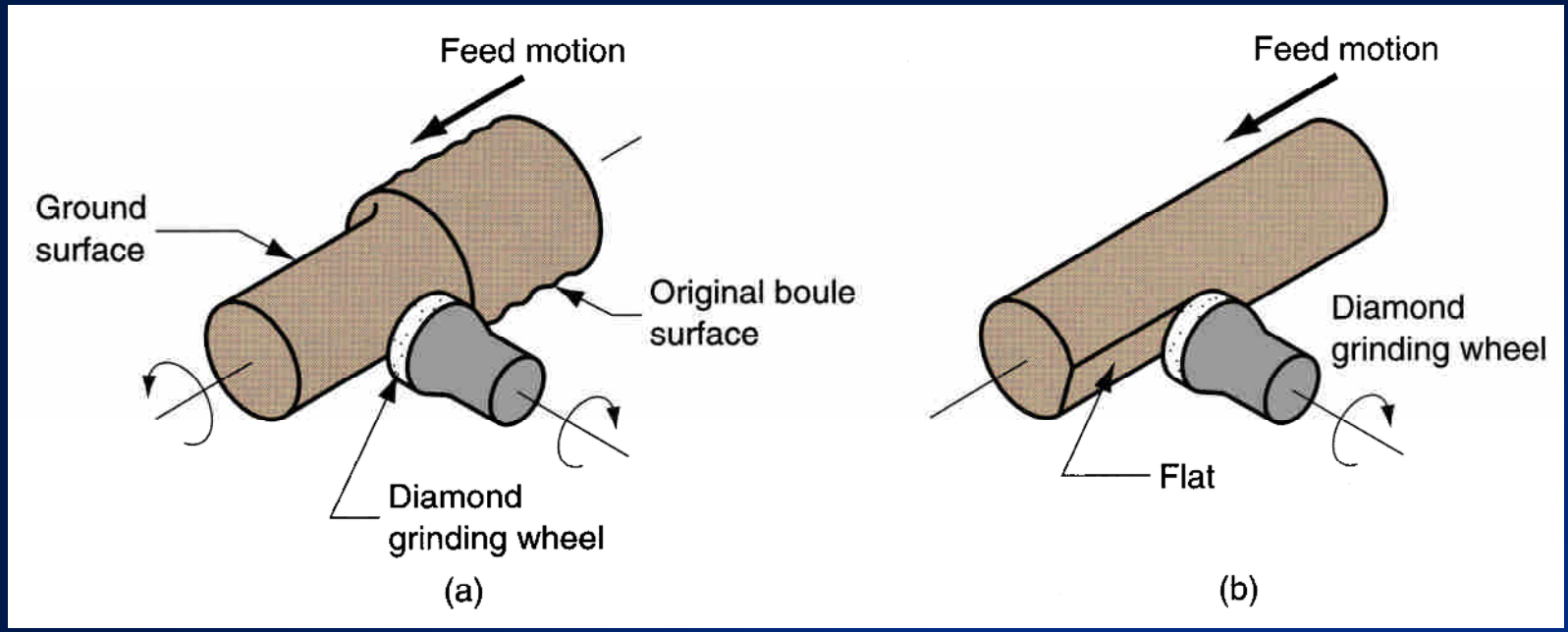

Figure 35.6 - Grinding operations used in shaping the silicon ingot: (a) a form of cylindrical grinding provides diameter and roundness control, and (b) a flat ground on the cylinder

Wafer Slicing

- A very thin ring-shaped saw blade with diamond grit bonded to internal diameter is the cutting edge
  - The ID is used for slicing rather than the OD for better control over flatness, thickness, parallelism, and surface characteristics of the wafer
- Wafers are cut ~ 0.5-0.7 mm (0.020-0.028 in.) thick, greater thicknesses for larger wafer diameters
  - To minimize kerf loss, blades are made very thin: about 0.33 mm (0.013 in.)

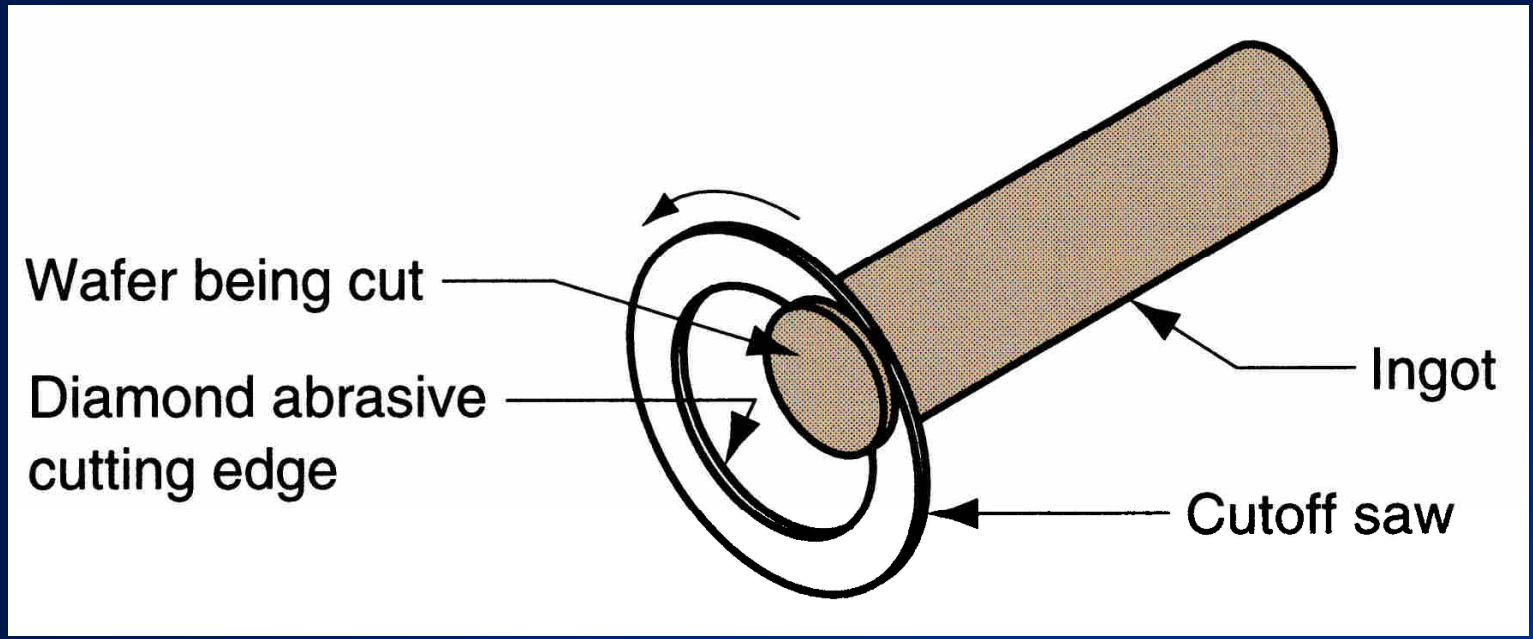

Figure 35.7 - Wafer slicing using a diamond abrasive cut-off saw

Wafer Preparation

- Wafer rims are rounded by contour-grinding wheel to reduce chipping during handling
- Wafers are chemically etched to remove surface damage from slicing
- A flat polishing operation is performed to provide surfaces of high smoothness for photolithography processes to follow
- Finally, the wafer is chemically cleaned to remove residues and organic films

Lithography

- An IC consists of many microscopic regions on the wafer surface that make up the devices and intraconnections as specified in the circuit design
- In the planar process, the regions are fabricated by steps that add, alter, or remove layers in selected areas of the wafer surface
- Each layer is determined by a geometric pattern representing circuit design information that is transferred to the wafer surface by *lithography*

Lithographic Technologies

- Several lithographic technologies are used in semiconductor processing:
  - Photolithography
  - Electron lithography
  - X-ray lithography
  - Ion lithography
- The differences are in type of radiation used to transfer the mask pattern to the wafer surface

Photolithography

- Uses light radiation to expose a coating of photoresist on the surface of the wafer
  - Common light source in wafer processing is *ultraviolet* light, due to its short wavelength
- A *mask* containing the required geometric pattern for each layer separates the light source from the wafer, so that only the portions of the photoresist not blocked by the mask are exposed

The Mask in Photolithography

Flat plate of transparent glass onto which a thin film of an opaque substance has been deposited in certain areas to form the desired pattern

- Thickness of glass plate is around 2 mm (0.080 in), while deposited film is only a few μm thick - for some film materials, less than one μm
- The mask itself is fabricated by lithography, the pattern being based on circuit design data, usually in the form of digital output from the CAD system used by circuit designer

Photoresist

An organic polymer that is sensitive to light radiation in a certain wavelength range

- The sensitivity causes either an increase or decrease in solubility of the polymer to certain chemicals
- Typical practice in semiconductor processing is to use photoresists that are sensitive to ultraviolet light
  - UV light has a short wavelength compared to visible light, permitting sharper imaging of microscopic circuit details on the wafer surface
- Also permits fabrication areas in plant to be illuminated at low light levels outside UV band

Contact Printing

Mask is pressed against resist coating during exposure

- Advantage: high resolution of the pattern onto wafer surface
- Disadvantage: physical contact with wafers gradually wears out mask

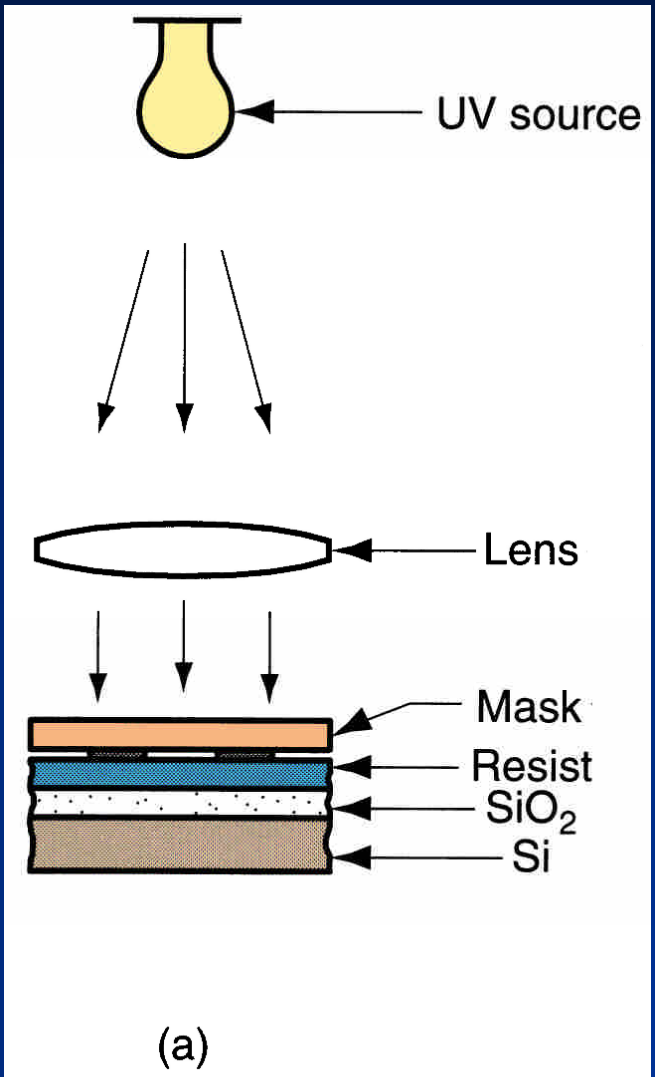

Figure 35.10 - Photolithography exposure techniques: (a) contact printing

Proximity Printing

Mask is separated from the resist coating by a distance of 10-25 μm (0.0004-0.001 in.)

- Eliminates mask wear, but image resolution is slightly reduced

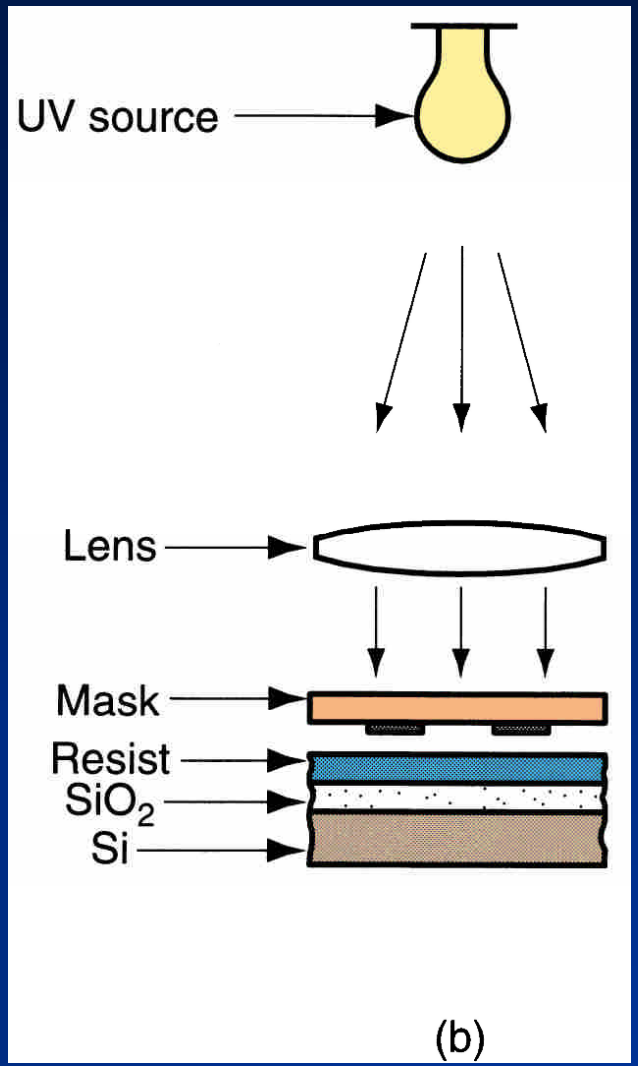

Figure 35.10 - Photolithography exposure techniques: (b) proximity printing

Projection Printing

High-quality lens (or mirror) system projects image through mask onto wafer

- Preferred technique because non-contact (thus, no mask wear), and optical projection can obtain high resolution

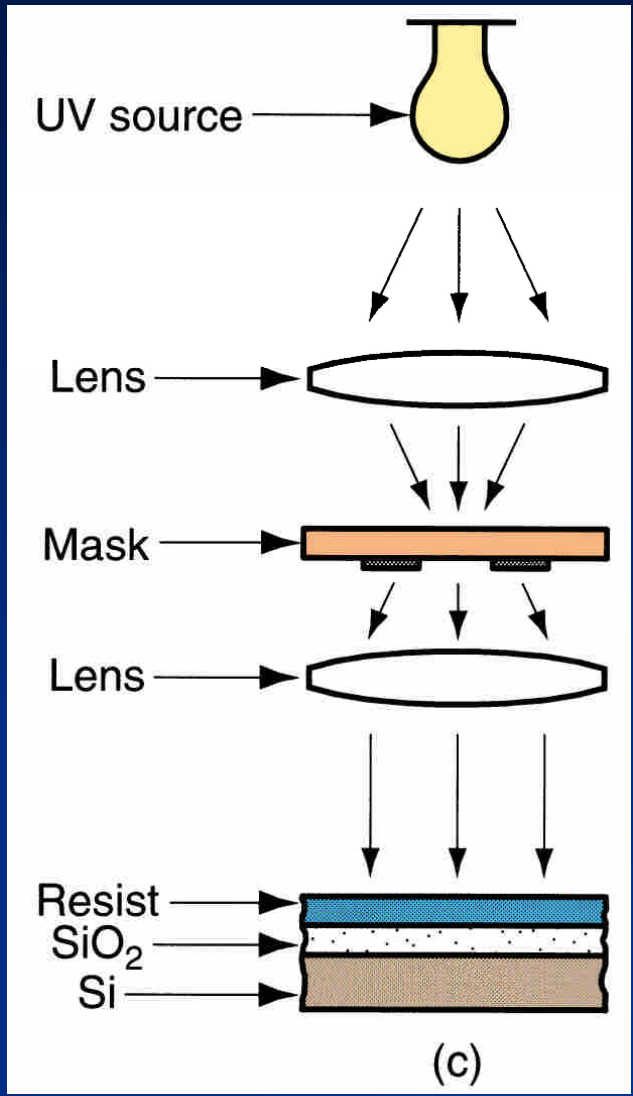

Figure 35.10 - Photolithography exposure techniques: (c) projection printing

Processing Sequence in Photolithography

- Surface of the silicon wafer has been oxidized to form a thin film of SiO_2
- It is desired to remove the SiO_2 film in certain regions as defined by mask pattern
- Sequence for a negative resist proceeds as follows:

1. The wafer is properly cleaned to promote wetting and adhesion of resist

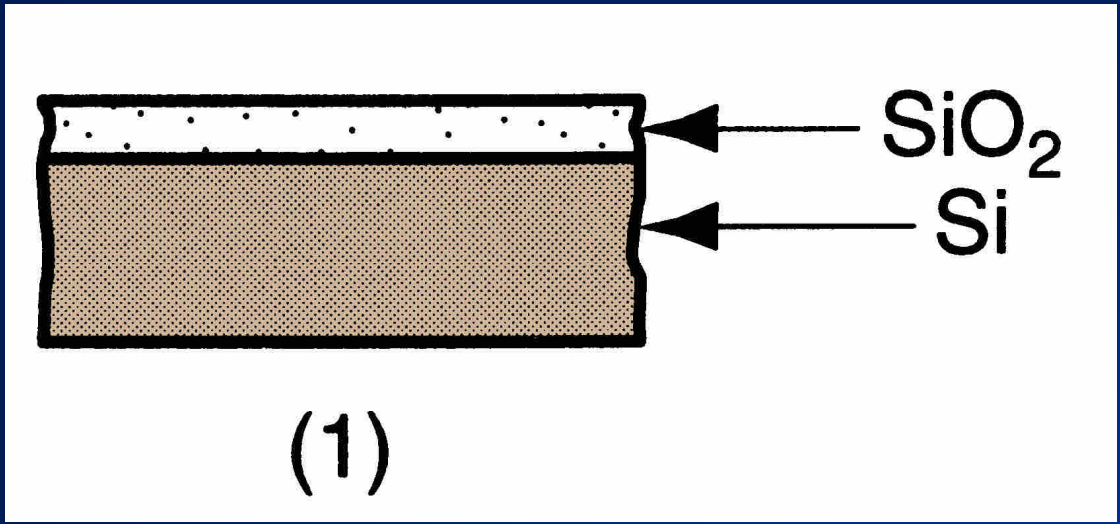

Figure 35.11 - Photolithography process applied to a silicon wafer: (1) prepare surface

2. A metered amount of liquid resist is fed onto center of wafer and wafer is spun to spread liquid and achieve uniform coating thickness

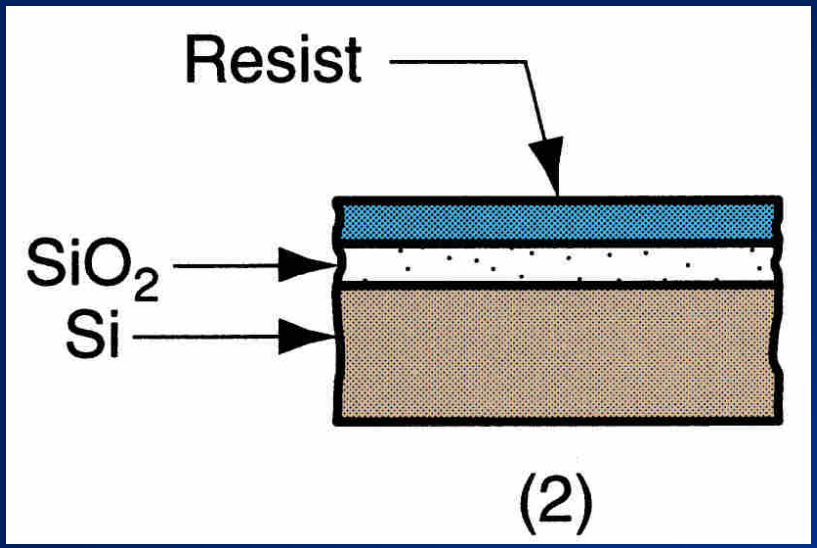

Figure 35.11 - (2) apply photoresist

3. Soft bake - purpose is to remove solvents, promote adhesion, and harden resist

- Temperature ~ 90°C (190°F) for 10-20 minutes

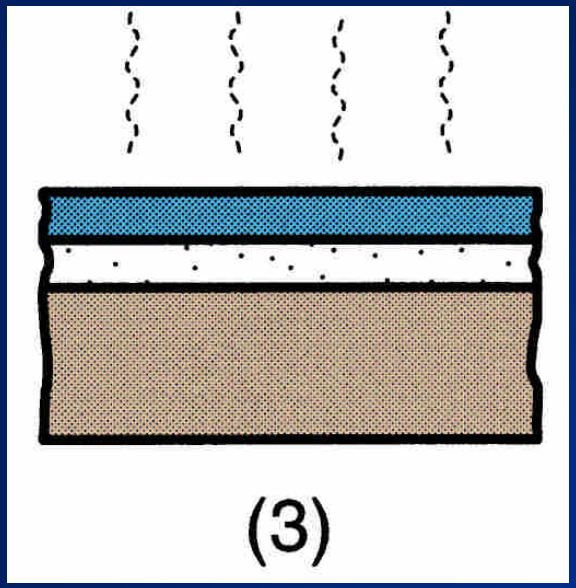

Figure 35.11 - (3) soft-bake

4. Pattern mask is aligned relative to wafer and resist is exposed through mask

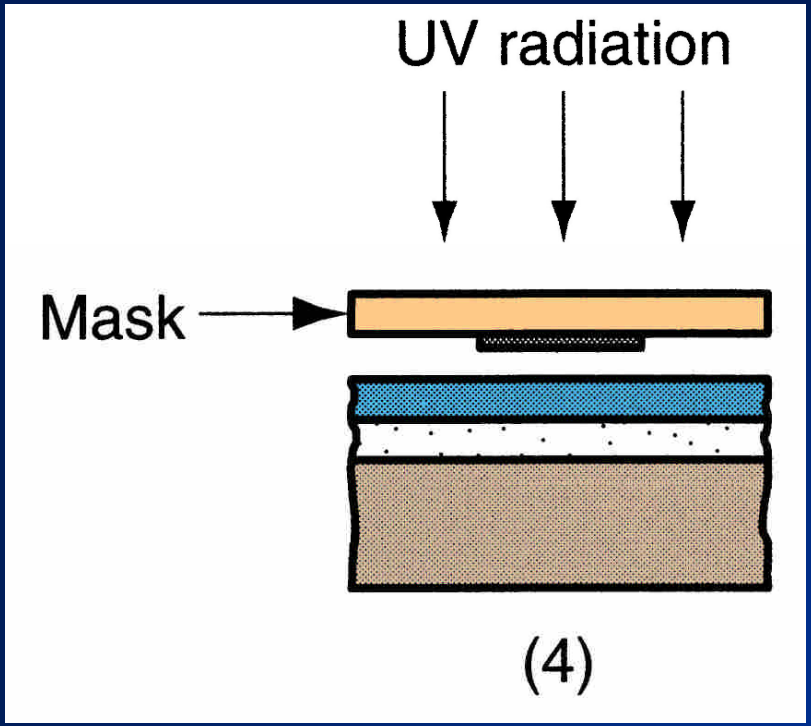

Figure 35.11 - (4) align mask and expose

5. Exposed wafer is immersed in developing solution, or solution is sprayed onto surface

- For negative resist, unexposed areas are dissolved, thus leaving SiO_2 surface uncovered in these areas

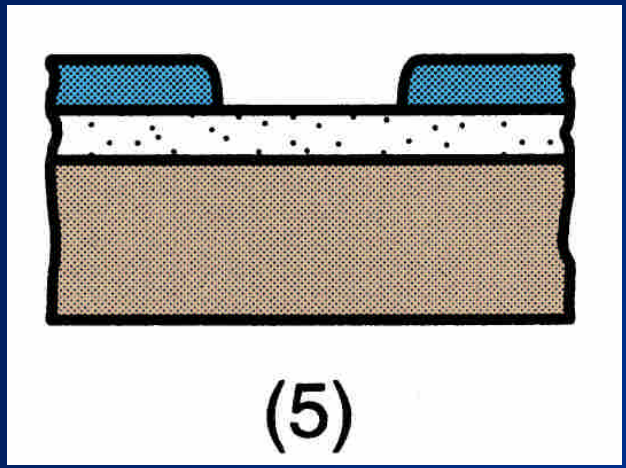

Figure 35.11 - (5) develop resist

6. Hard bake to expel volatiles remaining from developing solution and increases adhesion of resist especially at newly created edges of resist film

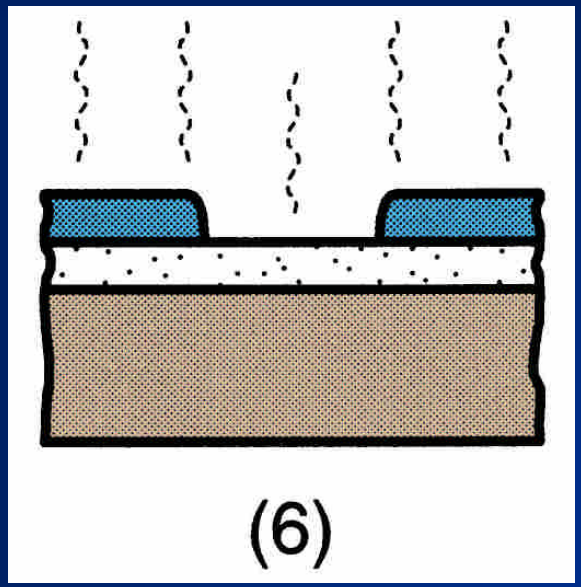

Figure 35.11 - (6) hard-bake

7. Etching removes SiO_2 layer at selected regions where resist has been removed

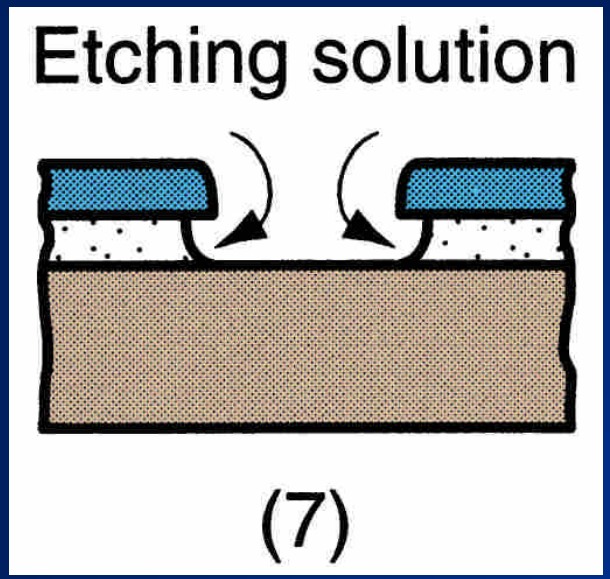

Figure 35.11 - (7) etch

8. Resist coating remaining on surface is removed

- Stripping is accomplished using either liquid chemicals or plasma etching

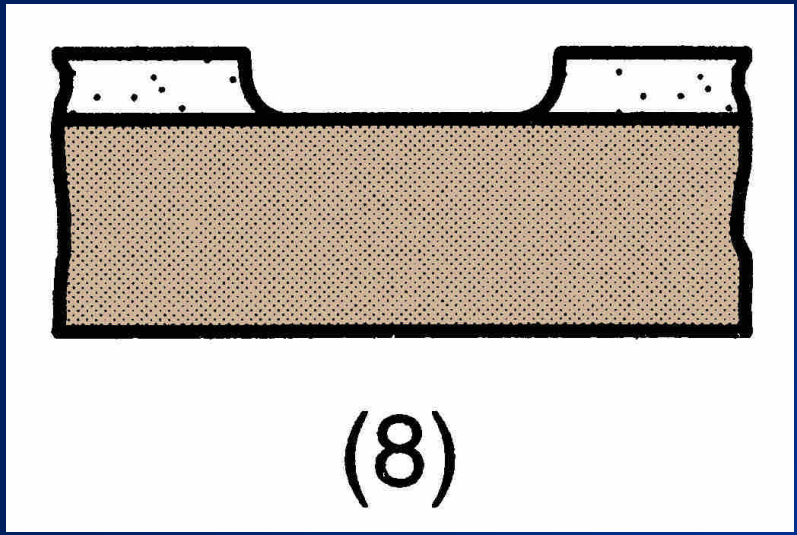

Figure 35.11 - (8) strip resist

Other Lithography Techniques

- As feature size in integrated circuits continues to decrease and UV photolithography becomes increasingly inadequate, other lithography techniques that offer higher resolution are growing in importance:
  - Extreme ultraviolet (EUV) lithography
  - Electron beam lithography
  - X-ray lithography
  - Ion lithography

Layer Processes Used in IC Fabrication (Part II)

- Steps to fabricate ICs on a silicon wafer consist of chemical and physical processes that add, alter, or remove regions that have been defined by photolithography
- These surface regions constitute insulating, semiconducting, and conducting areas that form the devices and their intraconnections in the IC
- Layers are fabricated one at a time, each layer requiring a separate mask, until all of the microscopic details of the electronic devices and conducting paths have been fabricated on wafer surface

Processes that Add, Alter, or Remove Layers in IC Fabrication

- *Thermal oxidation* – adds SiO_2 layer on Si substrate
- *Chemical vapor deposition* - adds various layers
- *Diffusion and ion implantation* - alters chemistry of an existing layer or substrate
- *Metallization processes* - adds metal layers for electrical conduction
- *Etching processes* - removes portions of layers to achieve desired IC details

Thermal Oxidation of Silicon

Exposure of silicon wafer surface to an oxidizing atmosphere at elevated temperature to form layer of silicon dioxide

- Oxygen or steam atmospheres are used, with the following reactions, respectively:

$$Si + O_2 \rightarrow SiO_2$$

or

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

Functions of Silicon Dioxide (SiO_2)

SiO_2 is an insulator, compared to Si which is a semiconductor

- Used as a mask to prevent diffusion or ion implantation of dopants into silicon
- Can be used to isolate devices in circuit
- Provides electrical insulation between levels in multi-level metallization systems

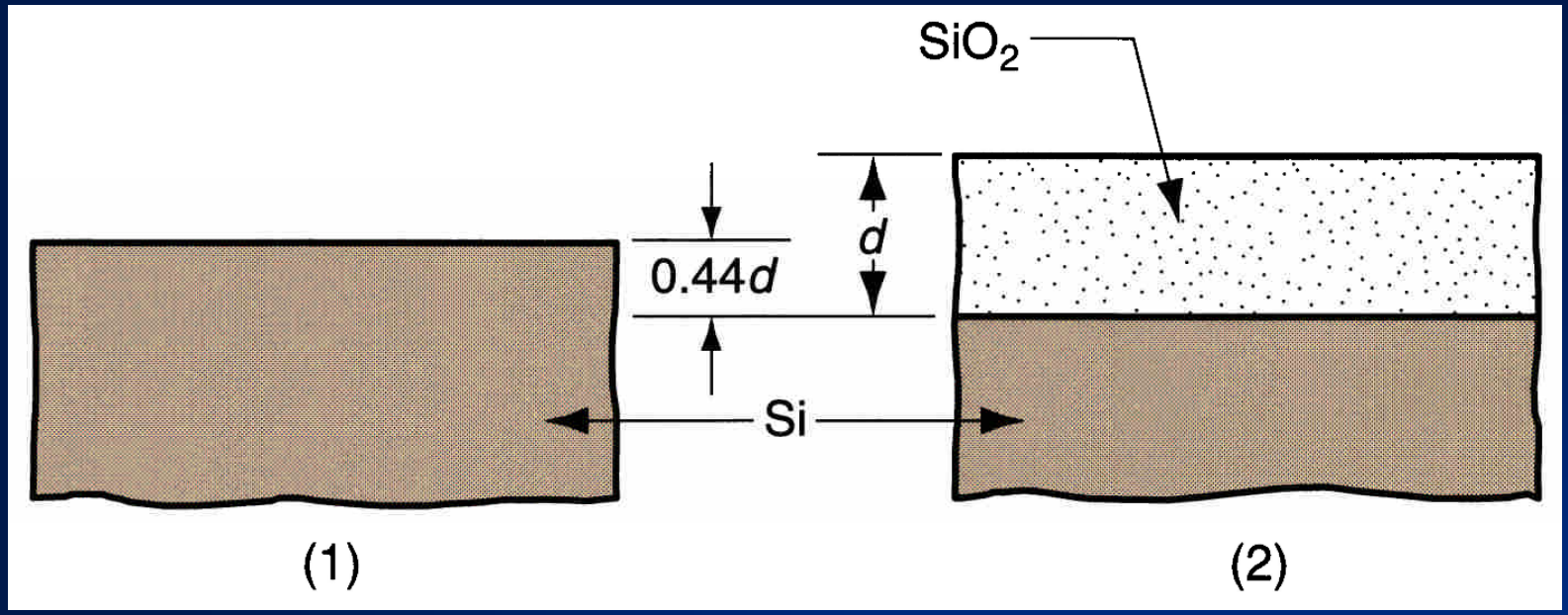

Figure 35.12 - Growth of SiO_2 film on a silicon substrate by thermal oxidation, showing changes in thickness that occur:

(1) before oxidation and (2) after thermal oxidation

Alternative Process for Adding SiO_2

- When a silicon dioxide film must be applied to surfaces other than silicon, then direct thermal oxidation does not work
- An alternative process must be used, such as chemical vapor deposition (CVD)

Introduction of Impurities into Silicon

- IC technology relies on the ability to alter the electrical properties of silicon by introducing impurities into selected regions of the surface
- Adding impurities into silicon surface is called *doping*
- Common doping elements are boron (B) which forms electron acceptor regions (p-type regions); and phosphorous (P), arsenic (As砷), and antimony (Sb銻), which form electron donor regions (n-type regions)
- Techniques for doping silicon are (1) diffusion and (2) ion implantation

Thermal Diffusion

Process in which atoms migrate from regions of high concentration into regions of lower concentration

- In semiconductor processing, diffusion is carried out to dope the silicon substrate with controlled amounts of a desired impurity
- Carried out in two steps:
  1. Predeposition - the dopant is deposited onto wafer surface
  2. Drive-in - heat treatment in which dopant is redistributed to obtain the desired depth and concentration profile

Ion Implantation

Vaporized ions of impurity element are accelerated by an electric field and directed at silicon substrate

- The atoms penetrate into surface, losing energy and finally stopping at some depth in crystal structure determined by mass of ion and acceleration voltage
- Advantages:
  - Can be accomplished at room temperature
  - Provides exact doping density

Metallization

Combines various thin film deposition technologies with photolithography to form very fine patterns of conductive material

- Functions of conductive materials on wafer surface:
  - Form certain components (e.g., gates) of IC devices
  - Provide intraconnecting conduction paths between devices on chip
  - Connect the chip to external circuits

Metallization Materials

- Aluminum - most widely used metallization material
  - Favored for device intraconnections and connections to external circuitry
- Other materials: polysilicon (Si); gold (Au); refractory metals (e.g., W, Mo); silicides (e.g., WSi_2, $MoSi_2$, $TaSi_2$); and nitrides (e.g., TaN, TiN, and ZrN)
  - Applications such as gates and contacts

Metallization Processes

- *Physical vapor deposition* – PVD metallization processes include vacuum evaporation and sputtering
- *Chemical vapor deposition* – CVD deposited materials include tungsten, molybdenum, and most silicides used in semiconductor metallization
- *Electroplating* - occasionally used to increase thickness of thin films

Etching

- Certain steps in IC manufacturing require material removal from surface, accomplished by etching away unwanted material
- Usually done selectively, by masking surface areas that are to be protected and leaving other areas exposed
- Two categories of etching process:
  1. Wet chemical etching
  2. Dry plasma etching

Wet Chemical Etching

Use of an aqueous solution, usually an acid, to etch away a target material

- Etchant is selected to chemically attack the specific material to be removed and not the protective layer
- In its simplest form, etching is accomplished by immersing the masked wafers in etchant for a specified time and then immediately transferring them to a thorough rinsing procedure to stop the etching
- Process variables: immersion time, etchant concentration, and temperature

- Chemical etching reaction is *isotropic*, resulting in an undercut below protective mask
- Mask pattern (resist) must be sized to compensate for this effect

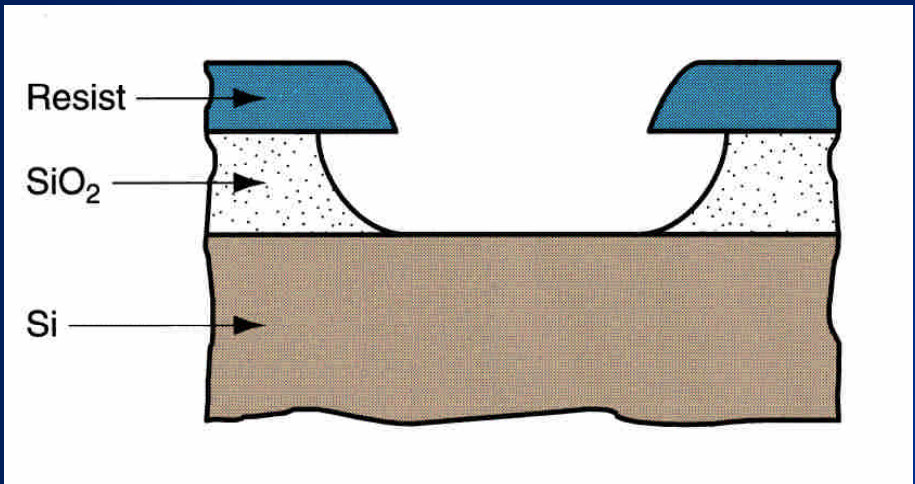

Figure 35.13 - Profile of a properly etched layer

Dry Plasma Etching

Uses an ionized gas to etch a target material

- Ionized gas is created by introducing an appropriate gas mixture into vacuum chamber and RF electrical energy is used to ionize a portion of the gas to create a plasma
- The high energy plasma reacts with the target surface, vaporizing material to remove it

Example: Process Integration in IC Fabrication

- An n-channel metal oxide semiconductor (NMOS) logic device will be used to illustrate processing sequence
- Sequence for NMOS ICs is less complex than for CMOS or bipolar technologies, although processes for these IC categories are similar
- Starting substrate is a lightly doped p-type silicon wafer, which will form the base of n-channel transistor

1. A layer of Si_3N_4 is deposited by CVD onto Si substrate using photolithography to define the regions – the layer will serve as a mask for thermal oxidation in step (2)

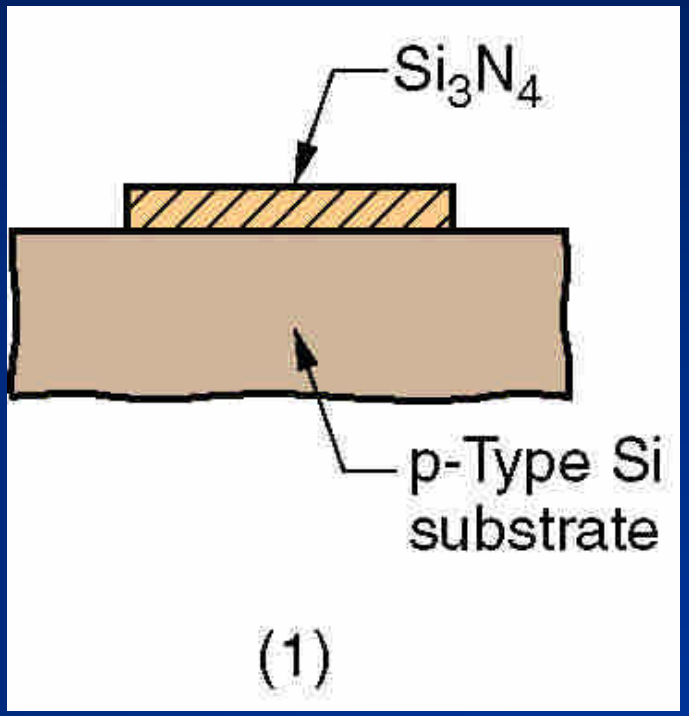

Figure 35.17 - IC fabrication sequence: (1) Si_3N_4 mask is deposited by CVD on Si substrate

2. SiO_2 is grown in exposed regions of surface by thermal oxidation
- SiO_2 regions are insulating and will isolate this device from other devices

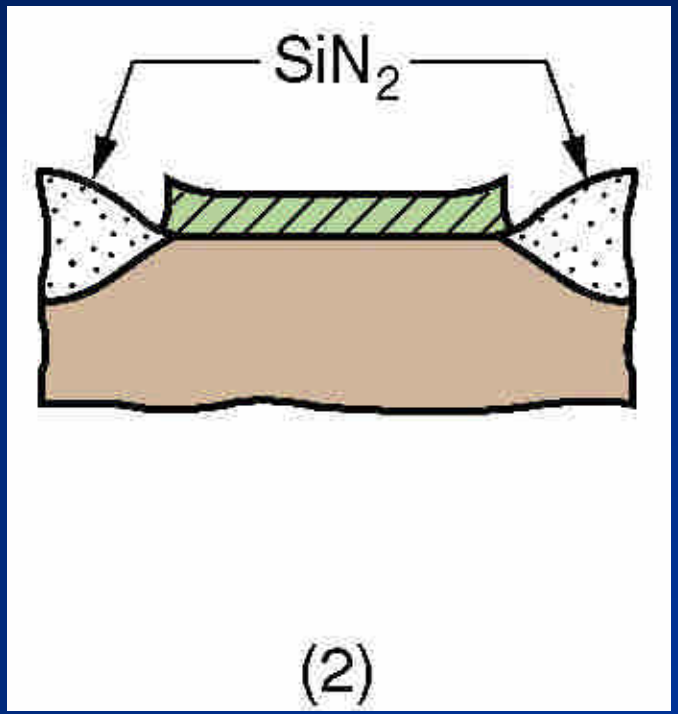

Figure 35.17 - (2) SiO_2 is grown by thermal oxidation in unmasked regions

3. The Si_3N_4 mask is stripped by etching

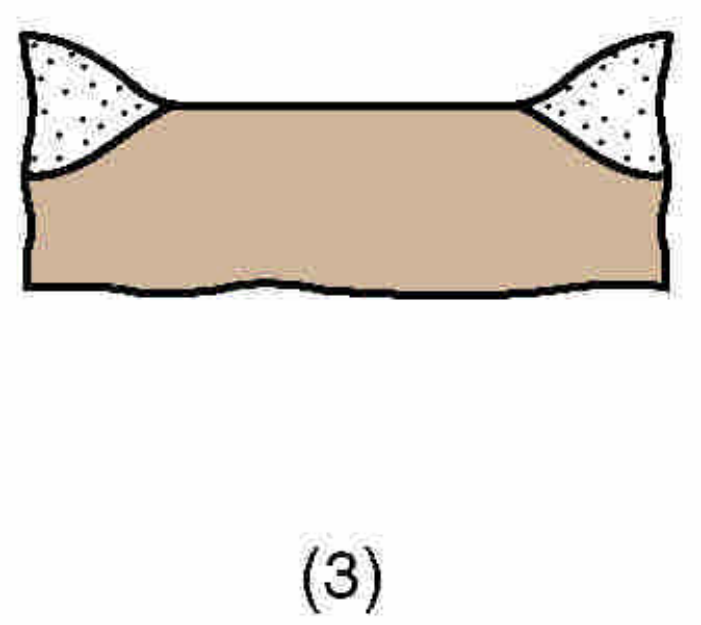

Figure 35.17 - (3) the Si_3N_4 mask is stripped

4. Another thermal oxidation is done to add a thin gate oxide layer to previously uncoated surfaces and to increase thickness of previous SiO_2 layer

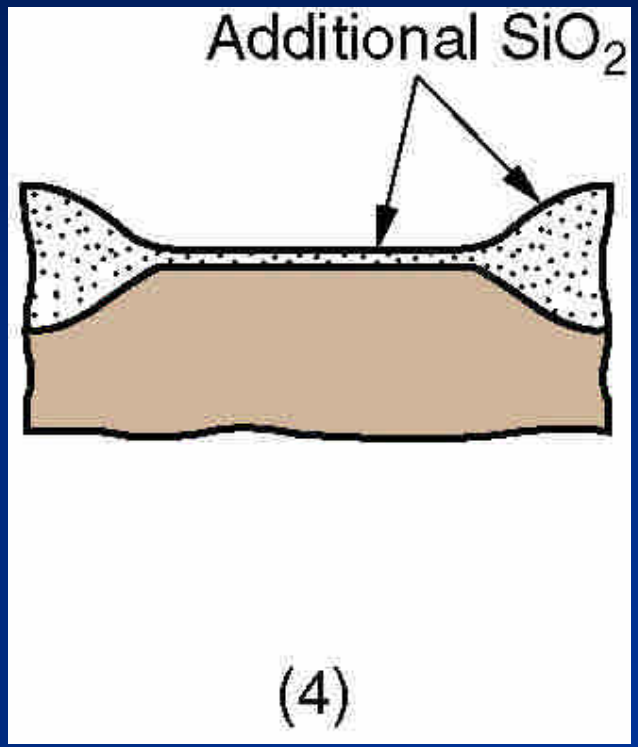

Figure 35.17 -(4) a thin layer of SiO_2 is grown by thermal oxidation

5. Polysilicon is deposited by CVD onto surface and then doped n-type using ion implantation

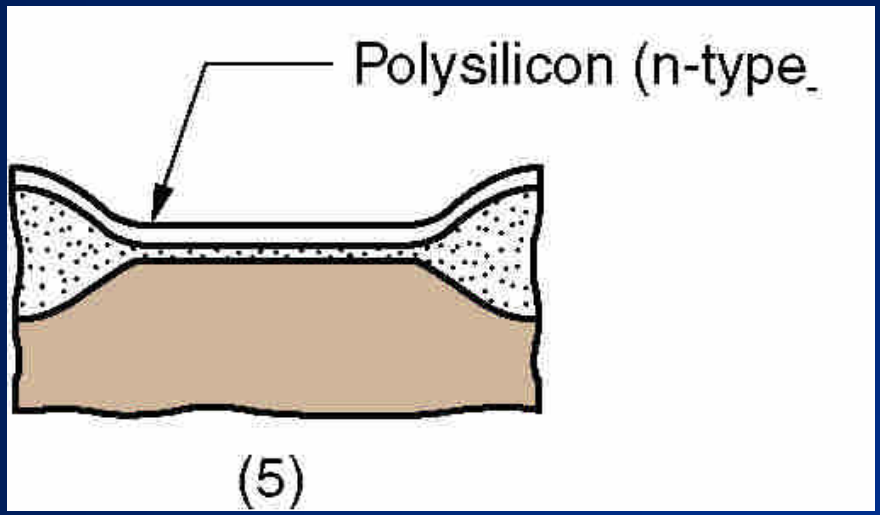

Figure 35.17 - (5) Polysilicon is deposited by CVD and doped n+ using ion implantation

6. The polysilicon is selectively etched using photolithography to form gate electrode of transistor

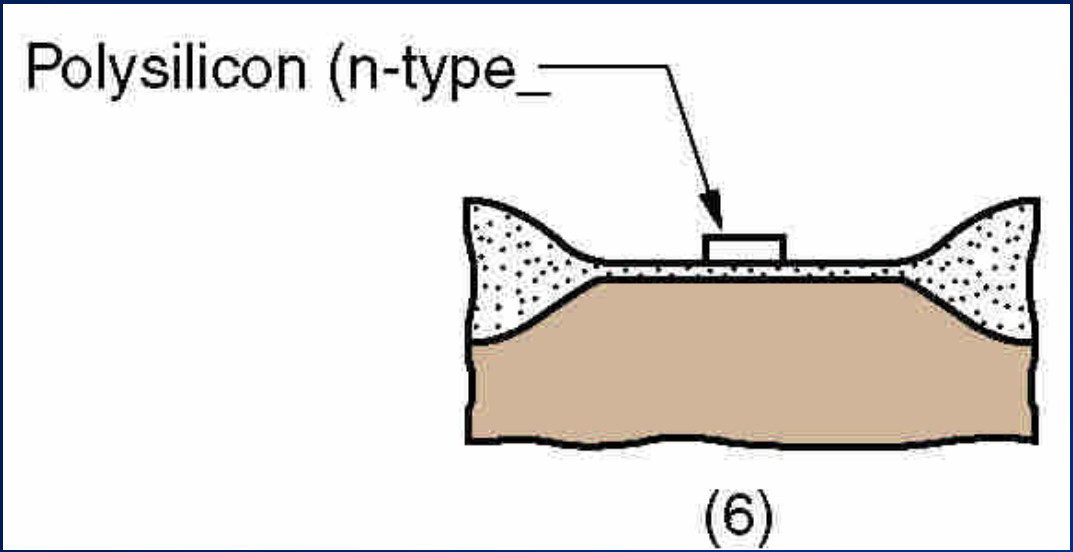

Figure 35.17 - (6) the poly-Si is selectively etched using photolithography to define the gate electrode

7. Source and drain regions (n+) are formed by ion implantation of arsenic (As) into substrate, selecting an implantation energy level that penetrates the thin SiO_2 layer but not the polysilicon gate or the thicker SiO_2 isolation layer

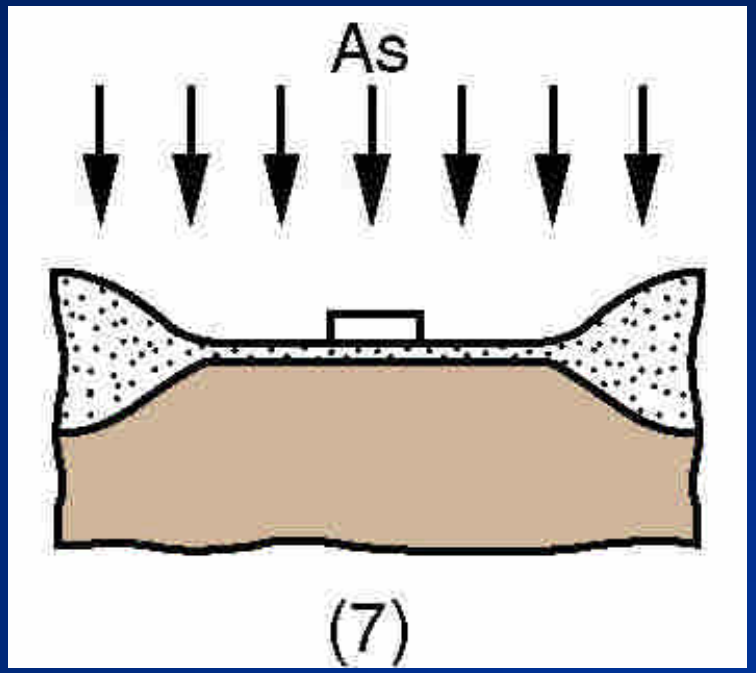

Figure 35.17 - (7) source and drain regions are formed by doping n+ in the substrate

8. Phosphosilicate glass (P-glass) is deposited onto the surface by CVD to protect the circuitry beneath

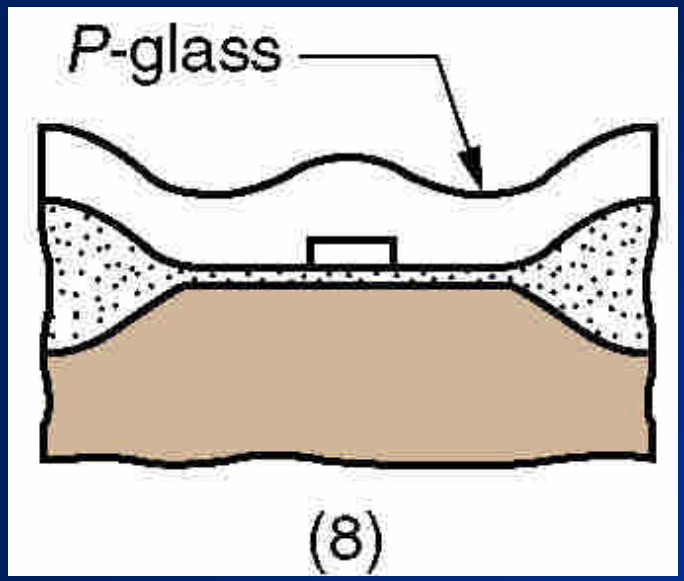

Figure 35.17 - (8) P-glass is deposited onto the surface for protection

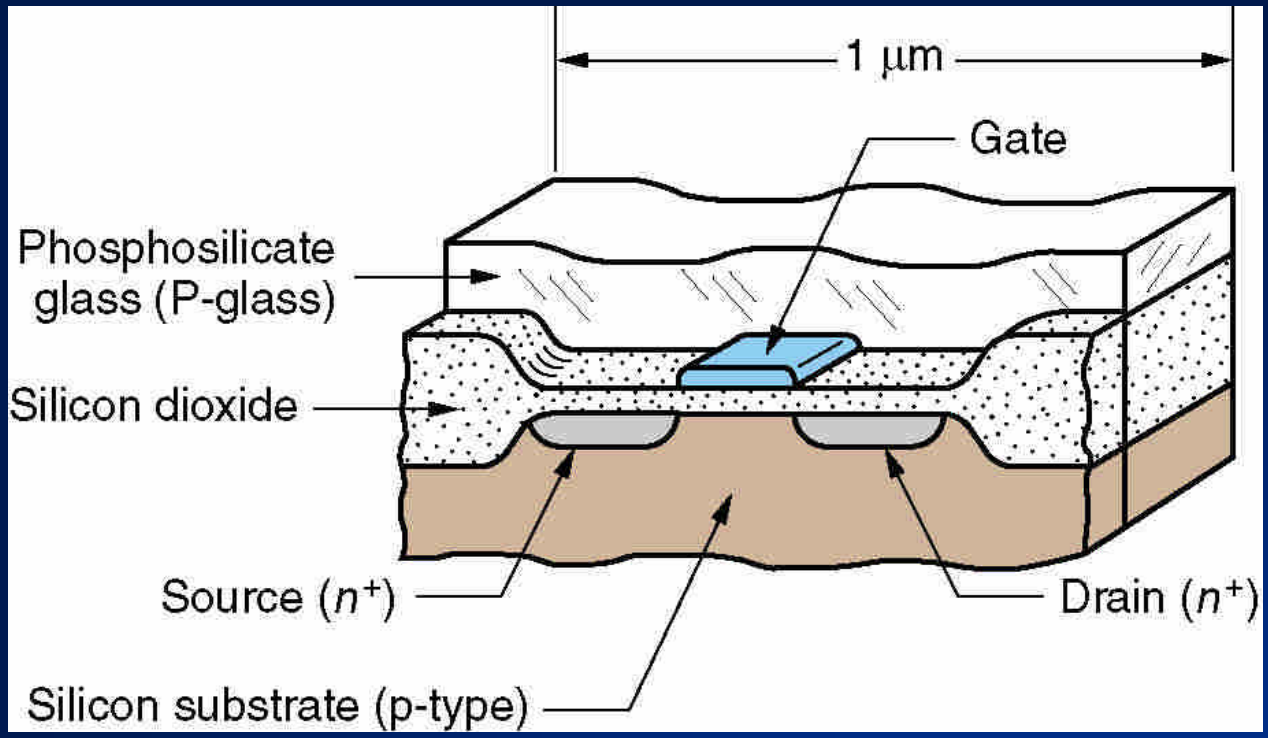

Figure 35.1 - Cross-section of a transistor (specifically, a MOSFET) in an integrated circuit. Approximate size of the device is shown; feature sizes within the device can be less than 1 μm with current technology.

IC Packaging (Part III)

The final series of operations to transform the wafer into individual chips, ready to connect to external circuits and prepared to withstand the harsh environment of the world outside the clean room

- Accomplished after all of the processing steps on the wafer have been completed

Design Issues in IC Packaging

- Electrical connections to external circuits
- Materials to encase chip and protect it from the environment (humidity, corrosion, temperature, vibration, mechanical shock)
- Heat dissipation
- Performance, reliability, and service life
- Cost

Manufacturing Issues in IC Packaging

- Chip separation - cutting wafer into individual chips
- Connecting it to the package
- Encapsulating the chip
- Circuit testing

IC Package Design

- Topics related to the design of an integrated circuit package:
  - Number of input/output terminals required for an IC of a given size
  - Materials used in IC packages
  - Package styles

Input/Output (I/O) Terminals in IC Packaging

- The basic problem is to connect many internal circuits on the chip to I/O terminals so that the appropriate electrical signals can be communicated to the outside world
- As the number of devices in the IC increases, the required number of I/O terminals also increases
- The problem is aggravated by IC trends:
  - Decreases in device size
  - Increases in number of devices in IC

IC Package Materials

- Ceramic (Al_2O_3)
  - Advantages: hermetic sealing of IC chip and highly complex packages can be produced
  - Disadvantage: poor dimensional control due to shrinkage during firing
- Plastic (epoxies, polyimides, and silicones)
  - Not hermetically sealed, but cost is lower
  - Generally used for mass produced ICs, where very high reliability is not required

Two Basic IC Package Styles for Mounting to a Printed Circuit Board (PCB)

1. Through-hole mounting, also called pin-in-hole (PIH) technology
   - IC package and other components have leads inserted through holes in PCB and soldered on underside
2. Surface mount technology (SMT)
   - Components are attached to surface of board (in some cases, both top and bottom surfaces)

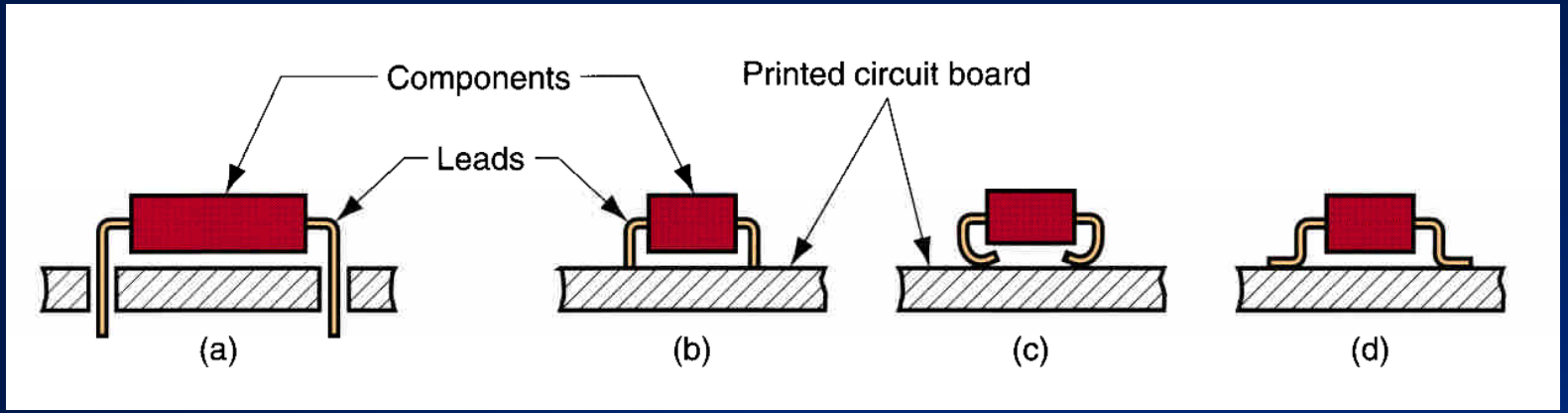

Figure 35.18 - Types of component lead attachment on a printed circuit board: (a) through-hole, and several styles of surface mount technology: (b) butt lead, (c) "J" lead, and (d) gull-wing

Major IC Package Styles

- Dual in-line package (DIP)
- Square package
- Pin grid array
- Some of these are available in both through-hole and surface mount styles, while others are designed for only one mounting method

DIP is currently the most common form of IC package, available in both through-hole and surface mount configurations

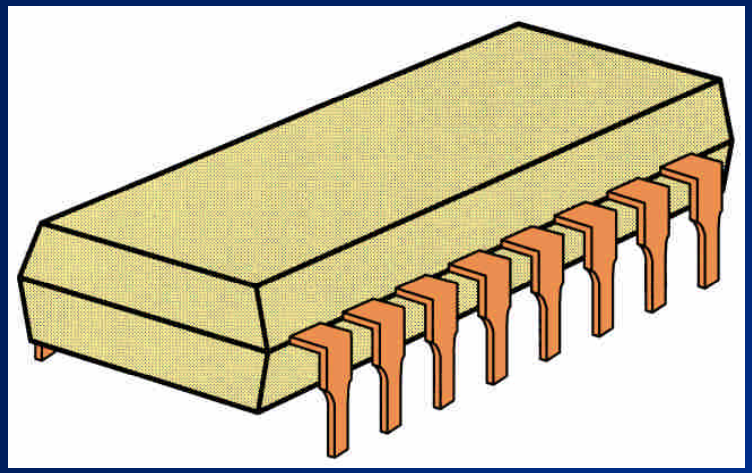

Figure 35.19 - Dual in-line package with 16 terminals, shown here in through-hole configuration

Square Package

- Leads are arranged around periphery so that number of terminals on a side is $n_{io}/4$

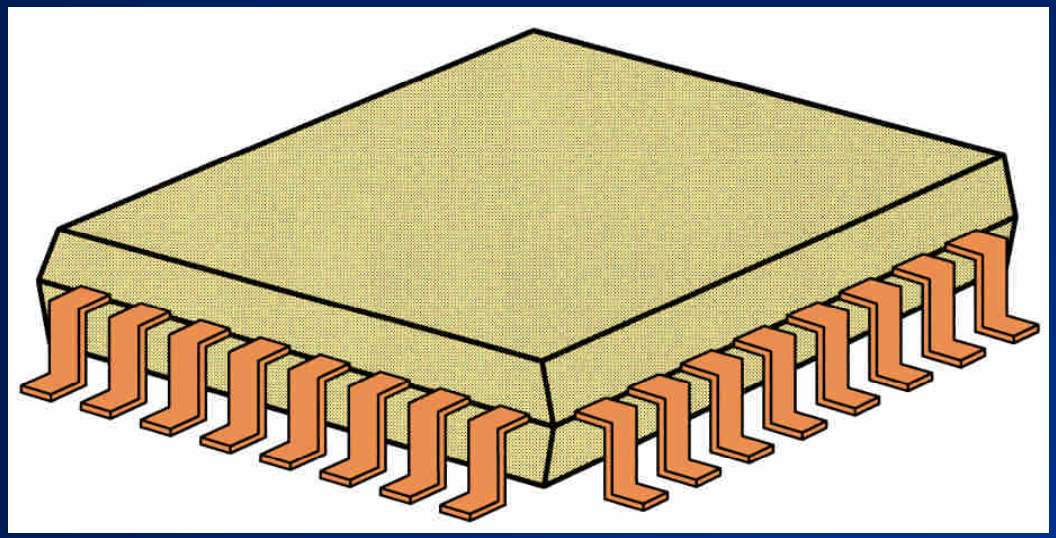

Figure 35.20 - Square leaded chip carrier (LCC) for surface mounting with gull wing leads

Pin Grid Array (PGA)

Two dimensional array of pin terminals on underside of a square chip enclosure

- Square matrix of pins maximizes number of leads on a package
- Ideally, entire bottom surface of package is fully occupied by pins, so pin count in each direction is square root of n_{io}
  - However, center area of package has no pins because this region contains IC chip

Processing Steps in IC Packaging

- Wafer testing
- Chip separation
- Die bonding
- Wire bonding
- Package sealing
- Final testing

Wafer Testing

Testing (called *multiprobe*) is accomplished by computer-controlled equipment that uses needle probes matching connecting pads on the chip surface

- Many of these tests are performed while ICs are still on wafer - before separation
- When probes contact pads, tests are carried out to indicate short circuits and other faults, followed by a functional test
- Chips that fail the test are marked with an ink dot
  - These defects will not be packaged

Chip Separation

A thin diamond-impregnated saw blade is used to cut wafer into individual chips

- The wafer is attached to a piece of adhesive tape mounted in a frame
  - Adhesive tape holds individual chips in place during and after sawing
  - The frame is a convenience in subsequent handling of the chips
- Chips with ink dots are now discarded

Die Bonding

- Automated handling systems pick separated chips from tape frame and place them for die bonding
- Various techniques are used to bond the chip to the packaging substrate, including:
  1. Eutectic die bonding – for ceramic packages
  2. Epoxy die bonding – for plastic packages

After die is bonded to package, electrical connections are made between contact pads on chip surface and package lead frame using small diameter wires

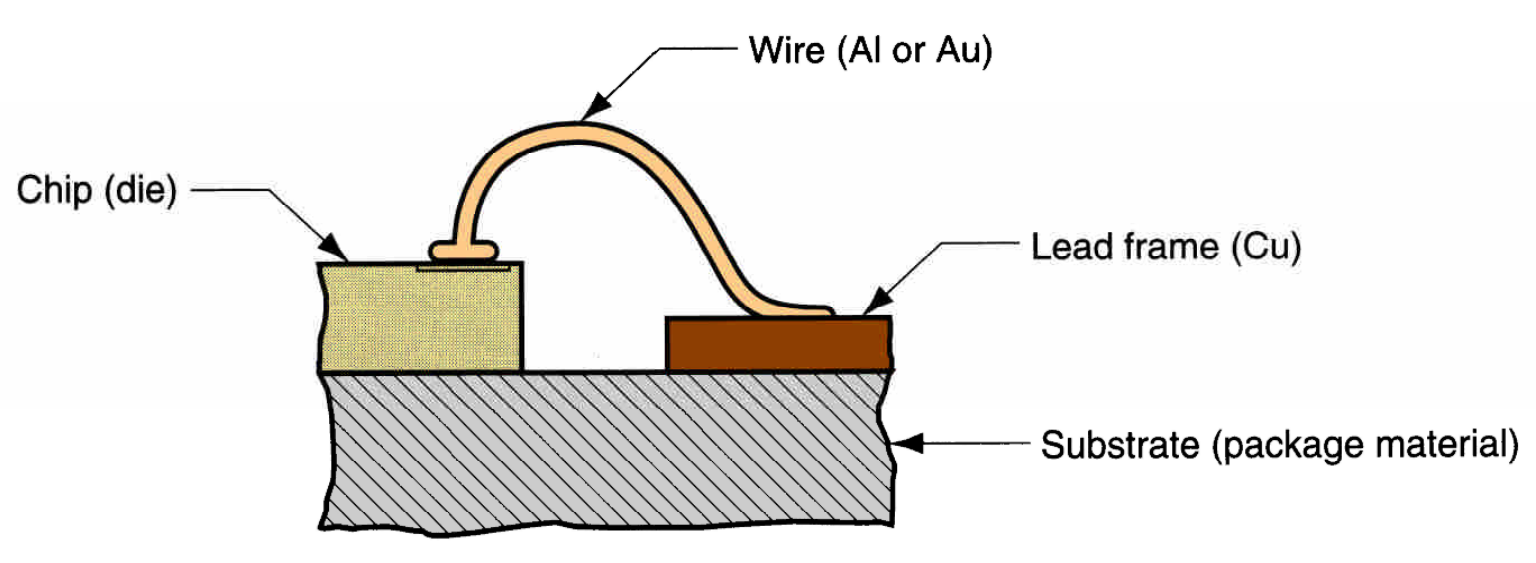

Figure 35.21 - Typical wire connection between chip contact pad and lead

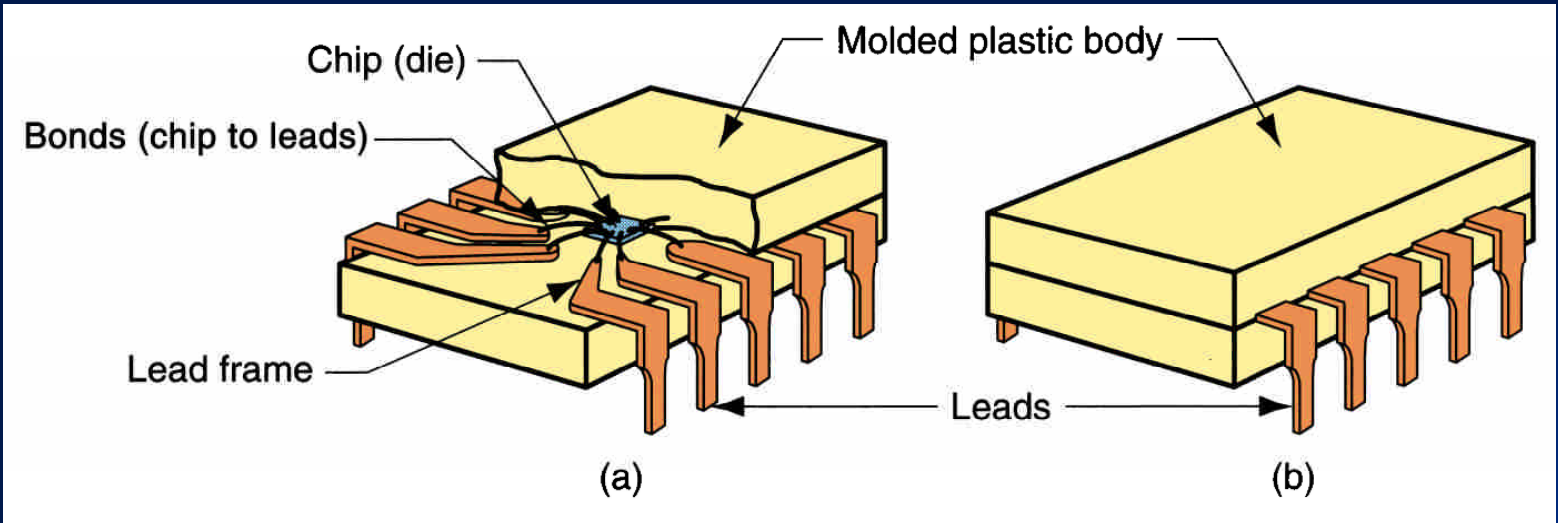

Figure 35.2 - Packaging of an integrated circuit chip: (a) cutaway view showing the chip attached to a lead frame and encapsulated in a plastic enclosure

Final Testing

- Upon completion of packaging sequence, each IC must undergo a final test
- Purpose of test:
  - Determine which units, if any, have been damaged during packaging
  - Measure performance characteristics of each device

Yields in IC Processing

- Fabrication of ICs consists of many processing steps performed in sequence
  - In wafer processing in particular, there may be hundreds of distinct operations performed on the wafer
- At each step, there is a chance that something may go wrong, resulting in the loss of the wafer or portions of it corresponding to individual chips

Yields of Major Processing Steps

1. *Crystal yield* Y_c - material in boule relative to starting amount of electronic grade silicon: $Y_c \sim 50\%$
2. *Crystal-to-slice yield* Y_s - material left after grinding boule and sawing into wafers (kerf losses): $Y_s \sim 50\%$
3. *Wafer yield* Y_w - wafers surviving processing relative to starting quantity: $Y_w \sim 70\%$
4. *Multiprobe yield* Y_m – proportion passing multiprobe test: $Y_m < 10\%$ to $Y_m > 90\%$
5. *Final test yield* Y_t – proportion to pass final test after packaging: $Y_t = 90\%$ to 95%

Probability Model to Predict Yield

A simple probability model to predict the final yield of good product is:

$$Y = Y_c\ Y_s\ Y_w\ Y_m\ Y_t$$

- Given the typical values at each step, the final yield compared to the starting amount of silicon is quite low

Wafer Processing is Key to Successful IC Fabrication

- For an IC producer to be profitable, high yields must be achieved during wafer processing
- This is accomplished by utilizing:
  - Purest possible starting materials
  - Latest equipment technologies
  - Good process control over processing steps
  - Maintenance of clean room conditions
  - Efficient and effective inspection and testing procedures