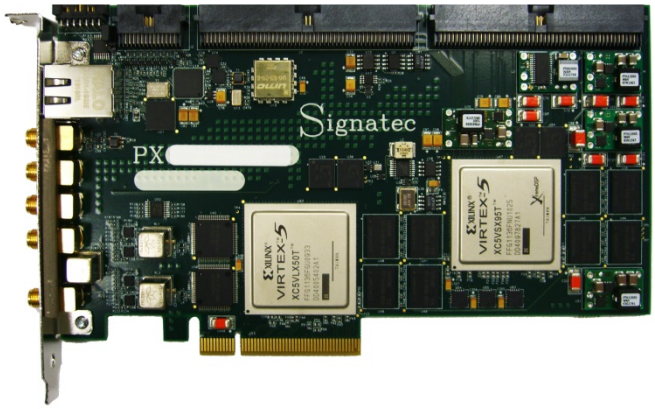
Product Information Sheet

PX14400D2

14-Bit, 400 MS/s, 2 CH DC-Coupled, PCIe Digitizer



FEATURES

- Up to 400 MHz Sample Rate per Channel
- 14 Bits of Resolution
- 2 DC-Coupled Analog Input Channels
- Bandwidth from DC to 248 MHz
- 512 MB Onboard RAM for Sample Acquisition
- 1.4 GB/s Sustained PCIe Data Streaming Rate
- Dedicated Xilinx Virtex-5 FPGA Processing Options
- 512 MB Onboard RAM for Dedicated FPGA Processing Option
- DDC, FFT, FIR Filtering, or User Custom FPGA Processing Routines
- Windows Scope App and Complete C SDK Included
- Windows and Linux Operating Systems Supported

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
  - Medical Diagnostics
  - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

OVERVIEW

The PX14400D2 is a dual channel DC-coupled waveform capture board that can acquire up to 400 MS/s on each channel with 14-bit resolution. (For AC-coupled requirements, refer to PX14400A product model.) The PX14400D2 analog front end has a signal frequency capture range of DC to 248 MHz with 3-pole Bessel filters on each input channel.

The PX14400D2 has six software selectable gain input voltage ranges for each channel. The full scale peak-to-peak input voltage ranges are 200mV, 333mV, 600mV, 1V, 1.6V, and 3V with various bandwidth specifications at each of these input ranges. Optional inline SMA attenuators are available for changing these levels if needed.

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any value from 20 MHz to 400 MHz (except for an un-settable range of 277 MHz to 308 MHz), offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, ±5 PPM reference clock or to an externally provided 10 MHz reference clock. The ADC may also be clocked from an external clock source.

The PX14400D2 has a primary sample-data RAM bank of 512 MB memory for onboard sample data storage. Alternatively, PCIe Buffered Acquisition mode utilizes the onboard RAM as a FIFO to provide non-stop continuous acquisition and streaming of sample data to the host PC via the PCIe interface. With PCIe Buffered Acquisition mode, the PX14400D2 can sustain up to a maximum 1.4 GB/s data streaming rate over its PCIe Gen1 x8 interface to the host PC for real-time high-speed processing and/or data recordings.

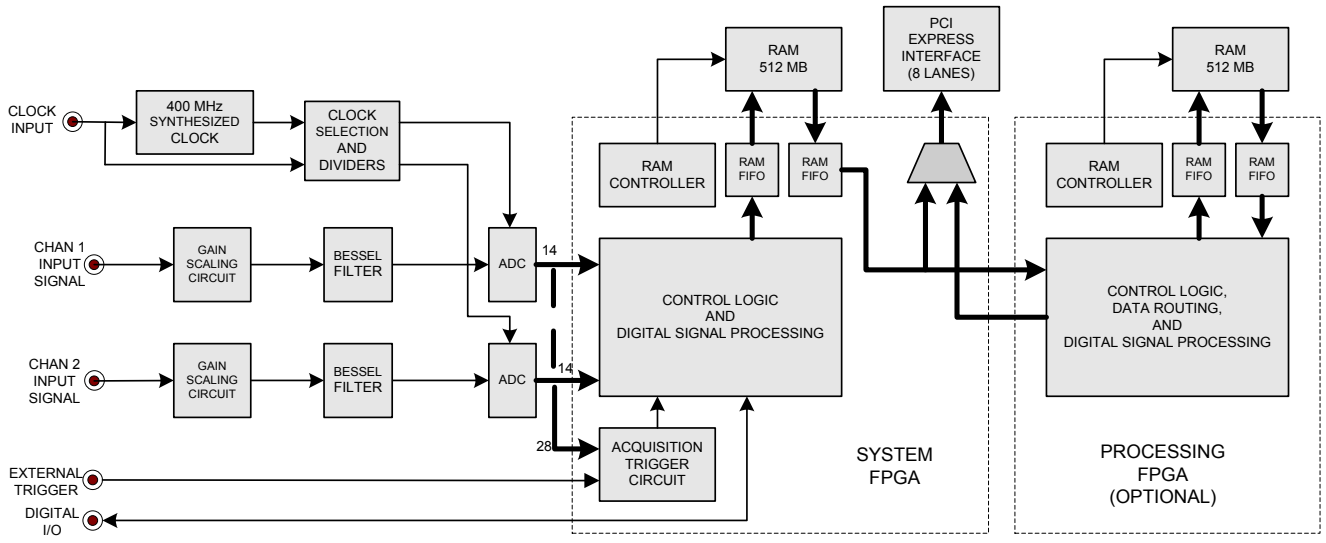
The PX14400D2 also provides an option for an onboard secondary Xilinx Virtex-5 SX50T or SX95T FPGA with its own 512 MB RAM bank for dedicated embedded signal processing. FPGA processing models of the PX14400D include DDC, FFT, and FIR Filter features standard. The processing FPGA is fully end user programmable, allowing for custom developed embedded processing routines.

Up to five PX14400D2 digitizers can be setup for synchronous acquisition operations for a total of 10 input channels by utilizing the separate Signatec SYNC1500 clock/trigger driver source card.

A Windows oscilloscope program, the PX14400 Scope App, allows the operator to view/edit all digitizer hardware settings as well as record and display acquisition data. It is included along with a full complete C SDK for custom application development.

HARDWARE DESCRIPTION

PX14400D2 Functional Block Diagram



Analog Input Front End

The functional block diagram shows a simplified mechanization for the PX14400D2. After input protection and coupling, the input signal is routed through a gain scaling circuit that provides six voltage ranges with full-scale peak-to-peak levels of 200mV, 333mV, 600mV, 1V, 1.6V, and 3V. An installed Bessel filter has a 3-pole Bessel characteristic to give a flat (constant) time delay response over the frequency range and sets the channel bandwidth for the following ranges:

Voltage Range	Bandwidth
200mV	106 MHz
333mV	182 MHz
600mV	239 MHz

Voltage Range	Bandwidth
1V	130 MHz
1.6V	201 MHz
3V	248 MHz

DC Offset control is implemented via 12-bit DACs which inject an offset voltage into the amplifier inputs to effectively cancel any offsets present in the input signal.

ADC data can be captured in dual channel or single channel mode. The onboard memory is not dedicated to a particular channel resource, so in single channel mode the entire signal memory can be used to capture data from channel 1 only or from channel 2 only.

External Inputs/Outputs

Besides the input signal channels, the PX14400D2 also provides SMA connections for a clock input, an external trigger input, and a digital input/output signal. The clock input can be used to supply the source clock for the ADCs or a 10 MHz reference clock for the internal synthesized clock. The digital I/O connector supports output modes of 0V, synchronized trigger, ADC clock divided by 2, or 3.3V and an input mode supporting a digital pulse for timestamp request.

ADC Clock Circuit

An internal synthesized clock is the primary clock source for the ADCs. This synthesized clock on the PX14400D2 allows for users to dial in almost any frequency possible for the onboard ADCs with resulting sampling clock performance that matches or beats most fixed crystal oscillator performance. The synthesizer can generate any frequency from 20 MHz to 400 MHz, except for an un-settable range of 277 MHz to 308 MHz. The ADC clock can also be supplied from the external clock input connector.

If the external clock input is the ADC clock source, it may be divided by any integer value from 1 to 20. For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second post-ADC emulated clock division feature can effectively divide down the clock rate by 1, 2, 4, 8, 16 and 32.

When the synthesized clock is selected, ADC clock jitter is extremely low at about 200 fS RMS. The jitter is independent of the clock divider setting. Clock jitter can reduce the SNR of the captured signal at high frequencies.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied reference clock. The internal reference clock is accurate to better than ±5 PPM. This sets the ADC clock accuracy to also be within ±5 PPM.

Under-Sampling and Anti-Alias Filtering

The PX14400D2 has a maximum digitization rate of 400 MHz which allows for capturing signal frequencies from DC to 248 MHz. Capturing signal frequencies that are more than one-half the sample rate is referred to as Under-Sampling. In this case the digitizer would acquire data in the second Nyquist zone.

Operating in this manner requires that signal frequencies from outside the band not be allowed to reach the ADC. This may involve the application of external band-pass filters to properly reject the out-of-band signals.

To capture a particular frequency band it may be necessary to reduce the ADC clock frequency so as to shift the resulting Nyquist bands to completely capture the desired frequency range. Reducing the sampling frequency will reduce the bandwidth that can be captured.

Operating Modes

The PX14400D2 has the following operating modes:

- **Standby** – Passive mode with no data activity.
- **RAM Acquisition** –Data is captured into onboard RAM.
- **PCIe Transfer** – Transfer data in onboard RAM to the PCIe bus after a completed RAM Acquisition.
- **PCIe Buffered Acquisition** –Data is simultaneously acquired and streamed to the PCIe bus, using onboard RAM as a FIFO.
- **SP PCIe Buffered Acquisition** – Same as PCIe Buffered Acquisition, but with data first routed to optional signal processing FPGA with resulting output data streaming to the PCIe bus.

Of particular interest are the PCIe Buffered Acquisition modes, where the RAM is operated as a large FIFO for acquiring data to the PCIe bus. Data may be put into RAM at a maximum data rate of 1.6 GB/s (2 channels at 400 MHz with 2 bytes per sample for 14-bit data) while also being extracted at this same rate by interleaving write and read data packets, though the transfer to the PCIe interface is limited to 1.4 GB/s maximum. Acquisitions at the full 1.6 GB/s rate is possible when FPGA processing is used resulting in reduced output data with an effective data transfer rate of 1.4 GB/s or less that can be sustained through the PCIe interface.

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. This is a digital input with LVCMOS signal level. Triggering may be set to occur on either the positive or negative going edge of the signal.

Acquisition may also be set to occur based on the amplitude level of either of the two input signals exceeding a programmed trigger level. The triggering threshold is a digital value that is compared against the digitized signal. The detection is edge based with either positive or negative excursion being selectable.

Two triggering modes are available: post trigger or segmented. In post trigger mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. PCIe Buffered Acquisition mode can be combined with either of these trigger modes for creating high-speed continuous (gap-free) or triggered/pulsed based data streaming to the host PC.

Up to five PX14400D2 digitizers can be setup for synchronous acquisition operations for a total of 10 input channels by utilizing the separate Signatec SYNC1500 clock/trigger driver source card. The SYNC1500 provides very precise clock and trigger signals distributed to the connected PX14400D2 digitizers simultaneously. Please refer to the Signatec SYNC1500 product data sheet for further details.

Samples Settings

There are several settings that affect the quantity and method of acquiring samples.

Active Memory Size – The number of samples that will be taken after which the memory will be considered “full” and acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt. The amount of memory that is activated for data acquisition may be set from 8 bytes to the full 512 megabytes in steps of 8 bytes. In PCIe Buffered Acquisition modes it is possible to operate in a “free run” mode whereby streaming data is collected until the digitizer is commanded to terminate the acquisition.

Segment Size – In Segmented Mode, the number of samples that will be taken each time a valid trigger signal is detected.

Pre-trigger Samples – The number of samples that will be recorded into RAM that occurred before the trigger event.

Trigger Delay Samples – The number of samples occurring after the trigger event that will be ignored.

Timestamps

The PX14400D2 can be configured to generate timestamps for certain events. A timestamp is a 64-bit unsigned value that represents a number of clock ticks. Upon transition from Standby operating mode to any acquisition operating mode, the timestamp counter will reset to 0 and increment once per acquisition clock cycle. As timestamps are generated, they are inserted into the Timestamp FIFO. Software can read timestamps from this FIFO as the acquisition progresses or after the acquisition completes. The timestamp mode determines how the PX14400D2 generates timestamps:

Timestamp per segment – Generates a timestamp at the start of each segment acquired while in segmented trigger mode.

Timestamp per external trigger – Generates a timestamp for each pulse received on the external trigger input.

Timestamp per digital IO pulse – Generates a timestamp for each pulse received on the digital I/O connector. This mode is useful if timestamp pulse is independent of the trigger signal, and can be used with GPS cards to correlate absolute time and position to the acquired sample index with the timestamp file.

PCIe Interface

The PX14400D2 implements a PCIe Gen1 x8 lane interface capable of streaming a sustained maximum data transfer rate of 1.4 GB/s with PCIe Buffered Acquisition mode to the host PC for real-time high-speed processing and/or data recordings.

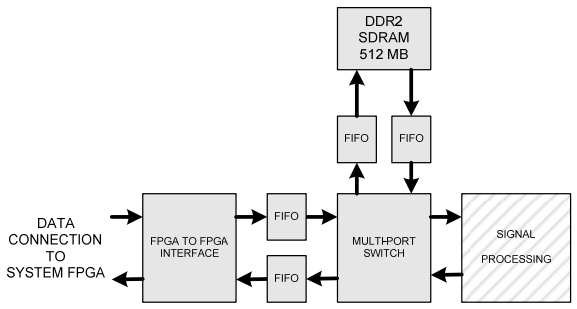
When conducting a sustained continuous or gap free data streaming operation to the host PC without any FPGA processed data reduction, the maximum dual channel sampling rate supported is 350 MHz and the maximum single channel sampling rate supported is 400 MHz.

When conducting a sustained triggered or pulsed data streaming operation to the host PC without any FPGA processed data reduction, the maximum 400 MHz sampling rate for dual or single channel operation is possible as long as the trigger rate and the number of samples per segment acquired produce an effective data transfer rate of 1.4 GB/s or less.

FPGA Signal Processing Option

The FPGA processing model versions of the PX14400D2 feature an onboard secondary Xilinx Virtex-5 SX50T or SX95T FPGA with its own 512 MB RAM bank for dedicated embedded signal processing. The following block diagram shows the data flow within the optionally available signal processing FPGA:

FPGA Signal Processing Block Diagram



When FPGA processing is enabled, acquired data is transferred from the System FPGA to the Signal Processing FPGA where the targeted signal processing routine is conducted. The resulting processed data output is then transferred back to the System FPGA, which can then stream the resulting data to the host PC system via the PCIe interface with PCIe Buffered Acquisition mode.

PX14400D2 FPGA processing models include the following signal processing routines:

Programmable Decimation and Down Conversion (DDC) – This is the default enabled processing feature on PX14400D2 FPGA processing models. It provides decimation processing for single channel mode only with decimation factors of 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, and 8192 for a specified NCO frequency.

Fast Fourier Transform (FFT) – Performs programmable zero padding of the data to 1k or 2k samples, Blackman Harris and Rectangular windowing, 1k or 2k FFTs, optional magnitude square calculation in dB, interleaving of FFT block of data with the raw block of data, and also allows for a programmable window function for single channel mode only.

Finite Impulse Response (FIR) Filtering – Provides programmable FIR filtering for one or two channels with the ability to load filter coefficients from a file source for each channel.

Any of these provided FPGA processing routines can be loaded onto the PX14400D2 with the PX14400 Scope App, which also detects the current loaded processing feature and displays the related interface for making settings that apply to the routine.

Custom FPGA Signal Processing Development

The processing FPGA is fully end user programmable, allowing for customized embedded processing routines to be developed and utilized with the PX14400D2. Signatec provides custom FPGA design services to meet specific application requirements for customers who don't want to program the FPGA themselves. Contact Signatec to discuss specific project requirements, feasibility, and scope for customized solutions.

Alternatively, the optional PX14400 FPGA Development Kit is provided for customers who want to develop their own embedded processing routines.

The Signatec PX14400 FPGA Development Kit requires the end user to have the Xilinx ISE Design Suite software sold directly by Xilinx and provides the native VHDL source code projects of the existing PX14400D2 FPGA processing routines for DDC, FFT, and FIR Filtering. These VHDL source code projects serve to demonstrate how to write real-time embedded signal processing routines for the onboard Xilinx FPGA device with its defined interfaces for utilizing the various FIFO, RAM, processing elements, and bus interface resources.

Purchase of the PX14400 FPGA Development Kit includes up to 5 hours of DynamicSignals engineering support. Additional hours of support can be purchased in units of 5-Hour Block Packages.

There are two PX14400D2 FPGA processing models that provide the following raw FPGA resources:

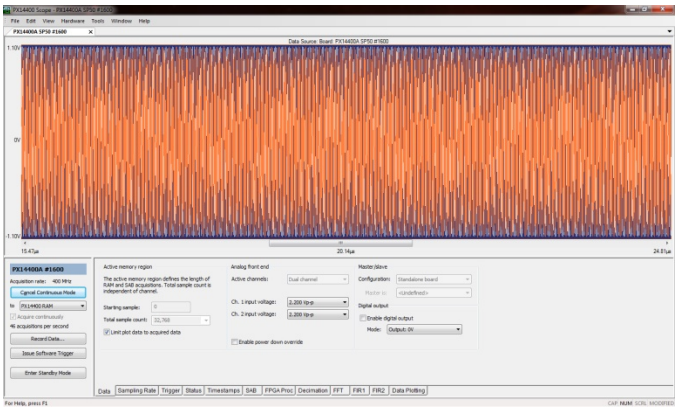
	PX14400D2-SP50	PX14400D2-SP95
FPGA Device	Xilinx Virtex-5 SX50T	Xilinx Virtex-5 SX95T
# of Logic Cells	52,224	94,208
kbits Block RAM	4,752	8,784
# of DSP Slices	288	640

The custom programmable FPGA logic needs to manage two data interfaces: the acquisition data interface and the user register interface. The acquisition data interface provides data from the PX14400D2 acquisition circuits to be processed by the user logic in the programmable FPGA. The register interface provides a way for user defined custom parameters to be dynamically set by the host PC system application.

The PX14400 Scope App includes a generic FPGA Processing interface for enabling FPGA processing and to read/write to specific registers for working with the custom user logic in the FPGA. For custom application software development, standard C functions are provided for interfacing with the FPGA registers.

Developed custom user logic firmware is packaged and uploaded to the PX14400D2 through its PCIe interface to the host PC utilizing the PX14400 Scope App. Alternatively the custom user logic firmware can also be directly loaded through the PX14400D2 JTAG header utilizing a Xilinx JTAG programmer sold directly by Xilinx.

Scope Application



The PX14400 Scope App software is a virtual oscilloscope application that allows the operator to view or edit all digitizer hardware settings as well as record and display acquisition data.

When the Scope App starts, it will automatically connect to all local PX14400 digitizer devices. Note that when the application starts up, the digitizer hardware is not accessed. This allows the Scope App to run without directly affecting any digitizer operations that may be in progress with other software.

The Scope App may be used to modify any of the various hardware settings that affect how the digitizer behaves. These settings are distributed over the tabbed view at the bottom of the main device form. The main interface is divided into three resizable panels.

The top panel is the 'Scope' panel and is used to display digitizer acquisition data, data recording snapshots, and previously recorded data files. The plot area can display multiple channels of independent or interleaved data of varying sample sizes (8-, 12-, 14-, 16-, 32- bit) and types (signed, unsigned, floating point) simultaneously. The default units displayed for the data are time (horizontally) and voltage (vertically), with optional settings for sample number (horizontally) and ADC value (vertically). Plotted data is read-only; there are no facilities to modify data with this interface.

The 'Data Plotting' tab in the Settings area controls many of the data plotting parameters. This includes scaling parameters, channel visibility, and channel source information. In addition, the mouse may be used to alter the horizontal and vertical scaling of the data as well as panning through the data.

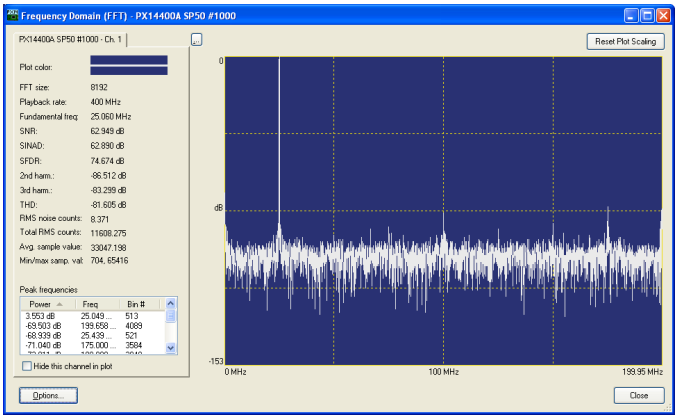
The bottom-left panel is the 'Control' panel and is used to start and stop data acquisitions and recordings. The options on this panel have to do with controlling the digitizer operating mode such as acquire data for a single instance, acquire data continuously, initiate a recording data session, issue software trigger, or enter standby mode.

The bottom-right panel is the 'Settings' panel and is a tabbed view with various tabs that control the various digitizer hardware settings. Certain tabs are only displayed if the underlying digitizer device supports those features. The Scope App allows for saving all digitizer hardware settings to a file that can be opened and applied to the hardware at a later time, thus saving time from manually re-applying settings for repetitive configurations. The tabbed interface settings include:

Data	Settings that control how much data to acquire for RAM acquisitions as well as analog front end settings and digital I/O settings.
Sampling Rate	Settings that affect the digitizer acquisition clock, which defines the sampling rate.
Trigger	Settings that affect the digitizer trigger. These settings relate how data is collected relative to external events.
Status	Contains an interface to read hardware status items with version and configuration information for various hardware, firmware, and software entities displayed.
Timestamps	Settings that affect timestamp modes and operations.
Data Plotting	Settings that affect how data is displayed in the Scope panel. Also provides interface for opening previously saved signal data files into the scope.

Scope App – FFT Analysis

The Scope App has the ability to do FFT analysis on digitizer (or file) data. FFT operations are performed on data sources that are currently displayed in the Scope panel and are displayed on the Frequency Domain (FFT) window.



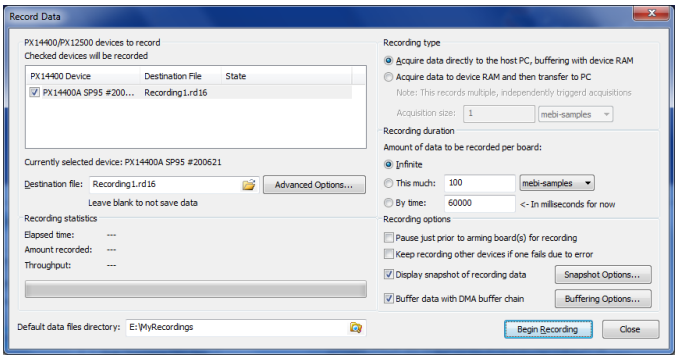
The FFT window is divided up into two regions. The left side is a tab control that contains various FFT and time-domain statistics. There is one tab for each channel of data. The right side contains the frequency domain plots of all channels.

Reported FFT and time-domain statistics include FFT Size, Playback Rate, Fundamental Frequency, SNR, SINAD, SFDR, 2nd Harmonic, 3rd Harmonic, THD, RMS Noise Counts, Total RMS Counts, Average Sample Value, Min/Max Sample Value, and Peak Frequencies.

FFT option settings include changing the FFT size, Windowing method used with options of Rectangular, Hanning, Hamming, and Blackman-Harris, controlling where the source time domain data will be obtained from (beginning of data source, selection on time-domain plot, or from specific given offset into the data source), enabling FFT averaging to average out any ambient noise in the frequency domain with averaged tracked resultant magnitude-squared FFT results shown, enable tracking of peak FFT frequencies, and ignore a specified percentage of noise margin outside of the fundamental frequency.

Scope App –Data Recordings

The Scope App Record Data interface is used to conduct data acquisition recordings.



The Scope App supports two types of data recordings:

Acquire Data Directly to the Host PC, Buffering with device RAM – Used to record one long continuous stream of gap-free data, or one long continuous stream of discrete data segments if in segmented mode (triggered/pulsed based capture), utilizing PCIe Buffered Acquisition mode. This is the most common type of data recording. In this mode the underlying host PC system and targeted data storage location must be able to sustain the acquisition streaming data rate, or a FIFO overflow error condition will occur and the recording stopped. Signatec also provides complete PC signal recording systems that are specifically tailored for real-time data streaming recording applications that require a guaranteed continuous transfer rate with no missing data; please refer to the Signatec Sig-Station and Signal Recording Systems product catalogs for further details

Acquire Data to RAM and then Transfer to PC – Used to record a series of non-contiguous acquisitions with PCIe Transfer mode. First, new data is acquired to RAM and then after the acquisition has completed, the data is transferred to the host system. Note that while data is being transferred to the system, no new data is being acquired. This type of recording is useful in cases where the targeted full acquisition rate may be too fast to support PCIe Buffered Acquisition mode.

The duration of the data recording to be conducted can be set to:

Infinite – Recording goes on indefinitely until manually stopped by the operator or targeted data storage location reaches full capacity.

Data Amount – Records the amount of data specified in total number of gibi-samples, mebi-samples, kibi-samples, or samples. Note: gibi-, mebi-, and kibi- prefixes denote 1073741824 (2^{30}), 1048576 (2^{20}), and 1024 (2^{10}) respectively.

Time – Converts the given total time specified in number of milliseconds into an equivalent sample count (which is a function of acquisition rate) and then records that much data. Note that the time amount specified is the entire time of recorded data, not including the time to wait for a trigger event.

Regardless of the recording duration type selected, a recording may be manually stopped anytime by clicking the 'Stop Recording' button in the Recording window.

Snapshots of the recording data can be displayed in the scope plot area during live recordings. An 8192 point snapshot is obtained roughly once a second by default. The snapshot setting can be modified to specify the desired targeted size in samples and desired targeted frequency in milliseconds.

Recording statistics are displayed during the live recording detailing the current elapsed time, the current amount recorded, and the current total data throughput rate.

There are various destination file data saving options that include: Append Data if it Already Exists, De-Interleave Data into Separate Files, Span Data Over Multiple Statically Size Files, Convert Data to Signed Format before Writing, Leave Room for Application Specific Data, Save Data as Text, and Add Operator Notes to Signatec Recorded Data Context (SRDC) Information.

The native file format for recorded PX14400 acquisition data is the RD16 file format. The RD16 moniker is derived from "Raw Data 16-bit" and is identified by the '.rd16' file extension. RD16 files are raw binary files that contain only acquisition data; there is no file header or additional information in the file. The first two bytes of the file are the first data sample. Samples in .rd16 files are 16-bits in size; however, for recorded 14-bit data, only the lower 14-bits are relevant (the upper two bits will always be zero). By default, multi-channel data is saved in interleaved format (i.e. Ch1, Ch2, Ch1, Ch2, Ch1, Ch2, etc.). Samples are stored in little-endian format; this is the native binary format for the x86 platform.

The simple raw data file format has two big advantages. First, it's very fast to write these files since data is written to the file exactly as it is received from the Signatec digitizer. If the underlying file system (PC host platform and storage destination) can keep up with the data rate, data can be streamed from the digitizer card to the file at the highest streaming recording rate supported. The second advantage is that this file format is very generic which makes it easy for other software to import and utilize the data, such as LabVIEW or MATLAB.

Signatec data samples are unsigned values and the recording RD16 data file can be read as binary data into MATLAB using the "uint16" to import the data as unsigned 16-bit format. Once the data is read into MATLAB, subtract 32768 from each sample value to center the data around 0; as unsigned samples have:

- Maximum possible data sample value: 0xFFFF == 65535
- Midscale sample value: 0x8000 == 32768
- Minimum possible data sample value: 0x0000 == 0

The RD16 file format does not store any context information about the details of the data in the file. Therefore by default the Scope App also generates a Signatec Recorded Data Context (SRDC) file. A SRDC file is a small generated XML-based formatted file that contains information about the associated RD16 data file that includes items such as channel count, input voltage range, sampling rate, source digitizer, operator notes, or any other user-defined data. SRDC files are identified by the '.srdc' file extension and reside in the same storage location of the RD16 file when generated. SRDC files are easily read by any XML-aware software.

The Scope App can be used to open and view previously saved data recording files in the Scope Panel on the "Data Plotting" tab and to view the SRDC contents about the recorded data file.

SOFTWARE DESCRIPTION (Continued) and ATTENUATORS

Software Development Kit for C/C++

Complete documented Application Programming Interfaces (APIs) with C/C++ callable function libraries for the PX14400 are included for custom software development.

In addition, complete fully commented source code for the Scope App is included along with individual project examples that illustrate how to use the function libraries for building custom applications.

Linux Software

The PX14400D2 is also supplied with Linux software that includes:

- Product kernel mode hardware drivers supporting both 32-bit and 64-bit Linux operating systems.
- User Mode Library – Full software C/C++ function library API for custom application development.
- Documented example application C source code projects that demonstrates: RAM acquisition and data transfer, acquisition recording with single device, and placing device into standby mode cancelling all acquisitions and transfers.

PX14400 Linux software is validated with Red Hat Enterprise Linux and Ubuntu Linux distributions. In general, user mode code can typically be ported to other Linux distributions as well.

Optional Software Packages

Optional software packages available for the PX14400 include:

LabVIEW Interface	LabVIEW Interface software includes supplied LabVIEW virtual instruments (VIs) for the PX14400 with full VI reference documentation for use within the LabVIEW environment.

Software Updates

Future software and manual updates are available for download for registered users for the lifetime of the PX14400 product at no additional charge.

Attenuators

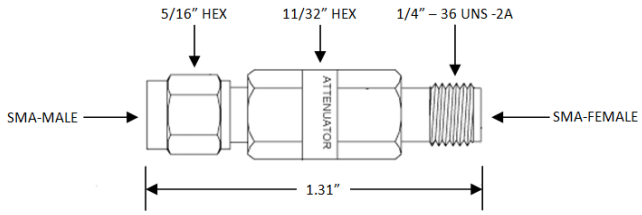
Use the following part number format to order optional SMA attenuators for use with the PX14400D2:

SMA Attenuator Part Number Format: **662-*dB*-1**

Insert the target attenuation value (see table below) in place of ***dB***.

EXAMPLE: **662-6-1** for 6 dB

The attenuator specifications are as follows:



Electrical Specifications					
Avg. Power (Watts)	Peak Power (Watts)	Freq. (GHz)	VSWR (Max)	Attenuation Value (dB)	Attenuation Tolerance
2	500	Hz-2.0 2.0-4.0	1.15:1 1.25:1	3, 6, 10, 20	± 0.6 dB ± 0.8 dB
		Hz-2.0 2.0-4.0	1.25:1 1.35:1	30	± 1.0 dB ± 1.5 dB

Mechanical Specifications	
Connectors	Brass Albaloy Plated
Male Pin	Brass Gold Plate
Female Pin	Beryllium Copper Gold Plate
Housing	Brass Albaloy Plate
Insulator	PTFE Virgin Electrical Grade
Operating Temperature	-67° F to +185° F / -55° C to +85° C
Weight	62 oz / 1.76 kg

PX14400D2 SPECIFICATIONS

External Signal Connections

Analog Input, Channel 1	: SMA
Analog Input, Channel 2	: SMA
Clock Input	: SMA
Trigger Input	: SMA
Digital Input/Output	: SMA

Analog Inputs

Full-Scale Volt. Ranges	: 200mV, 333mV, 600mV, 1V, 1.6V, 3V peak-peak
Impedance	: 50 ohms
Coupling	: DC
Bandwidth	
@ 220mV	: DC to 106 MHz (Bessel filter)
@ 33mV	: DC to 182 MHz (Bessel filter)
@ 600mV	: DC to 239 MHz (Bessel filter)
@ 1V	: DC to 130 MHz (Bessel filter)
@ 1.6V	: DC to 201 MHz (Bessel filter)
@ 3V	: DC to 248 MHz (Bessel filter)

External Trigger

Signal Type	: digital, LVCMOS signal level
Impedance	: >10k ohms
Bandwidth	: 50 MHz

Internal Synthesized Clock

Frequency Range	: 20 MHz to 400 MHz
Un-settable Range	: 277 MHz to 308 MHz
Resolution	: better than ±10 PPM
Accuracy	: better than ±5 PPM

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance	: 50 ohms
Frequency	: 20 MHz to 400 MHz
Amplitude	: 100mV to 2.0V peak-peak
Clock Dividers	: 1 to 20

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32

Reference Clock

Internal	: 10 MHz, ±5 PPM max.
External	: 10 MHz, ±50 PPM max. (required for lock)

Digital Input/Output

Type	: TTL logic level
Max. Frequency	: 200 MHz
Connection	: 50 ohms to FPGA I/O
Output Modes	: 0V, Synchronized Trigger, ADC Clock ÷ 2, 3.3V
Input Modes	: Digital pulse for timestamp request

Trigger Modes

Post Trigger	: single start trigger fills active memory
Segmented	: start trigger for each memory segment

Trigger Options

Pre-trigger Samples	: samples prior to trigger are stored; Single Channel: 8k max.; Dual Channel: 4k max. per channel
Trigger Delay Samples	: delay from trigger to data storage; Up to 64k digitizer clock cycles

Memory

Total Size for Acquisition	: 256 Megasamples (512 MB)
Segment Size	: Up to 128 Megasamples
Segment Re-Arm Time[1]	: 150 nanoseconds
Addressing	: DMA transfer from starting address

Performance (dB)

Dual Channel Operation		Channel 1	Channel 2
SNR	:	64.070	63.881
SINAD	:	62.337	62.364
SFDR	:	69.312	70.221
2nd Harm	:	-69.312	-70.349
3rd Harm	:	-71.459	-71.130
THD	:	-67.213	-67.678

Definition of Terms

SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

SINAD: Signal to Noise and Distortion: The ratio of the fundamental sinusoidal signal power to the total noise and distortion component power. In other words this is the ratio of the fundamental signal power to the measured power from the remainder of the detectable spectrum.

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

2nd Harm: Second Harmonic Distortion: The ratio of the power at twice the fundamental frequency to the power of the fundamental sinusoid.

3rd Harm: Third Harmonic Distortion: The ratio of the power at three times the fundamental frequency to the power of the fundamental sinusoid.

THD: Total Harmonic Distortion: The ratio of the total power of the second and third harmonics to the fundamental sinusoidal power.

Test Method

A filtered 12.0 MHz sine wave signal is applied to the channel 1 and channel 2 inputs. The digitizer clock setting is 400 MHz. The voltage range is 1.6V. Signal amplitude is set for 95% of full scale. Conduct averaging of a 4096 size FFT for 50 acquisition cycles. Performance measurements are made using a 4096 point FFT with a Blackman-Harris window. Signatec uses the first 10 bins to represent the DC term, 34 bins centered around the peak for the fundamental signal power, 9 bins centered at twice the fundamental for the second harmonic and 9 bins centered at three times the fundamental for the third harmonic. All other bins are considered to be noise.

Power Requirements

+3.3V	: 3.3 Amps max.
+12V	: 1.0 Amps max.

Absolute Maximum Ratings

Analog Inputs	: ±4V
Trigger Input	: -0.2V to +4V DC
Clock Input	: 5V peak-peak
Operating Temperature	: +32°F to +122°F / 0°C to 50°C
Storage Temperature	: -4°F to +158°F / -20°C to +70°C
Operating Relative Humidity	: 10% to 90%, non-condensing
Operating Vibration	: 0.25 G, 5 Hz to 500 Hz
Operating Shock	: 2.5 G, 11 ms, ½ sine
Board Dimensions	: 7.5" L x 4.3" H x 0.75" W 190.5 mm L x 109.22 mm H x 19.05 mm W

Notes:

1. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

PX14400D2 ORDERING INFORMATION

Part Number Configuration

The PX14400D2 part number nomenclature for ordering is as follows:

PX14400D2-[***FPGA Option***]**-A-200-**[***Multi-Card SYNC Option***]

[***FPGA Option***], required to select one of the following options**:**

DR = No Onboard Programmable FPGA

SP50 = Onboard Virtex-5 SX50T Programmable FPGA
(52,224 Logic Cells / 4,752 kbits Block RAM / 288 DSP Slices)
Includes DDC, FFT, and FIR Filtering FPGA Routines

SP95 = Onboard Virtex-5 SX95T Programmable FPGA
(94,208 Logic Cells / 8,784 kbits Block RAM / 640 DSP Slices)
Includes DDC, FFT, and FIR Filtering FPGA Routines

[***Multi-Card SYNC Option***], not required – ONLY specify if needed**:**

SY = Planned PX14400D2 Multi-Card Operations with SYNC1500. Requires purchase of separate SYNC1500 card to provide precise simultaneous clock and trigger signal distribution to each connected PX14400D2 digitizer. The SYNC1500 supports up to five connected PX14400D2 digitizers for a total of 10 input channels for synchronous acquisition operations. This option is NOT required for standalone independent operation of multiple PX14400D2 cards.

Part Number Order Examples

The following are some valid part number ordering examples (this listing does not depict all possible configurations):

PX14400D2-DR-A-200 = PX14400D2 with No Programmable FPGA and Gain-Scaling Front End

PX14400D2-SP50-A-200 = PX14400D2 with Programmable SX50T FPGA and Gain-Scaling Front End

PX14400D2-SP95-A-200 = PX14400D2 with Programmable SX95T FPGA and Gain-Scaling Front End

PX14400D2-SP95-A-200-SY = PX14400D2 with Programmable SX95T FPGA and Gain-Scaling Front End and for Multi-Card Synchronous Operation with separate SYNC1500

Documentation & Accessories

The PX14400D2 is supplied with a comprehensive operator's manual distributed with the software, which thoroughly describes the operation of both the hardware and the software. Also supplied are two four-foot coaxial cables with SMA to BNC connectors. Additional cables may be purchased separately. Supplied software contains:

- Windows 32-bit/64-bit Drivers and Scope App Software
- Complete Software Development Kit for C/C++ with Source Code Examples
- Linux 32-bit/64-bit Drivers and Example Projects

Product Warranty

All Signatec products carry a standard full 2-year warranty. During the warranty period, DynamicSignals will repair or replace any defective product at no cost to the customer. Warranties do not cover customer misuse or abuse of the products.

Signatec is a product brand of
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