Electronic Packaging for 5G Microwave and Millimeter Wave Systems

Professional Development Course (PDC)

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Abstract: Electronic packaging at microwave and millimeter wave frequencies is an important capability required for modern communication systems. This is because performance of the systems depends upon successful interconnections between subsystems, components, and parts. Since 5G systems rely on frequency bands approaching 100GHz, special care must be exercised in their design that is not required for 3G/4G systems. Therefore, this professional development course will provide attendees with the knowledge required for interconnects and packaging at the integrated circuit, circuit board, and system level. This includes essential information on materials, fabrication methods, transmission lines, interconnection methods, transitions, components, and integration methods such as 3D packaging. The course will start with specifics on 5G microwave and millimeter-wave communication systems, and major subsystems such as antennas and transmit/receive modules. This will be followed by details of technologies and solutions. The talk will conclude with a short review and predictions on the future directions of packaging technology. At the end of this course, attendees will have practical knowledge about electronic packaging for 5G systems.

• **Speaker Bio:** Dr. Rick Sturdivant is a recognized expert in the fields of electronic packaging and phased arrays. He is author or coeditor of:

  –*RF and Microwave Microelectronics Packaging II* (Springer Publishing, 2017)

  –*Transmit Receive Modules for Radar and Communication Systems* (Artech House, 2015)

  –*Microwave and Millimeter-wave Electronic Packaging* (Artech House, 2013).

• He has also contributed several book chapters, more than 50 journal papers and conference papers, and he holds seven patents from the USA.

• From 1989 to 2000, he engineered transmit receive modules for Hughes/Raytheon where he received the engineering excellence award for developing the world's first tile array module.

• Since the year 2000, he has started several successful technology companies providing solutions for wireless, microwave, millimeter-wave, and high-speed products.

• He is an Assistant Professor at Azusa Pacific University, and Founder and Chief Technology Officer of Microwave Products and Technology, Inc.

• He earned

  –Ph.D., Colorado State University

  –M.A., Biola University

  –M.S.E.E., University of California at Los Angeles

  –B.S.E.E., California State University at Long Beach

  –B.A., Vanguard University

List of Acronyms and Abbreviations

AESA	Active Electronically Scanned Array (type of antenna)
AP	Access Point
APAA	Active Phased Array Antenna
BH	Back Haul
BS	Base Station
FDMA	Frequency Domain Multiple Access
GHz	Giga Hertz (10^9 Hertz)
HPA	High Power Amplifier
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MHz	Mega Hertz (10^6 Hertz)
uWave	Microwave
mmWave	Millimeter-wave
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
PHY	Physical Layer
SDMA	Space Division Multiple Access
SON	Self Organizing Network
T/R	Transmit/Receive
WLAN	Wireless Local Area Network
VGA	Variable Gain Amplifier

Outline

1.0 Introduction
- What Is 5G?
- What Are The Implications For Electronic Packaging Technologies?

2.0 Fundamentals of uWave and mmWave Packaging
- Transmission Lines
- Dispersion
- Package Resonances
- Skin Depth
- Coupling (both beneficial and detrimental)
- Interconnects
- Heat Dissipation

3.0 Materials for 5G Packaging

4.0 Transitions and Interconnects used in uWave and mmWave

5.0 Transmit Receive Modules for 5G

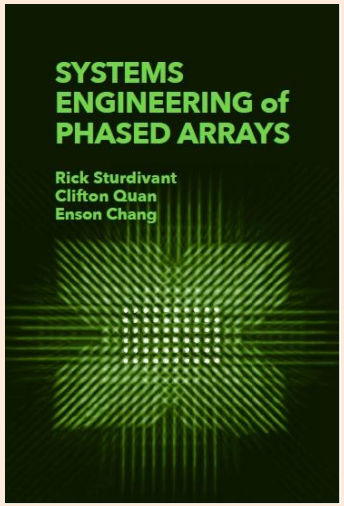
6.0 Heat Transfer for uWave and Millimeter-wave

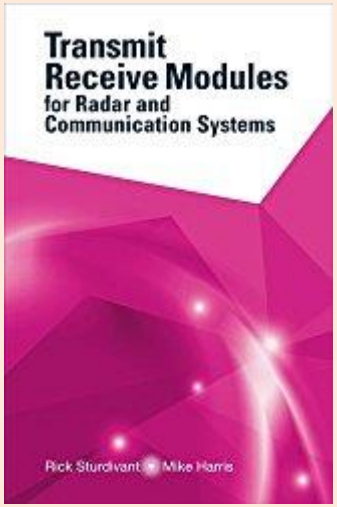
7.0 Phased Arrays for 5G

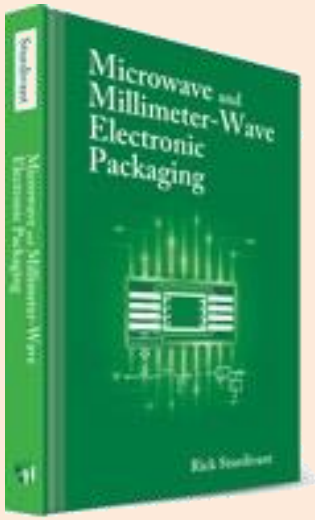
8.0 Conclusions

Content Of This Briefing Is Based Upon Three Books

- R. Sturdivant, *Microwave and Millimeter-wave Electronic Packaging* (Artech House, 2014).
- R. Sturdivant, M. Harris, *Transmit Receive Modules For Radar and Communication Systems* (Artech House, 2015)
- R. Sturdivant, C. Quan, E. Chang, *Systems Engineering of Phased Arrays* (Artech House, Expected Nov. 30, 2018).







Section 1.0: Introduction

1.1 Section Introduction
- What is 5G?
- Global Standards
- The IoT Impact

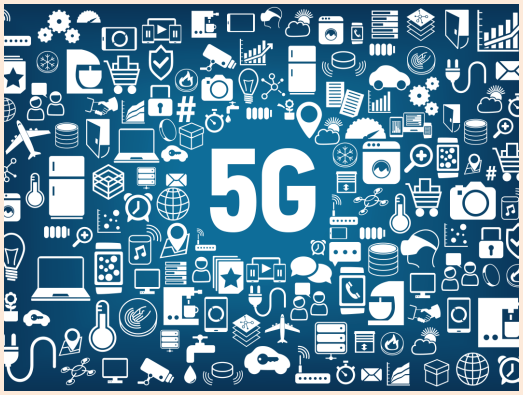
1.2 5G Physical Layer Architecture Assumptions
- What Is A Steerable Antenna
- 5G Use Cases
- 5G Relies Heavily On mmWave
- Benefits of Space Division Multiple Access

1.3 Implications For Electronic Packaging
- Physical Layer Electronic Components and Systems
- What Does This Mean For Electronic Packaging of 5G Systems

1.4 Section Conclusions

What is 5G?

- A system that will provide “1000 times increase in wireless capacity serving over 7 billion people (while connecting 7 trillion “things”), save 90% of energy per service provided, and create a secure, reliable and dependable Internet with zero perceived downtime for services.” [1]
- Simplified Two Part Definition
  - A set of various access hardware technologies and frequency bands
  - Built in computing intelligence that handles data very efficiently



[1] 5G Infrastructure PPP, The European Commission.

Global 5G Standards Activities

- Europe: 5G Public Private Partnership (5G-PPP)
  - European commission and private industry
- China: 5G Promotion Group (IMT-2020)
  - Strategy, vision, requirements. Research MOST 863-5G
- South Korea: 5G Forum
  - A public/private partnership for a national 5G strategy
- Japan: ARIB 2020 and Beyond Ad Hoc
  - Released: “5G Mobile and Wireless Communications Technology (2014)”

5G PPP
The 5G Infrastructure Public Private Partnership

IMT-2020

5G Forum

ARIB

5G Use Cases

- Mobile Broad Band Access
  - Even in crowded areas
  - In public transportation
  - High quality of services even in challenging network conditions
- Media Everywhere
  - Live TV at scale
  - On demand anything media
  - Mobile for in-home TV
- Remote Devices
  - Remote control of heavy machines
  - Factory automation and process control/monitoring
  - Smart grids
- Human and IoT Interaction
  - Immersive augmented reality
  - Immersive gaming
  - Surveillance
  - Smart houses
- Transportation
  - Smart Infrastructure
  - Connected Bus-Stops
  - Connected Trucks
  - Connected Cars
- Medical Devices
  - Real time health services
  - Remote monitoring

[4] 5G Use Cases, *Ericsson.*

Impact of IoT On 5G May Be Significant

Number of IoT Patents By Company

Source: lex-innova.com, INTERNET OF THINGS - 2016

- Characteristics
  - –Low data rates at each sensor
  - –Large Numbers of Devices
  - –Sensors
- Overall Data Requirement
  - –My estimates are that IoT devices will generate as much as 1 exabit (10^{18} bits ~ 10^{17} bytes) of data per year by 2020.
  - –A Brookings Institute Report has a much larger estimate at 44 zettabytes (10^{21} bytes) of data annually by the year 2020.
  - **–That's 10^{17} to 10^{21} bytes of data every year!**

Source: D.M. West, "How 5G technology enables the health internet of things," Report from: Brookings Institute: Center for Technology Innovation, July 2016

Key Physical Layer Items: mmWave Spectrum and Steerable Antennas

- Spectrum For 5G (highly dependent upon regulations for each country)

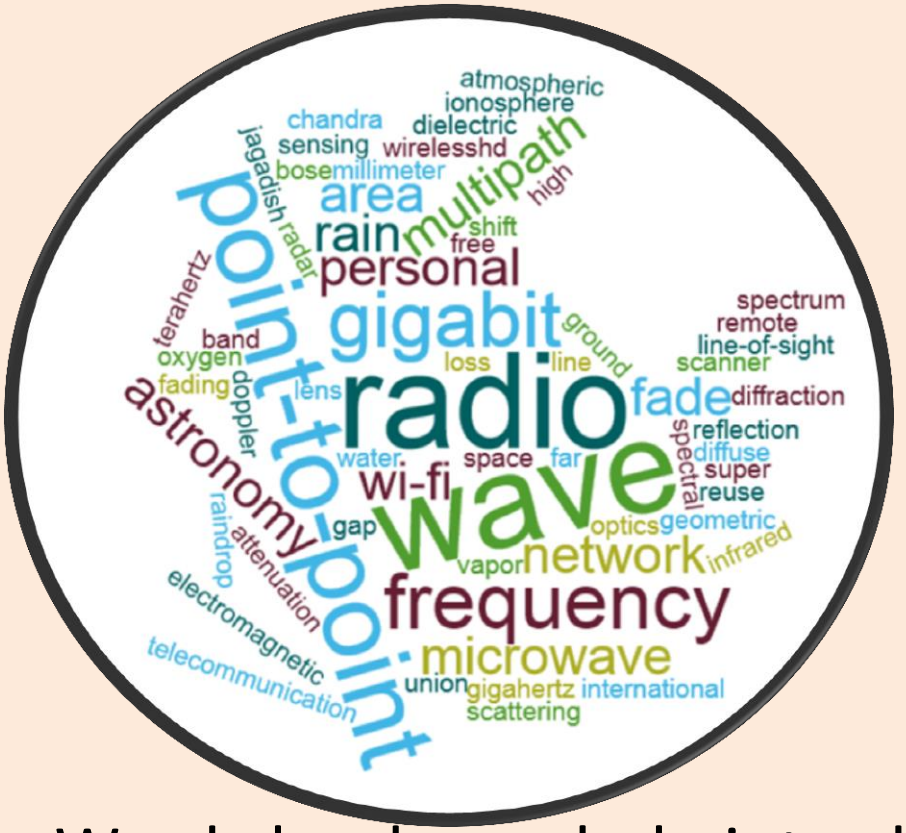
Parameter	4G LTE	5G Sub 6GHz	5G Low mmWave	5G High mmWave
Carrier Frequency	2GHz	< 6GHz	20-40 GHz	57-95 GHz (various bands)

For example, the FCC (USA) licenses 27.5-28.35GHz, 37-38.6GHz, 38.6-40GHz and other High mmWave bands

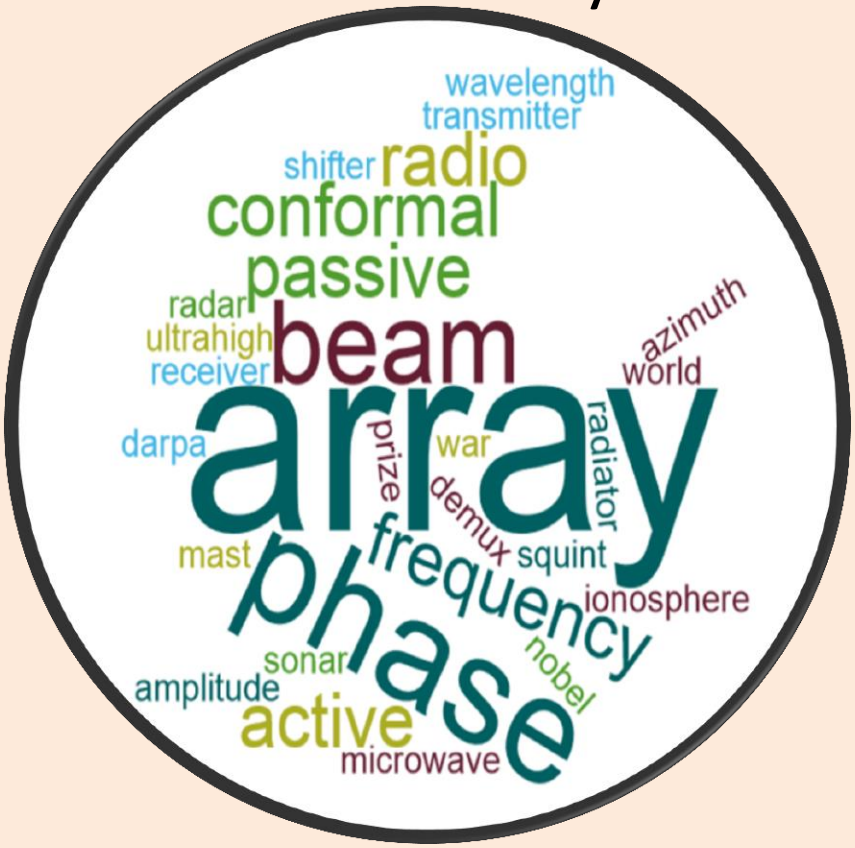
- Phased array antennas allow for SDMA

Two Critical Enabling Technologies For 5G Physical Layer

Millimeter-Wave



Phased Arrays

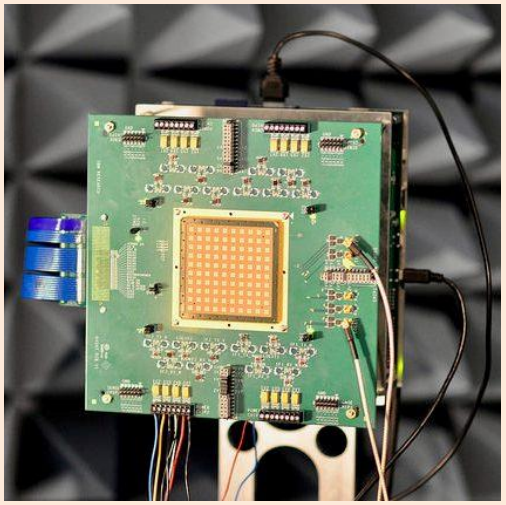


- Word clouds can help introduce some of the terminology used for these technologies

5G Physical Layer System Architecture Assumptions

- Utilizes Existing Mobile Infrastructure Below 6G
  - Existing 4G LTE in 2GHz and below frequency range
- Uses New Mobile Infrastructure Below 6GHz
  - Including below 2GHz and 3.5GHz
- Relies Upon Millimeter-wave Spectrum
  - In the 30GHz and 70GHz range
- Physical Layer Uses Phased Arrays

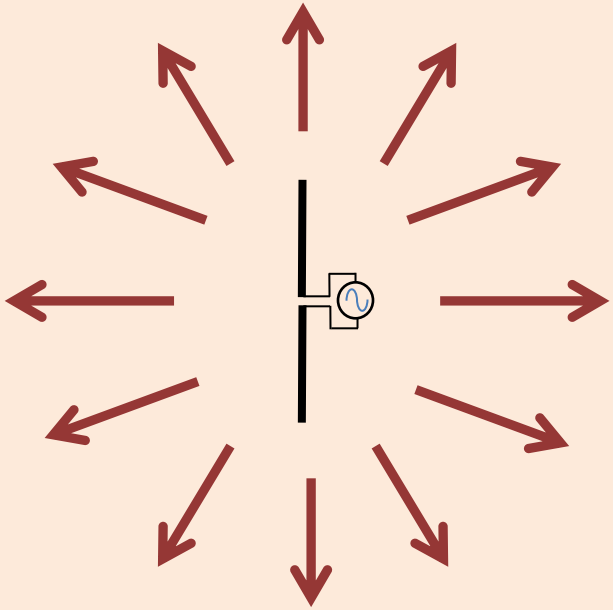
"We assume backhaul and access links share the same air interface, and all network elements (including BS, APs and UEs) are equipped with directional steerable antennas and can direct their beams in specific directions." [2]



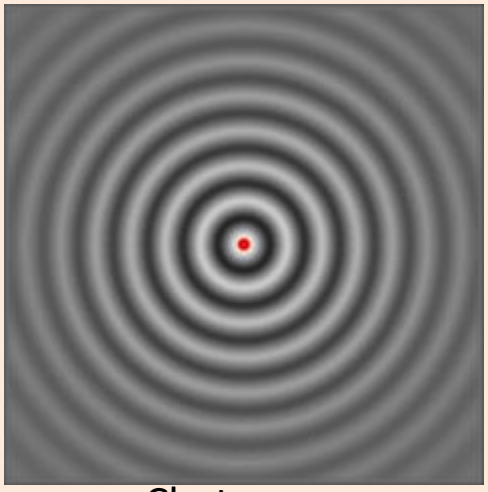
28GHz Silicon Based Phased Array [3]. Often called an AESA or APAA

[2] 5G PPP Architecture Working Group, *View on 5G Architecture (Version 2.0)*, July 18, 2017.
[3] "IBM and Ericsson Announce 5G mmWave Phased Array Antenna Module", *Microwave Journal*, Feb 2017.

What Is An Isotropic Antenna?



An Isotropic Antenna Radiates Energy Equally In All Spatial Directions



Chetvorno

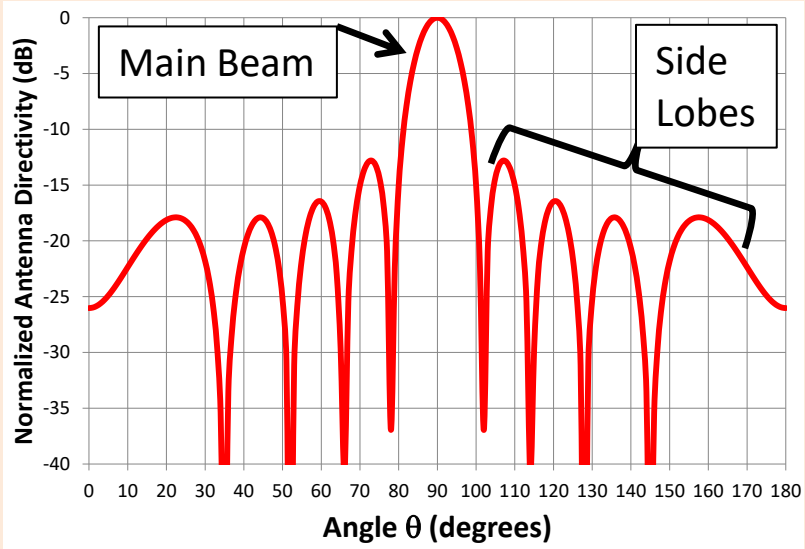
Animation Of An Isotropic Antenna

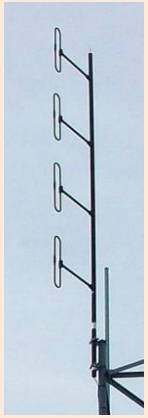
Isotropic Antenna

- An ideal antenna that radiates its power equally in all directions in 3D space.
- Used as a frame of reference for the gain of antennas.

Arrays Of Antennas Concentrate Radiated Energy In Desired Spatial Directions

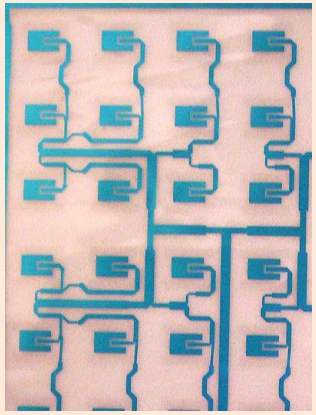
- Energy from the antenna elements and adds constructively in the broadside direction.
- Energy adds destructively in other directions.



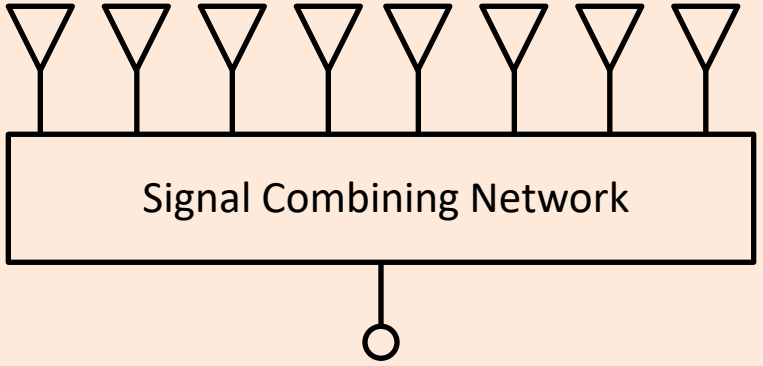


Milonica

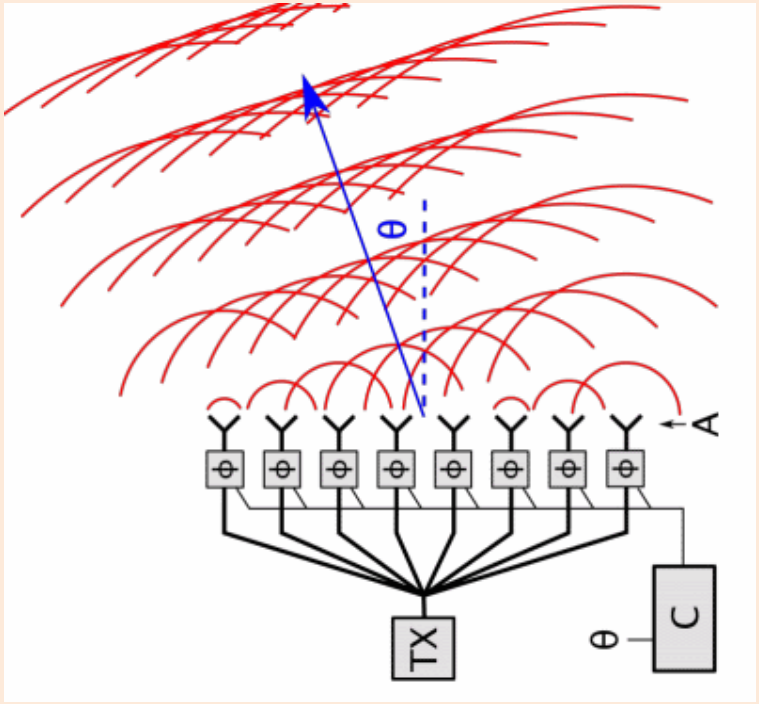
Vitaly V. Kuzmin



Ulfbastel



If Phase Shifters Are Added To Each Antenna Element In The Array, Then The Antenna Beam Can Be Steered



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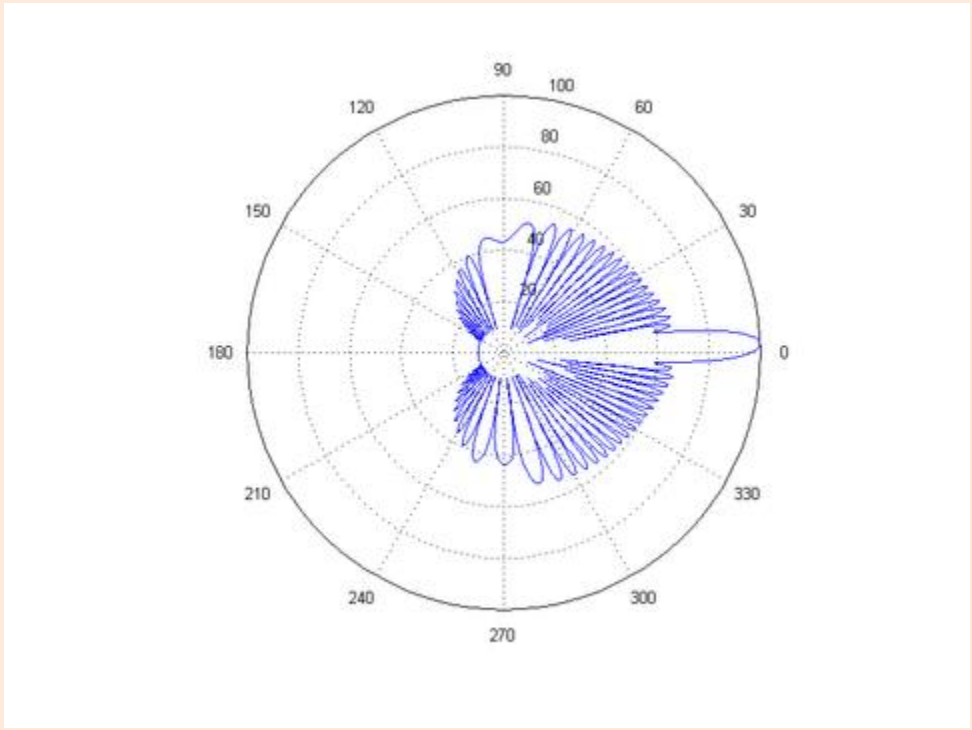
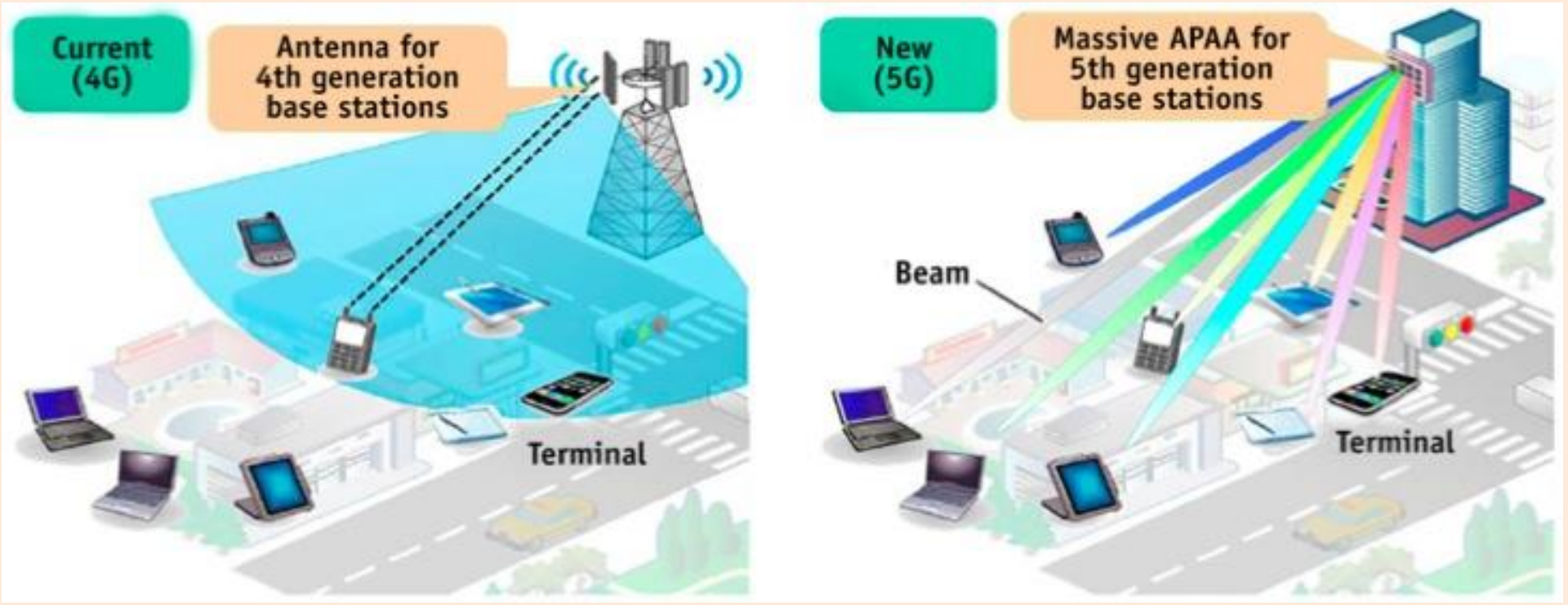
Phased Array: Radiates energy in preferential directions



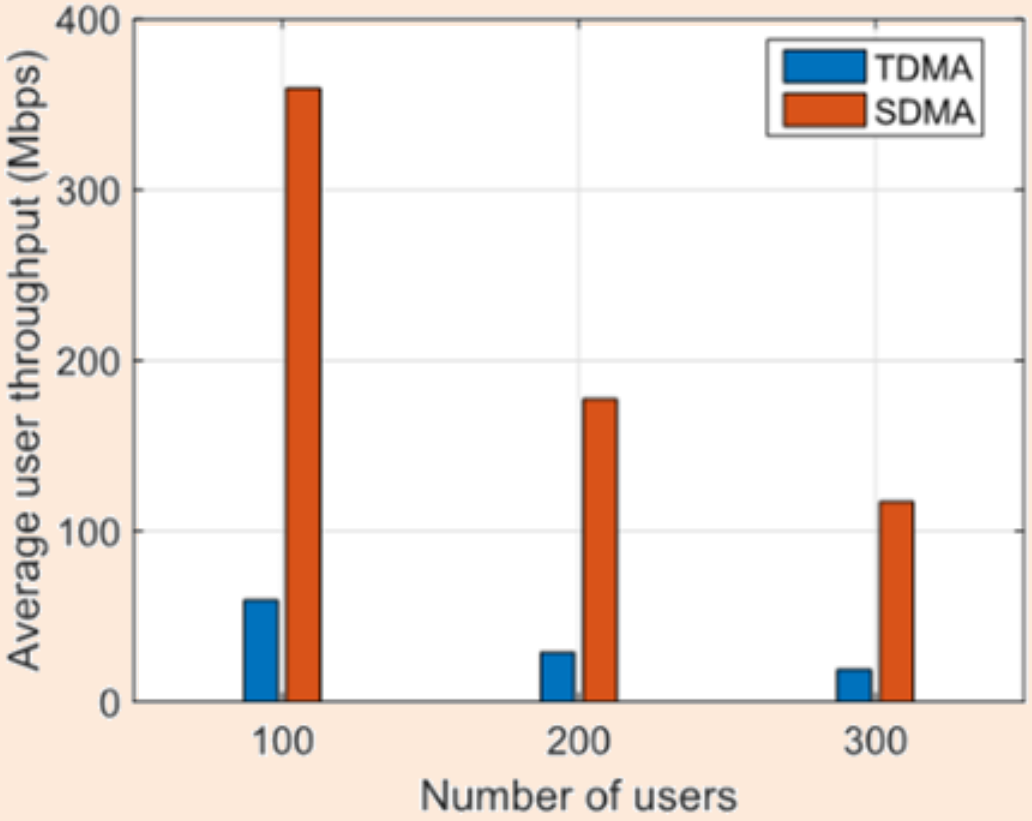
Maxter315

5G Systems Will Rely Heavily Upon Phased Arrays



http://www.iebmedia.com/index.php?id=11369&parentid=63&themeid=255&hft=92&showdetail=true&bb=1

Benefit Of 5G SDMA

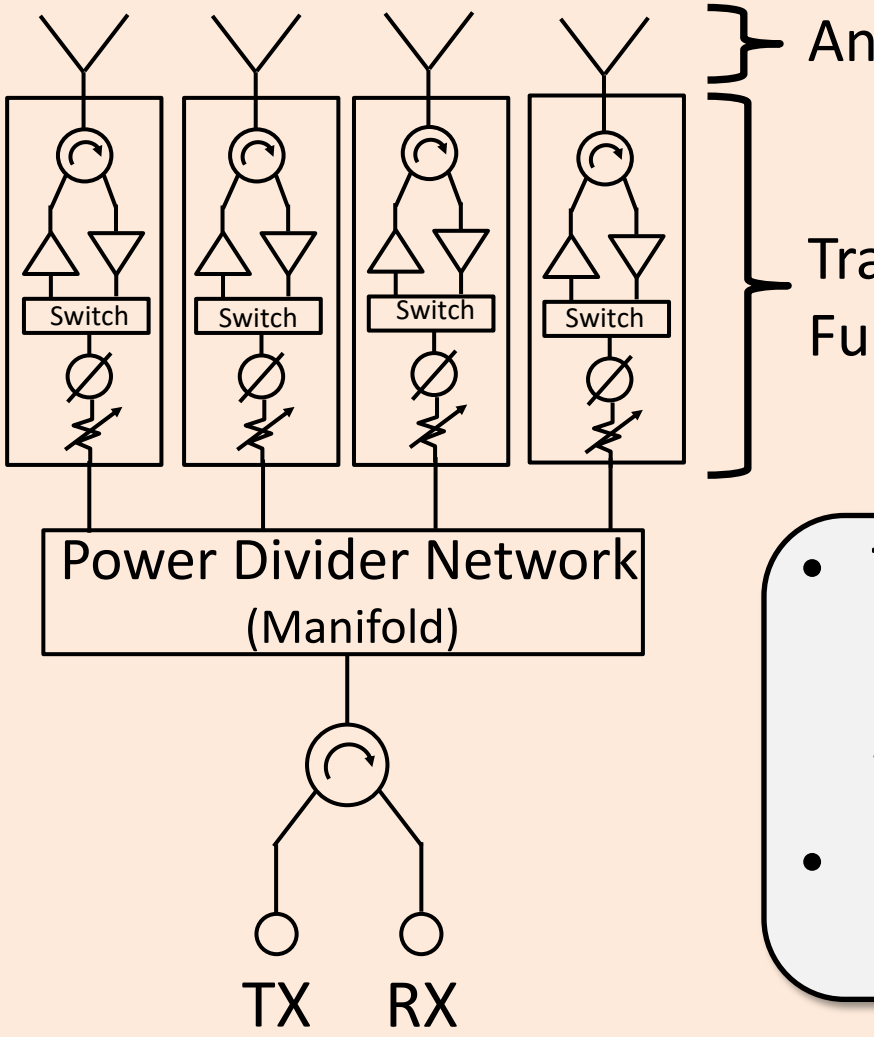


Comparison of user throughput for 28GHz band with 1GHz of available bandwidth [2]

Space Division Multiple Access (SDMA) uses information about user location to steer the antenna beam to communicate with users.

[2] 5G PPP Architecture Working Group, *View on 5G Architecture (Version 2.0)*, July 18, 2017.

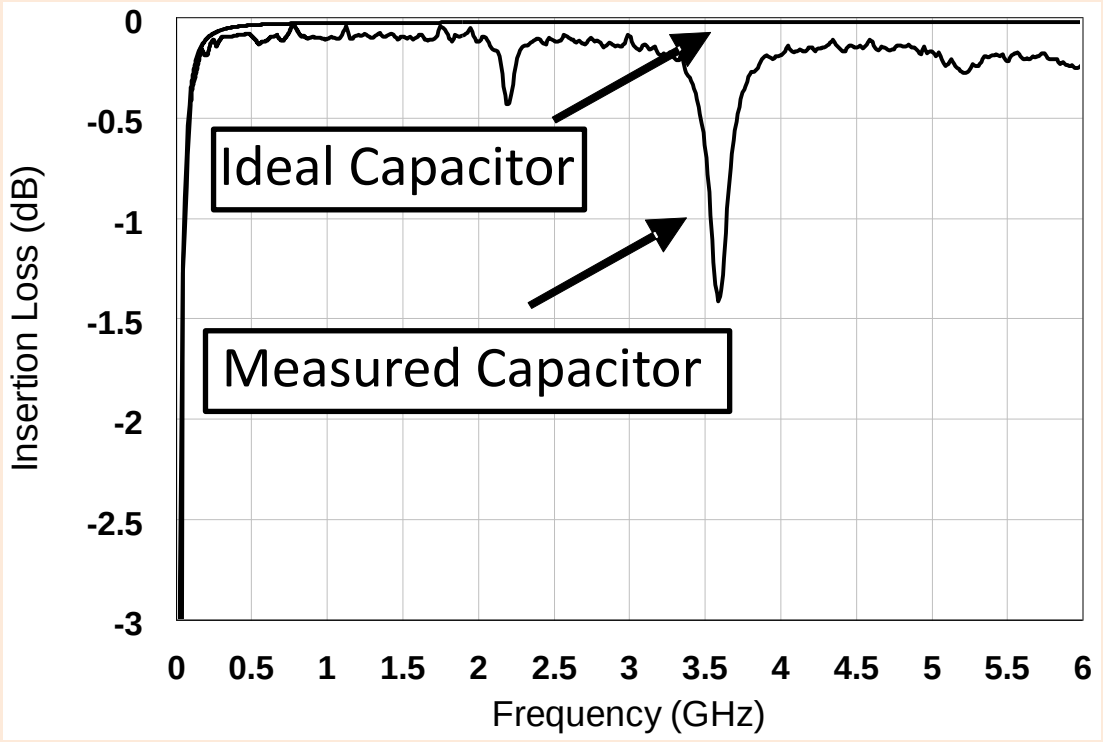
Active Electronically Scanned Array (AESA) Rely

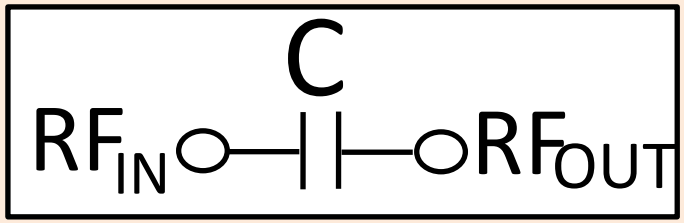


- Transmit Receive (T/R) Functionality Exists At Each Element Or Multiple Elements Within The Array
- Enables the antenna beam to be steered

What Does All This Mean For Electronic Packaging for 5G Systems?

A significant portion of 5G electronic packaging will be done at millimeter-wave frequencies.

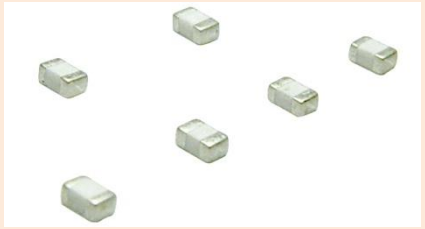




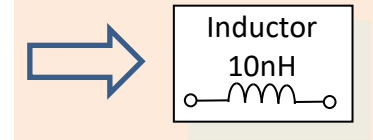
Example Of Distributed Effects On Lumped Elements

- For a lumped element inductor, the bandwidth over which it “looks” like an inductor is only a few GHz.
- Begins to deviate from an ideal inductor after about 1.2GHz

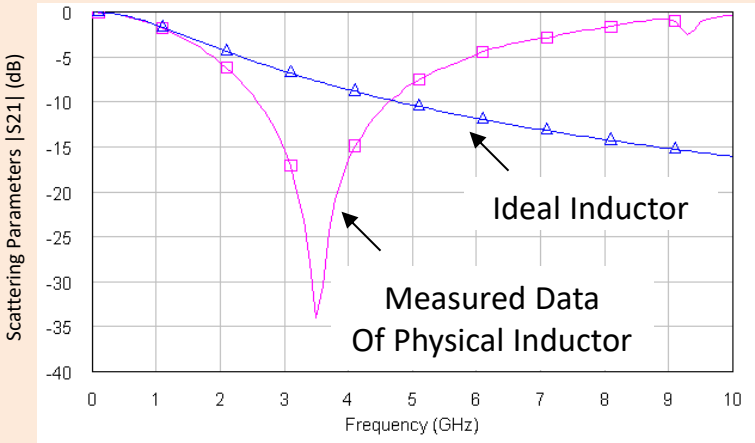
Physical Samples Of Inductors



Ideal Electrical Model



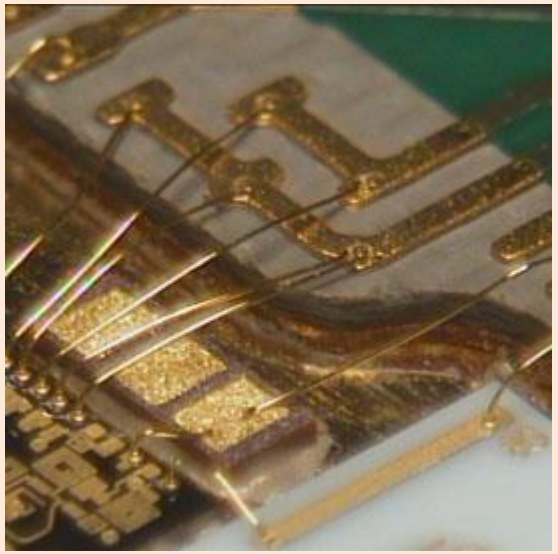
Comparison of Measured Data For A Lumped Inductor with Ideal Performance



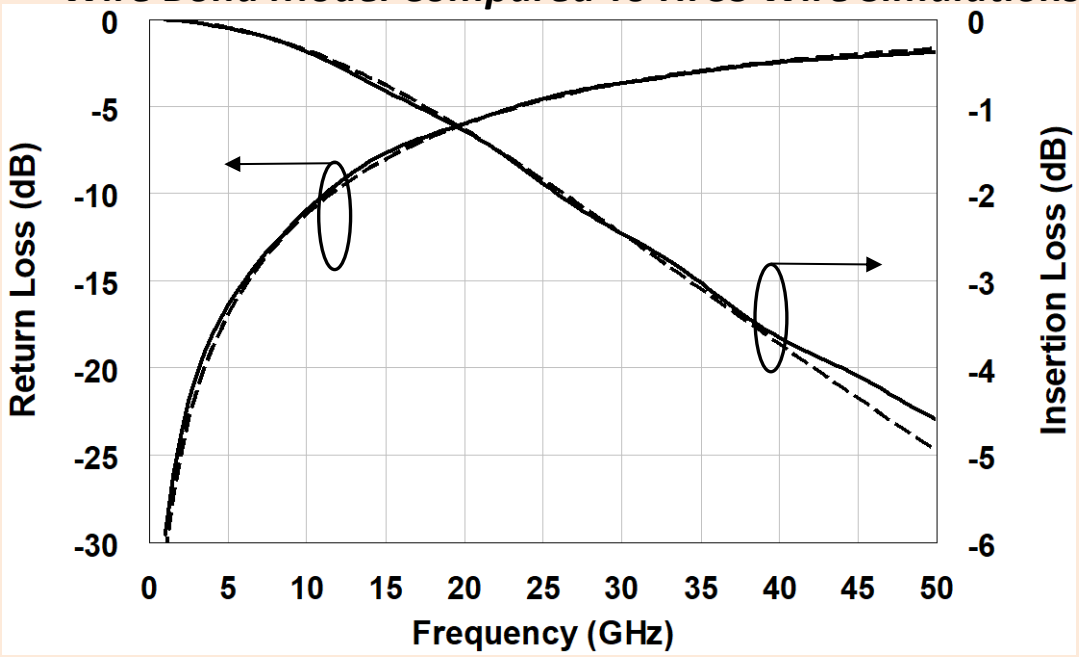
Measured Inductor
Johanson 0805 case
P/N L_15C10N_SER

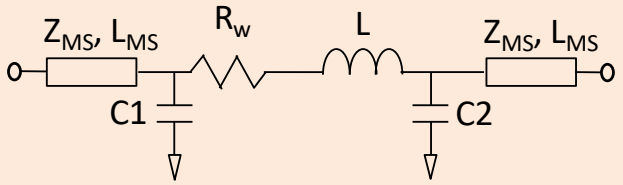
At Millimeter-wave, Physical Size of Components and Interconnects Are Comparable To A Wavelength

@ 71 GHz
Free Space Wavelength = 4.2mm
Wavelength In RO4003 = 2.2mm



Wire Bond Model Compared To HFSS Wire Simulations





mmWave Wire Bond Model

R. Sturdivant, "Broadband Electrical Modeling of Transitions and Interconnects Useful for PCB and Co-fired Ceramic Packaging," Presented at *2014 IMAPS RaMP Conference*, San Diego, CA.

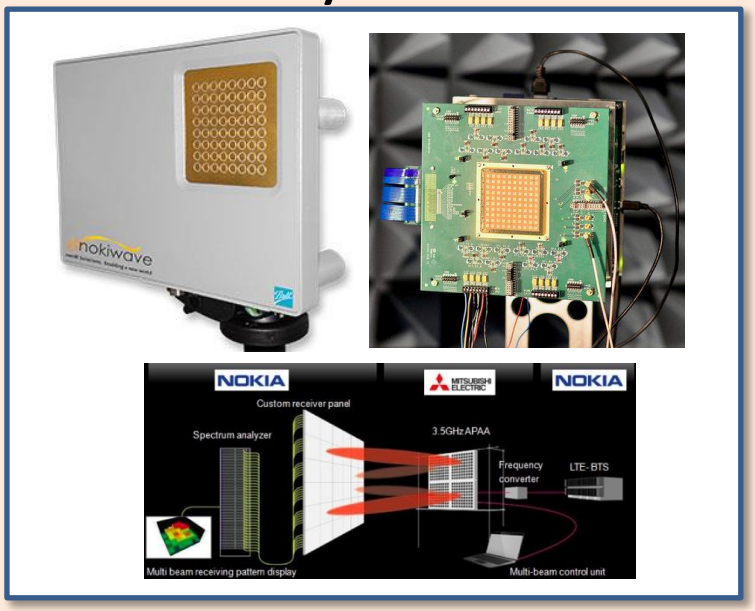
What Does All This Mean For Electronic Packaging for 5G Systems? (Continued)

5G electronic packaging will involve highly integrated solutions.

3G / 4G Systems

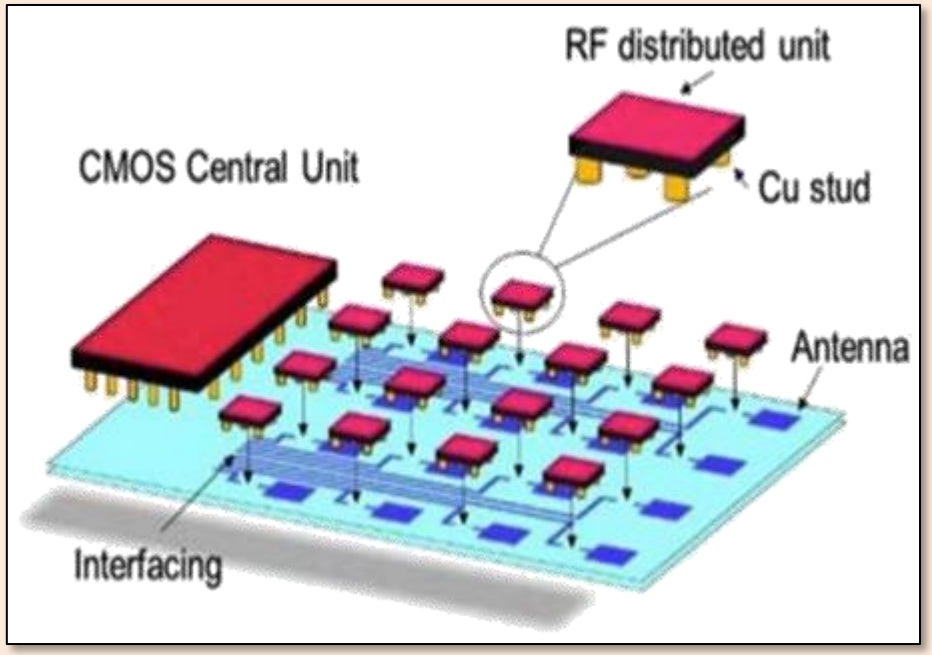
Antennas Are Separate Components That Are Separately Packaged

5G Systems



Antennas And Beam Steering Electronics Are Packaged Together

Highly Integrated Packaging Creates Additional Design Issues



- Electrical Signal Coupling
- Package Resonances
- Power dissipation and heat transfer
- High performance interconnects
- Materials compatibility

The same concerns that many packaging engineers have been dealing with, but with greater challenges

R. Jos, "Managing power dissipation in 5G design," MWee, June 13, 2016

Challenges of Packaging for 5G Add A Layer Of Complexity

Normal IC Packaging Issues

- Choose compatible materials for reliability
- Die attach method and interconnect method
- Metal system
- Sealing and die encapsulation

Additional Issues When Developing Packaging for 5G

- Design of the metal pattern and dielectric thickness to maintain 50 ohms
- Short interconnect lengths to minimize reflections.
- Careful material selection to minimize effect on electromagnetic fields in integrated circuits and packaging
- Coupling between traces, package resonance
- RF devices often have high dissipated power density

Section 1: Conclusions

- 5G Promises Significant Increases In Access
- 5G Physical Layer Leverages Two Main Items
  - Additional Spectrum at mmWave Frequencies
  - Phased Array Antennas
- The challenge of packaging at microwave and millimeter wave frequencies for 5G
  - Components and interconnects are large compared to a wavelength
  - Integration of 5G solutions is much more complex

Section 2: Fundamentals Of 5G Packaging

2.1 Transmission Lines

2.2 Dispersion

2.3 Package Resonances

2.4 Skin Depth

2.5 Coupling (both beneficial and detrimental)

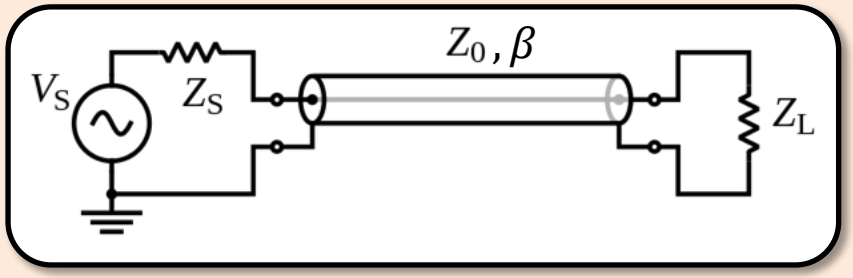
2.6 Interconnects

2.7 Heat Dissipation

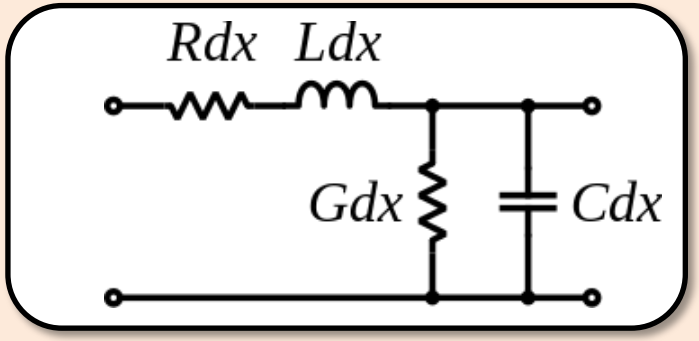
Section 2.1 Transmission Lines
Transmission Line Theory

- Transmission lines are used to carry alternating current signals such as radio frequency signals.

Schematic Of Transmission Line



Equivalent Model



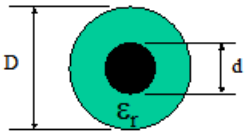
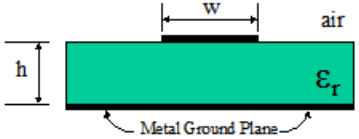
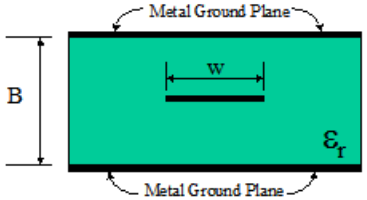
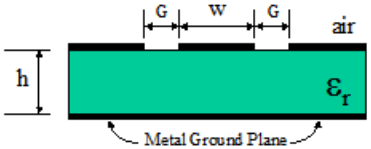
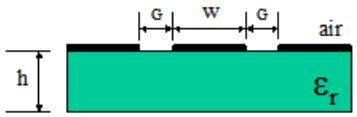
Coax Is A Familiar Transmission Line Type

$$\text{Line Impedance} = Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tilde{=} \sqrt{\frac{L}{C}}$$

If Losses Are Ignored

$$\text{Propagation Constant} = \beta = \frac{2\pi}{\lambda}$$

$$\lambda = \frac{v}{f} = \frac{c/\sqrt{\epsilon_r}}{f}$$

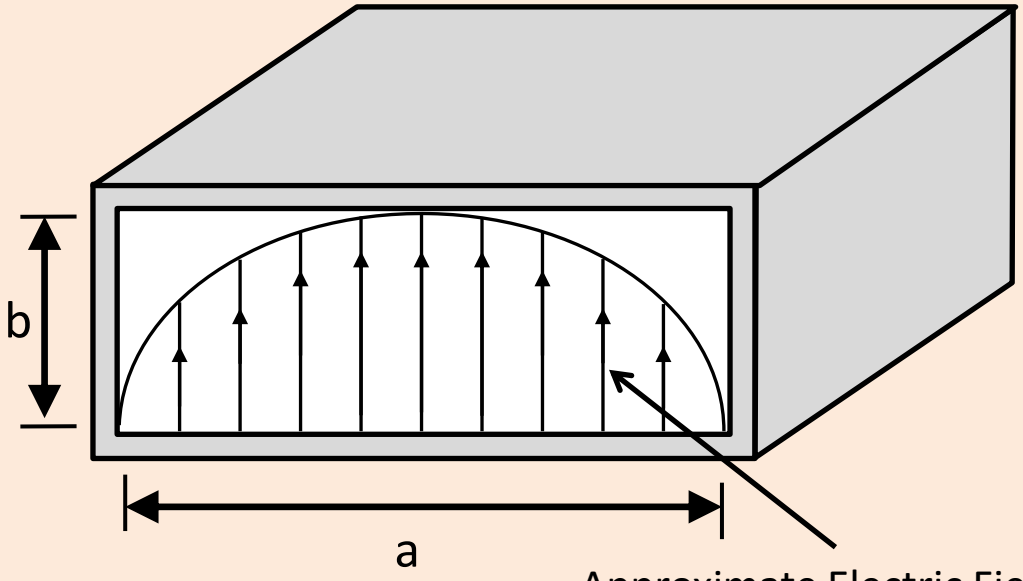
Transmission Line Type	Benefits	Drawbacks	Typical Uses
 Coax	1. Good isolation due to the external ground shield. 2. Low dispersion. 3. Wide band.	1. Difficult access to the signal line due to ground shield. 2. Physically large	1. TV and cable signal. 2. Lab testing. 3. Instrumentation.
 Microstrip	1. Physically small. 2. Low cost and ease of manufacturing. 3. Large industry base of compatible circuits and components. 4. Easy access to signal line.	1. Low isolation. 2. Higher dispersion. 3. Higher order mode propagation is MMW frequencies.	1. Printed circuit boards. 2. Microwave hybrids. 3. Antennas 4. Passive circuits and components. 5. MMICs
 Stripline	1. Low cost and ease of manufacturing. 2. No dispersion. 3. Physically small. 4. Low radiation and can be low coupling.	1. Difficult access to signal line. 2. Higher order mode propagation.	1. Buried signals in PWB and ceramic packages. 2. Signal distribution. 3. Couplers and other components.
 Coplanar Waveguide With Ground	1. Physically small. 2. Low cost and ease of manufacturing. 3. Large industry base of compatible circuits and components. 4. Easy access to signal line. 5. Lower dispersion.	1. Prone to higher order propagation modes and resonances. Requires careful via placement.	1. Printed circuit boards. 2. Microwave hybrids. 3. Antennas 4. MMICs
 Coplanar Waveguide	1. Physically small. 2. Low cost and ease of manufacturing. 3. Easy access to signal line. 4. Low dispersion.	1. Requires connection of grounds at discontinuities.	1. Antennas. 2. Suspended substrate circuits and components. 3. MMICs.

When Operating at Microwave and especially Millimeter-wave Frequencies, Special Care Must Be Taken To Avoid Higher Order Mode Propagation.

Therefore, the following slides will discuss how to design transmission lines taking into account higher order mode propagation.

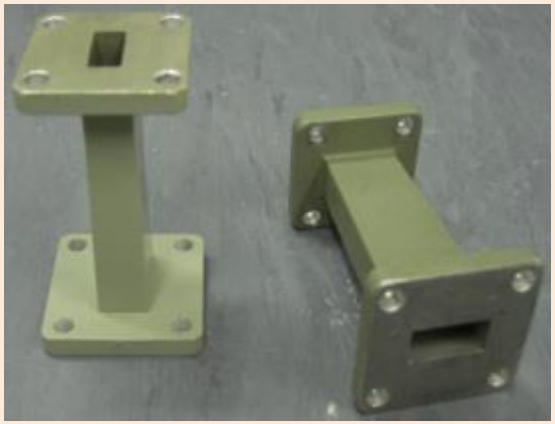
Adapted From: R. Sturdivant, "Fundamentals of packaging at microwave and millimeter-wave frequencies," Chapter 1 of *RF and Microwave Microelectronics Packaging (Springer, 2010)*

Waveguide Transmission Line



Approximate Electric Field Distribution For TE_{10} Mode

- Waveguide is commonly used in mmW systems.
- Normally, the goal is to have single mode propagation.
- Therefore, the TE_{10} mode is selected as the mode for the transmission line.



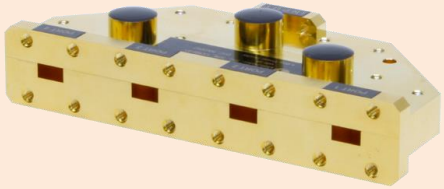
$$(F_c)_{mn} = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2}$$

$$(F_c)_{10} = \frac{1}{2a\sqrt{\mu_0\varepsilon_0}} = \frac{c}{2a}$$

Where:
μ = permeability in the waveguide
ε= permittivity in the waveguide
c = speed of light = $3x10^8$ m/s

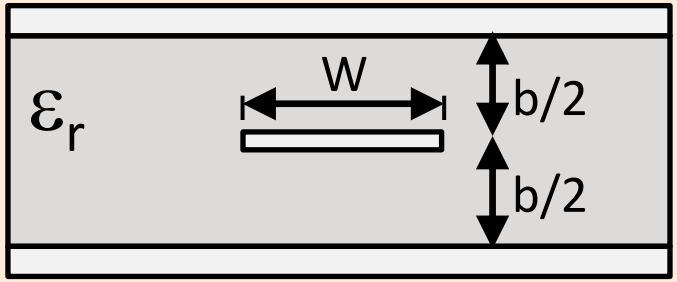
Table Of Common Waveguide Sizes

Name	Frequency Range	Cutoff Freq, Fc	Dimension a inch(mm)	Dimension b inch(mm)
WR75	10.00 to 15 GHz	7.869 GHz	0.75 [19.05]	0.375 [9.525]
WR62	12.40 to 18 GHz	9.488 GHz	0.622 [15.7988]	0.311 [7.8994]
WR51	15.00 to 22 GHz	11.572 GHz	0.51 [12.954]	0.255 [6.477]
WR42	18.00 to 26.50 GHz	14.051 GHz	0.42 [10.668]	0.17 [4.318]
WR34	22.00 to 33 GHz	17.357 GHz	0.34 [8.636]	0.17 [4.318]
WR28	26.50 to 40 GHz	21.077 GHz	0.28 [7.112]	0.14 [3.556]
WR22	33.00 to 50 GHz	26.346 GHz	0.224 [5.6896]	0.112 [2.8448]
WR19	40.00 to 60 GHz	31.391 GHz	0.188 [4.7752]	0.094 [2.3876]
WR15	50.00 to 75 GHz	39.875 GHz	0.148 [3.7592]	0.074 [1.8796]
WR12	60 to 90 GHz	48.373 GHz	0.122 [3.0988]	0.061 [1.5494]
WR10	75 to 110 GHz	59.015 GHz	0.1 [2.54]	0.05 [1.27]
WR8	90 to 140 GHz	73.768 GHz	0.08 [2.032]	0.04 [1.016]
WR6	110 to 170 GHz	90.791 GHz	0.065 [1.651]	0.0325 [0.8255]
WR7	110 to 170 GHz	90.791 GHz	0.065 [1.651]	0.0325 [0.8255]
WR5	140 to 220 GHz	115.714 GHz	0.051 [1.2954]	0.0255 [0.6477]

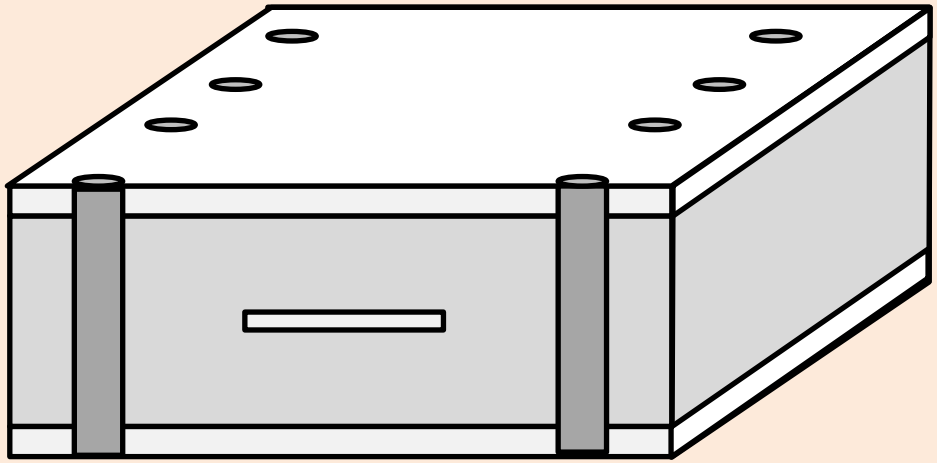


Millimeter-wave components using waveguide from Sage Millimeter
www.sagemillimeter.com

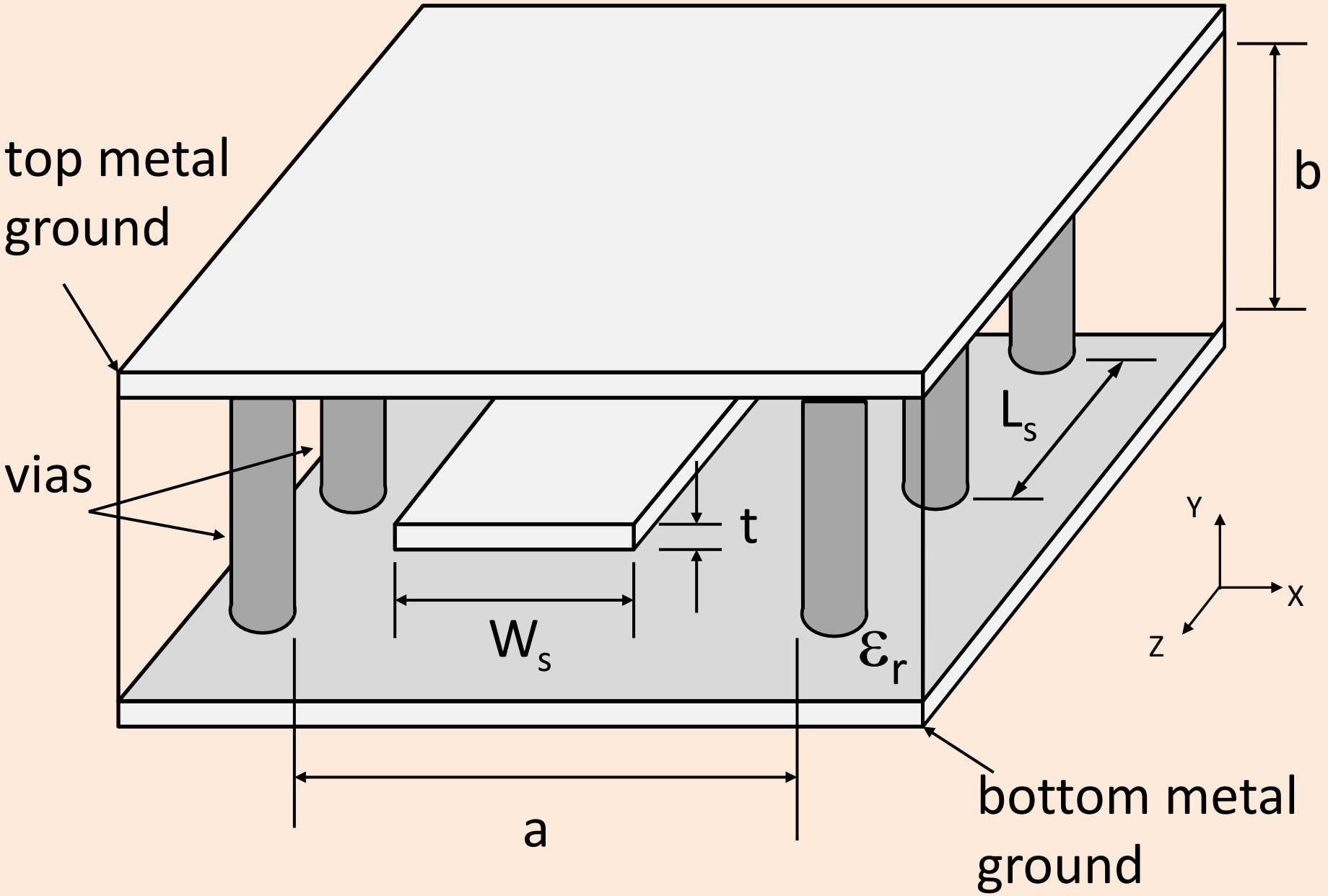
Design Equation For Stripline And Common Implementation With Vias



$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi W\left(0.8+\frac{t}{W}\right)}\right]$$

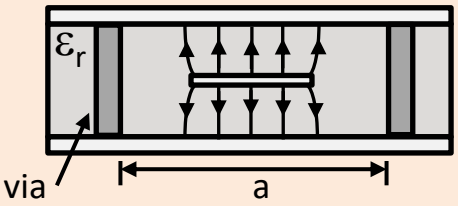


- The vias suppress the undesired waveguide mode that can propagate in the stripline.


top metal
ground
vias
b
L_s
t
W_s
ε_r
Y
X
Z
a
bottom metal
ground

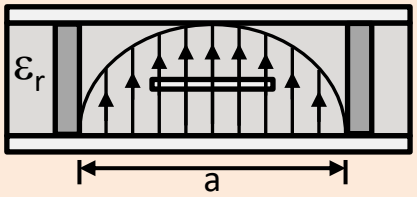
Design Of The Stripline Section Requires Careful Attention To Via Placement Detail

Stripline Desired Mode



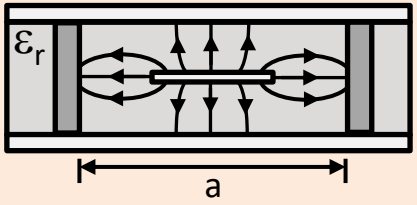
Avoiding the two undesired modes results in a limited range for acceptable values for dimension a.

Stripline Undesired Mode1



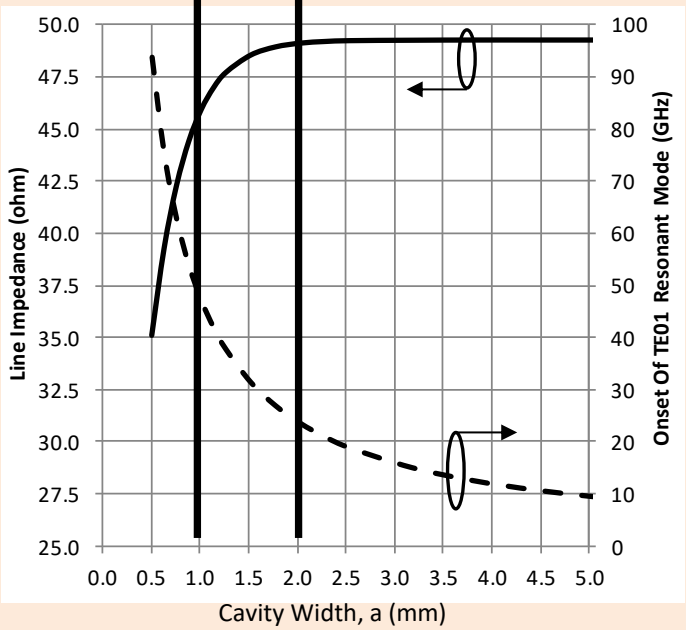
$$F_{sr1} = \frac{c}{2a\sqrt{\mu_r \varepsilon_r}}$$

Stripline Undesired Mode2



Simulate using quasi-static or full-wave simulator to determine change in impedance and effective dielectric constant as a function of spacing between vias.

Allowed Range For Dimension a



(for ε_r=9.8, b=1mm, w=0.203mm)

Design Procedure And Example For Stripline Transmission Line

Example: Consider the example of a stripline transmission line in HTCC alumina with a dielectric constant of 9.8 and allowed substrate thickness that must be a multiple of 0.125mm due to available green tape thicknesses with the fabricator. The frequency of operation is 20GHz. Using these design constraints, design a transmission line that is resonant free.

Step 1. Choose the thickness of the dielectric using . In most cases, the dielectric material is already determined which fixes ε_r and μ_r. The maximum operating frequency propagation on the line is also known for most applications which will determine f_{sr2}. To provide margin, it is good design practice is set f_{sr2} at 10-20% higher than is required. We will use a margin of 15% so that our maximum allows operation frequency which is the same as f_{sr2} = 1.15 x 20GHz = 23GHz. Use the equation for F_{sr2} and solve for b which is the thickness of the dielectric.

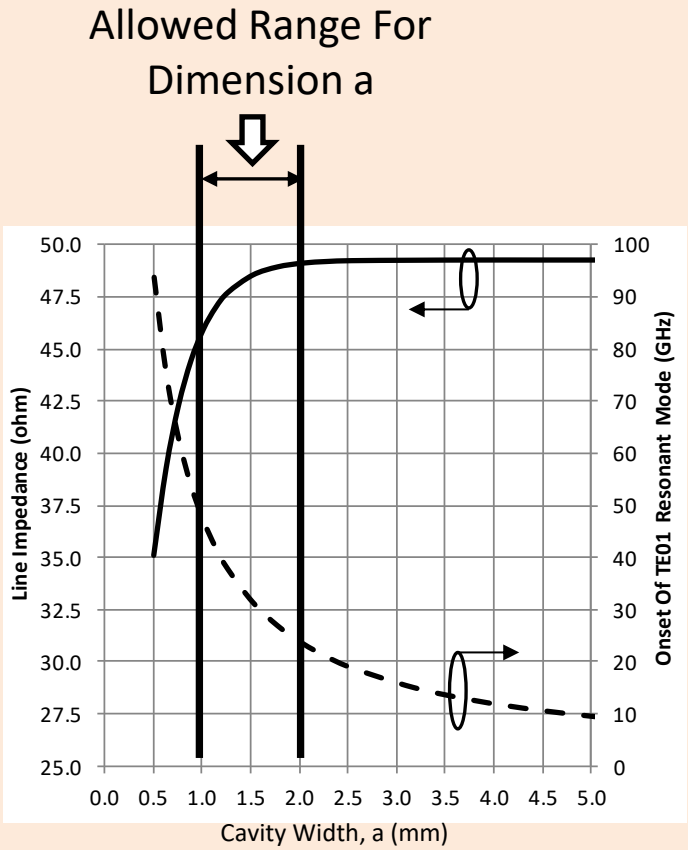
$$b = \frac{c}{4F_{sr2}\sqrt{\varepsilon_r \mu_r}} = 1.042mm$$

Since, the fabricator can only fabricate a dielectric with a thickness that is a multiple of 0.125mm, we will choose 1.0mm which means that the dielectric will be eight layers, each 0.125mm thick. The signal line will be symmetrically placed in the middle so there will be four layers above and four layers below the signal strip.

Design Procedure And Example For Stripline Transmission Line

Step 2. Next is the determination of the required line width for 50 ohm operation. Using a quasi static variational method of analysis (or other method) it was found that a line width of 0.203mm achieves about 50ohms.

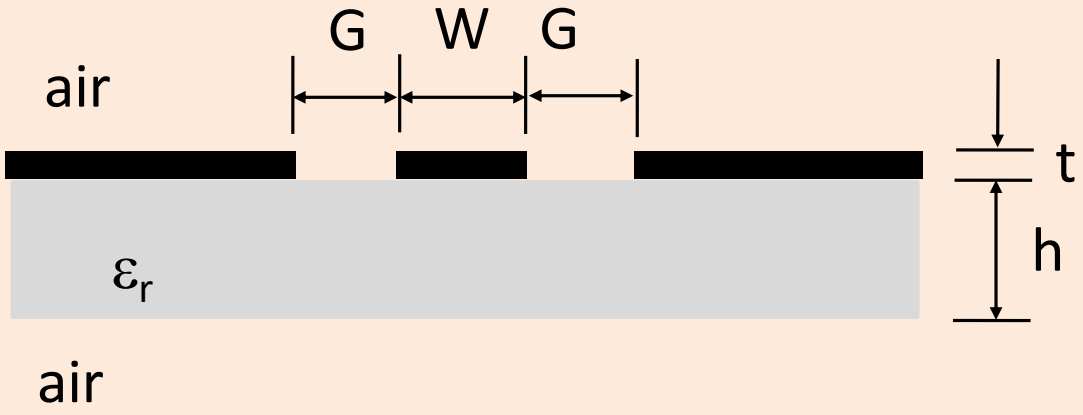
Step 3. The final step is to determine the width of the cavity. This is done by choosing the cavity width to be narrow so that the TE_{10} mode does not propagate, and at the same time, choosing the cavity width wide enough that the slot type mode is not excited on the strip which will increase the insertion loss. A good trade off is to keep the change in line impedance to be less than 5% and the TE_{10} mode at least 15% above the desired frequency range as illustrated in the figure. For this example, a cavity width of 1.5mm will be chosen. This results in the TE_{10} mode being pushed out to 30GHz and the change in line impedance is less than about 2%.



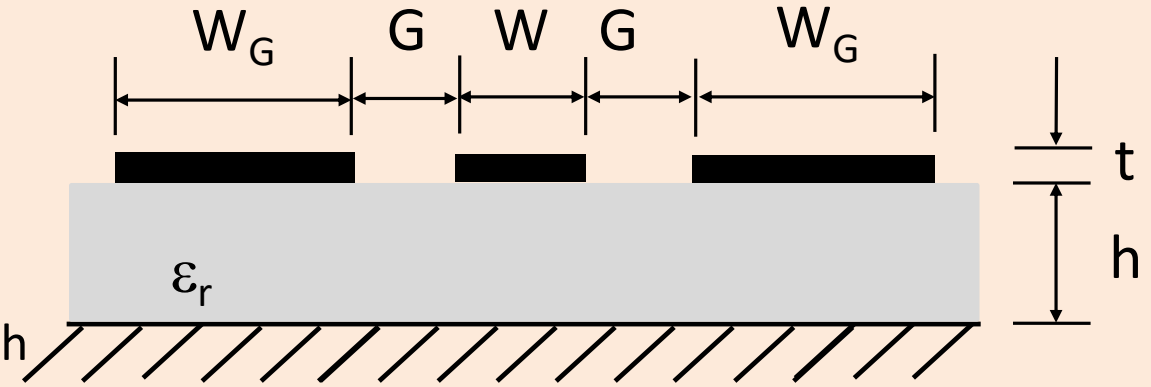
(for ε_r=9.8, b=1mm, w=0.203mm)

Coplanar Waveguide and Conductor Backed Coplanar Waveguide Transmission Lines

- Coplanar Waveguide
  - –Not used very often.
  - –Sometimes used for waveguide components such as filters



- Conductor Backed Coplanar Waveguide (CBCPW)
  - – Used in planar circuits such as printed circuit boards.



Design Equations For The Line Impedance of Conductor Backed Coplanar Waveguide

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{reff}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_3)}{K(k_3')}}$$

$$\varepsilon_{reff} = \frac{1 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_3)}{K(k_3')}}{1 + \frac{K(k')}{K(k)} \frac{K(k_3)}{K(k_3')}}$$

Where:

k = a/b

$k_3 = \tanh(\pi a/2h)/\tanh(\pi b/2h)$

$$k' = \sqrt{1 - k^2}$$

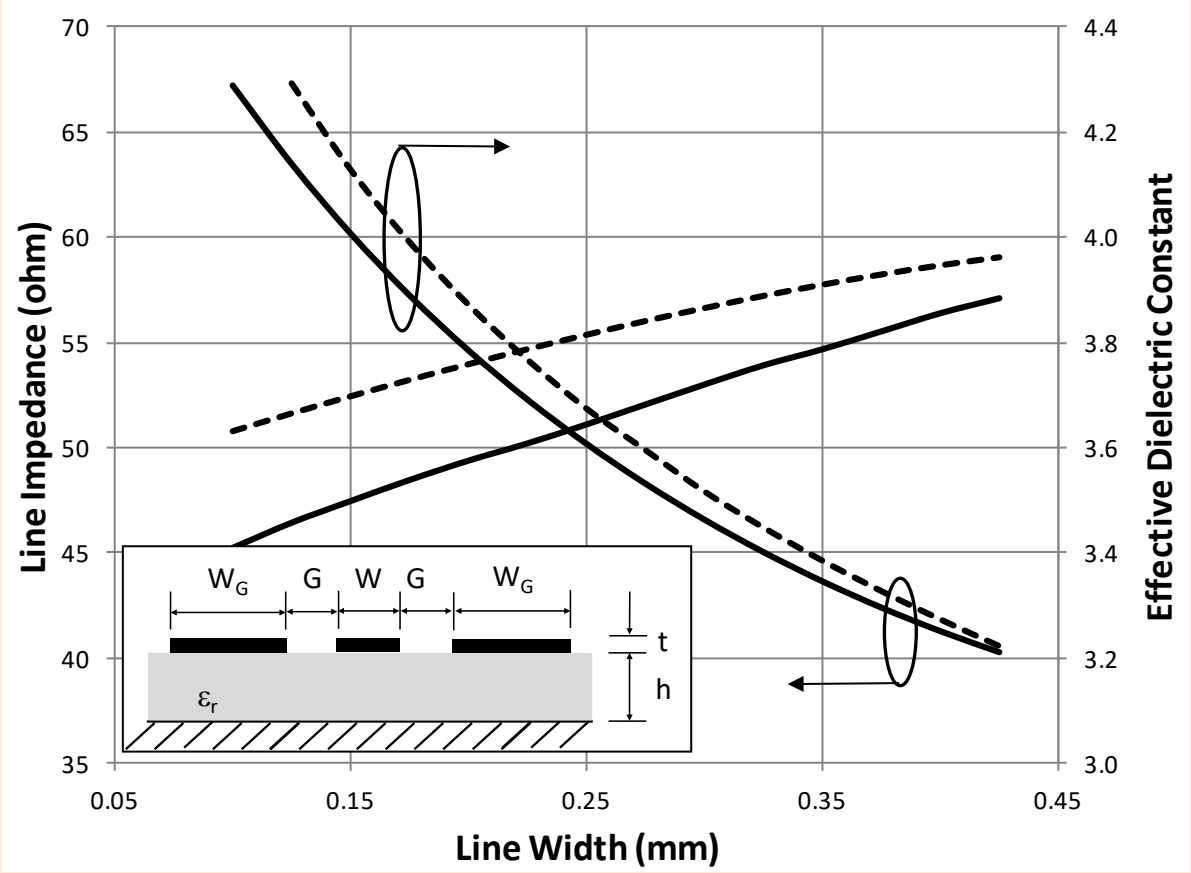
$$k_3' = \sqrt{1 - k_3^2}$$

a = W/2

b = W/2 + G

K(k) = complete elliptical integral of the first kind

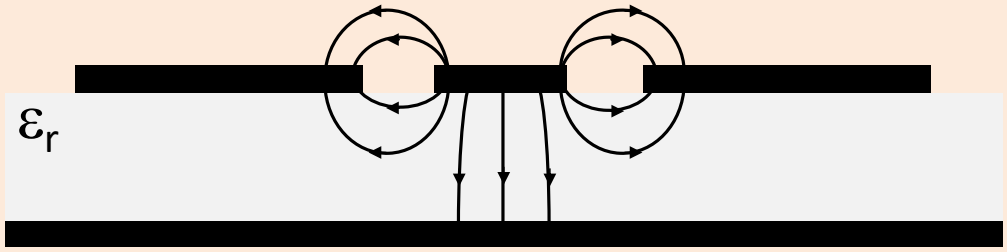
Comparison of Z_o and E_{reff} calculated value and HFSS simulated value.



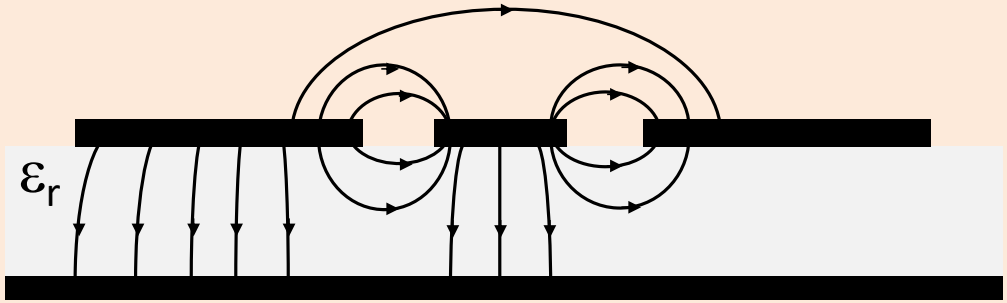
Use closed form approximations for the complete elliptical integral of the first kind for the calculations.

Avoid Undesired Modes In Coplanar Waveguide

Desired CBCPW Mode

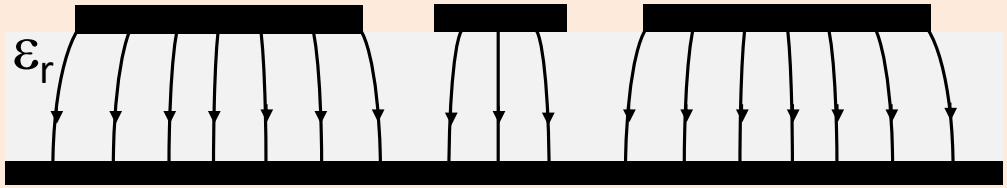


Undesired Slot Mode



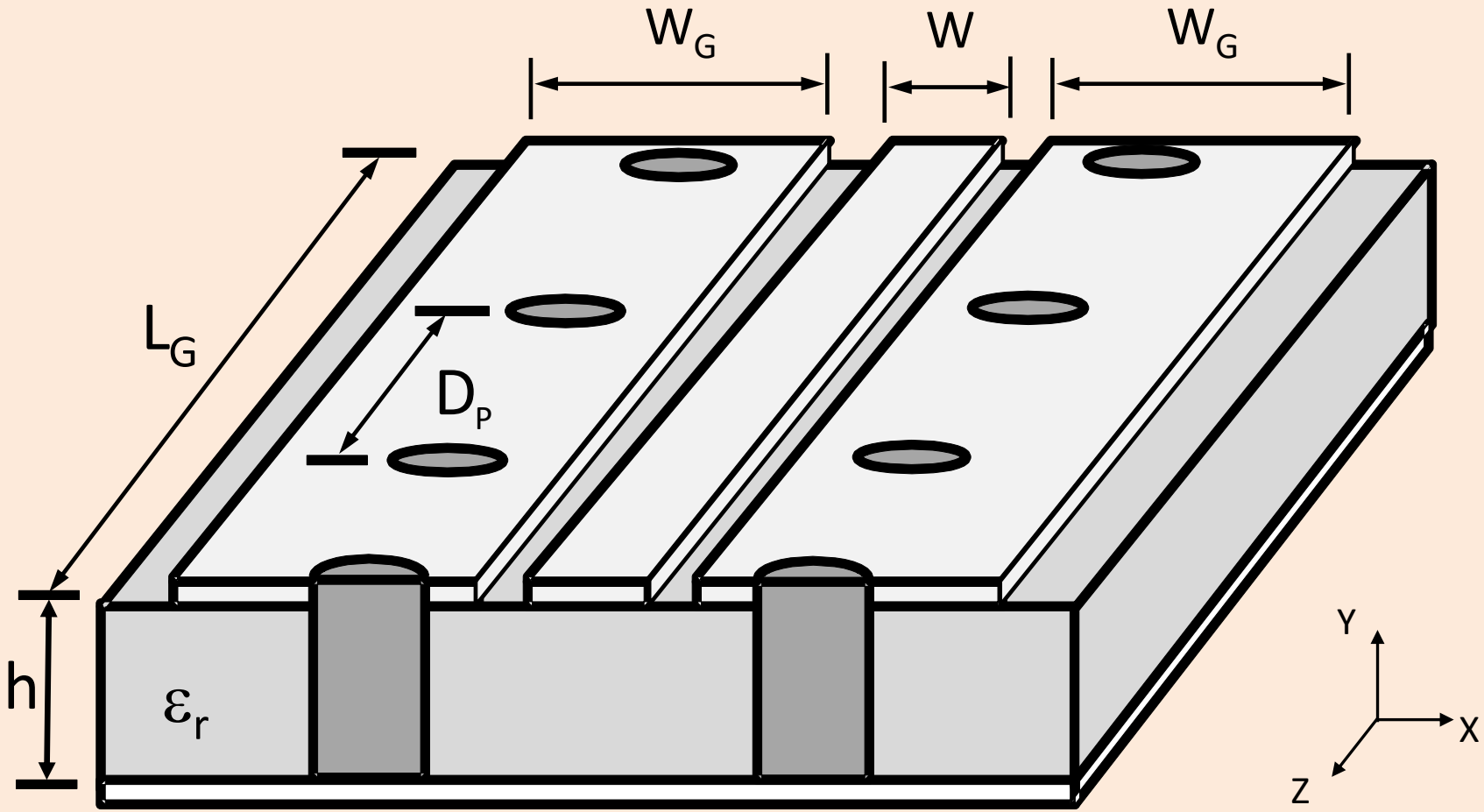
Controlled using vias connecting grounds together

Undesired Parallel Plate Mode



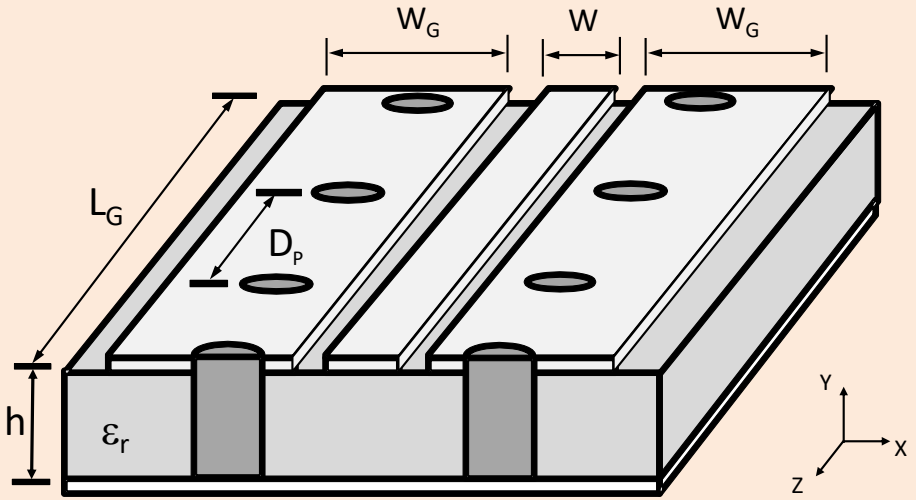
Controlled using vias connecting grounds together

Avoid Undesired Modes In Conductor Backed Coplanar Waveguide By Using Vias



It Is Possible To Predict The Excitation Of Undesired Resonances From The Topside Grounds

$$f_{mn} = \frac{c}{2\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m}{W_G}\right)^2 + \left(\frac{n}{L_G}\right)^2}$$



mode index		Resonant Frequency		
m	n	From The Above Equation	Simulated HFSS	Simulated MoM
0	1	12.17 GHz	12.5 GHz	12.9 GHz
0	2	24.35 GHz	24.55 GHz	25.46 GHz
0	3	36.52 GHz	36.55 GHz	37.74 GHz

Agreement is within 2.7%

Comparison of the equation and HFSS for the prediction of resonant modes on the topside ground plane of CBCPW with ε_r=6.0, h=0.2mm, W_G=1.016mm, L_G=5.03mm , W=0.203mm, G=0.152mm

Guidelines For Designing CBCPW Transmission Lines

- Use either closed form design equations that were presented or commercially available software for the design of the transmission lines to achieve the desired line impedance.
- The transmission line will support three modes: the desired CBCPW mode, the slot like mode and the parallel plate (or also called the microstrip like) mode. It is important to use vias to connect the topside grounds to the bottom side grounds to inhibit the excitation of the undesired modes.
- Proper placement of vias connecting the topside ground to the bottom side ground is critical to achieve the bandwidth required. The vias pitch D_p should be chosen to avoid the onset of a patch antenna type mode which resonates along the length of the line. In general, place the vias as close as is allowed by the design rules of the circuit board process. However, as a good rule of thumb, place the vias no more than a quarter wavelength away (this is half the distance that is predicted by the equation on the previous page with Lg replaced by Dp).
- Use multiple vias on the topside ground at the edge near the gap and the outside edge of the top metal.

Excellent References On Designing CBCPW To Avoid Undesired Modes

Liu, Y., Itoh, T., “Leakage phenomena in multilayer conductor-backed coplanar waveguides,” IEEE Microwave and Guided Wave Letters, Vol. 3, No. 11, 1993, pp. 426-427.

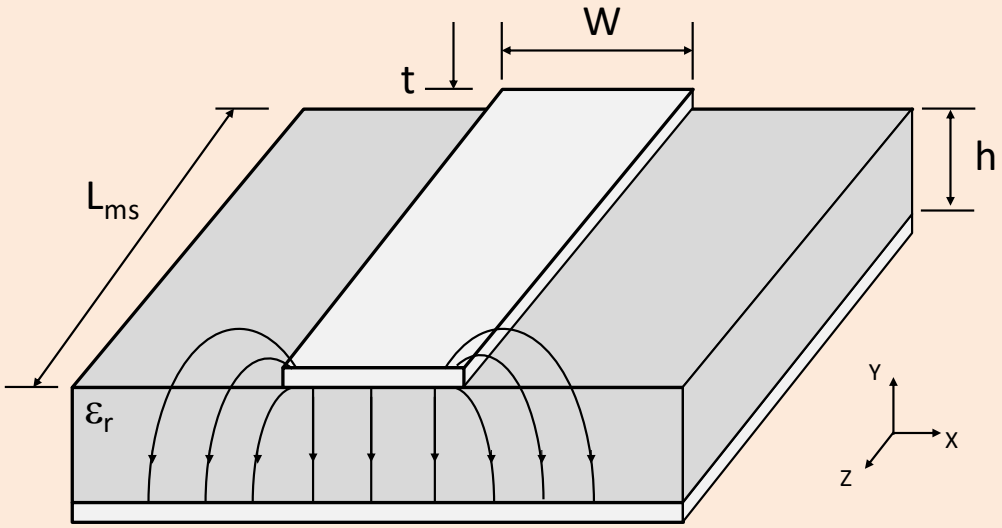
Jackson, R.W., "Mode Conversion at Discontinuities in Finite-Width Conductor-Backed Coplanar Waveguides," IEEE Trans. Microwave Theory Tech., Vol. 37, No. 10, 1989, pp. 1582-1589.

Beilenhoff, K., Heinrich, W., “Excitation of the parasitic parallel-plate line mode at coplanar discontinuities,” IEEE MTT-S International Microwave Symposium Digest, Denver, CO, June 8-13, 1997, pp. 1789-1792.

Schnieder, F., Tischler, T., Heinrich, W., “Modeling dispersion and radiation characteristics of conductor backed CPW with finite ground width,” IEEE Trans. Microwave Theory Tech., Vol. 51, No. 1, 2003, pp. 137-143.

Heinrich, W., Schnieder, F., Tischler, T., “Dispersion and radiation characteristics of conductor backed CPW with finite ground width,” IEEE MTT-S International Microwave Symposium Digest, Boston, MA, June 11-16, 2000, pp. 1663-1666.

Design Of Microstrip Lines



- Design equations for calculating the line impedance and effective dielectric constant of microstrip.
- Suggestion: Use commercially available transmission line impedance

$$when \left(\frac{W}{H}\right) < 1$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(8\frac{H}{W} + 0.25\frac{W}{H}\right) \quad (ohms)$$

$$when \left(\frac{W}{H}\right) \geq 1$$

$$Z_0 = \frac{120\,\pi}{\sqrt{\varepsilon_{eff}} \times \left[\frac{W}{H} + 1.393 + \frac{2}{3}\ln\left(\frac{W}{H} + 1.444\right)\right]} \quad (ohms)$$

$$when \left(\frac{W}{H}\right) < 1$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\left(\frac{H}{W}\right)\right)^{-1/2} + 0.04\left(1 - \left(\frac{W}{H}\right)\right)^2\right]$$

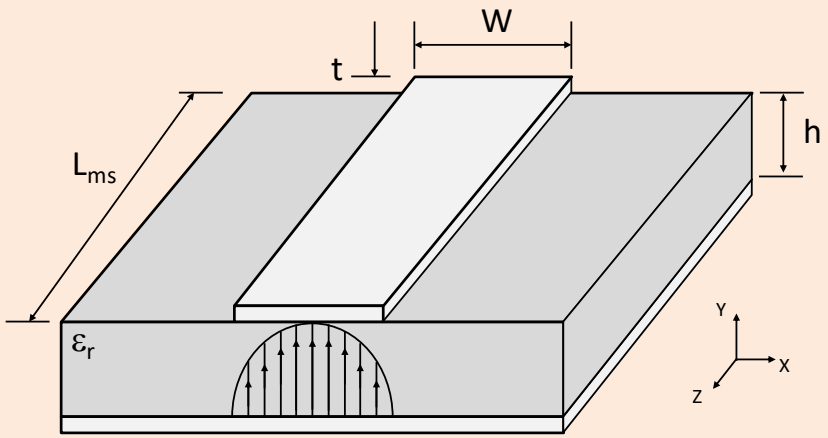
$$when \left(\frac{W}{H}\right) \geq 1$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\left(\frac{H}{W}\right)\right)^{-1/2}$$

Avoid The Transverse Higher Order Mode

$$F_c = \frac{c^2 \varepsilon_0 \sqrt{\varepsilon_r} Z_0}{2h\sqrt{\varepsilon_{reff}}}$$

Choose h so that F_c > 2 times your max operating frequency



- This is the mode that exists when the microstrip line width is equal to a half wavelength.
- Example: alumina substrate (ε_r = 9.8) and 0.5mm thickness with 50 ohm line and ε_{reff} = 6.839.
- Fc ~ 47GHz.
- However, a good rule of thumb is to set the maximum operating frequency to half the value calculated using this equation to accommodate the range of line impedances that may be needed.

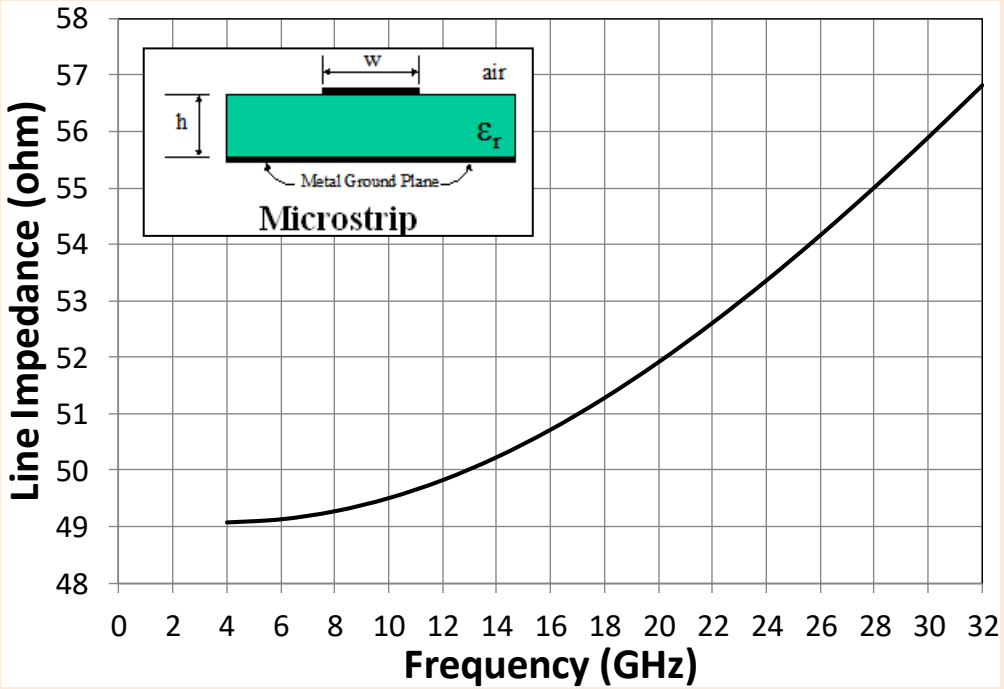
Summary For Microstrip Design

- **Step 1:** Choose substrate thickness so that the cut off frequency is twice your maximum operating frequency.
- **Step 2:** Design transmission line width to achieve the desired line impedances using the provided equations or a commercially available transmission line solver.

Section 2.2: Dispersion

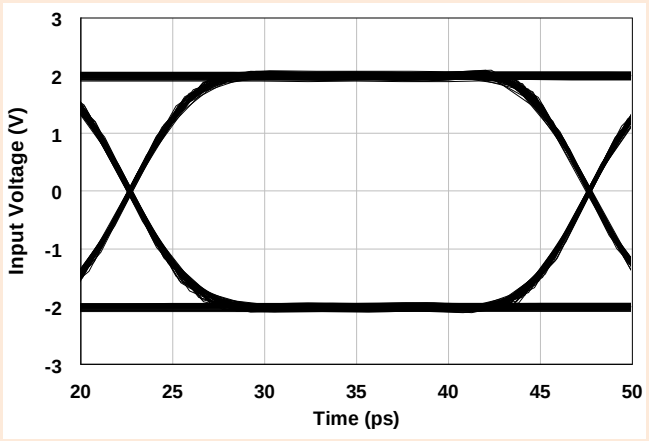
- What is dispersion and why is it important to packaging for 5G solutions?

Dispersion in transmission lines cause the line impedance and propagation constant to change as a function of frequency. Stated another way, the group delay of the signal will not be constant as a function of frequency if there is dispersion.



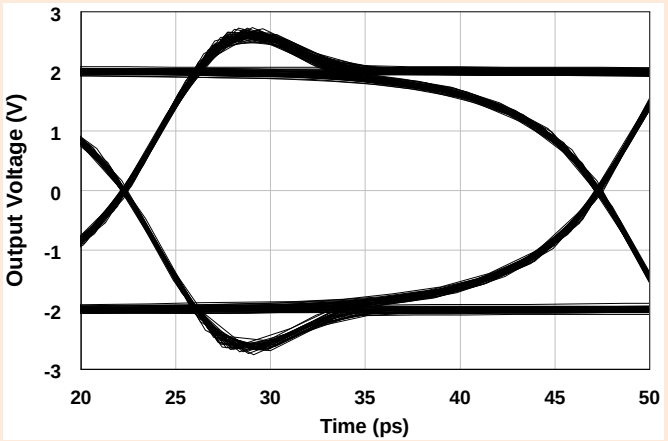
Dispersion in microstrip for h=635μm, w=635μm, ε_r=9.8 (alumina ceramic)

Dispersion Is Also A Concern For Wide Band Signals



Input Eye Diagram

w=0.422mm,
h=0.381mm, ε_r=9.8 and
line length of 3.81mm



Output Eye Diagram

- Dispersion reduces signal integrity and is particularly difficult for wideband signals.
- Causes
  - Overshoot
  - Eye closing
  - Increased jitter

Design Guideline For Microstrip To Avoid Dispersion

$$h < 0.05\lambda \Rightarrow \frac{h}{\lambda} < 0.05$$

But, $\frac{1}{\lambda} = \frac{f\sqrt{\varepsilon_r}}{c}$

Therefore, $\frac{h}{\lambda} = \frac{hf\sqrt{\varepsilon_r}}{c} < 0.05$

Solving for *h*, we obtain

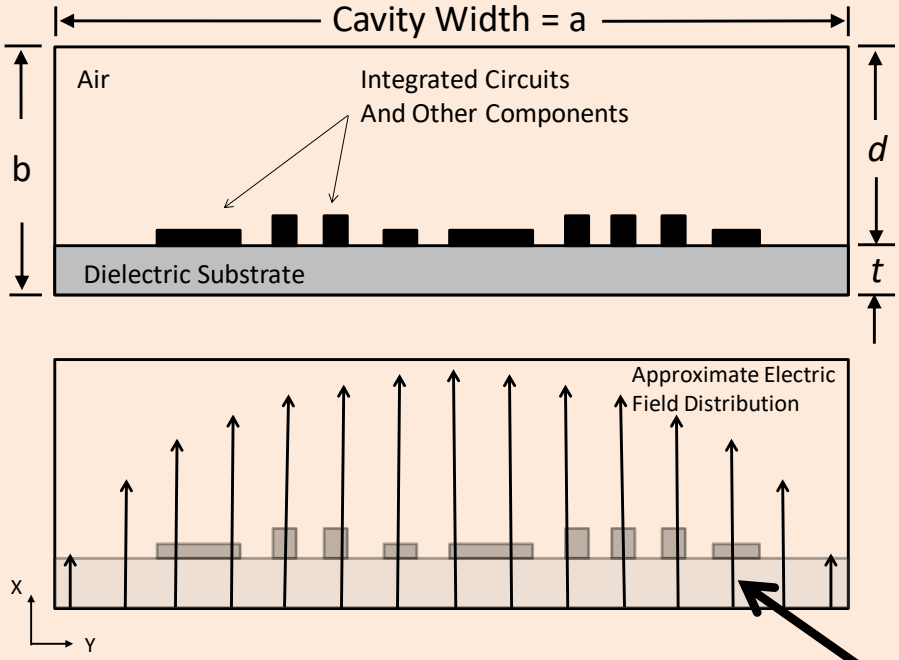
$$h < \frac{0.05c}{f\sqrt{\varepsilon_r}}$$

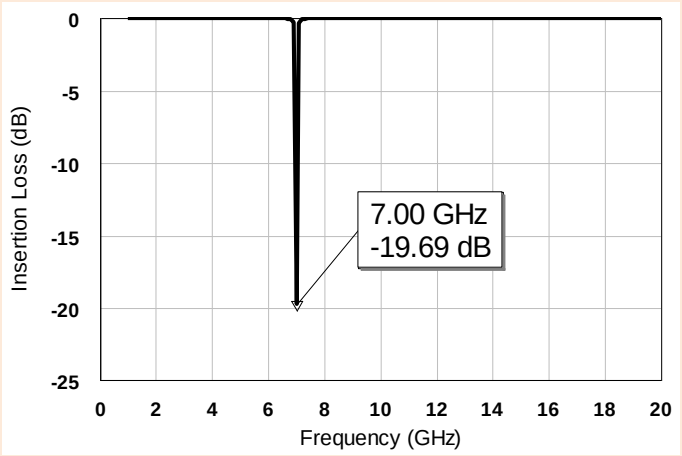
To avoid dispersion, choose substrate thickness that obeys this guideline

- For microstrip, dispersion effects increase as the thickness of the substrate increases.
- A guideline for microstrip lines is that the substrate thickness must be less than 5% of a wavelength.

Where:
c = velocity of light in free space
h = substrate thickness
ε_r = dielectric constant of substrate
f = max frequency of operation

Section 2.3: Package Resonances
In Packages And Housings Cause Energy To Be Sucked Out of The Desired Signal





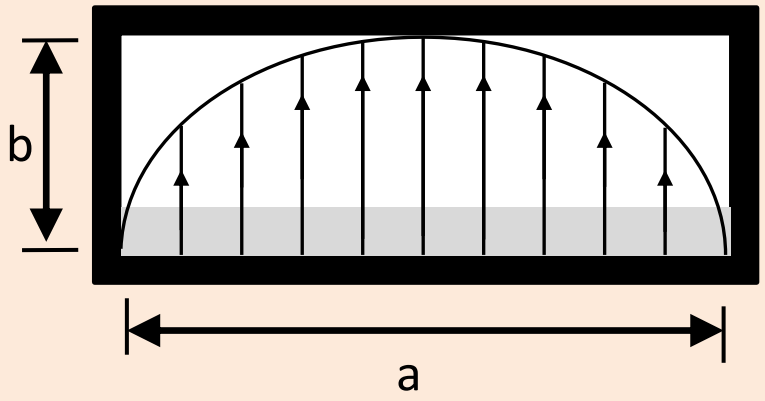
The cavity resonance frequency can be approximated as a TE10 waveguide mode resonance

Resonance Frequency Is Approximated By

$$f_r = \frac{c}{2a}$$

Where:
f_r = cavity resonance frequency
a = width of the cavity
c = velocity of light in free space

A Better Approximation Of The Resonant Frequency Is The LSM11 Mode



- The Logitudinal Section Magnetic (LSM) mode propagates in a dielectric filled waveguide.

Propagation constant for the LSM11 mode is give by

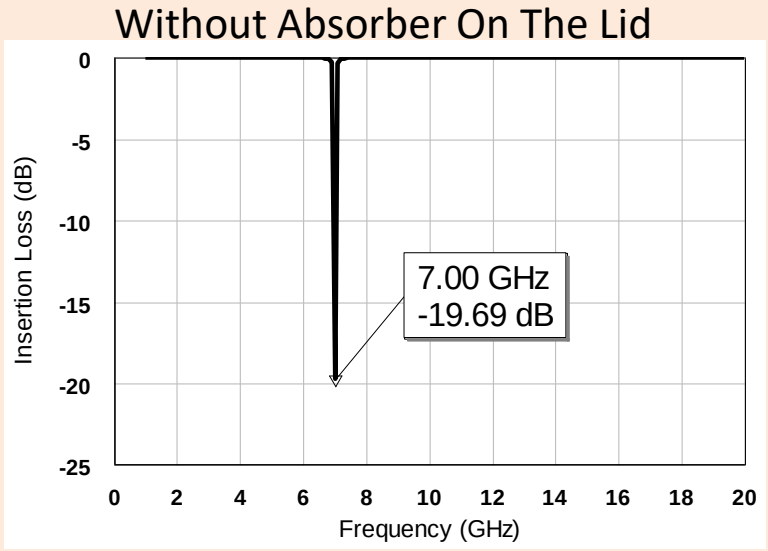
$$\gamma_{LSM11}^2 = \frac{Q}{2|P|} - \left(\frac{Q^2}{4|P|^2} - \frac{|T|}{|P|} \right)^{0.5}$$

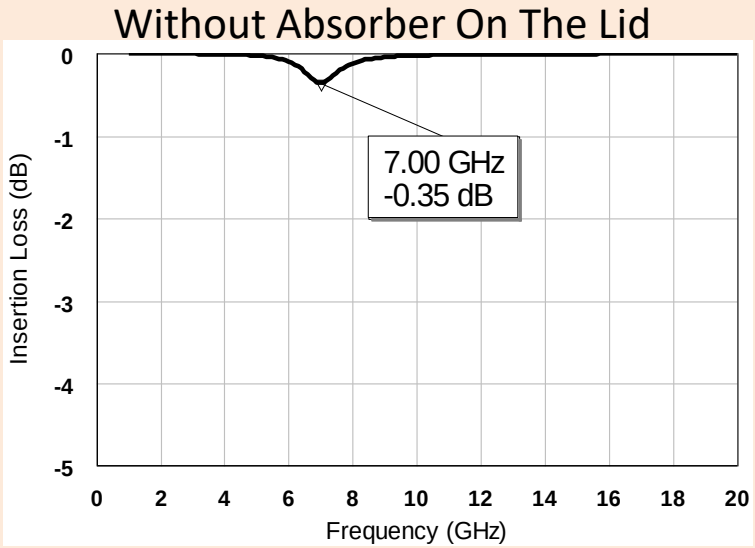
The full solution to the equation for the LSM11 mode is given in either of these references

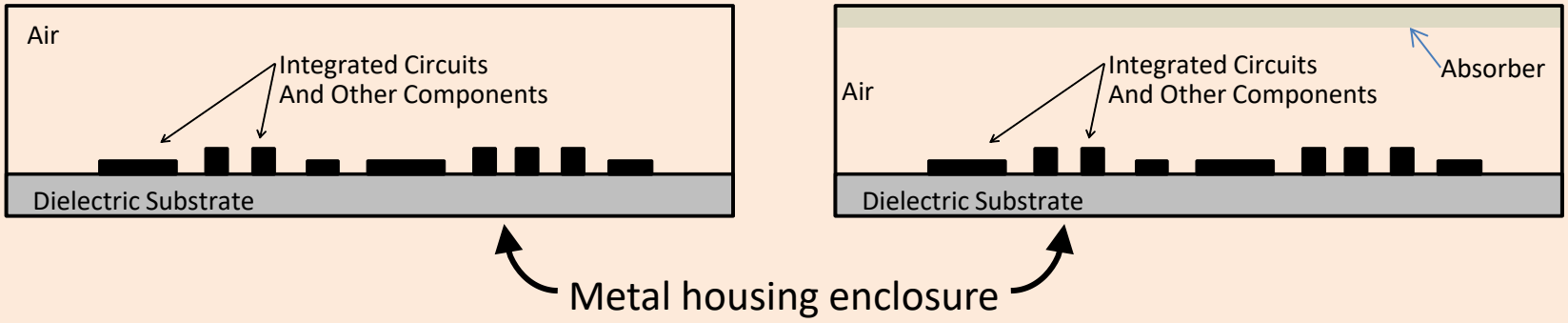
R. Sturdivant, *Microwave and Millimeter-wave Electronic Packaging* (Artech House, 2014), pp. 8-9.

R.E. Collin, *Field Theory of Guided Waves, 2nd Edition* (IEEE Press, 1991), pp. 428-429.

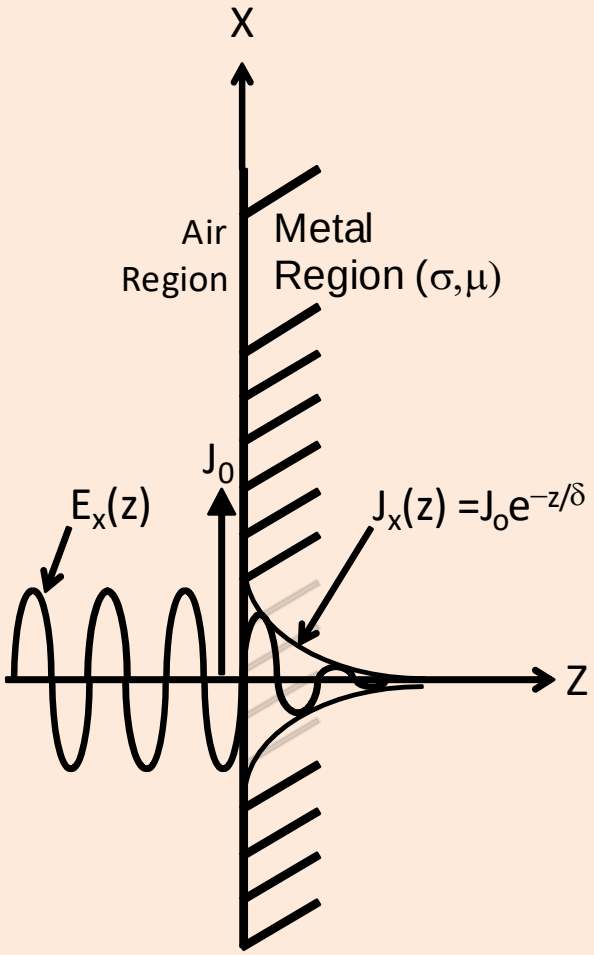
One Method To Reduce The Cavity Resonance Effect Is To Use Absorber In The Lid







Section 2.4: Skin Effect
Skin Effect Tells Us That The RF Current Only Penetrates A Small Distance Into The Metal



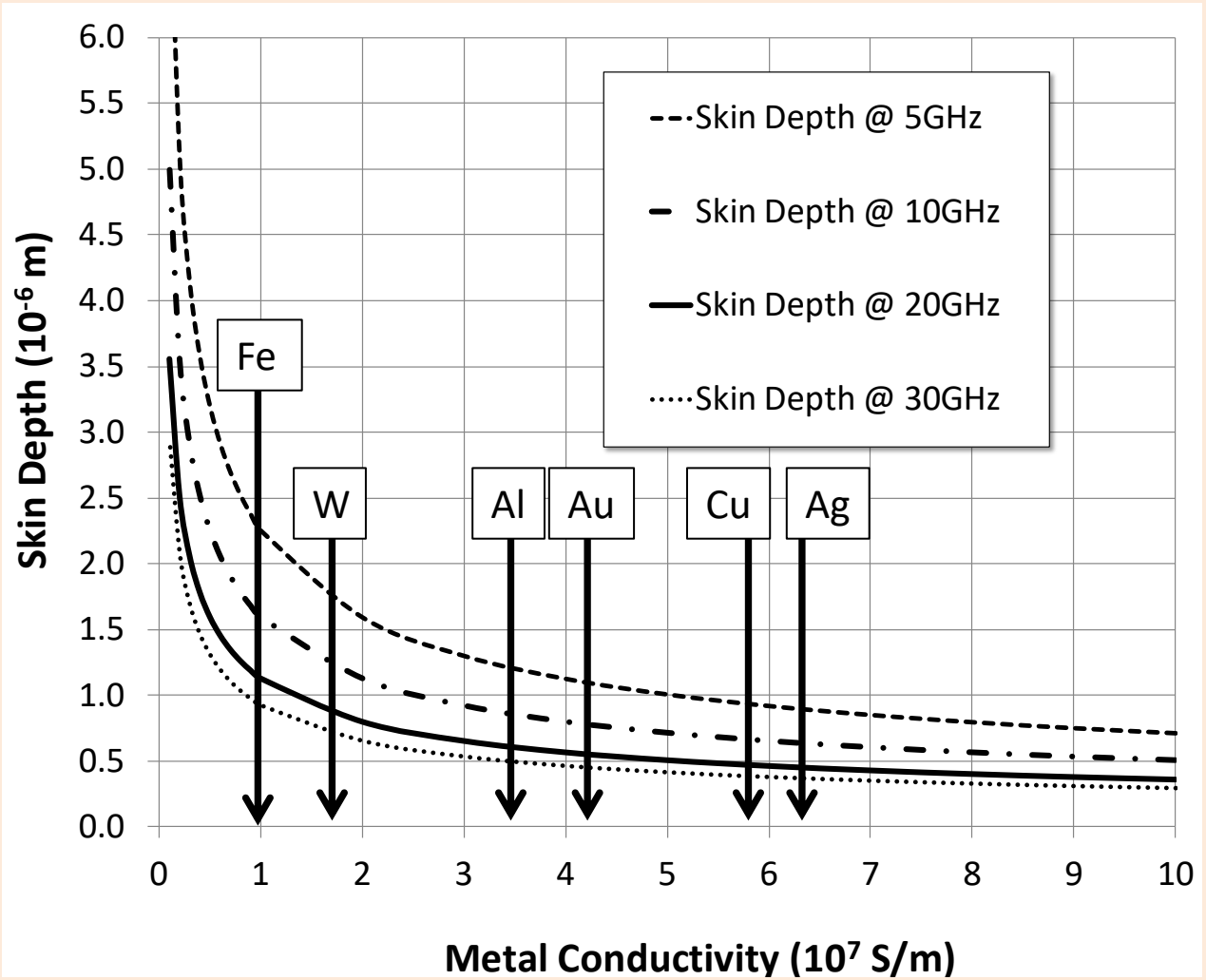
Skin effect is the tendency of an alternating electric current (AC) to become distributed within a conductor such that the current density is largest near the surface of the conductor, and decreases with greater depths in the conductor.

$$Skin\ Depth = \delta = \frac{1}{\sqrt{\pi \mu \sigma f}}$$

Where:
μ = permeability
σ = metal conductivity
f = frequency of concern

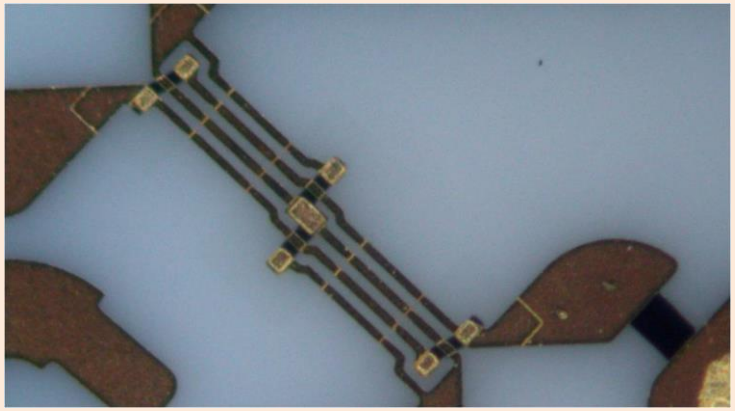
Skin Depth For A Few Different Metal Types As A Function Of Frequency

Metal Type	Conductivity 10^7 (S/m)
Silver	6.21
Copper	5.85
Gold	4.42
Aluminum	3.69
Tungsten	1.89
Iron	0.97

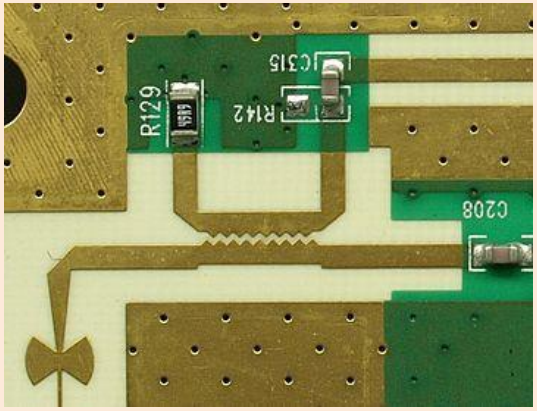


Section 2.5 Coupling
Coupling (Both Desired and Undesired)

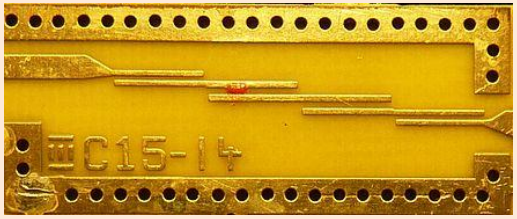
Coupling Can Be Used For Desired Functions

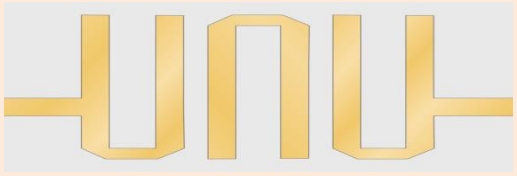


Lange Coupler



Directional Coupler



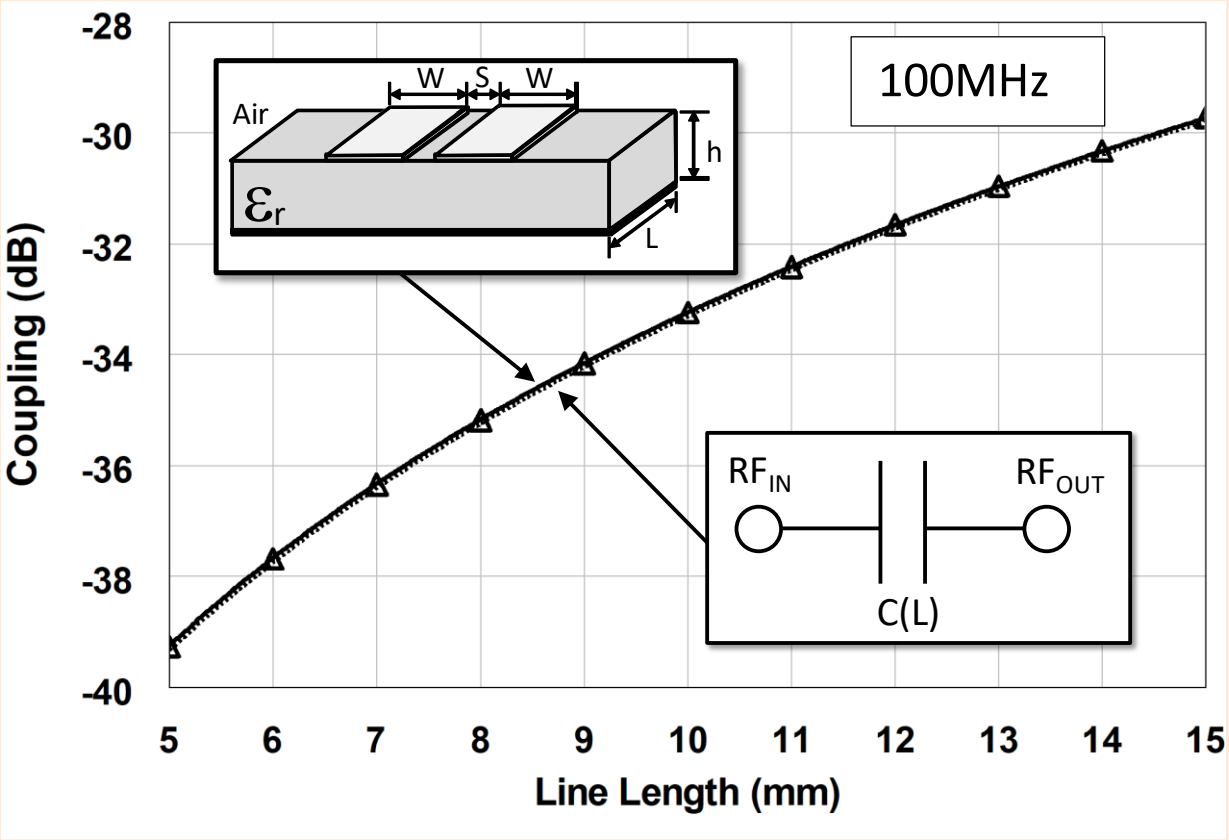


Filter

Coupling Can Also Cause Significant Undesired Effects

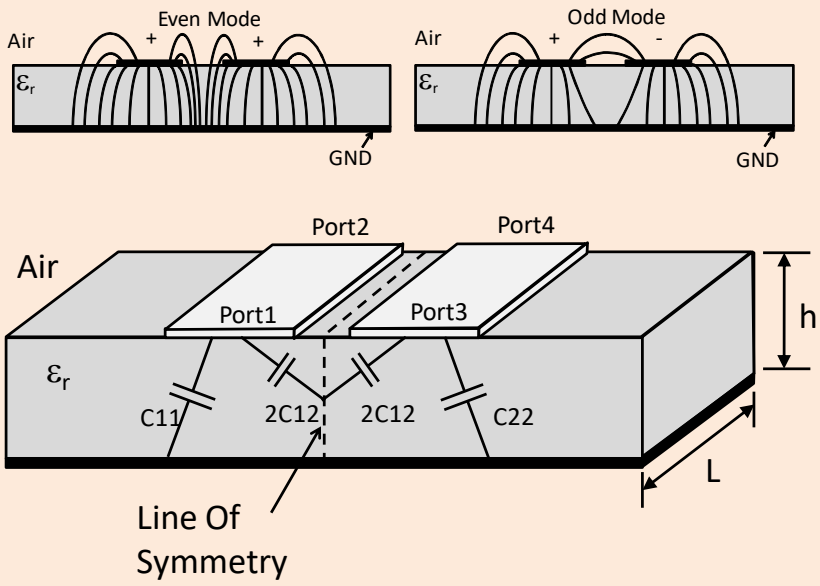
- Coupling can cause oscillations
- Coupling can cause undesired circuit resonances
- Coupling can cause undesired electromagnetic resonances
- Coupling can cause voltage spikes

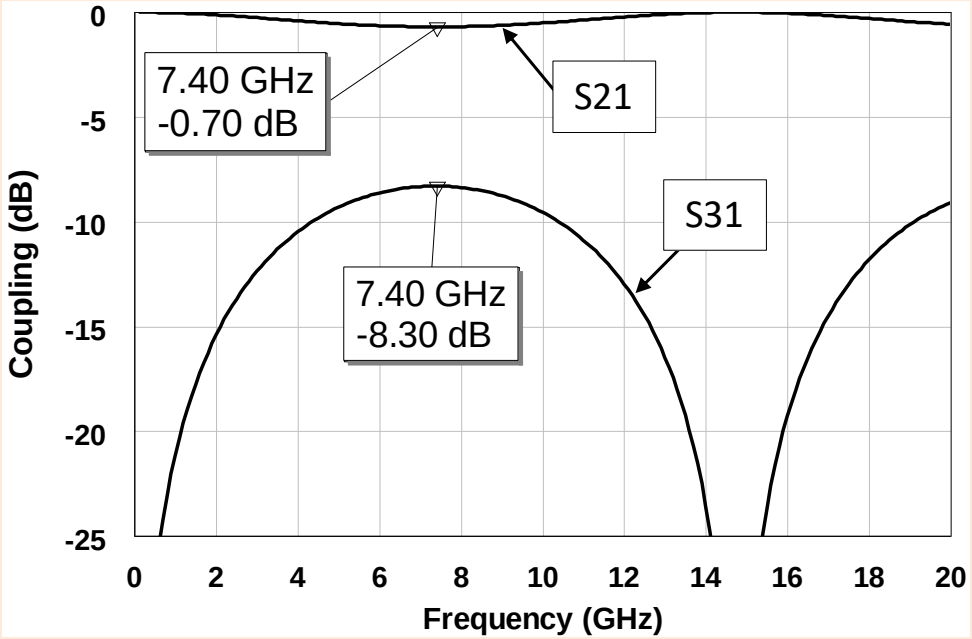
The Simple Model Of Coupling Uses A Capacitor

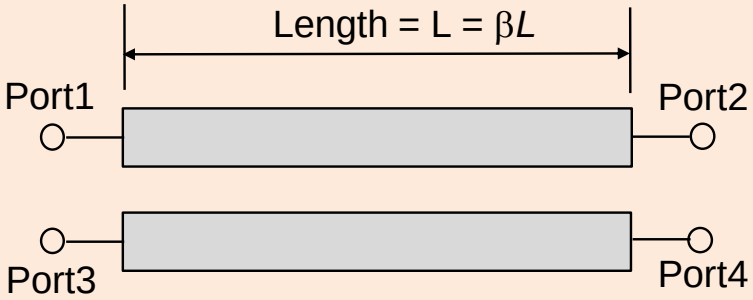


- At low frequencies, coupling can be modeled as a simple capacitor.
- On this approach, coupling increases as the length of the coupling structure increases.

A Higher Fidelity Model Of Coupling Uses Even and Odd Mode Analysis



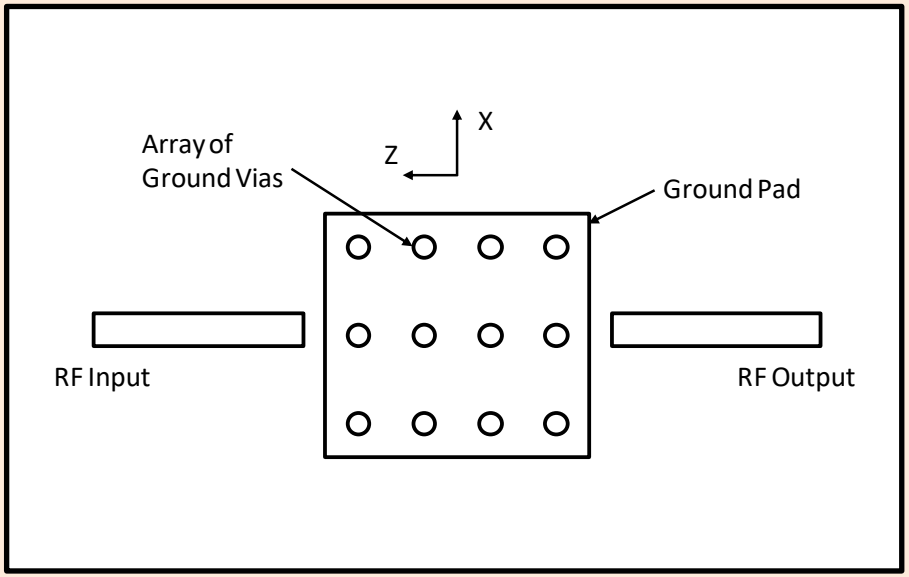




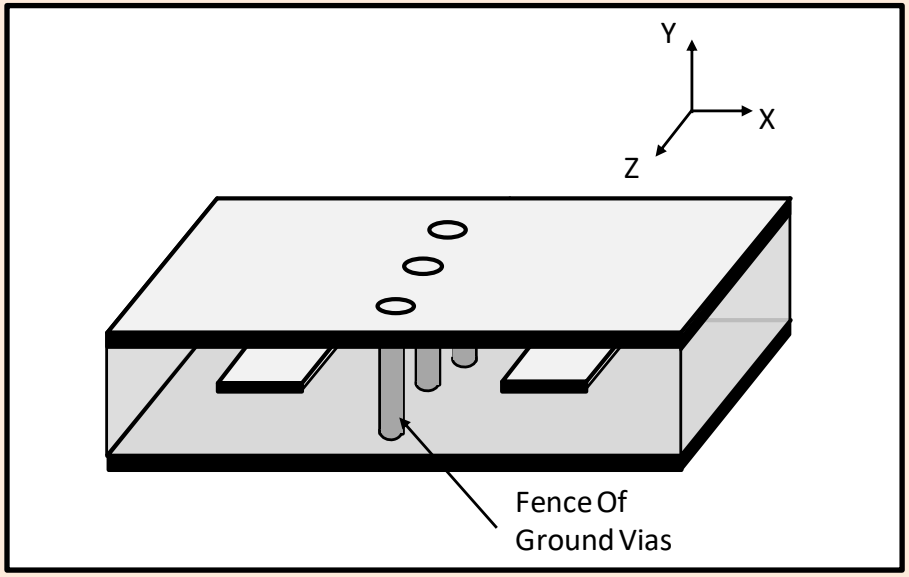
- Coupling is frequency dependent.
- Coupling also depends upon the length of the coupled section

The Importance Of Grounding For Isolation And Avoiding "Ground" Layer Resonances

Ground Metal Via Connection



Vias For Isolation

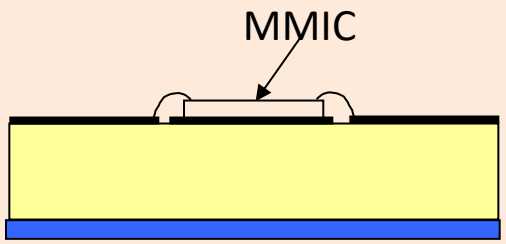


- Via arrays are essential for achieving acceptable ground contact. Otherwise ground metal will resonate
- Via fence is used to increase isolation between transmission lines and other circuits.

Section 2.6 Interconnects

Level 1 Interconnects A Few Options

1) Wire Bonds



1) Wire Bonding (Face-Up Die Mounting)

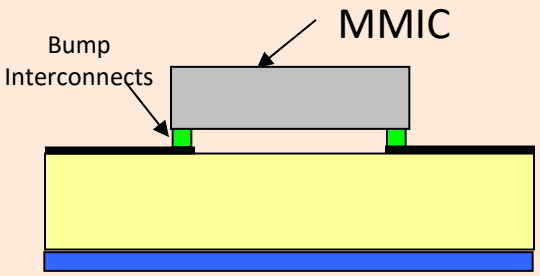
Benefits:

- Low cost and low barrier to entry
- This is the industry standard for die attach. Extensive installed manufacturing base

Drawbacks:

- Wire bond inductance and variability. This creates variability in performance
- Wire bond radiation into the module can cause resonances at millimeter-wave frequencies

2) Flip Chip



2) Flip Chip

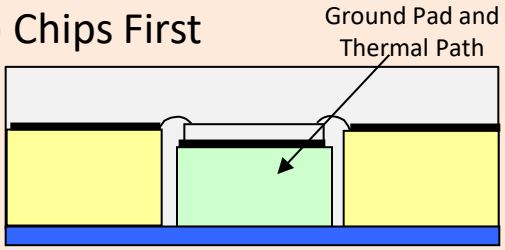
Benefits:

- Low inductance and highly repeatable interconnect
- Low radiation and some cost benefit (compared to wire bonds) at very high volume production

Drawbacks:

- Requires modified manufacturing and design processes(IC & module)
- Requires changes to design methods (CPW versus microstrip)

3) Chips First



3) Chips First

Benefits:

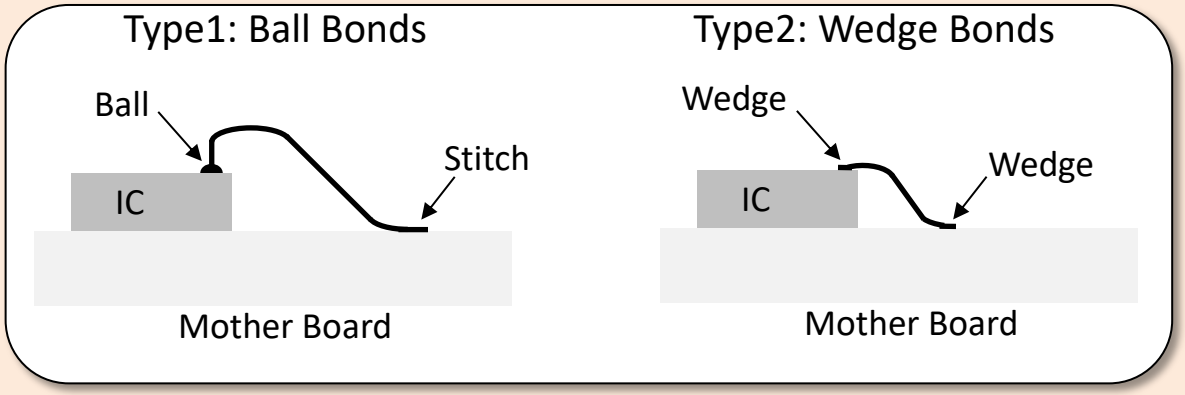
- Moderate/low inductance and highly repeatable interconnect

Drawbacks:

- Over molding affects MMIC performance
- Costly and module rework is difficult
- Requires modified manufacturing and design processes(IC & module)

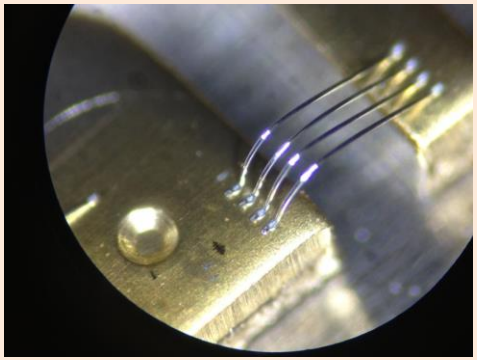
Wire Bonds Are Used Extensively In Microelectronics

Example of a wire bonding machine



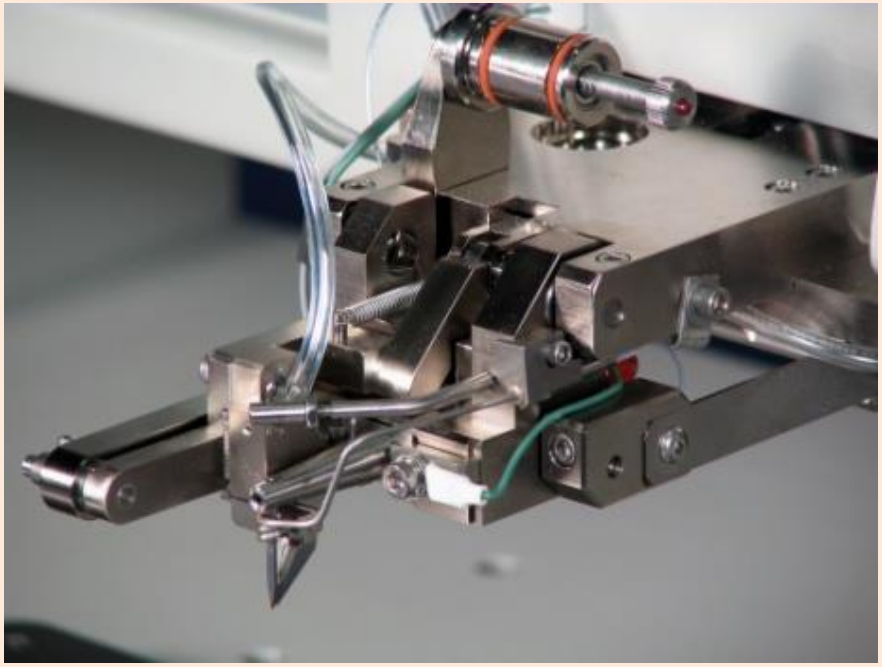
Broadly speaking, there are at least two types of wire bonds

- Wire bonds are the back bone for most microelectronic packaging.
- Properly accounting for their effects is critical at microwave and millimeter-wave frequencies.



Example of wedge bonds

Wire Bond Machines

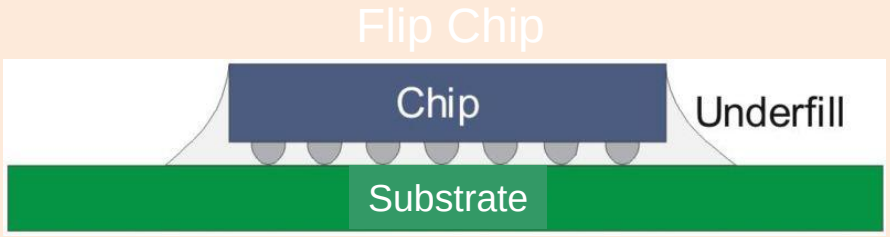


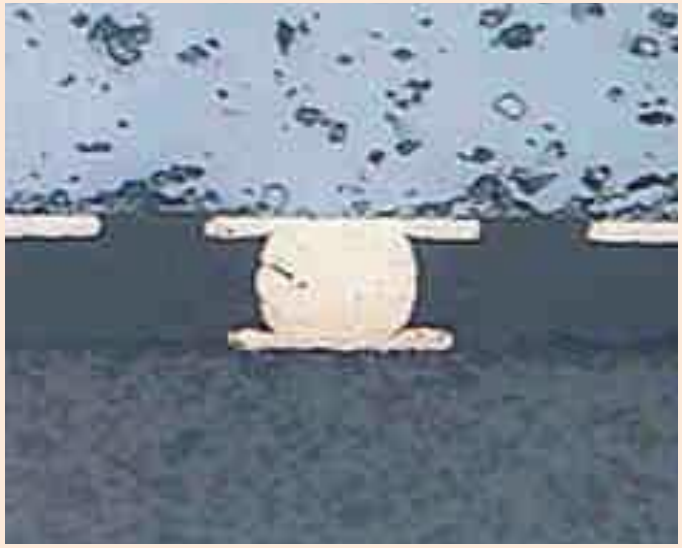
Flip Chip First Level Interconnect

- Chip interconnect by means of bumps with two technologies:

  (i) Thermocompression
  - Au bumps (using electroplating or stud bumps)
  - bonding by thermocompression

- (ii) Soldering
  - e.g., AuSn or PbSn bumps
  - chip bonding & soldering in reflow oven
- In Section 4, flip chip interconnects will be investigated in more detail



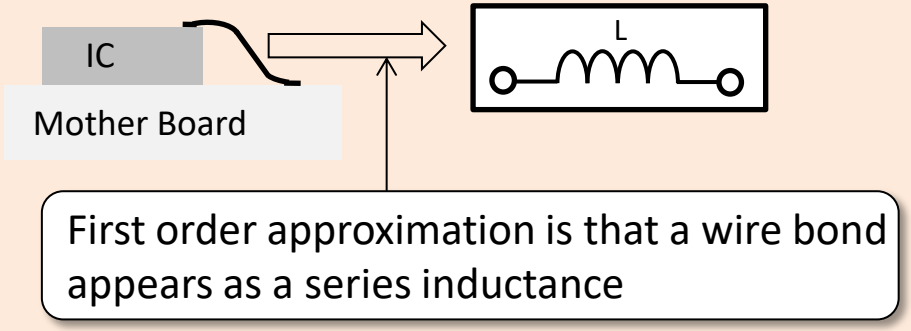


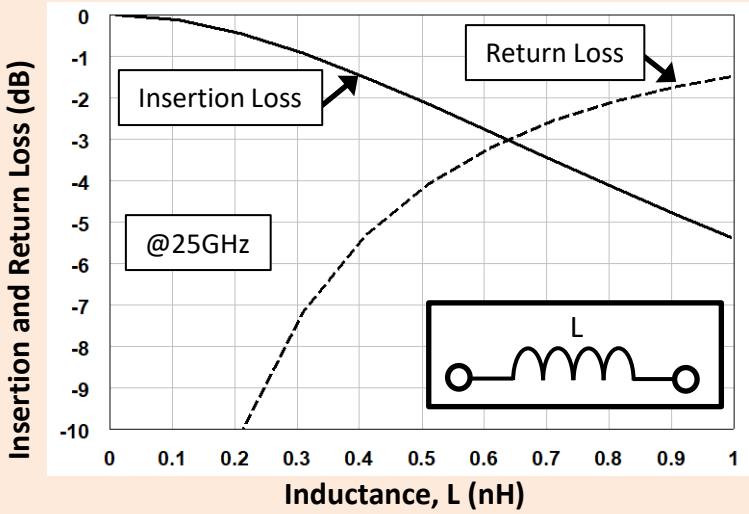
Additional Comparisons Between Flip Chip and Wire Bonding

- Flip Chip
  - Can be expensive to implement.
  - Most beneficial (electrical performance) at millimeter-wave frequencies.
    - Can provide significant benefit over wire bond electrical performance.
  - Reliability of the bump connection can be an issue for hard bumps
    - Requires careful material selection and modeling.
  - Thermal: How do you remove the heat from the flip chip
- Wire Bonding
  - Very common interconnect method.
  - Low cost.
  - Introduces series inductance
  - Slight temperature dependence in either wire resistance or inductance

One Approach To Wire bond Modeling Is To Approximate Its Electrical Performance As A Series Inductor

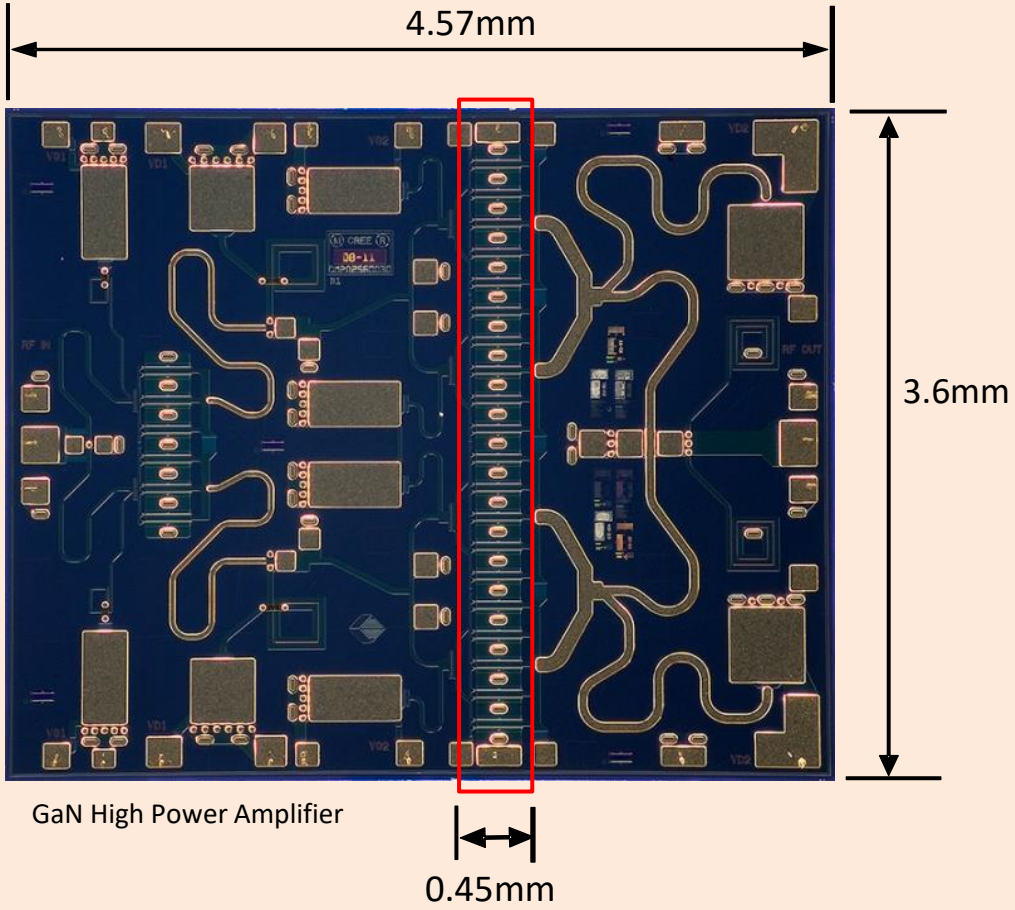
- If the simplified electrical model of a wire bond is a series inductor, at what inductance level will the electrical performance be negatively impacted?
- At 25GHz, the answer is that even a small amount of series inductance, as low as 0.2nH, will negatively impact electrical performance.
- In Section 4, detailed wire bond models will be developed.





2.7 Heat Dissipation For 5G

The Main Challenge Is The Large Heat Flux

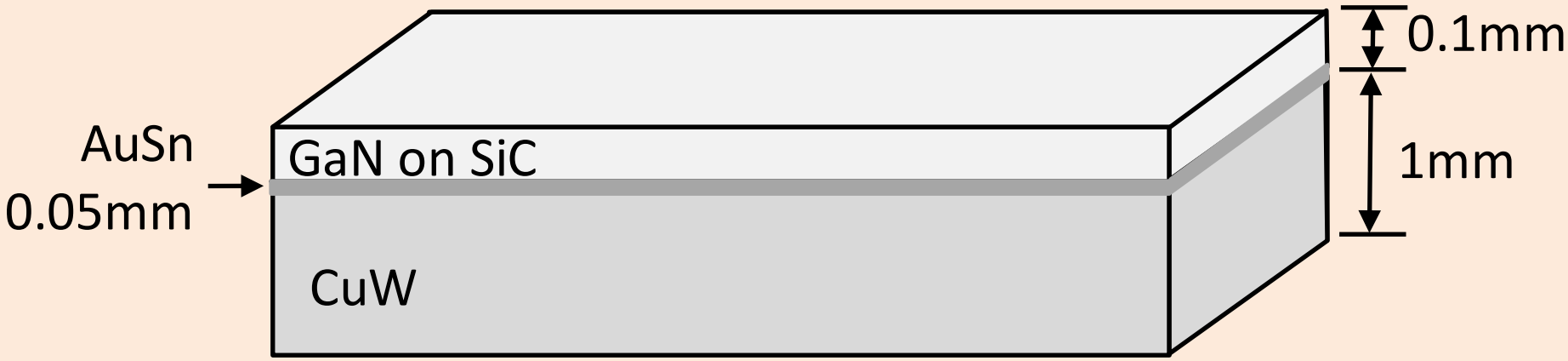


Heat Flux Is Calculated Using

$$\text{Heat Flux} = q = \frac{Q}{A} = \frac{38W}{0.045cm \times 0.36cm} = 2469W / cm^2$$

- The local heat flux in high power amplifiers operating at microwave and millimeter-wave frequencies can be several thousand Watts per square centimeter

One Way To Help Manage The Heat Flux Is To Braze High Thermal Conductivity Shims



- Copper Tungsten (CuW) shims have higher thermal conductivity at 180-220 W/mK
- CuW has a coefficient of thermal expansion that is matched to the semiconductor in the range of 7-9ppm/°C
- Heat transfer will be discussed in more detail in Section 7

Section 2 Conclusions

This section introduces several concepts that are important for packaging for 5G systems. Several of these concepts will be discussed in much more detail in later sections.

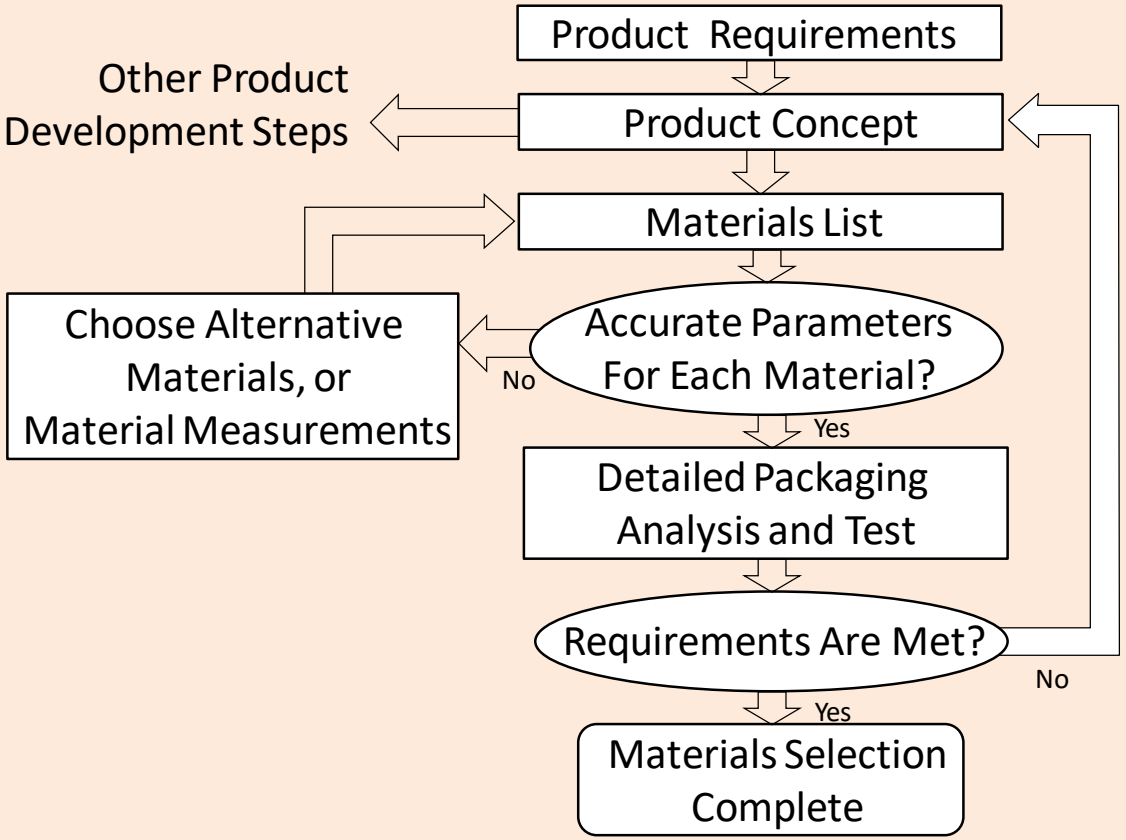
The main transmission line types used for packaging at 5G have been reviewed and design guidelines have been given. The guidelines are to achieve the desired line impedance and to avoid undesired effects such as dispersion.

Package resonances and circuit coupling were are introduced. Skin depth was also discussed along with interconnects and heat dissipation.

Section 3. Materials For 5G

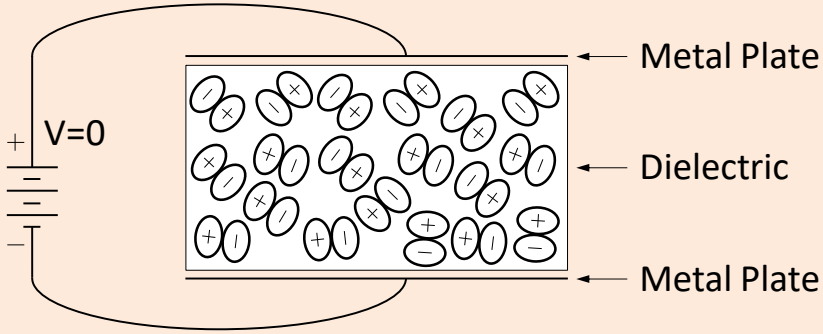
- 3.1 Process For Verification Of Materials Data
- 3.2 Dielectric Constant
- 3.3 Methods To Measure Dielectric Constant
- 3.4 Thermal Conductivity
- 3.5 Thermal Expansion
- 3.6 Ceramics and Fabrication Methods
  - Thin Film
  - Thick Film
  - Co-Fired Ceramics
- 3.7 Basic Printed Circuit Boards and Fabrication

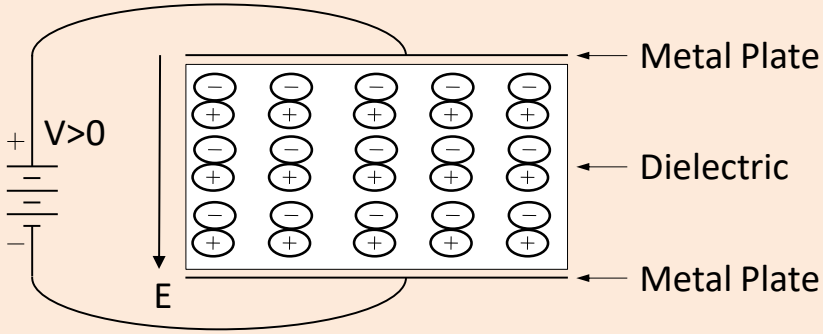
Section 3.1 Selection Of Materials Is A Basic But Essential Step In The Product Development Processes

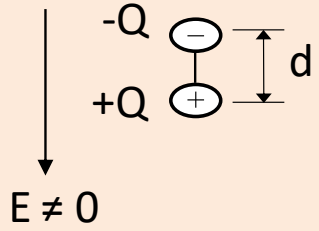


- The goal of the material selection process is to ensure that every material chosen has validated properties that are critical to system value delivery over the full life cycle.
- **<u>Guideline:</u>** Only use materials that have validated parameters.

Section 3.2: Dielectric Constant A Critical Parameter For Microwave And Millimeter-wave Materials







$$D = \varepsilon_0 E + P = \varepsilon_0 E + \varepsilon_0 \chi_e E = \varepsilon_0 \left(1 + \chi_e\right) E$$

But, if we let $\varepsilon_r = (1+\chi_e)$, then we have

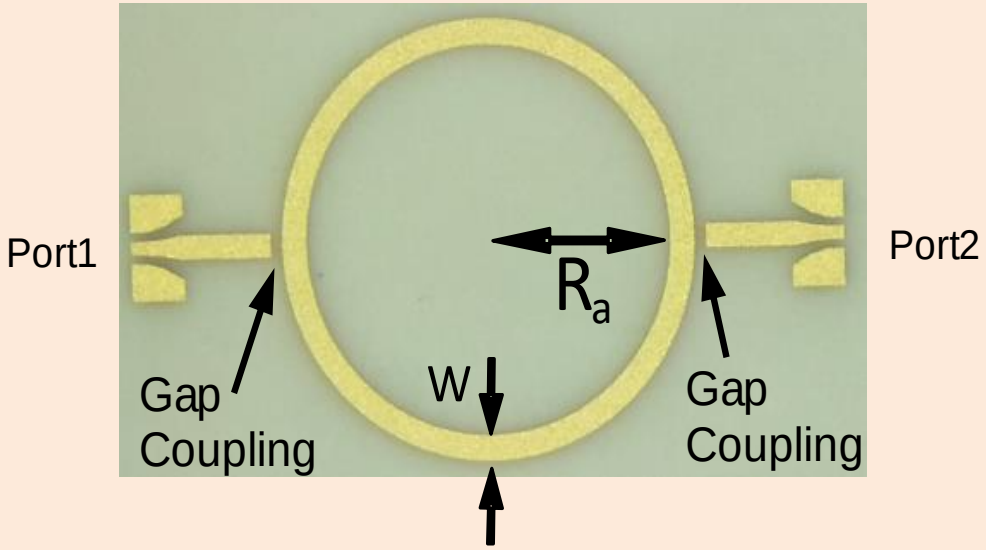
$$D = \varepsilon_0 \varepsilon_r E$$

Dielectric constant is a measure of a material's propensity to generate dipole moments in reaction to the presence of an electric field.

Where:
P = dipole moment density
Q = charge
χ_e = electric susceptibility (how easily dipole moments are generated)
ε = permittivity
ε_r = relative permittivity
ε_0 = permittivity of free space
E = electric field

Section 3.3 Methods To Measure Dielectric Constant

Ring Resonator Is One Method To Measure Dielectric Constant



- The ring resonator method can be used to obtain dielectric constant and an estimate on dielectric loss tangent

Approximations For Resonant Frequency

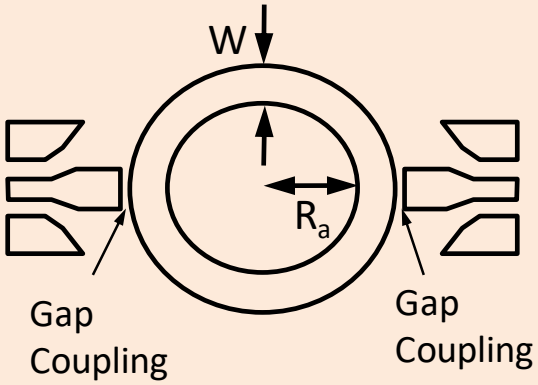
$$f_n = \frac{nc}{2\pi(R_a + \frac{W}{2})\sqrt{\varepsilon_{eff}(f)}}$$

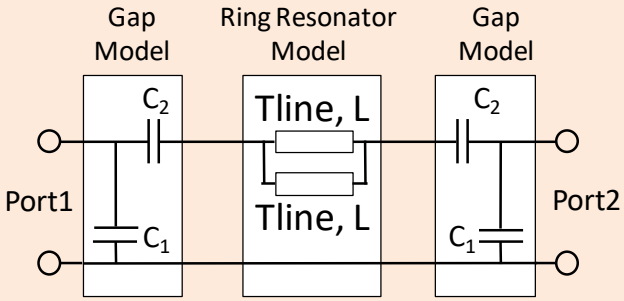
$$\varepsilon_{reff}(f,n) = \frac{nc}{2\pi(R_a + \frac{W}{2})f_n}$$

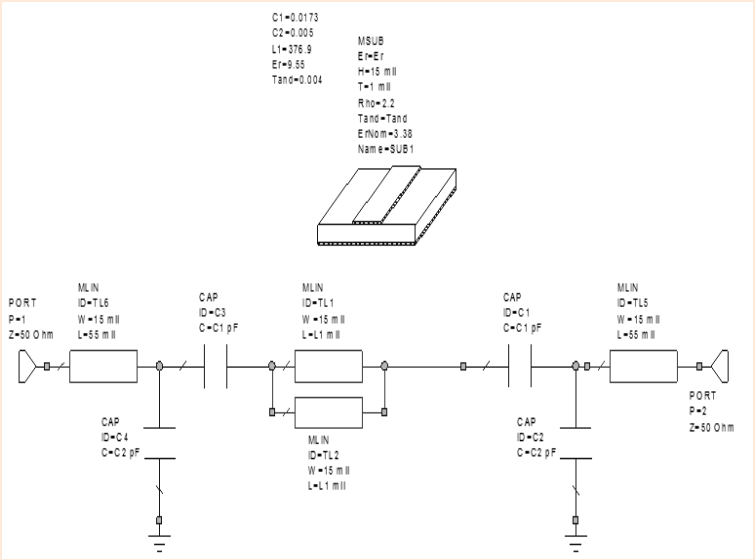
Calculate $\varepsilon_{reff}(f)$ using simulator or available equations

R. Sturdivant, "Materials and Transmission Line Measurements Comparing HTCC and Thick Film Alumina, Presented at 2014 IMAPS RAMP Conference, San Diego, CA.

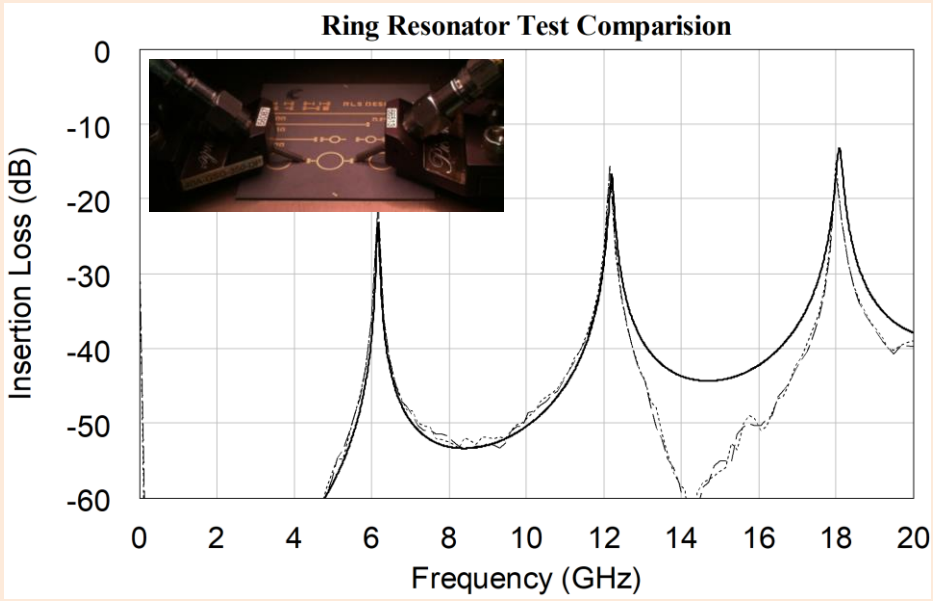
A More Accurate Method Is To Use A Circuit Simulator and Model The Ring Resonator







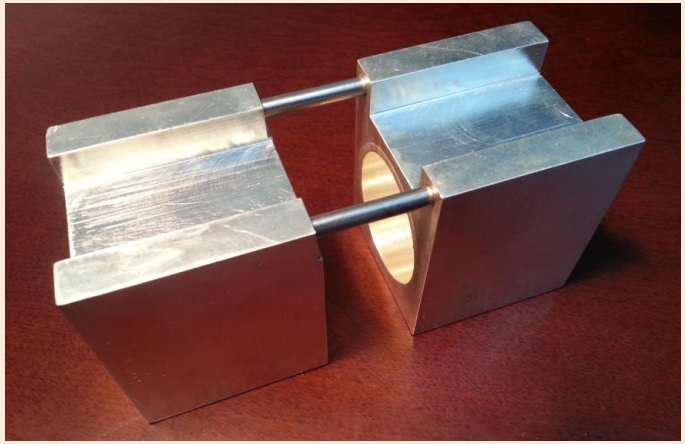
Circuit model for extracting dielectric constant and loss tangent



Measured and modeled data for alumina thick film ring resonator

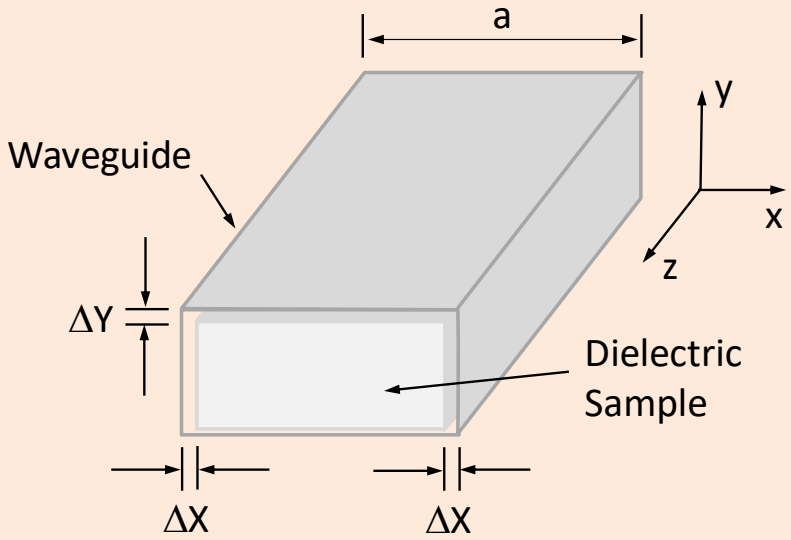
Other Methods To Measure Dielectric Constant and Loss Tangent

Split Cavity Resonator Method



G. Kent, "Non-destructive permittivity measurements of substrates," *IEEE Trans. on Instrumentation and Measurements*, Vol. 45, No. 1, 1996, pp. 102-106.

Filled Waveguide Method

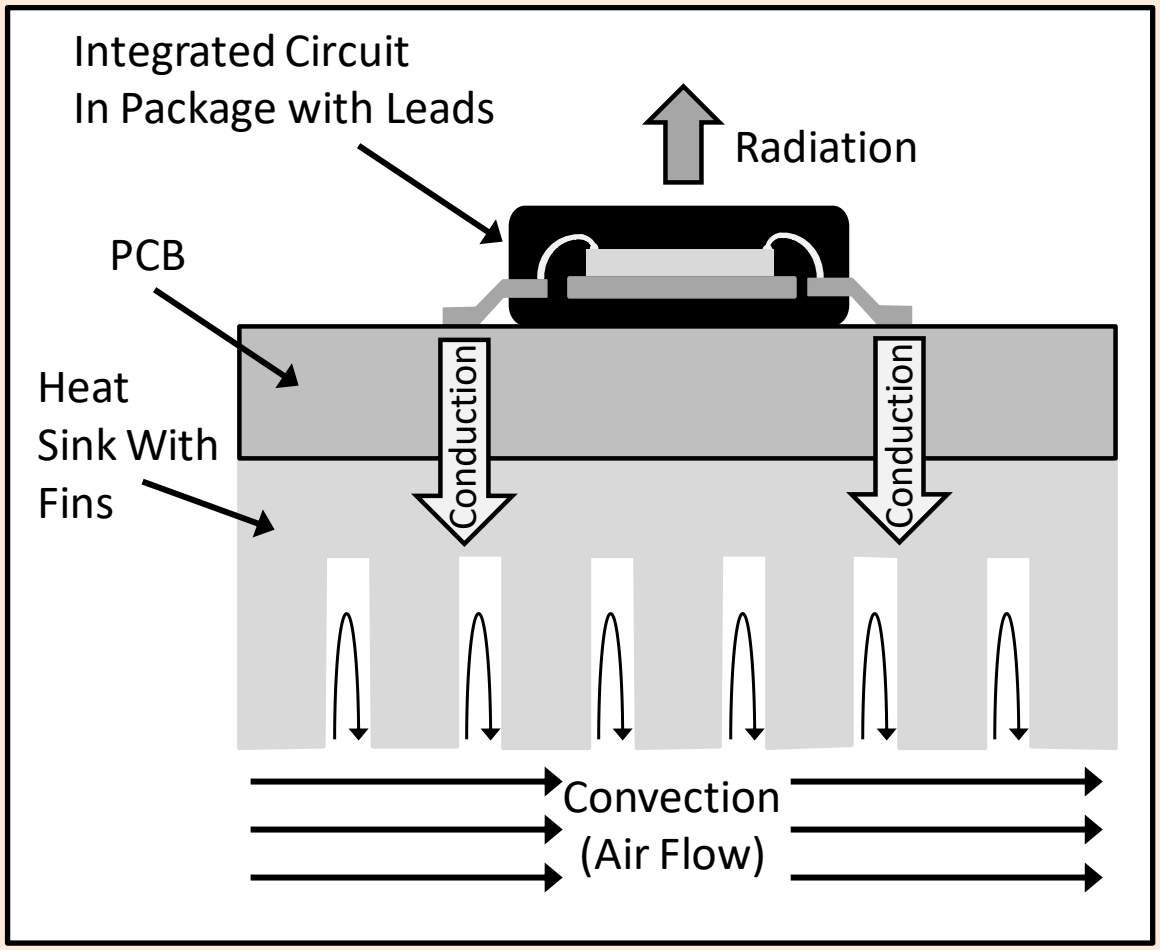


R. Sturdivant, "Millimeter-wave characterization of several substrate materials for automotive applications," in *Proceedings of the IEEE Electrical Performance of Electronic Packaging Conference*, Oct 2-4, 1995, pp. 137-139.

W. Bridges, et. al., "Measurement of the dielectric constant and loss tangent of thallium mixed halide crystals KRS-5 and KRS-6 at 95GHz," *IEEE Trans on Microwave Theory and Techniques*, Vol. 30, No. 3, 1982, pp. 286-292.

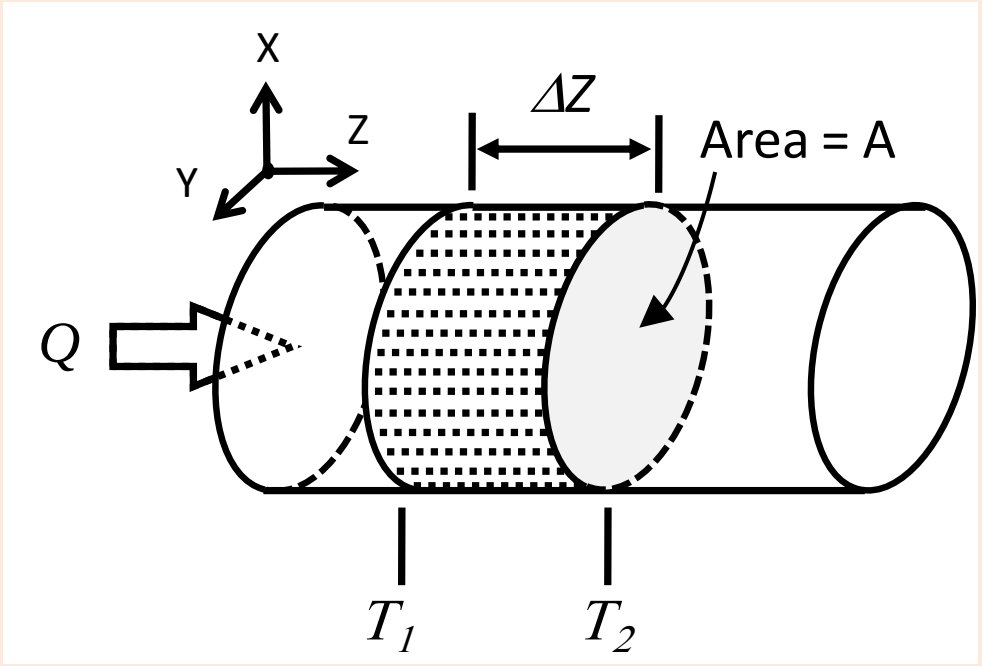
Section 3.4: Thermal Conductivity

Example Of An IC Package Generating Heat Which Is Conducted Away By The Materials



- How is the heat transfer capability of various materials characterized?
- We use thermal conductivity.

Thermal Conductivity Is Measured In W/mK and



$$Q = -kA\frac{\Delta T}{\Delta Z} = -kA\frac{T_2 - T_1}{\Delta Z}$$

$$\Delta T = T_2 - T_1 = \frac{Q\Delta x}{kA}$$

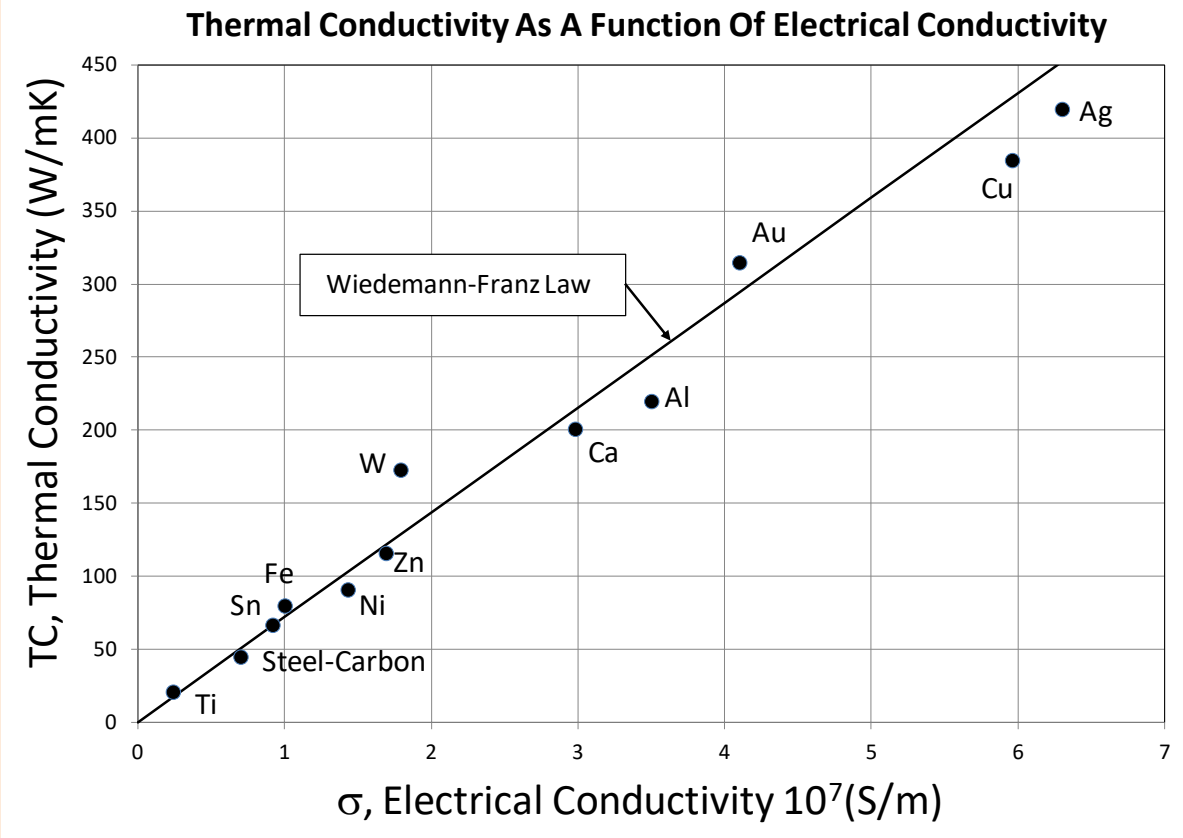
And

$$\text{Heat Flux} = q = \frac{Q}{A} = -k\frac{\Delta T}{\Delta Z}$$

- Jean-Baptiste Fourier (1768-1830) developed the first heat transfer equation.

Where:
Q = heat power (Watts or W)
k = thermal conductivity (W/mK)
A = cross-sectional area of heat flow (m^2)
$\Delta T/\Delta z$ = thermal gradient in the material (K/m)
$\Delta T = T_2 - T_1$ = temperature difference (K)
Δz = thickness of the section of material (m)
q = heat flux (W/m^2)

Thermal Conductivity and Electrical Conductivity Are Related To Each Other

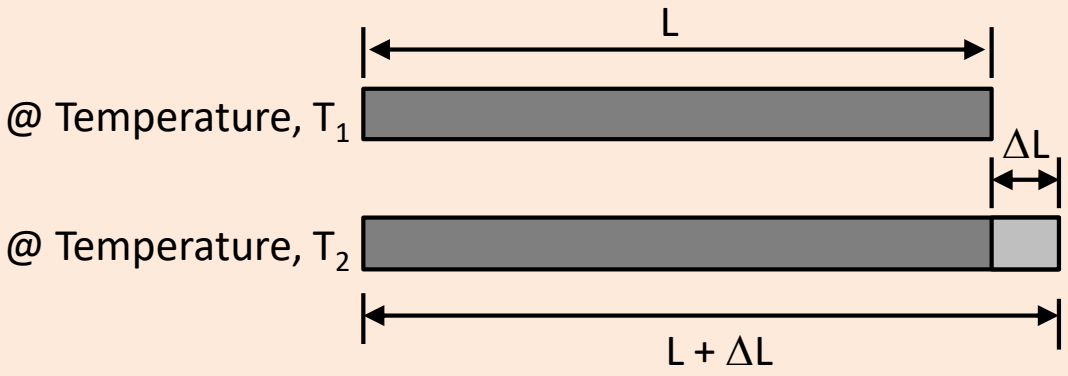


- Thermal conductivity and electrical conductivity in metals result from free electrons.

$$\frac{tc}{\sigma} = LT$$

Where:
tc = Thermal Conductivity
σ = electrical conductivity
L = Lorenz number = 2.45×10^{-8} (W ohm/K^2)
T = Temperature

Section 3.5: Thermal Expansion



- For simple linear expansion, a material changes dimension in one direction as temperature changes.

$$\Delta T = T_2 - T_1$$

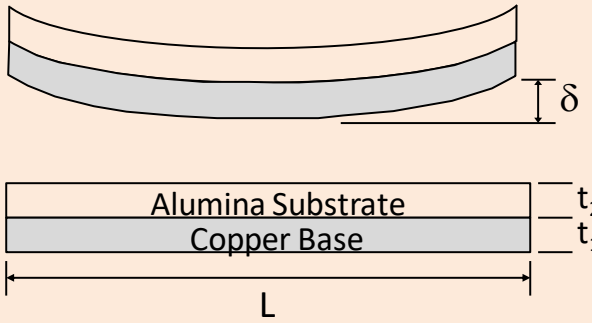
$$\alpha = \frac{1}{L}\frac{\Delta L}{\Delta T} = \frac{1}{L}\frac{\Delta L}{T_2 - T_1}$$

$$\Delta L = \alpha L \Delta T$$

Material	α (ppm/°C)
Aluminum	23.1
Copper	17
GaAs	5.8
Gold	14
Iron	11.8
Alumina Ceramic	7.2

Where:
α = coefficient of thermal expansion (ppm/°C)
ppm = part per million = 10^{-6}
L = length of the sample at temperature T_1
L + ΔL = length of sample at temperature T_2
$\Delta T = T_2 - T_1$ = change in temperature

Effect of CTE Mismatch On Rigidly Attached Materials



Section 3.6: Ceramic Substrates

- Thin Film Ceramics
- Thick Film Ceramics
- Co-Fired Ceramics

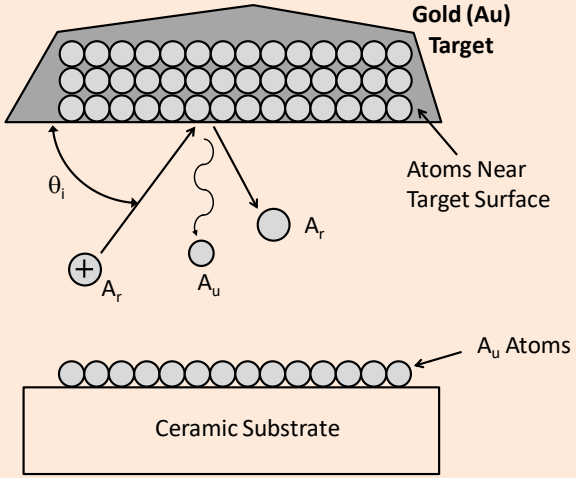
Thin Film Ceramic

Blank Ceramic Substrates

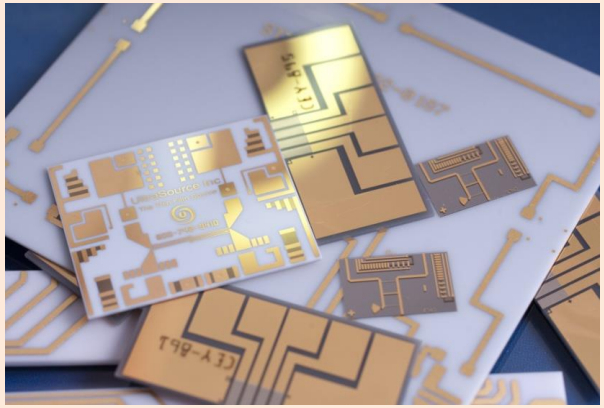
- Start with blank ceramic substrates.
- Sputter with metal layers.
- Chemically etch desired pattern.
- Final substrate has desired pattern.

Sputtering Machine

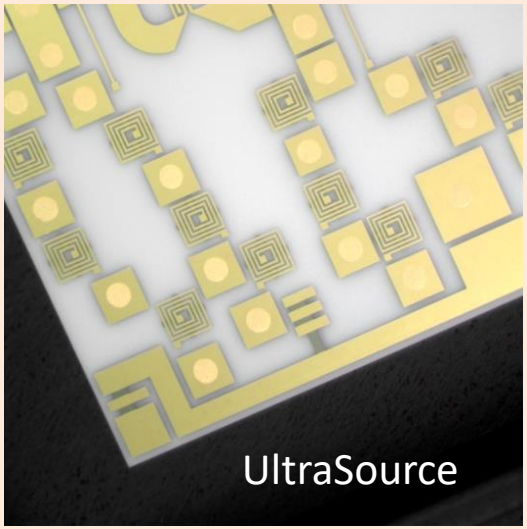
Inside The Sputtering Machine



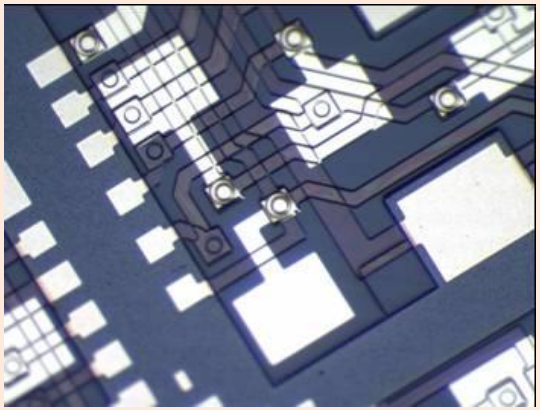
Result Is High Precision Patterned Ceramic

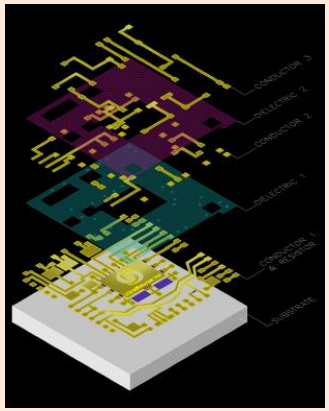


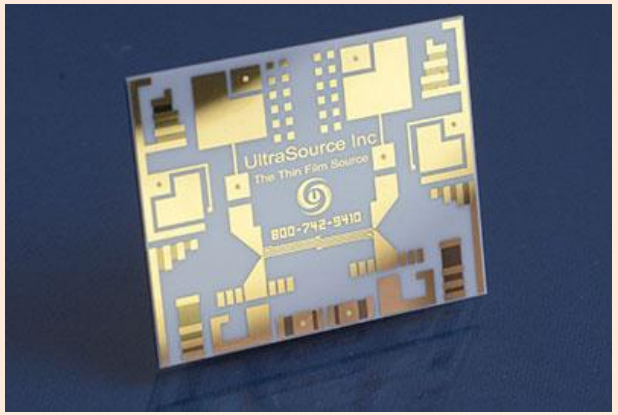
Advanced Thin Film Processes Achieve Sophisticated Ceramic Substrates



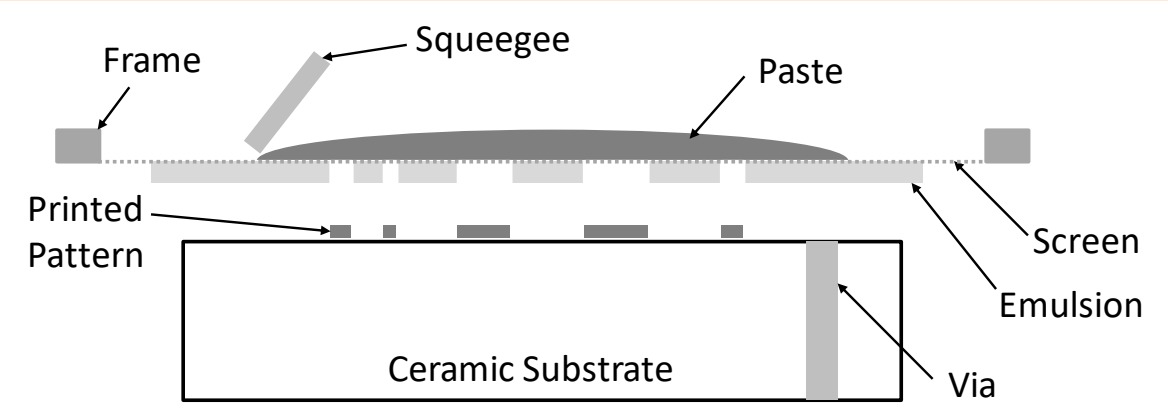
- Integrated capacitors
- Filled vias
- Bridges and Crossovers
- Polyimide multilayer





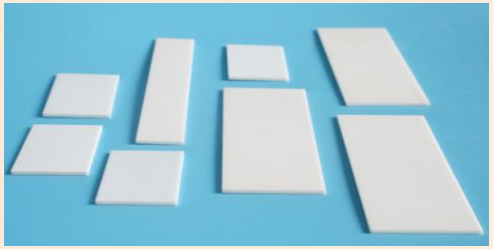


Thick Film Ceramic Is An Additive and Printed Manufacturing Process

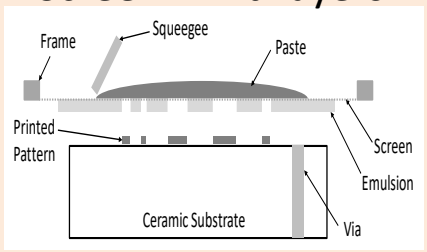


Repeat Print
And Fire To Achieve
Multiple Layers

Blank Ceramic Substrates

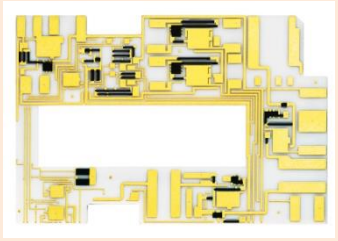


Screen Print Layers



Fire Layers In Belt Oven

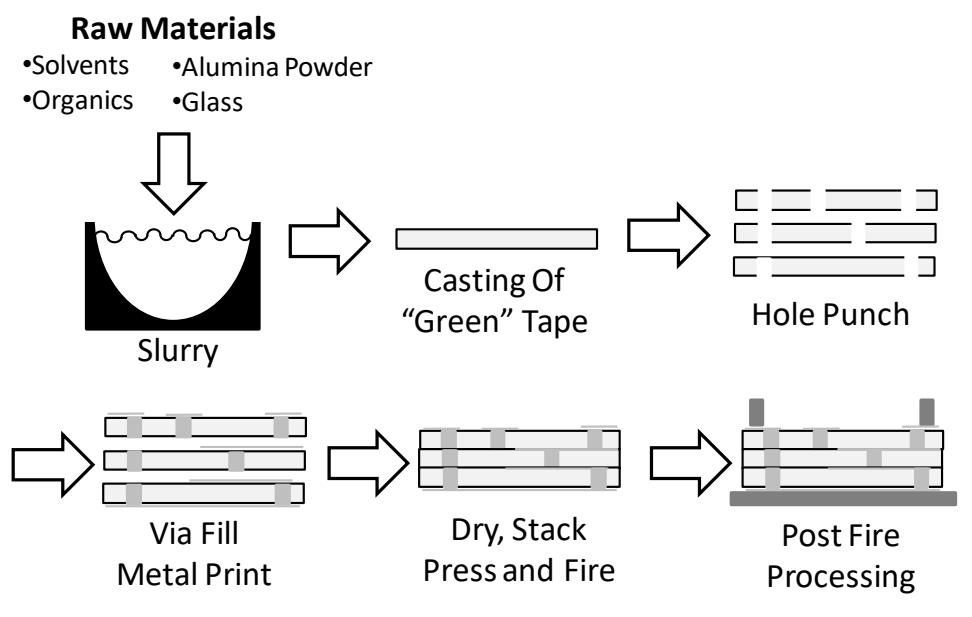
Result Is Thick Film Ceramic



Multi Layer Co-fired Ceramic

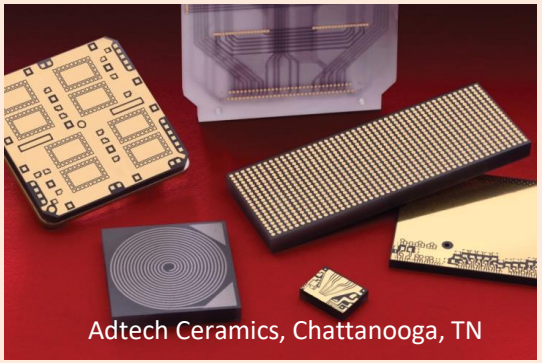
- There are multiple types of materials that are used for co-fired ceramic substrate processing
  - Alumina: Lower cost. Uses refractory metals such as molybdium, or tungsten. Thermal conductivity ~ 25 W/mK, CTE ~ 7ppm/°C
  - Aluminum Nitride: Main features are high thermal conductivity of 120-150 W/mK, CTE ~ 5ppm/°C. Also uses refractory metals.
  - Low Temperature Co-Fired Ceramic (LTCC): Materials have been formulated with relatively low dielectric loss tangent. Can use noble metals such as gold, silver, and copper.

Co-Fired Ceramic Manufacturing Process

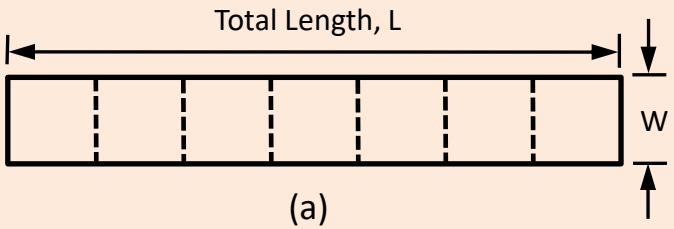


- Fabrication process starts with unfired layers that are punched with holes.
- The holes are filled and metal layers are printed.
- The layers are stacked, dried, and fired at high temperatures.
- Finally, post fire processes such as brazing to metal frames, pins and metal printing/etching.

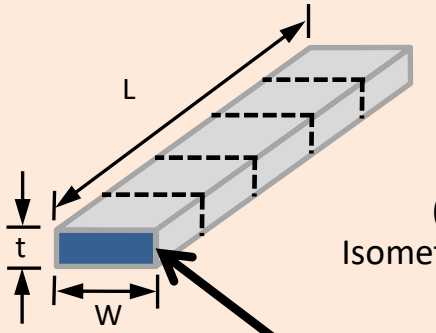

Adtech Ceramics, Chattanooga, TN


Adtech Ceramics, Chattanooga, TN

Co-Fired Ceramic Fabricators Specify Metal Conductivity in Ohm/sq



(a)
Top Down View



(b)
Isometric View

$$Area = A = W\ t$$

- Must convert ohm/sq into resistivity or conductivity for EM simulators.

From Definition Of Resistivity

$$R = \rho \frac{L}{A} = \rho \frac{L}{W\,t}$$

From Ohm/Square

$$R = \left(\frac{Ohm}{Sq}\right)\frac{L}{W}$$

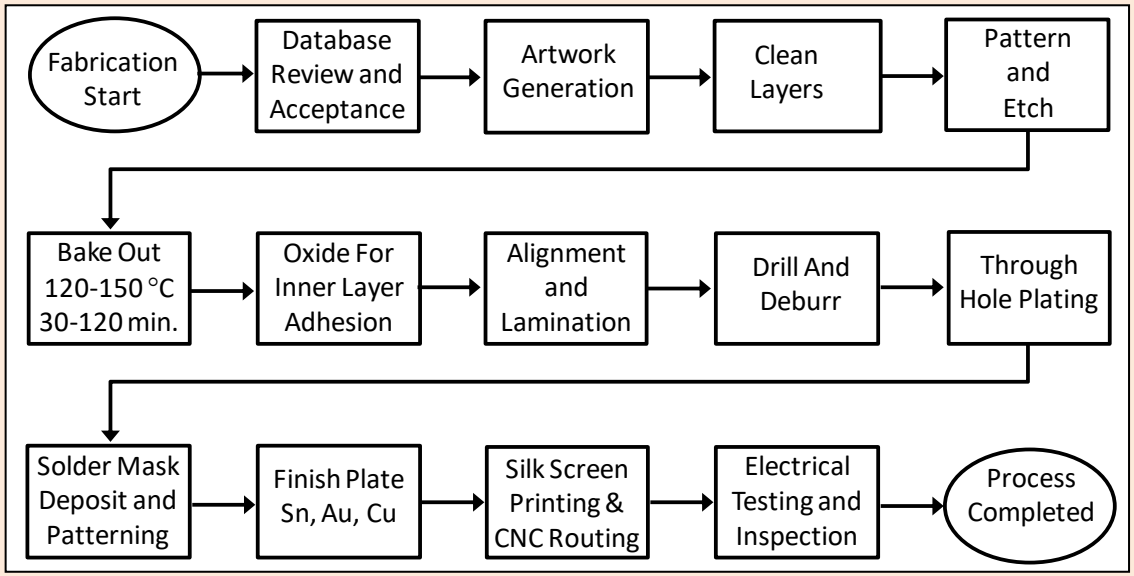
$$\rho \frac{L}{Wt} = \left(\frac{Ohm}{Sq}\right)\frac{L}{W}$$

Use This ρ for EM Simulator Input Data ⇨

$$\rho = \left(\frac{Ohm}{Sq}\right)t$$

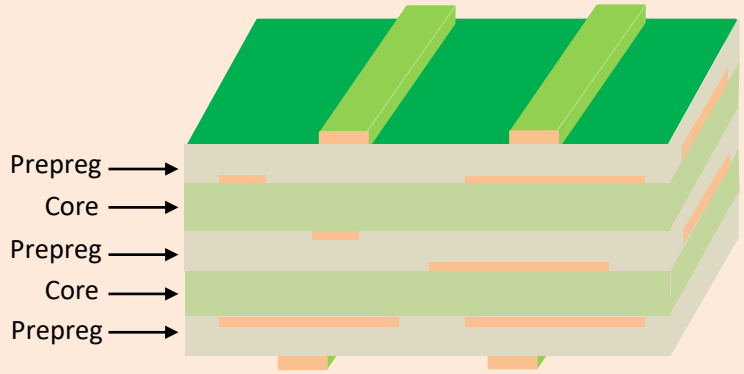
Section 3.7: Printed Circuit Board Fabrication

Simplified PCB Fabrication Process Flow



- Printed circuit boards (PCB) are used for low frequency applications and for microwave and millimeter-wave 5G systems

Image of PCB Showing layers and filled via



Section 3 Conclusions

- Additional concepts have been introduced and more detail presented on the factors affecting packaging for 5G
- Materials were discussed in moderate detail such as
  - Dielectric Constant
  - Methods To Measure Dielectric Constant
  - Thermal Conductivity
  - Thermal Expansion
- Ceramic substrates were briefly discussed
  - Thin Film Ceramics
  - Thick Film Ceramics
  - Co-Fired Ceramics
- Basics of printed circuit boards (PCB) were presented

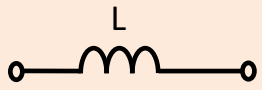
Section 4: Transitions And Interconnects Used In 5G Packaging

- 4.1 Using Wire Bonds For 5G Packaging: Modeling
- 4.2 Using Flip Chips For 5G Packaging: Modeling
- 4.3 Guidelines For Transition Design
- 4.4 Microstrip to Stripline Transition In Ceramic
- 4.5 Microstrip to Stripline Transition In PCB
- 4.6 Effect of Via Conductor Loss
- 4.7 Package to Motherboard Transition Modeling

Section 4.1: Wire Bond Modeling

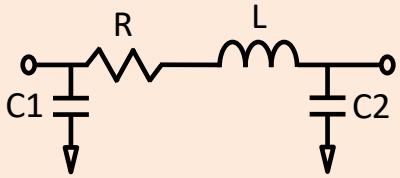
Let's Investigate Modeling The Wire Bond With Progressively Improving Fidelity

Low Fidelity Model



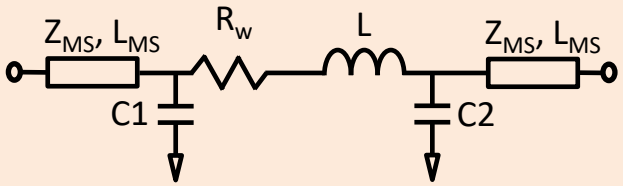
(a)

Moderate Fidelity Model



(b)

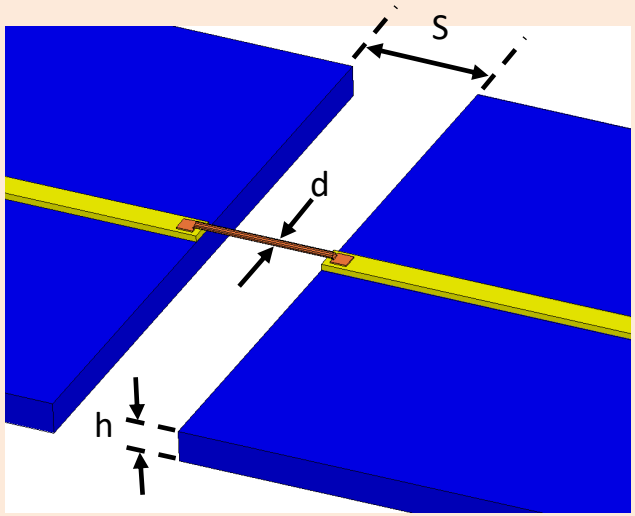
High Fidelity Model

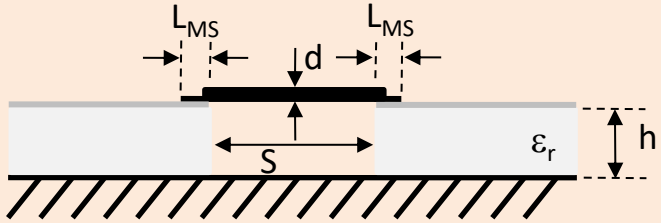


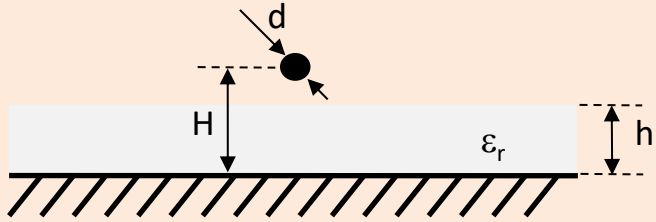
(c)

- Low Fidelity Model: Simple series inductor. Rule of thumb is that 1mm of wire has 1nH of inductance Which slightly over estimates the inductance in many cases, but can still be useful. Useful to a few GHz only.
- Moderate Fidelity Model: Adds shunt capacitance to account for the bond pads and wire shunt capacitance and series resistance of the wire. Useful to 10 GHz or more.
- High Fidelity Model: Adds transmission lines at the input to more accurately account for bond pad effects. Useful to over 50GHz.

Let's Begin The Process Of Developing A Wire Bond Model With A Simplified Wire Bond

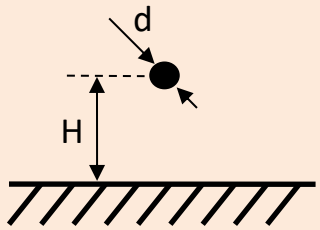




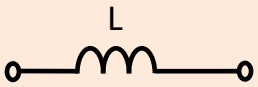


- The image shows a very simple straight wire bond between two substrates. Of course, this is impractical, but let's use it as our first step in developing a wire bond model.

Low Fidelity Model Does Not Accurately Capture The Wire Bond Effects On Phase



Low Fidelity Model

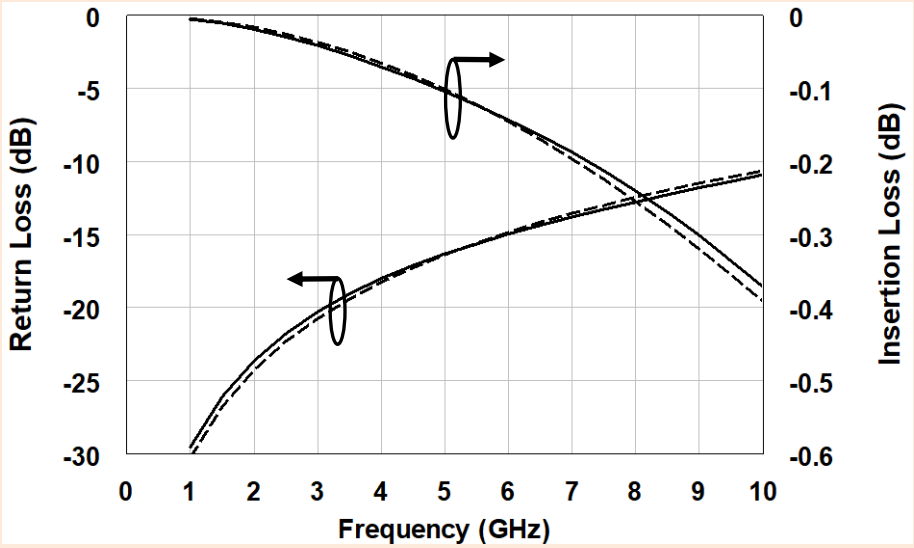


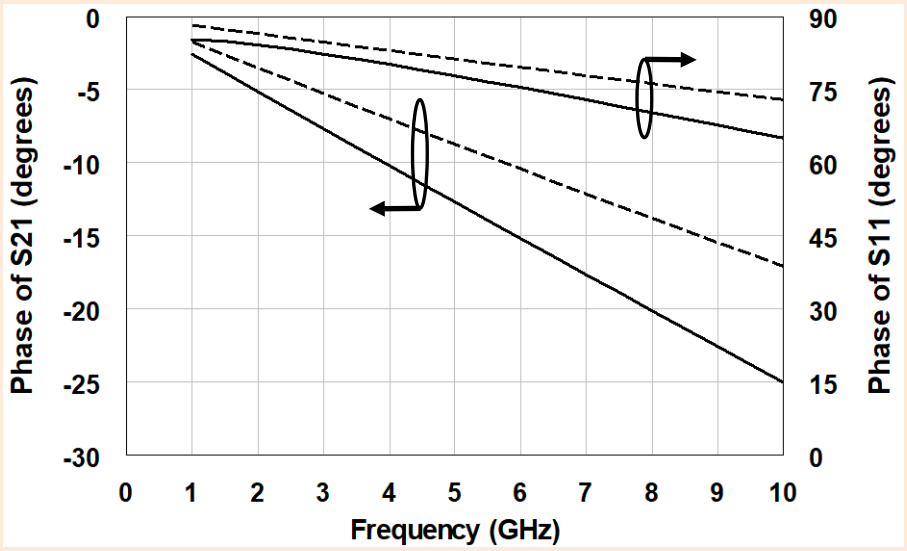
$$L \cong 2\ln\left(\frac{2H}{r}\right) \text{ nH/cm} \qquad (1)$$

Where:

L_g = Inductance of a wire over a ground plane
H = Distance of wire above the ground plane
r = radius of the wire = d/2
Assumes r << H

For H=0.163mm, d=0.0254mm, and a wire length of 0.75mm, L =0.489nH





The High Fidelity Model Treats The Wire As A Transmission Line For Calculating L, C1 and C2

Step 1: Treat wire bond as a transmission line and calculate its line impedance

$$Z_{ow} = \frac{60}{\sqrt{\varepsilon_{reff}}} \cosh^{-1}\left(\frac{1-u^2}{2R} + \frac{R}{2}\right) \quad (2)$$

Where:

$$R = \frac{2}{(4H/a - a/H)} \quad (2a) \qquad u = \frac{1}{(2H/a)^2 - 1} \quad (2b)$$

$$\varepsilon_{reff} = \frac{\ln\left(\frac{2H}{a}\right)}{\ln\left[\frac{2(H-h)}{a} + \frac{2h}{a\varepsilon_r}\right]} \quad (2c)$$

Step 2: Calculate L, C1, C2, R

$$L_{dist} = \frac{Z_{ow}\sqrt{\varepsilon_{reff}}}{v_o} \quad (3a)$$

$$C_{dist} = \frac{\sqrt{\varepsilon_{reff}}}{Z_{ow} v_o} \quad (3b)$$

$$L = L_{dist} \cdot \text{Wire Length} \quad (3c)$$

$$C1 = C2 = \frac{C_{dist} \cdot \text{Wire Lenght}}{2} \quad (3d)$$

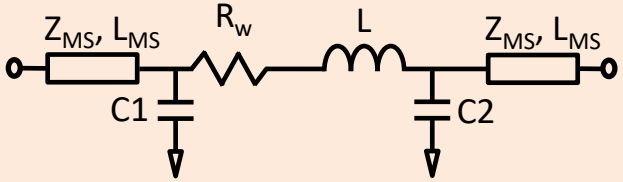
$$R_W = R_{DC} = \frac{\text{Wire length}}{\sigma A} \quad (3e)$$

Step 3: Calculate Z_{MS}, L_{MS}

Use any available transmission line simulator to calculate the impedance of the wire bond pad. Z_{MS} = wire bond pad line impedance, L_{MS}=wire bond pad length.

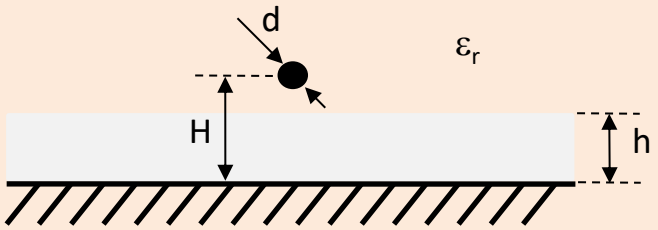
Where:

Z_{ow} = impedance of the wire bond over a grounded dielectric slab
a = d/2 = r = radius of the wire bond
L_{dist} = distributed inductance (H/m)
C_{dist} = distributed capacitance (F/m)
H = height of the wire bond
h = height of the substrate
e_{reff} = effective dielectric constant of the wire transmission line
e_r = dielectric constant of a substrate between the wire bond and ground
v_o = velocity of light in a vacuum
σ = conductivity of the wire
A = wire bond cross-sectional area = πr^2
Wire Length = 0.75mm

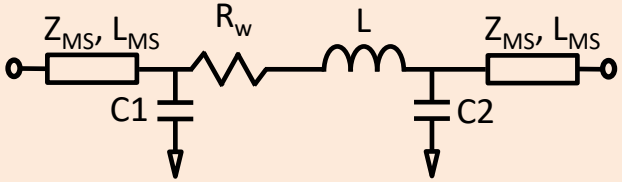


For a gold wire (σ=4.1x10^7 mho/m) with H=0.163mm, d=0.0254mm, and a wire length of 0.75mm, From Equations 2-4, we obtain: L_{dist}=651.9nH/m, L=0.489nH, C_{dist}=17.04pF/m, C1=C2=0.0064pF, Rw=0.036ohm.

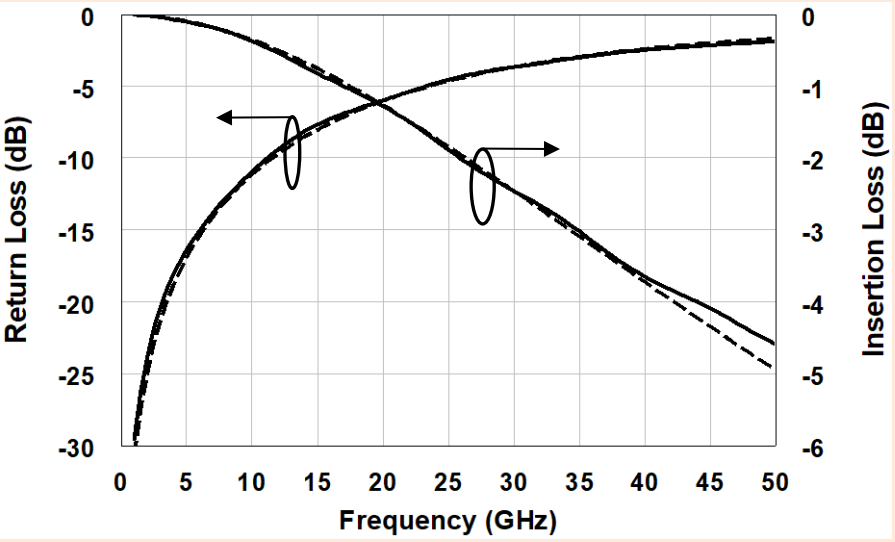
The High Fidelity Model Results In Excellent Agreement

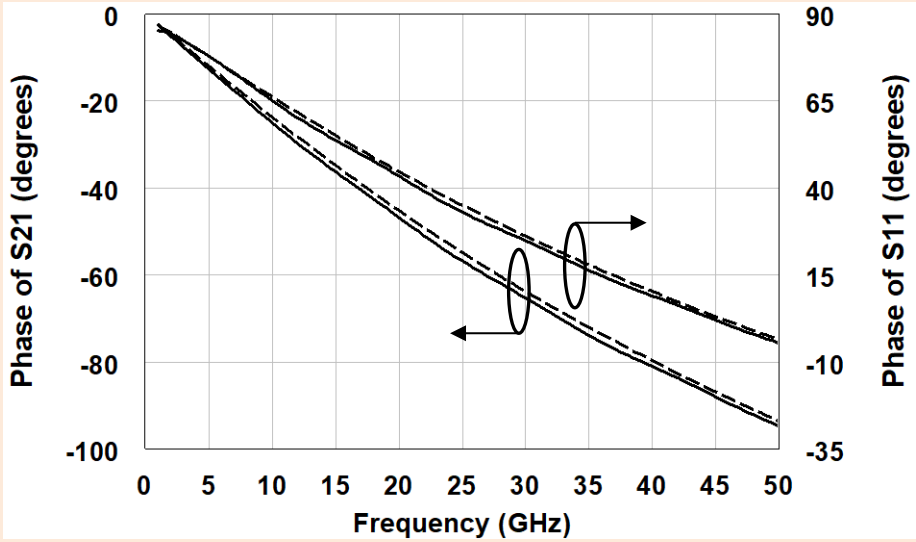


High Fidelity Model

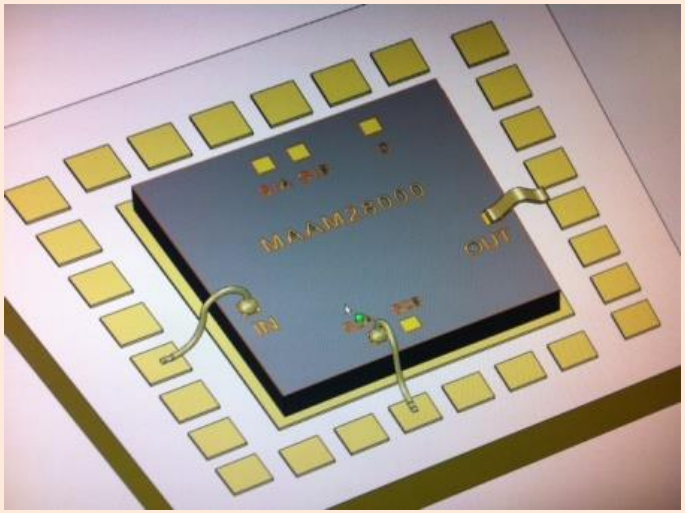


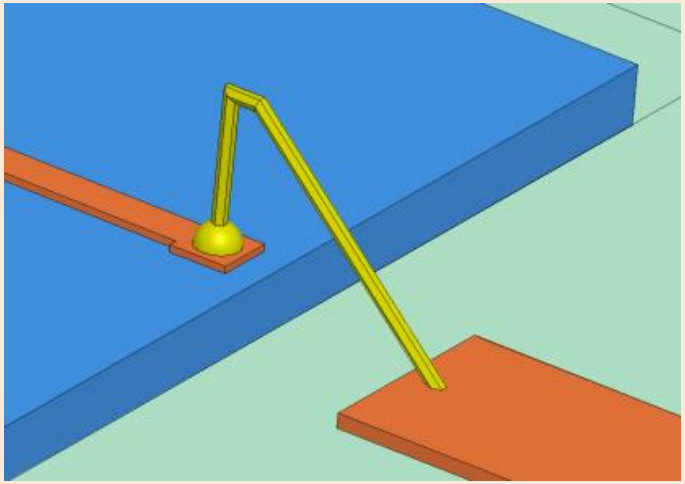
L = 0.489nH
C1 = C2 = 0.0064pF
R = 0.036 ohm
L_{MS} = 0.090 mm
Z_{MS} = 50.2 ohms (ε_{reff} = 6.01)





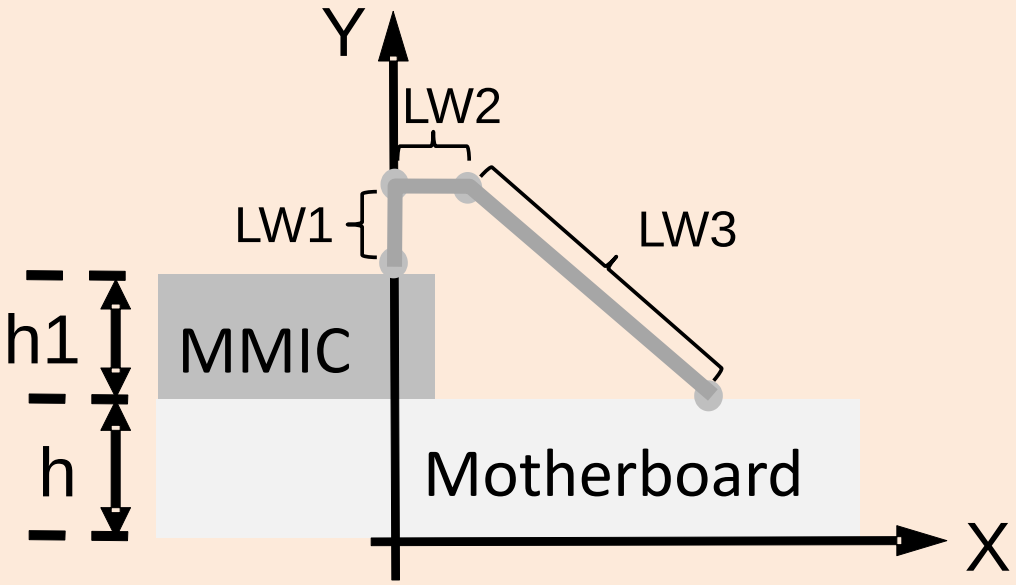
However, One May Rightly Object That This Wire Bond Model Up To This Point Is For A Simplified Unpractical Case

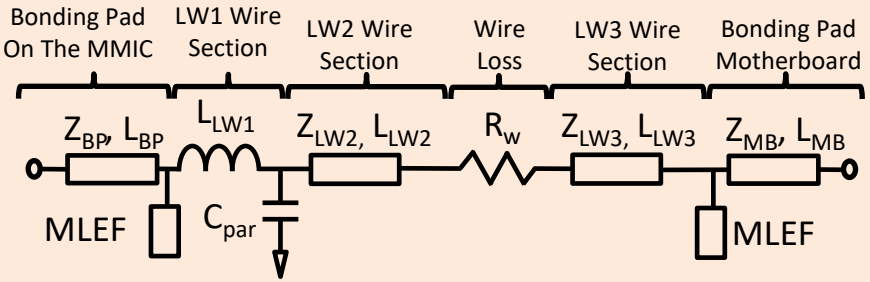




- This is a valid criticism, but the value of the prior analysis is that it demonstrates the method of wire bond analysis.
- A more complex and practical wire bond mode is shown to the left.
- It shows a GaAs MMIC integrated circuit wire bonded to a package using ball bonds and a ribbon bond.
- Also shown is a 3D model of the ball bond used for our electrical simulations.

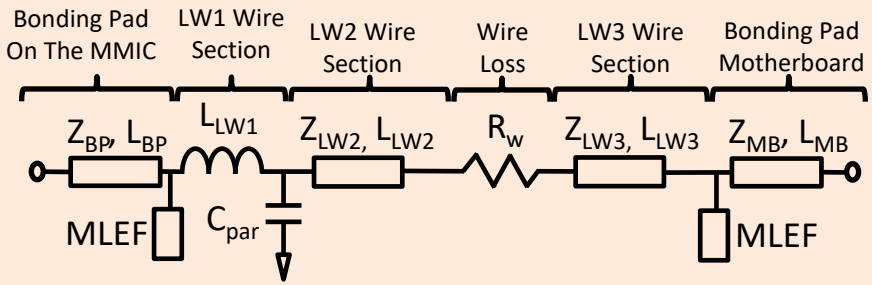
The Electrical Model For The Practical Wire Bond Contains Additional Circuit Elements



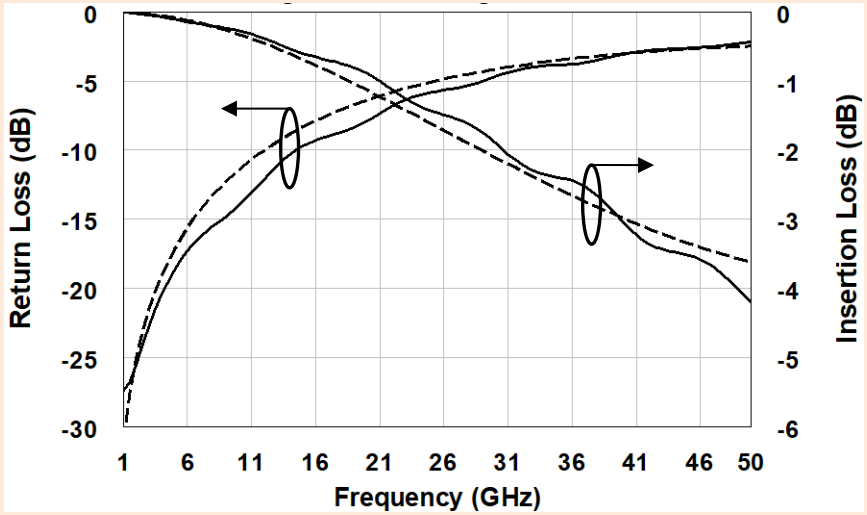


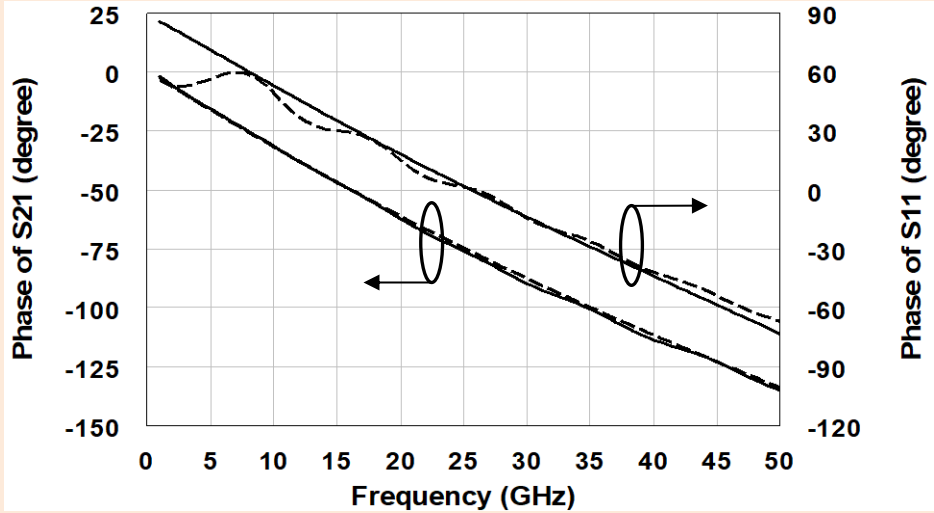
- The wire bond is approximated by three sections of wire. Each section is analyzed to determine its line impedance.
- LW1 is modeled as a lumped inductor (with C_{par}=0).
- LW2 and LW3 are modeled as sections of transmission line using equations 2-3.

The High Fidelity Model Applied To A Practical Wire Bond Shows Agreement To 50GHz



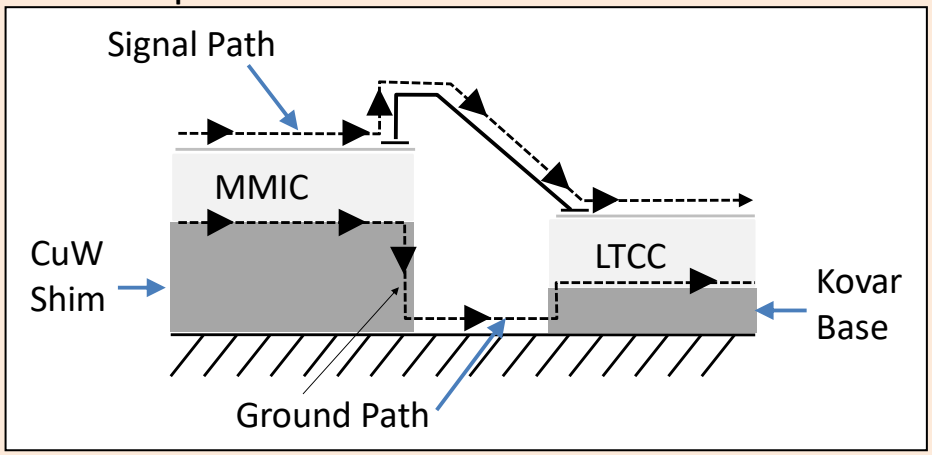
L_{LW1} = 0.135nH
Z_{LW2} = 267.9 ohm
$E_{reff(LW2)}$ = 1.092
$Length_{LW2}$ = 0.051mm
Z_{LW3} = 235.2 ohm
$E_{reff(LW3)}$ = 1.168
$Length_{LW3}$ = 0.503mm
L_{MS} = 0.090 mm
Z_{MS} = 50.2 ohms (e_{reff} = 6.01



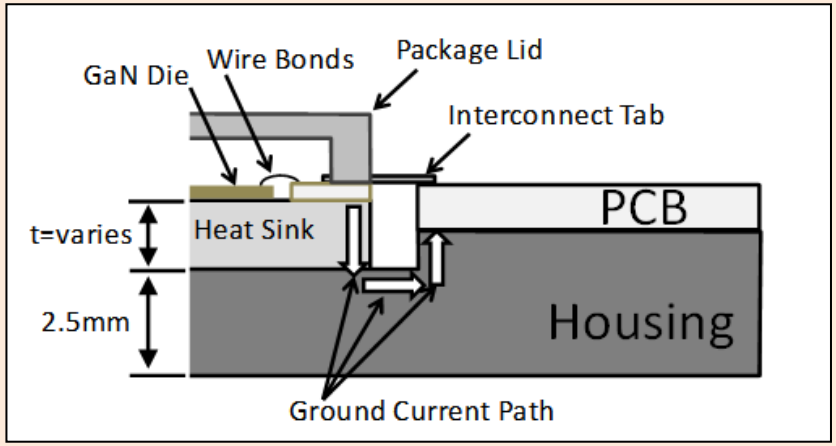


Ground Path Inductance In Wire Bond Transitions And Other Interconnects Can Be A Significant Issue For 5G Packaging

Example 1: Wire bond Ground Current



Example 2: Package Mount To PCB Ground Current

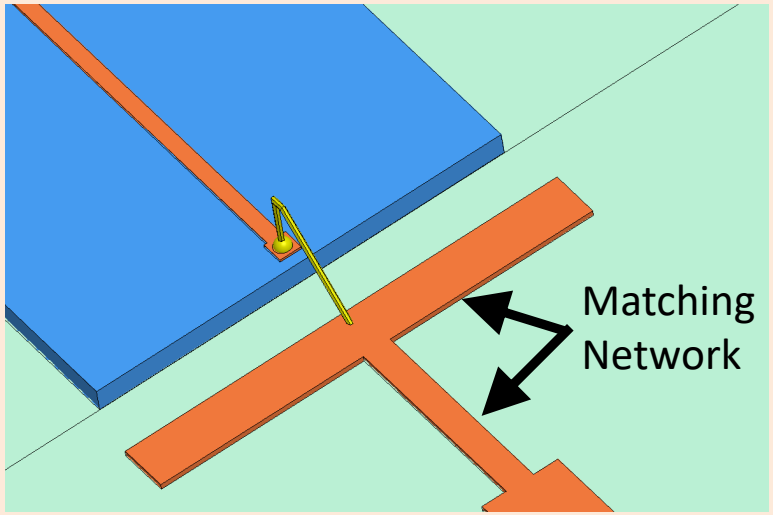


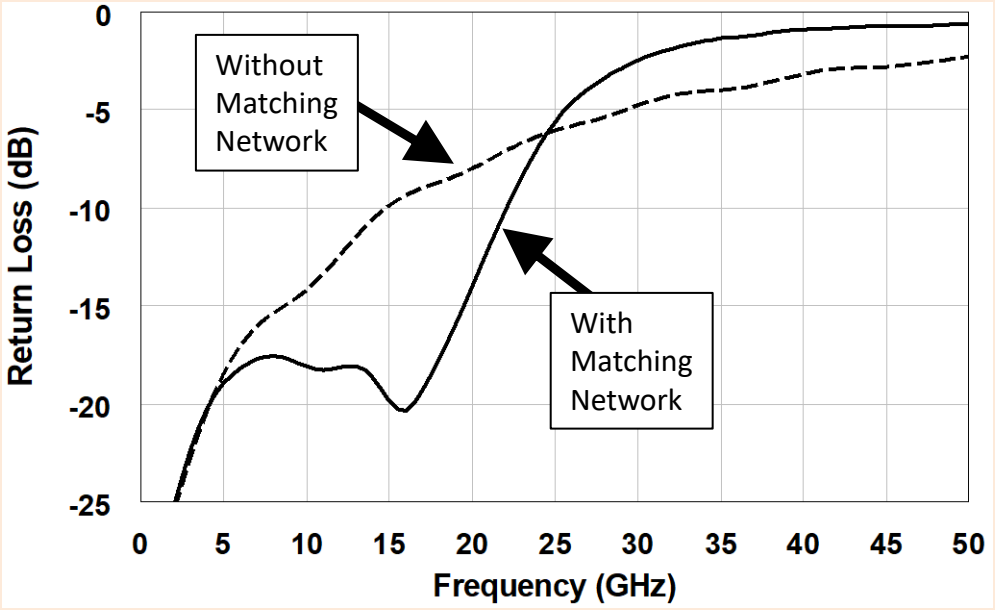
- If the ground return path is longer than the signal path, then it introduces an inductive effect.
- It has essentially the same effect as a series inductor and reduces the bandwidth.

R. Sturdivant, A. Bogdon, E.K.P. Chong, "Balancing thermal and electrical packaging requirements for GaN microwave and millimeter-wave high power amplifier modules," *Journal of Electronics Cooling and Thermal Control*, No. 7, pp. 1-7.

One Method To Overcome The Inductance Of The Wire Bond And Ground Plane Inductance Is To Use A Matching Network

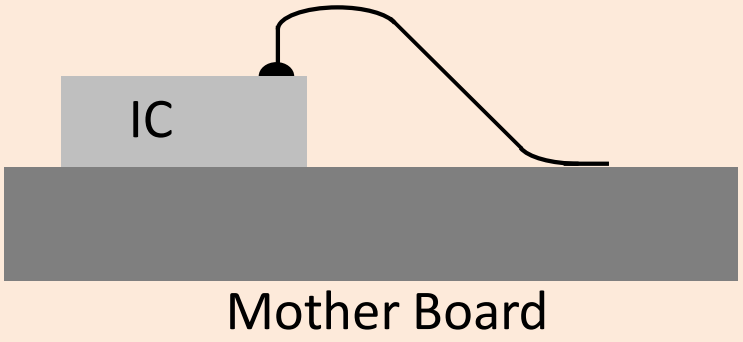
HFSS Simulation Model

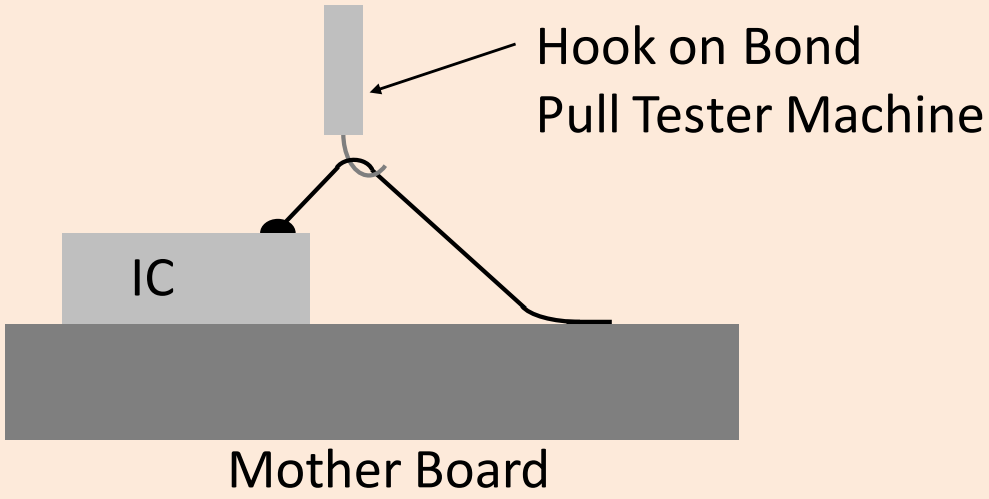




- The matching network increased the bandwidth from 9GHz to nearly 20GHz (using -15dB return loss as the bandwidth specification)

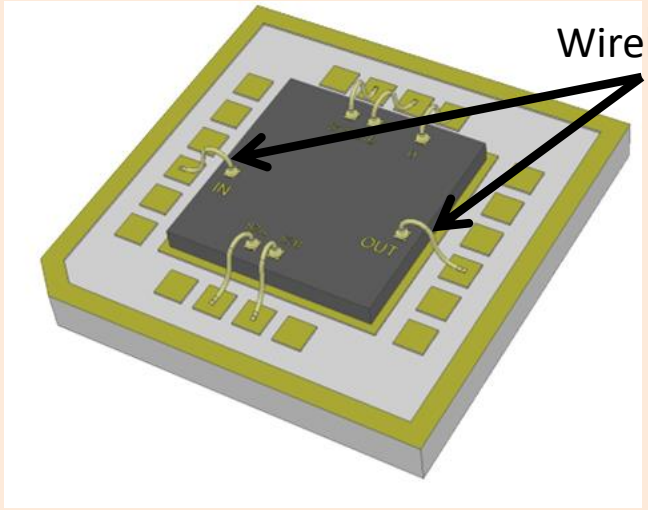
Wire Bond Reliability and The Bond Pull Test

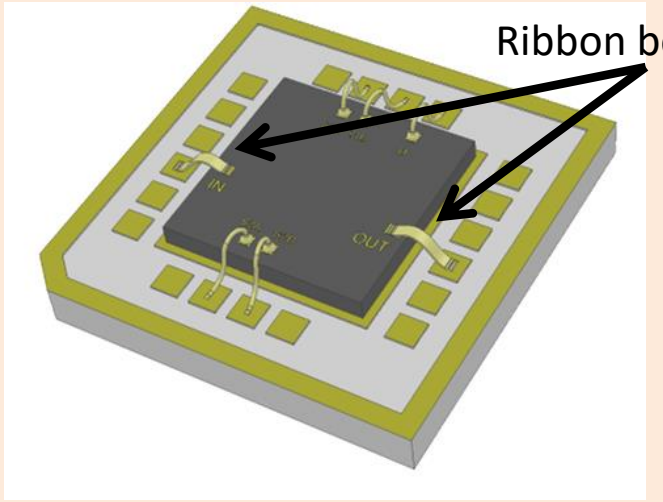




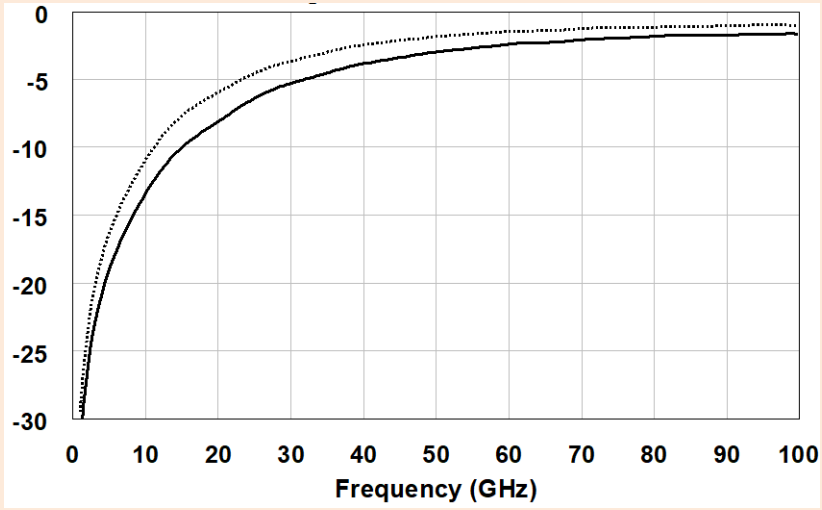
- MIL-STD-883 Method 2011.7 is used as a procedure for testing the bond strength of wire bonds.
- Typical specifications for wire bonds are a minimum of 3g pull strength for 25.4um gold wire.

Ribbon Bonds Compared To Wire Bonds



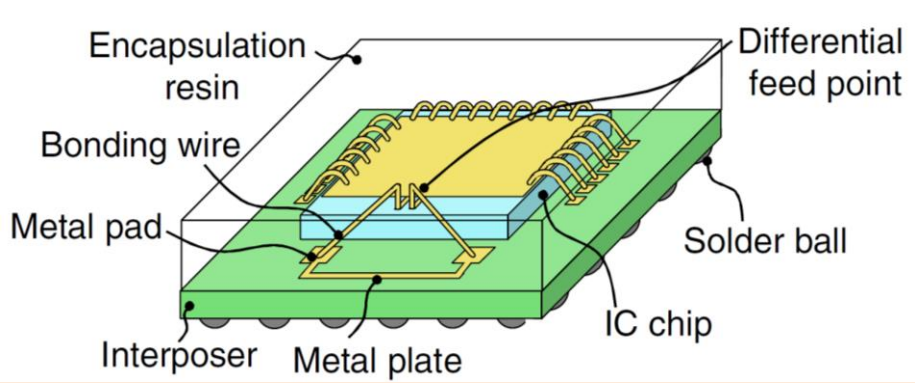


HFSS Simulation Of Return Loss 25.4um wire and 76.2um x 12.5um ribbon bond



- Simulations how a nominal benefit from using ribbon versus wire bonds

Wire Bonds Can Radiate and Have Limited Bandwidth

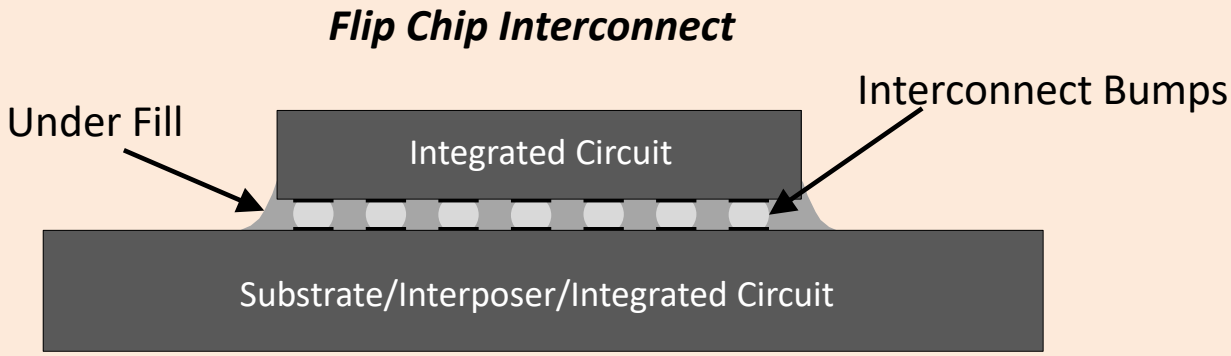


Example of wire bonds used as part of the antenna in a 60GHz package

- Wire bonds can radiate as antennas which can be a significant drawback at millimeter-wave frequencies.
- However, wire bonds radiation can be purposely used as an antenna as in the package show.
- An alternative is to use flip chip interconnects.

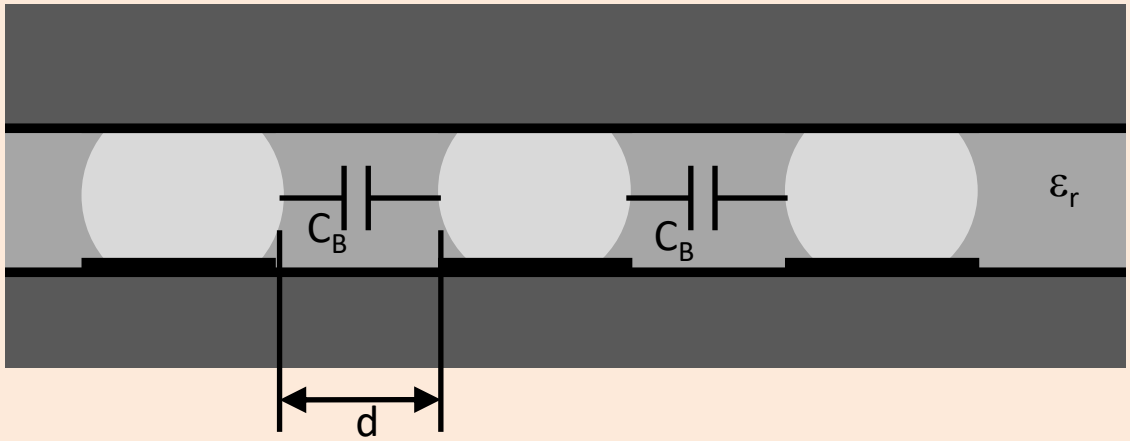
Y. Ysutsumi, et. al., "Bonding wire loop antenna in standard ball grid array package for 60GHz short-range wireless communications," IEE Trans. on Antennas and Propagation, Vol. 61, No. 4, 2013, pp. 1557-1563.

Section 4.2: Flip Chip Interconnect



- Interconnects can be made using multiple methods.
- The underfill material improves long term reliability of the solder bump connections
- For millimeter-wave and very high speed applications, underfill is frequently not used.

Why Does The Underfill Material Reduce The Bandwidth Of Solder Bump Interconnects?

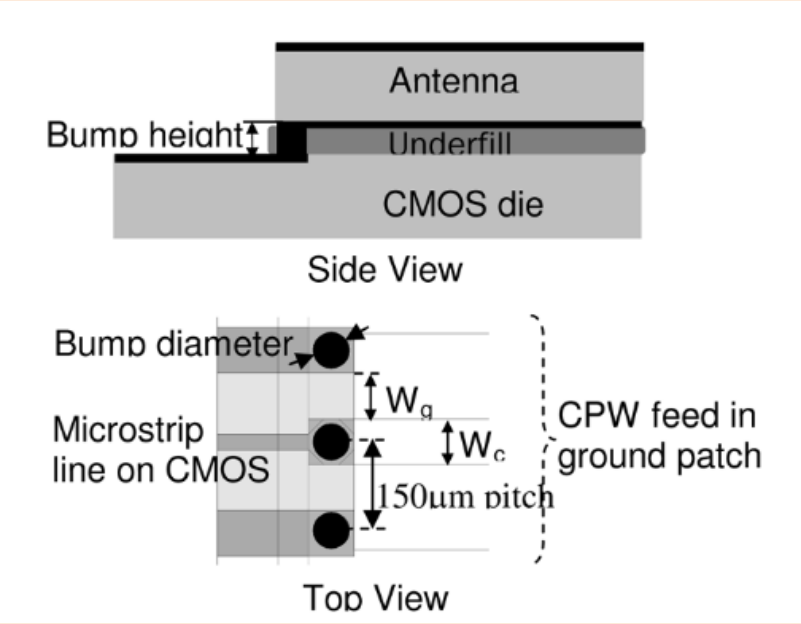


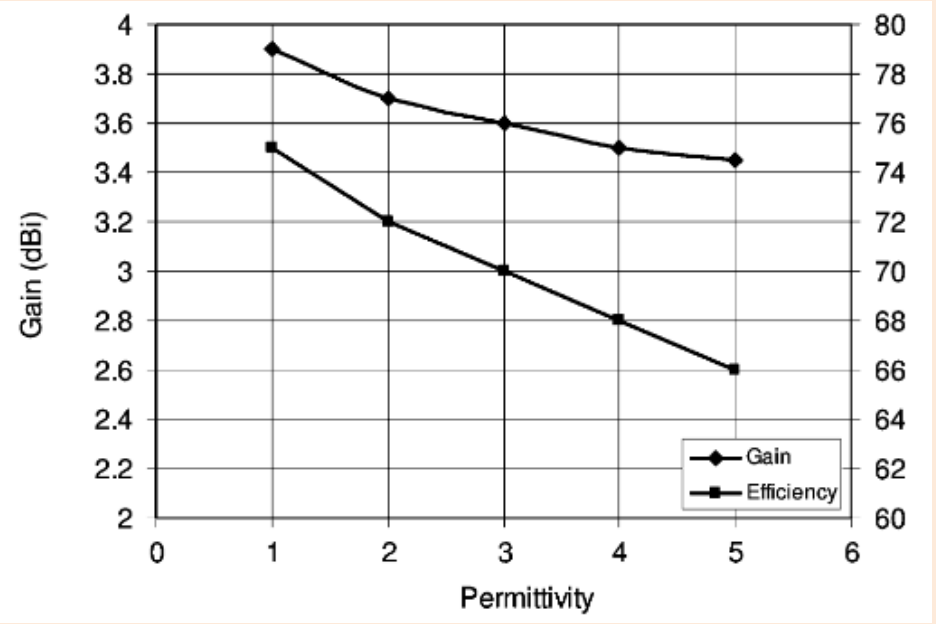
- Reason 1: The capacitance between ball contacts increases when uderfill material is used.
- Reason 2: The underfill material will have a dielectric loss tangent that will increase the insertion loss of the transition.

Using a parallel plate approximation

$$C_B = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

Example: Effect of Underfill Material Reduces The Gain of Antenna

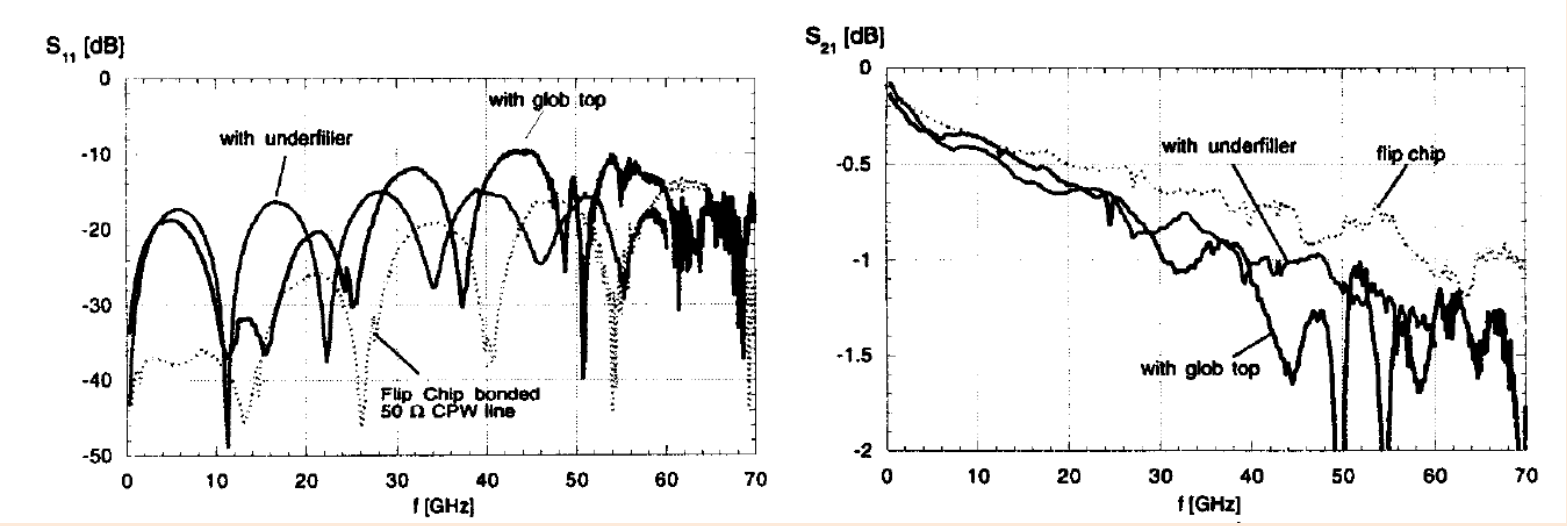




- Gain and efficiency decrease as the relative permittivity of the under fill is increased

Source: G. Felic, S. Skafidas, "Flip-chip interconnect effects on 60GHz microstrip antenna performance," *IEEE Antennas And Wireless Propagation Letters*, Vol. 8, 2009.

Example: Underfill Material Can Increase Insertion Loss and Cause Impedance Mismatch

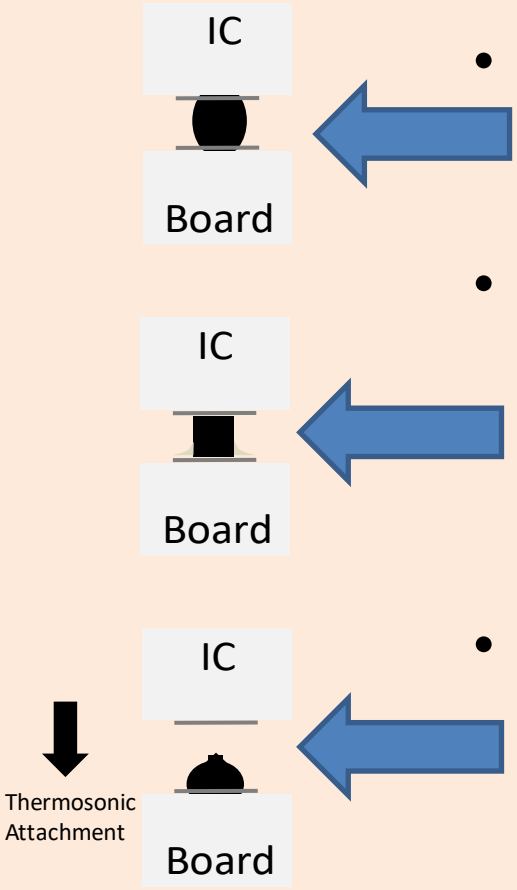


	without underfill	with undefill tan(δε)=0	with undefill tan(δε)=0.005
β/β0 @ 1 GHz	2.380	2.676	
α (dB/mm) @ 1 GHz	0.026	0.029	
Real(Z) [Ω] @ 1 GHz	49.8	44.2	
β/β0 @ 50 GHz	2.309	2.593	2.593
α (dB/mm) @ 50 GHz	0.146	0.165	0.181
Real(Z) [Ω] @ 50 GHz	47.9	42.8	42.8

- The dielectric loading caused by the underfill increases the capacitance at the ball interconnect.
- This causes impedance mismatch.
- The loss tangent of the dielectric material also causes losses.
- However, it is possible to design the structures to account for the underfill and to choose low loss tangent underfill.

Source: G. Baumann, et. al., "Evaluation of glob top and underfill encapsulanted active and passive structures for millimeter wave applications," European Microwave Conference, Jerusalem, Israel, Sept 8-12, 1997.
See Also: L. Hsu, "Design of flip-chip interconnect using epoxy-based underfill up to V-band frequencies with excellent reliability," IEEE Trans. Microwave Theory and Tech., Vol. 58, No. 8, Aug, 2010, pp. 2244-2250.

Flip Chip Interconnects For 5G Packaging
Three Fabrication Methods



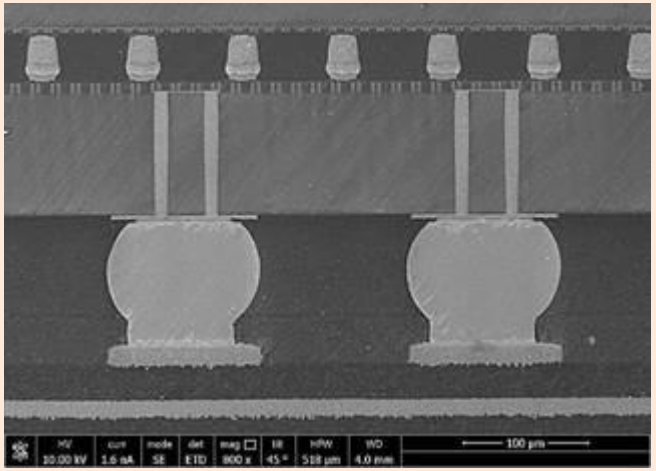
- **<u>Solder Bumps:</u>** The most common method is the Controlled Collapse Chip Connect (C4) process developed by IBM.
- **<u>Hard Bumps:</u>** The bump is constructed from copper, silver, or gold posts that are plated to the surface of the integrated circuit at the interconnect sites. The bumps are then solder to the motherboard.
- **<u>Thermosonic Ball Bumps:</u>** Ball bumps are placed on the IC at the interconnect sites. The IC is attached to the motherboard using thermosonic attach. Also called stud bumping. Bumps can also be Cu with solder.

E. J. Rymaszewski, J. L. Walsh, and G. W. Leehan, "Semiconductor Logic Technology in IBM" *IBM Journal of Research and Development*, 25, no. 5 (September 1981): 605.
Hard Bumps: See companies such as TLMI which provide gold bumps, copper, and indium hard bumps

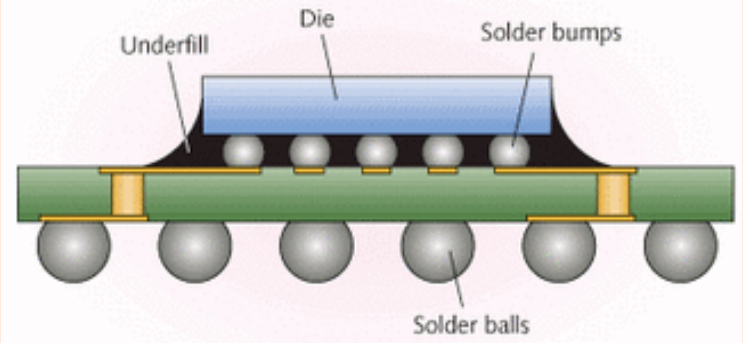
Board

Solder Bump Fabrication

Solder bumps and interposer layer



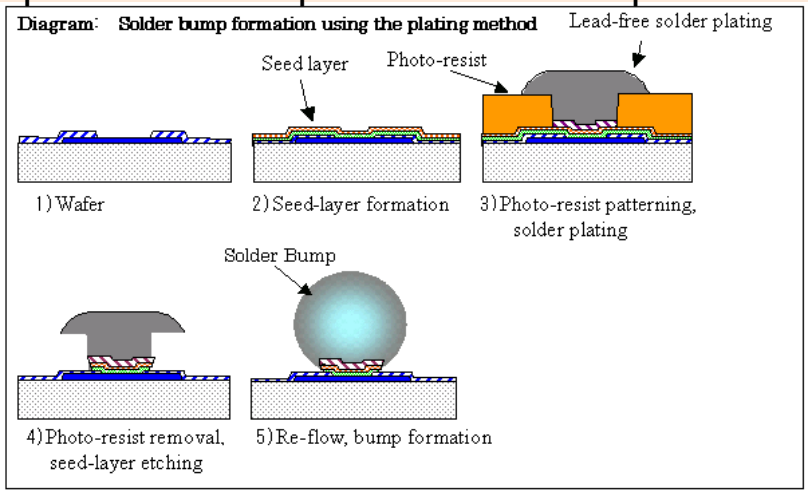
Source: Amkor Technology



W. Herbst, "The back-end process: Step 5—Flip chip attach process and material options," Solid State Technology (http://electroiq.com)

- The underfill material improves long term reliability of the solder bump connections
- For millimeter-wave and very high speed applications, underfill is frequently not used.

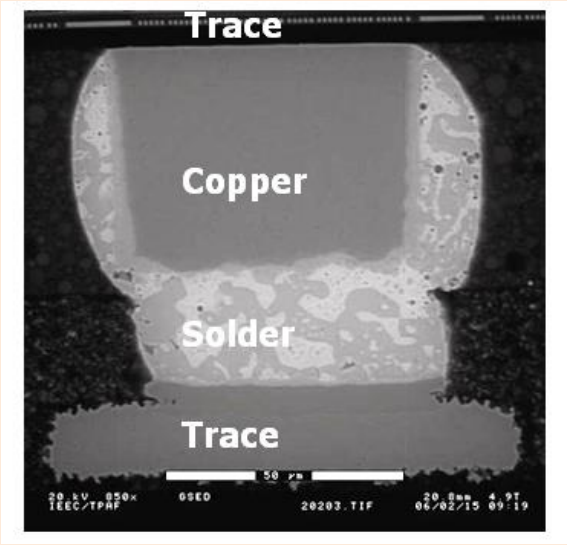
Example Process Steps For Solder Bump Formation



Source: Fujitsu

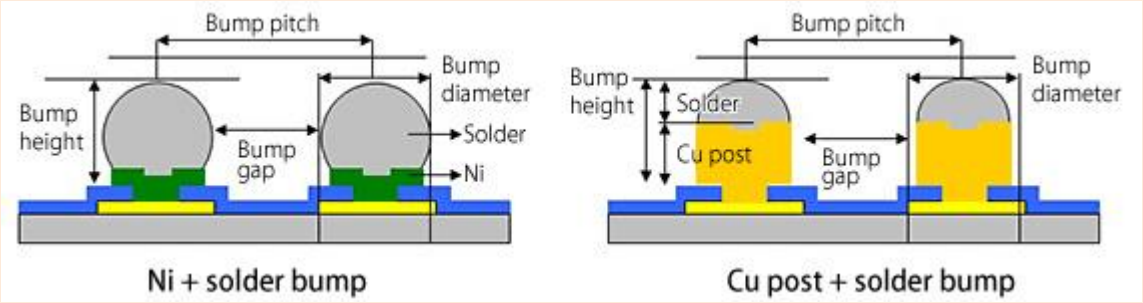
Hard Bump Fabrication

SEM of Copper Bump Attach



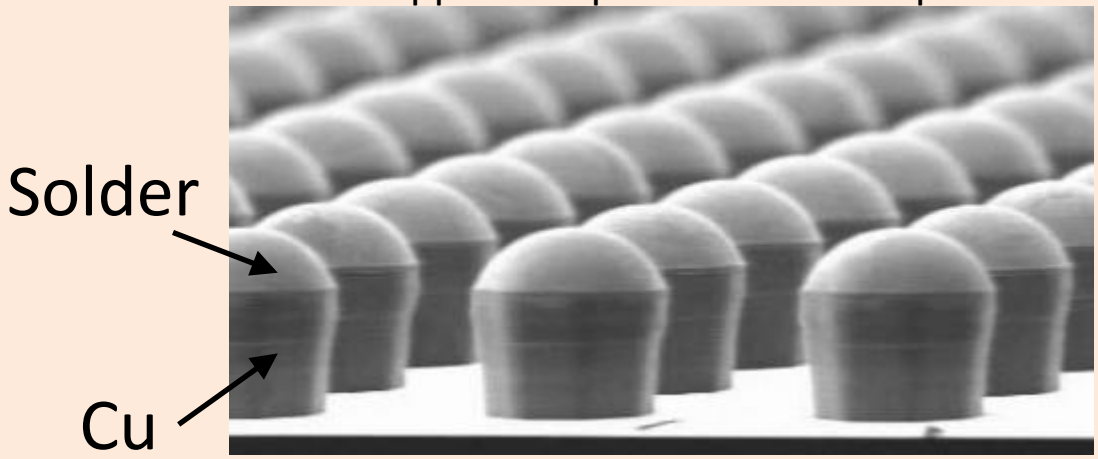
Source: Nextreme Thermal Solutions

Comparison of Solder Bump and Copper Post



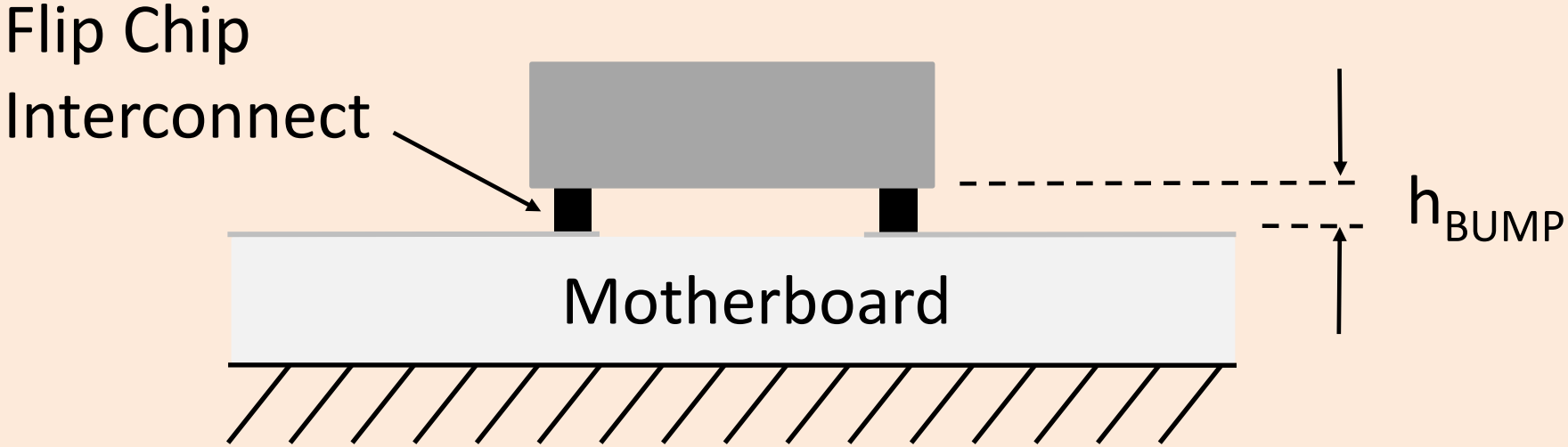
Source: Shinryo-The Kaiteki Corporation

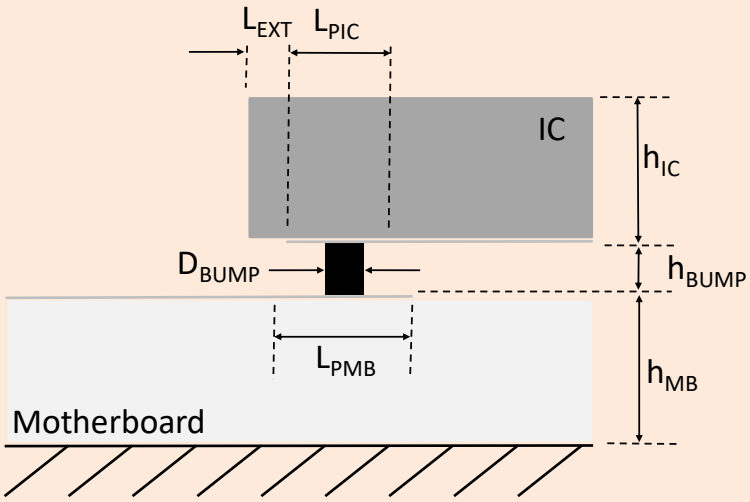
Copper Bumps With Solder Caps



Source: TLMI

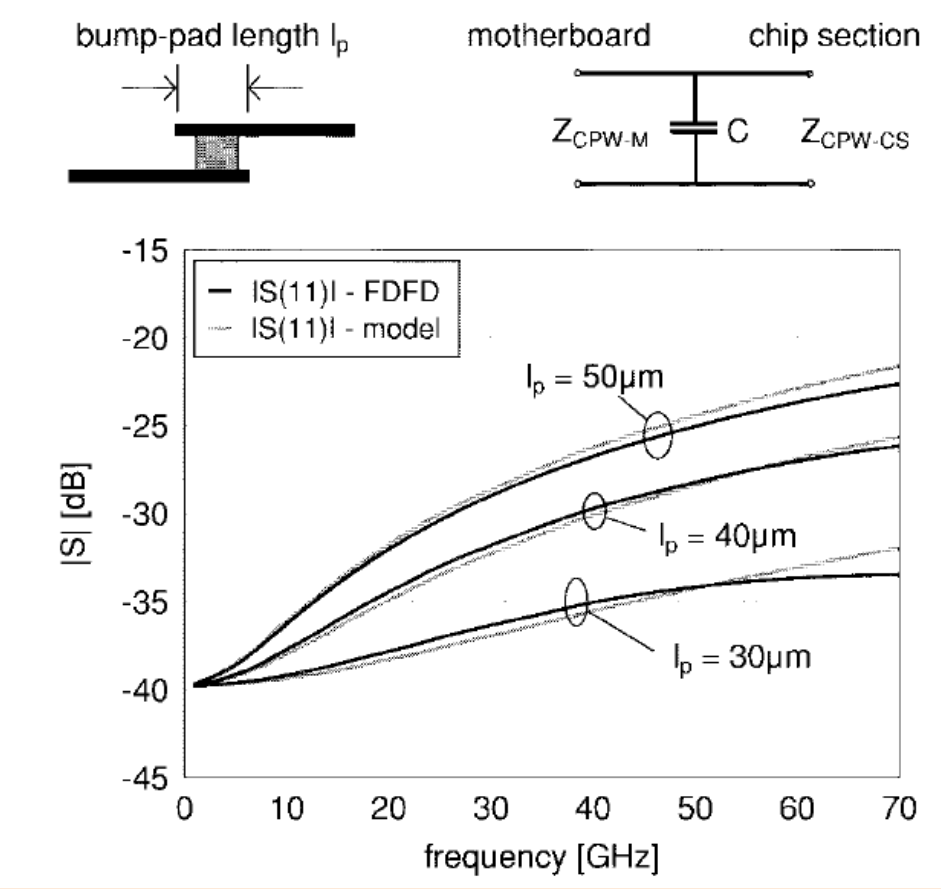
Electrical Modeling of Flip Chip Interconnects





h_{BUMP} = height of the bump (distance between chip and substrate)
h_{IC} = height of the integrated circuit
h_{MB} = height of the motherboard
L_{PMB} = diameter of the motherboard bump pad
D_{BUMP} = diameter of bump
L_{PIC} = diameter of the
L_{EXT} = extent of the IC beyond the bump pad

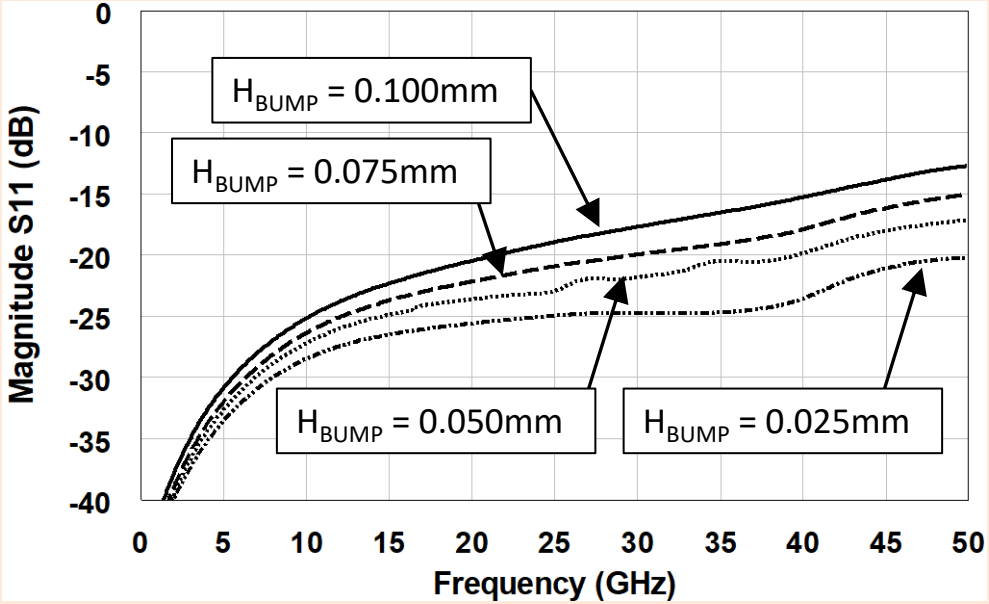
Flip Chip Interconnect Electrical Modeling



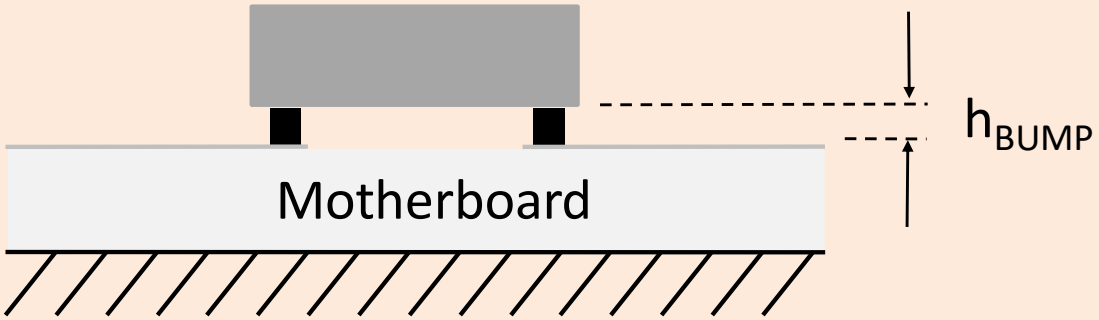
- A simple capacitance model can be used to capture the discontinuity effect at the bump contact.
- Plot is a comparison of FDTD electromagnetic model to the capacitance model.

W. Heinrich, A. Jentzsch, G. Baumann, "Millimeter-wave characteristics of flip-chip interconnects for multichip modules," IEEE Trans. Microwave Theory and Tech., Vol. 46, No. 12, Dec. 1998, pp. 2264-2268.

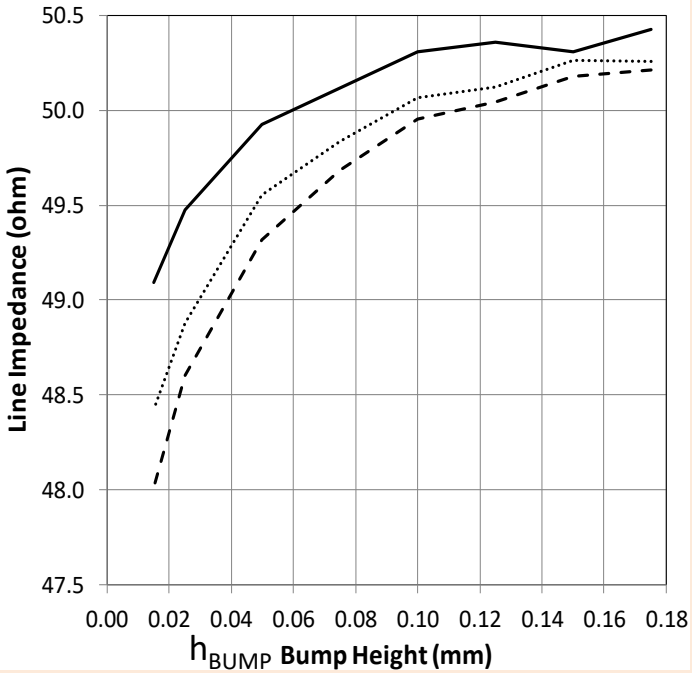
Bump Height Has An Effect On Flip Chip Interconnect

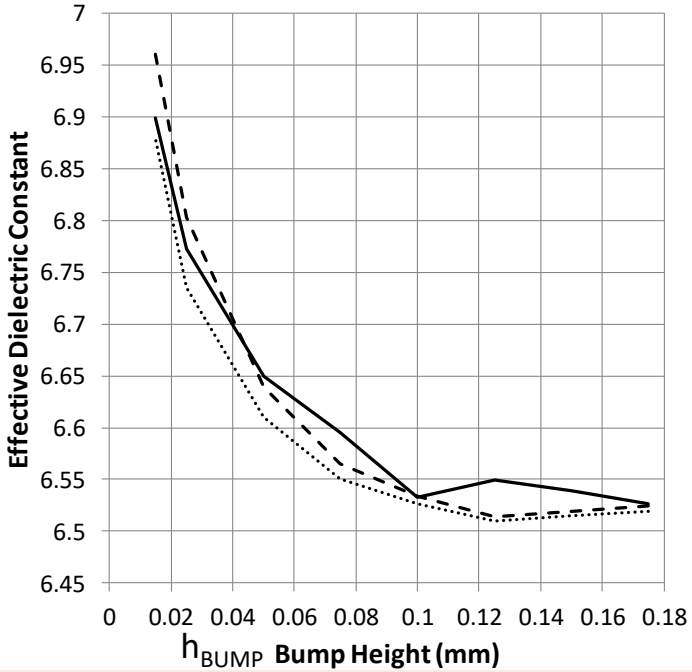


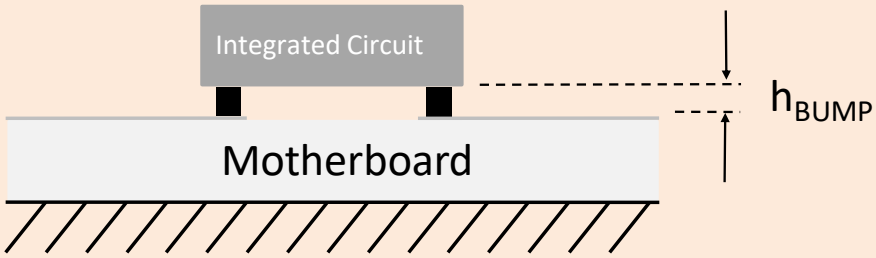
- Plot shows the return loss for a flip chip interconnect for bump heights of 0.025, 0.05, 0.075, and 0.10mm.



Bump Height Effects On Line Impedance and Effective Dielectric Constant

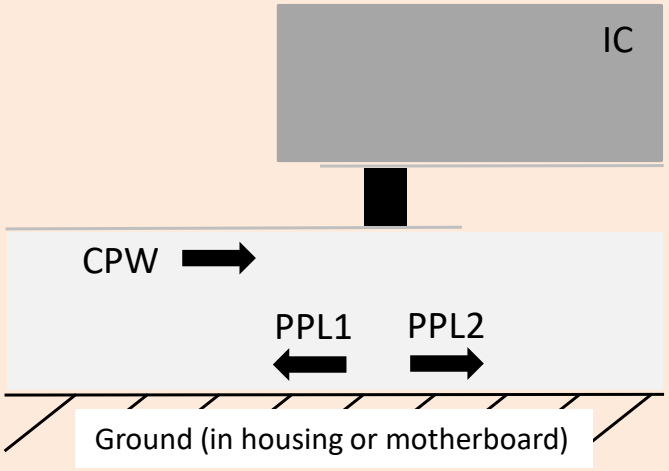


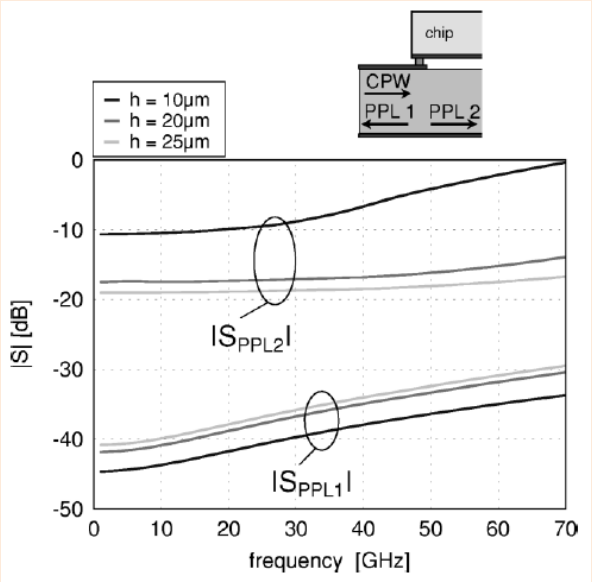




- For the case of coplanar waveguide transmission lines on the integrated circuit
- As bump height is reduced, the fields in the transmission line on the integrated circuit begin to interact with the mounting substrate.

Parasitic Modes At Flip Chip Interconnects

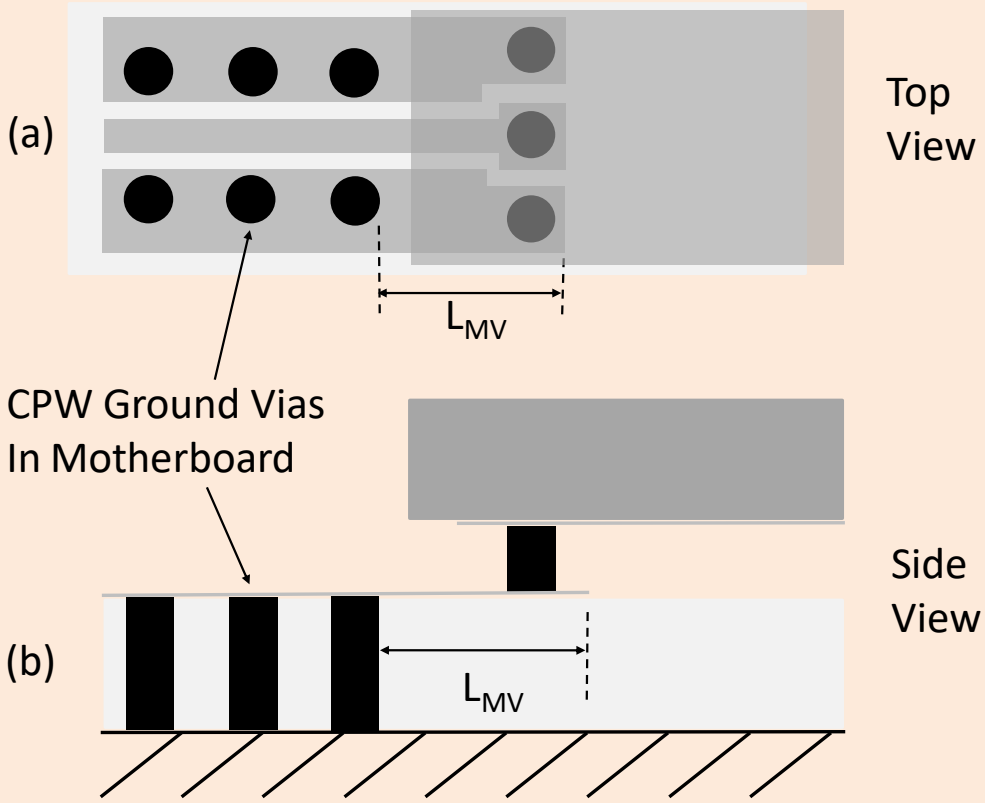




- Because of the ground plane under the motherboard, parasitic parallel plate (PPL) modes can propagate at the transition into the integrated circuit.
- The modes can propagate away from the transition.
- The result is reduced isolation between adjacent circuit elements.
- Severe circuit instabilities can result especially for high gain modules such as transmit receive modules.

Source: W. Heinrich, A. Jentzsch, G. Baumann, “Millimeter-wave characteristics of flip-chip interconnects for multichip modules,” IEEE Trans. Microwave Theory and Tech., Vol. 46, No. 12, Dec. 1998, pp. 2264-2268.

Resonant Mode At Flip Chip Interconnects



$$f_{MV} = \frac{c/\sqrt{\varepsilon_{reff}}}{4L_{MV}}$$

Avoid this resonance by placing vias all the way to the flip chip interconnect

- If vias are no properly placed at the transition into the flip chip, then a quarter-wave resonance can be set up.
- Therefore, proper grounding is required all the way to the flip chip interconnect.

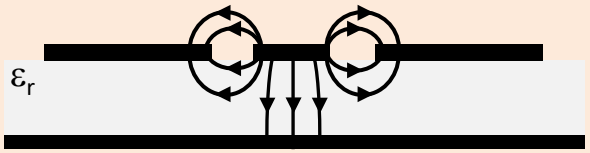
Comparison Between Wire Bonds and Flip Chip

- Wire Bonds
  - Flexible: Wire sizes, ribbon, wire materials, ball or wedge, etc.
  - Significant infrastructure: Significant installed manufacturing base
  - Low cost
  - Reliable
- Flip Chip
  - Higher frequency performance—Increase IC speed and bandwidth
  - Can distribute power and ground across the face of the IC
  - Can achieve significant I/O density
  - Reliable

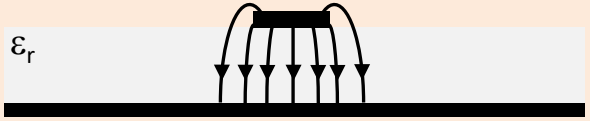
More Information: P. Elenius, L. Levine, “Comparing flip-chip and wire-bond interconnection technologies,” Chip Scale Review, July/August 2000, pp. 81-87.

Section 4.3: Transitions Between Transmission Lines

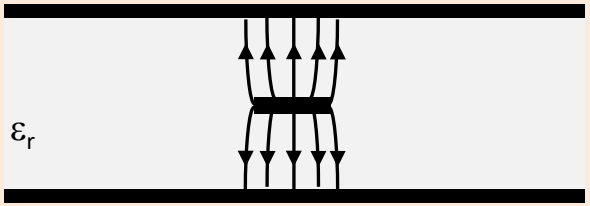
Guidelines For Proper Design Of Transitions Between Transmission Lines



Microstrip



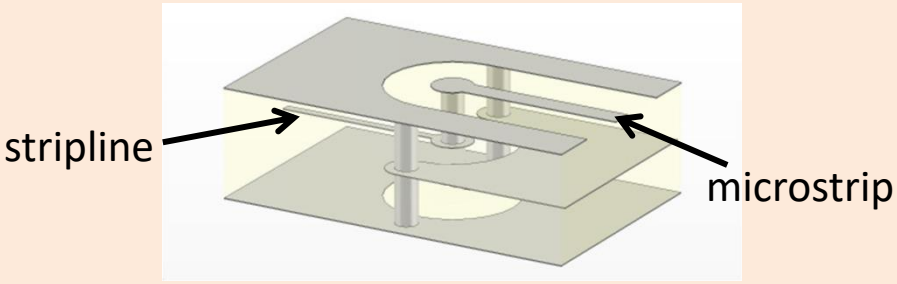
Microstrip



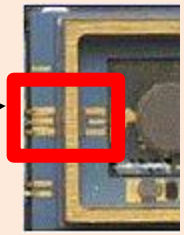
Stripline

1. Maintain the same field distribution between transmission lines: If the field distribution between to connecting transmission lines is similar, then the transition has the potential for wide bandwidth.
2. Smoothly transition between transmission line types: Avoid any abrupt changes in features.
3. Use impedance transformation when appropriate: It is possible to include matching circuitry which can be used to tune out undesired inductive or capacitive effects.
4. Minimize stray capacitance: Stray capacitance is one of the primary effects that reduces the bandwidth of microwave and millimeter-wave transmission line transitions.
5. Avoid the excitation of propagating higher order modes: Higher order modes have the potential to increase undesired coupling and increase insertion loss.

Section 4.4: Transition Between Stripline and Microstrip In Ceramic



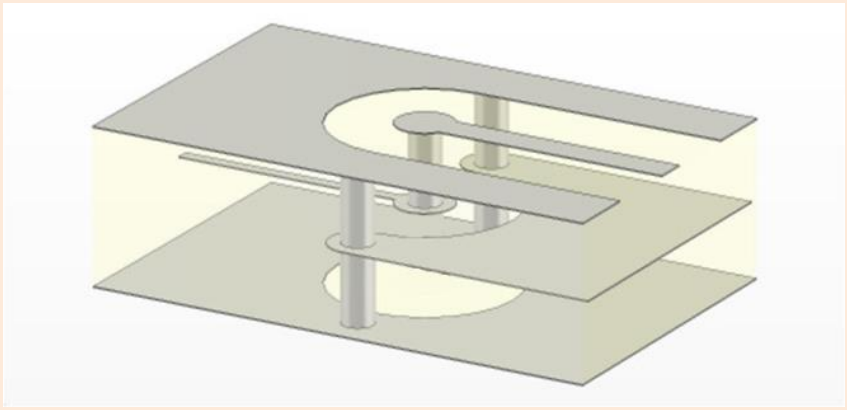
Vertical Transition



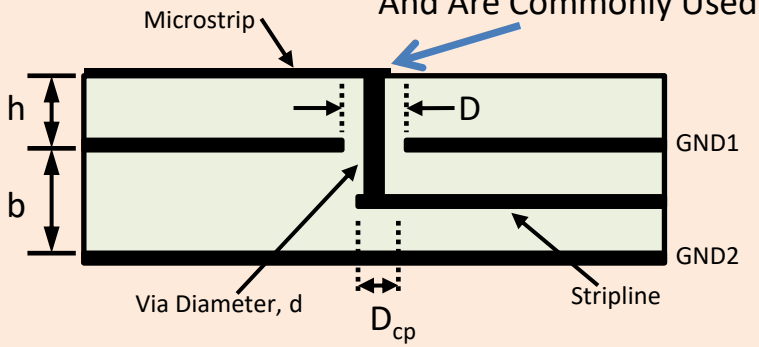
Output Transition
From A T/R Module

- This is a very common transition since many applications require the signal line to be buried inside the PCB at some point.
- Requires careful design of the transmission lines and transition area between the transmission lines.

The Equivalent Circuit Model Of The Transition Is An LC Network



In Multilayer Ceramics, Blind and Buried Vias Are Allowed And Are Commonly Used



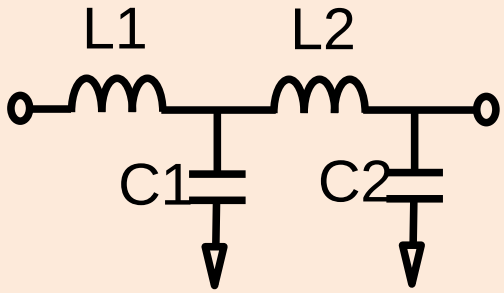
L1 = inductance of the via through substrate thickness h.

L2 = inductance of via through the top section of substrate thickness b.

C1 = capacitance created by via passing through the ground plane below the microstrip.

C2 = capacitance created by the via catch pad at the stripline interface.

Equivalent Circuit Model



The Model Creation Procedure Requires Three Steps

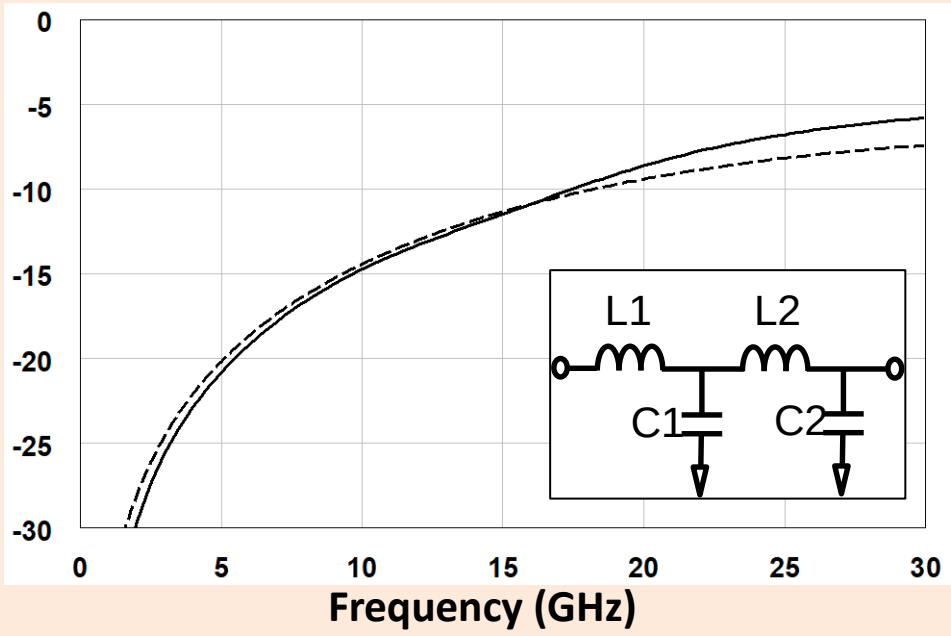
$$L_1 = L_{Via} = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right) + \frac{3}{2}\left(r - \sqrt{r^2+h^2}\right)\right] \quad (4)$$

h = length of the via (meters)
r = radius of the via (meters)

$$C_1 = A1 \cdot \left(h + \frac{b}{2}\right)\frac{\varepsilon_r}{60 \cdot v_o \ln(D/d)} \quad (5)$$

$$C_2 = \frac{A_{cp} \cdot \varepsilon_o \varepsilon_r}{spacing} = \frac{\pi\left(\frac{D_{CP}}{2}\right)^2 \varepsilon_o \varepsilon_r}{b/2} \quad (6)$$

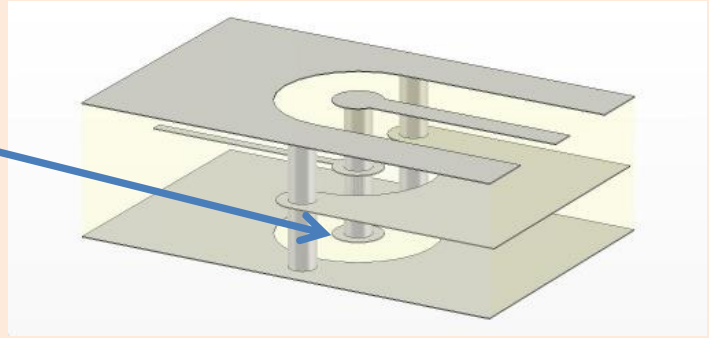
- **Step 1:** Calculate L1 and L2 using (4).
- **Step 2:** Calculate C1 using (5).
- **Step 3:** Calculate C2 using (6)

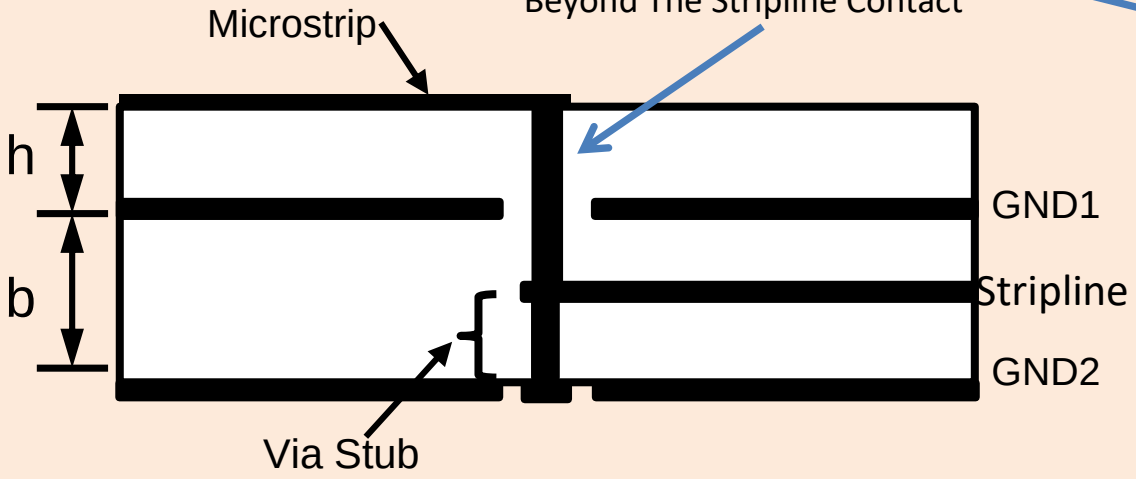


For LTCC (ε_r=7.8), h=0.25mm, b=0.5mm, D=0.55mm, d=0.2mm, D_{cp}=0.35mm which yield L1=0.0259nH, L2=0.108nH, C1=0.102pF, C2=0.0781pF

Section 4.5: Transition Applied To A PCB Which Uses Through Vias

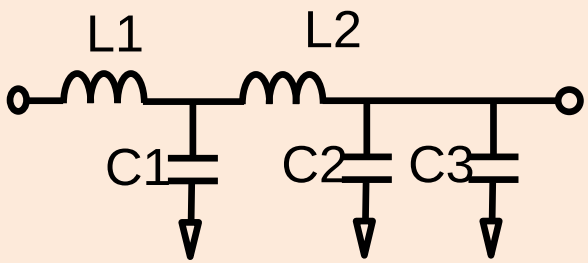
In Printed Circuit Boards, Blind And Buried Vias Are Less Commonly Used. This Means The Via Will Extend Beyond The Stripline Contact





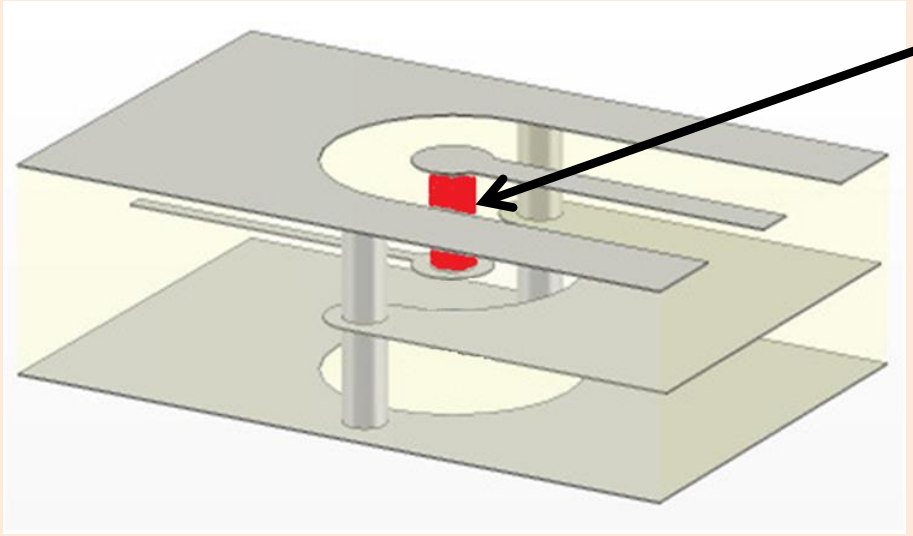
- Follow the same procedure as for the LTCC circuit board, but add a capacitance to account for the capacitive effect of the via stub.

Equivalent Circuit



$$C_3 = A2 \cdot \frac{b}{2} \frac{\varepsilon_r}{60 \cdot v_o \ln(D/d)}$$

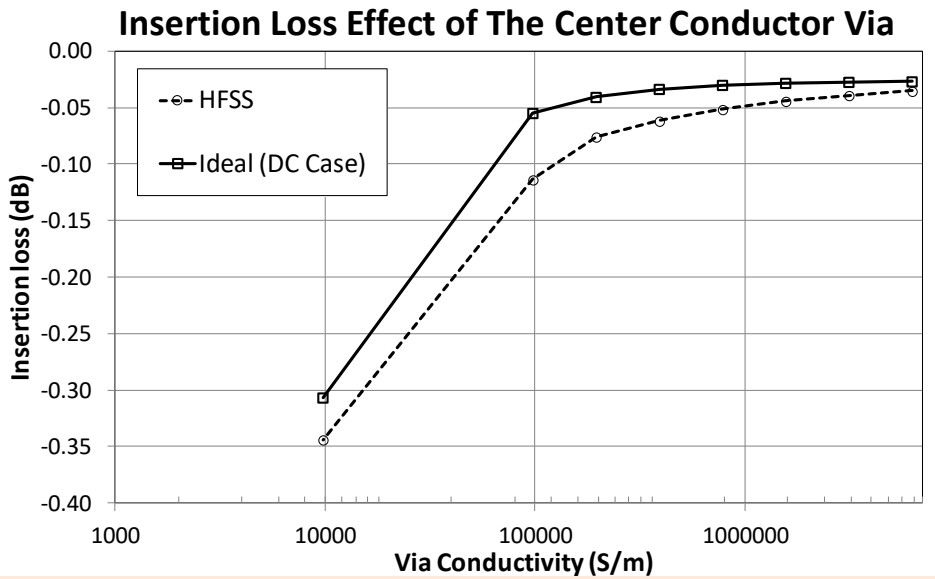
Section 4.6: Effect Of Via Conductor Loss Of On Electrical Performance



- Two Approaches Will Be Used
- Method 1
  - Use DC resistance of the via to calculate the conductor loss.
- Method 2
  - Take into the skin effect
  - Procedure:
    - Convert ohm/sq into resistivity
    - Perform EM simulation
    - Extract insertion loss as a function of metal conductivity
    - Modify circuit model to accommodate via resistance effect.

R. Sturdivant, E.K.P. Chong, "Modeling and Simulation of Via Conductor Losses in Co-fired Ceramic Substrates Used In Transmit/Receive Radar Modules," Presented at the *2016 IMAPS RaMP Conference*, San Diego, CA.

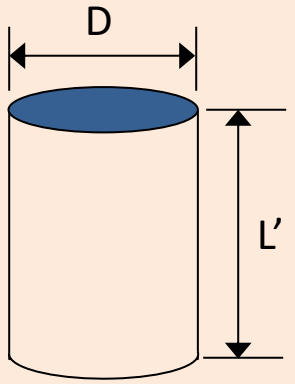
Method 1:The Via Can Be Modeled As A Simple Resistor For Insertion Loss Contribution



Considering DC (i.e., f=0) Current Only

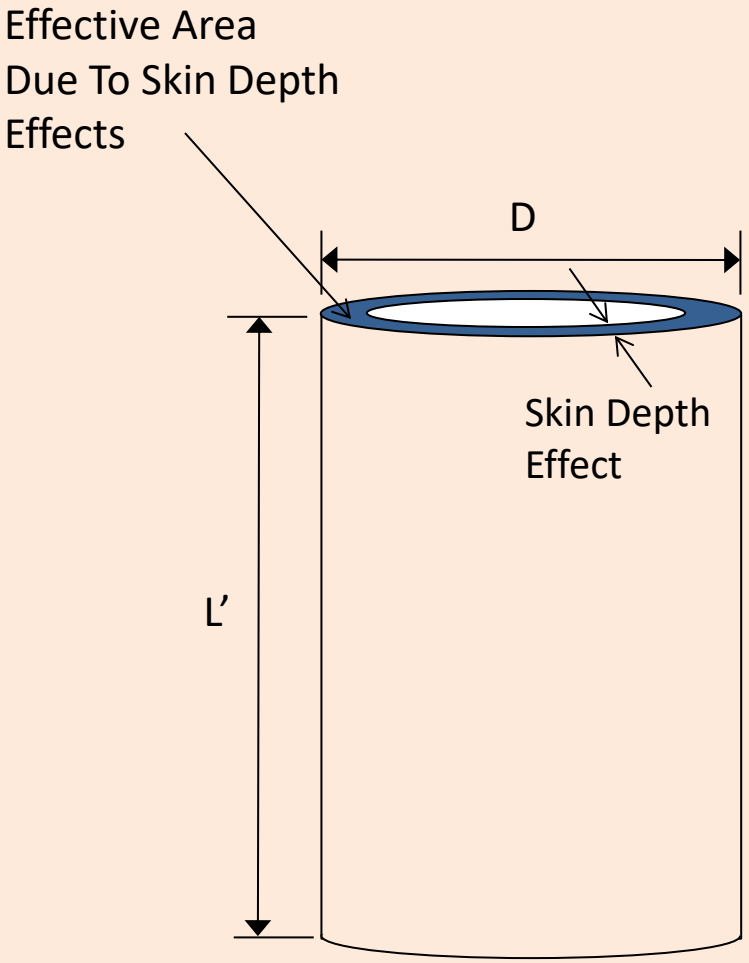
$$A' = \pi (D/2)^2$$

$$R' = \rho (L'/A') \quad (1)$$



- Contribution of resistive part to the insertion loss of the transition can be found from (1), but only if we were just concerned about DC effects (i.e., effects at zero frequency).
- However, (1) does not capture the full story because of the skin depth effect.

Method 2: Because of Skin Depth Effects, The Current Only Travels On The Surface Of The Via



$$A_{eff} = A' - A1$$

$$= \pi\left[\left(\frac{D}{2}\right)^2 - \left(\frac{D - n\delta}{2}\right)^2\right]$$

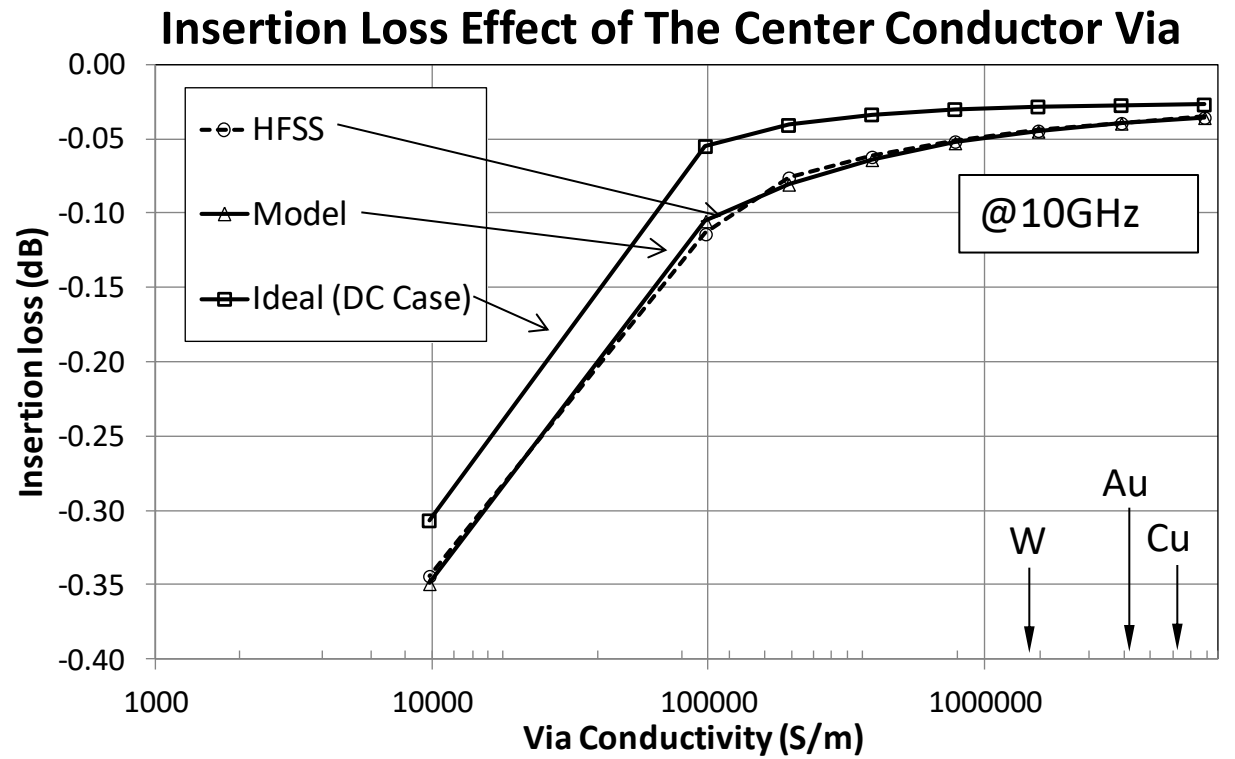
n= number of skin depths to include

$$R' = \rho\left(\frac{L'}{A_{eff}}\right)$$

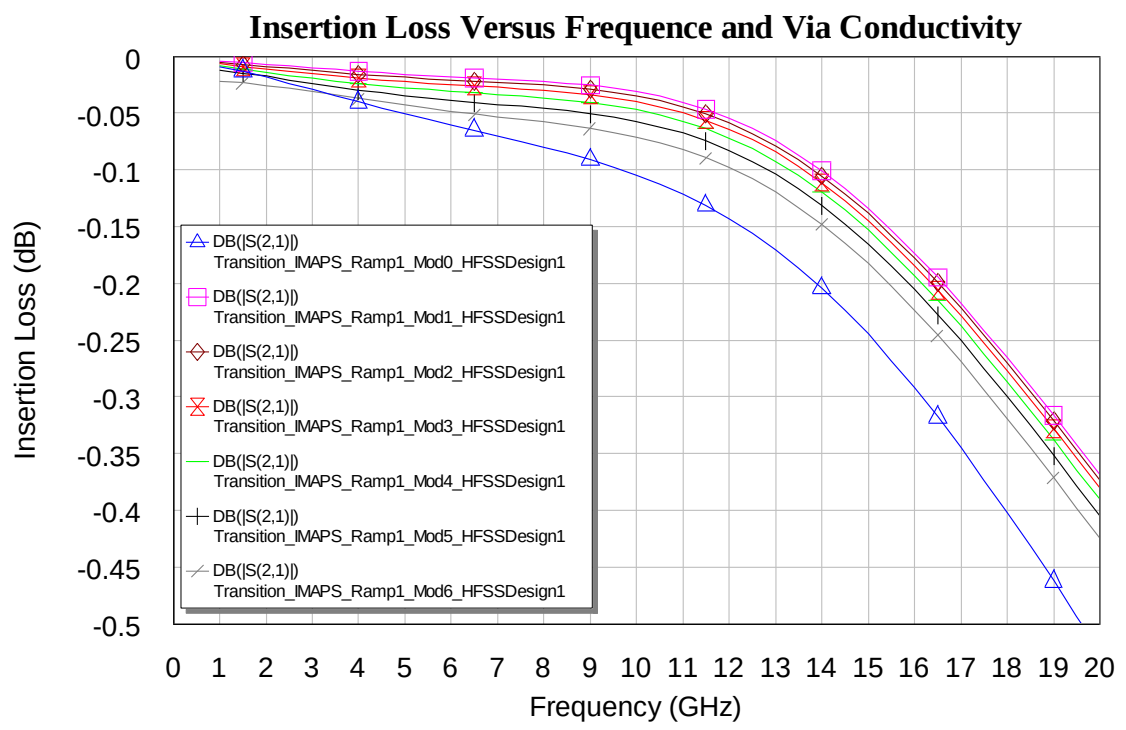
- Using the equation for R' for a more accurate estimate of the insertion loss

$$S21(dB) = 20\,LOG_{10}\left(\frac{2}{2 + R'/Z_0}\right)$$

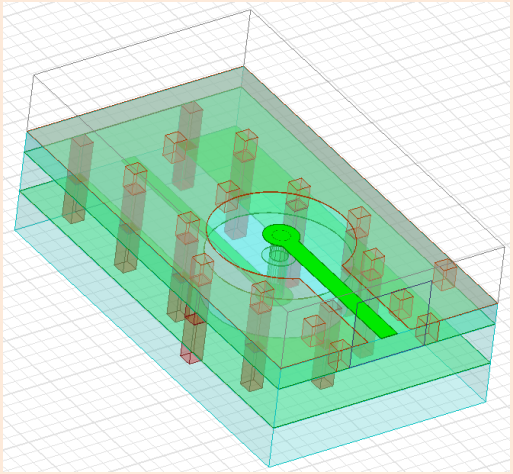
When Skin Depth Effects Are Taken Into Account, The Lumped Model Agrees With HFSS



Simulations Were Performed Using HFSS From Ansys



Alumina HTCC

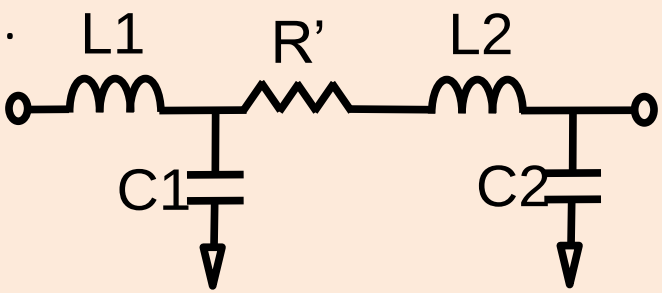


- Results show a steady increase in insertion loss as a function of frequency and via conductivity.
- Roll off above 10GHz is due to mismatch losses.

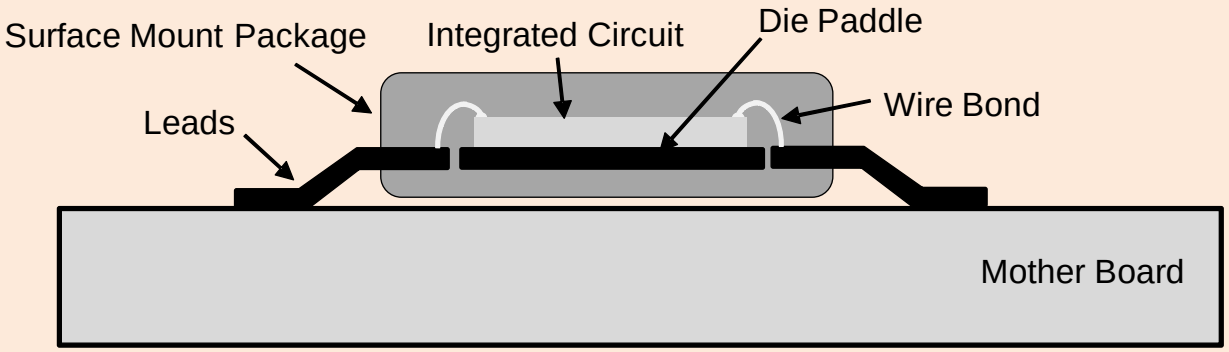
Result Of Investigating The Effect of Conductivity of Center Via

- The goal was to show the effect of the center conductor resistivity for vertical transitions.
- The investigation showed:
  - 1) For good conductivity metals, the contribution of the center conductor to overall insertion loss of the vertical transition is less than approximately 0.1dB.
  - 2) The skin depth effect must be accounted for when calculating the resistive part of the via transition.
- Suggestions For Further Study:
  - 1) All the vias including the ground vias in the location of the transition should be taken into account.
  - 2) A analytical solution for *n* should be calculated.

Modified Model →

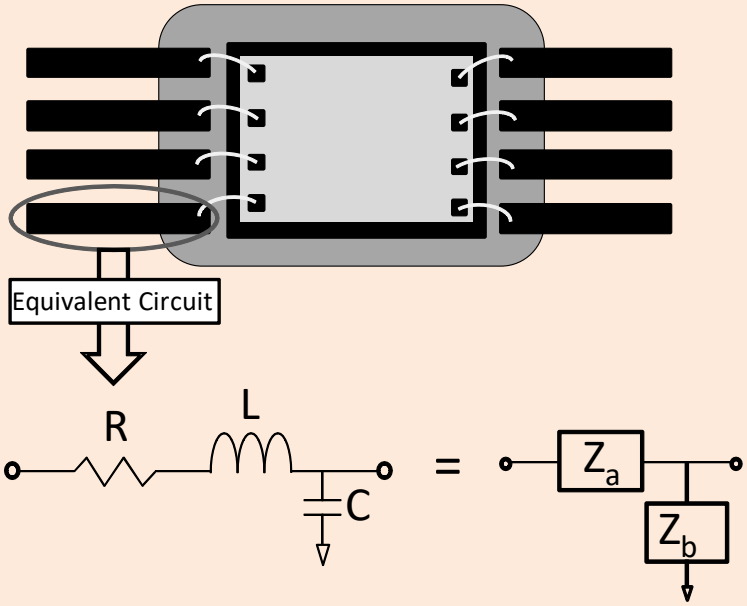


Section 4.7: Package Transition Modeling

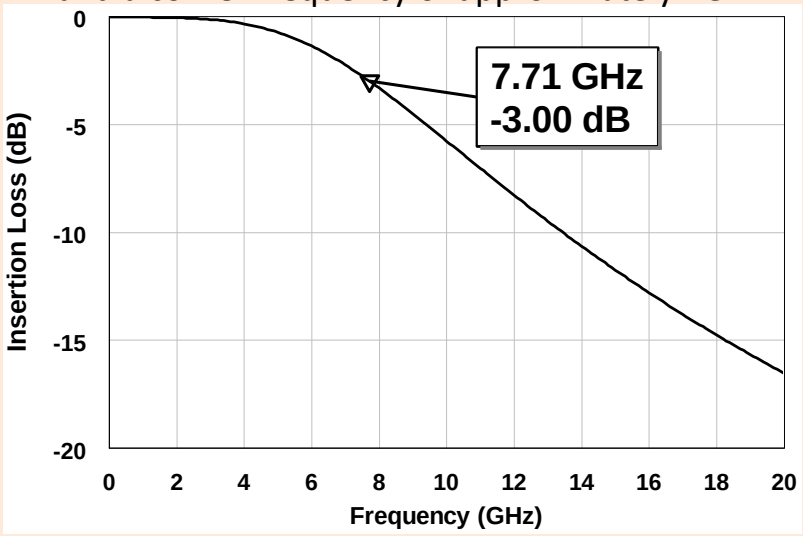


Side View Of A Package Mounted Onto A Motherboard As An Example Of A 2nd Level Interconnect (As Defined Here)

Simplified Model

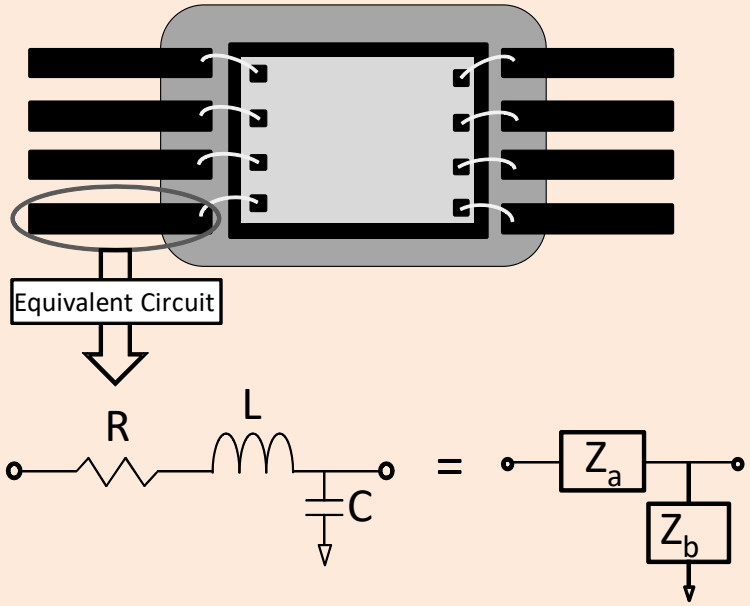


Simplified Model shows a 3dB bandwidth of 7.7GHz and a corner frequency of approximately 2GHz



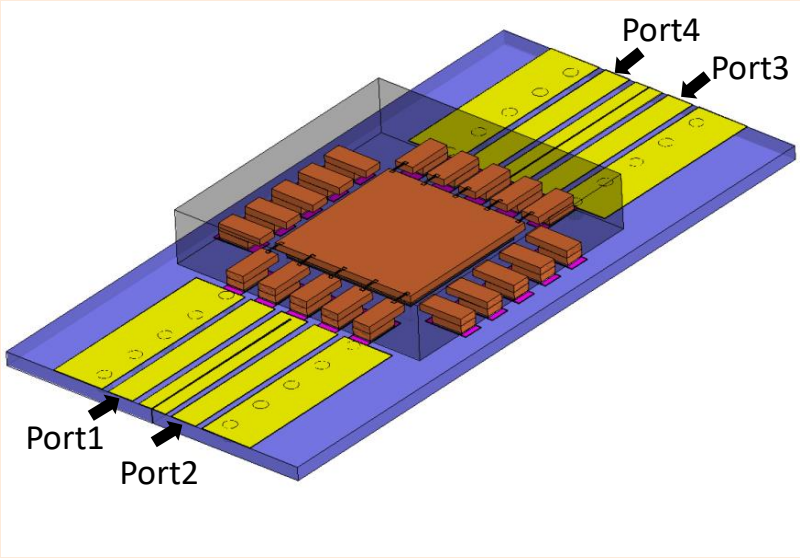
For a particular package, it was found that L = 1.4nH, R = 0.5ohm and C = 0.6pF

Benefits and Drawbacks of The Simplified Model

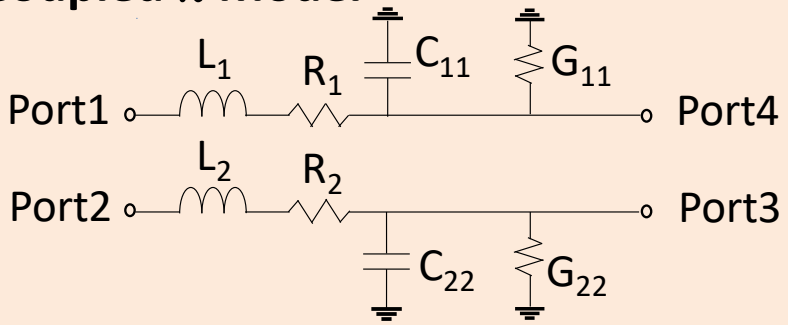


- Benefits
  - It captures some important physical effects such as the shunt inductance.
  - It is simple and easy to implement and analyze.
- Drawbacks
  - It neglects important effects such as coupling between package leads.

The LCR Model Is A Higher Model Fidelity Of Package To Motherboard Interconnects

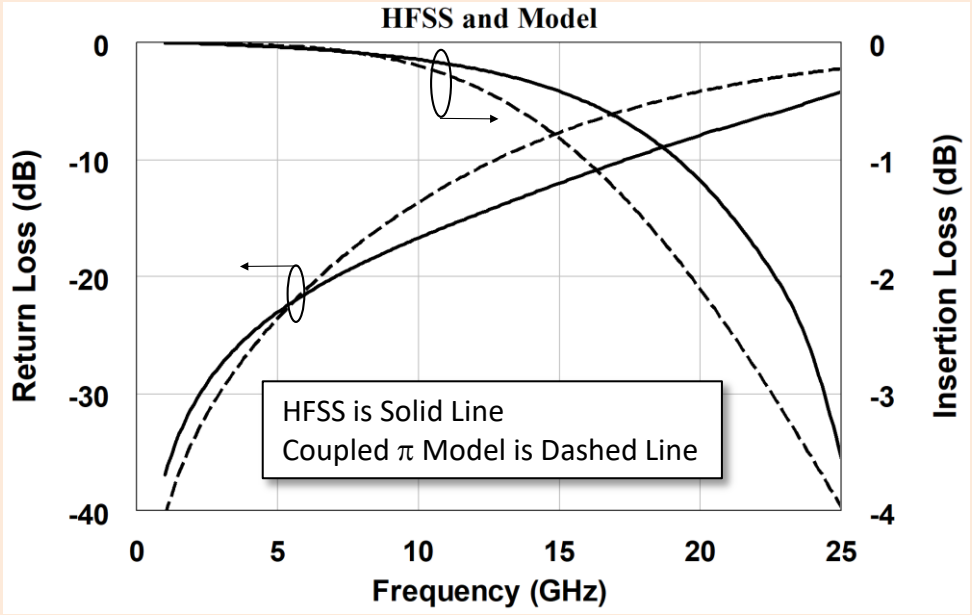


Coupled π Model



- The LCR Model provides a good agreement to EM simulations.

L1=L2 = 0.5722nH
R1=R2=0.0434 ohm
C11=C22=0.17pF
G11=G22=7.74x10^{-6} mho



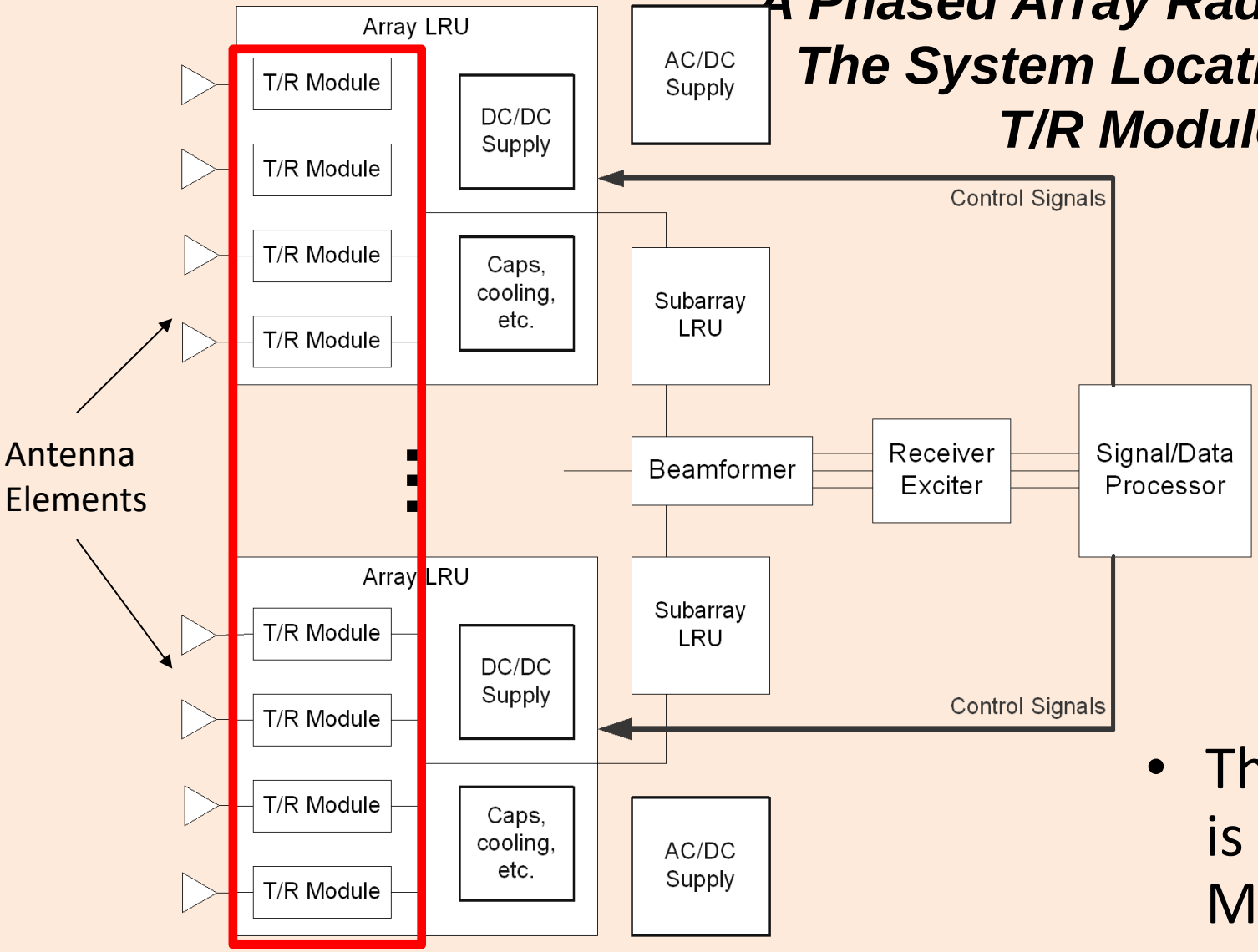
Section 4 Summary

- Simple model of an inductor for a wirebond is insufficient at microwave and millimeter-wave frequencies.
- Flip chip interconnect is an attractive interconnect for 5G systems but there are undesired modes and resonances that must be avoided.
- Transitions between transmission line types can be achieved and an example of microstrip to stripline was provided.
- SMT packaging is an attractive option for 5G systems and a method for modeling the transition was provided.

Section 5: Transmit Receive Modules For 5G

- 5.1 Block Diagram of Phased Array with T/R
- 5.2 Detailed Block Diagram of T/R Module For Half Duplex and Full Duplex Operation
- 5.3 Examples of Core Chips and T/R Integration With Antennas

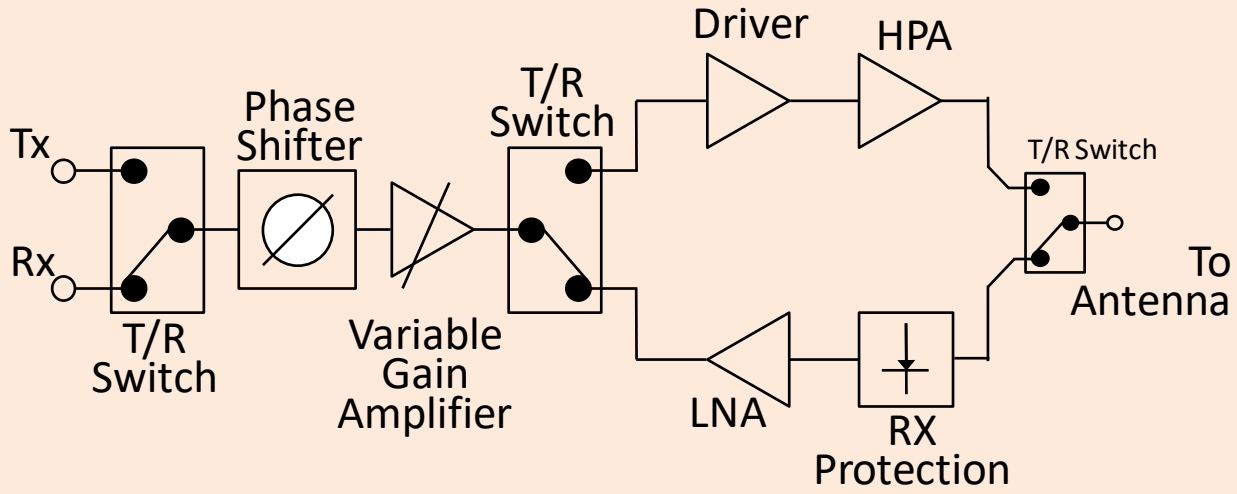
Section 5.1: Block Diagram Of A Phased Array Radar Showing The System Location Of The T/R Modules



- This section is on T/R Modules

Section 5.2: Detailed T/R Block Diagram

Basic T/R Functionality For Half Duplex Systems



Essentially all phased array T/R modules contain the functions represented by the block items shown in the figure.

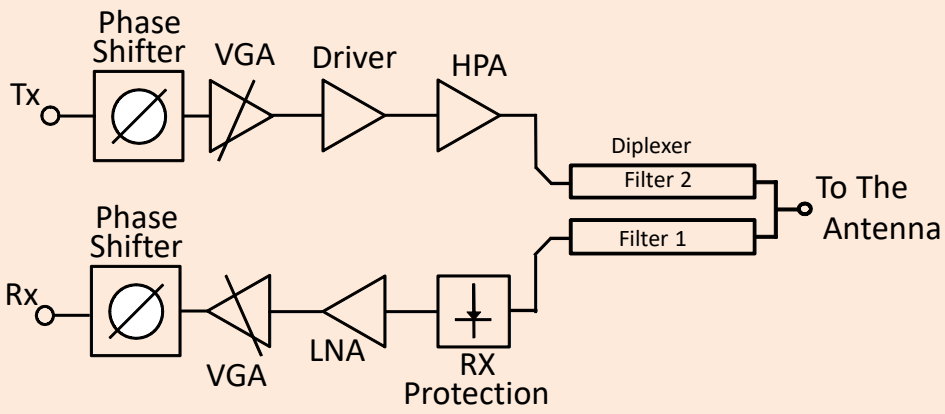
- In half duplex systems, the T/R module is combined as shown in the figure.
- A popular example is Wi-Fi

Definitions

Half Duplex: Use a single channel to transmit and receive. Therefore, receive is off while transmitting and transmit is off during receiving.

Full Duplex: Use separate channels to transmit and receive. Therefore, receive and transmit occur simultaneously.

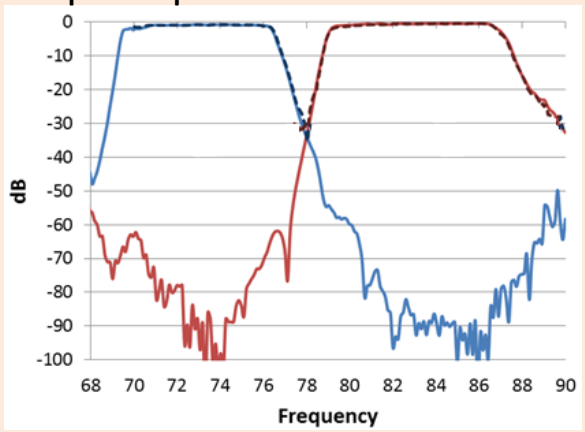
Full Duplex T/R Module



T/R Functions May Be Implemented In A Module, Individual Package, Multiple Packages, or SOIC with Multiple T/R In One Semiconductor Device

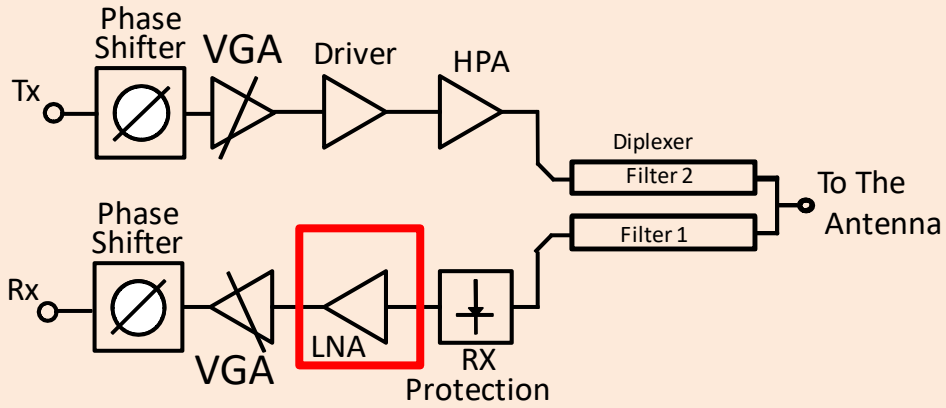
- The diplexer combines two filters (typically band pass filters or low pass and high pass filters at different frequencies).
- The isolation between the filters is high enough that the T/R module can transmit and receive at the same time.
- Challenge is the very high isolation required between channels. The specification is typically 55-60dB.

Example Diplexer Measured Data



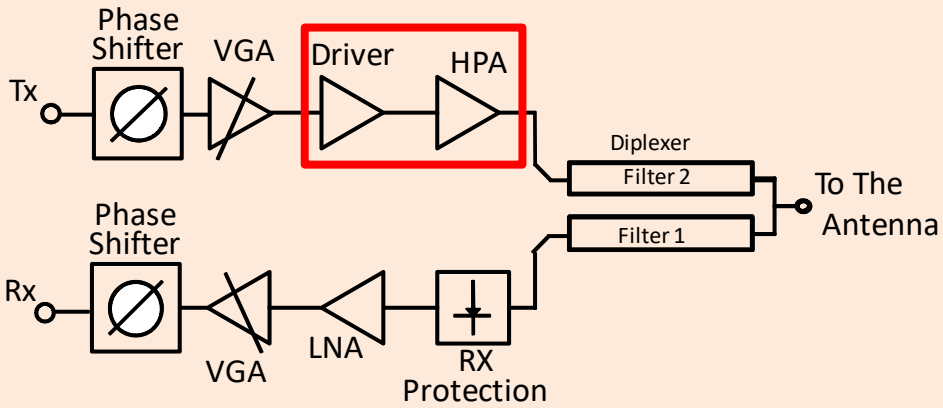
Source: Millitech

The Low Noise Amplifier Is An Important Component Since It Sets The Noise Figure Of The Receiver



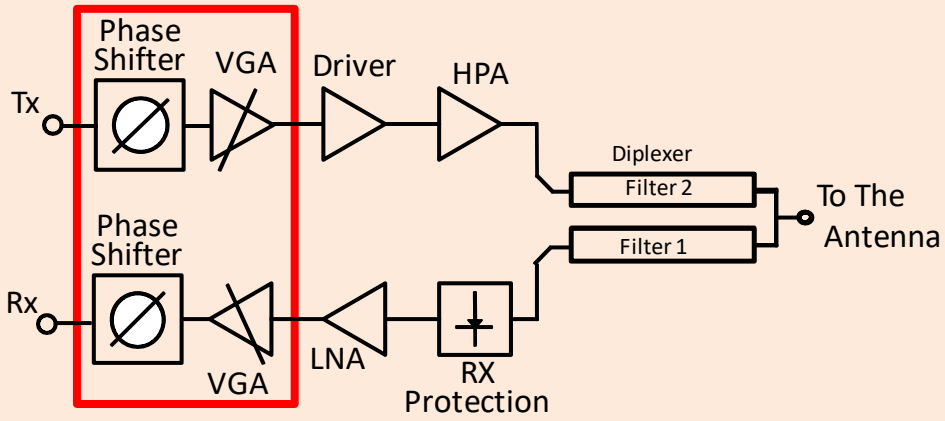
- The Low Noise Amplifier (LNA) provides gain, but adds very little to the noise figure.
- See Appendix A for more information on calculating system noise figure which demonstrates that the LNA sets the system noise figure.

High Power Amplifiers Increase The Transmit Signal Level To Achieve Link Range and Data Rate



- The driver amplifier and high power amplifier (HPA) combination provide the gain and the signal output power to the antenna.

The Phase Shifter Provides The Progressive Phase To Each Antenna Element To Enable Beam Steering



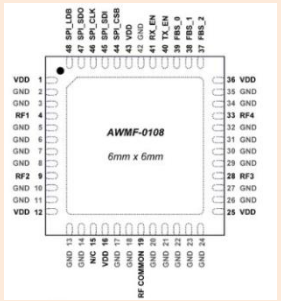
- The phase shifter and VGA are often called a core chip since it is provides the core functions of the phased array.

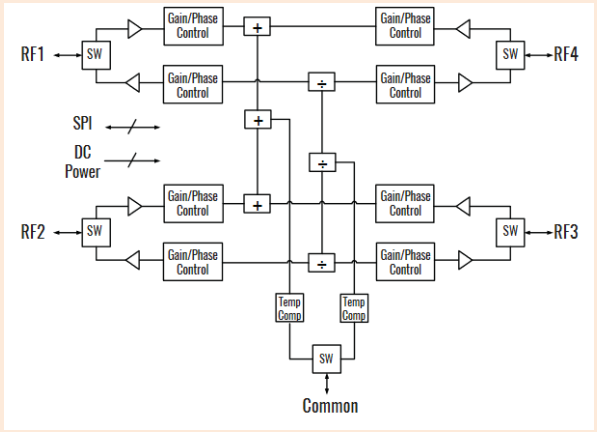
Section 5.3 Examples

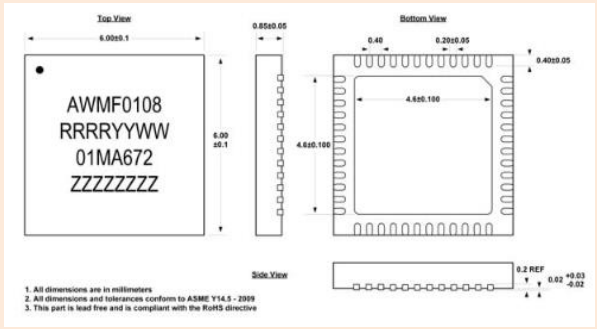
Example Core Chip From Anokiwave, The AWMF-0108 Ka-Band 5G Quad Core IC

Product Features

- 26.5 - 29.5 GHz operation
- Supports 4 radiating elements
- Tx/Rx half duplex operation
- +9 dBm Tx OP1dB
- +26 dB Tx gain
- +28 dB Rx coherent gain*
- 5.0 dB Rx NF
- -28 dBm Rx IIP3
- 5 bit phase control (LSB=11.25°)
- 5 bit gain control (LSB=1.0 dB)
- Fast beam steering
- Telemetry reporting
- 6x6 mm QFN
- +1.8 V operation
- 0.6 W DC Tx mode quiescent
- 0.8 W DC Tx mode at P1dB
- 0.5 W DC Rx mode



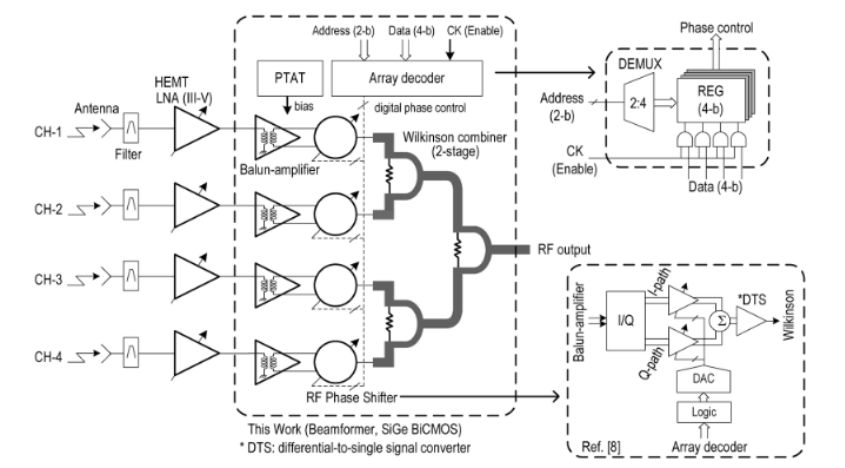


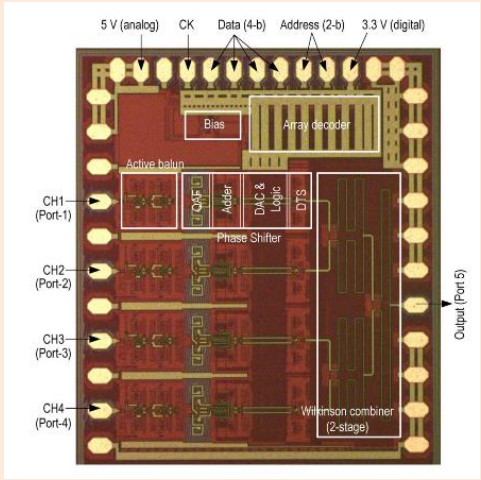


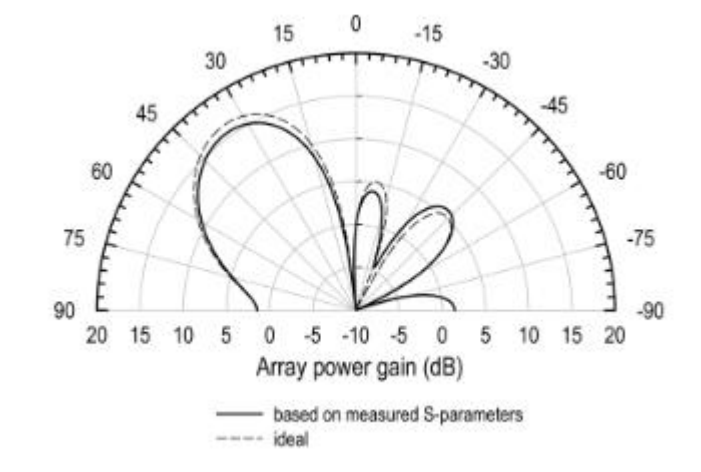
- 26.5-29.5 GHz operation
- Supports 4 radiating elements
- Tx/Rx half duplex operation
- Single antenna for Tx and Rx
- 5 bit phase and gain control
- Fast beam steering

http://www.anokiwave.com

Example Of A Q-Band (30-50GHz) Four Element Phased Array Core Chip







- Receive phased array that covers 5G bands
- Uses wire bond first level interconnects.

K. Koh, G. Rebeiz, "A Q-Band Four-Element Phased-Array Front-End Receiver With Integrated Wilkinson PowerCombiners in 0.18-um SiGe BiCMOS Technology," IEEE Trans. Microwave Theory and Tech., Vol. 56, No. 9, Sept 2008.

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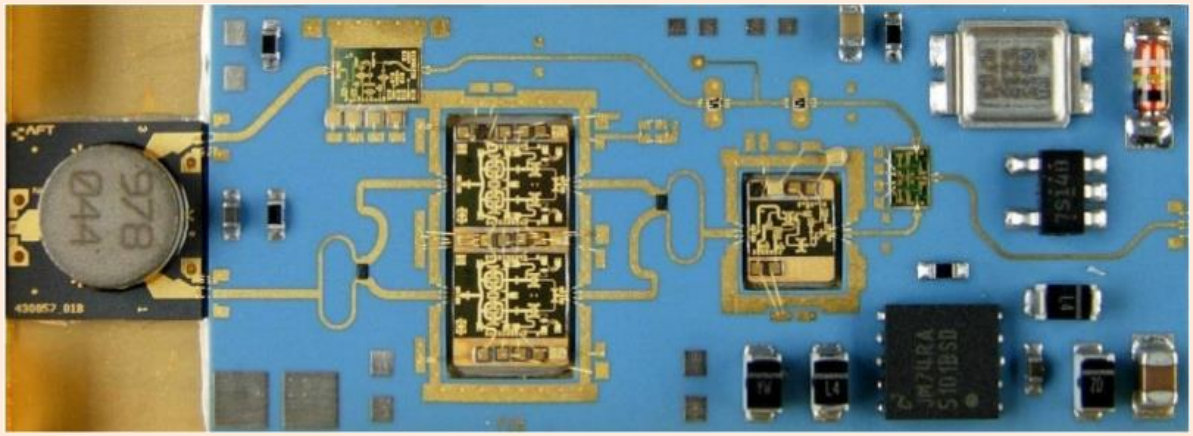
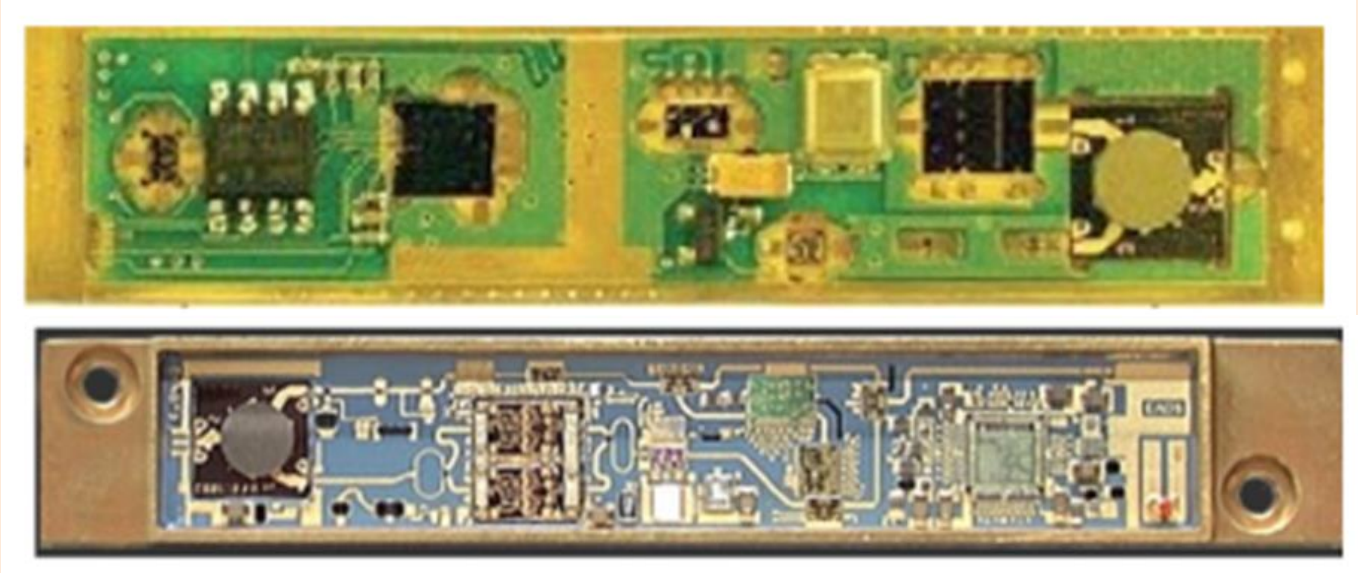
T/R Module Example: X-Band Using Low Temperature Cofired Ceramic (LTCC) and GaAs Integrated Circuits



- Uses Low Temperature Co-fired Ceramic (LTCC) Substrate
- GaAs integrated circuits
- Uses a circulator at the common port so the system is half duplex.
- The module is intended for use in a radar system.

P. Schuh, "GaN MMIC based T/R-Module Front-End for X-Band Applications," Proceedings of the 3rd European Microwave Integrated Circuits Conference, Amsterdam, Netherlands, Oct. 27-28, 2008.

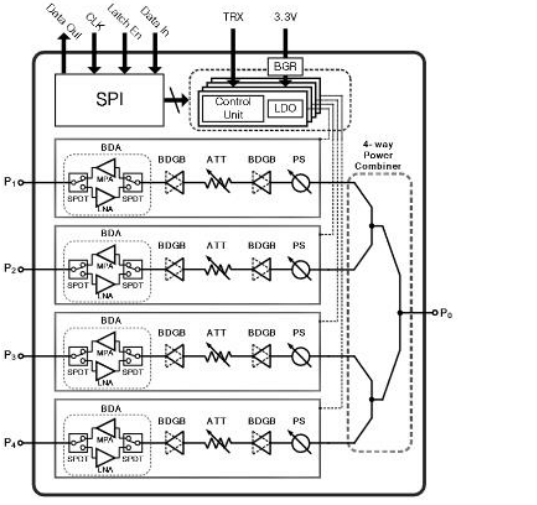
Other Examples Of Traditional Phased Array T/R Modules



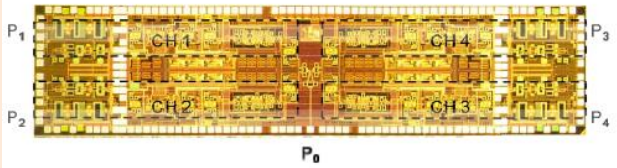
- Used either ceramic or laminate circuit boards
- Wire bonded GaAs integrated circuits

D. Gryglewski, et. al., "A 10W GaN based X-band T/R module for AESA," Int. Conf. on Microwave, Radar, and Wireless Comm., Krakow, Poland, May 9-11, 2016.

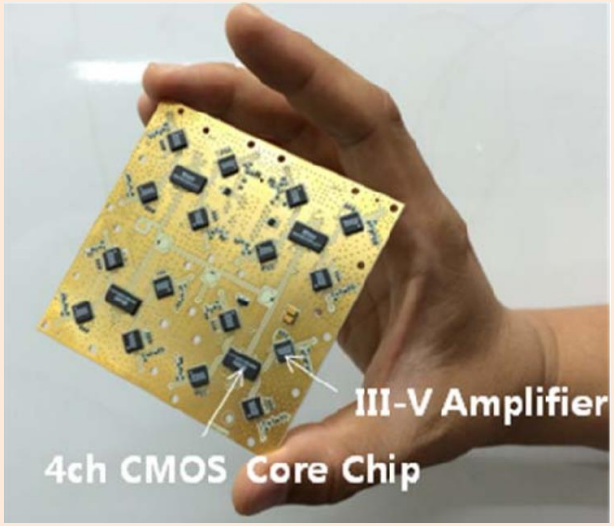
T/R Module Core Chip Integrated Onto A PCB



Block diagram of the four-channel X-band core chip



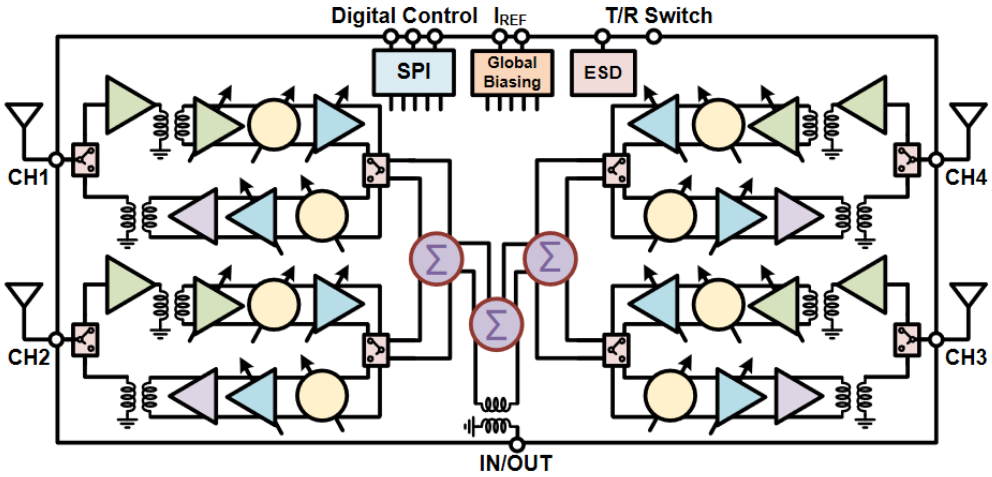
Micro photograph of the four-channel X-band core chip.
(chip size: 6.9 x 1.6 mm^2)



- Illustrates how the core chip can be integrated onto a PCB for form a four channel T/R module.

S. Sim, et. al., "A four channel bi-directional CMOS core chip for X-band phased array T/R modules," *Radar Conference*, Arlington, VA, USA, May 10-15, 2015

A Quad Core 28-32 GHz T/R For 5G Phased Arrays in SiGE BiCMOS

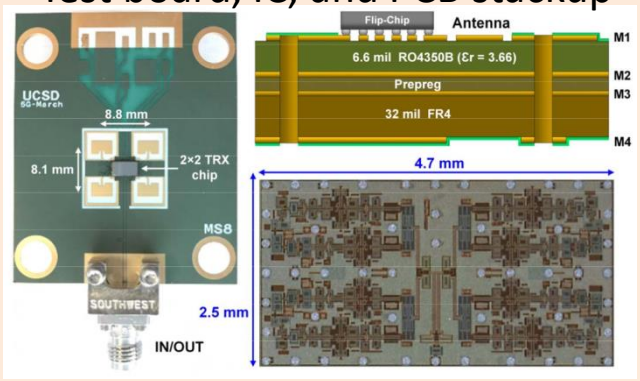


Block Diagram of a 2x2 T/R 5G Phased Array Chip

MEASURED CHIP SPECIFICATIONS

	RX (antenna port to common port)	TX (common port to antenna port)
f_o (GHz)	29	29
3 dB BW (GHz)	27-33	26-33
Gain (dB)	18	12
NF (dB)	4.6	-134 dBm/Hz at output
IP1dB / OP1dB (dBm)	-22 / -5	-0.5 / 10.5
IIP3 / OIP3 (dBm)	-12 / 6	9 / 21
Phase control	6-bits	6-bits
Gain control	3+4 bits, 14 dB	4-bits, 14 dB
Power cons. / ch (mW)	105	200 at P1dB

Test board, IC, and PCB stackup



- Uses clip chip interconnects on PCB
- First layer of the PCB uses Rogers Corp RO4350B
- Each core chip supports a four element subarray.
- Can be combined to form much larger arrays.

K. Kikaroglu, et. al., "A Quad-Core 28-32 GHz Transmit/Receive 5G Phased-Array IC with Flip-Chip Packaging in SiGe BiCMOS," IEEE MTT-S Int. Microwave Symposium, Honolulu, June 4-9, 2017.

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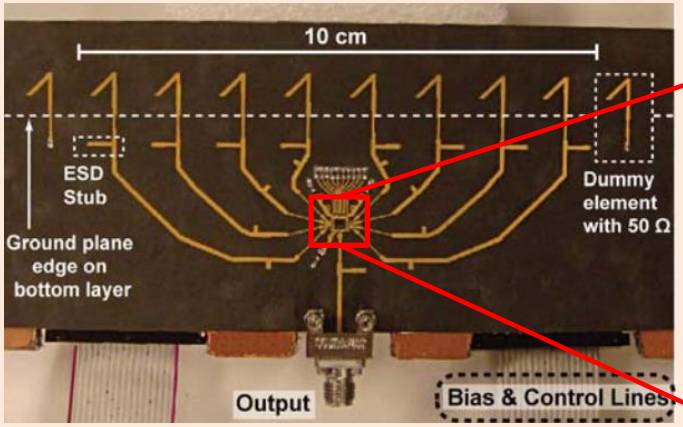
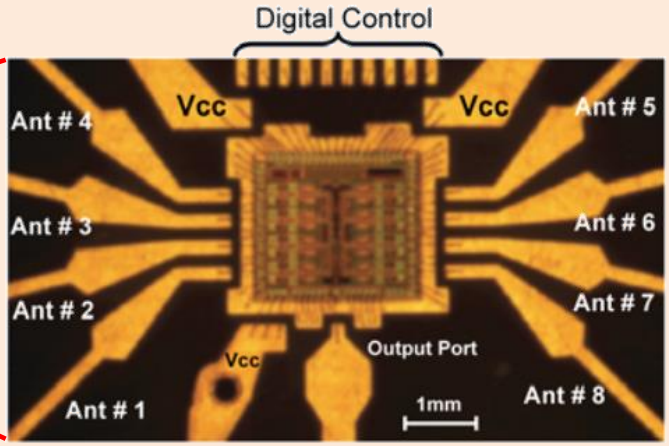
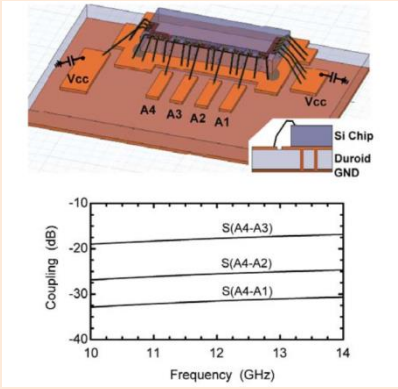
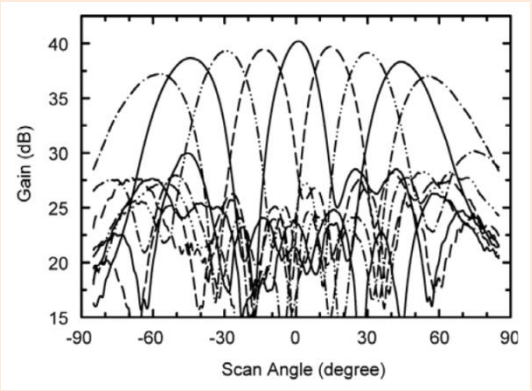
Ku Band Core Chip Integrated Into An Eight Element Phased Array



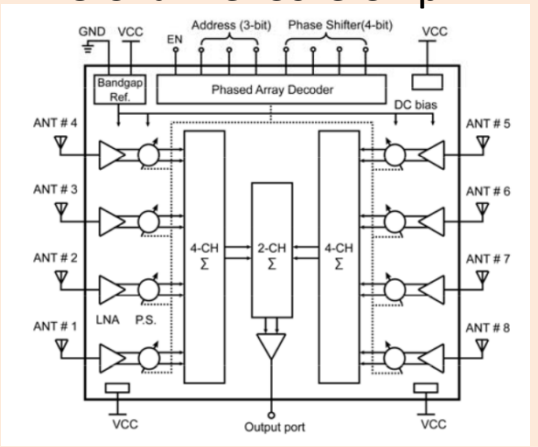






- Use wire bonds for the first level interconnect.
- Uses RT Duroid (Teflon) Substrate.
- Example of a packaging solution with the IC integrated with the antenna.

8 Channel Core Chip



Y.A. Atesal, et. al., "X/Ku-band 8-element phased arrays based on single silicon chips," IEEE Int. Microwave Symposium Digest, May 23-28, 2010, Anaheim, CA

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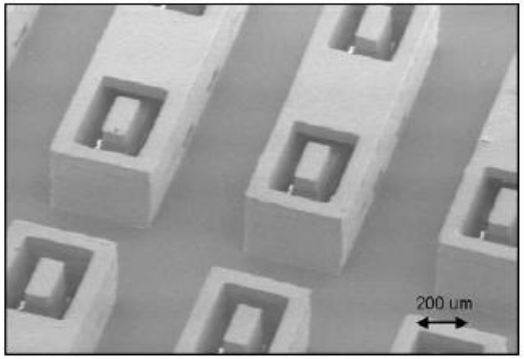
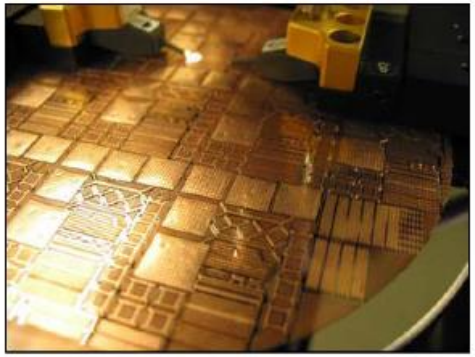
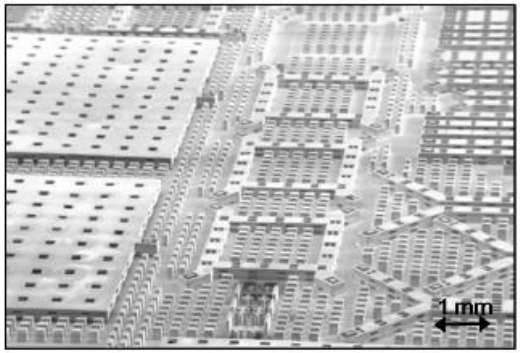
A Technology With Application To 5G Packaging Is 3D MERFS



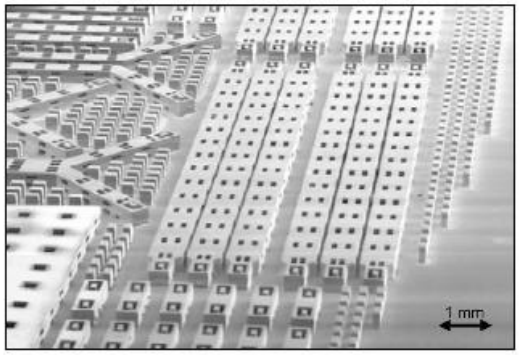
Short Recta-Coax used as "Launch" De-imbedding Test Structures



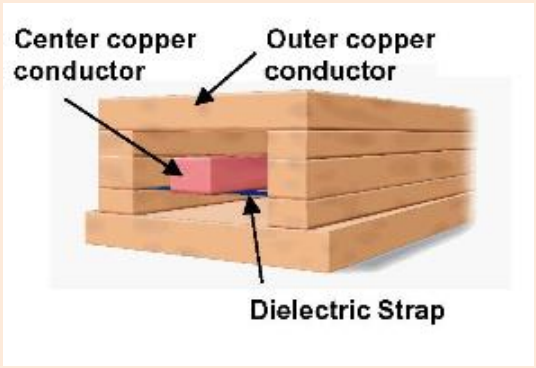
6-Inch 3-D MERFS Wafer on RF Probe Station

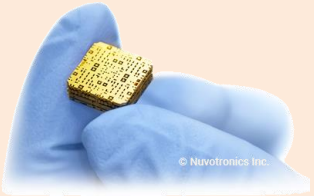


Cavity Resonators (left), Hybrid Couplers (center)



Isolation test structures (middle left), Attenuation test structures (center)





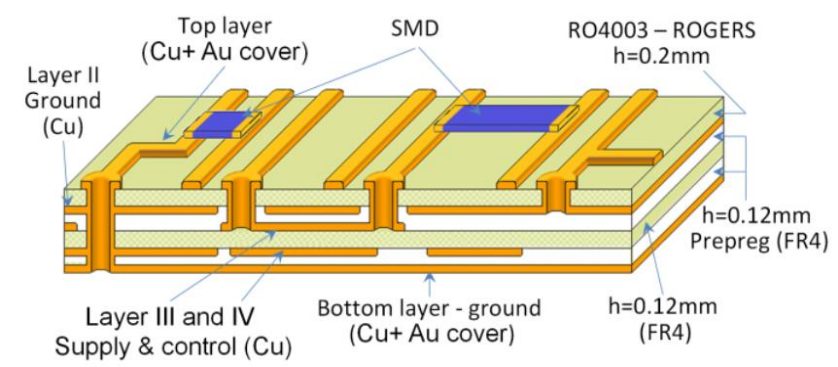
4 baluns, 10 splitters, 24 interconnects, 16 feeds

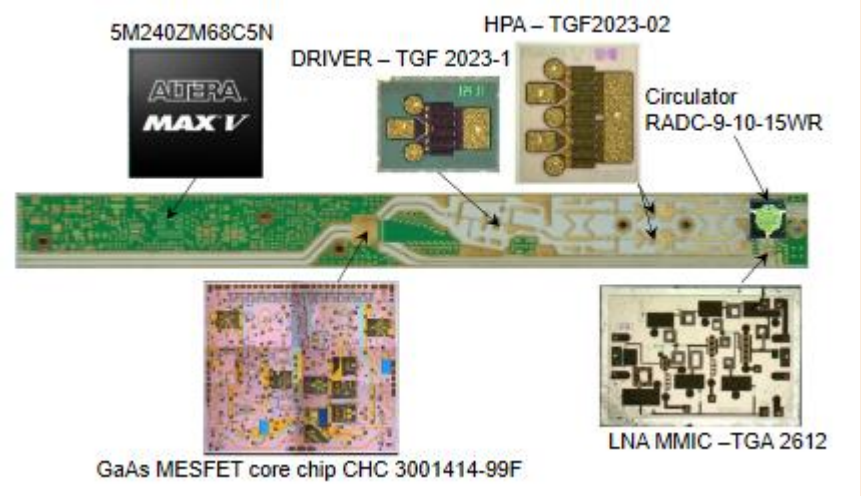
A supplier of 3D MERFS is Nuvotronics.com

- They allow for significant increase in packaging density.
- Critical for mmW phased arrays for 5G systems.

J. Evans, "3-D Micro Electro Magnetic Radio Frequency Systems (3-D MERFS) and other DARPA RF MEMS Programs," IEEE Compound Semiconductor Integrated Circuit Symposium, Nov. 12-15, 2006.

Example Of The PCB Material Stack Up For T/R Module



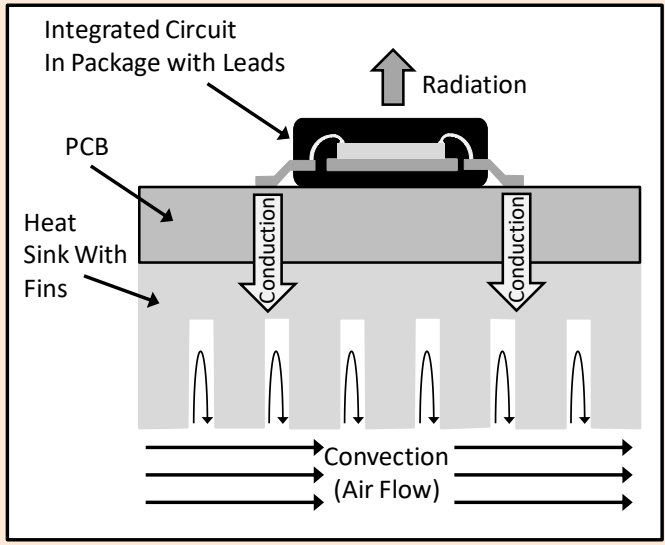


- Used a mix of high quality Rogers Corp RO4003 and FR-4 Layer with FR-4 Prepreg layers.
- Used to types of blind vias which increases the PCB fabrication process.
- High power amplifiers are impedance matched on the substrate to individual FETs for the driver and high power amplifier stages.

D. Gryglewski, "A 10W GaN based X-band T/R module for AESA," *International Conference on Microwave, Radar and Wireless Communications*, Krakow, Poland, May 9-11, 2016.

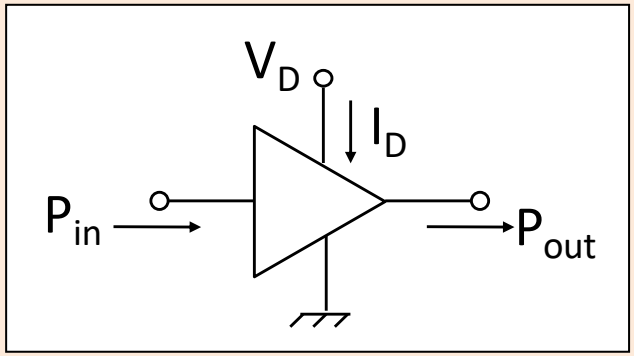
Section 6: Heat Transfer For Microwave and Millimeter-wave Packaging

- 6.1 Power Added Efficiency
- 6.2 Example: Power Dissipated In An Integrated Circuit
- 6.3 Heat Transfer and Reliability
- 6.4 Calculating Junction Temperature
- 6.5 Heat Spreading
- 6.6 Using Spice Simulator For Junction Temperature Simulation



Section 6.1: Power Added Efficience (PAE)
PAE Is A Measure Of The Effectiveness of An HPA To Generate Signal Output Power

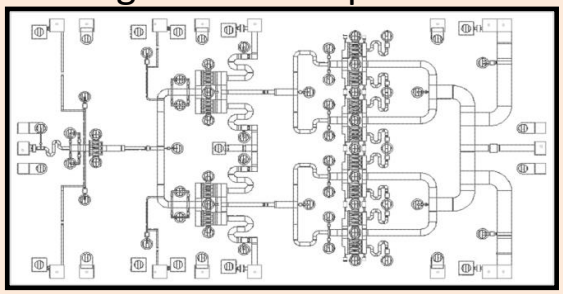
Block Diagram Of A High Power Amplifier



$$P_{DC} = V_D \cdot I_D$$

$$PAE = \eta = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}} = \frac{P_{RFOUT} - P_{RFIN}}{V_D \cdot I_D}$$

Layout of A High Power Amplifier For 28-30GHz



Where:
η = Power added efficiency, PAE
P_{RFOUT} = RF output power from the amplifier
P_{RFIN} = RF input power to the amplifier
P_{DC} = The dc power into the amplifier from the bias voltage and current

- Power Added Efficiency (PAE), which is expressed as a percentage, of an amplifier indicated how effective the amplifier is at converting the dc bias power into output power.
- In other words, it is a metric for how efficient the amplifier is in converting the bias power into output power, taking into account the input power

Section 6.2: Example Of Calculating The Power Dissipated In A High Power Amplifier

$$P_{DISS} = P_{DC} + P_{RFIN} - P_{RFOUT}$$

$$P_{DISS} = \frac{P_{RFOUT} - P_{RFIN}}{\eta} + P_{RFIN} - P_{RFOUT}$$

It is possible to determine the dissipated power for most amplifiers using data supplied by the manufacturer.

EXAMPLE: Consider an amplifier that delivers an output power of 200mW with an input power of 10mW and uses a bias voltage of 5V and bias current of 200mA. The dc power is:

P_{DC} = 5V x 0.2A = 1.0 Watts

$$\eta = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}} = \frac{0.2W - 0.01W}{1.0W} = 0.19 \text{ or} 19\%$$

$$P_{DISS} = P_{DC} + P_{RFIN} - P_{RFOUT} = 1.0W + 0.01W - 0.2W = 0.81W$$

Section 6.3: Heat Transfer Relates To Device Reliability

One goal of a thermal design is to achieve a required level of reliability (i.e. operating life time of the device) given the device dissipated power and junction temperature.

Arrhenius Equation

$$R = Ae^{(-E_a/kT)}$$

Where:
R = Rate at which the diffusion process occurs
A = Scaling constant
Ea = Activation energy
k = Boltzmann's constant = 8.617×10^{-5} (eV/K)
T = temperature, Kelvin

Derivation Of The Acceleration Factor Equation

$$MTTF_H \propto \frac{1}{R_H} = \frac{1}{A} e^{(E_a/kT_H)}$$

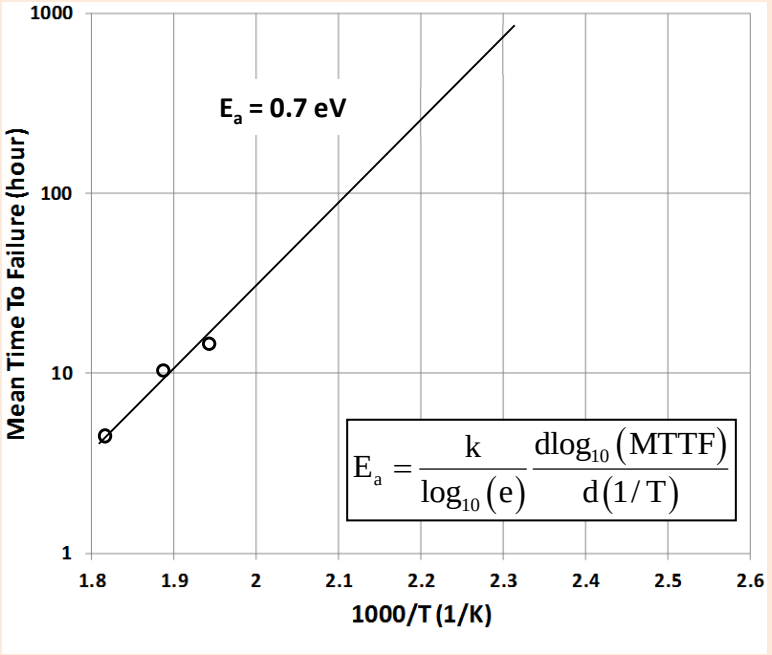
$$MTTF_L \propto \frac{1}{R_L} = \frac{1}{A} e^{(E_a/kT_L)}$$

$$MTTF_L = MTTF_H \exp\left[\frac{E_a}{k}\left(\frac{1}{T_L} - \frac{1}{T_H}\right)\right]$$

- Given the reliability at an elevated temperature, it is possible to estimate the reliability at a lower temperature using the Acceleration Factor equation.

Example Of Using The Acceleration Factor Equation

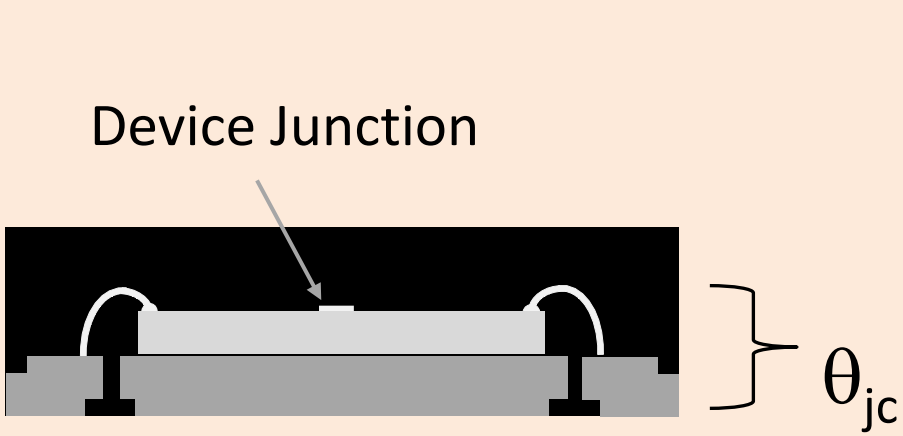
- As an example of its usefulness, consider the case of a semiconductor device that has a 500 hours lifetime at a junction test temperature of 160 °C with an activation energy, Ea of 0.7 eV. It is possible to find the lifetime if it is operated at a junction temperature of 60 °C as

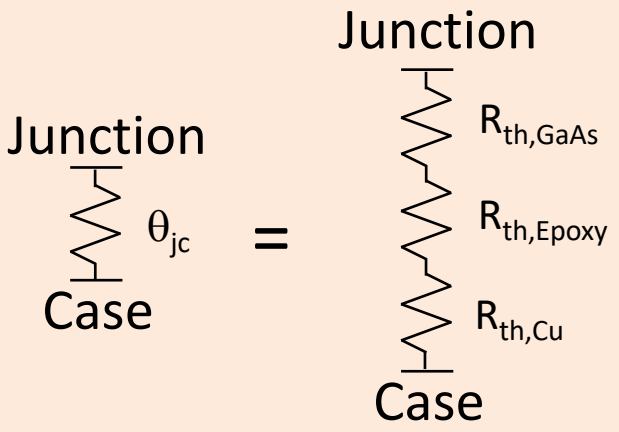


$$MTTF_L = MTTF_H \exp\left[\frac{E_a}{k}\left(\frac{1}{T_L} - \frac{1}{T_H}\right)\right]$$

$$MTTF_L = 1000 \exp\left[\frac{0.7}{8.617x10^{-5}}\left(\frac{1}{(273+60)} - \frac{1}{(273+160)}\right)\right] = 2.79x10^5 \text{ hours} = 31.9 \text{ years}$$

Section 6.4: Calculating The Junction Temperature Of The Semiconductor Device



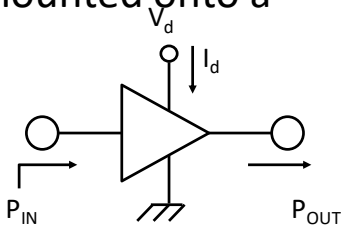


$$\text{Junction Temp} = T_{junction} = T_{case} + P_{DISS}\theta_{jc}$$

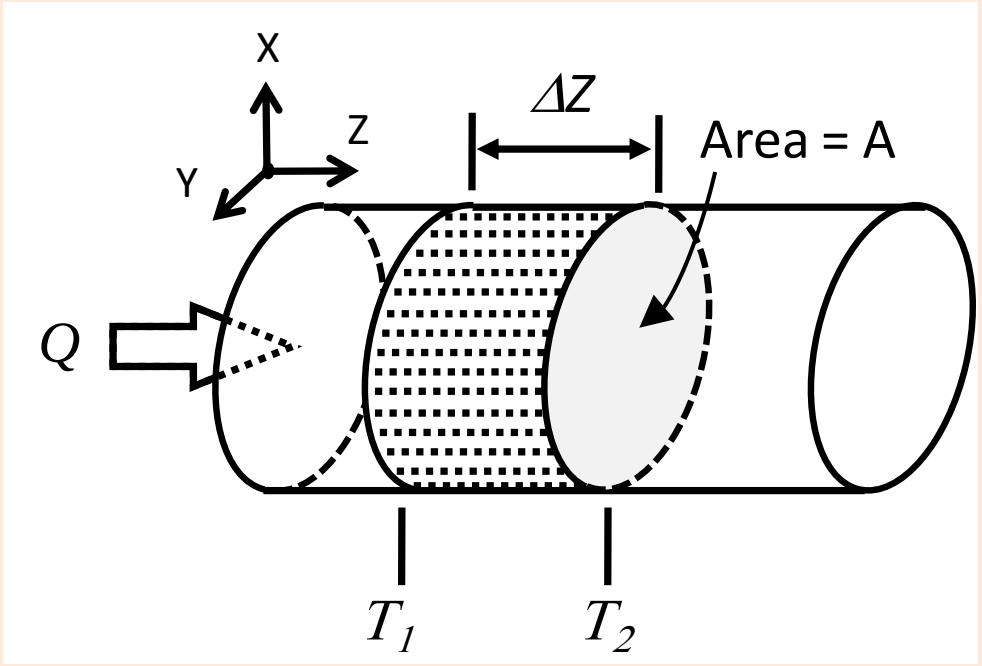
Example: Calculate the junction temperature of a 0.5W QFN packaged amplifier with 20dB gain, q_{jc} = 12 °C/W, bias voltage of Vd=5V, bias current of Id=750mA that is mounted onto a motherboard at a temperature of 40 °C.

$$P_{DISS} = P_{DC} - P_{RFOUT} = 5V \text{ x} 0.75A - 0.5W = 2.75W$$

$$T_{junction} = T_{mount} + P_{DISS}\theta_{jc} = 40\ C + 2.75W \text{ x} 12\ C/W = 73°C.$$



Thermal Conductivity



$$Q = -kA\frac{\Delta T}{\Delta Z} = -kA\frac{T_2 - T_1}{\Delta Z}$$

$$\Delta T = T_2 - T_1 = \frac{Q\Delta x}{kA}$$

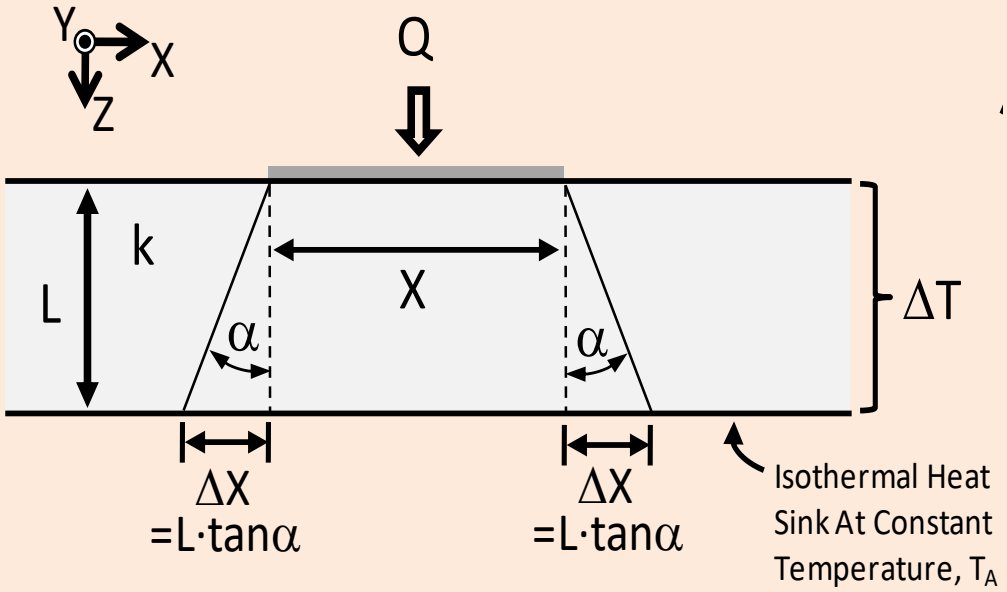
And

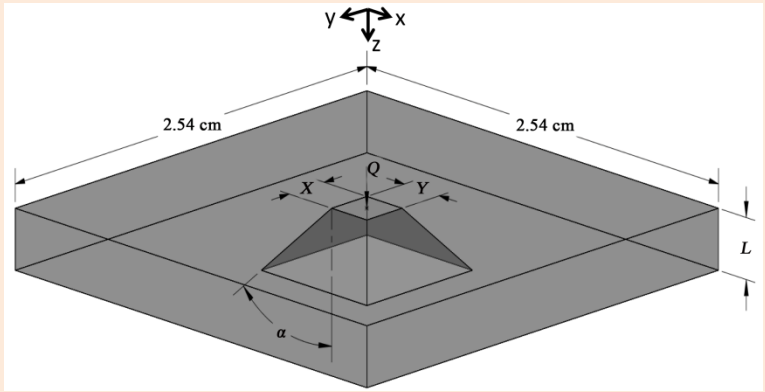
$$\text{Heat Flux} = q = \frac{Q}{A} = -k\frac{\Delta T}{\Delta Z}$$

- Jean-Baptiste Fourier (1768-1830) developed the first heat transfer equation.

Where:
Q = heat power (Watts or W)
k = thermal conductivity (W/mK)
A = cross-sectional area of heat flow (m^2)
$\Delta T/\Delta z$ = thermal gradient in the material (K/m)
$\Delta T = T_2 - T_1$ = temperature difference (K)
Δz = thickness of the section of material (m)
q = heat flux (W/m^2)

Section 6.5: Single Layer Heat Spreading Heat To An Isothermal Heat Sink





$$\Delta T = T_2 - T_1 = \frac{Q\Delta Z}{k(X \cdot Y)}$$

Equation A

$$X' = X + 2L \cdot \tan\alpha$$

$$Y' = Y + 2L \cdot \tan\alpha$$

Equation B

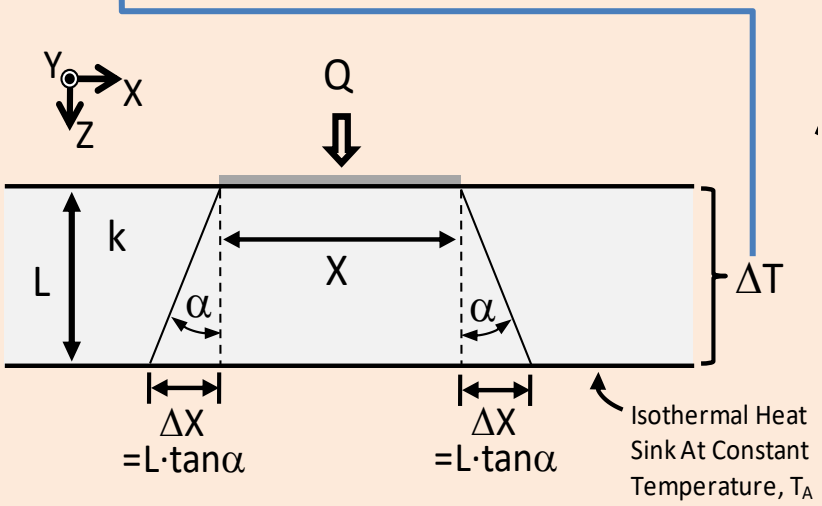
Where X' and Y' are the x and y dimensions on the bottom of the layer below the heat source.

This derivation follows the procedure outlined in:
R. L. Sturdivant, A.J. Bogdon, E.K.P. Chong, "A Simple Closed Form Solution to Single Layer Heat Spreading Angle Appropriate for Microwave Hybrid Modules," *Journal of Electronics Cooling and Thermal Control*, 2016, 5, 52-61.

Equation For The Temperature Drop In A Single Layer Material

Plugging Equations B into Equation A, We Obtain:

$$\Delta T = \frac{QL}{kA} = \frac{QL}{k\left(X + 2L\tan\alpha\right)\left(Y + 2L\tan\alpha\right)}$$

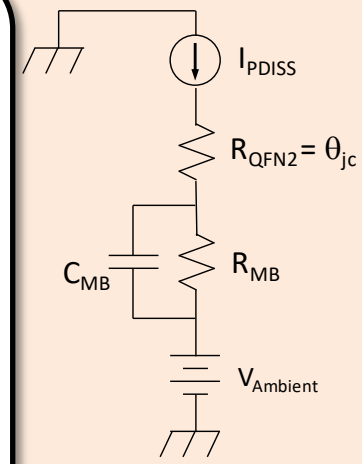


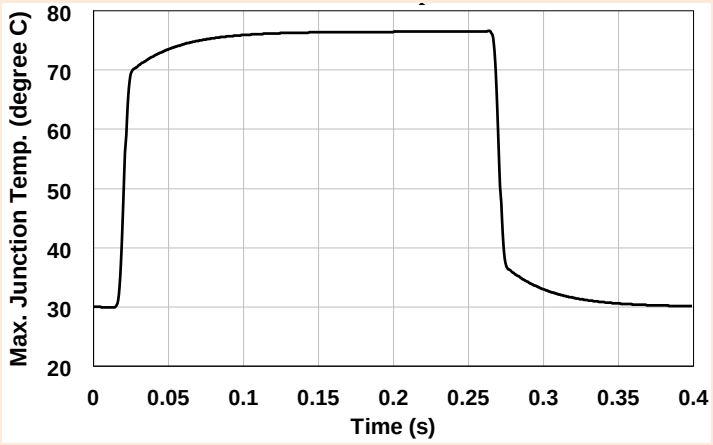
- For conservative estimates of the temperature rise, chose $\alpha = 0°$
- For more realistic estimates choose $\alpha = 20\text{-}35°$
- Others suggest 45° spreading angle

B. Guenin, (2003) The 45 Heat Spreading Angle—An Urban Legend? *Electronics Cooling*, **9**, 10-12.
Y. Xu, D.C. Hopkins, (2014) Misconception of Thermal Spreading Angle and Misapplication to IGBT Power Modules. *IEEE Applied Power Electronics Conference*, Fort Worth, 16-20 March 2014, 545-551. http://dx.doi.org/10.1109/apec.2014.6803362
C.R. Zimmer, (1983) Computer Simulation of Hybrid Integrated Circuits Including Combined Electrical and Thermal Effects. *Electro-Component Science and Technology*, **10**, 171-176. http://dx.doi.org/10.1155/APEC.10.171
R.F. David, (1977) Computerized Thermal Analysis of Hybrid Circuits. *IEEE Transactions on Parts, Hybrids, and Packaging*, **13**, 283-290. http://dx.doi.org/10.1109/TPHP.1977.1135213

Section 6.6: Using Spice Electric Circuit Simulators For Thermal Simulation

As an example, consider an LNA with a bias voltage of 5V and a current of 160mA dissipates 0.8W so the current, I_{PDISS}, is 0.8A. The manufacturer datasheet for the LNA gives the q_{jc} as 48 °C/W, which is represented in the schematic as the thermal resistance, R_{QFN2}. The motherboard has a thermal capacity, C_{MB}, of 0.003 W•s/°C and thermal resistance, R_{MB}, of 10 °C/W. Finally, the motherboard is connected to a heat sink at an ambient temperature of 30 °C. The heat sink is shown in the figure as a DC bias, $V_{Ambient}$. Circuit simulation determined that the junction temperature for a constant thermal dissipation is 76.4 °C. Figure 9.7(b) shows the transient response to a pulsed heat source. The results show that the thermal rise time is about 0.1s.





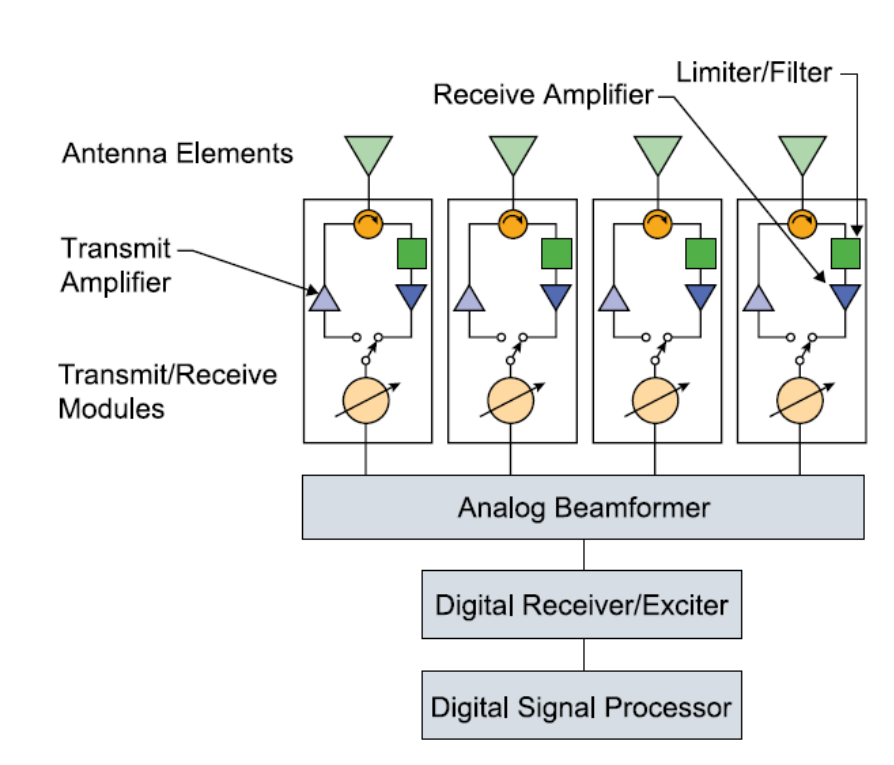
Parameter Type	Units for heat transfer	Units in the circuit simulator
Thermal Resistance	°C/W	Ohms
Thermal Mass	J/°C	Farads
Dissipated Power	Watts	Amps
Temperature	°C	Volts

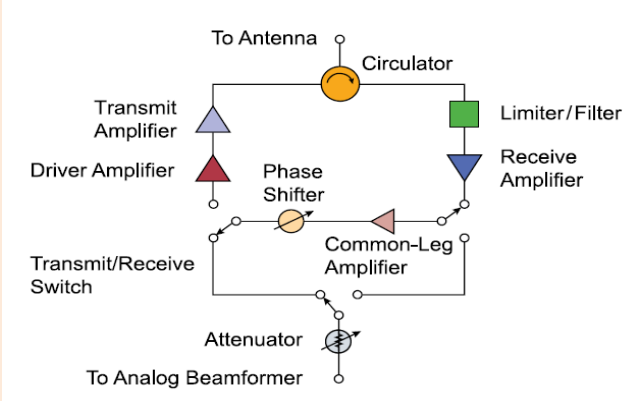
- Circuit simulation determined that the junction temperature for a constant thermal dissipation is 76.4 °C.
- The figure shows the transient response to a pulsed heat source. The results show that the thermal rise time is about 0.1s.

Section 7: Phased Arrays For 5G

- 7.1 Architecture 1: Analog Phase Shift At Each Element
- 7.2 Architecture 2: Sub Array Beam Steering
- 7.3 Architecture 3: Digital Beam Forming
- 7.4 Concluding Example of 5G Phased Array

Section 7.1: Analog Phase Shifting At Each Element

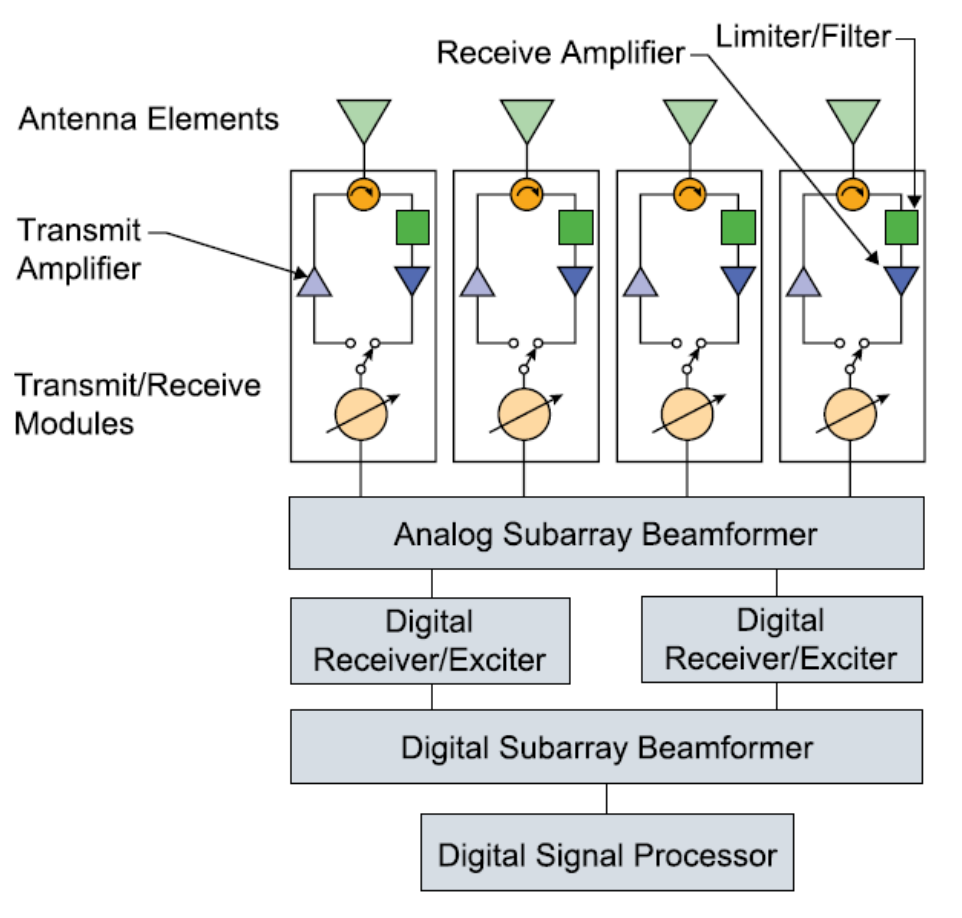




- Active phased array uses T/R modules at every element and analog beam former.
- Difficult to achieve multiple simultaneous beams.
  - Requires a separate analog beam former for each unique antenna beam.
  - Significant packaging challenge for arrays with more than three analog beam formers

J. Herd, M.D. Conway, "The evolution to modern phased array architectures," *Proceedings of the IEEE*, Vol. 104, No.3, March 2016/

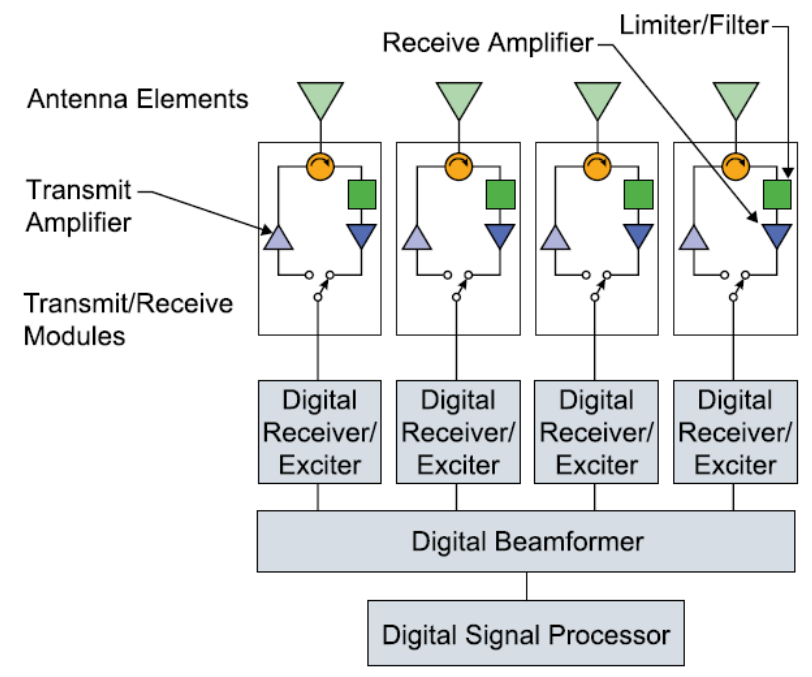
Section 7.2: Sub Array Digital Beam Forming Beam Steering



- Uses T/R modules at each antenna element in the array.
- Digital receiver and exciters are used at each subarray.
- Allows for simultaneous antenna beams from each sub array.
- Drawback: Grating lobes can be an issue requiring subarray overlapping

J. Herd, M.D. Conway, "The evolution to modern phased array architectures," *Proceedings of the IEEE*, Vol. 104, No.3, March 2016/

Section 7.3: Digital Beam Forming



- Element level digital phased array architecture.
- Phase shifting is performed digitally which means arbitrary digital delays can be applied to each element.
- Any number of simultaneous beams can be formed.

Benefits:

1) Improved adaptive pattern nulling (helps with interference issues).
2) Multiple simultaneous beams over the full scan volume.
3) Improved calibration.
4) Low side lobe levels
5) Array element pattern corrections can be easily implemented.

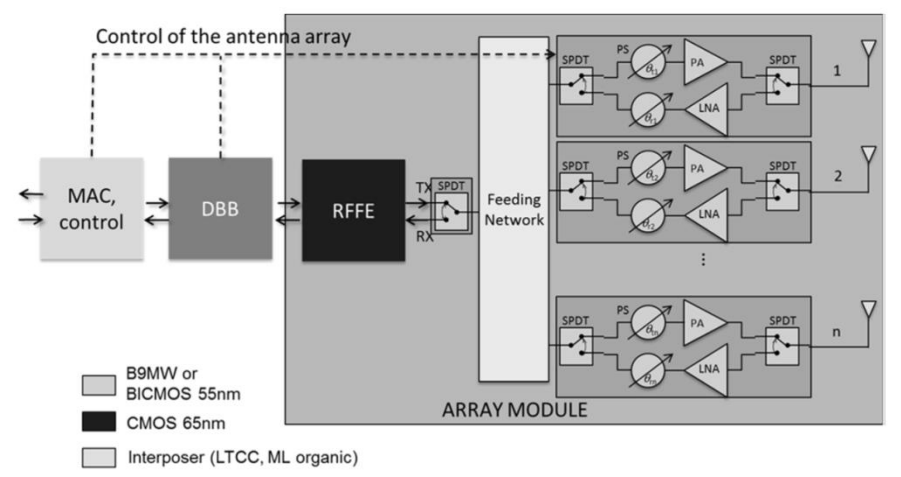
Drawbacks:

1) Requires RF digitizers at each element in the array which can be a packaging challenge
2) Power required by digitizers
3) Data bandwidth from the array can be enormous

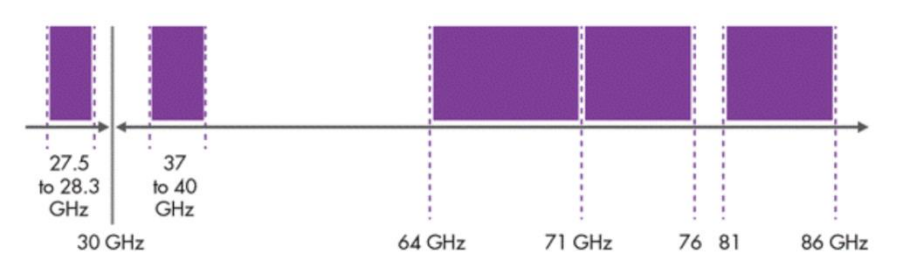
J. Herd, M.D. Conway, "The evolution to modern phased array architectures," *Proceedings of the IEEE*, Vol. 104, No.3, March 2016/

W. Hong, "Limitations of phased arrays for 5G wireless communications, *IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*, San Diego, CA, July 9-14, 2017.

Section 7.4: Small Cell Access Point Investigated In Europe Uses AESAs At Millimeter-wave



Overall Architecture Of The Millimeter-wave Access Point



Frequency bands being investigated as possible application of this architecture.

- This architecture was developed as part of the European project MiWaveS.
- This project aims to improve reconfigurability and performance of the mmW radio modules in the front end of small cell access points.
- The system is an AESA.

V. Puyal, “A Broad-band 55-nm BiCMOS T/R switch cor mmW 5G small cell access point,” IEEE Int. New Circuits and Systems Conf., Vancouver, BC, Canada, June 26-29, 2016,.

Section 8: Conclusions

- 8.1 Description of Heterogeneous Integration
  - One Motivator for Heterogeneous Integration
  - What are III-V semiconductors
- 8.2 Examples Of Several Heterogeneous Packaging Technologies
- 8.3 Summary And Concluding Remarks

Section 8.1 Heterogeneous Integration

A Method To Achieve Performance, Size, And Cost Targets For Large Scale 5G Deployment

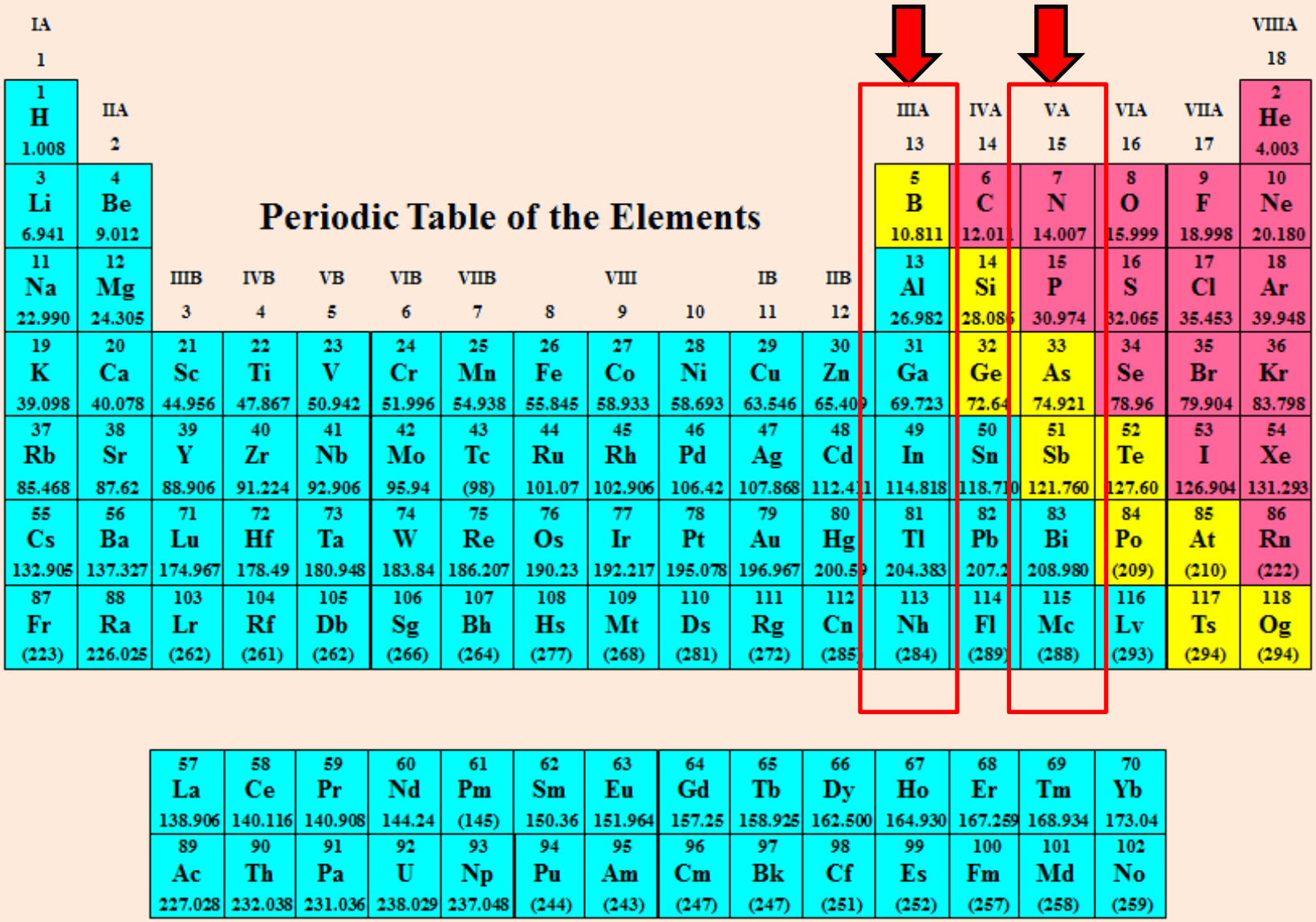
- Several development efforts have been funded to develop highly integrated packaging for millimeter-wave applications.
  - –DAPRA: Diverse Accessible Heterogeneous Integration (DAHI)
  - –DARPA: Compound Semiconductor Materials on Silicon (COSMOS)
  - –HiTek and SicFab (Germany): SiGe and InP Chip Integration
- These efforts seek to use wafer scale integration methods for circuits and systems from 30-500GHz.

One Of The Motivators For Heterogeneous Integration Is To Leverage Each Semiconductor Process For Its Particular Capabilities

		III-V Semiconductors			
Technologies	**Si CMOS**	**GaAs HEMT**	**GaN HEMT**	**InP HEMT**	**InP HBT**
Applications	• High-density integrated memory • High-density control and logic • Self-calibration and self-testing • Active dynamic load	• Microwave and mmW medium PAs • Low-noise amplifiers (LNAs) • Microwave transceivers	• Microwave and mmW high-PAs • High-power switches, power converters, and phase shifters • High-linearity switches • High-dynamic-range front ends • High survivability	• mmW and sub-mmW LNAs • Low-noise modules • Low-loss switches	• mmW and sub-mmW PAs • High-speed mixed-signal DACs and ADCs • mmW and sub-mmW transceivers • Highly linear circuits

- Each semiconductor processing technology has its own capabilities and applications.
- What is needed is the ability to integrate these capabilities to solve a new set of challenges such as 5G systems.

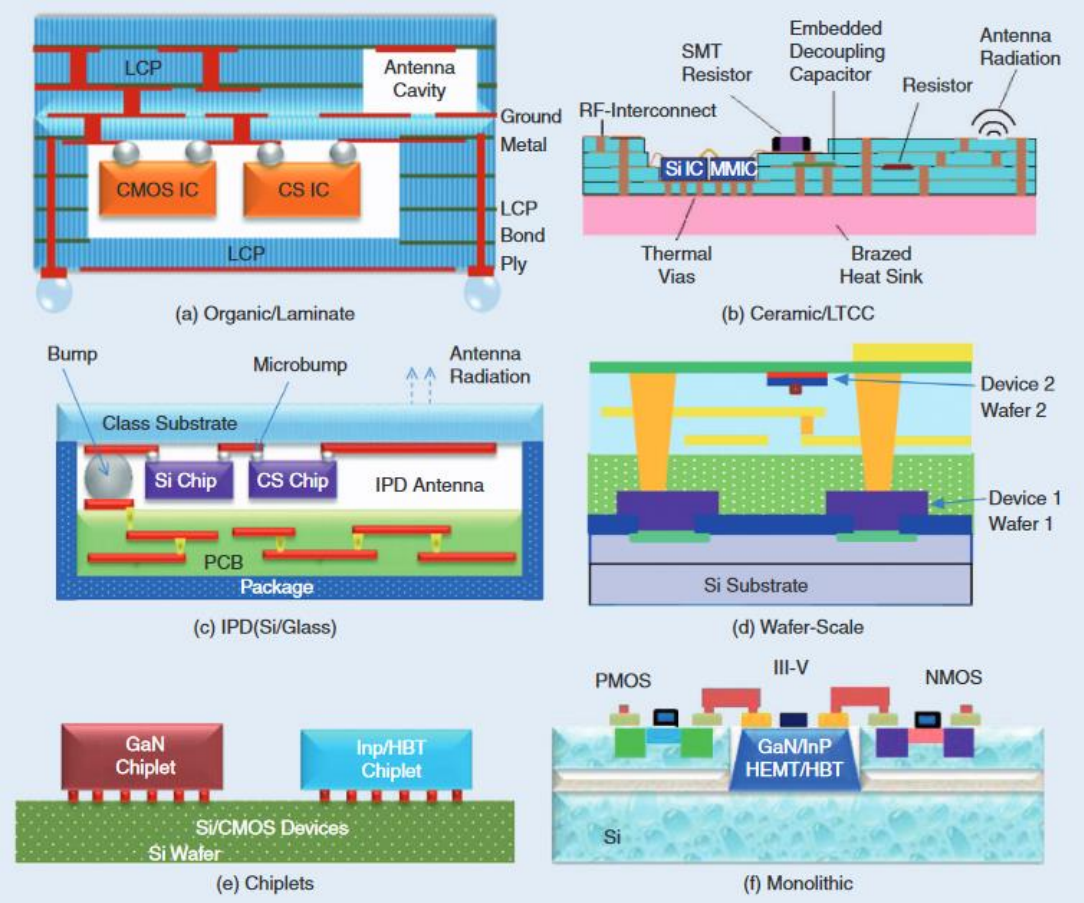
Periodic Table Of The Elements



IA 1	IIA 2	IIIB 3	IVB 4	VB 5	VIB 6	VIIB 7	8	VIII 9	10	IB 11	IIB 12	IIIA 13	IVA 14	VA 15	VIA 16	VIIA 17	VIIIA 18
1 H 1.008																	2 He 4.003
3 Li 6.941	4 Be 9.012											5 B 10.811	6 C 12.01	7 N 14.007	8 O 15.999	9 F 18.998	10 Ne 20.180
11 Na 22.990	12 Mg 24.305											13 Al 26.982	14 Si 28.086	15 P 30.974	16 S 32.065	17 Cl 35.453	18 Ar 39.948
19 K 39.098	20 Ca 40.078	21 Sc 44.956	22 Ti 47.867	23 V 50.942	24 Cr 51.996	25 Mn 54.938	26 Fe 55.845	27 Co 58.933	28 Ni 58.693	29 Cu 63.546	30 Zn 65.409	31 Ga 69.723	32 Ge 72.64	33 As 74.921	34 Se 78.96	35 Br 79.904	36 Kr 83.798
37 Rb 85.468	38 Sr 87.62	39 Y 88.906	40 Zr 91.224	41 Nb 92.906	42 Mo 95.94	43 Tc (98)	44 Ru 101.07	45 Rh 102.906	46 Pd 106.42	47 Ag 107.868	48 Cd 112.411	49 In 114.818	50 Sn 118.710	51 Sb 121.760	52 Te 127.60	53 I 126.904	54 Xe 131.293
55 Cs 132.905	56 Ba 137.327	71 Lu 174.967	72 Hf 178.49	73 Ta 180.948	74 W 183.84	75 Re 186.207	76 Os 190.23	77 Ir 192.217	78 Pt 195.078	79 Au 196.967	80 Hg 200.59	81 Tl 204.383	82 Pb 207.2	83 Bi 208.980	84 Po (209)	85 At (210)	86 Rn (222)
87 Fr (223)	88 Ra 226.025	103 Lr (262)	104 Rf (261)	105 Db (262)	106 Sg (266)	107 Bh (264)	108 Hs (277)	109 Mt (268)	110 Ds (281)	111 Rg (272)	112 Cn (285)	113 Nh (284)	114 Fl (289)	115 Mc (288)	116 Lv (293)	117 Ts (294)	118 Og (294)

57 La 138.906	58 Ce 140.116	59 Pr 140.908	60 Nd 144.24	61 Pm (145)	62 Sm 150.36	63 Eu 151.964	64 Gd 157.25	65 Tb 158.925	66 Dy 162.500	67 Ho 164.930	68 Er 167.259	69 Tm 168.934	70 Yb 173.04
89 Ac 227.028	90 Th 232.038	91 Pa 231.036	92 U 238.029	93 Np 237.048	94 Pu (244)	95 Am (243)	96 Cm (247)	97 Bk (247)	98 Cf (251)	99 Es (252)	100 Fm (257)	101 Md (258)	102 No (259)

Section 8.2 Examples Of Material Stackups For Advanced Multilayer, Multichip, and Heterogeneous Packaging

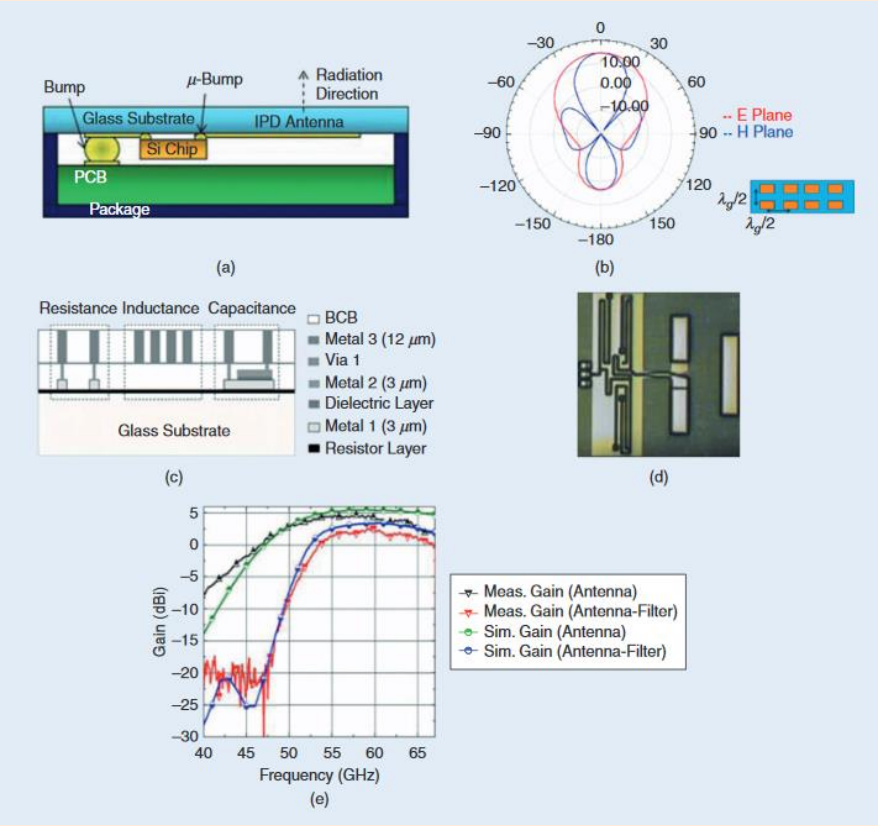


Examples of Heterogeneous Integration for mmW circuits

- (a) organic laminate-based packaging
- (b) low-temperataure co-fired ceramic (LTCC)-based
- (c) integrated passive device (IPD) (Si/glass)-based.
- (d) wafer-cale/epitaxy transfer
- (e) chiplets-based
- (f) monolithic integration

K. K. Samanta, "Pushing the envelope for heterogeneity," *IEEE Microwave Magazine*, March/April 2017, pp. 28-43.

An Example Is The Integrated Passive Devices (IPD) From STMicroelectronics

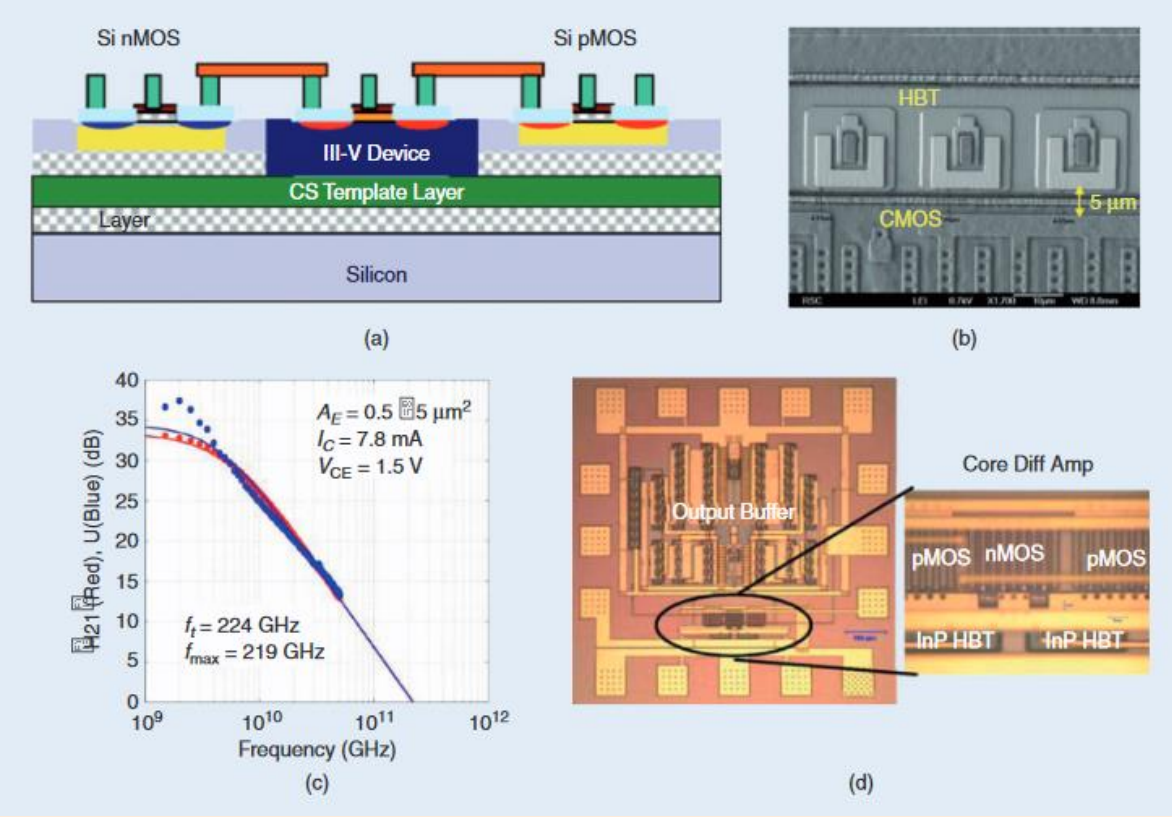


- Capable of integrating antennas due to the low dielectric constant and low loss tangent.
- Can be integrated with PCB to create higher levels of integration.
- Demonstrated 60GHz performance

K. K. Samanta, "Pushing the envelope for heterogeneity," *IEEE Microwave Magazine*, March/April 2017, pp. 28-43.

C. Calvez, et. al., "New millimeter wave packaged array on IPD technology," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, New Orleans, LA, USA, Jan 11-13, 2010.

Direct Monolithic Integration Allows For Low Inductance Interconnects, Low Conductor Losses, And Compact Size Which All Contribute To Enabling mmW Capabilities



- Direct Integration of Si CMOS and III-V transistors (InP HBT)
- Base material is Si wafers.

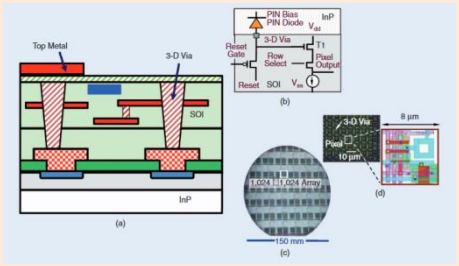
K. K. Samanta, "Pushing the envelope for heterogeneity," *IEEE Microwave Magazine*, March/April 2017, pp. 28-43.

T. E. Kazior , J. R. LaRoche , et al., " High performance mixed signal circuits enabled by the direct monolithic heterogeneous integration of InP HBT and Si CMOS on a silicon substrate," *IEEE J. Solid State Circuits*, vol. 44 , no. 10 , Oct. 20 0 9, pp. 1– 4.

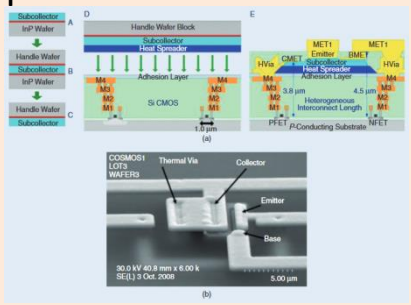
Other Methods For Highly Integrated Packaging For 5G Systems

- Wafer Bonding Integration
  - 3D wafer bonding integration of III-V and Si circuits
- Epitaxial-Transfer Integration
  - The epitaxial layer of the III-V semiconductor is transferred to Si substrates
- Chiplet Technology
  - Integrates chip scale devices (such as InP HBTs) onto silicon substrates.

Wafer Bonding Integration



Epitaxial Transfer Method

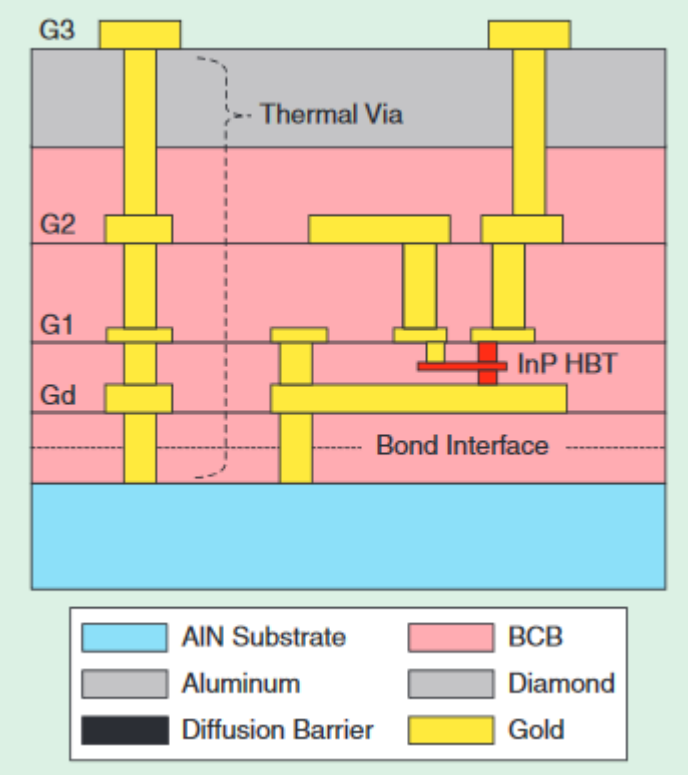


Cross-section Of Heterogeneous Chiplet Technology

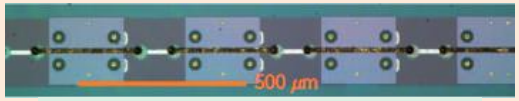
K. K. Samanta, "Pushing the envelope for heterogeneity," *IEEE Microwave Magazine*, March/April 2017, pp. 28-43.

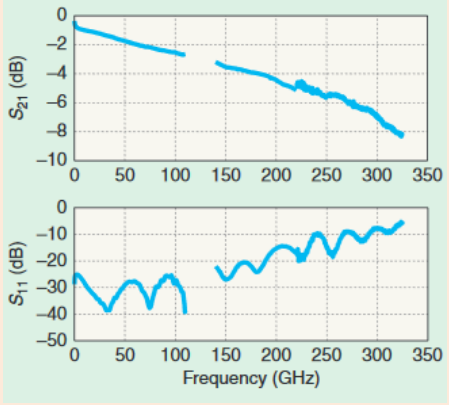
Wafer Bonding Process Integrating SiGe and InP HBT

Sketch Of Cross Section Of Transferred InPh HBT

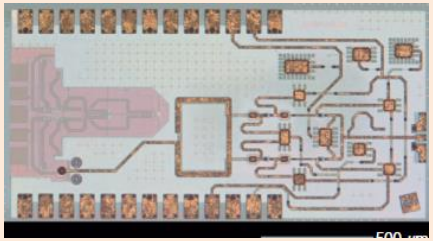


Fabricated And Measured Wideband RF Transitions Between InP and BiCMOS Regions





mmW Source at 328GHz SiGe VCO Integrated With InP Amplifier

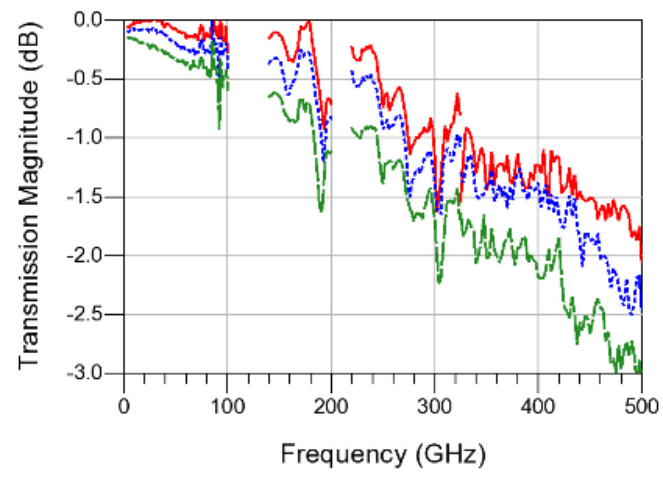


- Silicon first, low temperature wafer bonding process with thermal solutions for the heat generated in the InP devices.
- Process designed for low loss, wide band interconnects
- Allows for tight heterogeneous integration to 500GHz.

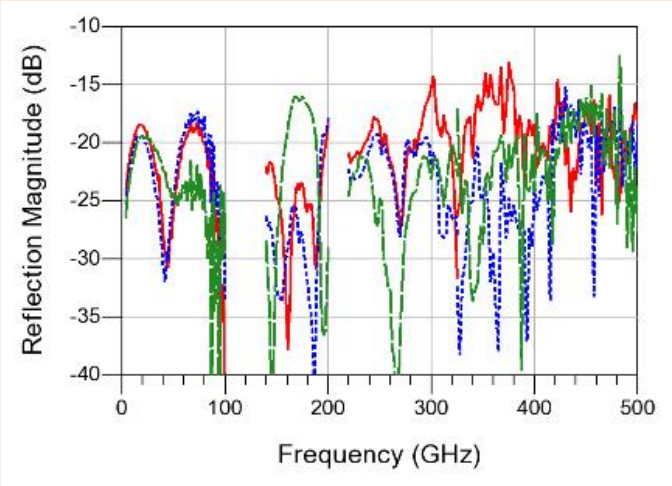
N. Weimann, M. Hossain, V. Krozer, W. Heinrich, M. Lisker, A. Mai, B. Tillack, “Tight focus toward the future,” *IEEE Microwave Magazine*, March/April 2017, pp. 74-82.

Flip Chips and Signal Transitions In Heterogeneous Integration Can Achieve 500GHz Bandwidth

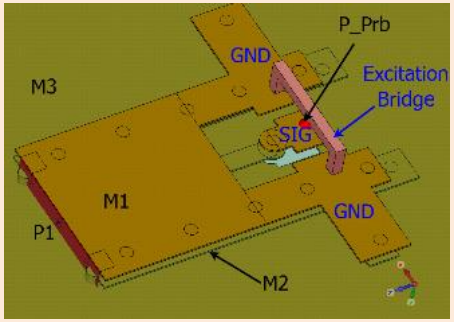
Measured Transition Transmission Magnitude



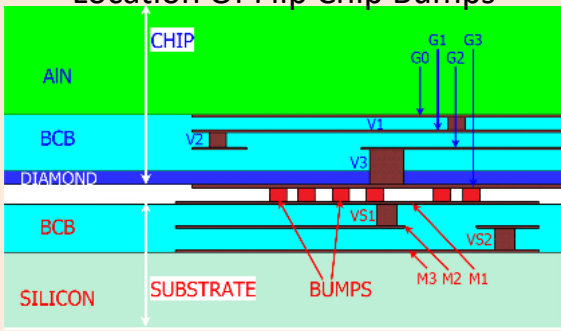
Measured Transition Reflection Coefficient



Model of One Of The Transitions



Package Cross Section Showing Location Of Flip Chip Bumps



- Flip chips and signal transitions are important to heterogeneous integration.
- It is possible to achieve 500GHz bandwidth.
- To Required Conditions For Wide Performance:

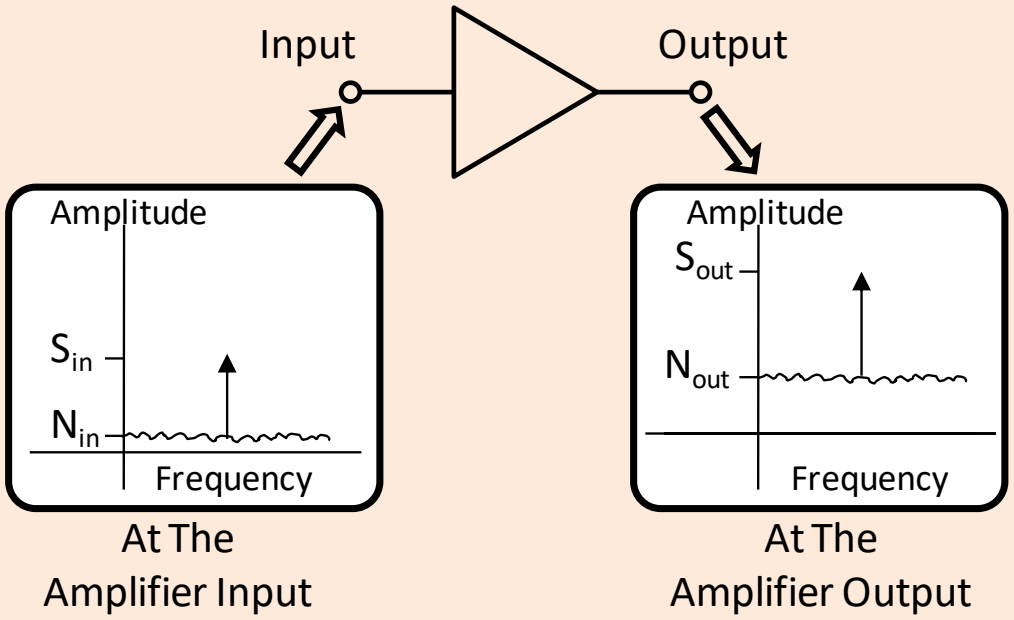
  1) Impedance matching over the full bandwidth.

  2) Suppression of excitation of higher order modes.

Section 8.3: Summary And Concluding Remarks

- Summary
  - Introduced 5G systems
  - Discussed how mmW packaging will be required
  - Fundamental of 5G packaging
  - Materials for 5G packaging
  - Transitions and interconnects
  - T/R modules
  - Heat transfer for 5G packaging
  - Phased arrays
  - Heterogeneous 3D packaging
- Concluding Remarks
  - Feel free to reach out to me to continue the discussion or if you have question or comments.
  - You may reach me by email

Appendix A: Cascaded Noise Figure



Noise factor is illustrated in the figure. It shows an amplifier with an input port and output port. It also shows the signal entering the input and exiting the output. The input signal has noise and the desired signal which are both amplified. In the process of amplification, the noise is increased which is calculated using

$$F = \text{Noise Factor} = \frac{S_{in} / N_{in}}{S_{out} / N_{out}}$$

Where:

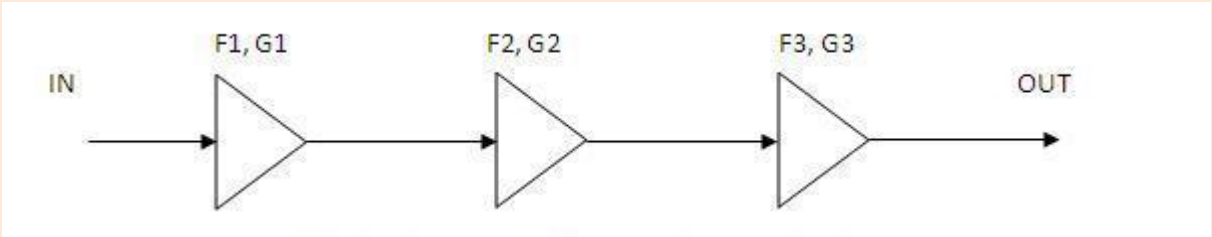
S_{in} = level of the signal at the input

S_{out} = level of the signal at the output

N_{in} = level of the noise at the input

N_{out} = level of the noise at the output

Low Noise Amplifiers And System Noise Figure



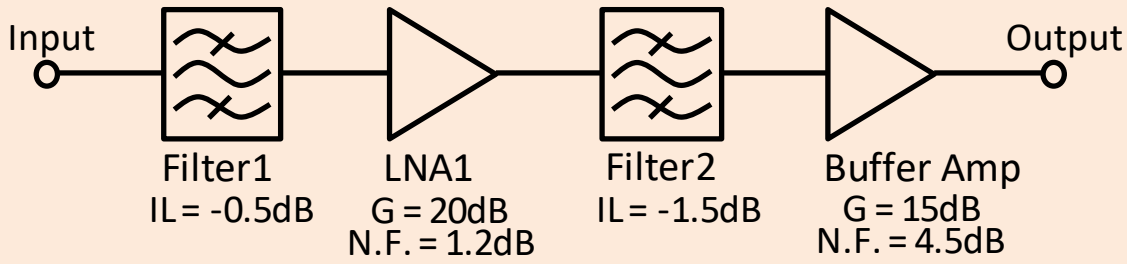
- Since a low noise amplifier imparts a relatively low amount of noise to the signal it amplifies, it can be used to set the overall noise figure of the module (and system).
- This is due to the fact that in a chain of components the noise figure is determined, in large part, by the first amplifier. The noise factir of a cascaded of components in a T/R module can be obtained using the Friis equation

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{G_1 G_2 \cdots G_{N-1}}$$

And the noise figure in dB is calculated using

$$NF(dB) = 10 \cdot \log_{10}(F)$$

Example: Find The Cascaded Noise Figure For The Components In The Figure



$$F_1 = F_{Filter1} = 10^{|ILFilter1|/10} = 10^{0.5/10} = 1.122$$
$$F_2 = F_{LNA1} = 10^{1.2/10} = 1.318$$
$$F_3 = F_{Filter2} = 10^{|ILFilter2|/10} = 10^{1.5/10} = 1.413$$
$$F_4 = F_{Buffer} = 10^{4.5/10} = 2.818$$

$$G_1 = G_{Filter1} = 10^{ILFilter1/10} = 10^{-0.5/10} = 0.891$$
$$G_2 = G_{LNA1} = 10^{20/10} = 100$$
$$G_3 = G_{Filter2} = 10^{ILFilter2/10} = 10^{-1.5/10} = 0.708$$
$$G_4 = G_{Buffer} = 10^{15/10} = 31.622$$

For passive element such as filters, attenuators, coupler, and circulators, the noise figure is taken to be the magnitude of the insertion loss.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} = 1.122 + \frac{1.318 - 1}{0.891} + \frac{1.413 - 1}{0.891 \cdot 100} + \frac{2.818 - 1}{0.891 \cdot 100 \cdot 0.708} = 1.512$$

$$NF(dB) = 10 \cdot \log_{10}(F) = 10 \cdot \log_{10}(1.512) = 1.796 dB$$

- Step 1: Convert dB values for gain and noise figure into gain factor and noise factor (i.e., not dB)
- Step 2: Plug into cascade equation to find the cascaded noise factor.
- Step 3: Convert the noise factor back to noise figure in dB