Programmable Logic Design

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Lecture 14:
CPLD and FPGA market view

Choose yourself and new technologies

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Wrocław University of Technology

EUROPEAN SOCIAL FUND

Project co-financed from the EU European Social Fund

Plan

- Xilinx family
  - CoolRunner II series
  - EasyPath-6 series
  - Spartan-6 series
  - Virtex-6 series
  - 7-th series
  - Extensible Processing Platforms

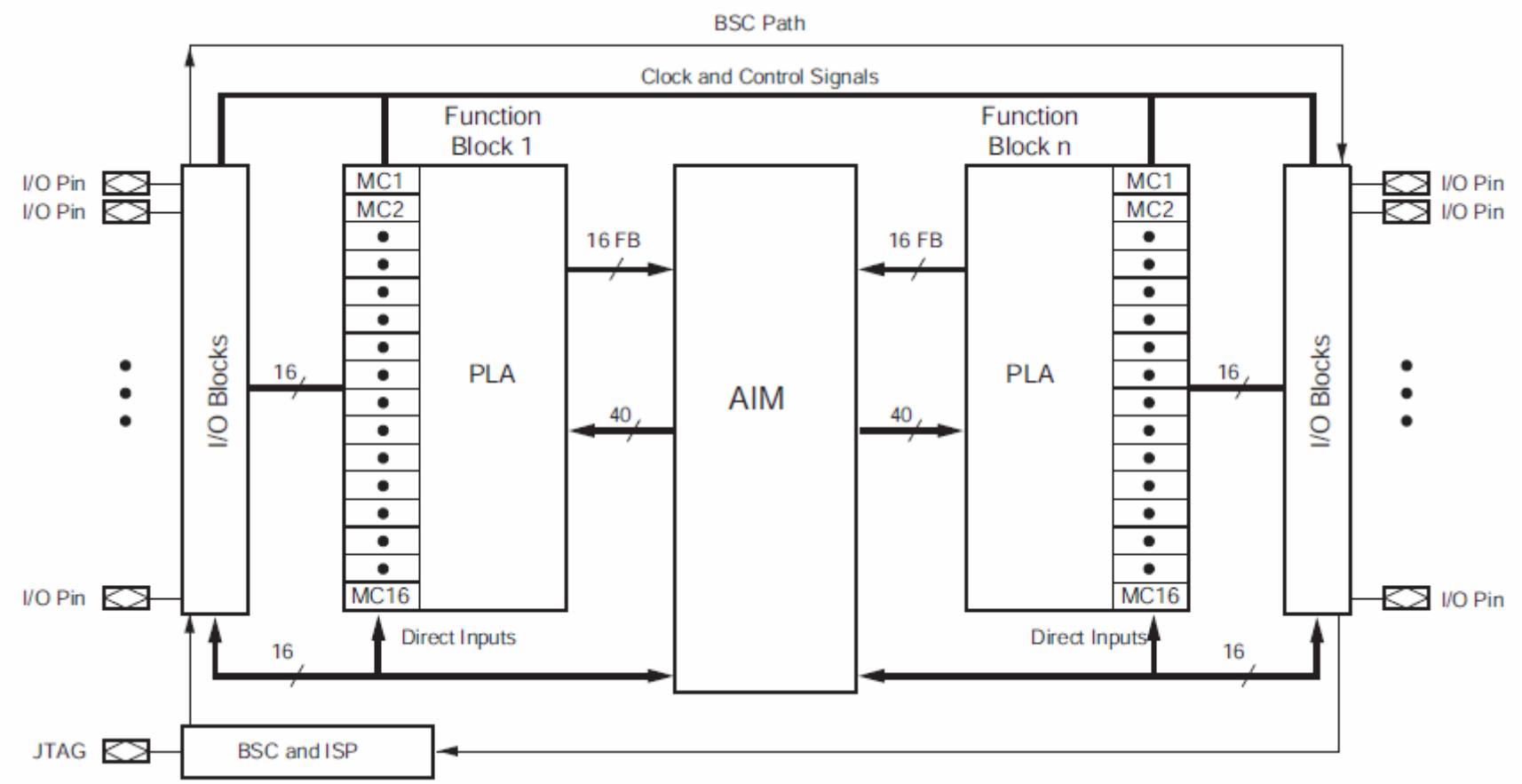
Xilinx family

Xilinx family

- Xilinx family of FPD consists of:
  - CPLD – CoolRunner II series
  - FPGA:
    - EasyPath-6 (low cost)
    - Spartan-6 (low end)
    - Virtex-6 (high end)

CoolRunner II series

CoolRunner II series - architecture



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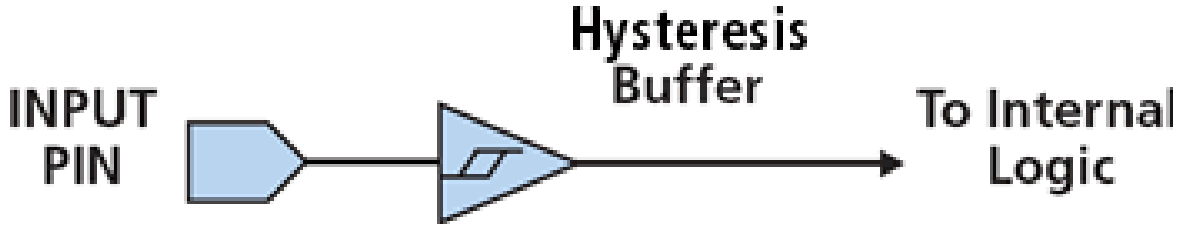
CoolRunner II series - features

- Multiple I/O banking (2-4):
  - Including different bus interface I/O voltage levels
  - Voltage translation of peripheral devices
  - Memory to microcontrollers
  - Communication between wired interfaces

CoolRunner II series - features

- Input hysteresis (500mV):
  - Improved noise immunity
  - Reduced power consumption
  - Superior signal integrity



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CoolRunner II series - features

- DualEDGE flipflops:
  - Distributes divided clock globally then double locally at macrocell
  - Use 2x clocking for double data rate applications
  - No additional insertion delay
  - Available in all CoolRunner-II CPLDs

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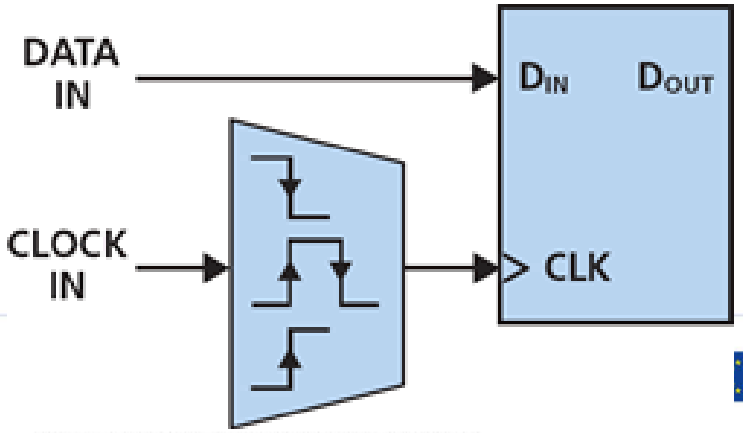



XILINX
VIRTEX
EasyPath-6

EasyPath-6 series - features

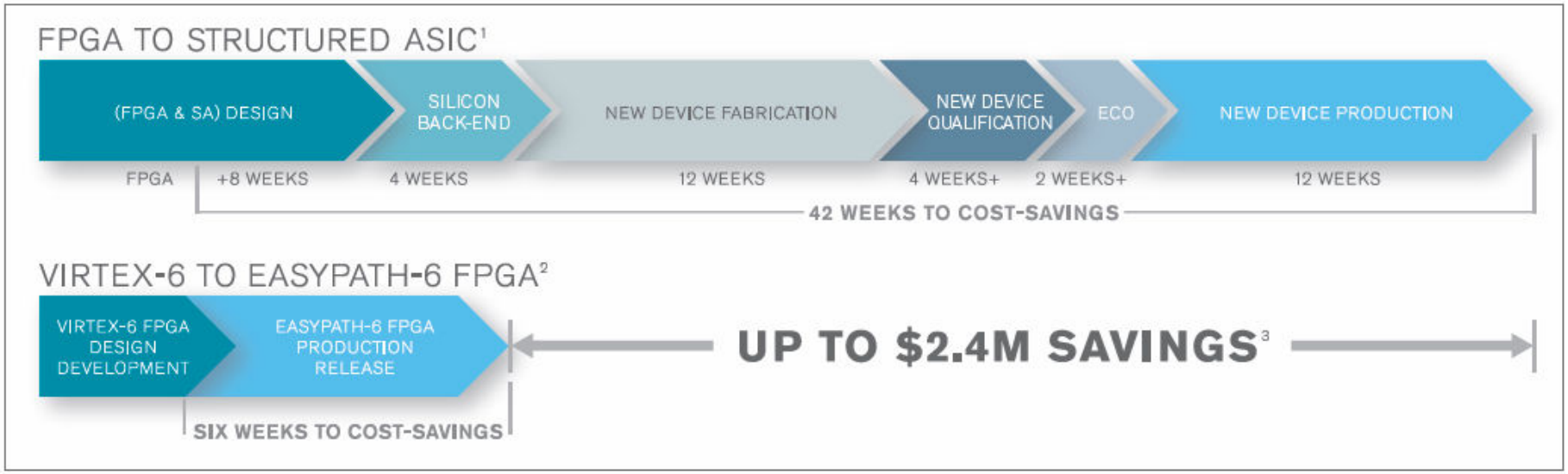
- EasyPath-6™ FPGAs offer a fast, simple and risk-free solution for cost reducing Virtex-6 FPGA designs.
- EasyPath-6 FPGAs deliver production volume devices in just six weeks with the lowest total product cost of any FPGA cost reduction solution.
- The cost savings are also available free of additional design constraints, re-engineering requirements, or re-layout of boards.

EasyPath-6 series - features

- EasyPath-6 FPGAs are architecturally equivalent to Virtex-6 FPGAs and match the FPGA datasheet specifications for functionality and timing.
- Unlike ASICs, the EasyPath-6 FPGA silicon requires no-requalification.
- Additionally, all Xilinx and third-party Intellectual Property (IP) for Virtex-6 FPGAs is supported by EasyPath-6 FPGAs without change or re-verification, and with no additional royalty, conversion or licensing fees.

EasyPath-6 series - features

TIME-TO-MARKET COMPARISON



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XILINX
SPARTAN

Spartan-6 series - features

- The Spartan®-6 family provides leading system integration capabilities with the lowest total cost for high-volume applications
- Spartan-6 is a lowcost programmable alternative to custom ASIC products with ease of use
- Good solution for high-volume logic designs, consumer-oriented DSP designs, and cost-sensitive embedded applications

Spartan-6 series - features

- Spartan-6 Family:
  - Spartan-6 LX FPGA: Logic optimized
  - Spartan-6 LXT FPGA: High-speed serial connectivity
- Designed for low cost:
  - Multiple efficient integrated blocks
  - Optimized selection of I/O standards
  - Staggered pads
  - High-volume plastic wire-bonded packages

Spartan-6 series - features

- Multi-voltage, multi-standard SelectIO™ interface banks
  - Up to 1,080 Mb/s data transfer rate per differential I/O
  - Selectable output drive, up to 24 mA per pin
  - 3.3V to 1.2V I/O standards and protocols
  - Low-cost HSTL and SSTL memory interfaces
  - Hot swap compliance
  - Adjustable I/O slew rates to improve signal integrity

Spartan-6 series - features

- High-speed GTP serial transceivers in the LXT FPGAs
  - Up to 3.125 Gb/s
  - High-speed interfaces including: Serial ATA, Aurora,
  - 1G Ethernet, PCI Express, OBSAI, CPRI, EPON,GPON, DisplayPort, and XAUI
- Integrated Endpoint block for PCI Express designs (LXT)
- Low-cost PCI® technology support compatible with the 33 MHz, 32- and 64-bit specification.

Spartan-6 series - features

- Efficient DSP48A1 slices
  - High-performance arithmetic and signal processing
  - Fast 18 x 18 multiplier and 48-bit accumulator
  - Pipelining and cascading capability
  - Pre-adder to assist filter applications
- Integrated Memory Controller blocks
  - DDR, DDR2, DDR3, and LPDDR support
  - Data rates up to 800 Mb/s (12.8 Gb/s peak bandwidth)
  - Multi-port bus structure with independent FIFO to reduce design timing issues

Spartan-6 series - features

- Abundant logic resources with increased logic capacity
  - Optional shift register or distributed RAM support
  - Efficient 6-input LUTs improve performance and minimize power
  - LUT with dual flip-flops for pipeline centric applications
- Block RAM with a wide range of granularity
  - Fast block RAM with byte write enable
  - 18 Kb blocks that can be optionally programmed as two independent 9 Kb block RAMs

Spartan-6 series - features

- Clock Management Tile (CMT) for enhanced performance
  - Low noise, flexible clocking
  - Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion
  - Phase-Locked Loops (PLLs) for low-jitter clocking
  - Frequency synthesis with simultaneous multiplication, division, and phase shifting
  - Sixteen low-skew global clock networks

Spartan-6 series - devices

Device	Logic Cells[1]	Configurable Logic Blocks (CLBs)			DSP48A1 Slices[3]	Block RAM Blocks		CMTs[5]	Memory Controller Blocks (Max)[6]	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices[2]	Flip-Flops	Max Distributed RAM (Kb)		18 Kb[4]	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540

Spartan-6 series – DSP48A1

- Spartan-6 FPGAs contain dedicated, full-custom, low-power DSP slices, combining high speed with small size, while retaining system design flexibility:
  - Up to 180 efficient, second generation DSP48A1 slices
  - High-performance arithmetic and signal processing
  - Each slice containing a fast 18 x 18 multiplier and a 48-bit accumulator capable of operating at 250 MHz speed
  - Pipelining and cascading capability
  - Pre-adder to assist filter applications
  - 40% lower power consumption: 1.38mW/ 100MHz at a 38% toggle rate


XILINX
VIRTEX

Virtex-6 series - features

- Virtex®-6 family provides the newest, most advanced features in the FPGA market
- Virtex-6 FPGAs contain many built-in system-level blocks
- Virtex-6 FPGAs offer the best solution for addressing the needs of:
  - high-performance logic designers,
  - high-performance DSP designers,
  - high-performance embedded systems designers with unprecedented logic, DSP, connectivity, and soft microprocessor capabilities.

Virtex-6 series - features

- Three sub-families:
  - Virtex-6 LXT FPGAs: High-performance logic with advanced serial connectivity
  - Virtex-6 SXT FPGAs: Highest signal processing capability with advanced serial connectivity
  - Virtex-6 HXT FPGAs: Highest bandwidth serial connectivity
- Compatibility across sub-families
  - LXT and SXT devices are footprint compatible in the same package

Virtex-6 series - features

- Advanced, high-performance FPGA Logic
  - Real 6-input look-up table (LUT) technology
  - Dual LUT5 (5-input LUT) option
  - LUT/dual flip-flop pair for applications requiring rich register mix
  - Improved routing efficiency
  - 64-bit (or two 32-bit) distributed LUT RAM option per 6-input LUT
  - SRL32/dual SRL16 with registered outputs option

Virtex-6 series - features

- 36-Kb block RAM/FIFOs
  - Dual-port RAM blocks
  - Programmable
    - Dual-port widths up to 36 bits
    - Simple dual-port widths up to 72 bits
  - Enhanced programmable FIFO logic
  - Built-in optional error-correction circuitry
  - Optionally use each block as two independent 18 Kb blocks

Virtex-6 series - features

- High-performance parallel SelectIO™ technology
  - 1.2 to 2.5V I/O operation
  - Source-synchronous interfacing using ChipSync™ technology
  - Digitally controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support with integrated write-leveling capability

Virtex-6 series - features

- Advanced DSP48E1 slices
  - 25 x 18, two's complement multiplier/accumulator
  - Optional pipelining
  - New optional pre-adder to assist filtering applications
  - Optional bitwise logic functionality
  - Dedicated cascade connections
- GTX transceivers: up to 6.6 Gb/s
  - Data rates below 480 Mb/s supported by oversampling in FPGA logic.
- GTH transceivers: 2.488 Gb/s to beyond 11 Gb/s

Virtex-6 series - features

- Integrated 10/100/1000 Mb/s Ethernet MAC block
  - Supports 1000BASE-X PCS/PMA and SGMII using GTX transceivers
  - Supports MII, GMII, and RGMII using SelectIO technology resources
  - 2500Mb/s support available
- 1.0V core voltage (-1, -2, -3 speed grades only)

Virtex-6 series - devices

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks			MMCMs[4]	Interface Blocks for PCI Express	Ethernet MACs[5]	Maximum Transceivers		Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb[3]	36 Kb	Max (Kb)				GTX	GTH		
XC6VLX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	4	12	0	9	360
XC6VLX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	4	20	0	15	600
XC6VLX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	4	20	0	15	600
XC6VLX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	4	24	0	18	720
XC6VLX365T	364,032	56,880	4,130	576	832	416	14,976	12	2	4	24	0	18	720
XC6VLX550T	549,888	85,920	6,200	864	1,264	632	22,752	18	2	4	36	0	30	1200
XC6VLX760	758,784	118,560	8,280	864	1,440	720	25,920	18	0	0	0	0	30	1200
XC6VSX315T	314,880	49,200	5,090	1,344	1,408	704	25,344	12	2	4	24	0	18	720
XC6VSX475T	476,160	74,400	7,640	2,016	2,128	1,064	38,304	18	2	4	36	0	21	840
XC6VHX250T	251,904	39,360	3,040	576	1,008	504	18,144	12	4	4	48	0	8	320
XC6VHX255T	253,440	39,600	3,050	576	1,032	516	18,576	12	2	2	24	24	12	480
XC6VHX380T	382,464	59,760	4,570	864	1,536	768	27,648	18	4	4	48	24	18	720
XC6VHX565T	566,784	88,560	6,370	864	1,824	912	32,832	18	4	4	48	24	18	720

New breed of FPGAs

New Xilinx FPGA devices

Features	Artix-7	Kintex-7	Virtex-7	Spartan-6	Virtex-6
Logic Cells	352,000	480,000	2,000,000	150,000	760,000
BlockRAM	19Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	1,040	1,920	3,600	180	2,016
DSP Performance (symmetric FIR)	1,248GMACS	2,845GMACS	5,335GMACS	140GMACS	2,419GMACS
Transceiver Count	16	32	96	8	72
Transceiver Speed	6.6Gb/s	12.5Gb/s	28.05Gb/s	3.2Gb/s	11.18Gb/s
Total Transceiver Bandwidth (full duplex)	211Gb/s	800Gb/s	2,784Gb/s	50Gb/s	536Gb/s
Memory Interface (DDR3)	1,066Mb/s	1,866Mb/s	1,866Mb/s	800Mb/s	1,066Mb/s
PCI Express® Interface	Gen2x4	Gen2x8	Gen3x8	Gen1x1	Gen2x8
Agile Mixed Signal (AMS)/XADC	Yes	Yes	Yes		Yes
Configuration AES	Yes	Yes	Yes	Yes	Yes
I/O Pins	600	500	1,200	576	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V
EasyPath Cost Reduction Solution	-	-	Yes	-	Yes

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Artix-7

Kintex-7

Vitrex-7

Artix-7 series - features

- Low power and low cost family for high volume applications
- 28nm architecture:
  - Higher capacity
  - Higher performance
  - Lower power consumption
- Agile Mixed Signal technology
- Unified architecture with Kintex-7 and Virtex-7

Artix-7 series - features

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			Clock Mgmt Tiles (CMTs)[4]	PCIe[5]	GTPs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18Kb	36Kb	Max (Kb)						
XC7A8	8,000	1,250	100	20	40	20	720	2	0	0	1	4	200
XC7A15	15,360	2,400	200	40	80	40	1,440	2	0	0	1	4	200
XC7A30T	33,600	5,250	400	80	104	52	1,872	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500
XC7A350T	360,000	56,250	4,638	1,040	1,030	515	18,540	12	1	16	1	12	600

Kintex-7 series - features

- High-performance for cost-sensitive applications
- 2x better price-performance than previous generation high-performance FPGAs
- 50% lower power consumption than previous generation high-performance FPGAs

Kintex-7 series - features

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTXs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	7	1	28	1	7	350
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Virtex-7 series - features

- Highest Bandwidth and System Performance
- 2x higher system performance than Virtex®-6 FPGAs
- Industry's only single-FPGA solution for 400G applications
- Industry's only 2 million logic-cell FPGA

Virtex-7 series - features

Device[1]	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[3]	Block RAM Blocks[4]			CMTs[5]	PCIe[6]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[7]	Max User I/O[8]	SLRs[9]
		Slices[2]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7V585T	582,720	91,050	6,938	1,260	1,590	795	28,620	18	3	36	0	0	1	17	850	N/A
XC7V1500T	1,465,920	229,050	16,163	1,620	1,938	969	34,884	18	3	36	0	0	1	17	850	3
XC7V2000T	1,954,560	305,400	21,550	2,160	2,584	1,292	46,512	24	4	36	0	0	1	24	1,200	4
XC7VX330T	326,400	51,000	4,388	1,120	1,500	750	27,000	14	2	0	28	0	1	14	700	N/A
XC7VX415T	412,160	64,400	6,525	2,160	1,760	880	31,680	12	2	0	48	0	1	12	600	N/A
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A
XC7VX550T	554,240	86,600	8,725	2,880	2,360	1,180	42,480	16	2	0	64	0	1	16	600	N/A
XC7VX690T	693,120	108,300	10,888	3,600	2,940	1,470	52,920	20	3	0	80	0	1	20	1,000	N/A
XC7VX980T	979,200	153,000	13,838	3,600	3,000	1,500	54,000	18	3	0	72	0	1	18	880	N/A
XC7VX1140T	1,139,200	178,000	17,700	3,360	3,760	1,880	67,680	24	4	0	96	0	1	22	1,100	4
XC7VH290T	284,000	44,375	4,425	840	940	470	16,920	6	1	0	24	8	1	6	300	1
XC7VH580T	580,480	90,700	8,850	1,680	1,880	940	33,840	12	2	0	48	8	1	12	600	2
XC7VH870T	876,160	136,900	13,275	2,520	2,820	1,410	50,760	18	3	0	72	16	1	13	650	3

Artix,Kintex,Virtex-7 series - features

Maximum Capability	Artix-7 Family	Kintex-7 Family	Virtex-7 Family
Logic Cells	360K	478K	1,955K
Block RAM(1)	19 Mb	34 Mb	68 Mb
DSP Slices	1,040	1,920	3,600
Peak DSP Performance(2)	1,248 GMACS	2,845 GMACS	5,335 GMACS
Transceivers	16	32	96
Peak Transceiver Speed	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Peak Serial Bandwidth (Full Duplex)	211 Gb/s	800 Gb/s	2,784 Gb/s
PCIe Interface	x4 Gen2	x8 Gen2	x8 Gen3
Memory Interface	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	600	500	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Package Options	Low-Cost, Wire-Bond, Lidless Flip-Chip	Low-Cost, Lidless Flip-Chip and High-Performance Flip-Chip	Highest Performance Flip-Chip

DSP slice - features

- 25 × 18 two's complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features:
  - optional pipelining,
  - optional ALU,
  - dedicated buses for cascading

DSP slice - operation

- Each DSP slice can operate up to 638 MHz
- The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single instruction-multiple-data (SIMD) arithmetic unit:
  - dual 24-bit add/subtract/accumulate
  - quad 12-bit add/subtract/accumulate

Low-Power Gigabit Transceivers- features

- High-performance transceivers capable of up to 6.6 Gb/s (GTP), 12.5 Gb/s (GTX), 13.1 Gb/s (GTH), or 28.05 Gb/s(GTZ) line rates depending on the family
- Low-power mode optimized for chip-to-chip interfaces
- Advanced Transmit pre and post emphasis, and receiver linear (CTLE) and decision feedback equalization (DFE), including adaptive equalization for additional margin.

PCIe features

- Compliant to the PCI Express Base Specification 2.1 or 3.0 (depending of family) with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s), Gen2 (5 Gb/s), and Gen3 (8 Gb/s) depending on device family
- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC (ECRC) Advanced Error Reporting and ECRC features

XADC features

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

Extensible Processing Platforms

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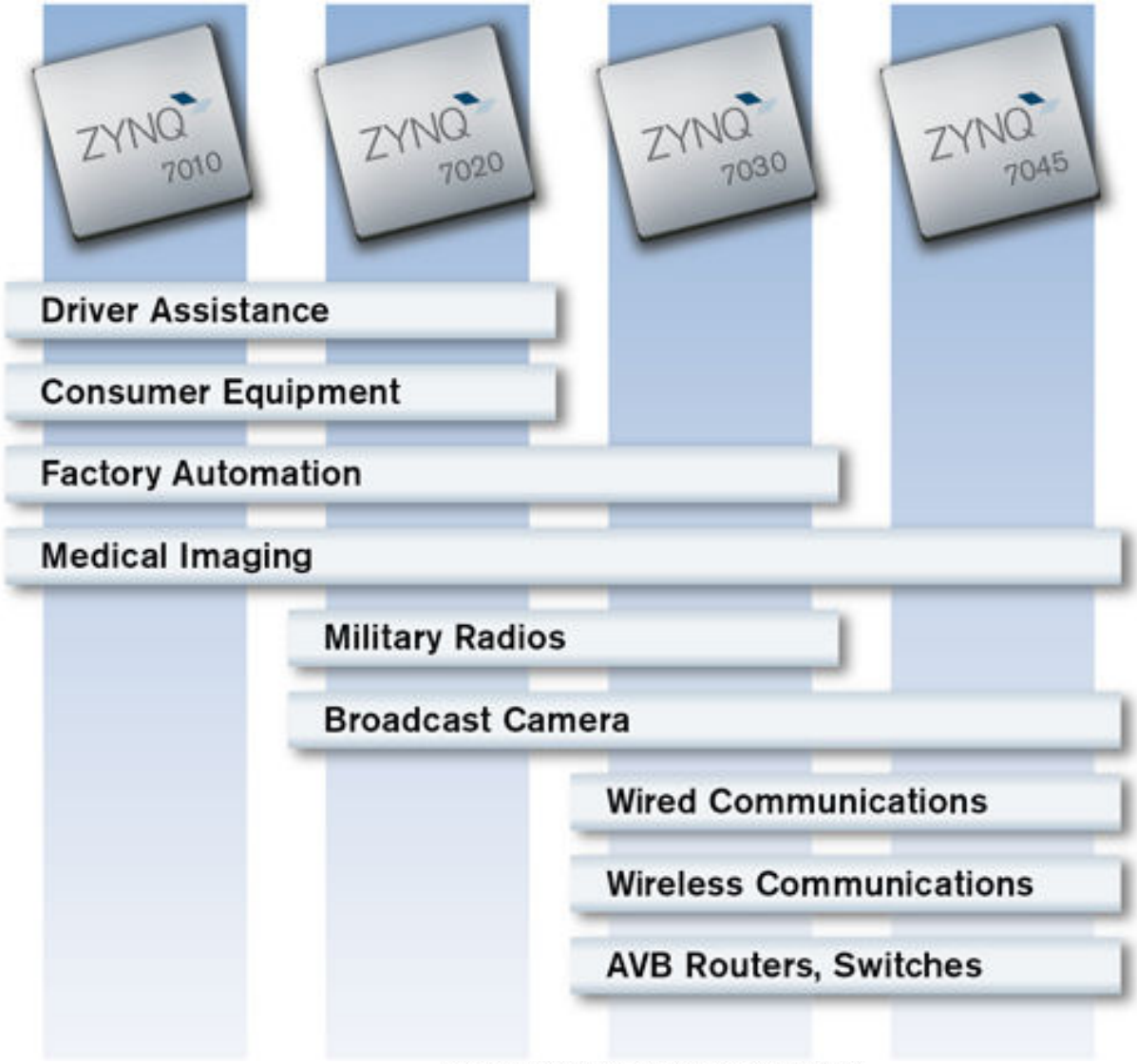
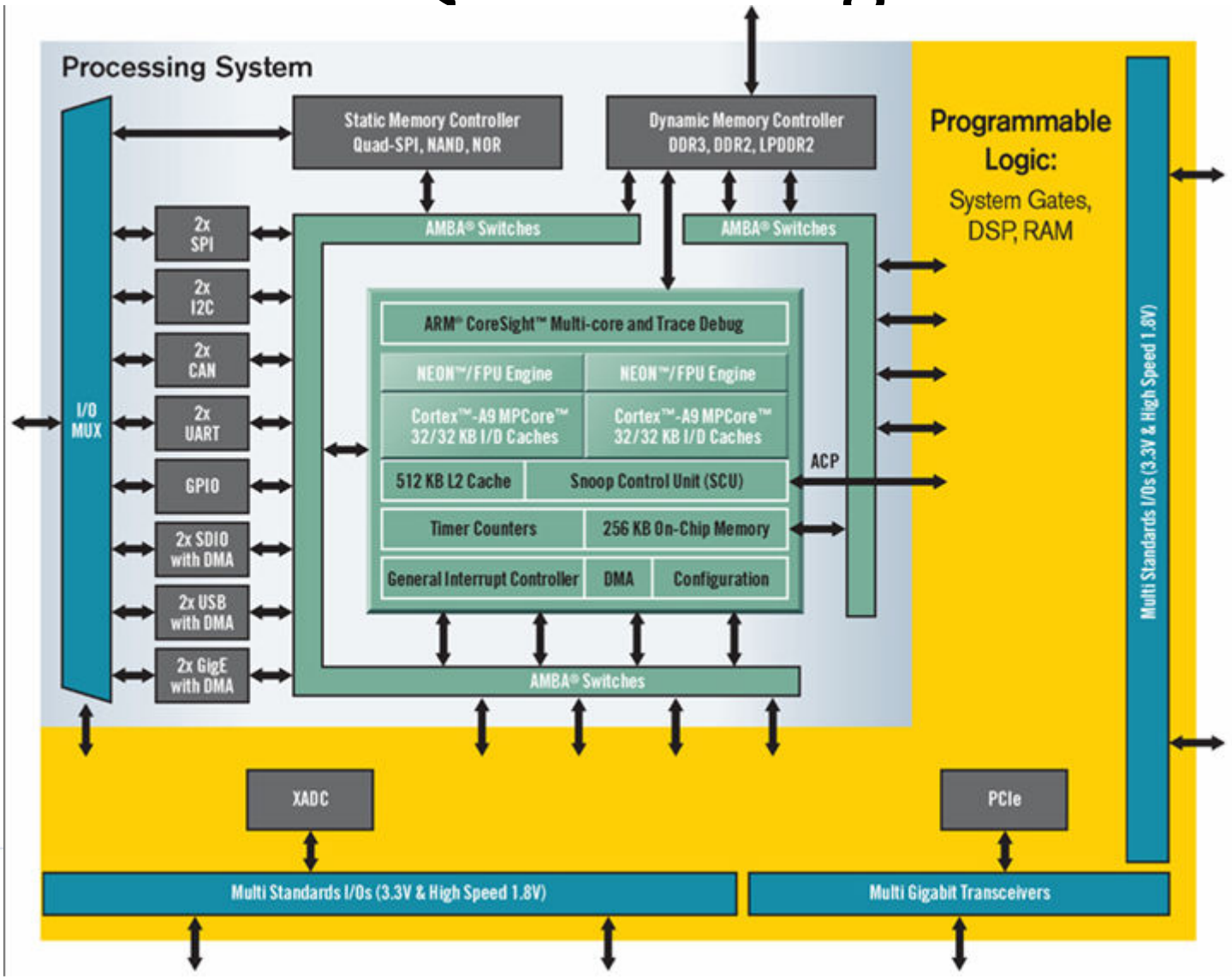
EPP features (ZYNQ-7000)

- A new class of product
- Combines an industry-standard ARM® dual-core Cortex™-A9 MPCore™ processing system with Xilinx 28nm programmable logic unified architecture
- This processor-centric architecture offers the flexibility and scalability of an FPGA combined with ASIC-like performance and power and the ease of use of an ASSP

ZYNQ-7000 - applications



ZYNQ block diagram



ZYNQ features

- Dual ARM Cortex™-A9 MPCore
  - Up to 800MHz
  - Enhanced with NEON Extension and Single & Double Precision Floating point unit
  - 32kB Instruction & 32kB Data L1 Cache
- Unified 512kB L2 Cache
- 256kB on-chip Memory
- DDR3, DDR2 and LPDDR2 Dynamic Memory Controller

ZYNQ features

- 2x QSPI, NAND Flash and NOR Flash Memory Controller
- 2x USB2.0 (OTG), 2x GbE, 2x CAN2,0B 2x SD/SDIO, 2x UART, 2x SPI, 2x I2C, 4x 32b GPIO
- AES & SHA 256b encryption engine for secure boot and secure configuration
- Dual 12bit 1Msps Analog-to-Digital converter
- Up to 17 Differential Inputs

ZYNQ features

- Advanced Low Power 28nm Programmable Logic:
  - 28k to 350k Logic Cells (approximately 430k to 5.2M of equivalent ASIC Gates)
  - 240KB to 2180KB of Extensible Block RAM
  - 80 to 900 18x25 DSP Slices (58 to 1080 GMACS peak DSP performance)
- PCI Express® Gen2x8 (in largest devices)
- 154 to 404 User IOs (Multiplexed + SelectIO™)
- 4 to 16 12.5Gbps Transceivers (in largest devices)

ZYNQ features

		Zynq-7000 Product Table (Software View)			
	Device Name	Z-7010	Z-7020	Z-7030	Z-7045
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
	Processor Extensions	NEON™ and Single/Double Precision Floating Point			
	Maximum Frequency	800 MHz			
	L1 Cache	32 KB Instruction, 32 KB Data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	External Memory Support	DDR3, DDR2, LPDDR2			
	External Static Memory Support	2x QSPI-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART (2), 2x CAN2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Security	AES and SHA 256b for secure boot			
	Peripherals and Static Memory Multiplexed I/O(1)	54			
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix™-7 FPGA	Kintex™-7 FPGA	Kintex™-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates(3))	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	2,180KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	1080 GMACS
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs			
	Security	AES and SHA 256b for secure configuration			
	Multi-Standards 3.3V I/O(2)	100	200	250	350
	Serial Transceivers(2)	—	—	4	16

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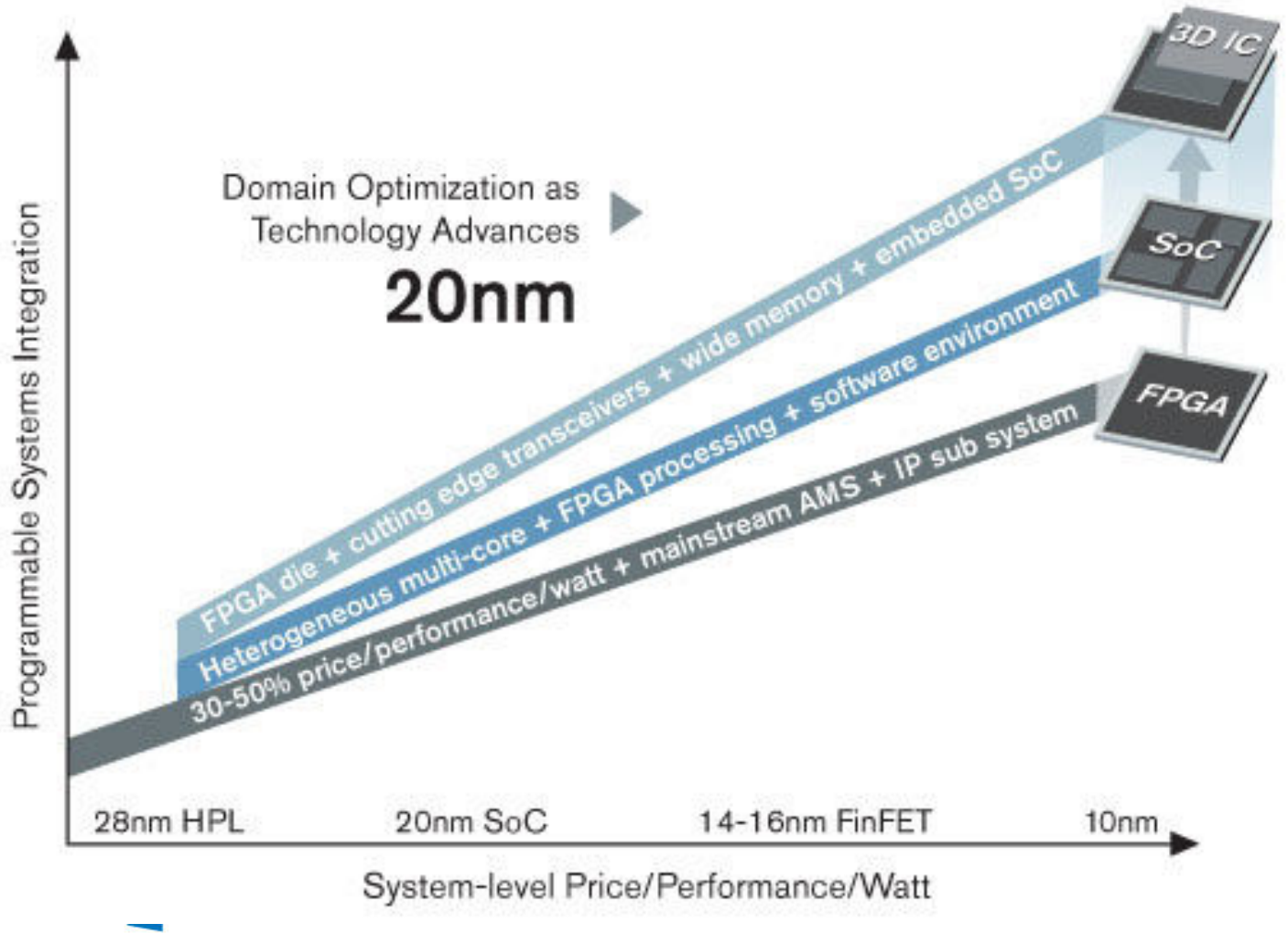
Future

Future



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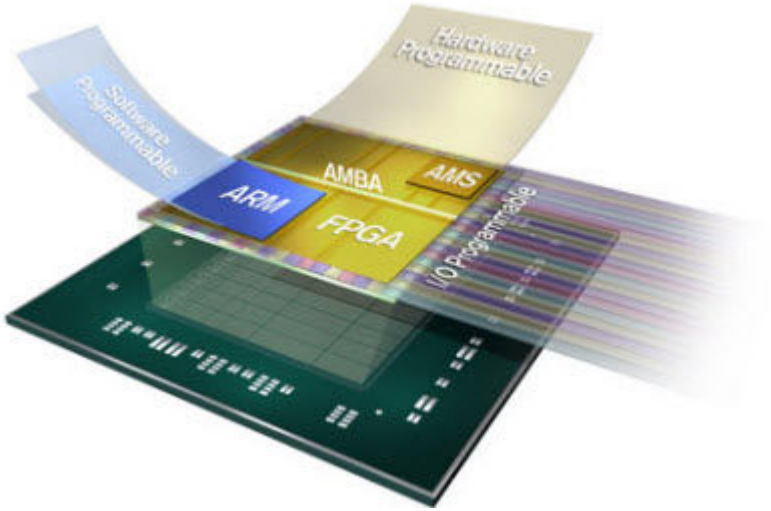
Future

- Xilinx is following development in three main areas:
  - All Programmable 20nm FPGA:
    - Price-performance-per-watt improvement up to 50%
    - Memory bandwidth x 2 times
    - Better (faster) transceivers

Future

– 2nd Generation All Programmable SoC:

- Multi-core heterogeneous processing architecture

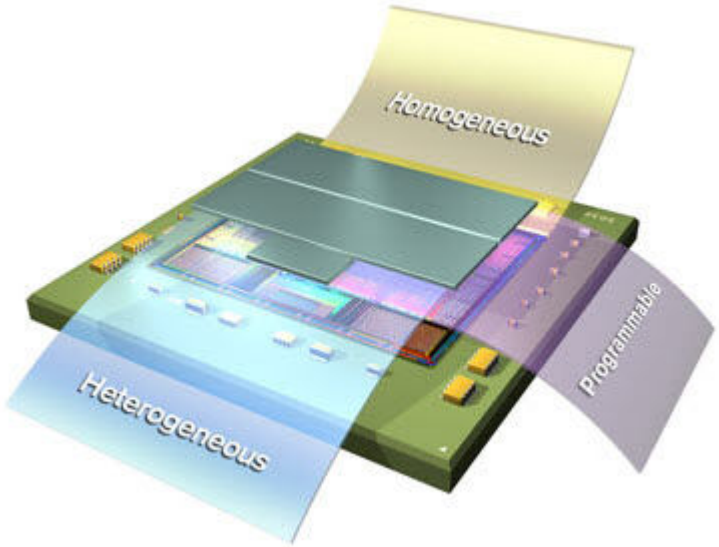


- Thanks to increased bandwidth between the processing system and the programmable logic, the new architecture delivers higher levels of programmable systems integration and performance at a fraction of the power consumption

Future

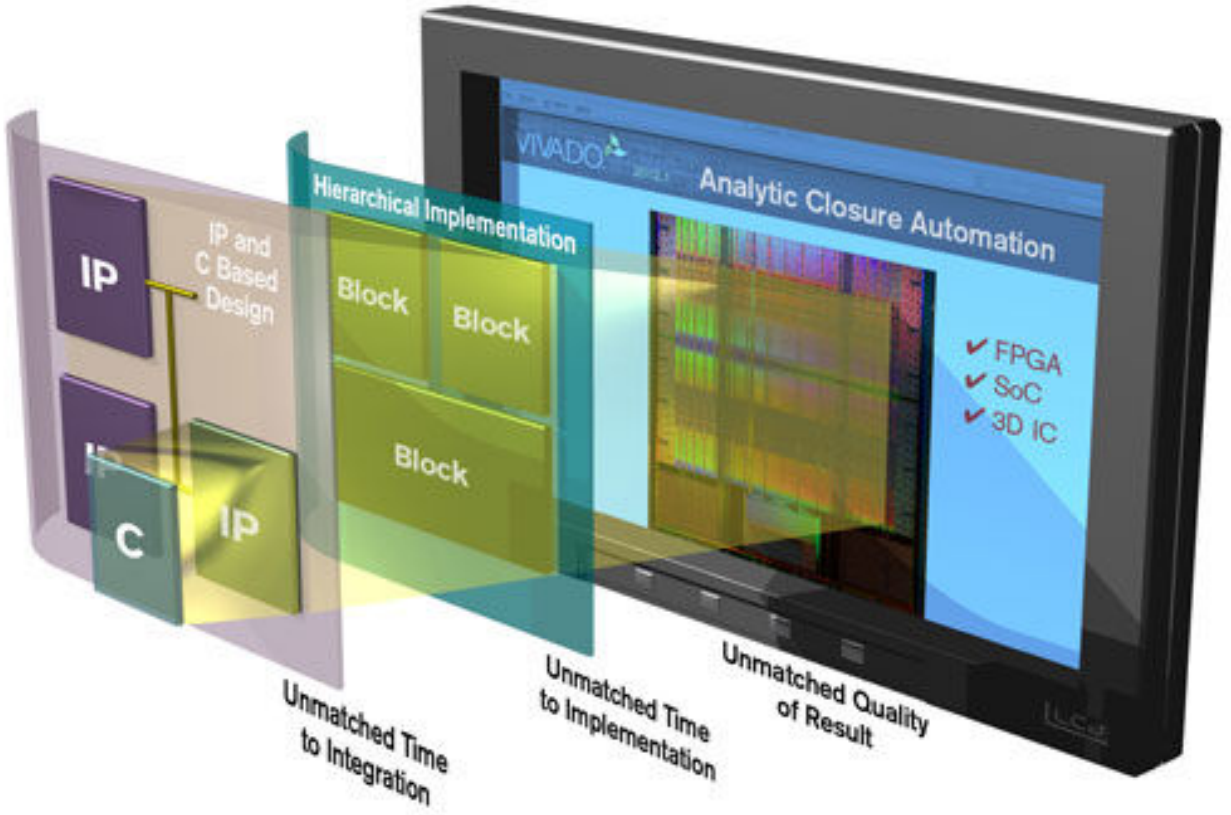
– 2nd Generation All Programmable 3D IC:

- Combination of multiple dies of different types



Future

- Together with the new hardware the Next Generation Design Suite will be available.



Future

- The modified Vivado suite will:
  - deliver significant quality of results, routability, utilization, and productivity advantages
  - productivity for the front end design process will be multiplied by more than 4X with high level synthesis and IP integration tools
  - productivity in design implementation will improve by more than 4X due to faster hierarchical planning and analytic place and route engines

Thank you for your attention

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EUROPEAN SOCIAL FUND
Project co-financed from the EU European Social Fund

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[2] EasyPath-6 family documentation; www.xilinx.com

[3] 7-th series documentation; www.xilinx.com