Prospect for the memory Packaging technology

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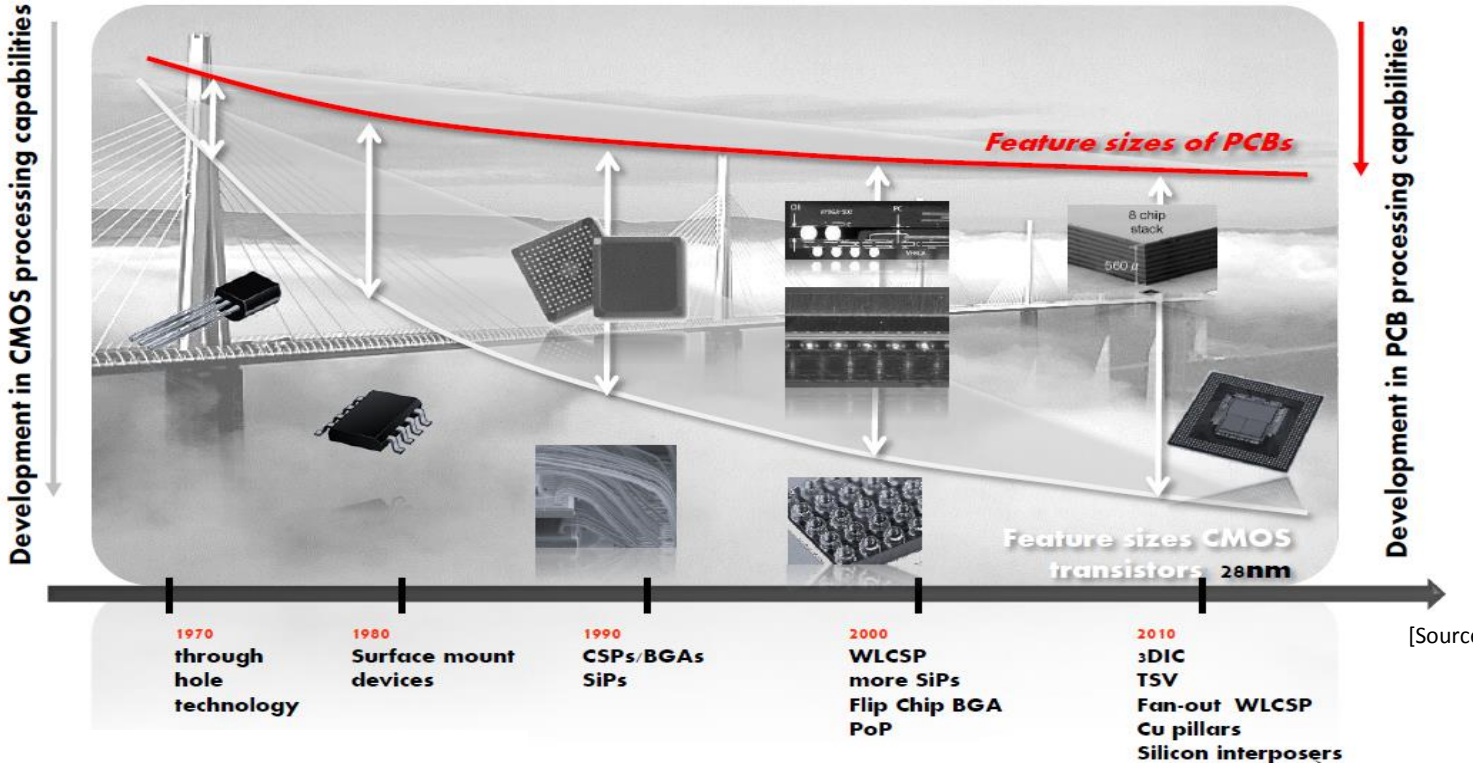
Agenda

1. Electronic Packaging Trend
2. Memory Packaging Roadmap
3. Innovative Packaging Technology
   - Package
   - Process
   - Material
4. Conclusion

Electronic Packaging Development Trend

Packaging technology is developing to compensate the technology gap between Si and PCB tech.



[Source] Yole Development

◯ **Bridging the gap between Si and PCB process capabilities**

- High I/O & speed : PGA → FBGA → Flip Chip → WLP/TSV

◯ **Improvement by the high functionality of IT application**

- High Density & Functionality, High thermal dissipation.

Memory Packaging Roadmap

Flip chip and TSV/WLCSP are promising technologies to satisfy faster speed, wider bandwidth and smaller/thinner package

	Past	*Present*	*Near Future*
Device Market	PC/Notebook	Smart Phone/Tablet PC /Smart Device	IoT (Wearable Device, Smart Car, Smart Home and so on) / Cloud(Big Data)
Memory Package	***DRAM***		
	BOC, TSOP, RDL DDP/QDP, Flip Chip, TSV, 2.5D SiP***, 3D SiP, Optical Interconnection		High Performance & Density
	PoP, eMCP, FOWLP**, Flexible Package		Thin Profile
	NAND Flash		
	eMMC (with Controller), UFS, SSD, EMI* Shield, BGA SSD, NAND TSV		High Performance & Density

*EMI: Electro Magnetic Interference
**FOWLP: Fan-out Wafer Level Package
***SiP: System in Package

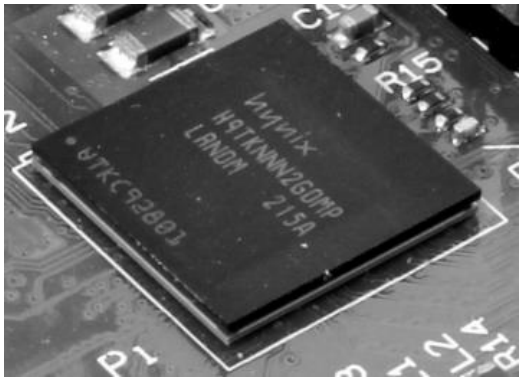
Innovative Packaging Technology - Package

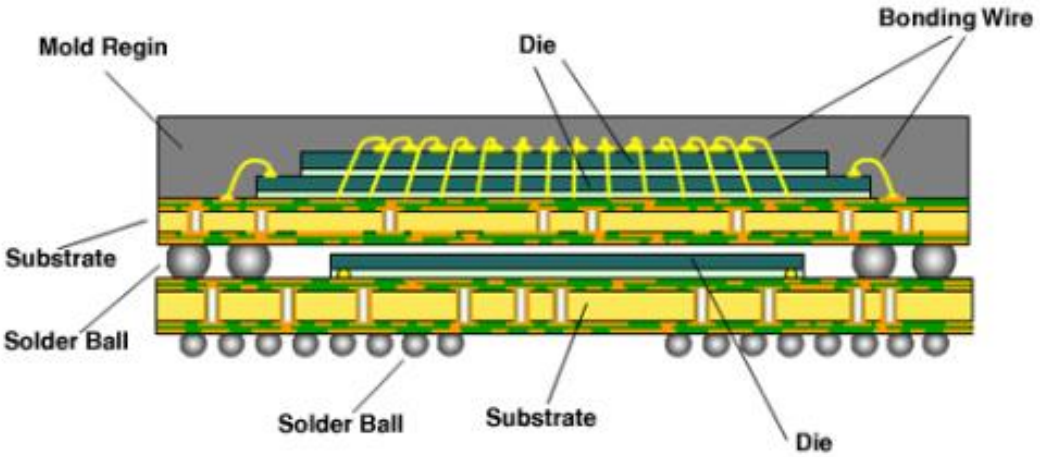
① Package Stack

AP & Memory package stack is widely being used.

PoP (Package on Package)

- Mobile Application: AP + Memory
- Top/Bottom PKG Warpage Control





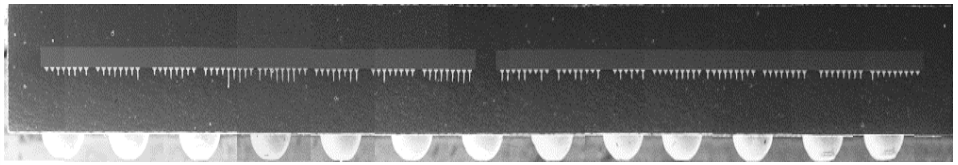
Innovative Packaging Technology - Package

② Chip Stack (Planar)

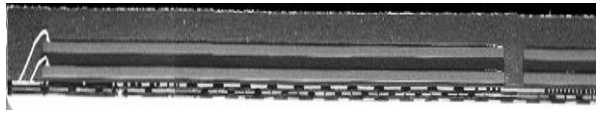
Planar chip stack is driven by low cost and high density requirement
2.5D SiP is a suitable solution to place memory dies near SoC

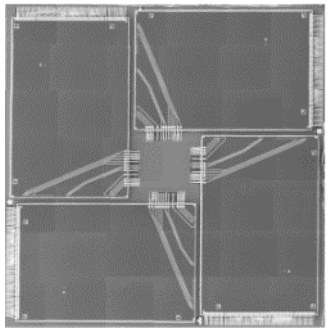
Planar Stack Package

- BOC/Flip chip planar DDP(Dual Die Package)



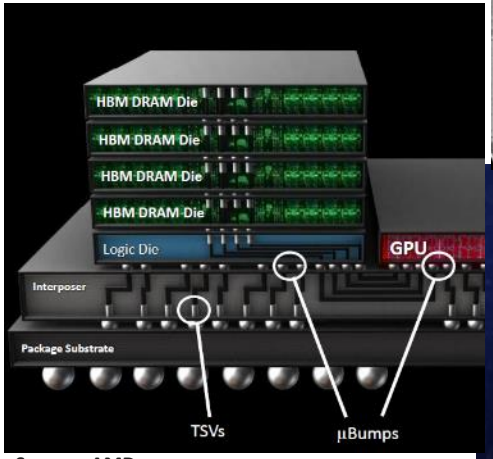
- Pinwheel package
  - Thin Profile
  - Improve Signal Integrity



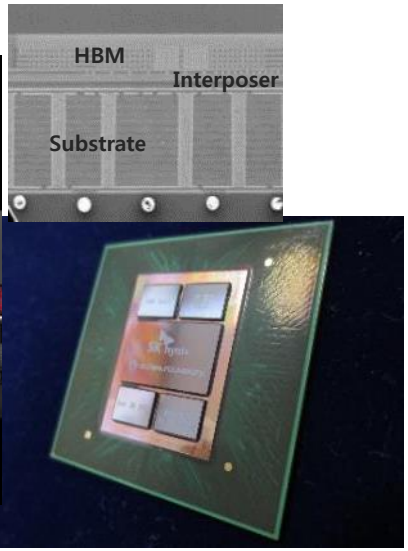


2.5D SiP

- SoC + 2/4/8 HBMs(High Bandwidth Memory) on interposer
- Various structures : CoCoS, CoWoS (TSMC), EMIB (Intel)



Source : AMD



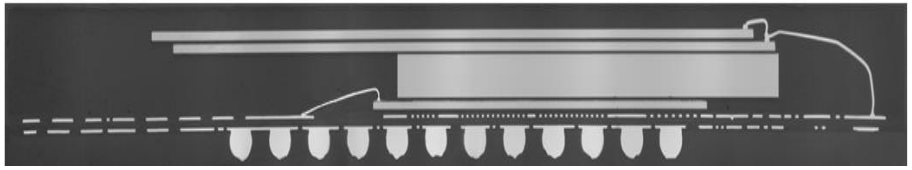
Innovative Packaging Technology - Package

② Chip Stack (Vertical)

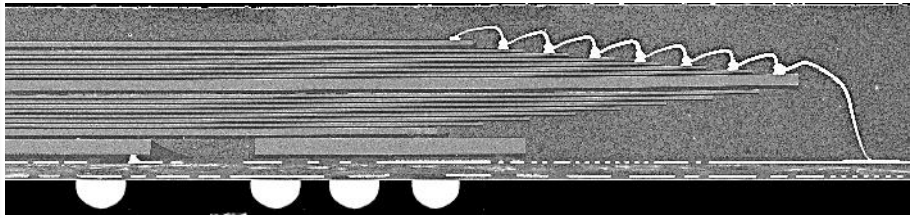
Conventional chip stack using wiring and TSV chip stack are implemented

Wire Interconnection

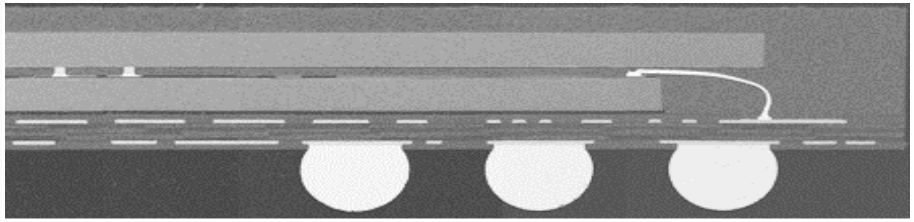
- MCP (Multi Chip Package)



- UFS (Universal Flash Storage)

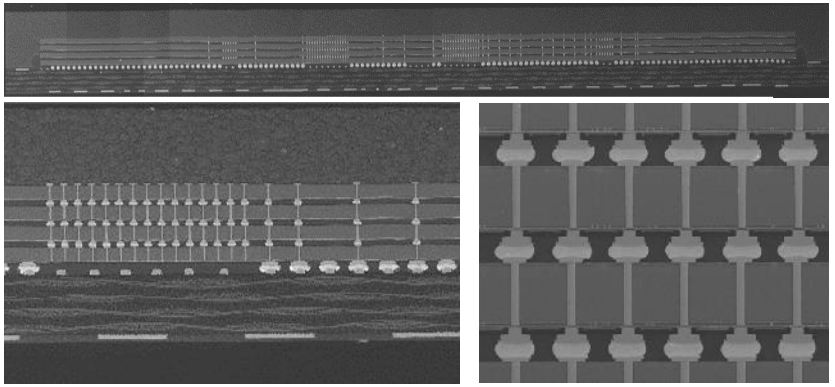


- CoC (Chip on Chip)

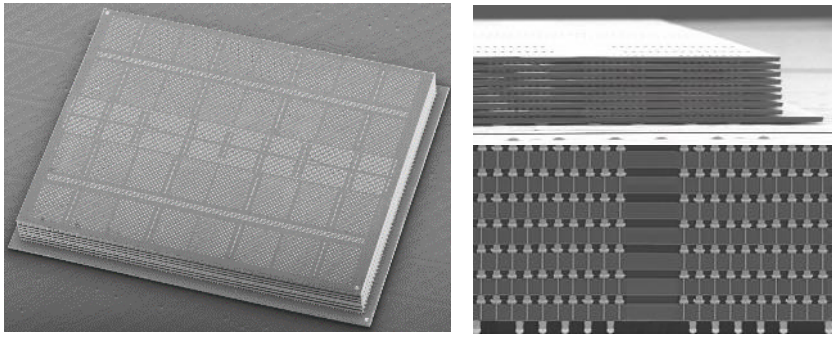


TSV Interconnection

- 3DS



- HBM (High Bandwidth Memory)

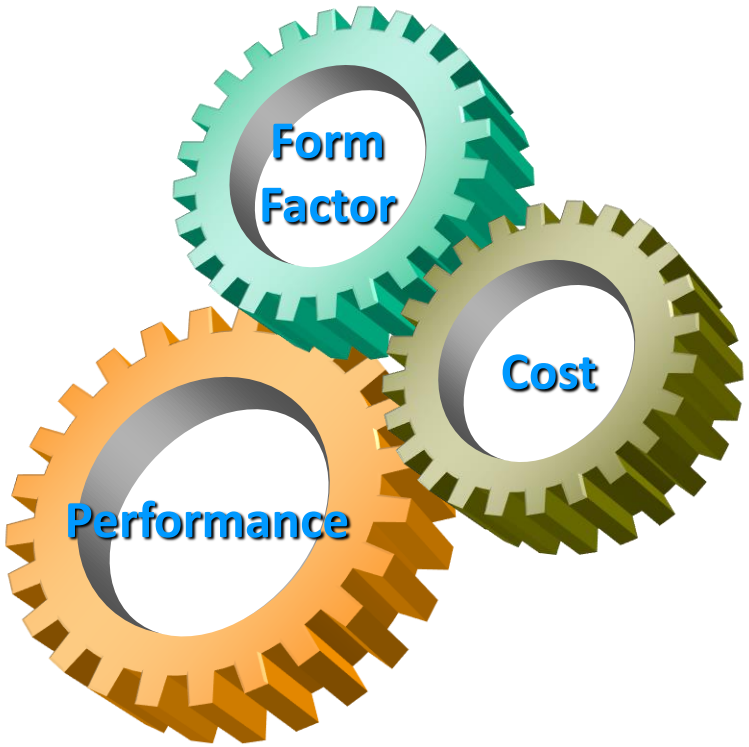


Innovative Packaging Technology - Package

③ Fan out package

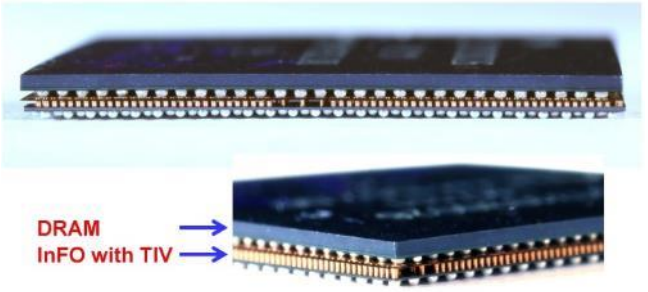
FOWLP is a promising solution, but cost reduction is needed.

Market Driver for Fan-out



Fan-out Packaging for SiP

- PoP Bottom Package with Logic (Mobile AP)
  - TSMC InFO[1]
  - Amkor SLIM[2] & SWIFT[3]
  - SPIL SLIT[4]



*Source: http://gigglehd.com/zbxe/14078384

[1]InFO (Integrated Fan Out Wafer Level PKG), [2]SLIM (siliconless integrated module), [3]SWIFT (Silicon Wafer Integrated Fan-out Tech.), [4]SLIT (Silicon-less Interconnect Tech.)

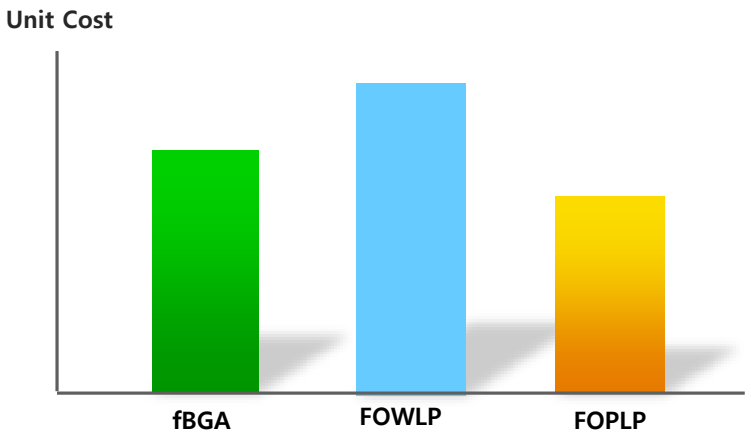
Innovative Packaging Technology - Package

③ Fan out package

FOWLP is a promising solution, but cost reduction is needed.

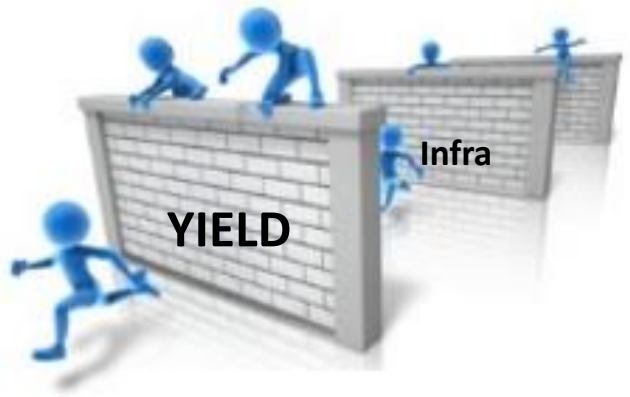
Cost Reduction Challenges for FOWLP

- High Packaging Cost
- Cost Reduction by Panel Level Packaging



Hurdle of FOPLP

- Yield
  - Warpage Control
  - Die Bonding Accuracy
  - Panel Handling
- Infra Investment



Conclusion

SK hynix is leading new and advanced memory package development against diverse and rapidly changing circumstances of semiconductor industry

Thanks for Your Time