First International Computer,Inc

Protable Computer Group HW Department

Board name : Mother Board Schematic

Project :

Version :

Initial Date :

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1. Schematic Page Description :

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7. DDR Layout Guideline
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9. Yonah processor (2/2)
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11. Clock Generator
12. Clock Buffer
13. VN896 Host (1 OF 4)
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15. VN896 Video (3 OF 4)
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20. LCD Connector
21. CRT Connector
22. TV-Out VT1623M
23. VT8237A PCI/USB (1/3)
24. VT8237A IDE/AC-LINK (2/3)
25. VT8237A V-LINK/MII/LPC (3/3)
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29. USB CNN
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38. Azalia VT1708A Codec
39. AMP MAXIM9789AETJ
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42. Screw Hole
43. EC_PMX
44. Power Block
45. POWER (CPU CORE)
46. ACIN, BATIN and ADPOUT1
47. Charger
48. DCIN
49. 5VDDA/S/M, 3VDDA/S/M
50. 1.05VDDM/1.5VDDM
51. 2.5VDDA/M, 1.5VA/1.8VM
52. DDR 1.8VDDS/0.9VDDM
53. Daughter Board
54. (U) USB Board
55. (F) Finger Printer Board

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)
AD23	CardBus

PCIINT	CHIP
IRQA	MiniPCI/NB
IRQB	MiniPCI/CardBus
IRQC	MiniPCI
IRQD	

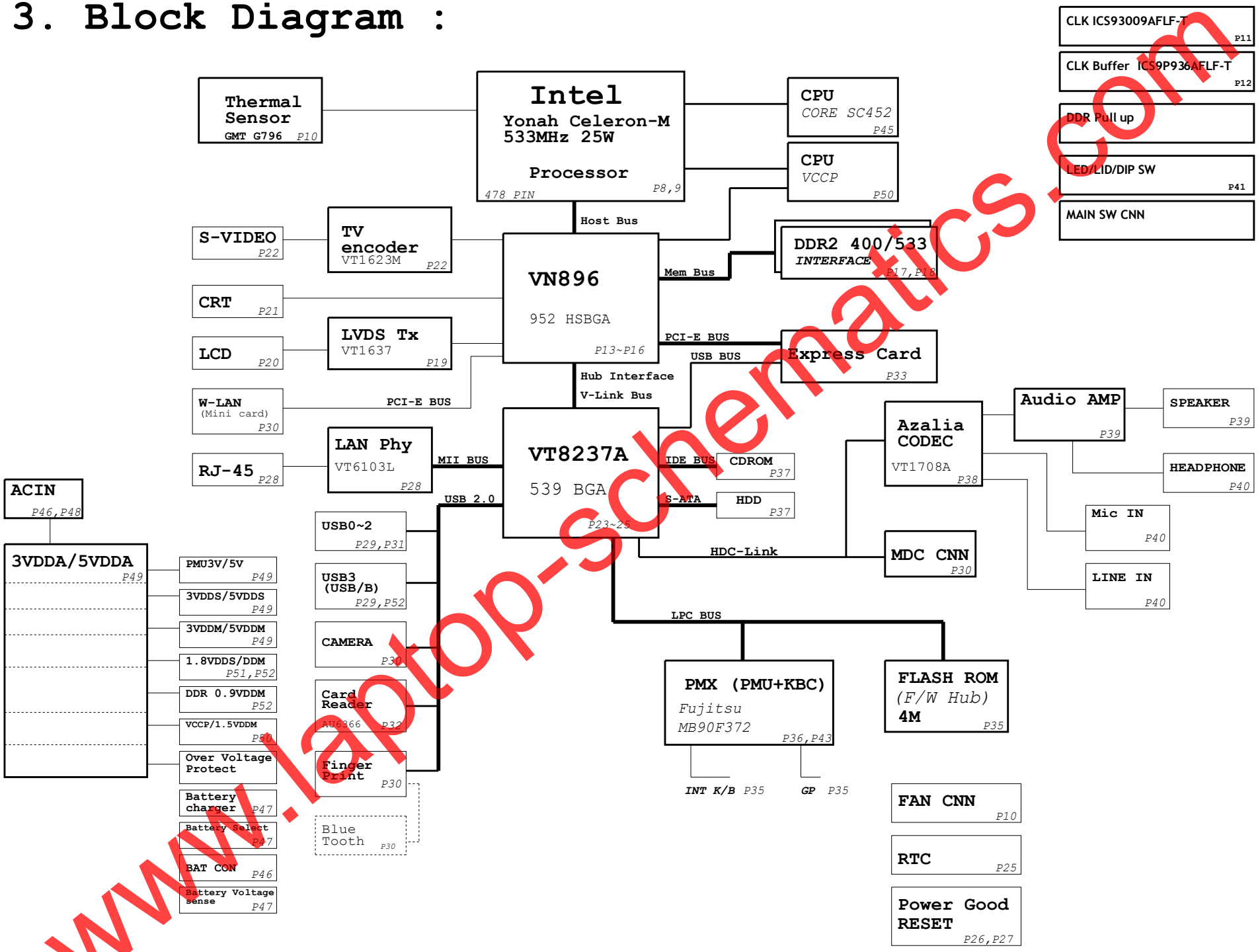
BUSMASTER

REQ	CHIP
REQ0 / GNT0	MiniPCI
REQ1 / GNT1	CardBus
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Desciption	
IRQ0	System timer	
IRQ1	Keyboard	
IRQ2	(Casacde)	
IRQ3	LAN / MODEM	
IRQ4	~~Serial Port~~	
IRQ5	AUDIO / VGA / USB	
IRQ6	~~FLOPPY DISK~~	
IRQ7	~~LPT~~	
IRQ8	RTC	
IRQ9	ACPI	
IRQ10	FIR (Disable by default)	(MODEM/LAN)
IRQ11	Cardbus	
IRQ12	~~PS/2 mouse~~	
IRQ13	FPU	
IRQ14	HDD	
IRQ15	CDROM	

DMA Channel	Device	
DMA0	FIR (disable by default)	(MODEM / LAN)
DMA1	~~ECP~~	
DMA2	~~FLOPPY DISK~~	
DMA3	AUDIO	
DMA4	(Cascade)	
DMA5	Unused	
DMA6	Unused	
DMA7	Unused	

3. Block Diagram :



4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR_0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

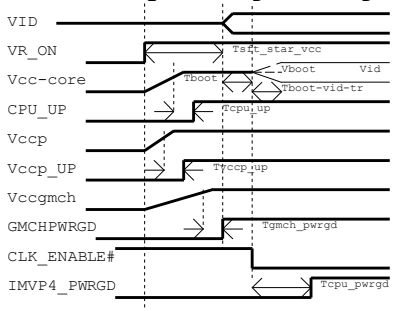
5.Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Stripline Layer
Layer 4		Stripline Layer
Layer 5		Ground Plane
Layer 6		Component Side,Microstrip signal Layer

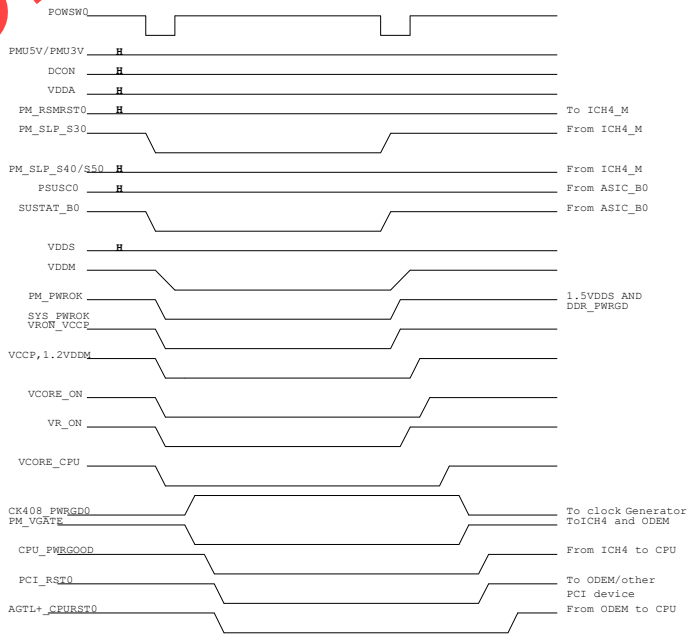
7. power on & off & S3 Sequence :

Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING

S3 SUSPEND AND RESUME TIMING



8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

DDR Signal Groups

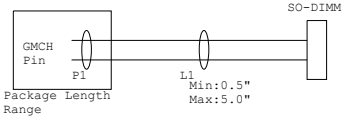
Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS#[3:0]
Command	SMA[12:6,3:0] SBA[1:0] SRAS# SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

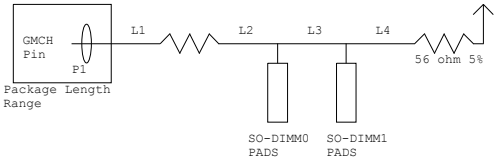
CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between + & -)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH	4.5" ~ 9.0 "	5 / 20 mils	* 66MCLK_ICH (AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
AGPCLK_ATI	MAX : 8.5"		
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2.Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5"~9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" ~ 12.5"	5 / 20 mils	

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerehve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

Data Signals Topologies and Routing Guidelines

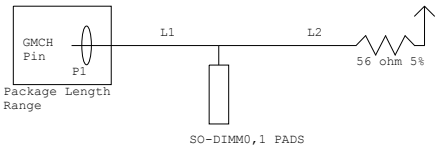


Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5", Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0 "
Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 0.5"
SDQ/SDM to SDQS : +/- 25 mils

SDQ/SDM to SDQS Mapping

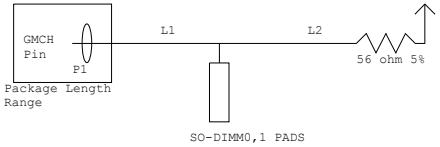
Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

Control Signals Topologies and Routing Guidelines



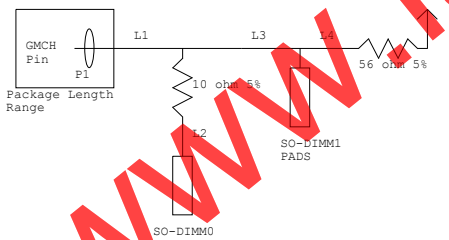
Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

CPC Signals Topologies and Routing Guidelines

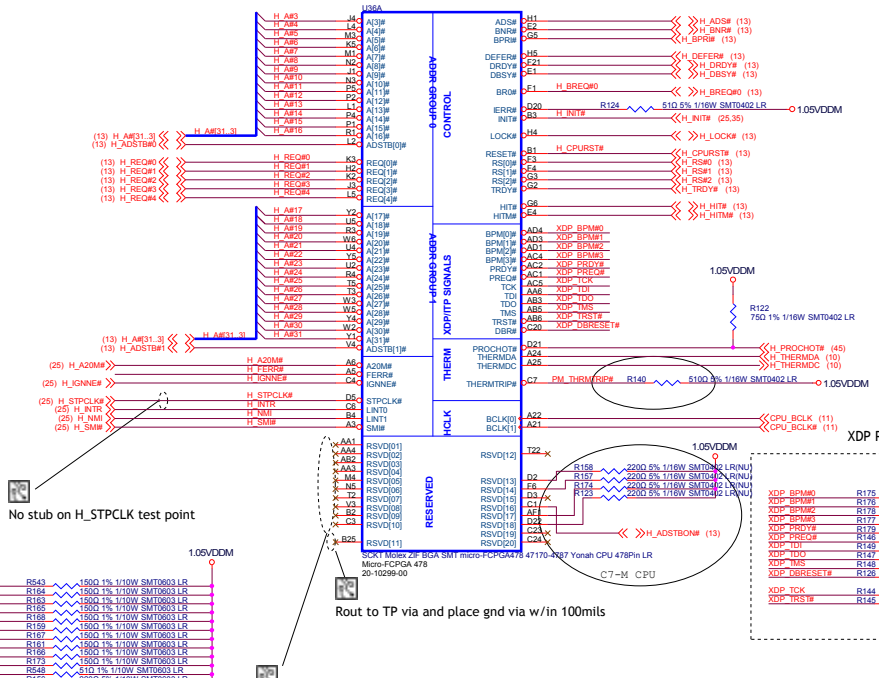


Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

Command Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.0"
L3 : Max 2.0"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"



Topology : FERR#

CPU	ICH7m	VCCP	Rtt
L1	L2		

L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line

Topology : PWRGOOD

CPU	ICH7m
L1	

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#

CPU	GMCH
L1	

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# SMI# , STPCLK#

CPU	ICH7m
L1	

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#

GMCH	CPU
L1	

L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#

GMCH	CPU	ICH7m	VCCP
L2	L1	L3	Rtt

L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

Topology : FERR#

CPU	ICH7m	VCCP	Rtt
L1	L2		

L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line

Topology : IGNNE# , SMI# , STPCLK#

VCCP	CPU	IMVP6	VCCP
Rtt			Rtt
L4	L2+L1		L3

L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Strip-line

Lenght must be Matching :
H_ADSTBON# ,
H_ADSTB#0,H_ADSTB#1

FSB Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# ,HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

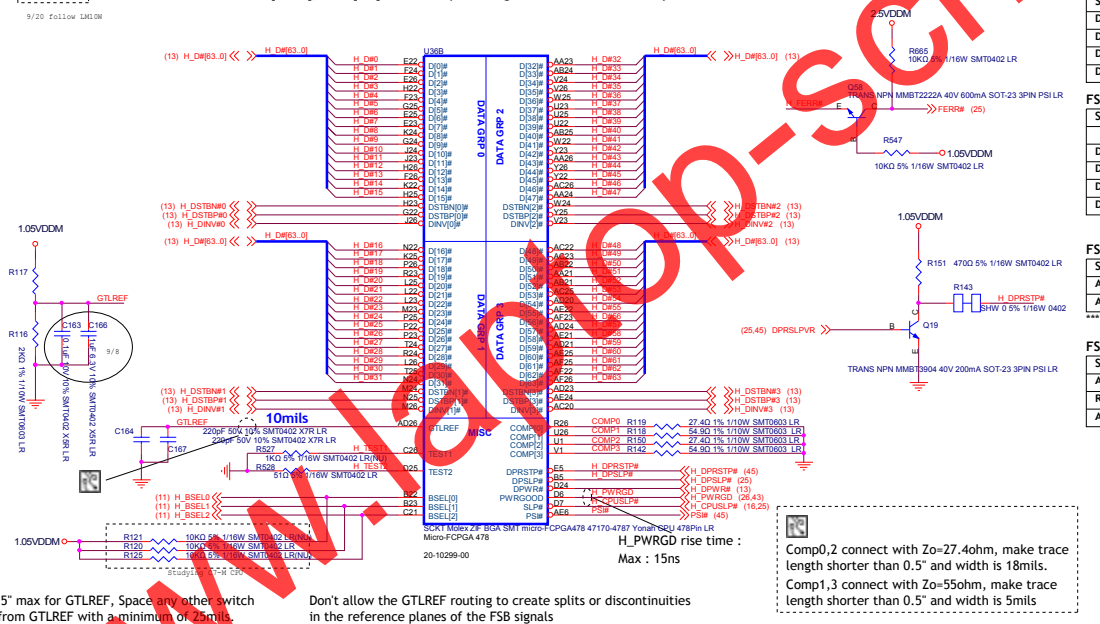
FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

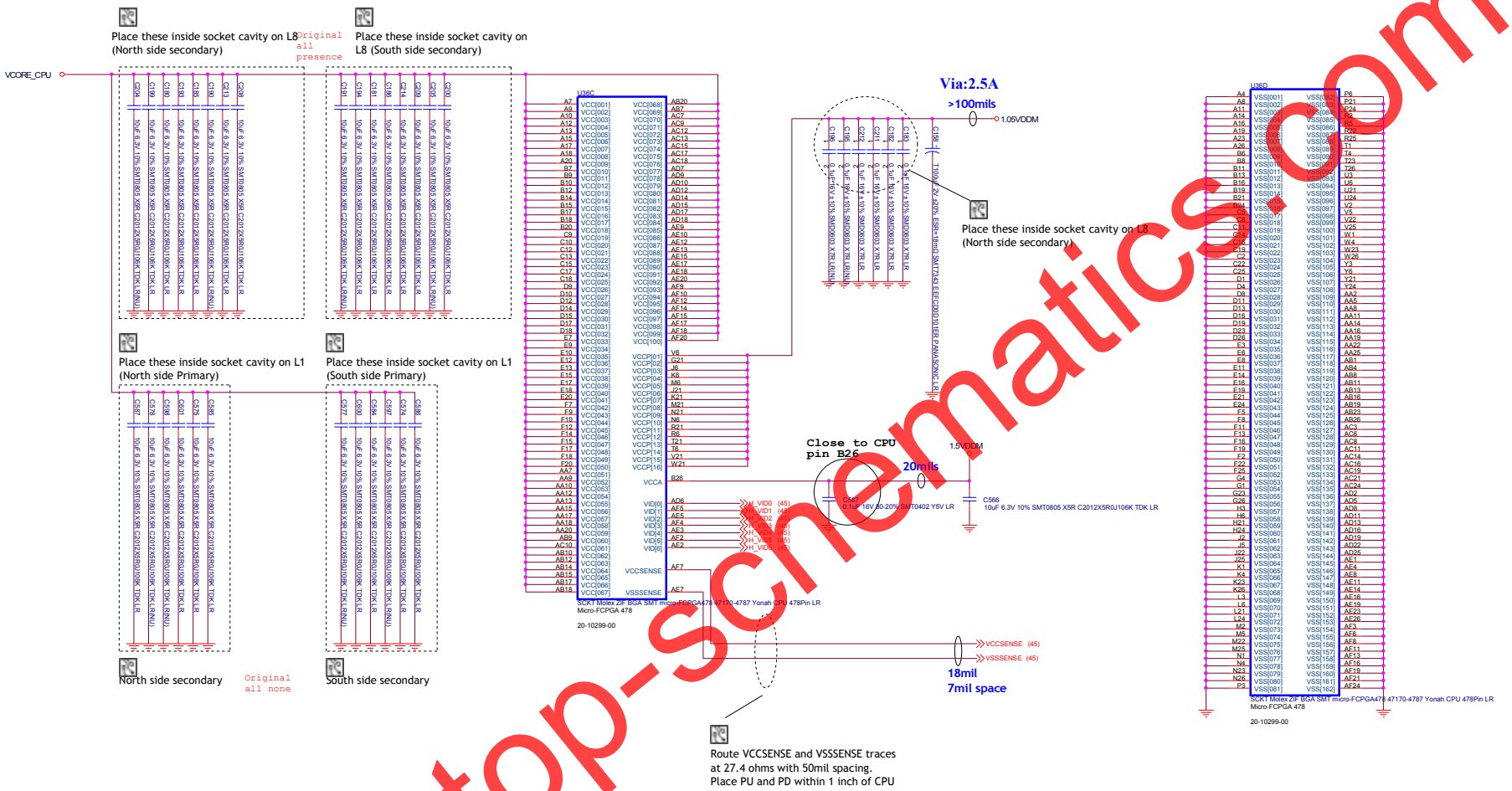
Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

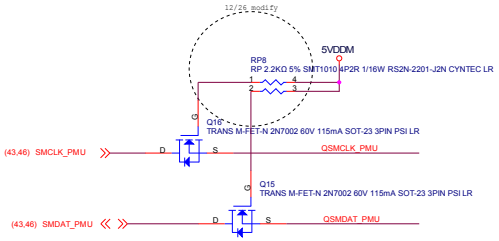
*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

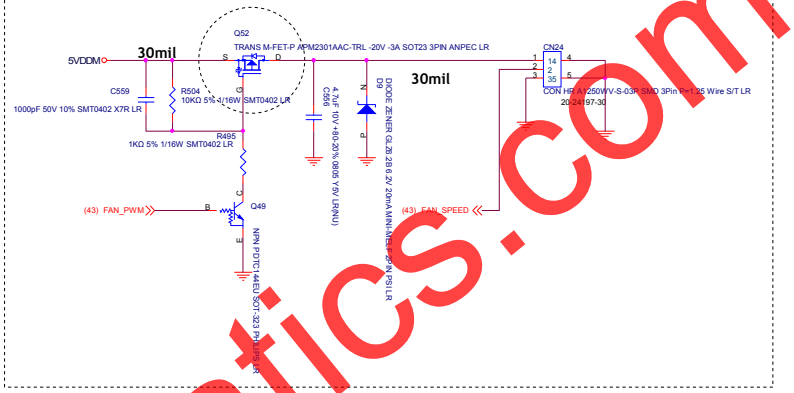
Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 ~5.5 inch	55+/-15%	4 & 8 mils



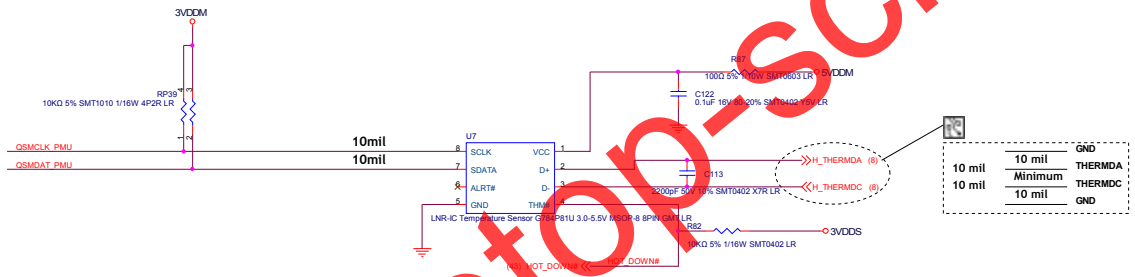


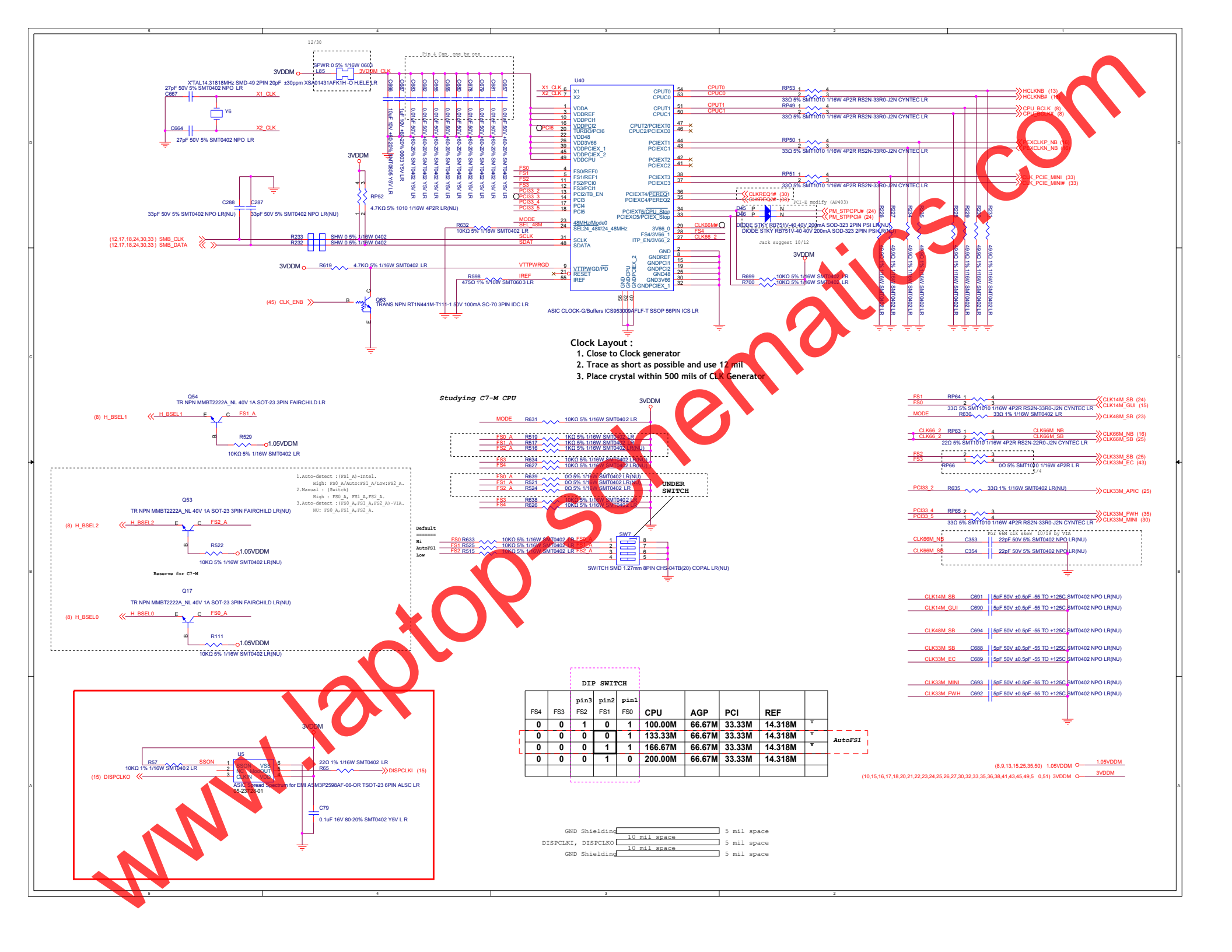


FAN connector

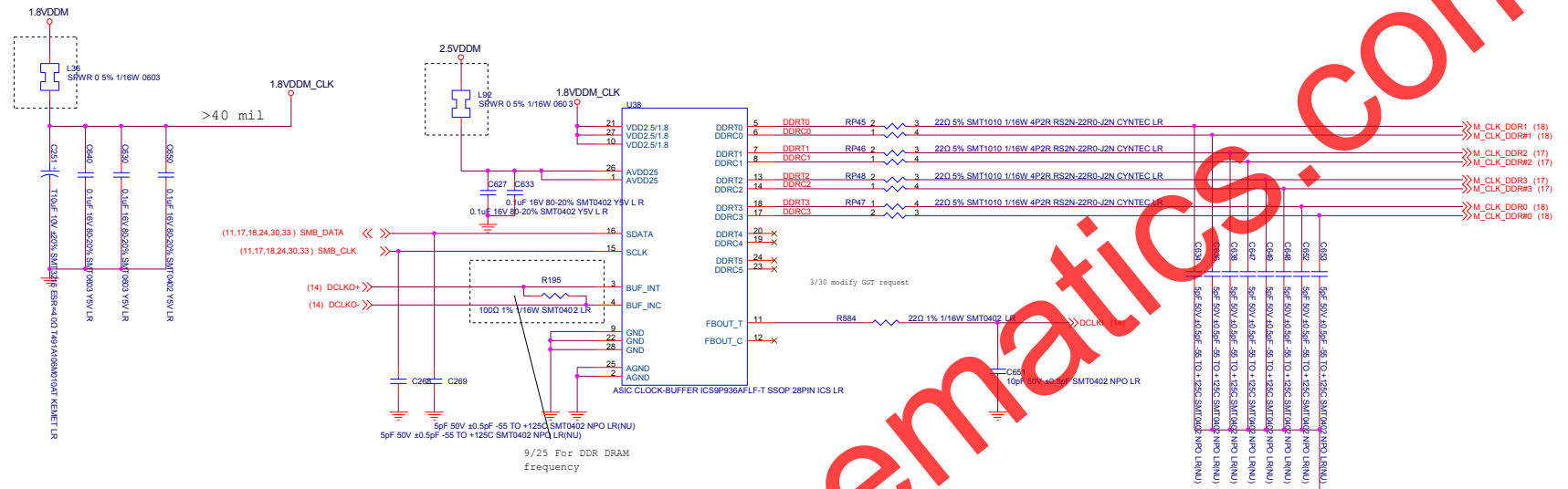


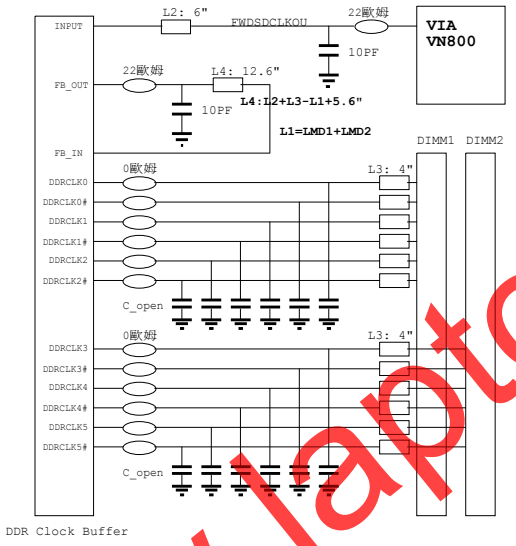
THERMAL SENSOR





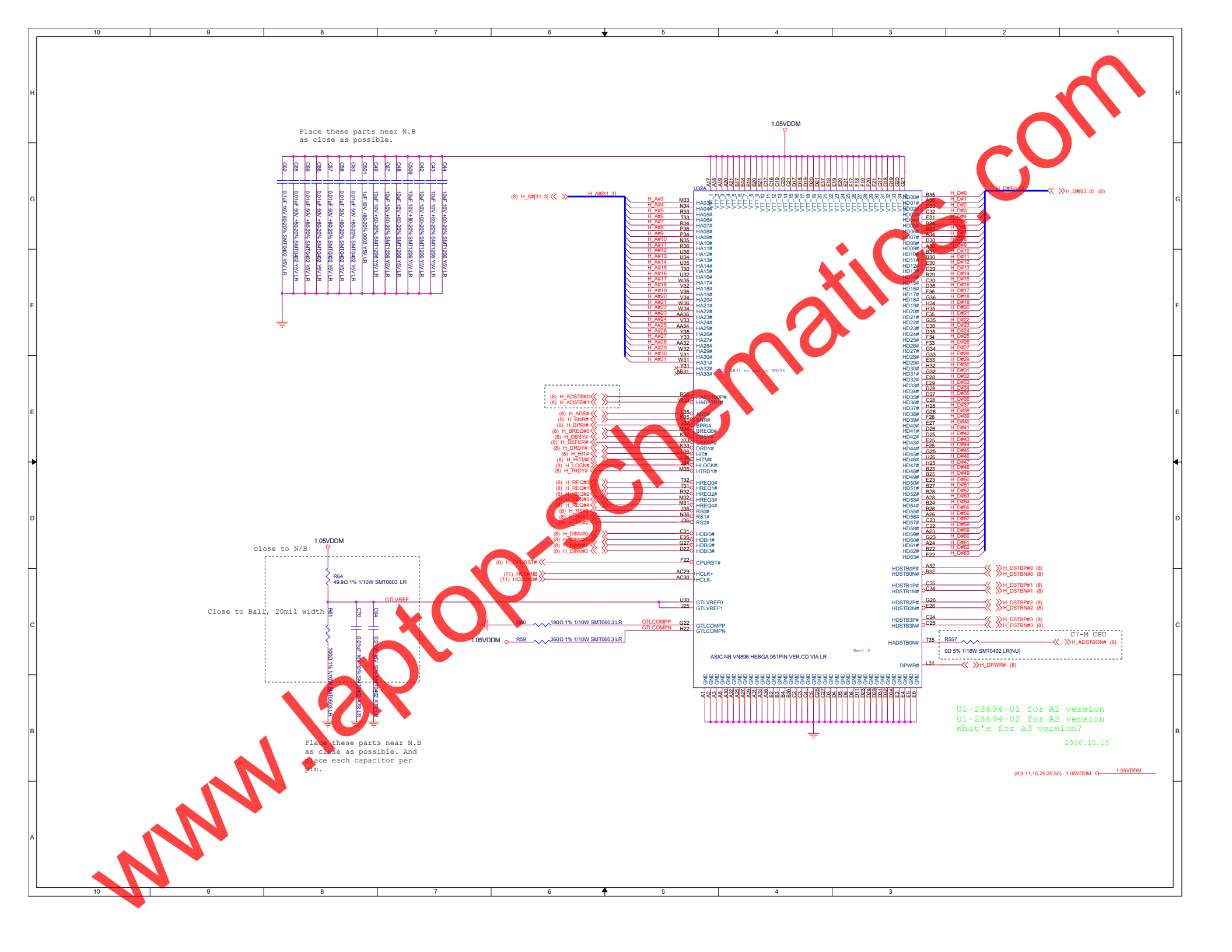
DDR CLOCK BUFFER

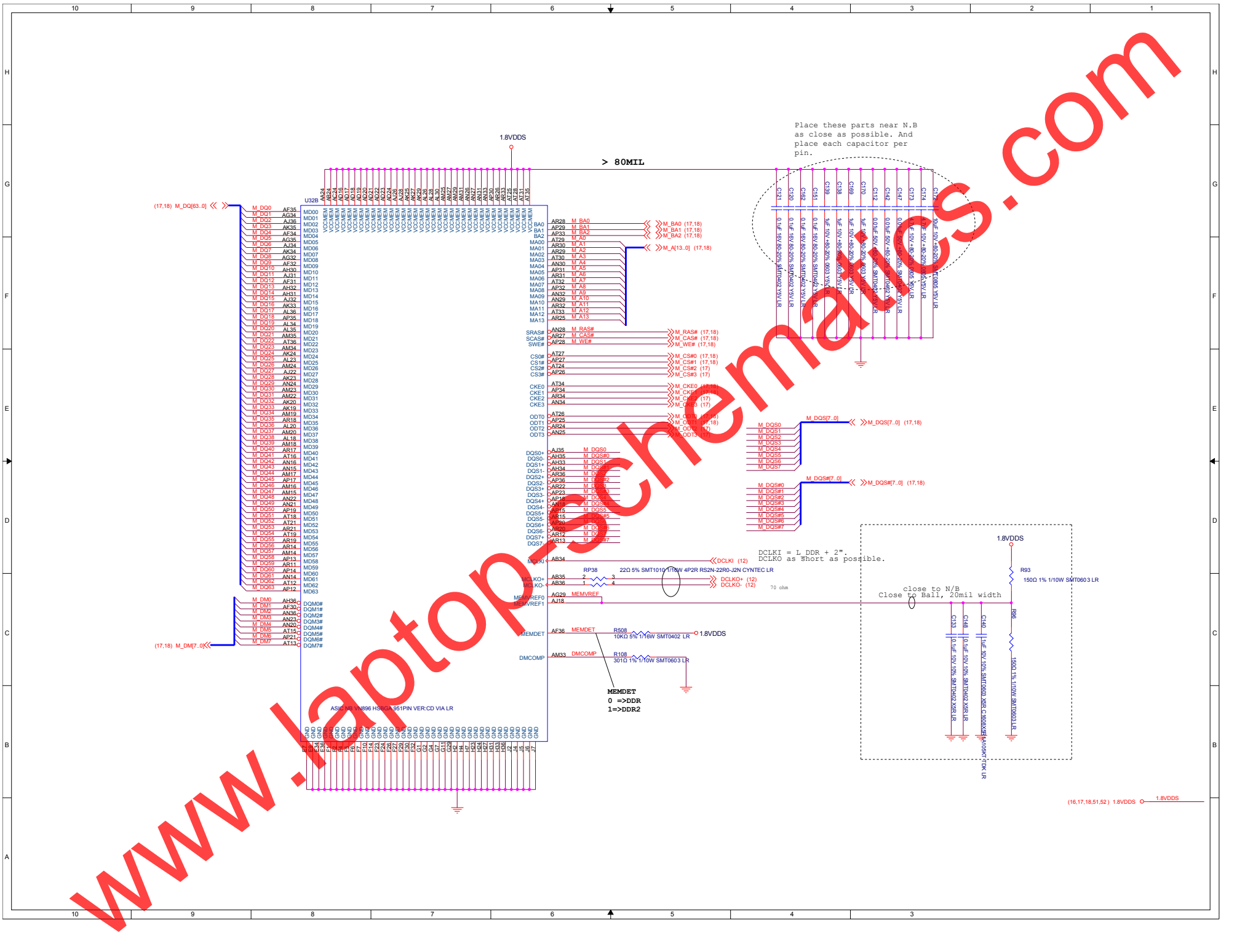


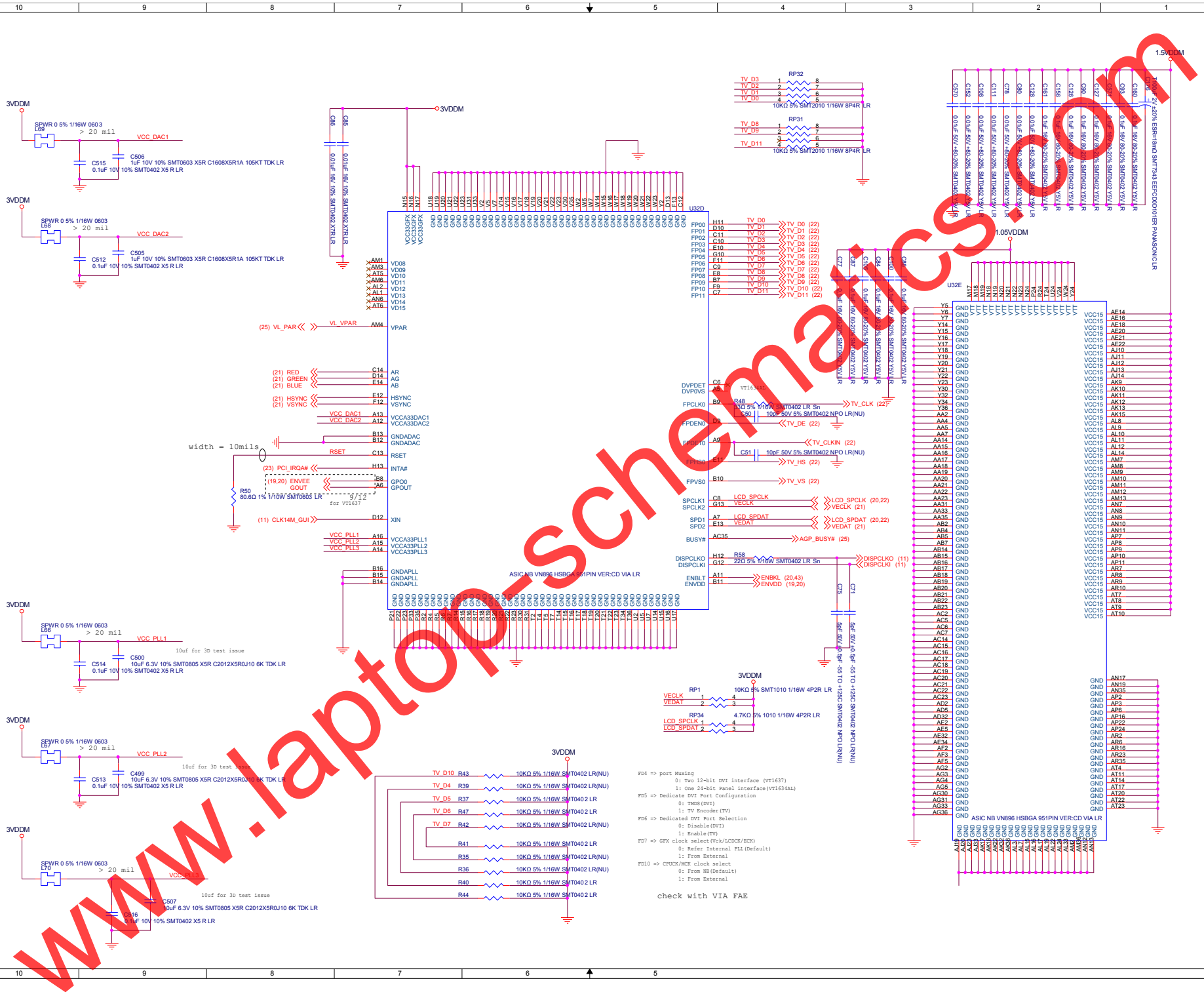


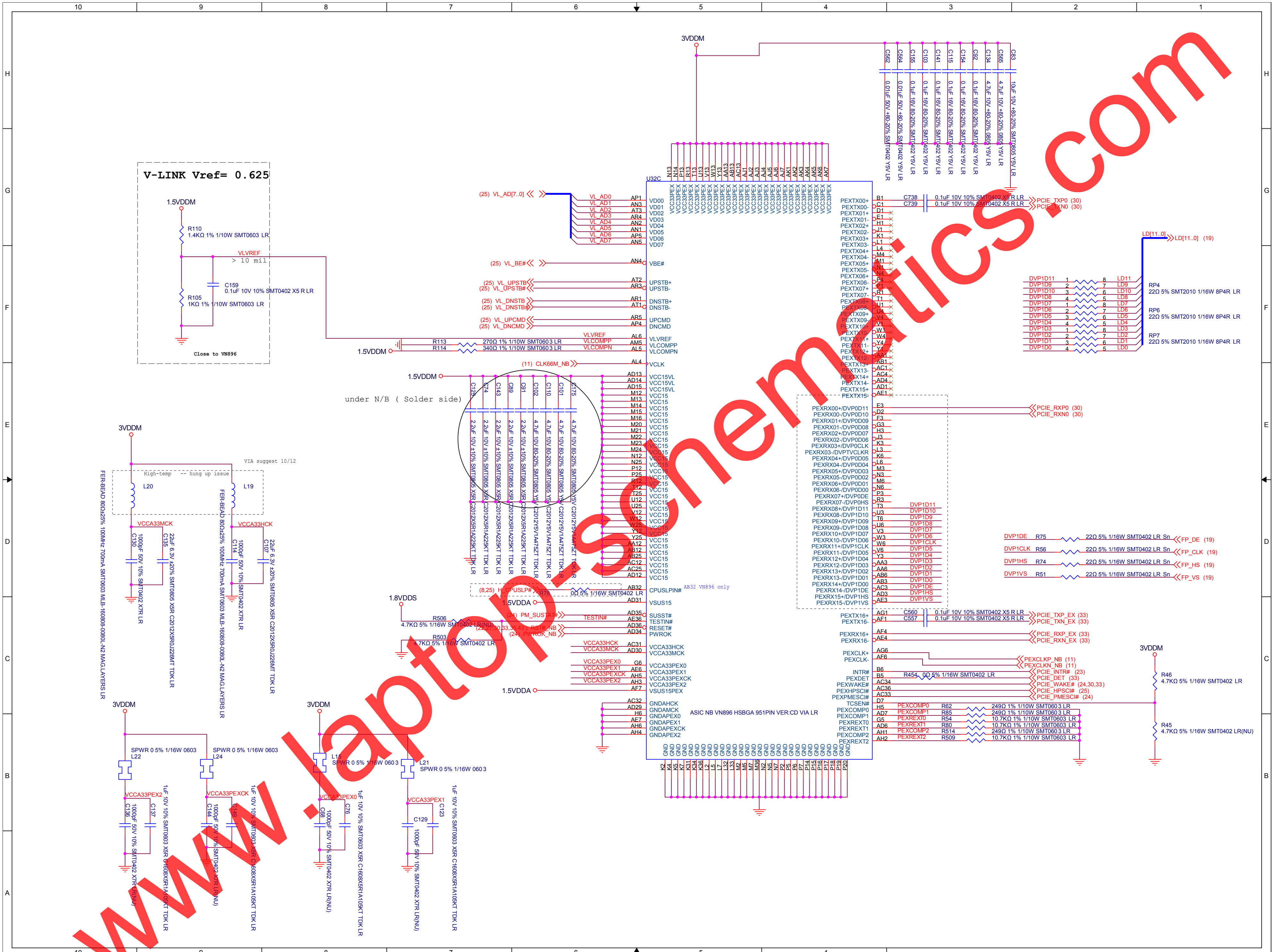
(8,19,22,23,24,25,26,51) 2.5VDDM — 2.5VDDM

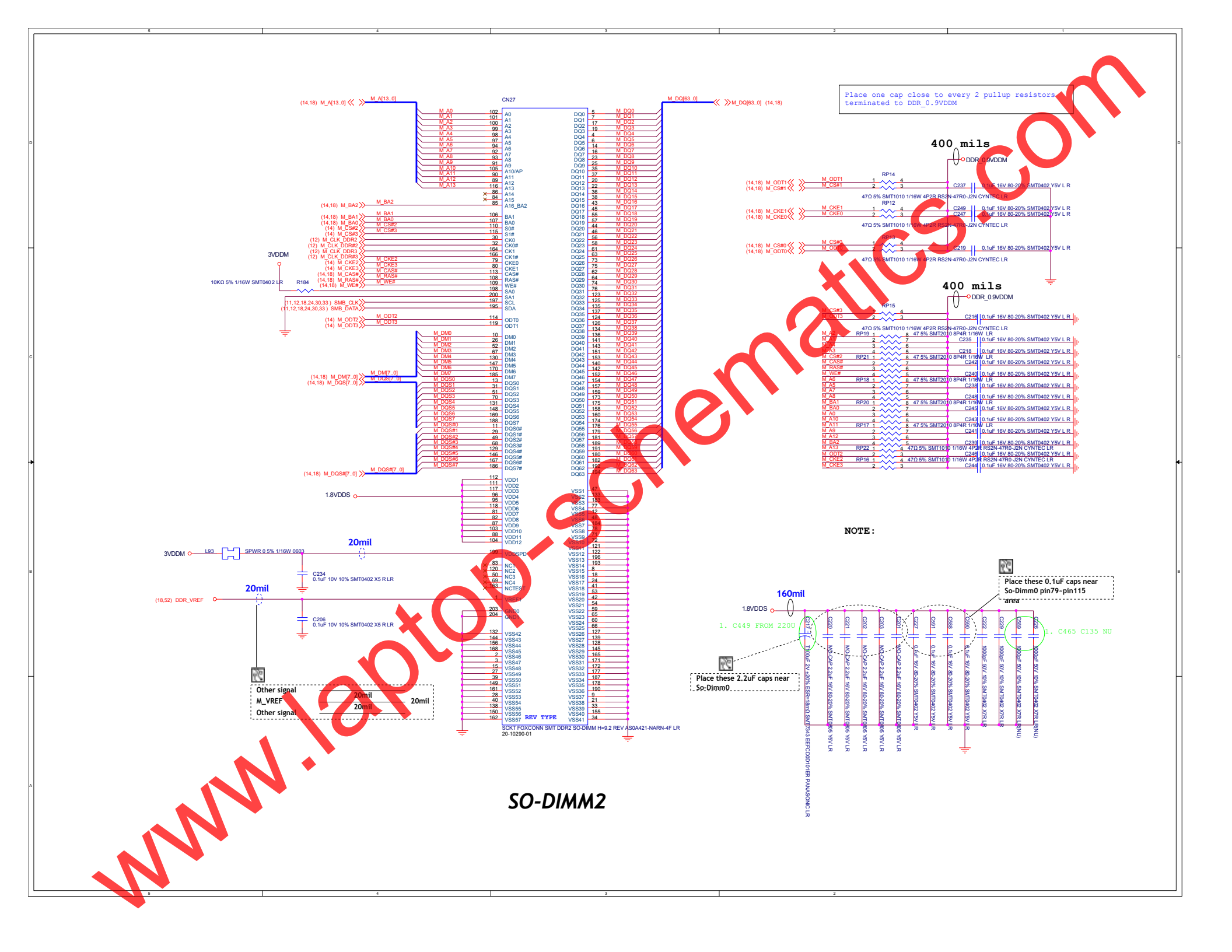
(51) 1.8VDDM — 1.8VDDM

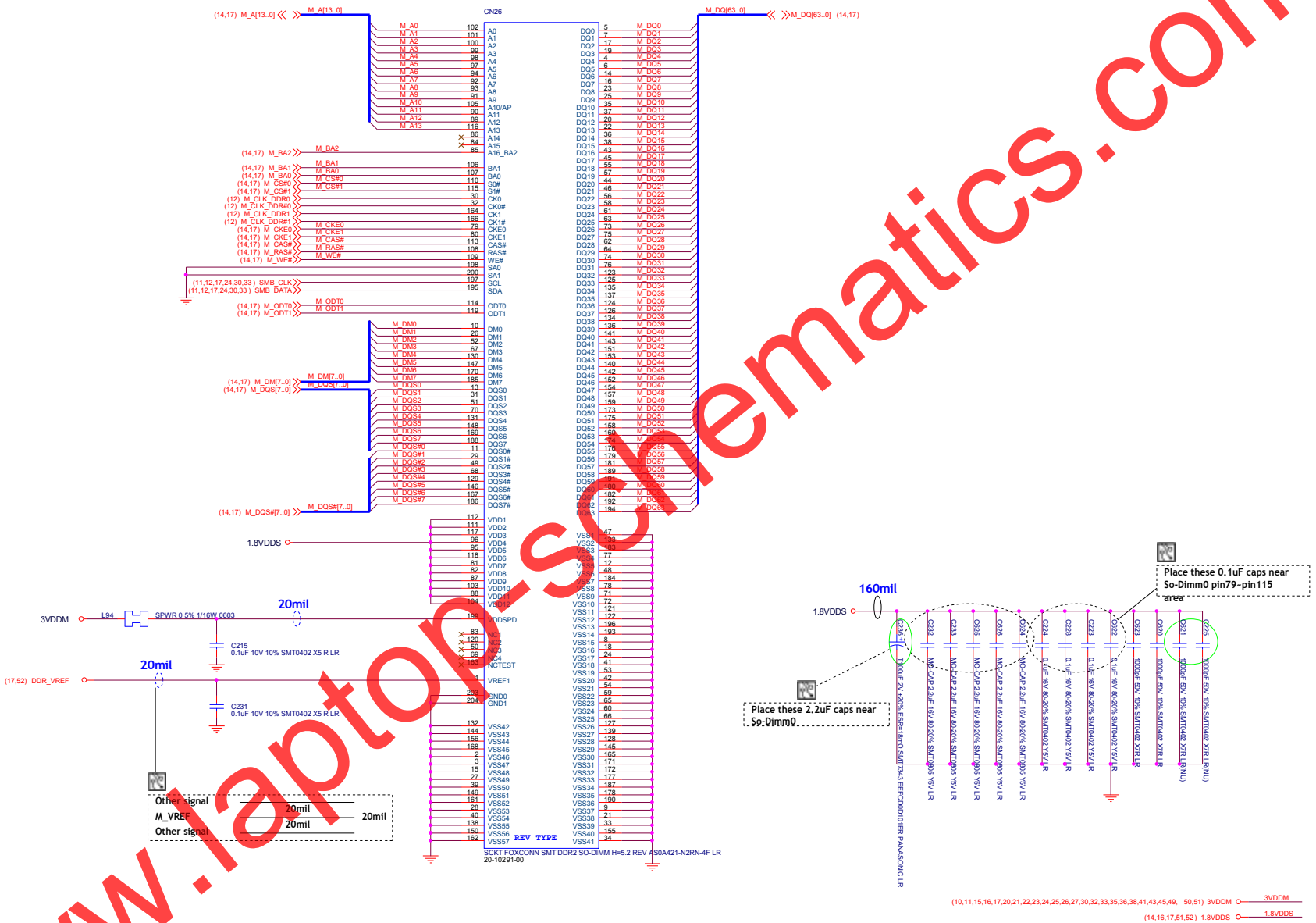




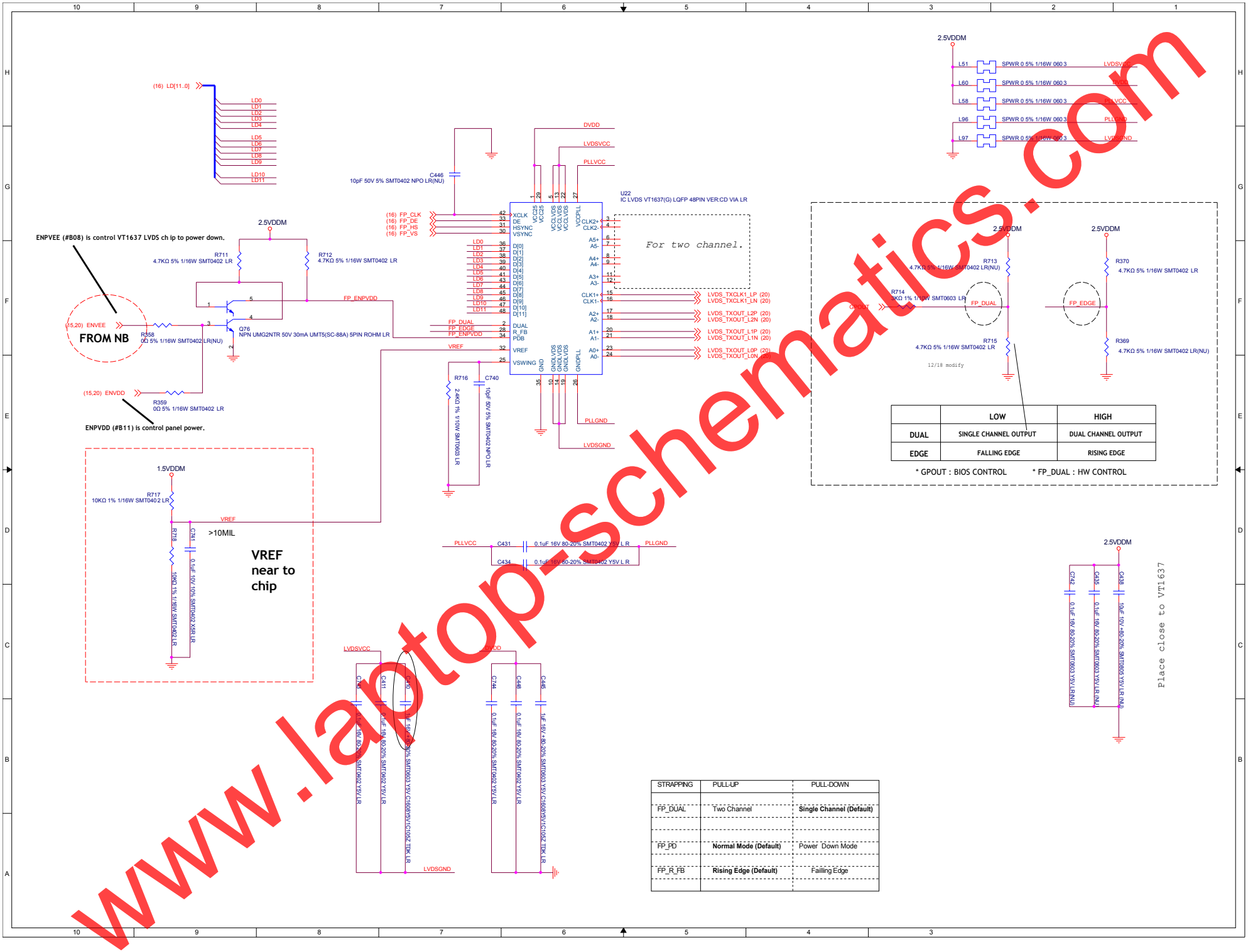

3VDDM
1.5VDDM
1.05VDDM
U32D
U32E
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
width = 10mils
check with VIA FAE
www.laptop-schematics.com

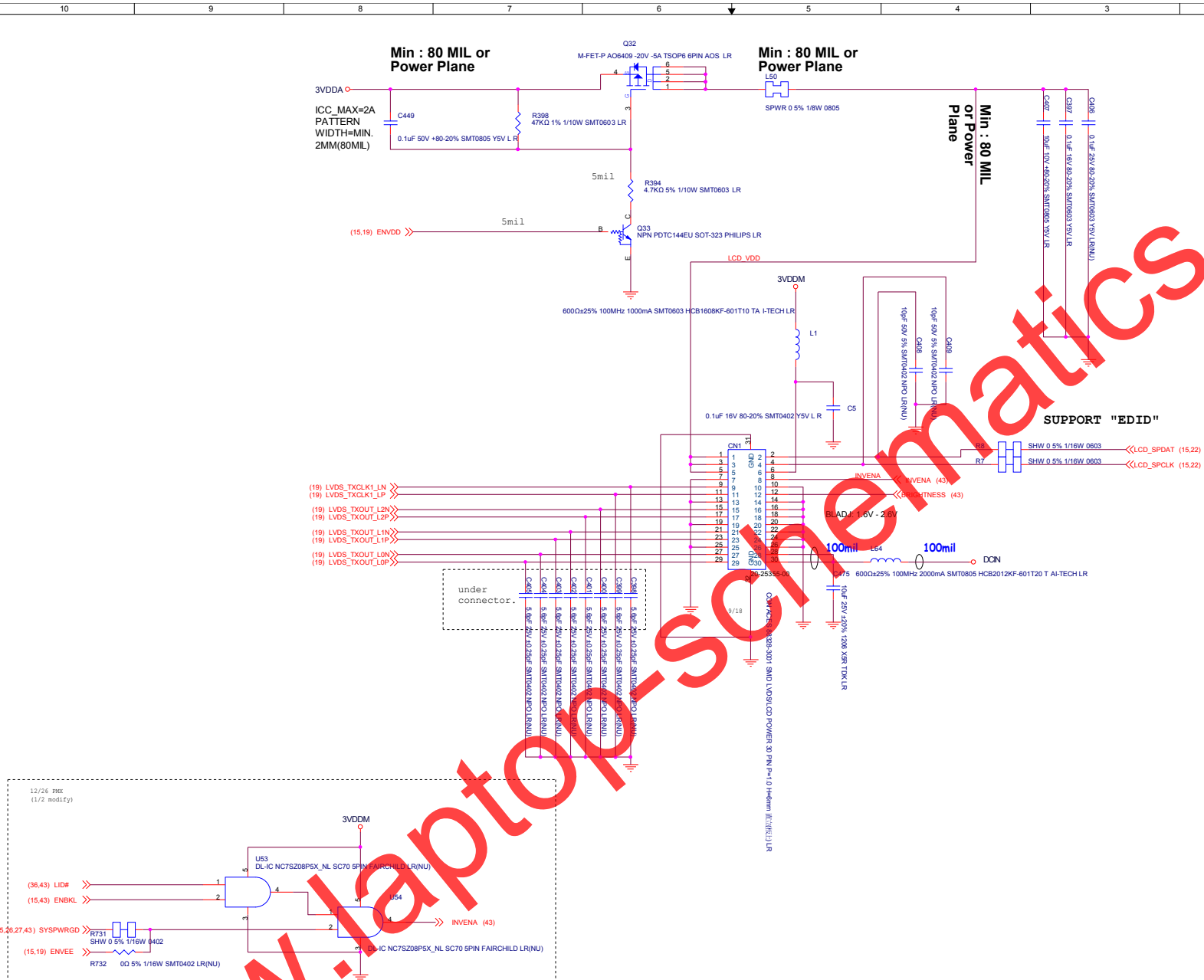






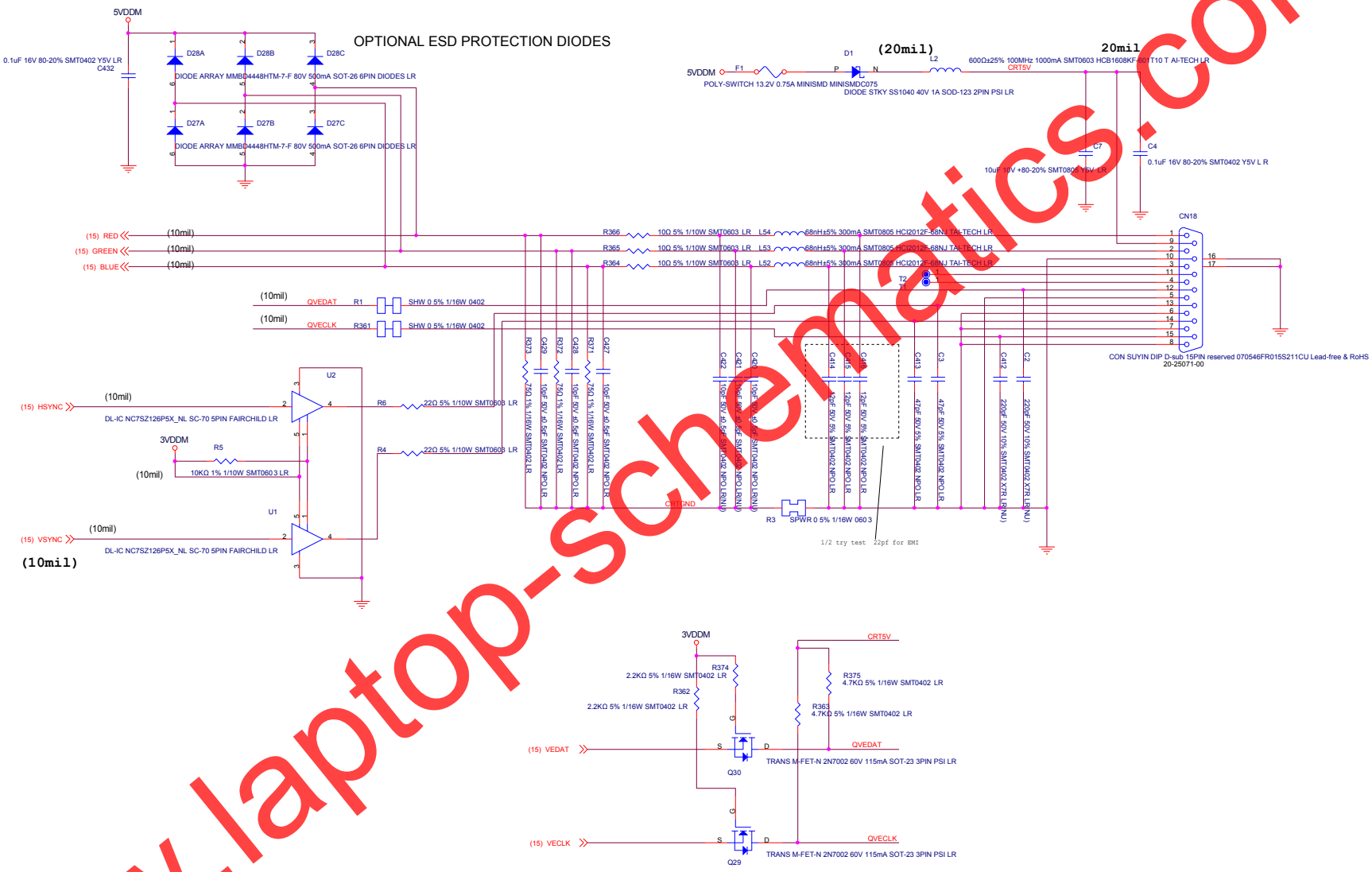
SO-DIMM1

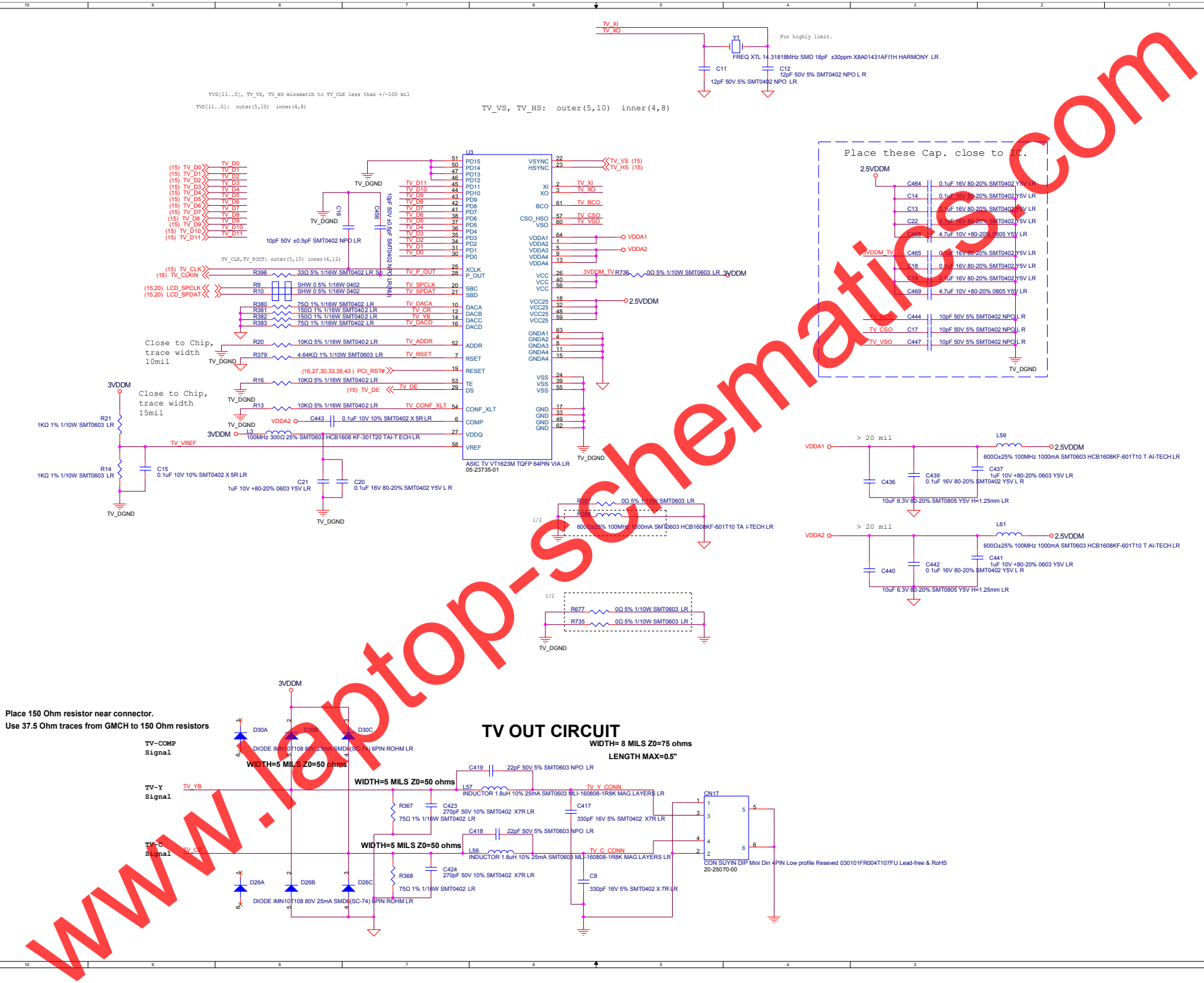


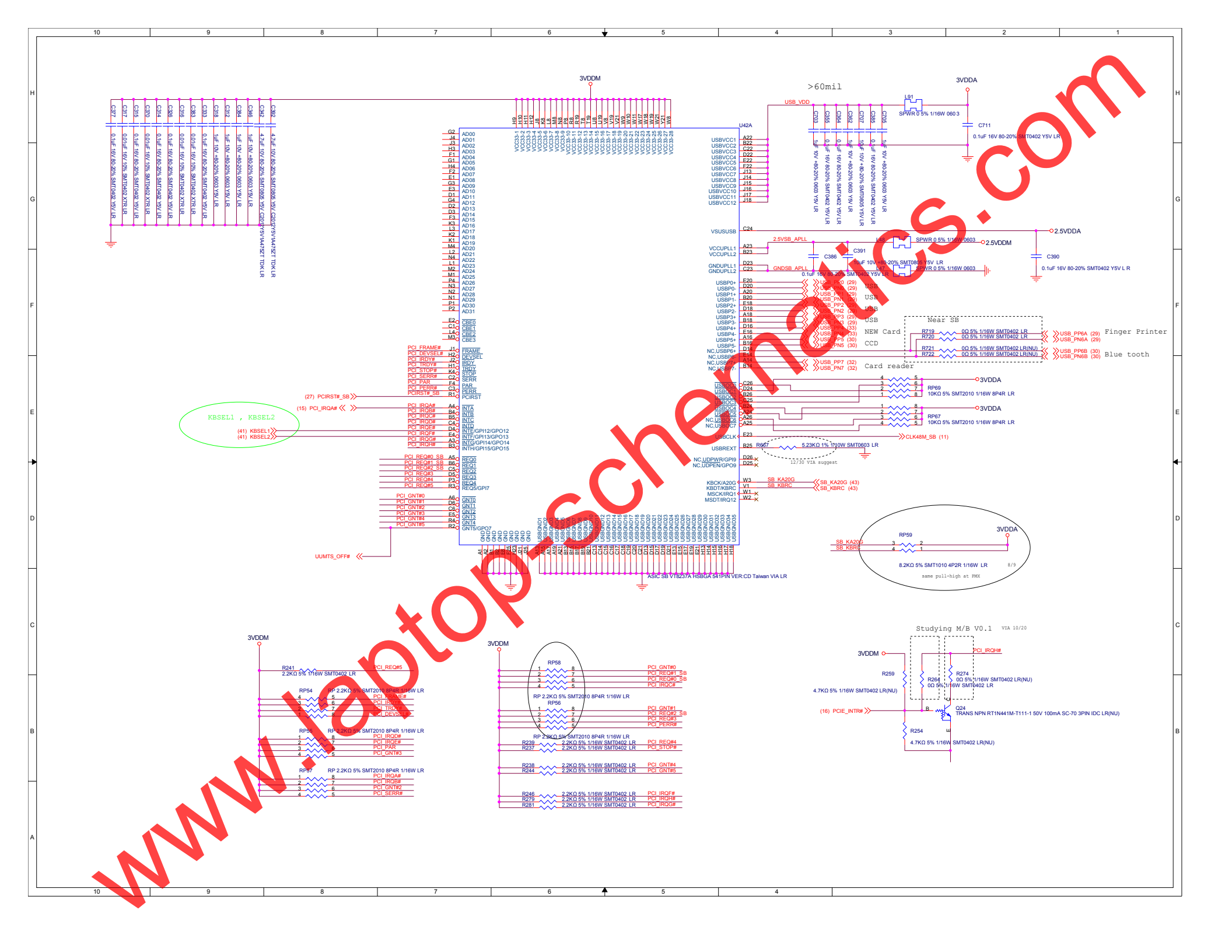


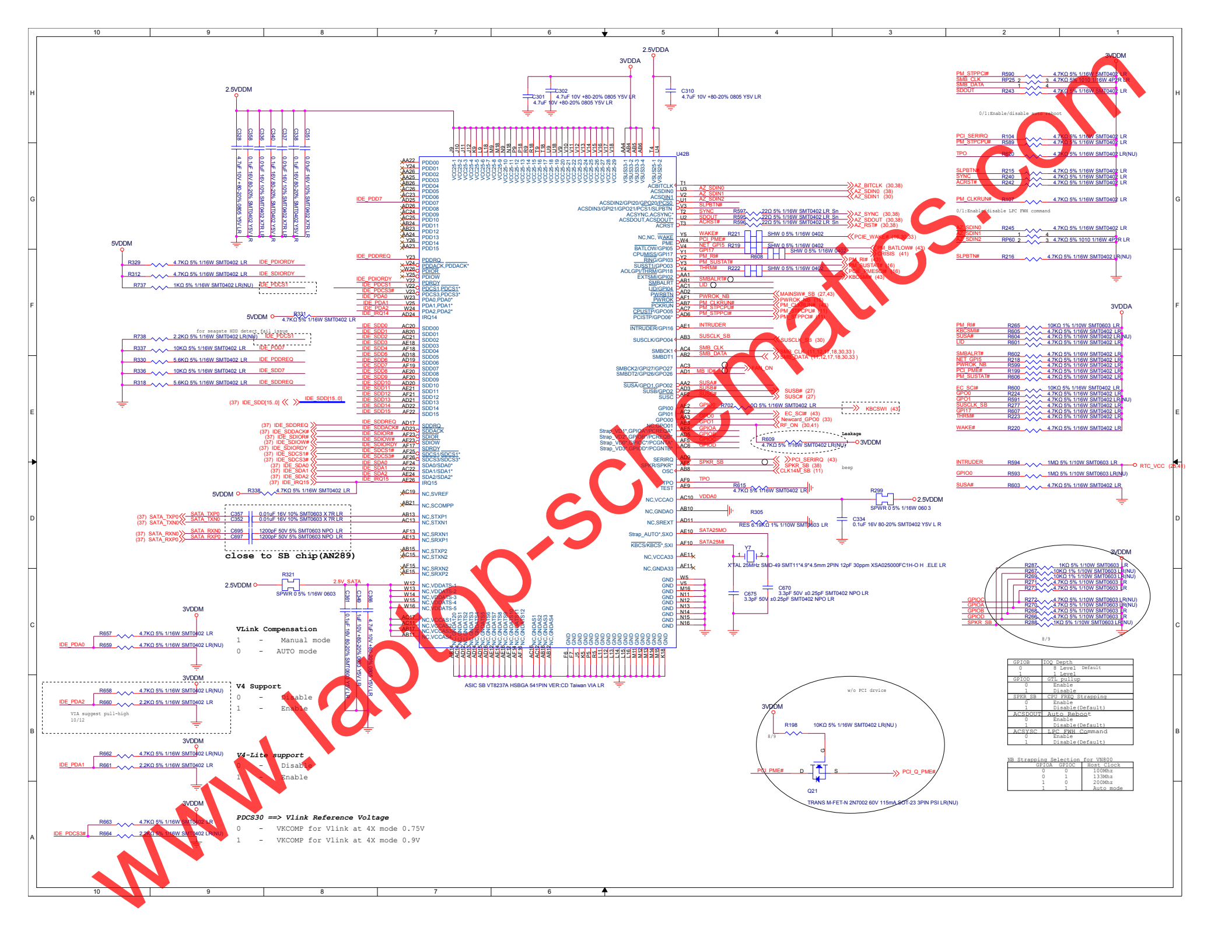
LVDS Interface

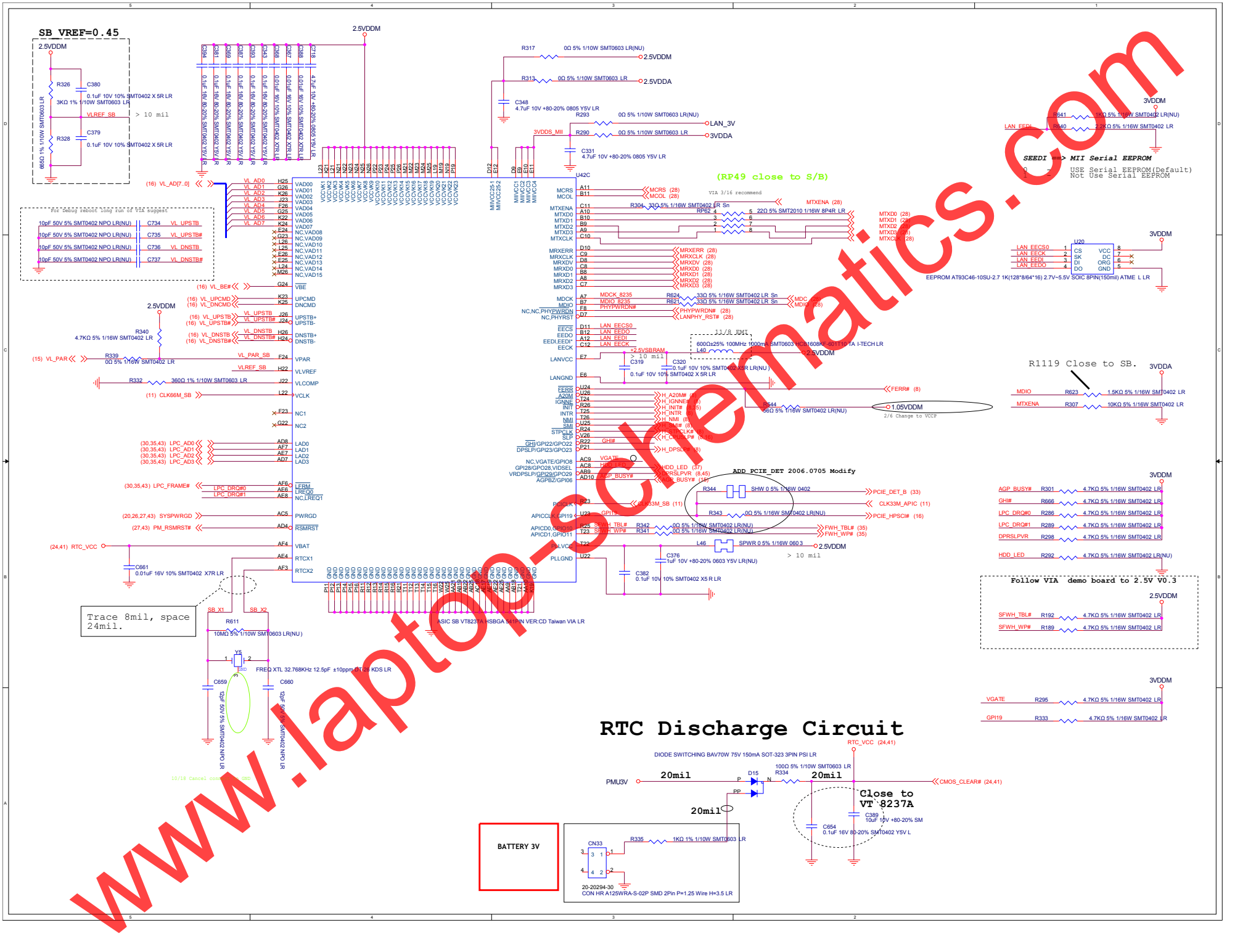
Signal	LENGTH	TRACE	SPACE	TRACE MUTCHING	Impedance	Note
LVDS	10" Cable MAX 16"	4 mils (stripline) 6 mils (microstrip)	20 mils 7 mils (edge to edge) 20 mils (pair to pair) 20 mils (to non LVDS signal)	+/-20 mils (data to clock) +/-20 mils (with a clock pair) X +/-20 mils (clock to clock)	100 ohms +/-15%	Breakout region from NB should be less than 500 mils



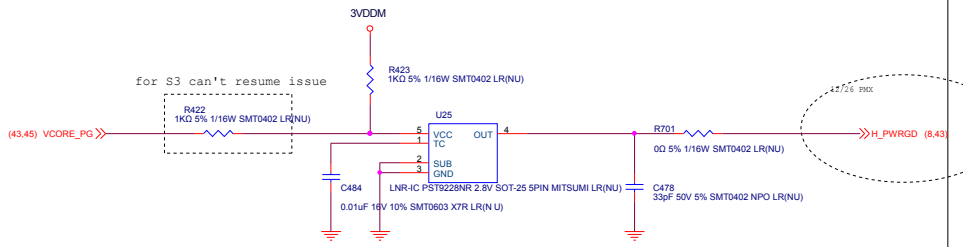

TV_XI
TV_XO
Y1
For highly limit.
FREQ XTL 14.31818MHz SMD 18pF ±30ppm X8A01431AFI1H HARMONY LR
C11
12pF 50V 5% SMT0402 NPO LR
C12
12pF 50V 5% SMT0402 NPO L R
TVD[11..0], TV_VS, TV_HS missmatch to TV_CLK less than +/-100 mil
TVD[11..0]: outer(5,10) inner(4,8)
TV_VS, TV_HS: outer(5,10) inner(4,8)
U3
ASIC TV VT1623M TQFP 64PIN VIA LR
05-23735-01
TV_DGND
10pF 50V ±0.5pF SMT0402 NPO LR
10pF 50V ±0.5pF SMT0402 NPO LR(NA)
TV_CLK,TV_POUT: outer(5,15) inner(4,12)
Close to Chip, trace width 10mil
Close to Chip, trace width 15mil
3VDDM
2.5VDDM
VDDA1
VDDA2
Place these Cap. close to IC.
C464 0.1uF 16V 80-20% SMT0402 Y5V LR
C14 0.1uF 16V 80-20% SMT0402 Y5V LR
C13 0.1uF 16V 80-20% SMT0402 Y5V LR
C22 0.1uF 16V 80-20% SMT0402 Y5V LR
C468 4.7uF 10V +80-20% 0805 Y5V LR
C465 0.1uF 16V 80-20% SMT0402 Y5V LR
C18 0.1uF 16V 80-20% SMT0402 Y5V LR
C19 0.1uF 16V 80-20% SMT0402 Y5V LR
C469 4.7uF 10V +80-20% 0805 Y5V LR
C444 10pF 50V 5% SMT0402 NPO L R
C17 10pF 50V 5% SMT0402 NPO L R
C447 10pF 50V 5% SMT0402 NPO L R
L59
L61
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 T AI-TECH LR
C436
C439 0.1uF 16V 80-20% SMT0402 Y5V L R
C437 1uF 10V +80-20% 0603 Y5V LR
10uF 6.3V 80-20% SMT0805 Y5V H=1.25mm LR
C440
C442 0.1uF 16V 80-20% SMT0402 Y5V L R
C441 1uF 10V +80-20% 0603 Y5V LR
R367 0Ω 5% 1/10W SMT0603 LR
R368 0Ω 5% 1/10W SMT0603 LR
R677 0Ω 5% 1/10W SMT0603 LR
R735 0Ω 5% 1/10W SMT0603 LR
Place 150 Ohm resistor near connector.
Use 37.5 Ohm traces from GMCH to 150 Ohm resistors
TV OUT CIRCUIT
WIDTH= 8 MILS Z0=75 ohms
LENGTH MAX=0.5"
TV-COMP Signal
TV-Y Signal
TV-C Signal
WIDTH=5 MILS Z0=50 ohms
D30A
D30B
D30C
D26A
D26B
D26C
DIODE IMN10T108 80V 25mA SMD6(SC-74) 6PIN ROHM LR
L57 INDUCTOR 1.8uH 10% 25mA SMT0603 MLI-160808-1R8K MAG.LAYERS LR
L56 INDUCTOR 1.8uH 10% 25mA SMT0603 MLI-160808-1R8K MAG.LAYERS LR
C419 22pF 50V 5% SMT0603 NPO LR
C418 22pF 50V 5% SMT0603 NPO LR
C423 270pF 50V 10% SMT0402 X7R LR
C424 270pF 50V 10% SMT0402 X7R LR
C417 330pF 16V 5% SMT0402 X7R LR
C8 330pF 16V 5% SMT0402 X 7R LR
CN17
CON SUYIN DIP Mini Din 4PIN Low profile Reseved 030101FR004T107FU Lead-free & RoHS
20-25070-00
www.laptop-schematic.com



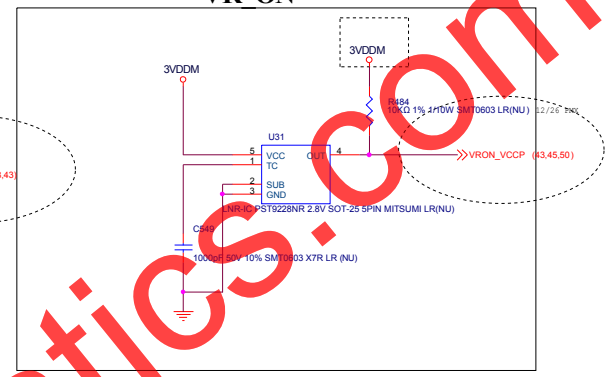




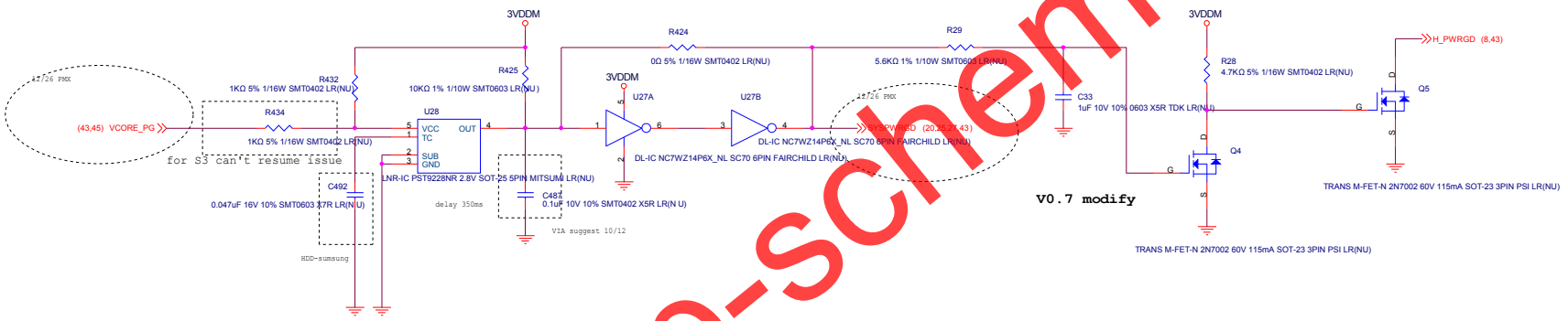
CPU POWER OK CIRCUIT



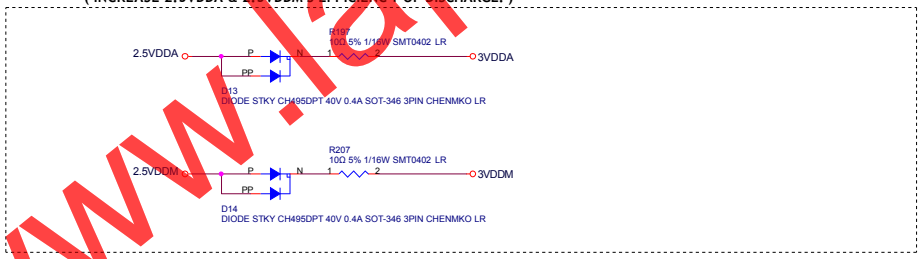
VR_ON LM10W-- connect 5VDDM



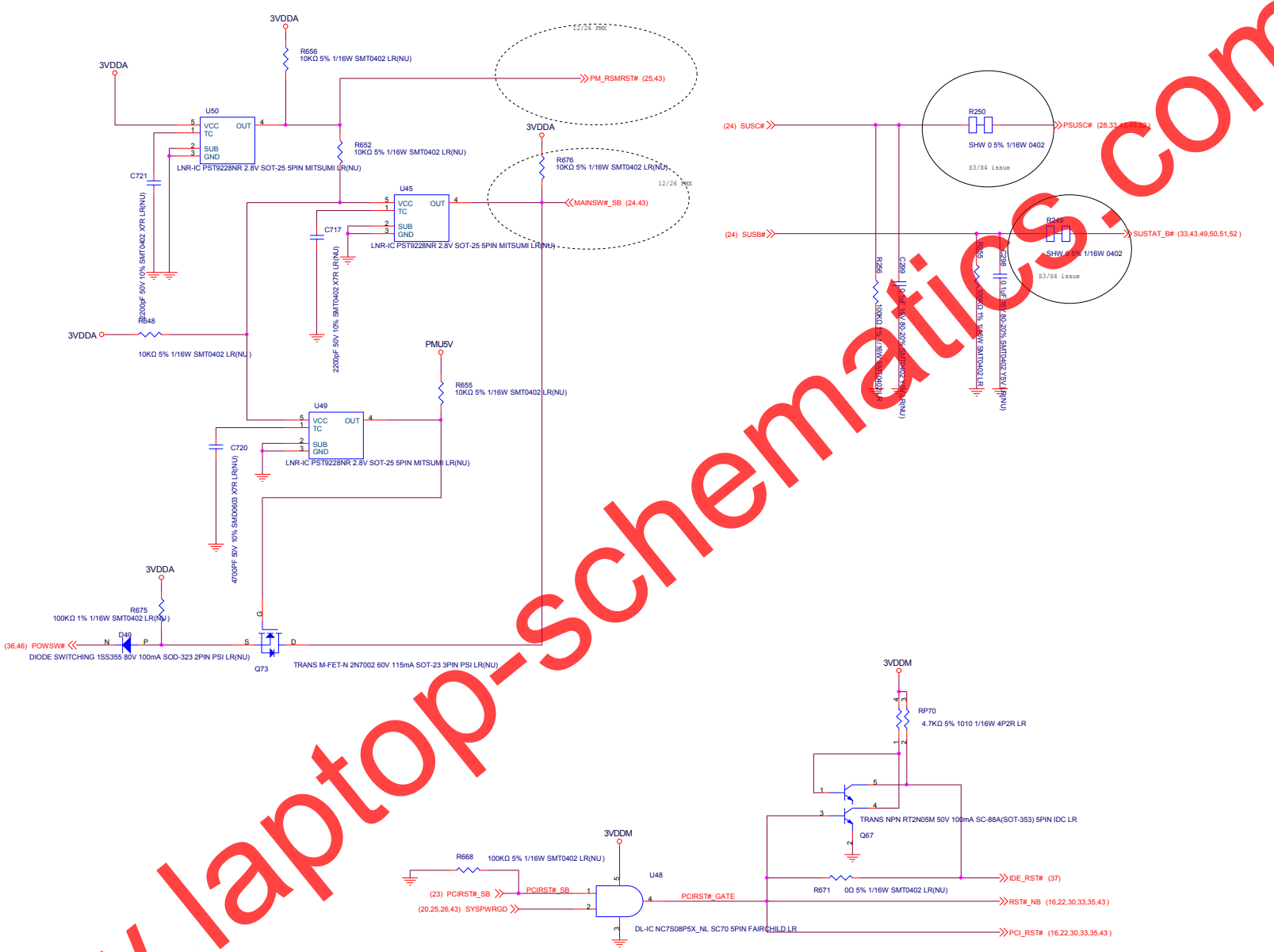
SYSTEM POWER OK CIRCUIT

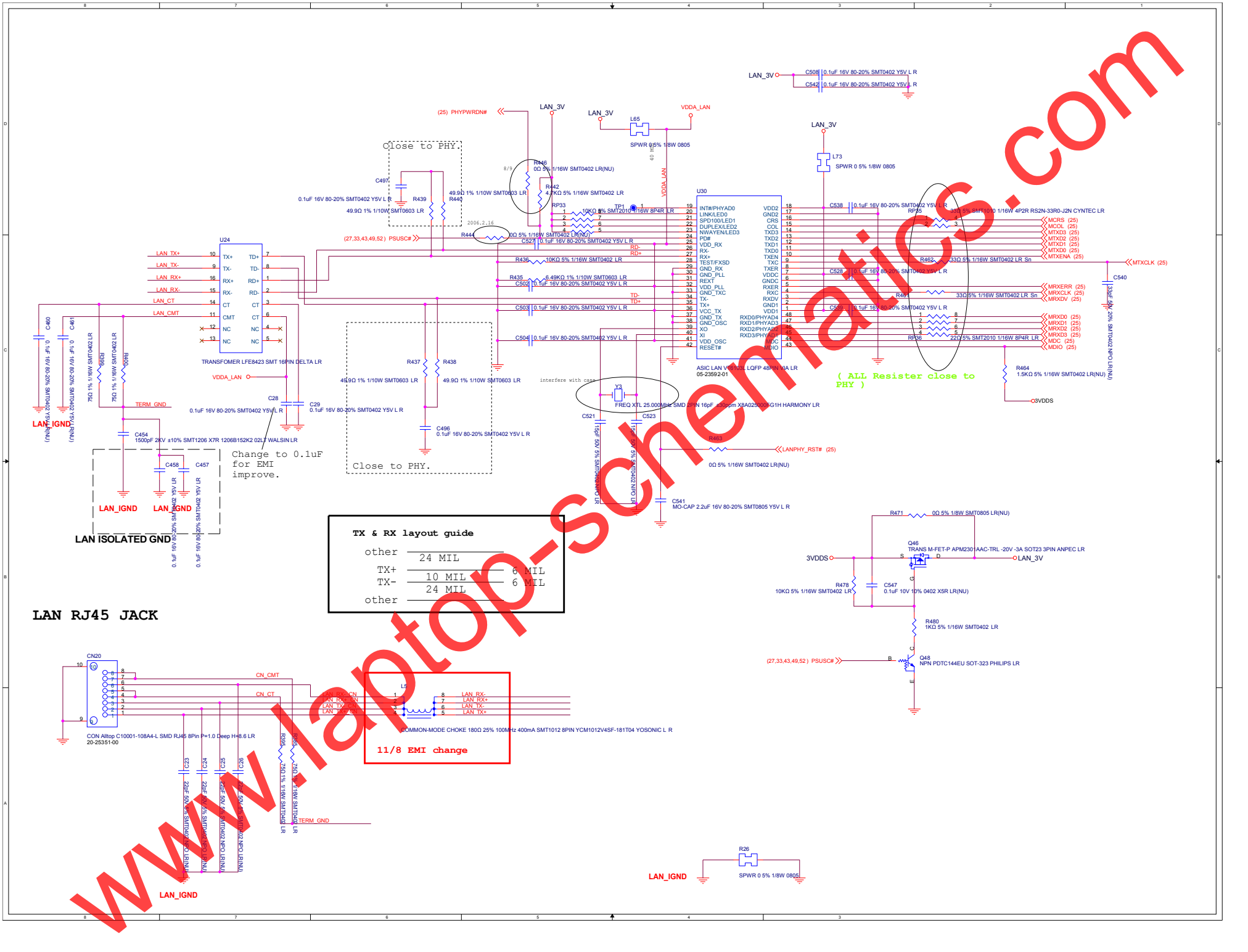


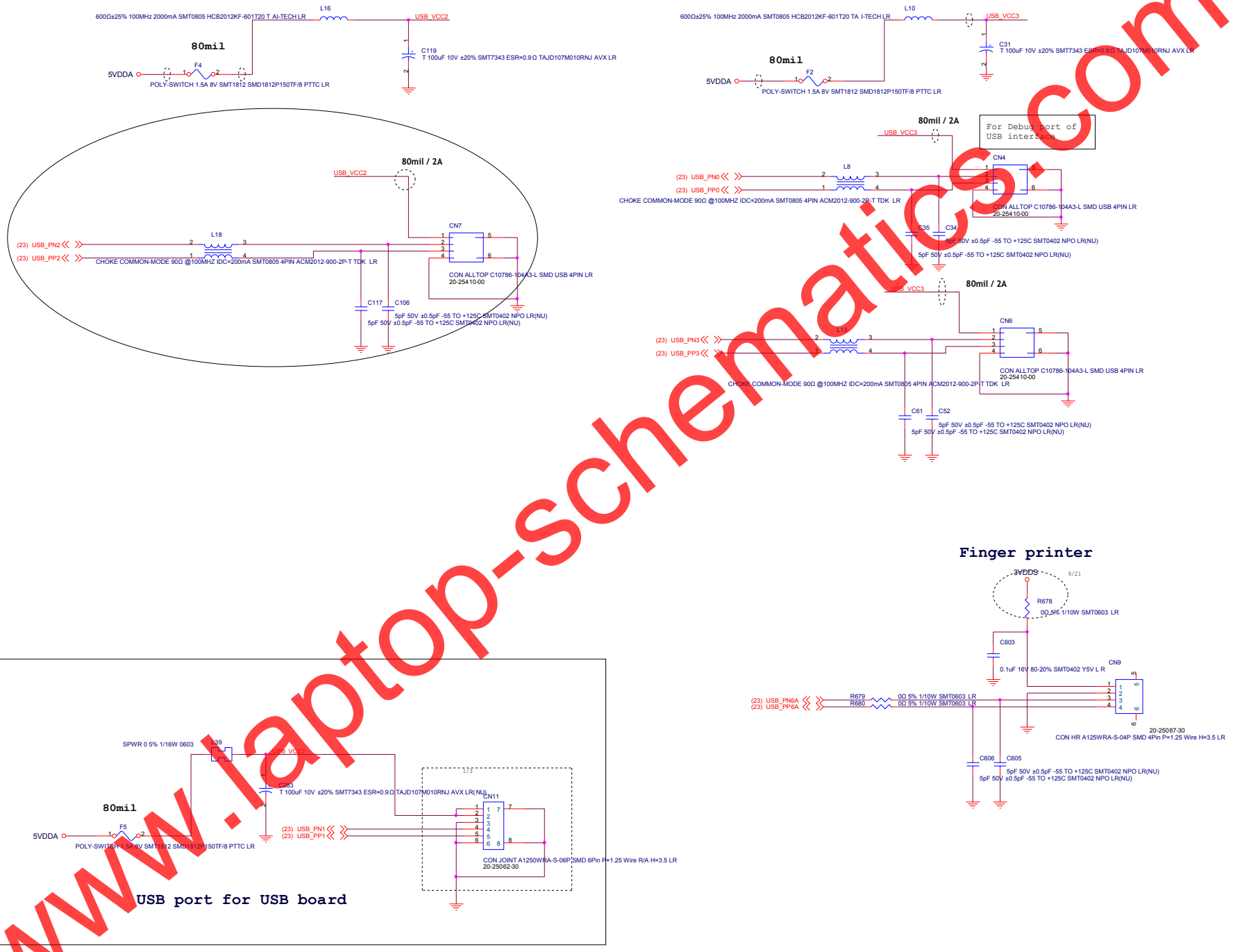
20060824A-FOLLOW LM10W V0.4. FOR RTC DELAY ISSUE.
(INCREASE 2.5VDDA & 2.5VDDM'S EFFICIENC Y OF DISCHARGE.)



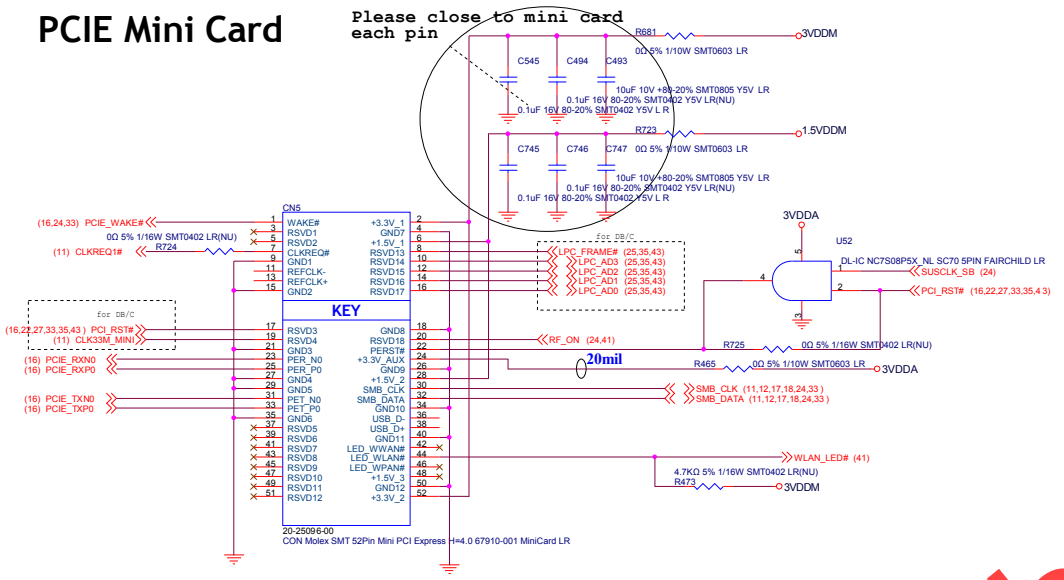
RESUME
RESET

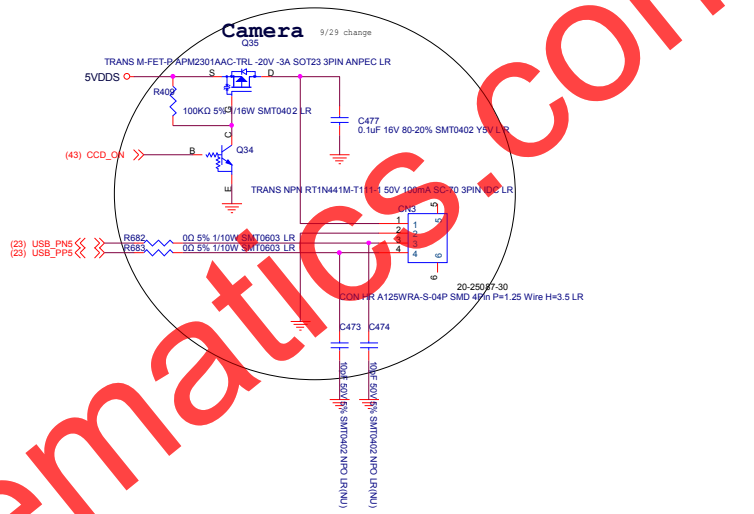


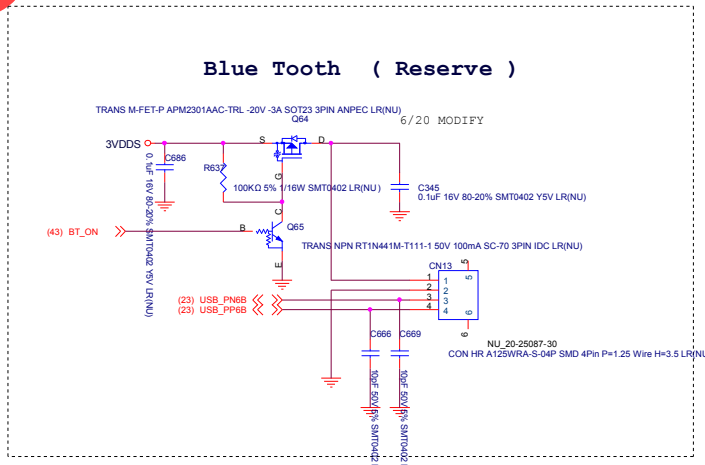




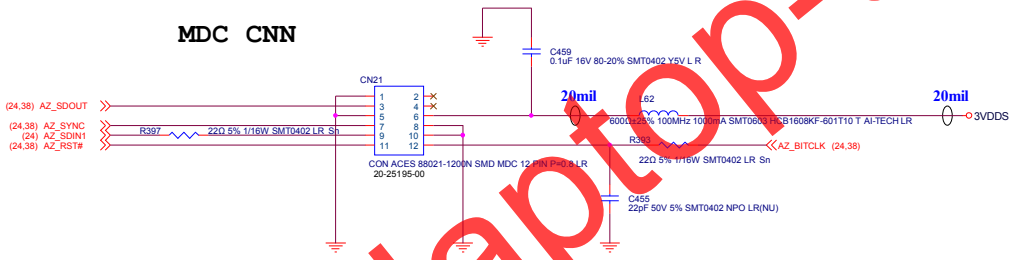
PCIE Mini Card







MDC CNN



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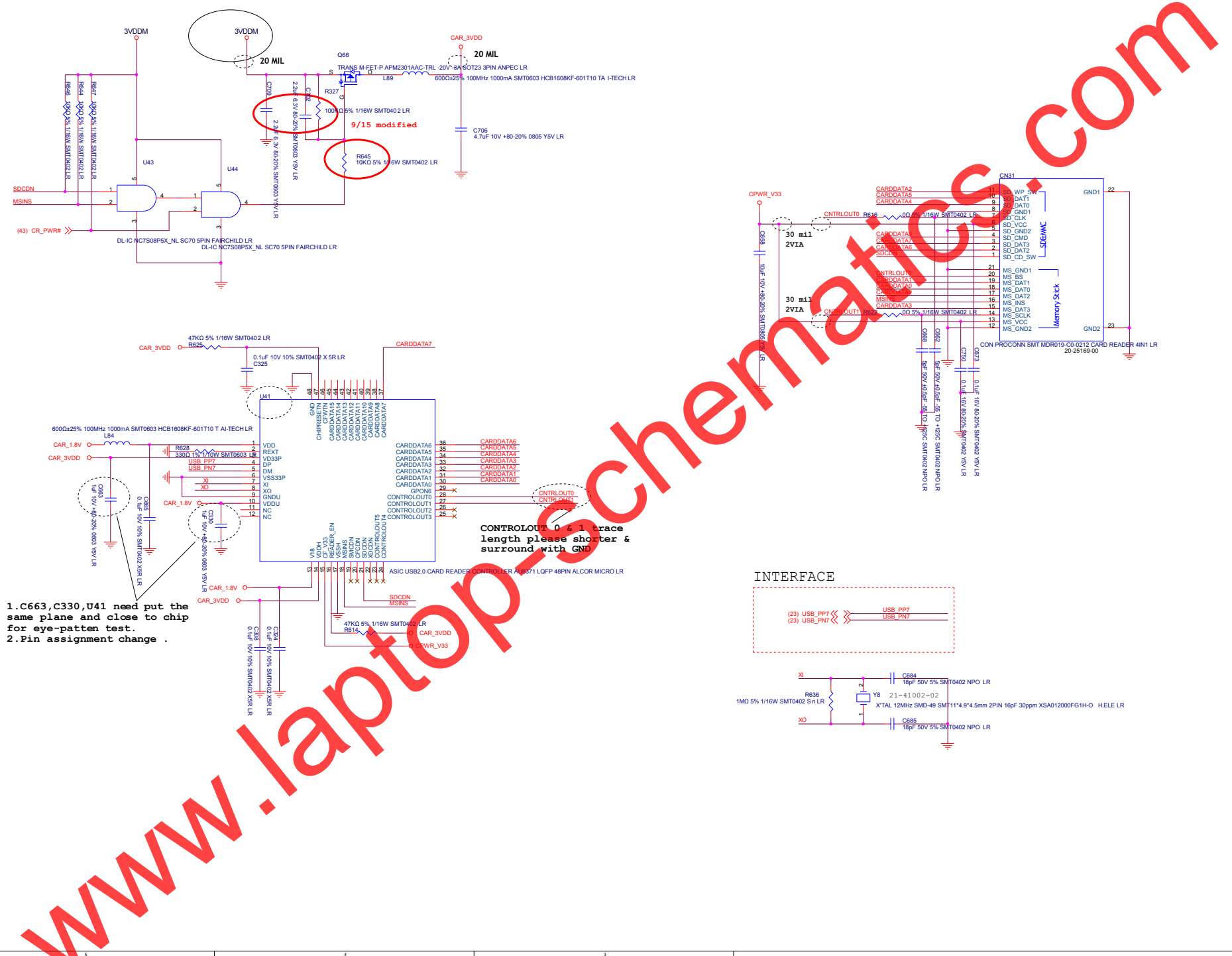

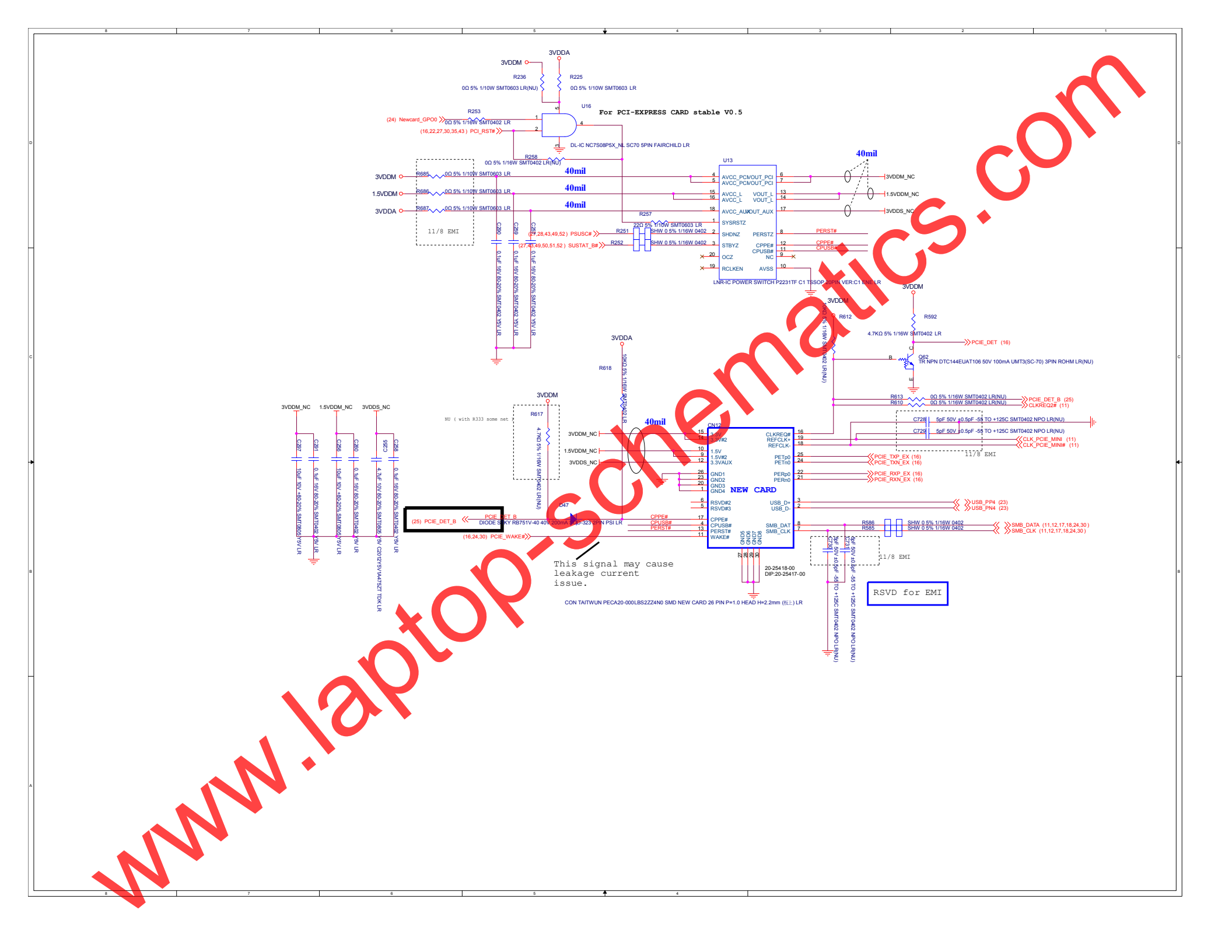

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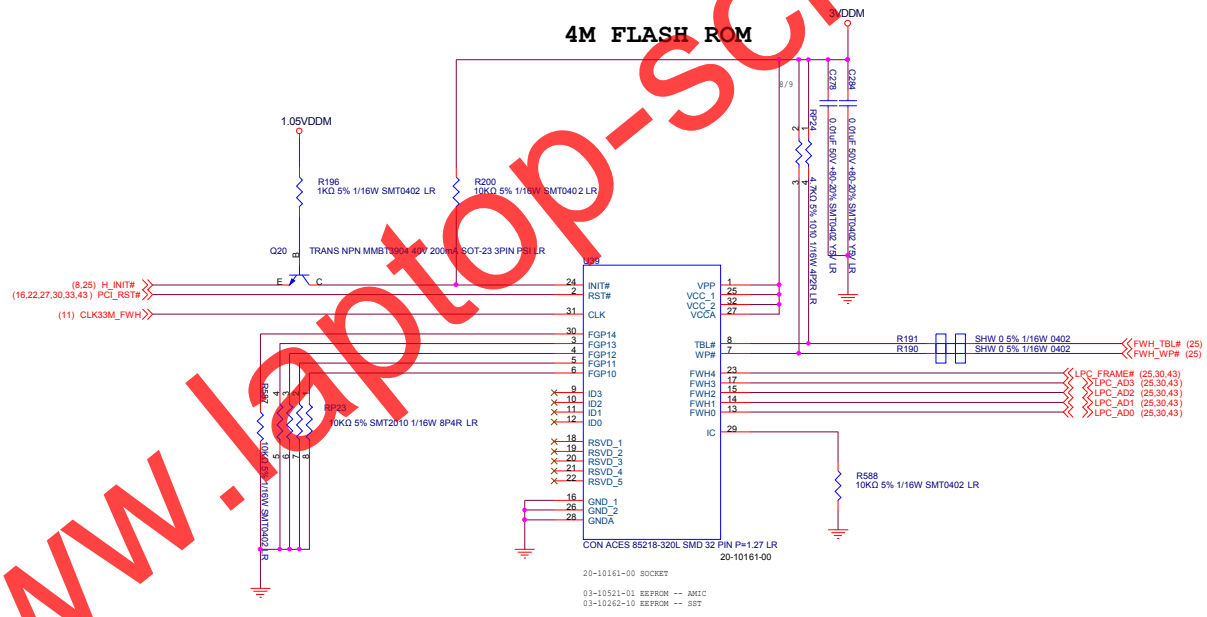
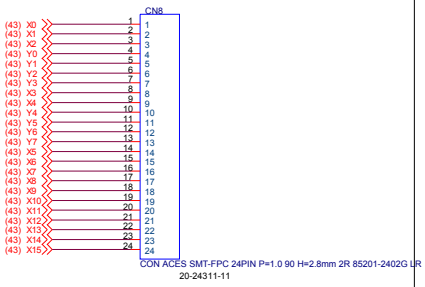
4M FLASH ROM



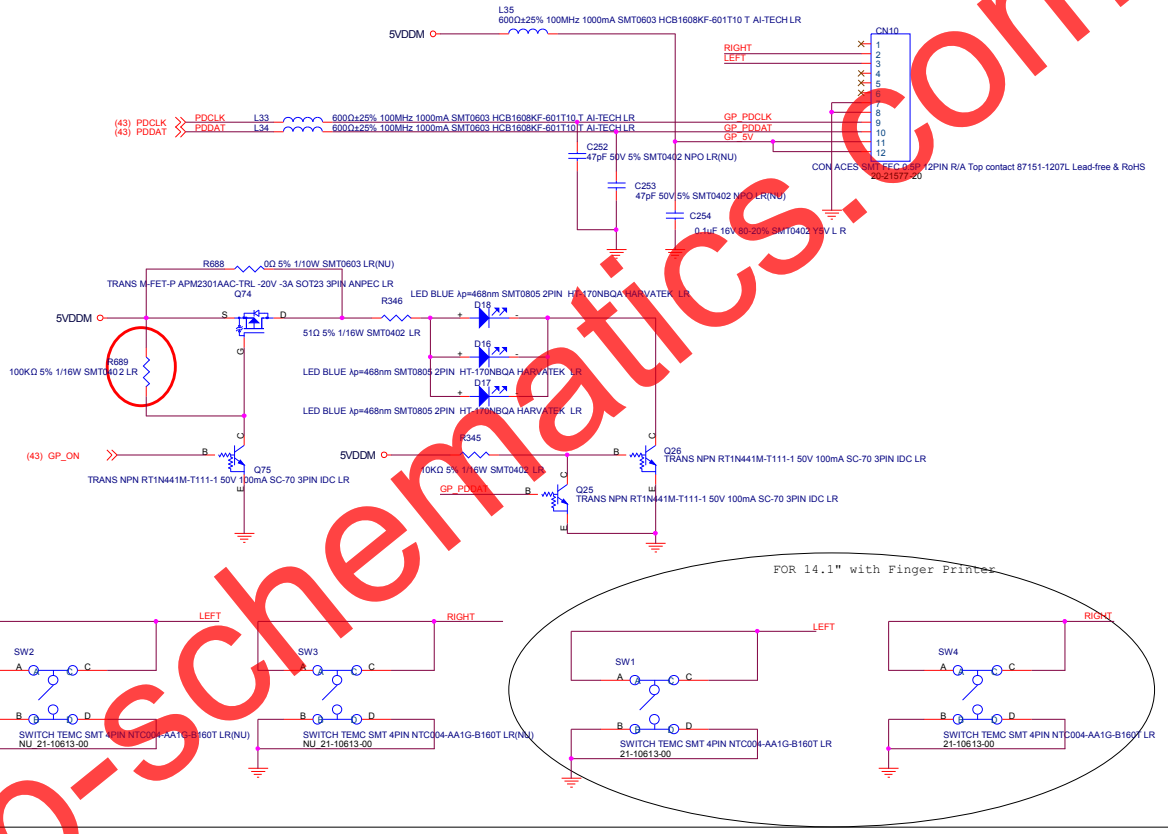
Same as CTx projects

INT KB CNN

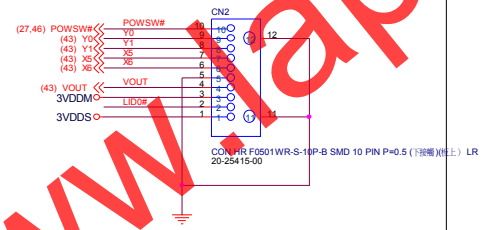


GLIDE PAD CONNECTOR

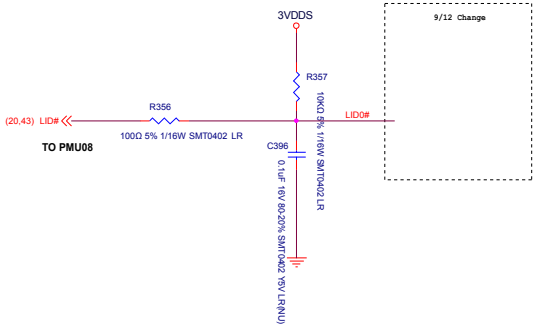
GLIDE PAD Pin define
For ALPS



SWITCH BOARD CONNECTOR



LID Switch



NOTE

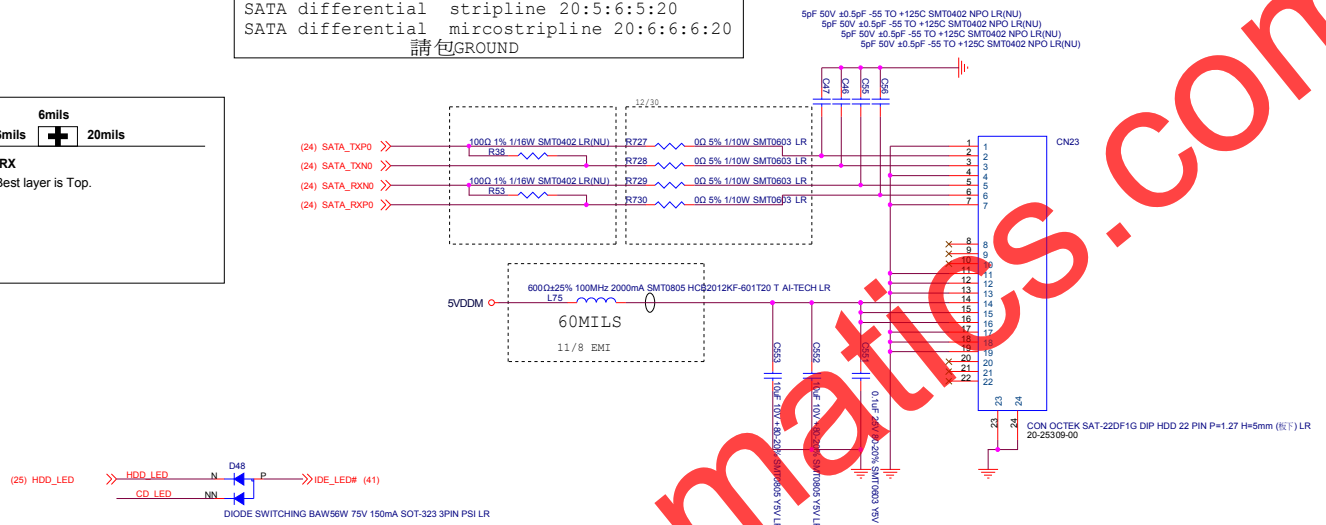
SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

SATA Layout Note:

MS or SL:

6mils 6mils 6mils 6mils
20mils + 6mils − 20mils − 6mils + 20mils
TX RX

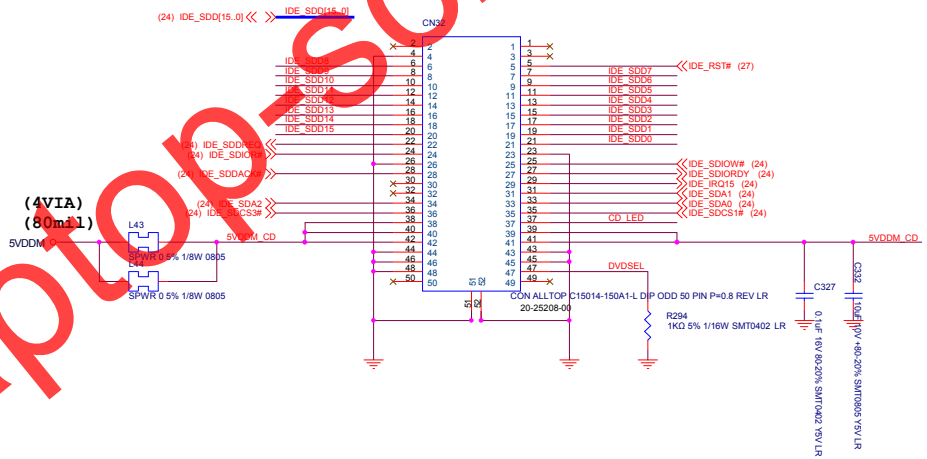
* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.



IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN



AZALIA CODEC LAYOUT

10mil — GND_POWER
10mil — 10mil — AC97_PCBEEP
10mil — GND_POWER
10mil — GND_POWER
10mil — 10mil — AC97_BITCLK
10mil — GND_POWER

10mil — GND_POWER
10mil — 10mil — 14MCLK_AC97
10mil — GND_POWER

A_GND — 10mil
LINE_OUT_L — 10mil
A_GND — 10mil
LINE_OUT_R — 10mil
A_GND — 10mil

INSERT: GROUND
REMOVE: FLOATING

U17 — ASIC AUDIO CODEC ALC268-GR LQFP 48PIN REALTEK LR

(40) HPDET — R308 39.2KΩ 1% 1/10W SMT0603 LR
(40) LINE_IN_JD — R275 10KΩ 1% 1/16W SMT0402 LR
(40) MIC1IN_JD — R276 20KΩ 1% 1/16W SMT0402 LR
SYS_BEEP — SENSE_A

PCBEEP, Sense A, NC, NC, MIC2-L, MIC2-R, CD_L, CD_R, CD_GND, MIC1-L, MIC1-R, LINE1-L, LINE1-R, NC, DMIC_CLK, EAPD, SPDIFO, GPIO0/DMIC-12, GPIO3/DMIC34, SDATA_OUT, BCLK, SYNC, RESET#, DVDD, DVDD_IO, AVDD1, AVDD2

LINE-OUT-L, LINE-OUT-R, MONO_OUT, HP-OUT-L, HP-OUT-R, VREF, MIC1-VREFO-L, LINE1-VREFO, MIC2-VREFO, MIC1-VREFO-R, GPIO1, NC, Sense B, SDATA_IN, JDREF, DVSS_1, DVSS_2, AVSS1, AVSS2, NC

10mil — SPK_OUT_L (39), SPK_OUT_R (39)
10mil — HP_OUT_L (39), HP_OUT_R (39)
C309 0.1uF 16V 80-20% SMT0402 Y5V LR
C313 10uF 6.3V 80-20% SMT0805 Y5V H=1.25mm LR — AUDIO_GND (39,40)
MIC1_VREFO_L (40)
LINE_IN_VREFO_L (40)
MIC_VREFO_R (40)

(40) MIC1_L — MIC1_L
(40) MIC1_R — MIC1_R
(40) LINE_I_L — LINE_I_L
(40) LINE_I_R — LINE_I_R
EAPD
(40) SPDIFO

C311 22pF 50V 5% SMT0402 NPO LR(NU)

(24,30) AZ_SDOUT — R291 0Ω 5% 1/16W SMT0402 LR
(24,30) AZ_BITCLK — R285 22Ω 5% 1/16W SMT0402 LR Sn
(24,30) AZ_SYNC — R282 0Ω 5% 1/16W SMT0402 LR
(24,30) AZ_RST# — R280 0Ω 5% 1/16W SMT0402 LR

R284 22Ω 5% 1/16W SMT0402 LR Sn — AZ_SDIN0 (24)
R310 RES 5.1KΩ 1% 1/16W SMT0402 LR

3VDDM_AUDIO — (20mil)
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
AVDDS — (20mil)
C363 10uF 10V +80-20% SMT0805 Y5V LR
C306 0.1uF 16V 80-20% SMT0402 Y5V LR
Please close to CODEC CHIP
(39,40) AUDIO_GND

HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#

ICH7m — L1 — L2 — 39ohm — L3 — HD Audio — MDC CONN

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.5"~2.5" L2 <= 0.1" L3 = 1"~8"

*** L3 can be extened up to 15" if HD Audio docking is not used

HD Audio-ACZ_SDIN

ICH7m — L1 — 39ohm — L2 — HD Audio

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.1"~15" L2 <= 0.5"

*** Breakout can be routed 4 on 4 up to 50 0 mils

(24) SPKR_SB — R260 22K 5% 1/16W 0402 LR — C300 1uF 10V +80-20% 0603 Y5V LR — SYS_BEEP
R263 47KΩ 5% 1/16W SMT0402 LR
(39,40) AUDIO_GND

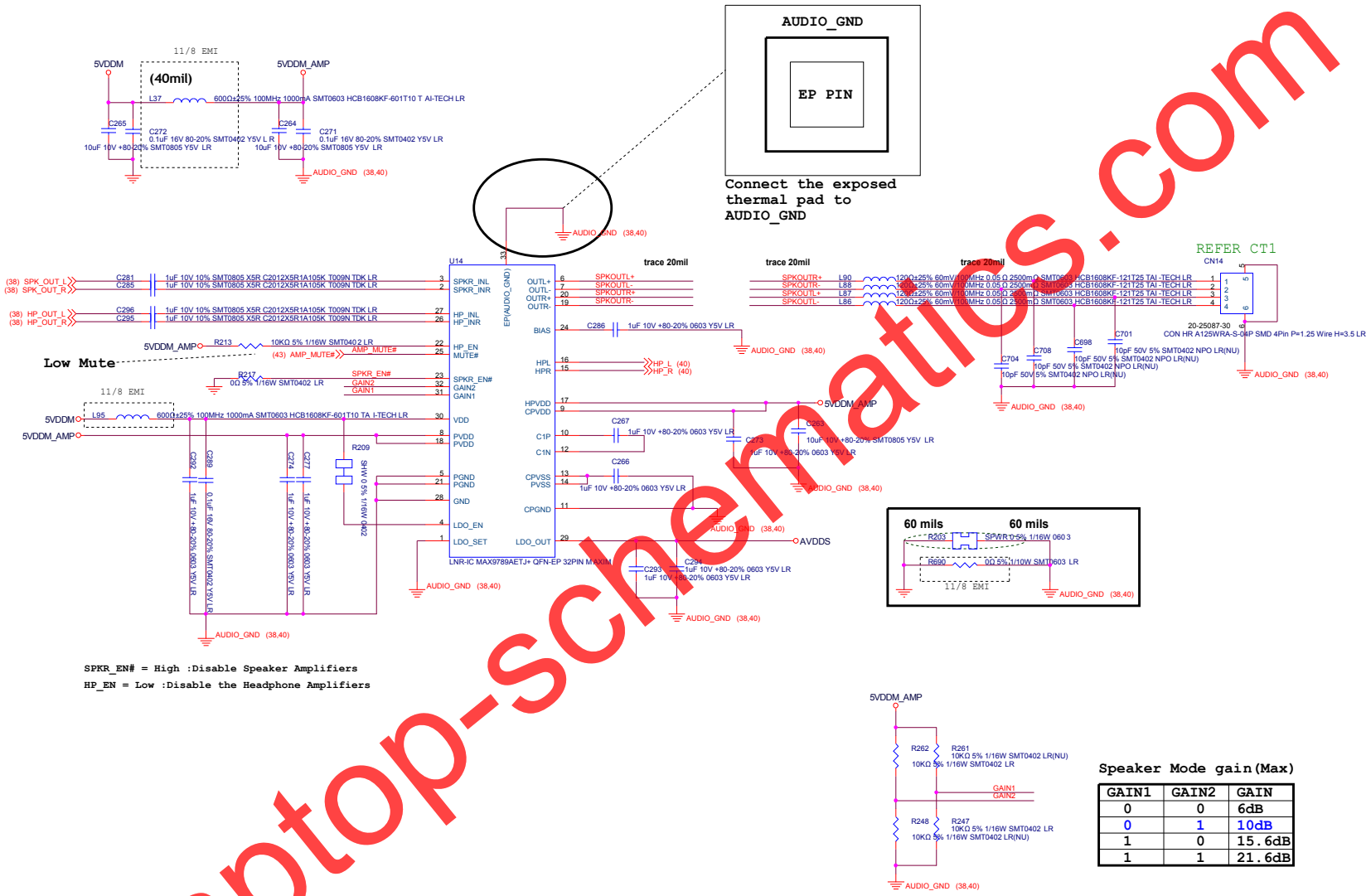
3VDDM — L2 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR — 3VDDM_AUDIO
Please close to CODEC CHIP
20 mils
C356 10uF 10V +80-20% SMT0805 Y5V LR
C350 0.1uF 16V 80-20% SMT0402 Y5V LR

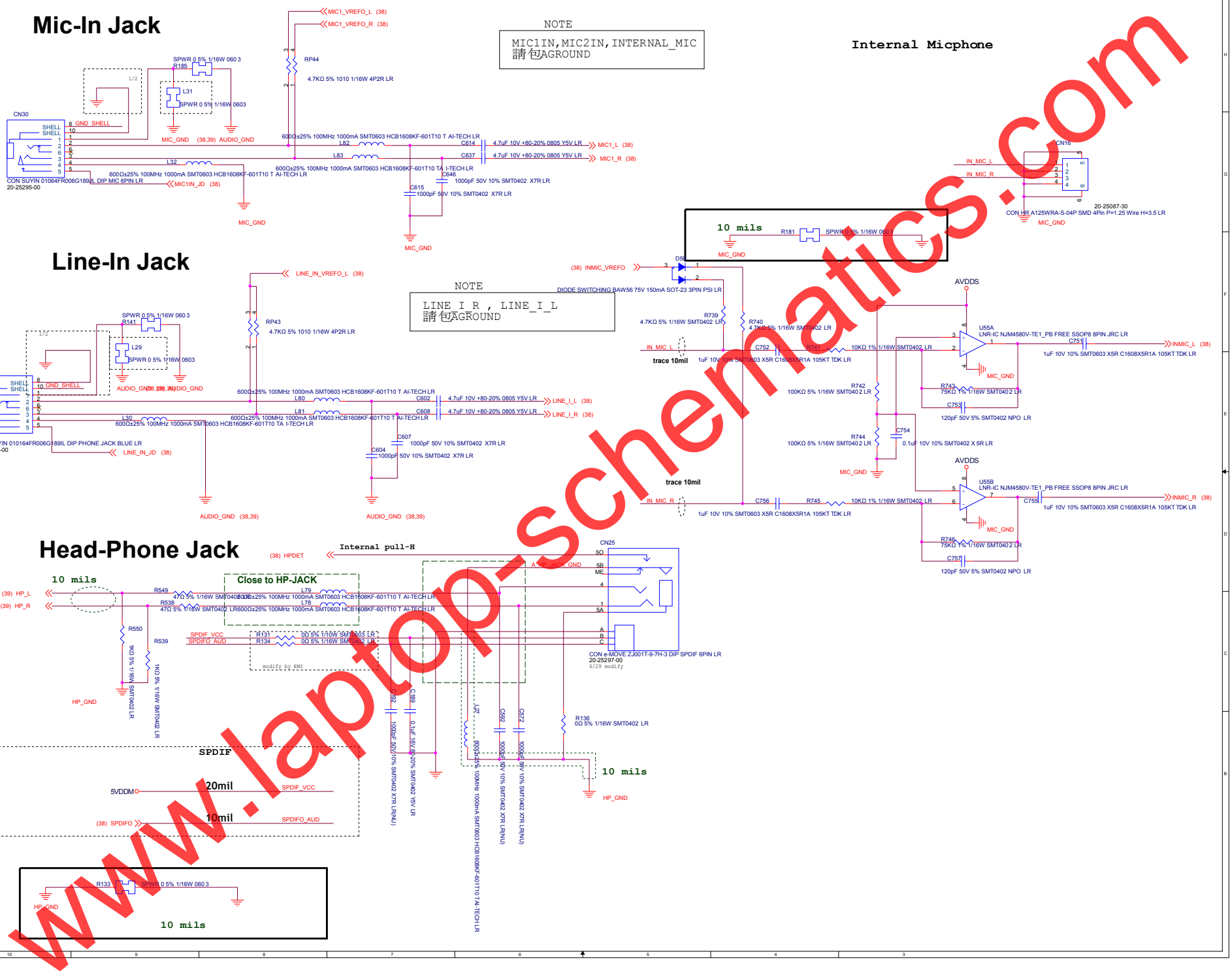
(10,21,24,36,37,39,40,49) 5VDDM — 5VDDM
(10,11,15,16,17,18,20,21,22,23,24,25,26,27,30,32,33,35,36,41,43,45,49,50,51) 3VDDM — 3VDDM
(39,40) AVDDS — AVDDS

AZALIA CODEC POWER

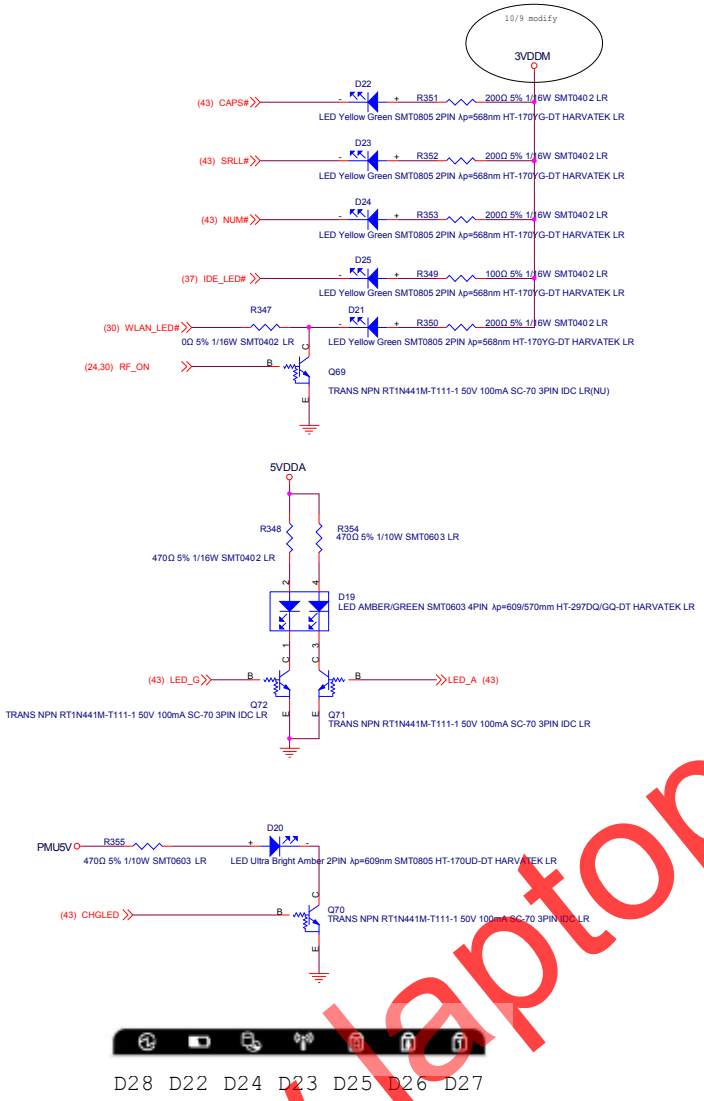
5VDDM — (20mil) — C373 0.1uF 16V 80-20% SMT0402 Y5V LR(NU)
C360 0.1uF 16V 80-20% SMT0402 Y5V LR(NU)
U21 — VIN, BYP, SHDN, GND, VOUT
LNR-IC LDO G924-475T1Uf 4.75V SOT23-5 5PIN GMT LR(NU)
NU_05-31717-01
200mA — (20mil) — AVDDS
C378 10uF 10V +80-20% SMT0805 Y5V LR(NU)
(39,40) AUDIO_GND

Reserve (Power from Maxin IC)

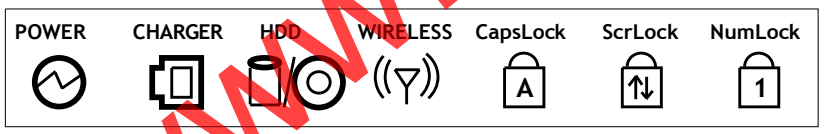



Mic-In Jack
NOTE
MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND
Internal Micphone
Line-In Jack
NOTE
LINE_I_R , LINE_I_L
請包AGROUND
Head-Phone Jack
Internal pull-H
Close to HP-JACK
10 mils
SPDIF
20mil
10mil
trace 10mil
CON SUYIN 01064FR006G189IL DIP MIC 6PIN LR
20-25295-00
CON SUYIN 010164FR006G189IL DIP PHONE JACK BLUE LR
20-25325-00
CON e-MOVE ZJ001T-9-7H-3 DIP SPDIF 6PIN LR
20-25297-00
20-25087-30
CON HR A125WRA-S-04P SMD 4Pin P=1.25 Wire H=3.5 LR
DIODE SWITCHING BAW56 75V 150mA SOT-23 3PIN PSI LR
LNR-IC NJM4580V-TE1_PB FREE SSOP8 8PIN JRC LR
AVDDS
MIC_GND
HP_GND
AUDIO_GND
5VDDM
www.laptop-schematics.com

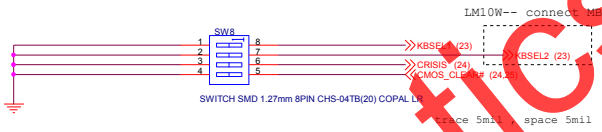
LED indicator control logic



D28 D22 D24 D23 D25 D26 D27

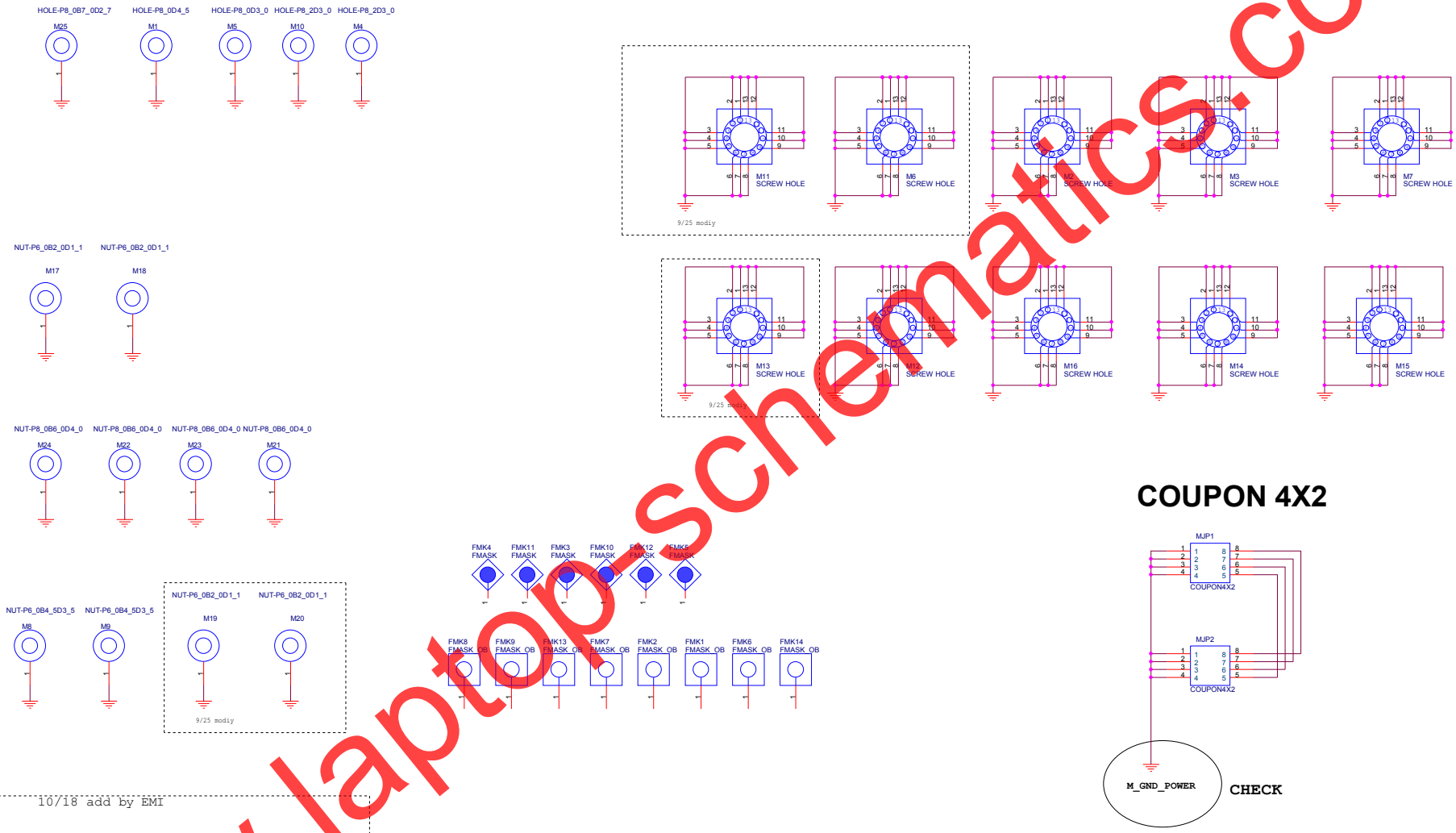


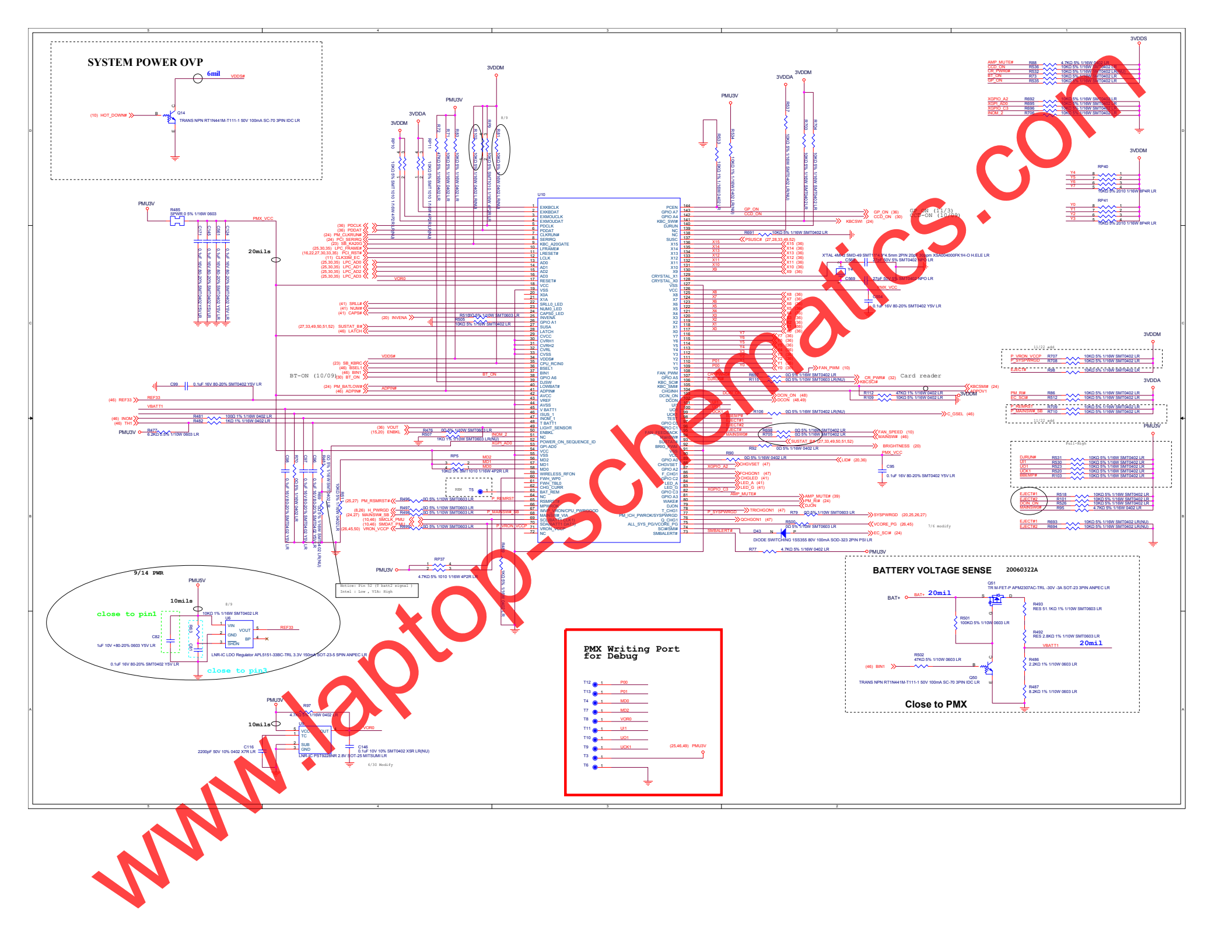
DIP SWITCH



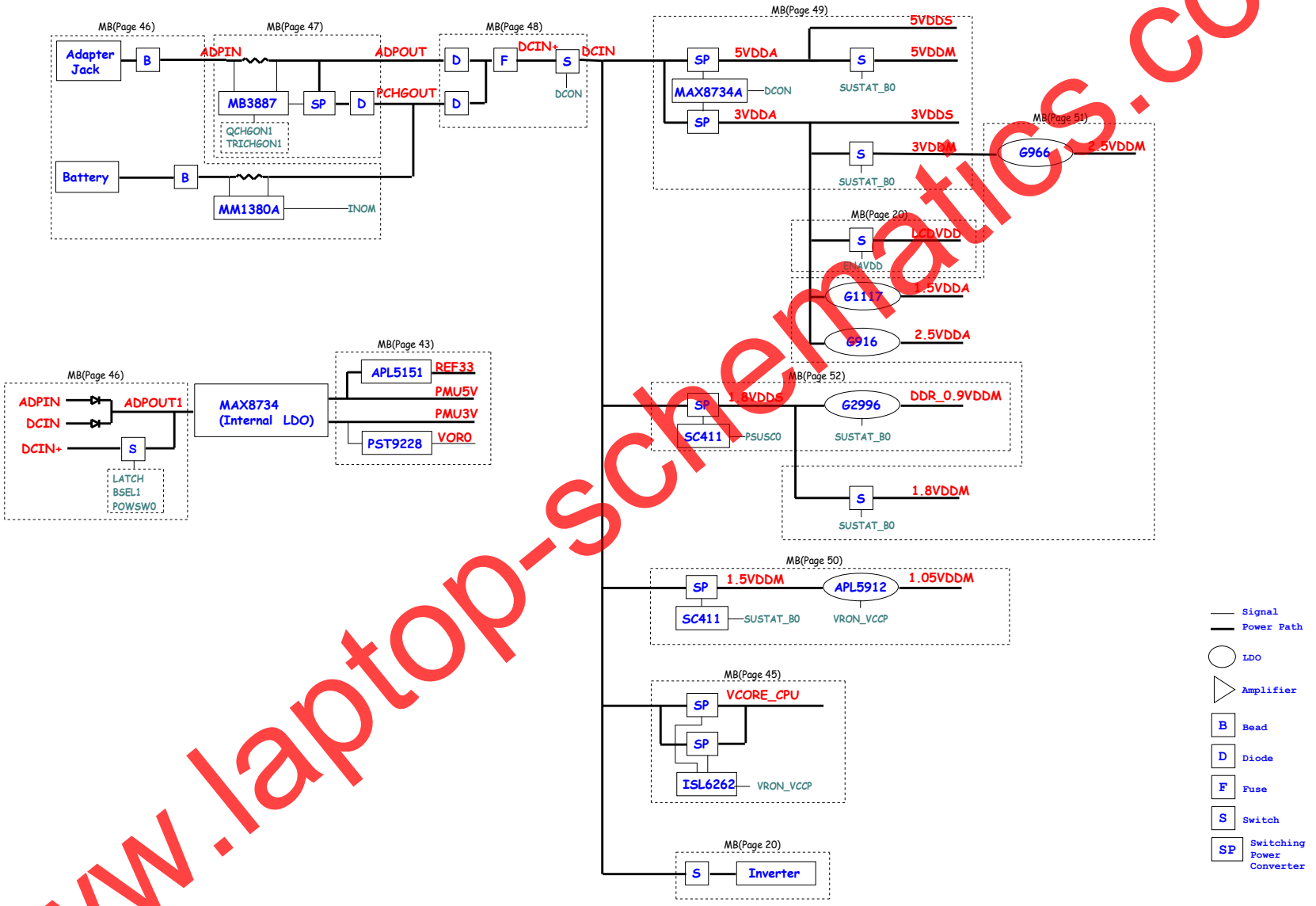
KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

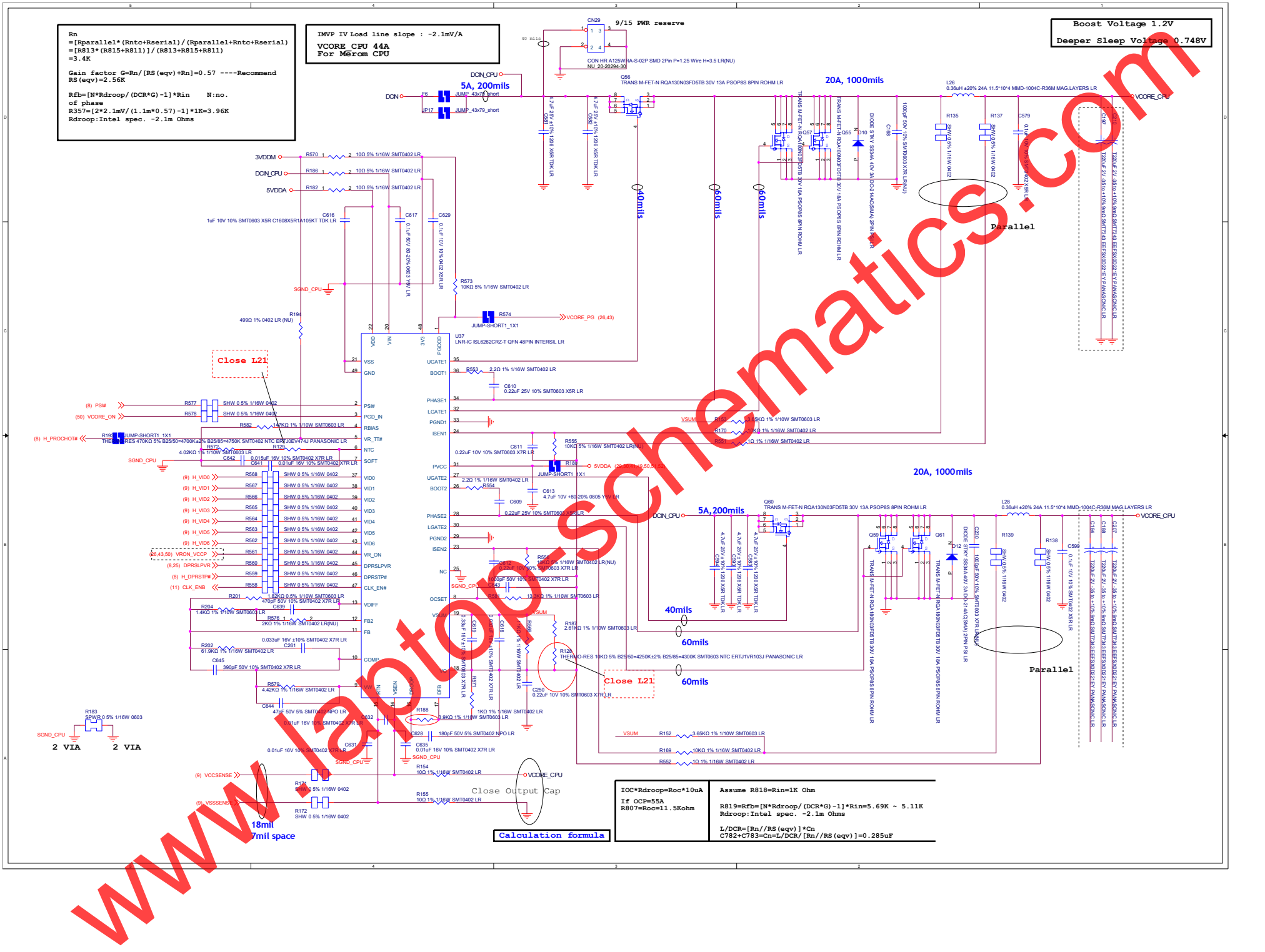
MB_ID0	ON	Reserved
	OFF	Reserved
LCDSEL	ON	Reserved
	OFF	Reserved
PASS0	ON	Override
	OFF	Available
DVDSEL	ON	CD-ROM
	OFF	DVD
CMOS_CLEAR	ON	Reset RTC
	OFF	NONE



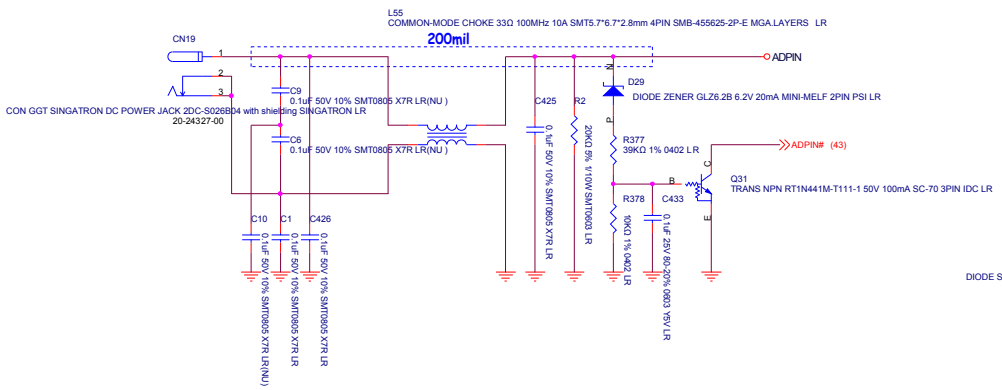

SYSTEM POWER OVP
BATTERY VOLTAGE SENSE
20060322A
PMX Writing Port for Debug
Close to PMX
9/14 PWR
U10
PMU3V
3VDDM
3VDDA
3VDDS
VDDS#
REF33
VBATT1
BT-ON (10/09)
Card reader
www.laptop-schematics.com

Power Block

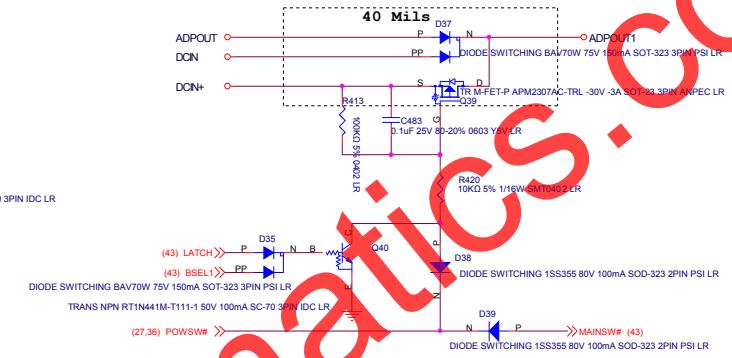




ACIN

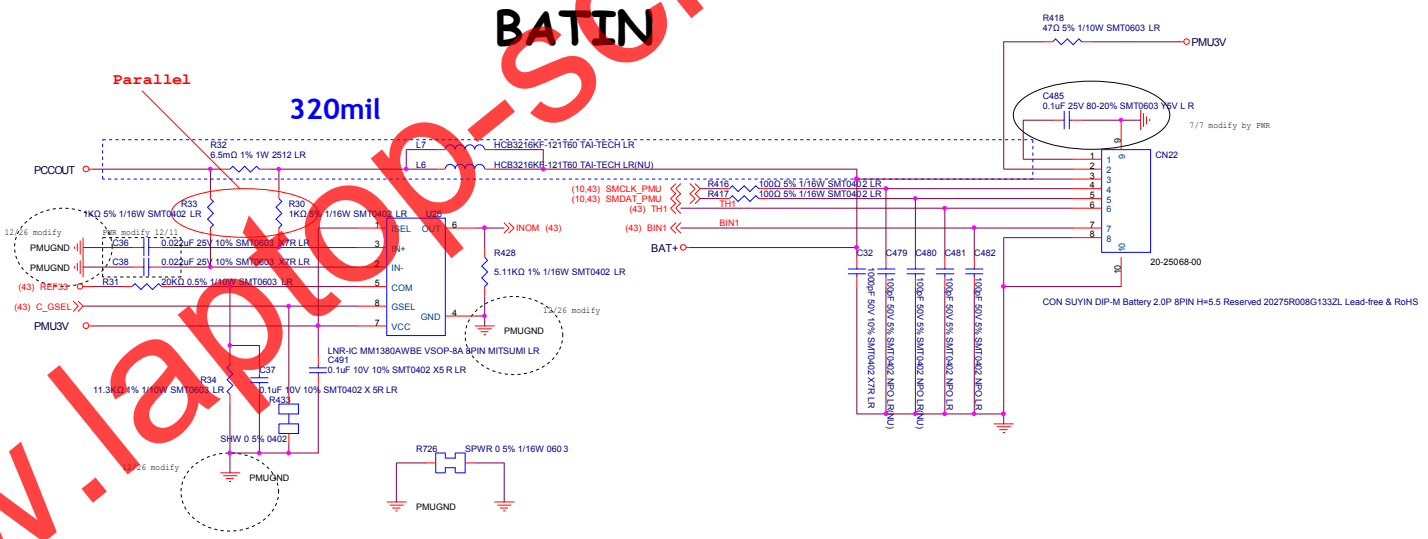


ADPOUT1, MAINSW#

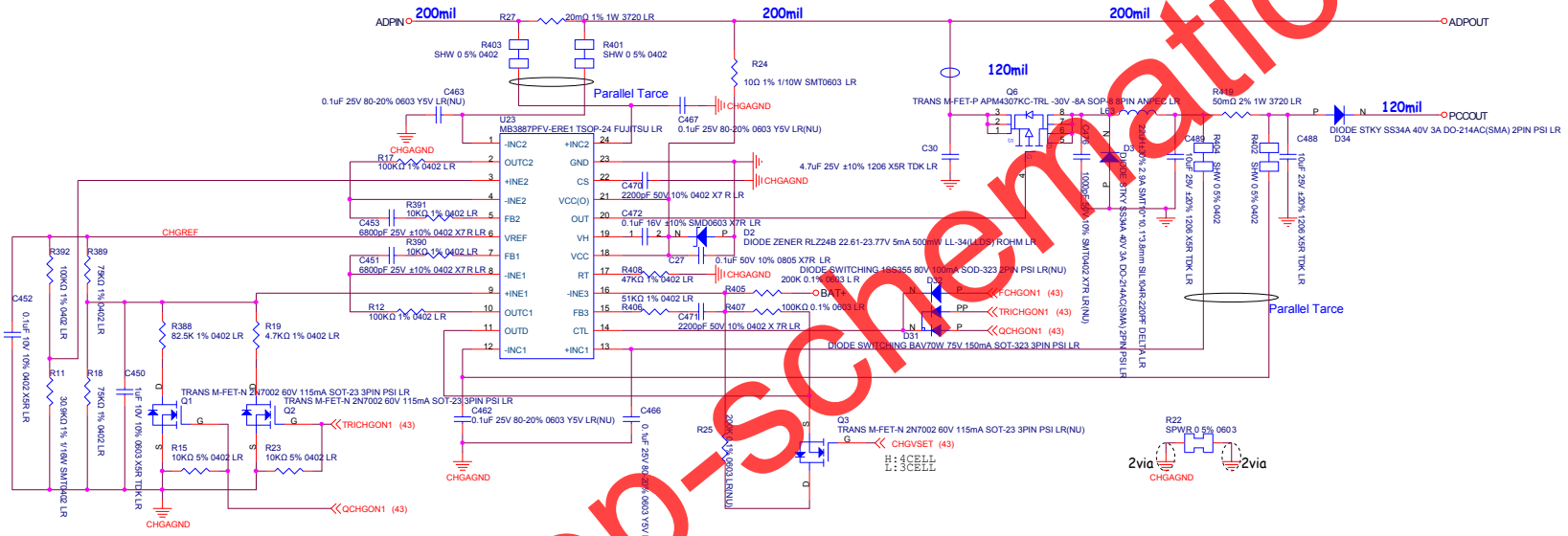


All Trace > 12mils

BATIN

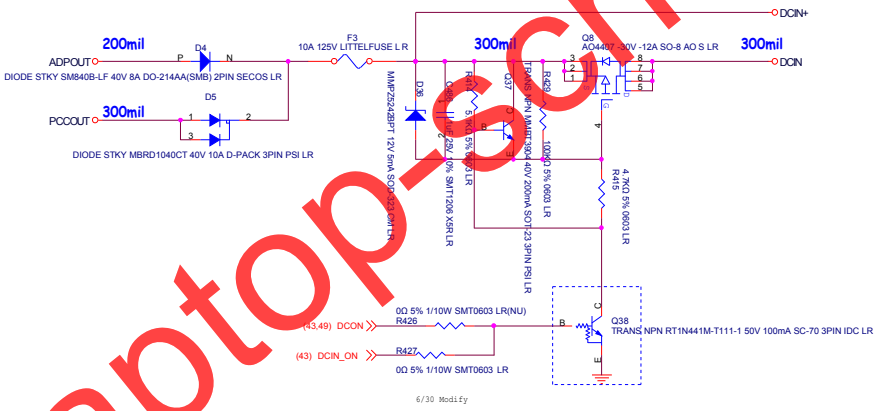


Charger

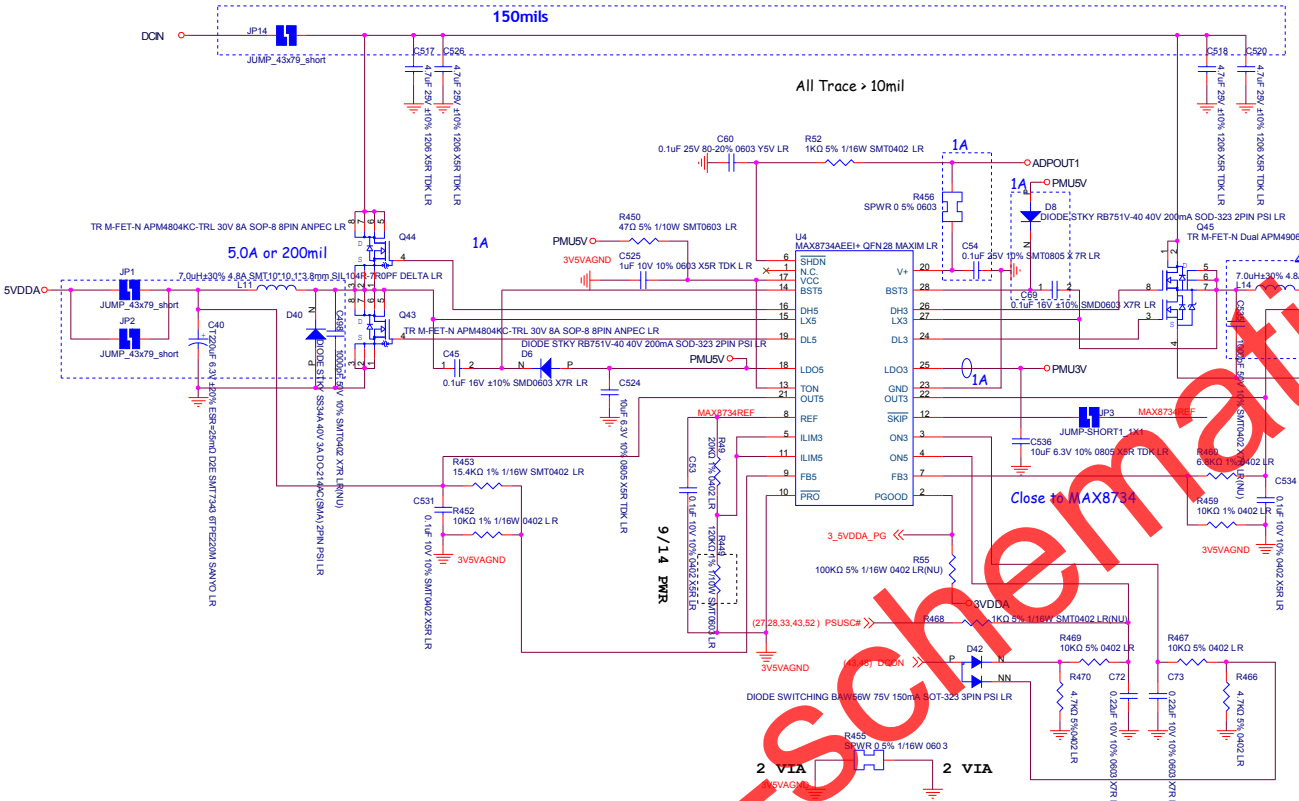


FCHG = 2.5A
QCHG = 1.71A
TCHG = 0.278A

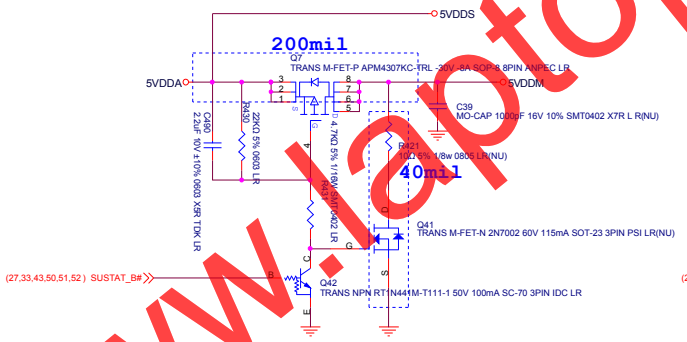
DCIN



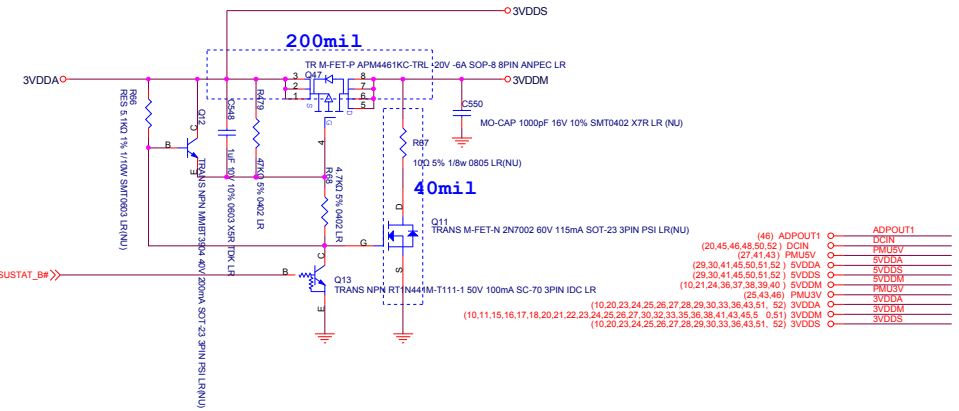
5VDDA/S/M, 3VDDA/S/M



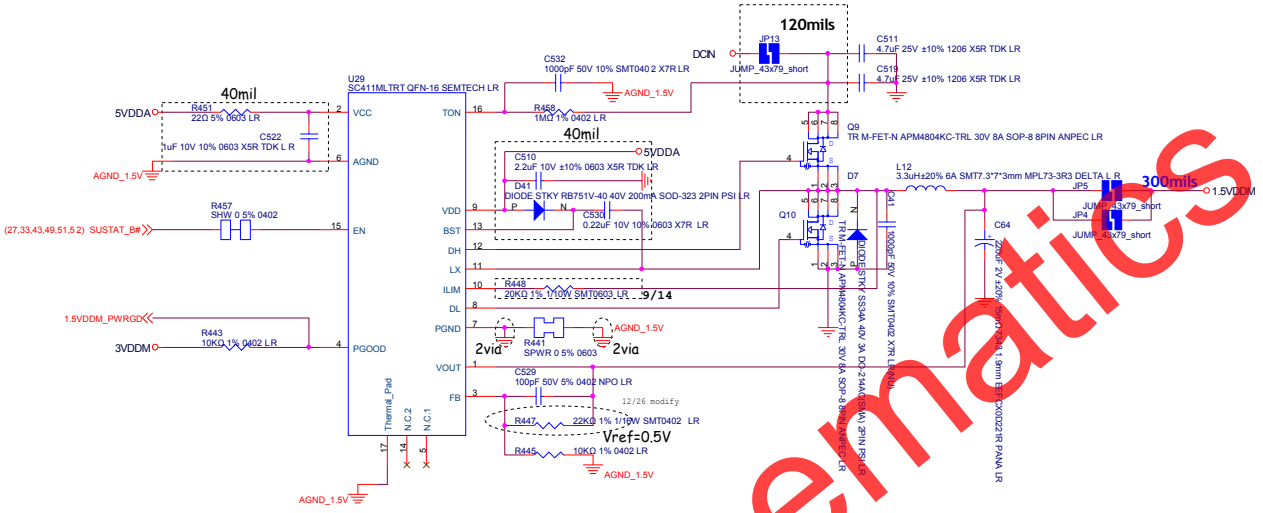
5VDDS/5VDDM



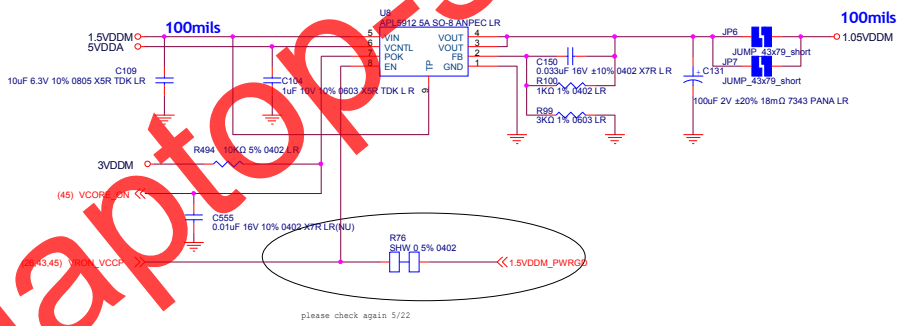
3VDDS/3VDDM



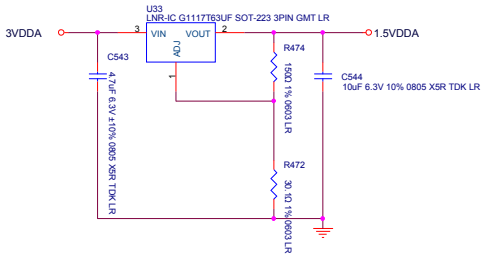
1.5VDDM



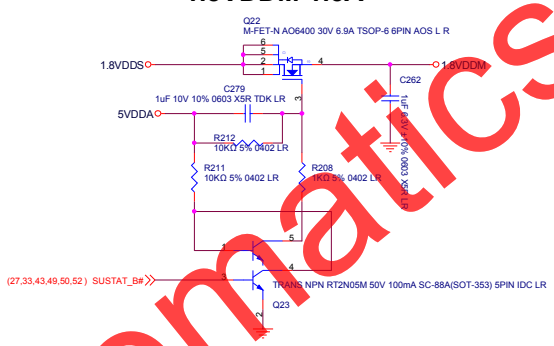
VCCP



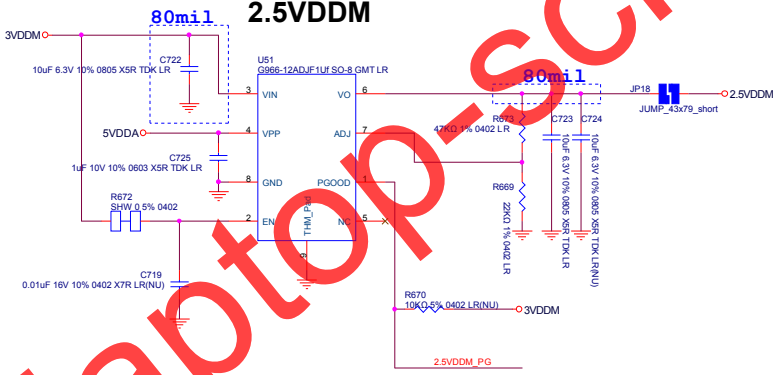
1.5VDDA 0.5A



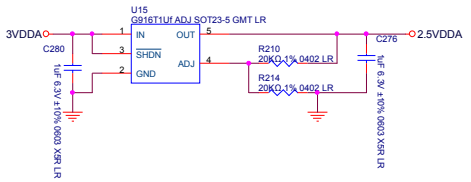
1.8VDDM 1.5A



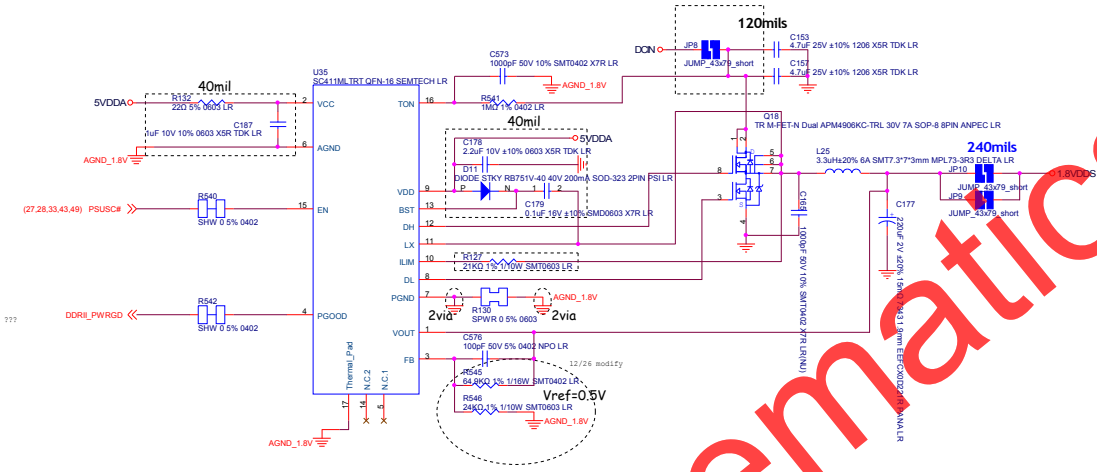
2.5VDDM



2.5VDDA 0.5A



1.8VDDS



0.9VDDM