QSFP+ 40 Gbs 4X Pluggable Transceiver

Introduction

This design guide provides the information needed to incorporate OptixCom's fiber optics products in the customer's system. The QSFP+ series of transceiver products are designed to integrate four data lanes each of which operating at 10 Gb/s for an aggregated 40 Gb/s bandwidth. The optical interface uses a parallel 12-fiber MTP (MPO) connector. The QSFP+ series of the transceiver products are compliant with the QSFP+ mutli-source agreement. For more detail information, please refer to the URL ftp://ftp.seagate.com/sff/INF-8438.PDF or visit OptixCom web site: http://www.OptixCom.com for the official documentation.

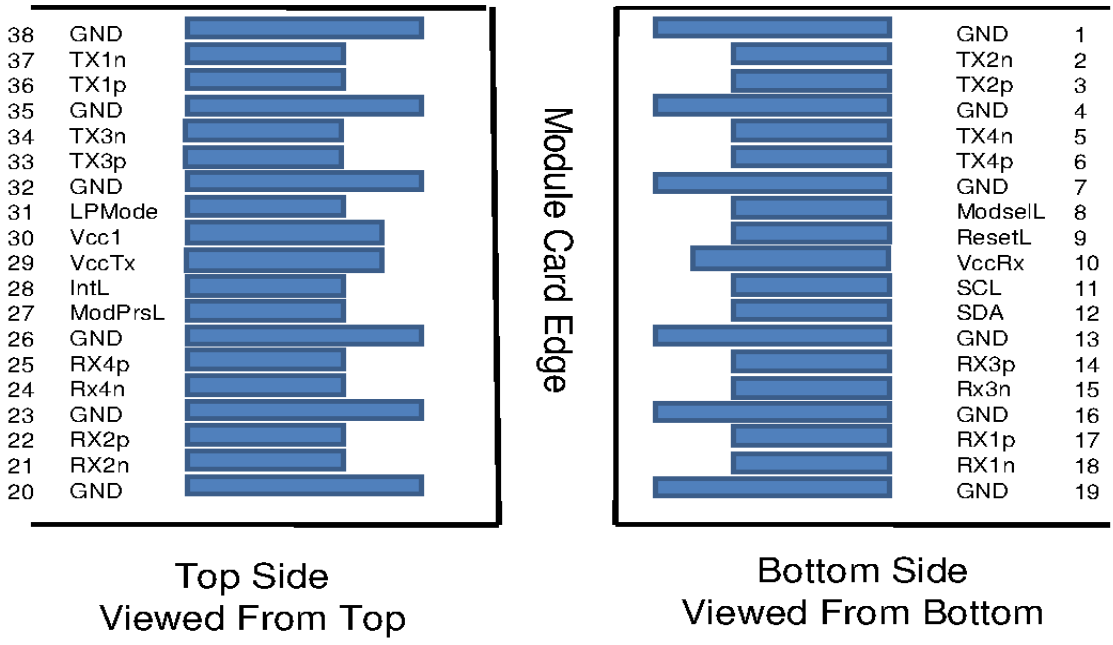
The reference guide covers the following topics:

A.Pin Assignment & Description
B.Package Outline
C.Host Board Design and Mechanical Layout
D.Connector Insertion, Extraction, and Retention Force
E.Connector Interface
F.Timing Requirements of Control and Status I/O
H. Module Definition Interface and Data Field Description

A. Pin Assignment & Description

The diagram shows the module PCB edge from the top and bottom view. The connector pads on the PCB of the transceiver are designed for a sequenced mating.

· First mate ground contacts · Second mate power contacts · Third mate signal contacts



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Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPraL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	3.3V Power Supply Transmitter	2	2
30		Vcc1	3.3 Power Supply	2	2

31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	1
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	1
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

Notes 1:

GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Notes 2:

Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Section E. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

ModSelL
ResetL
LPMode
ModPrsL
IntL

ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode

The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).

The module has two modes a low power mode and a high power mode. The high power mode operates in one of the four power classes.

When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

The modules 2-wire serial interface and all laser safety functions must be fully operational in this low power mode. The module shall still support the completion of reset interrupt in this low power mode.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate a power consumption greater than 1.5W and the module is in low power mode it must reduce its power consumption to less than 1.5W while still maintaining the functionality above. The exact method of accomplishing low power is not specified, however it is likely that either the Tx or Rx or both will not be operational in this state.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that its power consumption is less than 1.5W then the module shall be fully functional independent of whether it is in low power or high power mode.

The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_ override bit is in the high state and the Power_set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power_override bit is high and the Power set bit is low. Note that the default state for the Power_override bit is low. A truth table for the relevant configurations of the LPMode and the Power_over-ride and Power_set are shown in the following Table. At Power up, the Power_override and Power_set bits shall be set to 0.

Power Mode Truth Table

LPMode	Power_Override Bit	Power_Set Bit	Module Power Allowed
1	0	X	Low Power
0	0	X	High Power
X	1	1	Low Power
X	1	0	High Power

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready)is read with a value of '0' and the flag field is read.

Low Speed Electrical Specification

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

The QSFP+ low speed electrical specifications are given in the following Table. This specification ensures compatibility between host bus masters and the 2-wire interface.

Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max(= 3.0mA
	VOH	Vcc -0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total Bus Capacitive Load For SCL and SDA	Cb		100	pF	3.0k Ohms Pullup resistor, max
			200	pF	1.6k Ohms Pullup resistor, max
LPMode, Reset and ModSelL	VIL	-0.3	0.8	V	I Iin I <= 125 uA for 0V V Vin, Vcc
	VIH	2	VCC + 0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL = 2.0mA
	VOH	VCC -0.5	VCC + 0.3	V	

High Speed Electrical Specification

Rx(n)(p/n)

Rx(n)(p/n) are QSFP+ module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP+ module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 1600 mVpp or the relevant standard, whichever is less.

Note: Due to the possibility of insertion of QSFP+ modules into a host designed for QSFP+, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output
impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function.

Tx(n)(p/n)

Tx(n)(p/n) are QSFP+ module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP+ module. The AC coupling is inside the QSFP+ module and not required on the Host board. For operation at 6Gbps and below the inputs will accept single-ended voltage swings between 250 mV to 800 mV and differential voltage swings between 500 mVpp to 1600 mVpp. For best EMI results, single-ended swings between 250 mV and 600 mV and differential voltage swings between 500 mVpp to 1200 mVpp are recommended. For operation above 6Gbps see the appropriate specification, e.g. 802.3ba Annex 86A, FC-PI-4, FC-PI-5 or the InfiniBand specification. For 10G Ethernet reference SFF-8431.

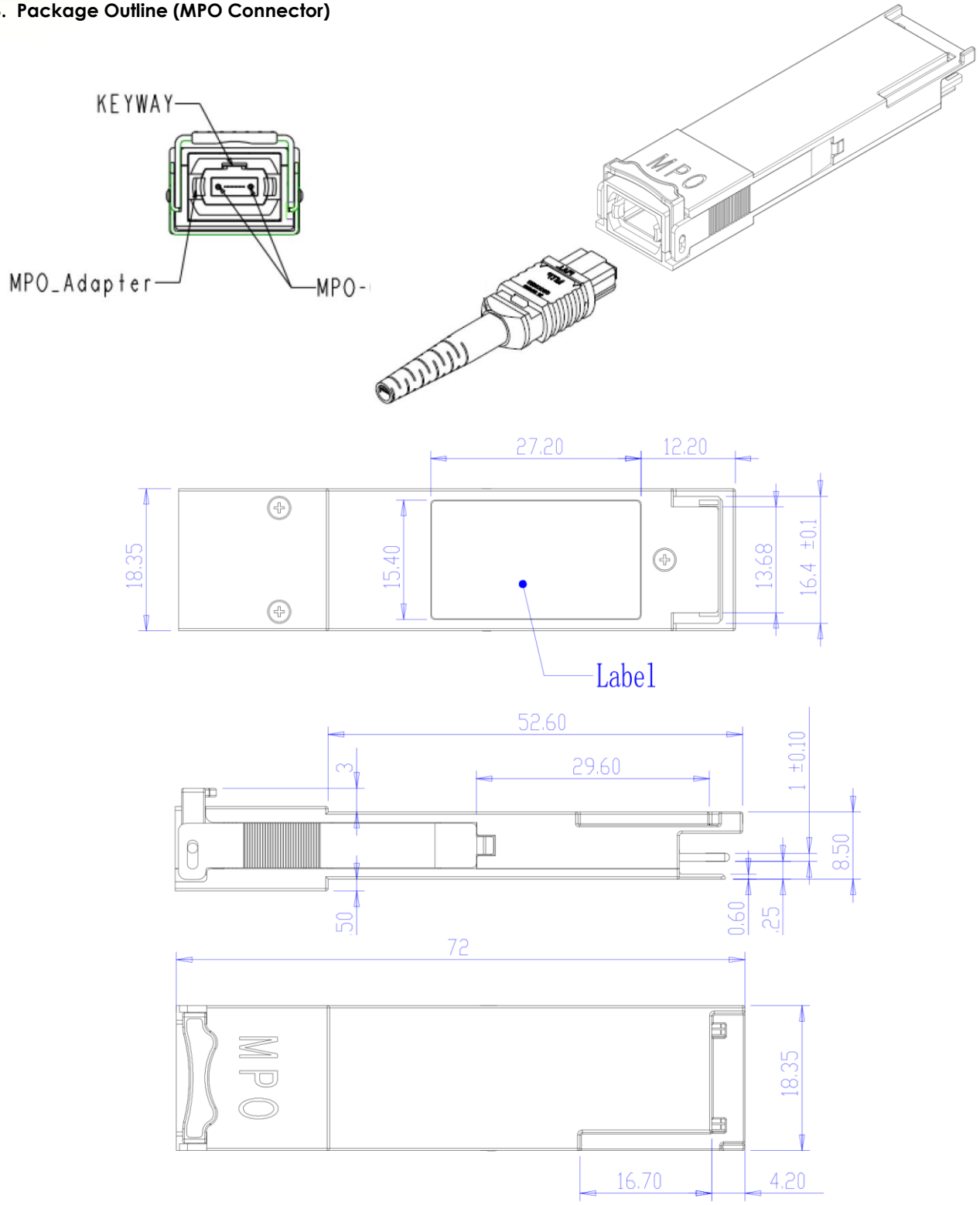
Due to the possibility of insertion of QSFP+ modules into a host designed for QSFP interface per INF-8438i the damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set.

Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

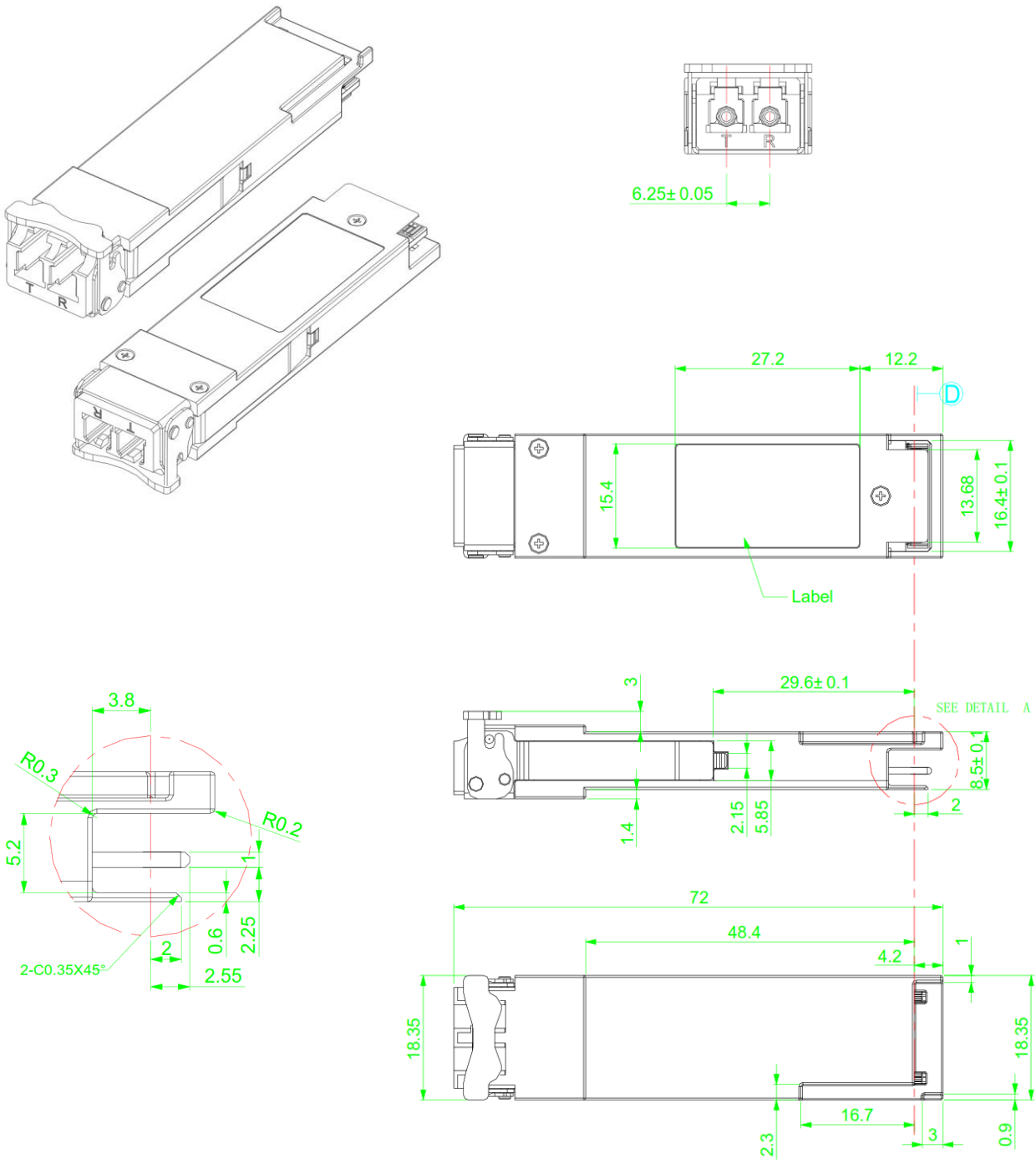
In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function.

B. Package Outline (MPO Connector)



Unit: mm, typical tolerance for these dimensions is ± 0.2 mm

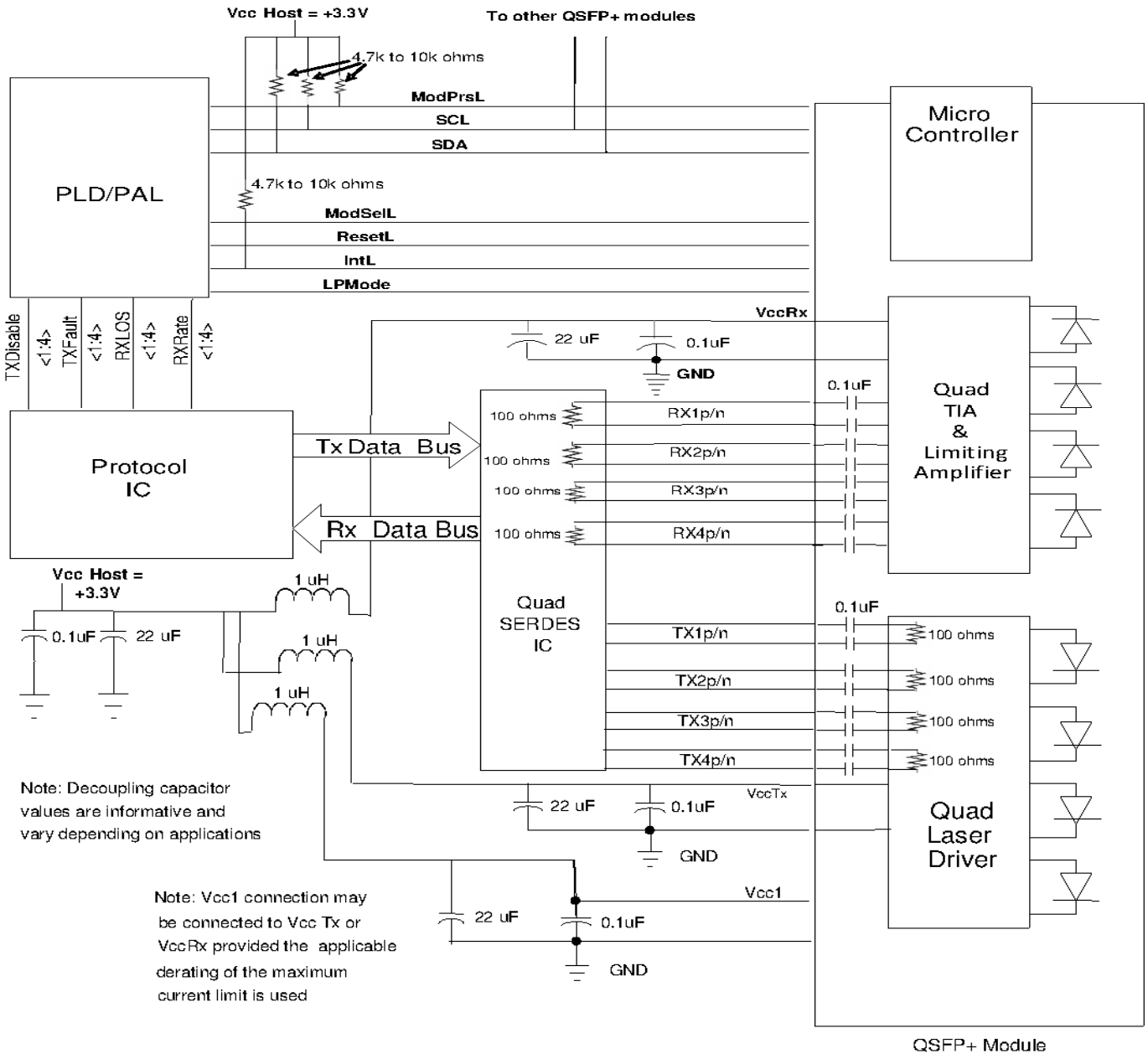
Package Outline (LC Connector)



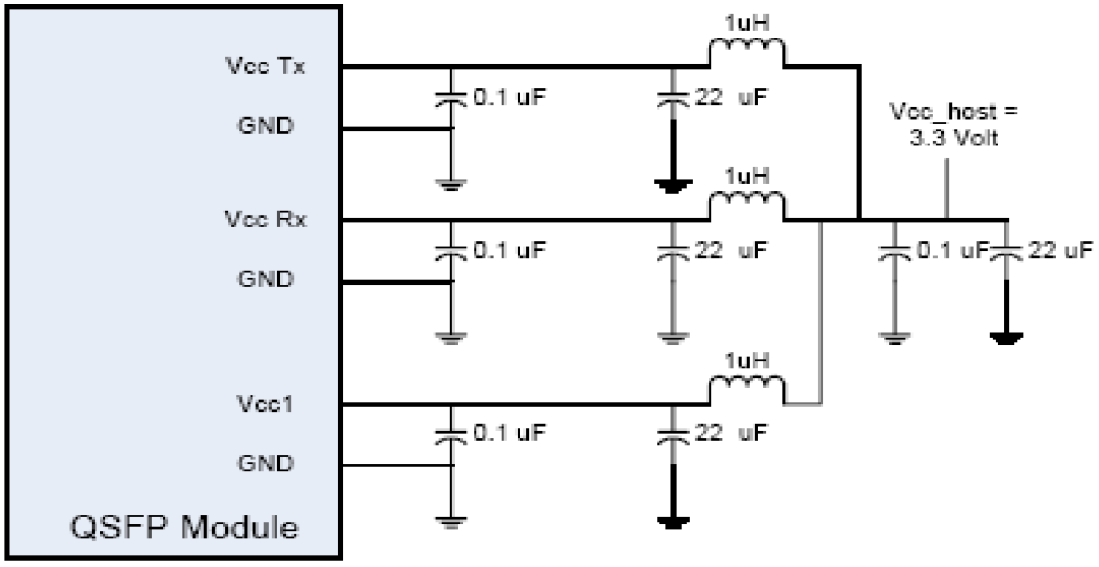
Unit: mm, typical tolerance for these dimensions is ± 0.2 mm

C. Host Board Design and Mechanical Layout

Example Host Board Schematic



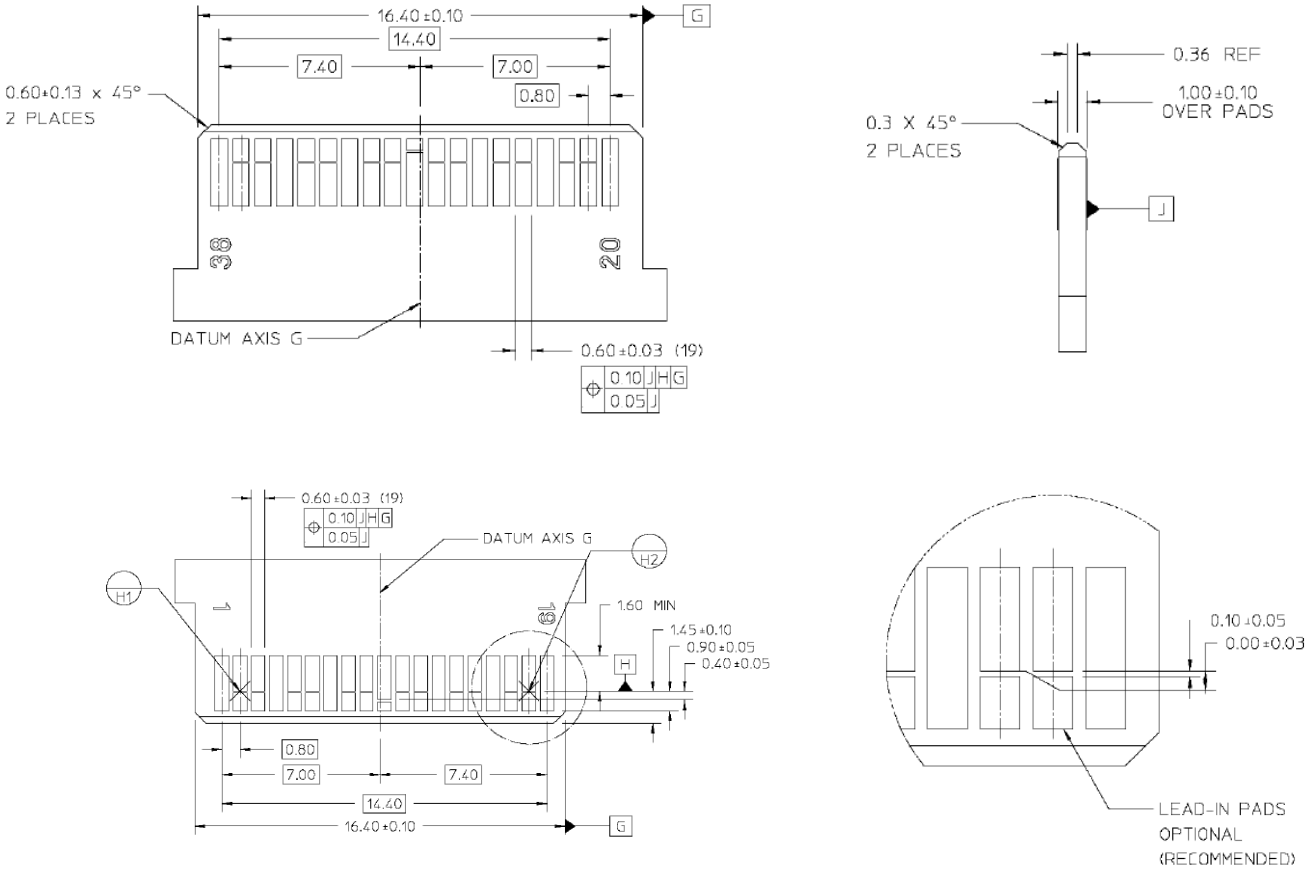
Recommended Host Board Power Supply Filtering



Power Supply Specification

Parameter	Min	Nominal	Max	Unit	Condition
Vcc	---	3.3		V	Measured at Vcc Tx, Vcc Rx and Vcc1.
Vcc Set Point Accuracy	-5	---	5	%	Measured at Vcc Tx, Vcc Rx and Vcc1.
Power Supply Noise Including Ripple	---	---	50	mV	1kHz to frequency of operation measured at Vcc host.
Sustained Peak Current at hot plug with LPMode Pin asserted	---	---	495	mA	
Maximum instantaneous Current with LPMode asserted	---	---	600	mA	
Module sustained Peak Current with LPMode Pin deasserted	---	---	750	mA	
Maximum instantaneous current with LPMode deasserted	---	---	900	mA	

Pattern Layout for QSFP+ Printed Circuit Board

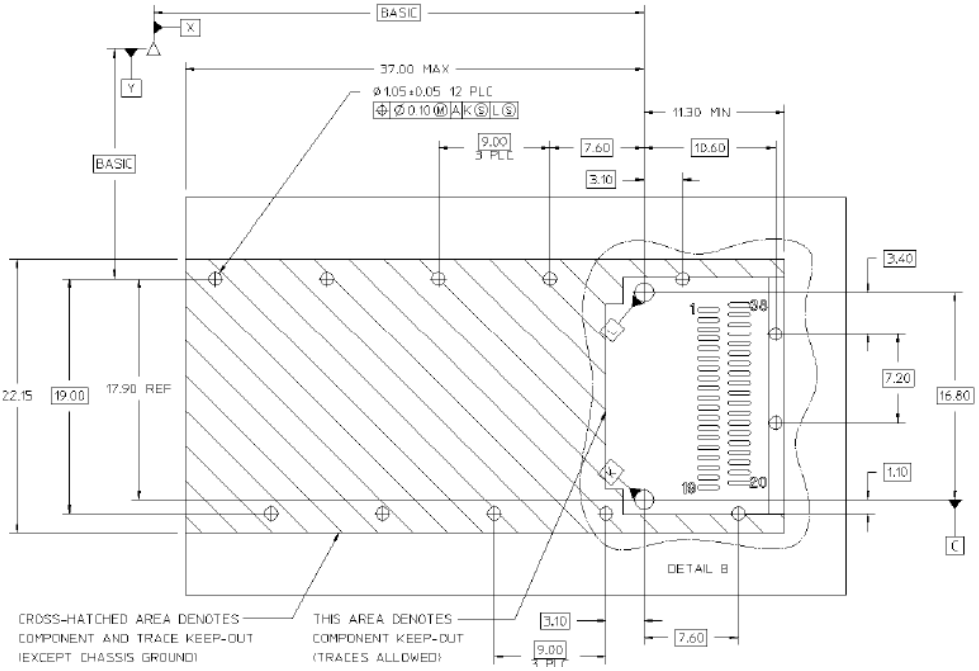


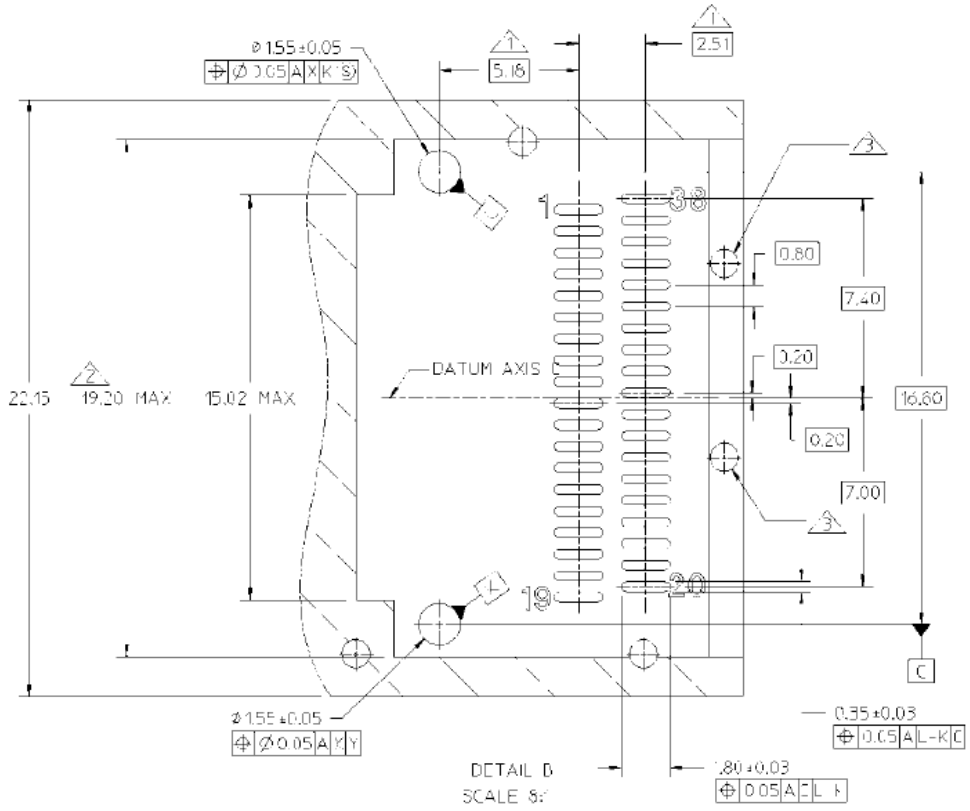
Notes:

1. Contact Pad Plating
   - 0.38 Micrometers Min Gold Over
   - 1.27 Micrometers Min Nickel
2. No Solder Mask Within 0.05 mm of Defined Pad Location
3. Alternate Contact Pad Plating
   - 0.03 Micrometers Min Gold Over
   - 0.30 Micrometers Min Palladium Over
   - 1.27 Micrometers Min Nickel

Datum H Targets are defined by the respective pad centerlines and the leading edge of the Target Pads.

QSFP+ Host PCB Mechanical Layout



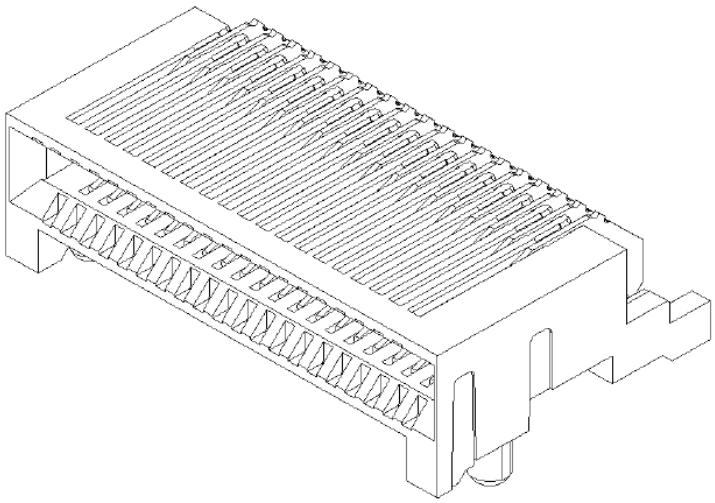


D. Connector Insertion, Extraction, and Retention Force

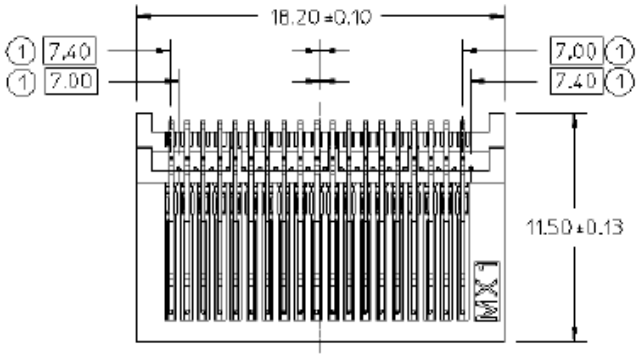
Measurement	Min	Max	Units	Comments
QSFP+ Module Insertion	0	40	N	
QSFP+ Module Extraction	0	30	N	
QSFP+ Module Retention	90	N/A	N	No damage to module below 90N
Cage Retention (Latch Strength)	180	N/A	N	No damage to module below 180N
Cage Retention in Host Board	114	N/A	N	Force to be applied in a vertical direction, no damage to cage.
Insertion / Removal Cycles , Connector / Cage	100	N/A	Cyc.	Number of cycles for the connector and cage with multiple modules.
Insertion / Removal Cycles, QSFP+ Module	50	N/A	Cyc.	Number of cycles for an individual module.

E. Connector Interface

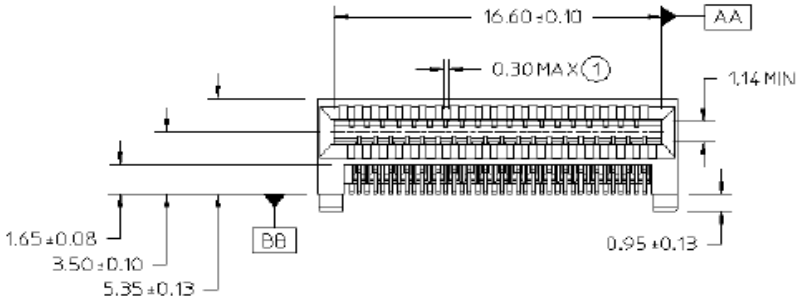
Electrical Connector Illustration

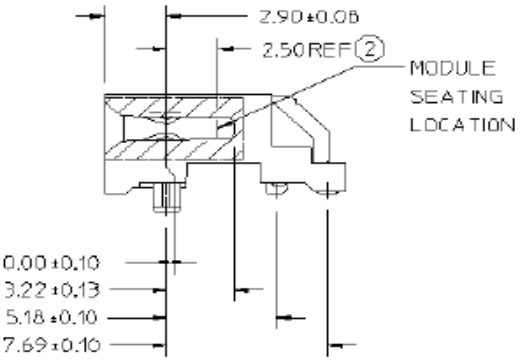


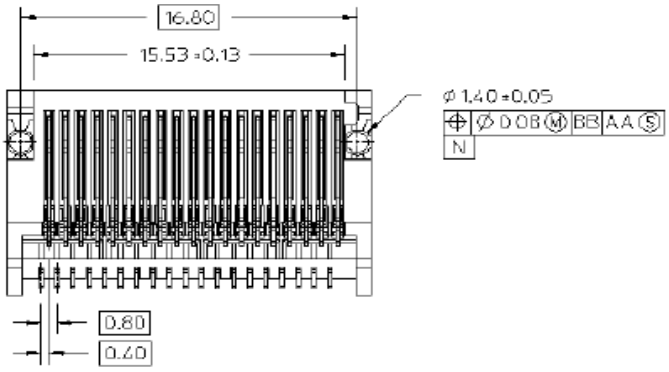
Electrical Connector Specification



1. Contact must be within 0.30 wide tolerance zone. The centerline of the tolerance zone is defined by the indicated basic dimensions relative to datum 'AA' regardless of feature size.
2. Paddle card not to bottom against receptacle card slot.

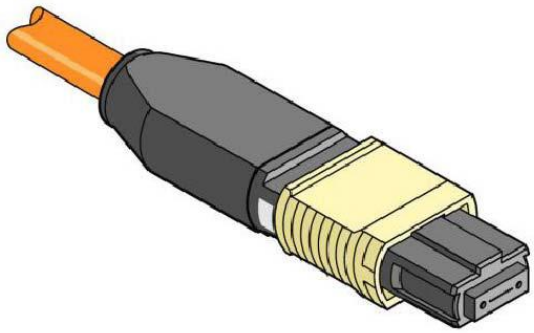


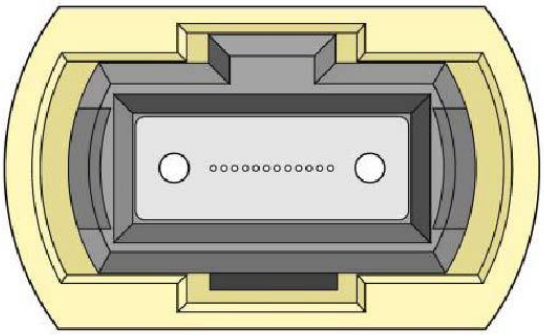


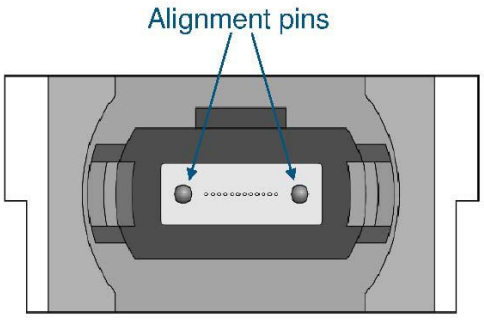


MPO Optical Cable connection

Aligned key (Type B) MPO patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is defined in TIA-568. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.







Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

F. Timing Requirements of Control and Status I/O

Timing Specification

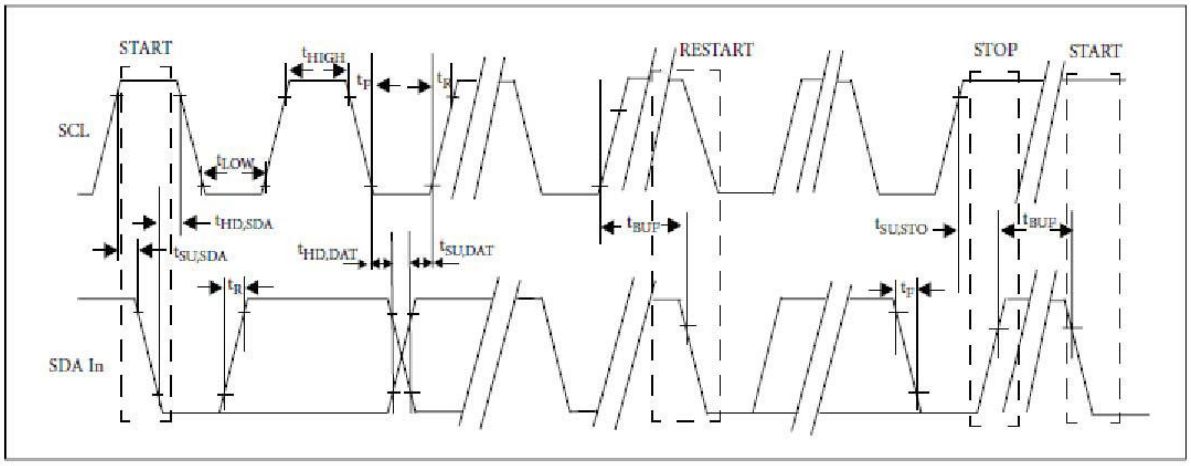
- Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to a Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Nomenclature for all registers more than 1 bit long is MSB-LSB.

- Management Interface Timing Specification

In order to support a multi-channel device a higher clock rate for the serial interface is considered. The timing requirements are shown below. QSFP+ is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs.

QSFP+ Timing Diagram



Before initiating a 2-wire serial bus communication, the host shall provide setup time (Host_select_setup) on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement (Host_select_hold) is satisfied. The 2-wire serial interface address of the QSFP+ module is 1010000X (A0h). In order to allow access to multiple QSFP+ modules on the same 2-wire serial bus, the QSFP+ pinout includes a ModSelL or module select pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

- Serial Interface Protocol

The module asserts LOW for clock stretch on SCL.

- Timing for Soft Control and Status Functions

Timing for QSFP+ soft control and status functions are described in the following Table.

Management Interface timing parameters

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	---
Clock Pulse Width Low	tLOW	1.3	---	µs	---
Clock Pulse Width High	tHIGH	0.6	---	µs	---
Time bus free before new transmission can start	tBUF	20	---	µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6	---	µs	---
START Set-up Time	tSU.STA	0.6	---	µs	---
Data In Hold Time	tHD.DAT	0	---	µs	---
Data in Set-up Time	tSU.DAT	0.1	---	µs	---
Input Rise Time (400kHz)	tR.400	---	300	ns	From (VIL,MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400kHz)	tF.400	---	300	ns	From (VIH,MIN + 0.15) to (VIL,MAX – 0.15)
STOP Set-up Time	tSU.STO	0.6	---	µs	---
ModSelL Setup Time	Host_select_setup	2	---	ms	Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time	Host_select_hold	10	---	µs	Delay from completion of a serial bus sequence to changes of Module select status
Aborted sequence – bus release	Deselect _Abort	2	---	ms	Delay from a host deasserting ModSelL (at any point in a bus sequence) to the QSFP+ Module releasing SCL and SDA

Timing for QSFP+ Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_int	2000	ms	Time from power on[2] , hot plug or rising edge of reset until the module is fully functional[3]. This time does not apply to non-Power level 0 modules in Low Power State.
Reset Init Assert Time	t_reset_unit	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[2] until module responds to data transmission over the 2-wire serial bus.
Monitor Data Ready Time	t_data	2000	ms	Time from power on[2] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted.
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[3].
LPMode Assert Time	ton_LPMode	100	µs	Time for assertion of LPMode (Vin: LPMode=Vih)until module power consumption reaches Power Level 1.
LPMode Deassert Time	toff_LPMode	300	ms	Time for deassertion of LPMode (Vin: LPMode=Vil) until module is fully functional[3,5]
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL	500	µs	Time from clear on read[4] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value=0b)[1] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel	100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification

Parameter	Symbol	Max	Unit	Conditions
Power _Override or Power_Set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value = 1b)[1] until module power consumption reaches Power Level 1
Power_Override or Power_Set Assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared (value = 0b)[1] until the module is fully functional[3]

Note 1. Measured from falling clock edge after stop bit of write transaction.

Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table of page 9.

Note 3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications.

Note 4. Measured from falling clock edge after stop bit of read transaction.

Note 5. Does not apply to power level 1 modules.

I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	80	µs	Time from loss of Rx input signal until the squelched output condition is reached.
Rx Squelch Deassert Time	toff_Rxsq	80	µs	Time from resumption of Rx input signals until normal Rx output condition is reached.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached.
Tx Disable Assert Time	ton_txdis	100	ms	Time from Tx Disable bit set (value =1b)[1] until optical output falls below 10% of nominal.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal.
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Note 1: Measured from falling clock edge after stop bit of write transaction.