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Quality Requirements on Microcircuits

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1 Scope

1.1 Application

This specification 105 63-RYT Uen relates to both assembled and unassembled microcircuits (also known as bare dies) for use in Ericsson manufactured equipment. The object of this specification is to prescribe requirements on the design, manufacturing and quality control of microcircuits to be used at Request for Quotation as a part of the component specification as well as a base for technical audits of the supplier. It is also used as the baseline when compiling qualification plans for application specific components developed for Ericsson.

Microcircuits delivered to Ericsson or external certified Electronic Manufacturing Services (EMS) must fulfill the requirements stated in this specification and in the document, General Quality Requirements on Components 105 63-2031 Uen that is referred to in the Specific Purchase Agreement, SPA and should be read in parallel.

By Ericsson is meant any part of Ericsson Worldwide or external certified Electronic Manufacturing Services (EMS) organization making use of this specification as reference for technical issues and purchasing of microcircuits.

1.1.1 Procurement

This document is used as a part of the product specification for microcircuits. The latest revision of 105 63-RYT Uen is always valid. The latest revision is available through the respective purchasing departments, technical services or Electronic Data Interchange (EDI).

2 Requirements on design

2.1 Design for reliability

2.1.1 Current density stress

The Manufacturer is obliged to have documented the applicable design rules for the internal conductors (metallization stripes, contact areas, bonding interfaces etc.).

2.1.2 Thin oxide voltage stress

The circuit must be designed so the expected field strength over the oxide does not cause time dependent dielectric breakdown.

2.1.3 Power cycling

Power variation due to traffic load changes is a main consideration for mobile communication equipment. Efforts must be put into avoiding thermal fatigue failures arising from the temperature cycling due to power dissipation in the die.

The Manufacturer must also avoid thermal cycling fatigue of bond system, bond wires and flip chip joints by proper design, taking into consideration the maximum current that will pass through the connections during normal operating conditions.

Components in packages with low capability to take care of stresses generated on parts mounted to a board (e.g. WLP) should be soldered to the test board at power cycling tests.

2.1.4 Soft error rate

Microcircuits must be designed and assembled in such a manner that the soft error rate is minimized at system level. The total soft error rate at normal supply voltage shall be less than 2000 FIT at sea level if nothing else is agreed upon. The level can be verified by system tests, accelerated testing or theoretical calculation.

2.1.5 Hot carrier effects

Microcircuits must be designed so the degradation due to hot carrier effects during its lifetime is minimized.

2.1.6 Negative Bias Temperature Instability, NBTI

Circuits must be designed to avoid degradation due to NBTI over the full temperature range.

2.1.7 Non-volatile memory data retention

Re-programmable non-volatile memories must be designed to show reliable function during repeated write/erase cycles as well as during long time storage of data. The tests described in JESD47 table 1 a shall be used and estimations of field life time shall be documented and made available. For One Time Programmable circuits only the data retention test is applicable.

2.1.8 ESD sensitivity

Microcircuits must be designed to minimize ESD sensitivity due to pulses from Human Body Model (HBM) and Charge Device Model (CDM). Standards classified by the Manufacturer must be in accordance to JEDEC standards as described in 5.2.1 test 12 a and 12 b.

ESD test is mandatory on all devices and can not be based on similarity decisions.

2.1.9 Latch-up

The design must prevent Latch-up during normal operating conditions. In order to meet the JESD 78, each component design must be qualified by testing for Latch-up limits.

2.1.10 Unassembled microcircuits (bare dies)

Design data and electrical test data, specifically required for the application of bare dies, must be provided as agreed between the Manufacturer and Ericsson or in accordance to what is stated in JESD 49.

2.2 DfT and DfM

The vendor must ensure and be able to demonstrate that the aspects of the product design process include the methodologies by which the end product is truly manufacturable (i.e. DFM) and ensure that the testability (i.e. DFT) of the end product is competently and sufficiently developed.

2.3 Product package design

The required package must fulfill the requirements specified in the relevant Product specification, 1301-NNN xxx xxxx.

2.3.1 Terminal and pad identification

An orientation identification index (terminal no. 1) must be clearly visible on the package and detectable by the vision system when the component is mounted.
Bare dies must be identified with an appropriate designator. If requested proper documentation must be available.

2.3.2 Hermetic packages

Hermetic packages must be sealed with glass, metal or ceramic material (or combinations of these).
Metal or ceramic packages sealed with epoxy or similar are not considered to be hermetic.
The use of organic or polymeric materials inside hermetic packages must be qualified, based on a separate qualification procedure and adequate out-gassing procedures must be followed.

The outside surface of the package must not absorb krypton or helium in such a way that it may influence leak test results.

2.3.3 Plastic packages

The combinations of materials (e.g., mold compound, lead-frame, heat sink and the passivation of the die) must be properly selected so the packaged device can meet the requirements of the tests in paragraph 5. The mold must be free from voids and cracks.

Molding compound and lead-frame have to be tested to secure that no migration of lead-frame material between leads and between lead and die pad will take place. Test methods may vary but includes voltage, temperature and humidity as driving forces. This is especially important for packages with small pitch and silver plated bond fingers.

Integrity must be a major concern when designing plastic packages.
After mounting, the package must have an approved integrity.
Plastic packages must be designed to meet MSL (Moisture Sensitivity Level) 3, one week shelf life or longer. Exceptions are handled case by case.
Relevant Ericsson or external certified Electronic Manufacturing Services (EMS) units must be notified if MSL 3 not can be fulfilled.

2.3.4 Thermal resistance

The packages must be designed to fulfill the requirements in the relevant Product specification and reported according to JESD 51-12.01

2.3.5 Pick-up area

The component must have a flat pick-up area to secure safe pick-and-place operation. Wafer level packages shall have a backside protection to avoid die damages during pick and place.

2.3.6 Package warpage

Area array packages have to be characterized for warpage during the reflow soldering process. JESD22B112 describes the methodology. The maximum level of warpage is described in appendix 1. The requirements are based on an iNEMI work published in reference 6.5.6 and stated in appendix 1.

2.3.7 Board rework

Reworkability of the printed board assembly has to be considered when designing packages. Testing of component removal from the board without damaging the board or surrounding components is a part of package development. Also, how to assemble a replacement part with reliable solder joints has to be tested.

2.4 Design modifications

Qualification of a Major change shall be done as described in JESD 47.

2.5 Internal connecting system

2.5.1 Die attach

The die attach material used shall be selected with consideration taken to lead-frame material as well as other parameter likes e.g. electrical and thermal conductivity.

The Manufacturer must have a system in place to control important parameters like die attach thickness, die tilt, fillet height and die shear strength.

Monitoring tests must be performed to ensure that total amount of voids in the die attach is less than 10% of the die area.

2.5.2 Wire bonding

The Manufacturer must have design rules when selecting bond wires regarding capability of passing DC currents. Max DC currents must be according to MIL-PRF-38535

The Manufacturer must have a system in place to measure and control bonding parameters like bond pull strength, ball shear strength, wire sweep, wire-to-wire isolation distance and bond cratering.

For hermetic encapsulation, monometallic bonding system is preferred; i.e. the bond wire and the die metallization are made of the same material.
In case a gold- aluminum system is used in a hermetic package, the bond strength test shall be preceded by dry heat storage at 250°C for minimum 168h.

2.5.3 Flip-chip connections

Components where the die is connected by flip chip technology will be subject for more severe chip-package interaction than in the wire bond case. JEP-156A shall be used as base for design and testing.

Electromigration of flip-chip joints is a concern. JEP-154 shall be used to address this problem in design and testing.

2.6 Die surface protection

2.6.1 Passivation

The die must be effectively protected by a passivation layer(s).

2.7 Terminals

2.7.1 Finish

Protrusions and growths on leads must not occur and are cause for rejection. All types of plating must be designed or treated to avoid such occurrence at any time during normal operation, manufacturing, shipment or storage. Partial bridging between leads, including solder trapped in cracks, is also cause for rejection.

Partly uncovered copper areas and minor cracks in the plating are considered as cosmetic deviations and accepted from a reliability point of view as long as the solderability requirements are fulfilled. Gold plating may be used only if stated in the relevant Product specification or if the plating has a thickness of less than 20nm.

The plating recommendations from iNEMI regarding whiskers risks are applicable, see reference 6.5.3. Bright tin plating is not an acceptable terminal finish. Whiskers testing shall be done according to JEDEC Standard JESD22A121 and no whisker with a length over 40 µm shall appear before, during or after the testing.

2.8 Second level (solder joint) reliability

The Manufacturer or their subcontractor must have a process for evaluation of solder joint reliability on packages by testing and simulation. The simulation models must be verified by sample testing. JESD 94 gives basic information about temperature cycle testing for solder joint fatigue. Upon request the Manufacturer shall be able to present simulation or test data to support Ericsson in the evaluation process.

2.9 Mission profile

The unique requirement for components in Ericsson products are that they should survive 10-15 years with continuous service. In most cases services during maximum rating conditions are not expected more than for a limited time per day but in certain applications the time may approach 24 h per day. As mission profiles are application dependent they are communicated separately.

2.10 Safety

2.10.1 Self ignition

Flammability testing must be performed according to paragraph 5.2.2, test 15.

3 Requirements on manufacturing

3.1 Storage of materials

The conditions, specified in JESD 49 paragraph 3.9, are required for the storage of bare dies.

3.2 Packaging for transport

3.2.1 General

The date code must not be older than 24 months at the time of delivery for assembled microcircuits.
Exemptions must be verified by solderability tests, according to J-STD-02.

3.2.2 Marking of transportation package

For bare dies the generic type and revision number must also be provided.

3.2.3 Protection against ESD

Marking according to EIA 471 or JESD 625.

3.2.4 Moisture barrier bag (MBB) requirements

All plastic surface mounted devices must be delivered in a condition suitable for lead-free soldering processes. Procedures for handling of dry pack according to J-STD-033 must be implemented by the Manufacturer.
If an MBB is required it must have protective properties according to EIA 583 *Packaging Material Standards for Moisture-Sensitive Items*.
The MSL classification shall follow the procedure described in J-STD-020.

3.2.5 Tape and reel requirements

Carrier tape peel off strength, component placement within cavity and punched carrier tape dimension are important for smooth SMA production in Ericsson sites. EIA-481 shall be followed and all changes must be notified to Ericsson by a PCN.

The tape and the reel must have a specified maximum baking temperature that is verified to not cause any problem in the following SMA process. This temperature shall be marked on the reel and visible for human reading.

4 Requirements on quality assurance

4.1 Quality assurance procedures

4.1.1 Product reliability monitoring

Manufacturers must have a continuous product reliability monitor program to secure that this specification is met on an ongoing basis. The use of a failure mechanism driven approach to optimize the monitoring is encouraged. The supplier shall make product reliability monitor results available on request.

4.2 Improvement program

4.2.1 Quality and reliability expectations

Ericsson expects the following quality levels.

1. AOQ (Average Outgoing Quality) <10 ppm.
2. Early Life Failure Rate <50 ppm for the first one year of operation.
3. The Required Lifetime dependent on major failure mechanisms >10-15 years.
4. Long Term Failure Rate <1 FIT @ 55°C ambient in typical service.

This shall not be regarded as final requirements. Actual requirements regarding the above parameters are stated in the applicable Product Specification and/or GPA.

5 Required quality level

5.1 General

This chapter defines the required quality of delivered microcircuits.
The Manufacturer is not obliged to perform the tests exactly as specified. The Manufacturer must, however, ensure that microcircuits delivered to this quality specification will fulfill the specified requirements. Knowledge Based Qualification as outlined in JESD91, “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms” and JESD94, “Application Specific Qualification using Knowledge Based Test Methodology” is accepted based on evidence of successful use.

The qualification can be according to JESD 47 or according to tests specified below. Family qualification and Qualification by similarity as described in JESD 47 can be used.

The statistical sampling plans and procedures given by IEC 60410 are applicable. When fixed sample sizes (SS/c) are given, alternate corresponding numbers from LTPD (Lot Tolerance Percentage Defective) tables are accepted.

The level of early failures must be kept to a minimum by process control and if necessary by screening. Due to sample size limitations the showed failure levels might be higher than stated in 5.2.1 test 4 at time for the initial qualification but must be fulfilled as more samples are available.

For bare dies the required quality level(s) are specified in the Product specification.

A failure in a microcircuit shall be deemed to include any deviance from the specifications applicable for such microcircuit, including, for the avoidance of doubt, intermittent failures.

Post stress failure criteria according JESD47 shall be used. Degradation analysis with delta measurements shall be made to ensure performance over the expected life time. Preferably the degradation is measured at start of the test, at all interim test occasions and at the end. Examples are found in JEP 118.

5.1.1 Qualification plan

A qualification plan is expected to be available for all devices in development. For circuits designed for Ericsson this plan shall be agreed upon at time for contract writing.

5.1.2 Qualification report

A report describing the tests done before release of the product shall be available upon request and include motivation for qualification by similarity decisions. JESD69 can be used as a template. For components developed for Ericsson the report is a part of the final product delivery.

5.1.3 Characterization

Characterization at least according to JESD86 is expected and should be available upon request.

5.2 Qualification and monitoring tests

Package codes in the tables:

1. A = Area Array Packages (BGA, CSP, QFN etc)
2. B = Plastic surface mounted
3. C = Hermetic through hole mounted
4. D = Bare dies
5. H = Hermetic surface mounted
6. P = Plastic through hole mounted

5.2.1 Device qualification tests

Test no	Pack type	Test	Conditions	SS/c
1	All	Pre- and Post- Stress Electrical test (TST)	According to applicable component specification.	All components in test
2	All	Electrical Parameter Assessment (ED)	JESD86, according to datasheet or product specification	30/0 3 lots
3a	All	High Temperature Operating Life (HTOL)	JESD22-A108, JESD85, T_j≥125°C, 1000h , Vcc≥Vcc max	231/0 3 lots
3b	ABCHP	RF Biased Life (RFBL)	JESD226, T_j≥125°C, 1000h, when applicable	15/0
3c	ABCHP	Power Temperature Cycling (PTC)	JESD22-A105, only if power ≥1W or delta Tj≥40°C, 1000 cycles, Tcase -40/125°C, when applicable	15/0
4	All	Early Life Failure Rate (ELFR)	JESD22-A108 and JESD74, Tj≥125°C t≥48 h, 100 FPM	JESD47 for sample size
5	All	Low Temperature Operating Life (LTOL)	JESD22-A108, Tj≤50°C, 1000 h, Vcc≥Vcc max	32/0 1 lot
6	ABCHP	High Temperature Storage Life (HTSL)	JESD22-A103, cond. A, +150°C 1000h	75/0 3 lots
7	All	Non-Volatile Memory UnCycled High Temperature Data Retention (UCHTDR)	JESD22-A117, Conditions and requirements according to JESD47	231/0 3 lots
8	All	Non-Volatile Memory Cycling Endurance (NVCE)	JESD22-A117, Conditions and requirements according to JESD47	231/0 3 lots
9	All	Non-Volatile Memory Post Cycling High Temperature Data Retention (UCHTDR)	JESD22-A117 Conditions and requirements according to JESD47	117/0 3 lots
10	All	Non-Volatile Memory Low-Temperature Data Retention and Read Disturb (LTDDR)	JESD22-A117, Conditions and requirements according to JESD47	114/0 3 lots
11	All	Latch up (LU)	JESD 78, Class II, Immunity level A (level B allowed but must be reported according to JESD78)	3/0
12a	All	Soft error rate test, accelerated (ASER)	JESD89-2 and JESD89-3 at Ta=25°C <2000 FIT or mutually agreed level	3/0
12b	All	"or" Soft error rate test, system (SSER)	JESD89-1, Minimum of 1E+06 device hours or 10 fails	
13a	All	ESD (HBM)	JS-001, class 1C, (1000V) or mutually agreed level	3/0
13b	All	ESD (CDM)	JS-002, class C1 (250V) or mutually agreed level	3/0

5.2.2 Package qualification tests

Test no	Pack type	Test	Conditions	SS/c
1	All	Pre- and Post- Stress Electrical test (TST)	According to applicable component specification.	All compo-nents in test
2	ABP	Sold. Pre-conditioning (PC)	J-STD-020, procedure according to JESD22-A113	All compo-nents in test no 4-6
		Not MBB packed comp.	Level 1 (85°C/85% RH,168h)	
		MBB packed comp.	Level 3 (30°C/60% RH,168h)	
3	AB	Warpage characterization	JESD22-B112, dry and soaked condition, see appendix 1 for allowed warpage levels	3 of each cond.
4	ABCHP	High Temperature Storage Life (HTSL)	JESD22-A103, JESD22-A113 cond. A, +150°C 1000h	75/0 3 lots
5	ABP	Temperature Humidity Bias (THB) or (HAST)	JESD22-A101, 85°C/85% RH, 1000h or JESD22-A110, 130°C/85% RH, 96h	75/0 3 lots
6	ABCHP	Temperature cycling (TC)	JESD22-A104, cond. B, -55/125°C 700 cycles or cond. C, -65/150°C 500 cycles	75/0 3 lots
7	ABP	Unbiased Temperature/Humidity (UHAST)	JESD22-A118, 130°C/85% RH, 96 h	75/0 3 lots
8	ABCHP	Wire bond shear (BS)	JESD22-B116, Ppk>1.66 or Cpk>1.33	150 bonds / 5 units
9	A (only if ball)	BGA ball shear test (SBS)	JESD22-B117	150 bonds / 5 units
10	ABCHP	Bond Pull strength (BPS)	M2011, Ppk>1.66 or Cpk>1.33	150/0 (bonds) 5 units
11	BCHP	Solderability (SD)	J-STD-02	66/0 (leads) 3 lots
12	CH	Mechanical shock	JESD22-B104, cond. B 1500g	116/0 3 lots
13	CH	Vibration, var. frequencies	JESD22-B103	116/0 3 lots
14	CH	Internal Water Vapor	MIL-STD-883/1018	3/0
15	ABP	Flammability	UL 94V-0	Bulk
16	ABCHP	Marking permanency	JESD22-B107	8/0
17	BCHP	Lead Integrity	JESD22-B105, for hermetic packages followed by test JESD22- A109	8/0
18	BCHP	Tin Whiskers Acceptance (WSR)	JESD22-A121 and JESD201	Class 2

5.2.3 Lot acceptance tests

Test no	Pack type	Test	Conditions	SS/c	Insp. level/ AQL%
1	ABCHP	Electrical tests	Product specification		S1/0.02
2	ABCHP	External visual	JESD22-B101		S4/0.1
3	ABH	Co-planarity	Product specification or JESD22-B108 method 1, (seating plane) < 0.1 mm		II/0.02 pin-count
4		Process Average Testing (PAT)	AEC Q001		As agreed
5		Statistical Bin/Yield Analysis	AEC Q002		As agreed
6	All	Dimensions	JESD22-B100		S4/0.1
7	CH	Hermeticity, fine leak	JESD22-A109, cond. A		II/0.04
8	CH	Hermeticity, gross leak	JESD22-A109, cond. C		II/0.04

5.2.4 Wear-out tests

In many cases dedicated wear-out tests for specific failure mechanisms is the only way to show life times longer than a few years. JEP 122 gives detail on how these calculations shall be done.

5.2.4.1 Electromigration

The Manufacturer must perform appropriate testing to provide characterization data, of the metallization system, in order to demonstrate less than 0.1% failures after 10 years operation @ max allowed T_j for the layout dimensions used.
This characterization data must cover the metallization and contact process as a whole, using accelerated current and temperature testing of test structures on the wafer rather than individual types.

The test methods described in JESD 61 can be used.
Calculation models are described in JESD 63. If other methods are used details and results must on request be provided as a written report.
Acceleration factors must be justified by experimental data. The layout design rules must be based on the wear-out test result and a procedure to check that the design rules are used in the actual circuit design must be in place.

5.2.4.2 Time Dependent Dielectric Breakdown (TDDB)

The Manufacturer must perform appropriate testing to provide characterization data of oxide integrity, in order to demonstrate less than 0.1% failures after 10 years operation @ max allowed T_j for the layout dimensions used.
The data must cover all critical dielectric layers.

The test methods described in JESD 35 can be used. If other methods are used details and results must on request be provided as a written report. Acceleration factors must be justified by experimental data.

5.2.4.3 Hot Carrier Injection (HCI)

The Manufacturer must perform appropriate testing to provide characterization data of hot carrier injection, in order to demonstrate less than 0.1% failures after 10 years operation @ minimum operating temperature for the layout dimensions used.
The data must cover all critical transistor types.

The test methods JESD 28 (NMOS) and JESD 60 (PMOS) can be used. If other methods are used details and results must on request be provided as a written report.
Acceleration factors must be justified by experimental data. The layout design rules must be based on the wear-out test result and a procedure to check that the design rules are used in the actual circuit design must be in place.

5.2.4.4 Negative Bias Temperature Instability (NBTI)

The Manufacturer must perform testing to provide characterization data on the negative bias temperature instability for critical transistors. The requirement is less than 0.1% failures after 10 years operation @ maximum allowed junction temperature and gate oxide electrical field. Test method and extrapolation model shall be according to JESD90 or similar.

5.2.4.5 Stress induced voiding (SM)

The Manufacturer must perform testing to secure that metal voiding or migration due to temperature induced stress does not occur during normal use. The extrapolated failure level shall be less than 0.1% after 10 years operation @ maximum allowed temperature. Testing shall be done according to JEP139.

6 References

6.1 Ericsson documents

6.1.1 Product specification, 1301-NNN xxx xxx Uen

6.1.2 General quality requirements on components, 105 63-2031 Uen

6.2 IEC publications

6.2.1 Sampling plans and procedures for inspection by attributes, IEC 60410

6.3 Military specifications

6.3.1 Test methods and procedures for microelectronics, MIL-STD-883

6.3.2 Performance specification: general specification for integrated circuits manufacturing, MIL-PRF-38535

6.4 JEDEC specifications

6.4.1 Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices, J-STD-020

6.4.2 Standard for handling, packing, shipping and use of moisture/reflow sensitive surface mount devices, J-STD-033

6.4.3 Component test methods, JESD 22

6.4.4 A procedure for measuring N-channel MOSFET hot-carrier-induced degradation at maximum substrate current under DC stress, JESD 28

6.4.5 Procedure for wafer-level-testing of thin dielectrics, JESD 35

6.4.6 Customer notification of product/process changes by semiconductor suppliers, JESD 46

6.4.7 Stress-test driven qualification of integrated circuits, JESD 47

6.4.8 Information Requirements for the Qualification of Silicon Devices, JESD 69

6.4.9 Procurement standard for known good die, JESD 49

6.4.10 Methodology for the thermal measurement of component packages (single semiconductor packages), JESD 51

6.4.11 A procedure for measuring P-channel MOSFET hot-carrier-induced degradation at maximum gate current under DC stress, JESD 60

6.4.12 Isothermal electro-migration test procedure, JESD 61

6.4.13 Standard method for calculating the electro-migration model parameters for current density and temperature, JESD 63

6.4.14 Latch-up in CMOS integrated circuits, JESD 78

6.4.15 Measurement and reporting of alpha particle and terrestrial cosmic ray induced soft errors in semiconductor devices, JESD 89

6.4.16 Requirements for handling electrostatic discharge sensitive (ESDS) devices, JESD 625

6.4.17 Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes, JESD22A121

6.4.18 High Temperature Package Warpage Measurement Methodology, JESD22B112

6.4.19 Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) – Component Level JS-001-2012

6.4.20 RF Biased Life (RFBL) Test Method JESD226

6.4.21 A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities JESD 90

6.4.22 Guidelines for GaAs MMIC and FET Life Testing, JEP 118

6.4.23 Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress, JEP-154

6.4.24 Chip-Package Interaction, Understanding, Identification, and Evaluation, JEP156A

6.4.25 Failure Mechanisms and Models for Semiconductor Devices, JEP-122

6.5 Other specifications

6.5.1 Symbol and label for electrostatic sensitive devices, EIA 471

6.5.2 8 mm Through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling, EIA 481

6.5.3 Tests for flammability of plastic material, international standard, UL 94

6.5.4 EIA 583 *Packaging Material Standards for Moisture-Sensitive Items*

6.5.5 Recommendations on Lead-Free Finishes for Components Used in High-Reliability Products, International Electronic Manufacturing Initiative, iNEMI, tin whisker user group

6.5.6 Recent Trend of Package Warpage Characteristic, by Wei Keat Loh, Ron Kulterman, Tim Purdie, Haley Fu, Masahiro Tsuriya

7 Document revision information

Rev	Description
M	2.2.2 and 2.2.3: Rephrased. 2.3: JEP 117 is added as spec for PNC's 3.6.1: Changed req. to 18 month date code at time of delivery. 3.6.3: Changed to: The same protective properties as MIL-B-81705 Type 1. 5.2.3: Test 1a and 1b Ericsson spec. 105 82-103 Uen only as reference. 5.2.3: Test 2 changed req. 5000 ppm residual gas in package. 5.2.3: Test 5 and 6 corrected the conditions referred to in gross and fine leak.
N	The documents and standards valid today regarding requirements on component quality are added. Paragraphs for Acceptance criteria, Quality agreements and Ship-to-stock/Ship-to-line are removed. These requirements are included in the General Purchase Agreement (GPA). Paragraphs for Ericsson component design system, Building in reliability (BIR), Human body model and Charged device model are also removed. 1.1: reference to ETX 105 63-ROK 101 Uen removed. 2.2: Reference to 1301-RYT Uen removed. 4.1.1: Reference to 1/105 63-RYT Uen removed. See also change markings.
S	2.1.6 OTP memories added 2.2.3 Lead-frame metal migration precautions added 2.2.6 Warpage testing added 2.7.2 Whiskers requirement better specified 3.6.4 Clarified the MSL requirements 3.6.5 NTK reference deleted 5.2 New definition of package code A and new layout 5.2.1 ESD MM as optional. 5.2.3 Test method added to the coplanarity test and 0.1 mm req. Removed Area array packages from lead integrity test. 6. A Jedec sub-title introduced
T	Rewritten to fit new JESD47. 2.1.2 NBTI added 2.7.2 SnPb removed as surface finish and simplified text 2.8 Test method reference added 3.6.4 MSL marking on MBB 4.2.1 New more demanding wording 5.1 Definition of failure added 5.2.1-5.2.3 Rewritten based on JESD47

Rev	Description
	5.2.4 NBTI and Stress voiding added
U	1.1.2 Qualification removed 2.1.4 Soft error rate level changed to 2000 FIT 2.2 Added paragraph on DfT and DfM 2.3.5 Added text about backside protection for WLP 4.1.1 Replaced qualification maintenance with relibility monitoring 5.1 Short note about family qualification added 5.2 Tin whisker test added and some other adjustments to test tables 5.2.4 Changed Tj=85 ^{o}C to max allowed Tj
V	The repeated references to 10563-2031 have been removed reducing the number of paragraphs. 1.1 Some adjustment of the text 2.1.6 Added a NBTI paragraph 2.1.8 Removed the Machine Model 2.1.9 Text adjustment 5.1 Added requirements on failure criteria and delta measurements 5.2.1 Added RF HTOL and removed MM EDS test. Changed levels on HBM and CDM ESD test 5.2.2 Removed note regarding humidity test of high power devices
X	1.1 Clarification of how the spec shall be used and relation 10563-2031 2.1.3 Added detail about power cycling problems 2.1.7 More use of reference to JESD47 2.1.8 Clarify the need for ESD test 2.3.3 New text to clarify MSL requirement 2.3.4 Changed reference 2.3.6 New requirements on warpage 2.3.7 New requirement on rework 2.5.3 New paragraph on internal flip-chip joints 2.9 New paragraph on mission profile 3.2.1 New reference 3.2.4 New reference 3.2.5 Added tape and reel requirements 4.2.1 Changed to 10-15 years life expectation 5.1 Added comment about qualification by similarity and degradation measurement 5.1.1 Added paragraph on qualification plan 5.1.2 Added paragraph on qualification reporting 5.1.3 Added paragraph on characterization 5.2.1-3 Many changes in the test tables 5.2.4 Added text and reference. Changed life time requirements in the wear-out tests to 10 year and 0.1% accumulated failures Appendix 1 Added warpage requirement table

Appendix 1

Warpage requirements

Flatness requirements during reflow applies to temperature range from 150 °C to reflow peak. Positive (+) warpage is defined as corners down (convex package) and negative (-) is defined as corners up (concave package) during reflow.

Maximum warpage (µm)		
Pitch (mm)	Warpage (+)	Warpage (-)
0.3	75	70
0.4	90	75
0.5	95	75
0.65	110	80
0.8	160	110
1	205	125
1.27	210	130
1.5	210	130