A Quick Guide to Synopsys University Program Resources

Courseware & SolvNetPlus

University Program, Synopsys Taiwan

May 2021

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Contents

- Membership Benefit
- Teaching Resources (courseware, generic libraries, PDKs)
- Knowledge Base (SolvNetPlus)

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- **Membership Benefit**
- Teaching Resources (courseware, generic libraries, PDKs)
- Knowledge Base (SolvNetPlus)

Membership Benefits

IC Design and EDA Curriculum:

- Full Semester Courses – ***80+ courses*** for Bachelor and Master programs
- Workshops/Lectures - ***30 courses***
- Short Lectures/Labs - ***28 courses***

Teaching Support:

- ***32/28nm*** & ***90nm*** Generic Libraries and iPDK's
- Generic Memory Compiler

Access to SolvNetPlus for Synopsys knowledge base:

- **Document –** contains product release note, installation guide, user guide & reference manual
- **Training –** contains on-line videos for short trainings, CES training courses, and product update trainings
- **Search –** provides an advanced search engine to retrieve information from various sources, such as documentation, articles, training, and so on.

*Requires SolvNetPlus account to access above-mentioned resources.

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Teaching Resources

Teaching Resources
教學資源

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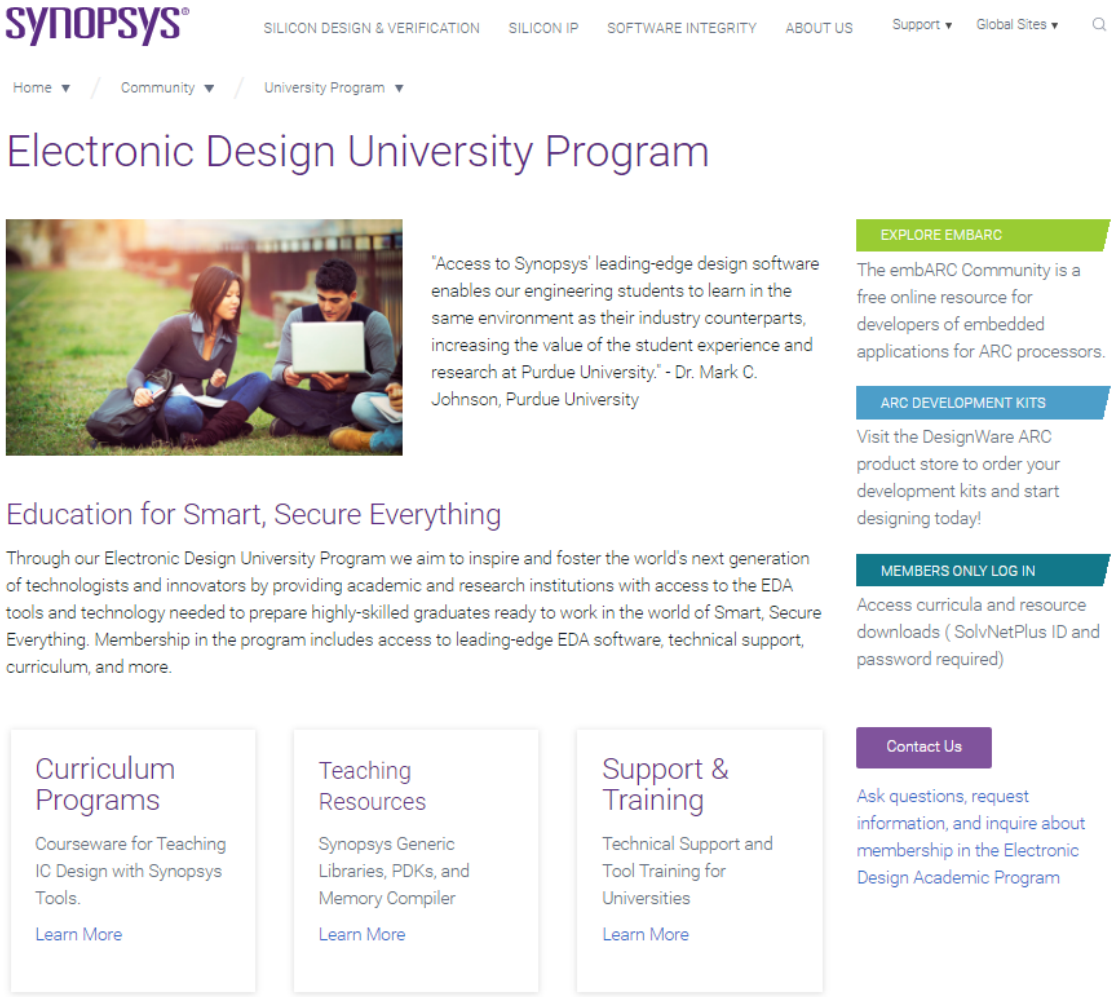
☞ Access through:
www.synopsys.com/community/university-program.html



Teaching Resources

IC Design and EDA Curriculum

IC Design Courses

Bachelor

- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital Integrated Circuits
- IC Design Flow
- IC Design Introduction
- IC Testing
- IC Synthesis and Optimization
- Introduction to Microelectronic Circuits
- IC Synthesis and Optimization
- Introduction to Semiconductor Devices
- Linear Algebra
- Logic Design
- Microprocessor Systems
- Numerical Methods
- Scripting Languages for Beginners
- Static Timing Analysis
- Synthesis and Optimization of Digital Integrated Circuits
- Technical Writing

Master

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- EDA Tools
- FPGA Prototyping
- IC Design for Thermal Issues
- IO Design
- Low Power Design
- Low Power Design with Synopsys 32/28nm Generic Library
- Mixed-Signal IC Design
- Modeling and Optimization of IC Interconnects
- Rad-hard IC Design
- RF IC Design
- Synopsys EDA Tool Flow for Front-End Digital IC Design
- Synopsys EDA Tool Flow for Back-End Digital IC Design
- Thermal and Electro-Thermal Simulation: Achievements and Trends

Short Lectures and Workshops

Short Lectures

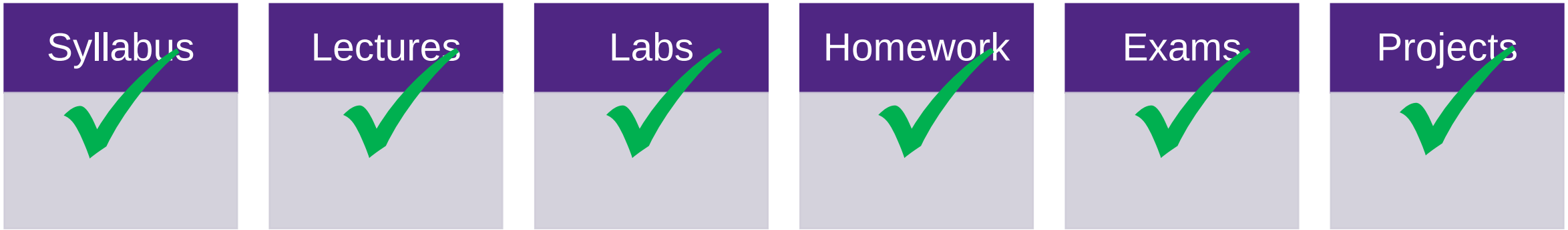
- Basic Perl Programming
- Characterization with SiliconSmart
- Circuit Simulation Transient Analysis
- Compiler Optimization and Code Generation
- Computer Networks
- Digital Design with Verilog
- Digital System Design and Simulation with VHDL
- Embedded Systems Design
- How to Create an Interoperable PDK
- IC Fabrication
- IC Simulation Theory
- Introduction to RF Communication
- Introduction to Verilog HDL
- Low Power Design w/Synopsys 32/28nm Generic Library
- Low Power Methodology Manual for 32/28nm
- Operational Research
- Optimization Methods
- Physical Verification Russet Development
- Power-Performance Optimization of Digital Circuits
- Process Variation Aware Design
- RF Circuits
- Scripting Languages
- Sequential Elements
- Signal and Power Integrity
- Statistical Techniques for Timing Analysis
- Subthreshold Design and Implementation
- Synthesizing OpenSPARC with 32/28nm EDK
- Techniques for Circuit Simulation
- User Interface Design
- Verification Methodology for Low Power

Workshops

- Advanced Design of Digital Circuits for Specific Applications
- ASIC Design Flow Tutorial Based on Synopsys 32/28nm Library
- ASIC Design Flow Tutorial Based on Synopsys 90nm Library
- Chip Design
- Computer Arithmetic Applied to High-Performance Cryptography
- Design for Testability
- Full Custom IC Design Flow with Synopsys Custom Tools
- Project Management
- Software Methodology Module for Custom Designer
- Synopsys Design Flow Tutorial
- Synopsys IC Design Flow Based on 90nm Generic Library
- SystemVerilog Verification Tutorial
- TCAD Course
- TCAD for VLSI Design
- TCAD Quick Start Guide
- TCAD Short Course
- Universal Verification Methodology

Full Semester Courses

- Topics cover all aspects of IC/SoC design
- Courseware for Bachelor and Master level programs
- Full-semester courses contain ~15 weeks of material and include the following components



Teaching Resources

Teaching Support (Generic Libraries, PDKs, Generic Memory Compiler)

Generic Libraries (EDK)

- 32/28nm and 90nm

- Enables students to master advanced design methods using the latest Synopsys EDA tools
- Includes:

Digital Standard Cell Library	I/O Cell Library	I/O Special Cell Library	Embedded Memories
Phase Locked Loop	Low Power Memories	Reference Designs	

- Used by Synopsys for:

Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Interoperable Process Design Kits (iPDKs)

- 32/28nm and 90nm

- Enables students to master AMS/Custom design with the Synopsys custom implementation tool suite
- Includes:

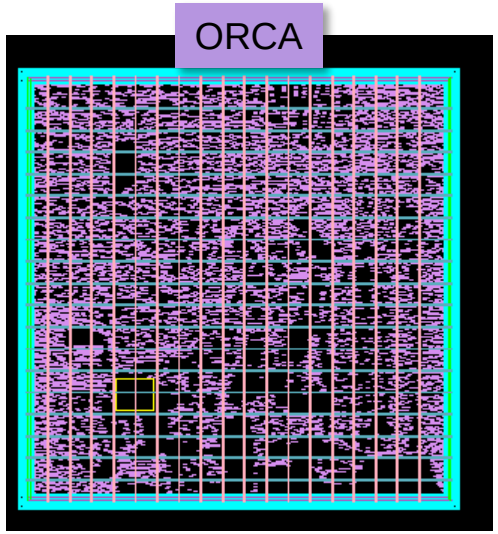
Technology Files	Parasitic Extraction Files	Symbol Library and Python PCells	Embedded Memories
Physical Verification Files	HSPICE Models	Callback Scripts	Setup Files

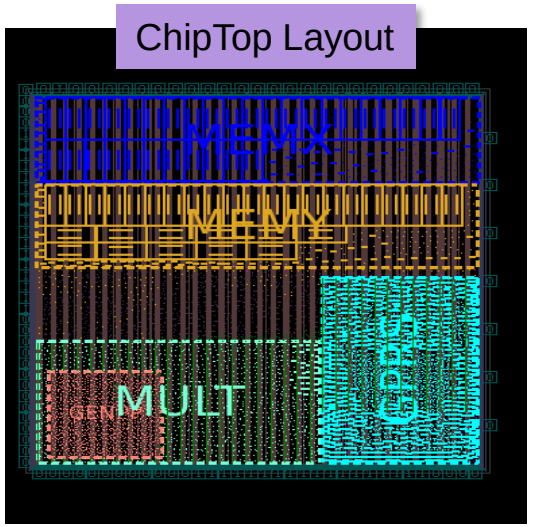
Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Reference Designs Supported by Synopsys EDKs

- **DesignWare® ARC 600 Academic Core** - 32-bit RISC processor core optimized for embedded applications and DSP tasks
- **ARM® Cortex® - M0 DesignStart™ Processor** - Entry-level configuration of ARM Cortex-M0 microprocessor[1]
- **OpenSPARC T1** - 64-bit multicore processor[2]
- **LEON3** - 32-bit embedded processor[2]
- Sample Processor Designs - included in EDK
  - ORCA for timing analysis
  - ChipTop for low power design

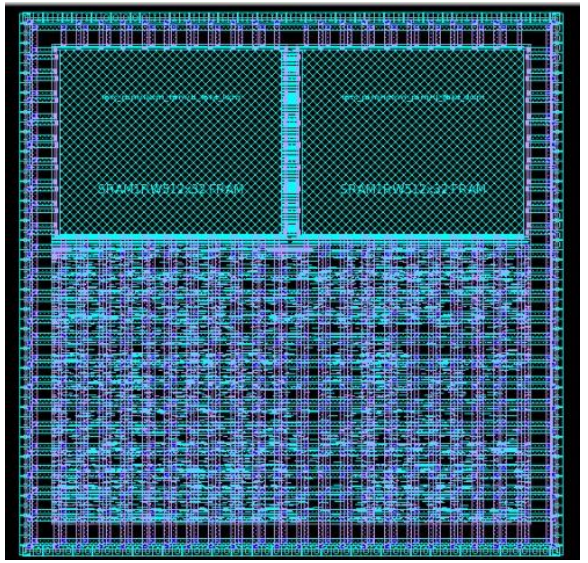
1. *Available through ARM DesignStart for Processor IP portal*
2. *Available via GNU General Public License*





DesignWare ARC 600 Processor Design

- Synthesis scripts optimized for 32/28nm EDK that can be used to easily redesign the academic version of the ARC 600 processor
- Synopsys curriculum for the ARC 600
  - IC Synthesis Based on DesignWare ARC 600 Core, includes:
    - Lecture slides
      - Covers ARC 600 details and EDA tool use
    - Laboratory works
      - Step-by-step guide of the ARC 600 design process

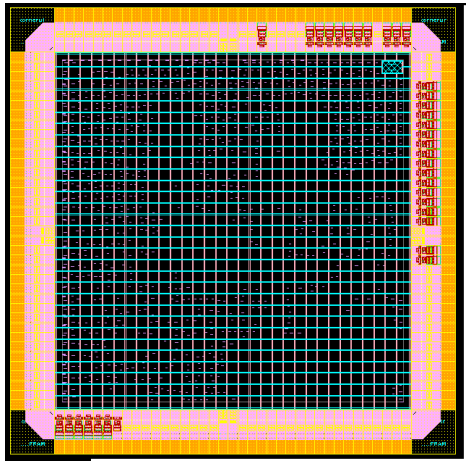


Apply in Members Only for access to the DesignWare ARC 600 Academic Core:
https://www.synopsys.com/apps/protected/university/members.html

ARM Cortex-M0 DesignStart Processor Design

- Complete Synthesizable Solution
  - Pre-configured Verilog netlist derived from commercial Cortex-M0 processor
  - Simple testbench
  - Example test code
- Scripts to implement the ARM Cortex-M0 DesignStart design using Synopsys 32/28nm EDK and EDA tools
- Synopsys curriculum for the ARM Cortex-M0
  - IC Synthesis Based on ARM Cortex-M0 DesignStart Processor

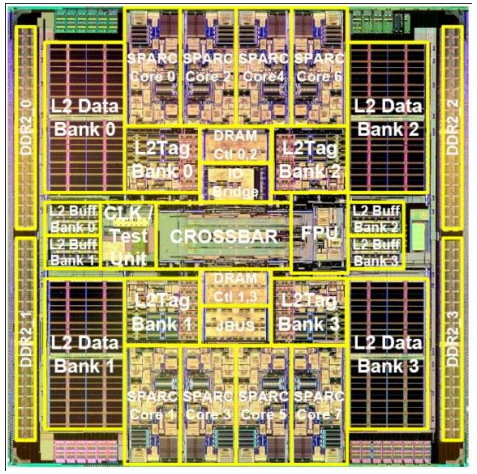
Download from ARM DesignStart for Processor IP portal:
http://arm.com/products/processors/designstart-processor-ip

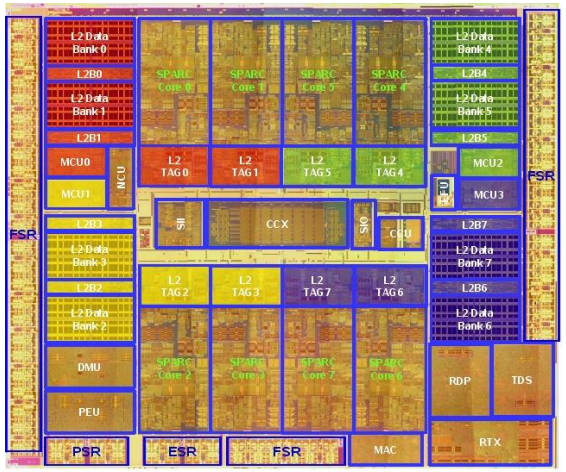


OpenSPARC Processor Design

- Scripts to enable OpenSPARC design using Synopsys 32/28nm EDK and Design Compiler
- Implemented low power design techniques
- Synopsys curriculum for OpenSPARC
  - Computer Architecture
  - Includes:
    - Physical design scripts for IC Compiler
    - Scripts to enable small block reuse for educational purposes
    - Various lab projects based on small blocks

Download OpenSPARC:
http://www.opensparc.net





Synopsys Generic Memory Compiler

- Configurable software that automatically generates static RAM circuits of different types and sizes with all required deliverables
- Generate custom memory instances for educational ICs
- Designed for use with Synopsys EDKs and EDA tools
- Optimized for the Synopsys Digital Design Flow
- Supports multiple technologies (90nm, 32/28nm, etc.)

User interface

- Command line
- GUI

Supported memory types

- 1 port SRAM
- 2 port SRAM
- 1 port Low Power SRAM
- 2 port Low Power SRAM

*"Using the Synopsys Generic Memory Compiler in our complex processor for DSP application was a **great time-saving tool**. It helped the students generate the SRAM they wanted in a snap, saving them critical time to concentrate on the rest of the complex design."*

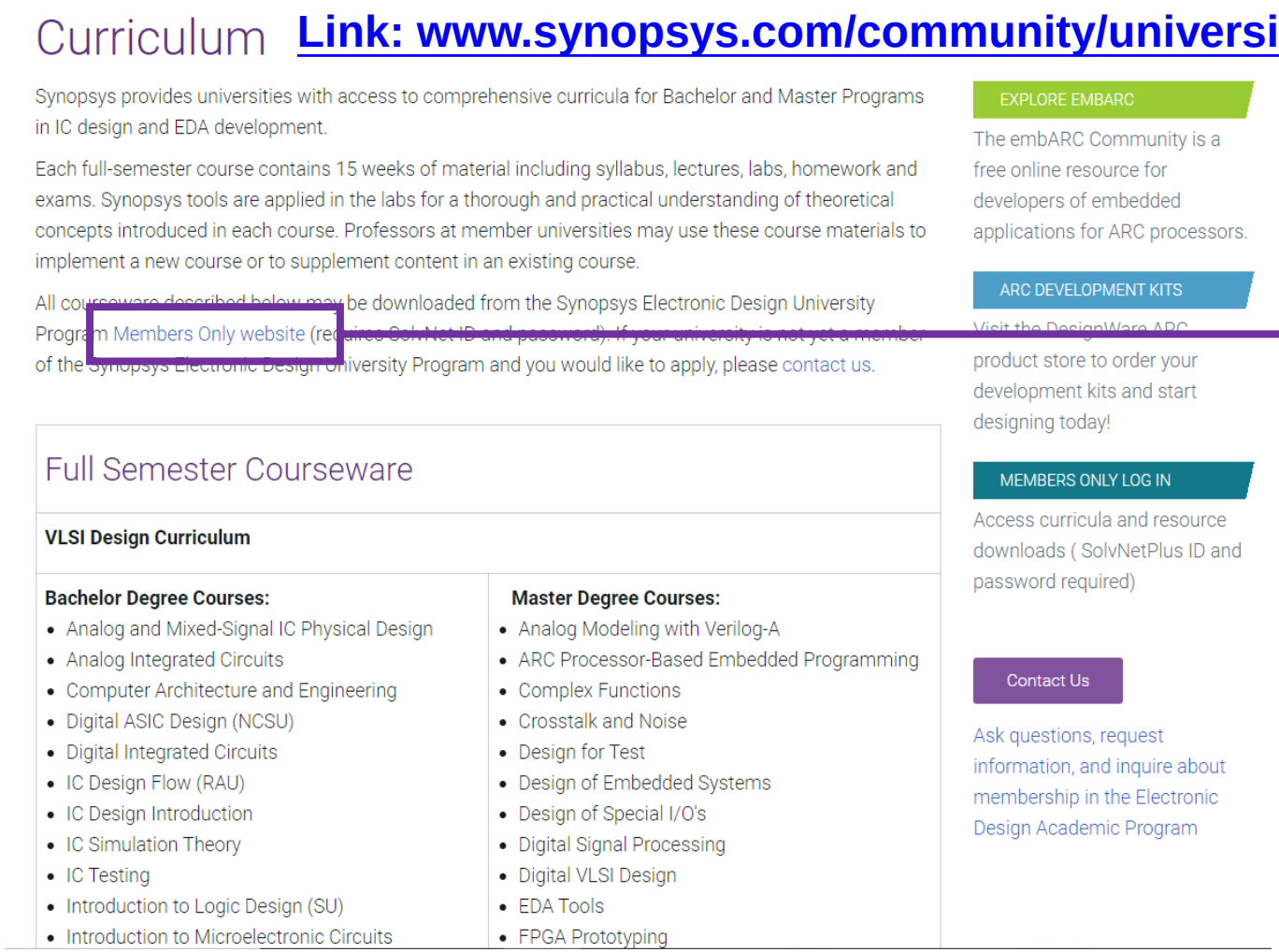
Dr. Maged Ghoneima, American University in Cairo

Get started w/ Teaching Resources

Link: www.synopsys.com/community/university-program.html

01 Go to Electronic University Program website

Select the Teaching Resources that you need, then click on “ Members Only website”.



Curriculum

Link: www.synopsys.com/community/university-program.html

Synopsys provides universities with access to comprehensive curricula for Bachelor and Master Programs in IC design and EDA development.

Each full-semester course contains 15 weeks of material including syllabus, lectures, labs, homework and exams. Synopsys tools are applied in the labs for a thorough and practical understanding of theoretical concepts introduced in each course. Professors at member universities may use these course materials to implement a new course or to supplement content in an existing course.

All courseware described below may be downloaded from the Synopsys Electronic Design University Program Members Only website (requires SolvNet ID and password). If your university is not yet a member of the Synopsys Electronic Design University Program and you would like to apply, please contact us.

Full Semester Courseware

VLSI Design Curriculum

Bachelor Degree Courses:

- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital ASIC Design (NCSU)
- Digital Integrated Circuits
- IC Design Flow (RAU)
- IC Design Introduction
- IC Simulation Theory
- IC Testing
- Introduction to Logic Design (SU)
- Introduction to Microelectronic Circuits

Master Degree Courses:

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- Digital VLSI Design
- EDA Tools
- FPGA Prototyping

EXPLORE EMBARC

The embARC Community is a free online resource for developers of embedded applications for ARC processors.

ARC DEVELOPMENT KITS

Visit the DesignWare ARC product store to order your development kits and start designing today!

MEMBERS ONLY LOG IN

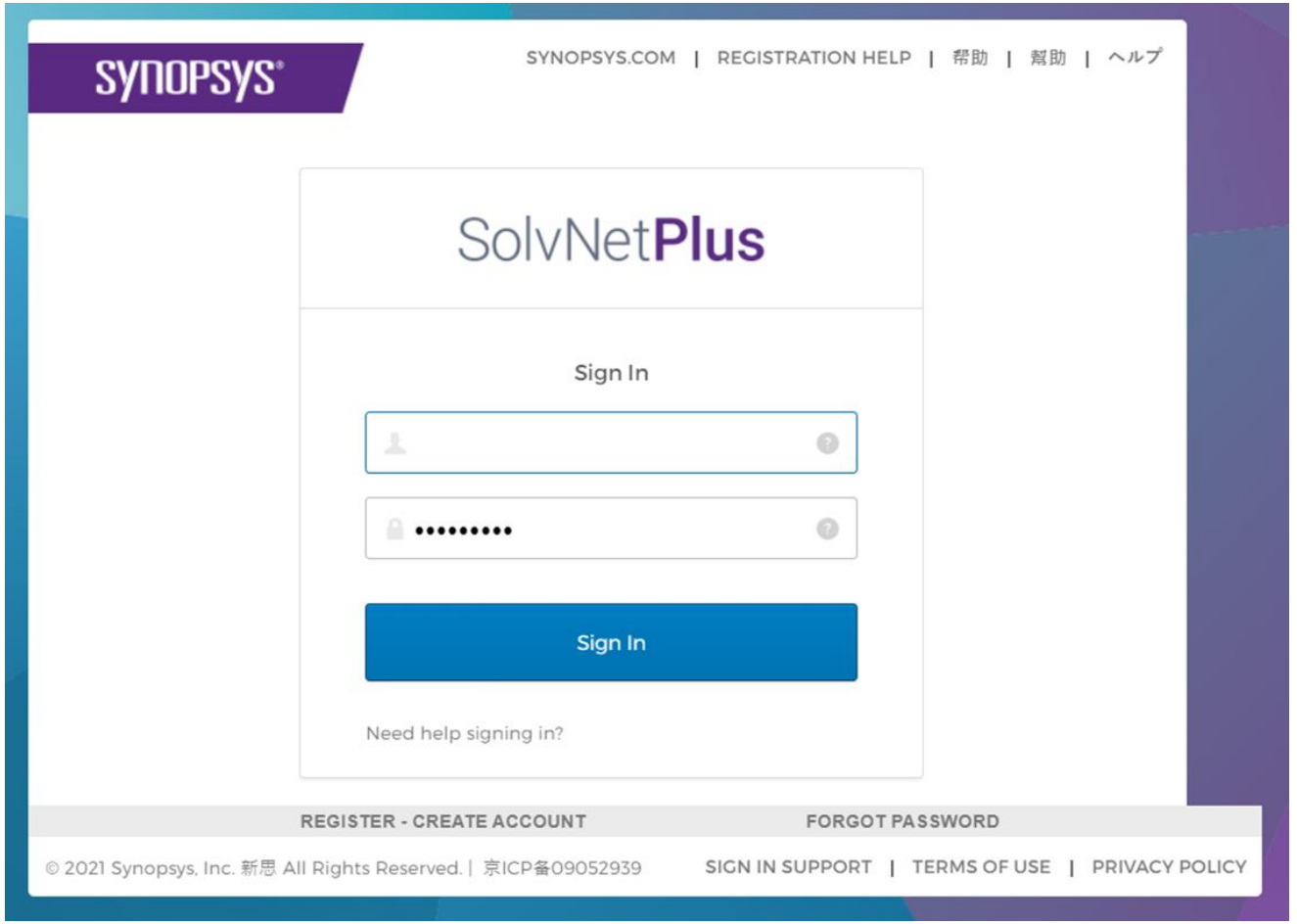
Access curricula and resource downloads (SolvNetPlus ID and password required)

Contact Us

Ask questions, request information, and inquire about membership in the Electronic Design Academic Program

- Requires a SolvNetPlus account to sign in.
- Please contact *Synopsys University Program – Taiwan (chunhsu@synopsys.com)* for membership enquiry.

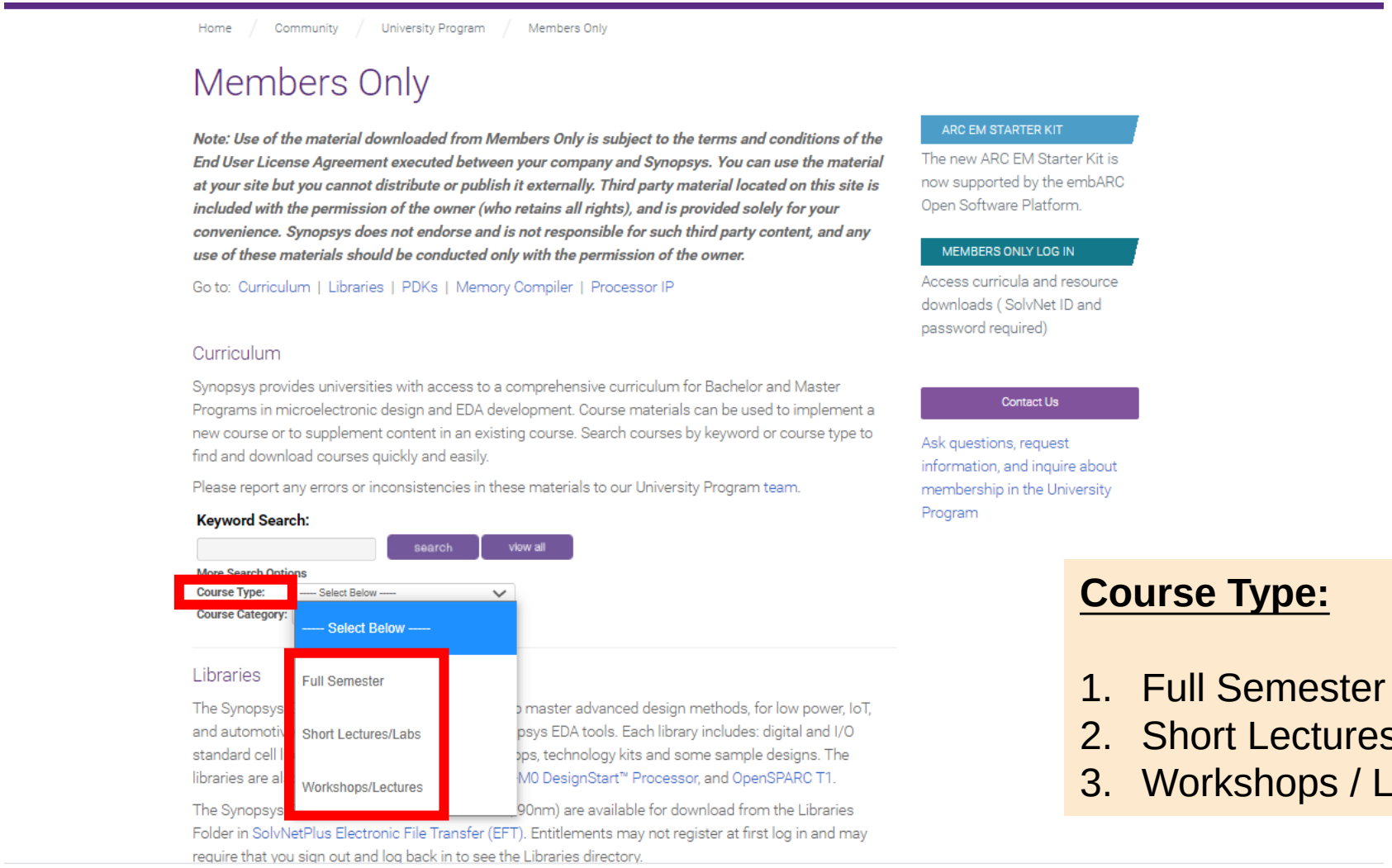
02 Log-in with Synopsys SolvNetPlus credential



https://www.synopsys.com/apps/protected/university/members.html

03 Insert course name in the search engine

Search by “Course Type”



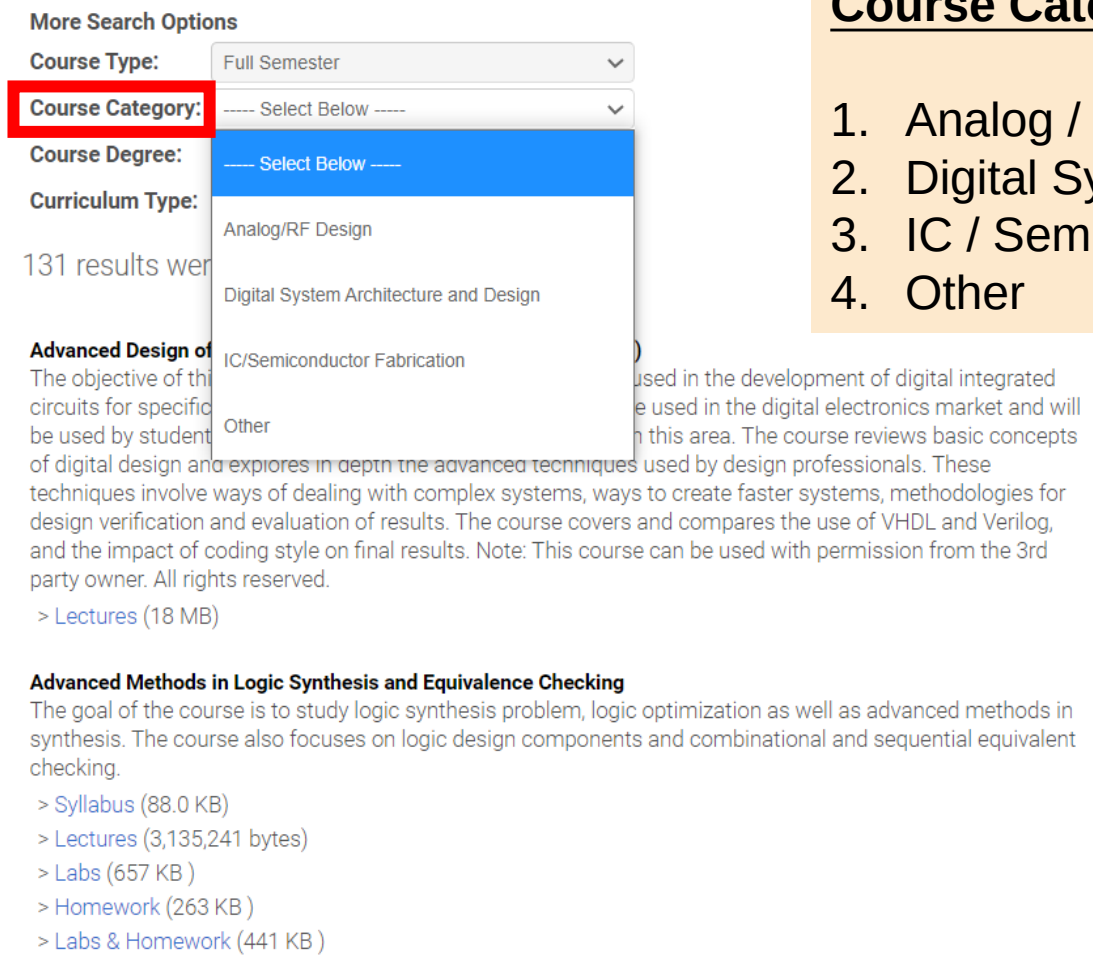
Course Type:

1. Full Semester
2. Short Lectures / Labs
3. Workshops / Lecturers

03 Insert course name in the search engine (cont.)

Search by “Course Category”

Example : Full Semester



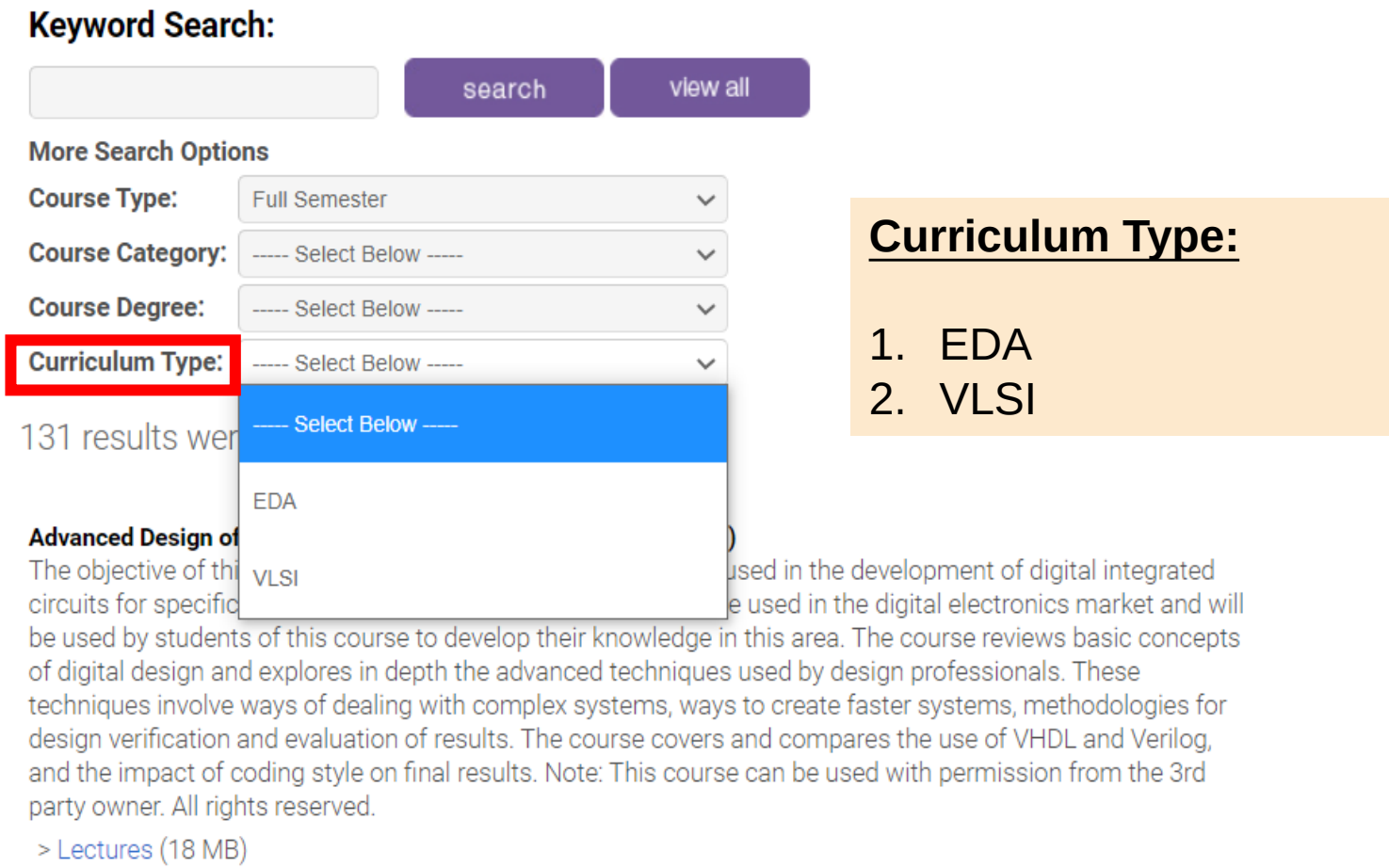
Course Category:

1. Analog / RF Design
2. Digital System Architecture and Design
3. IC / Semiconductor Fabrication
4. Other

03 Insert course name in the search engine (cont.)

Search by “Curriculum Type”

Example : Full Semester



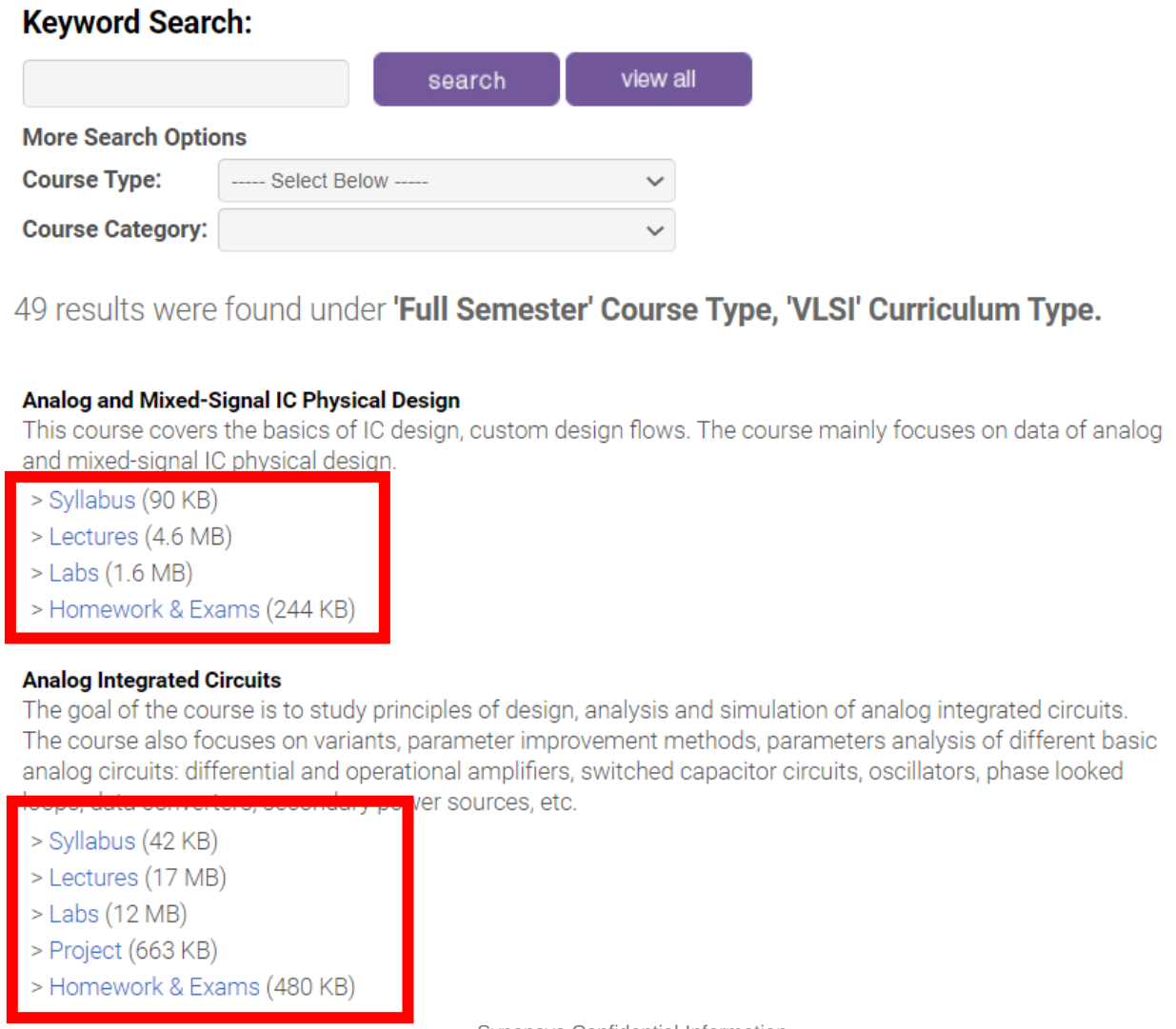
Curriculum Type:

1. EDA
2. VLSI

04 Access to the courseware

Start to download course syllabus, lecturer slides, labs or exams

Example : Full Semester



Course Contents:

1. Syllabus
2. Lectures
3. Labs
4. Project
5. Homework & Exams

Contents

- Membership Benefit
- Teaching Resources (courseware, generic libraries, PDKs)
- **Knowledge Base (SolvNetPlus)**

Knowledge Base

Knowledge Base 知識庫

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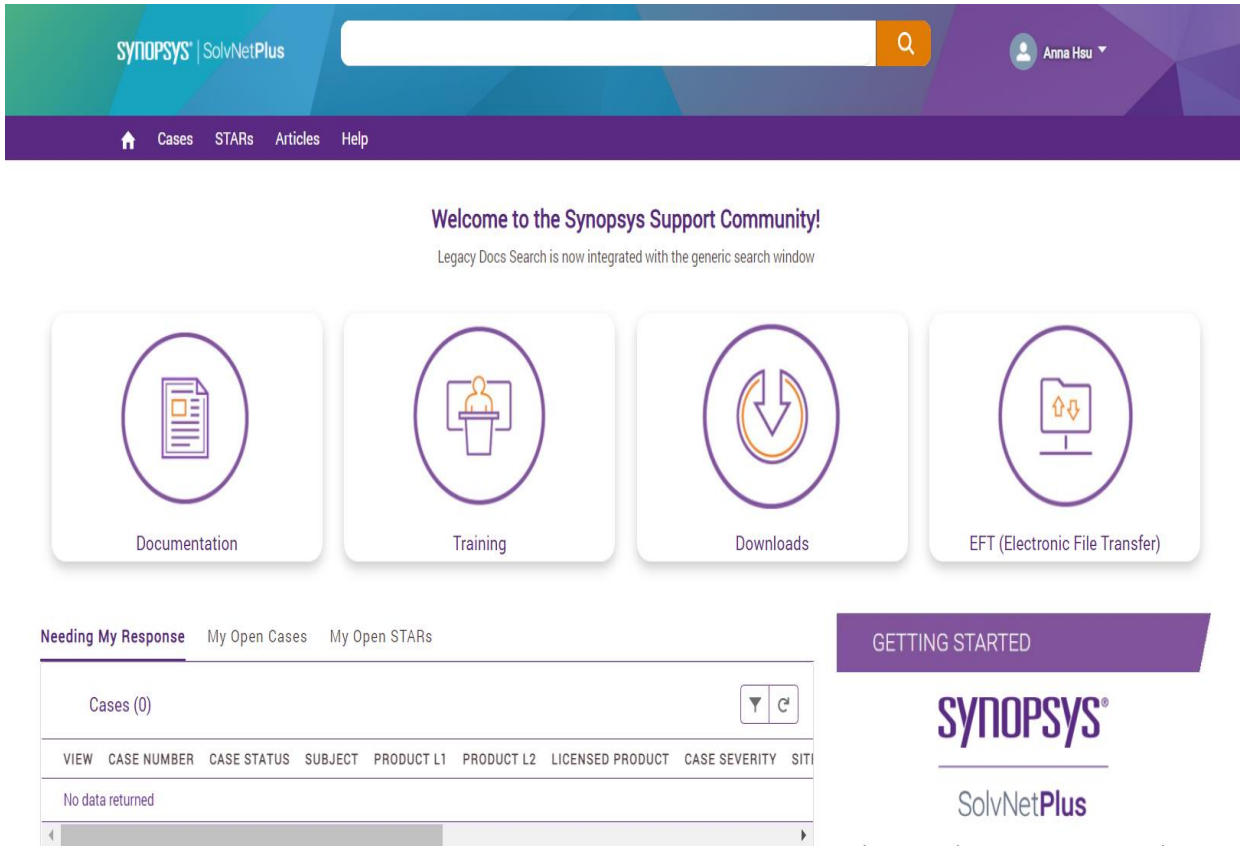
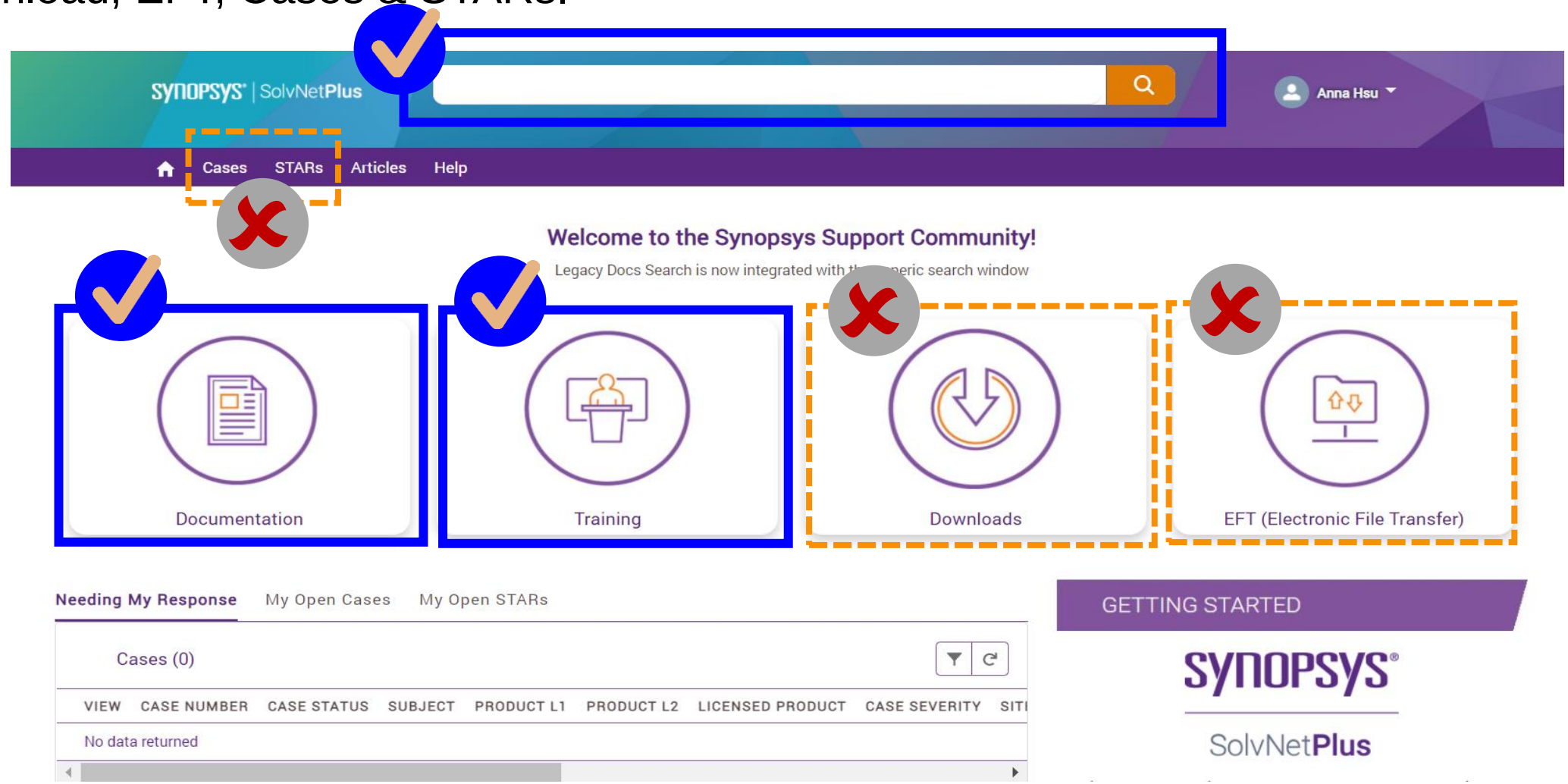


Knowledge Base

SolvNetPlus (Documentation, Training & Search)

Get Oriented with SolvNetPlus

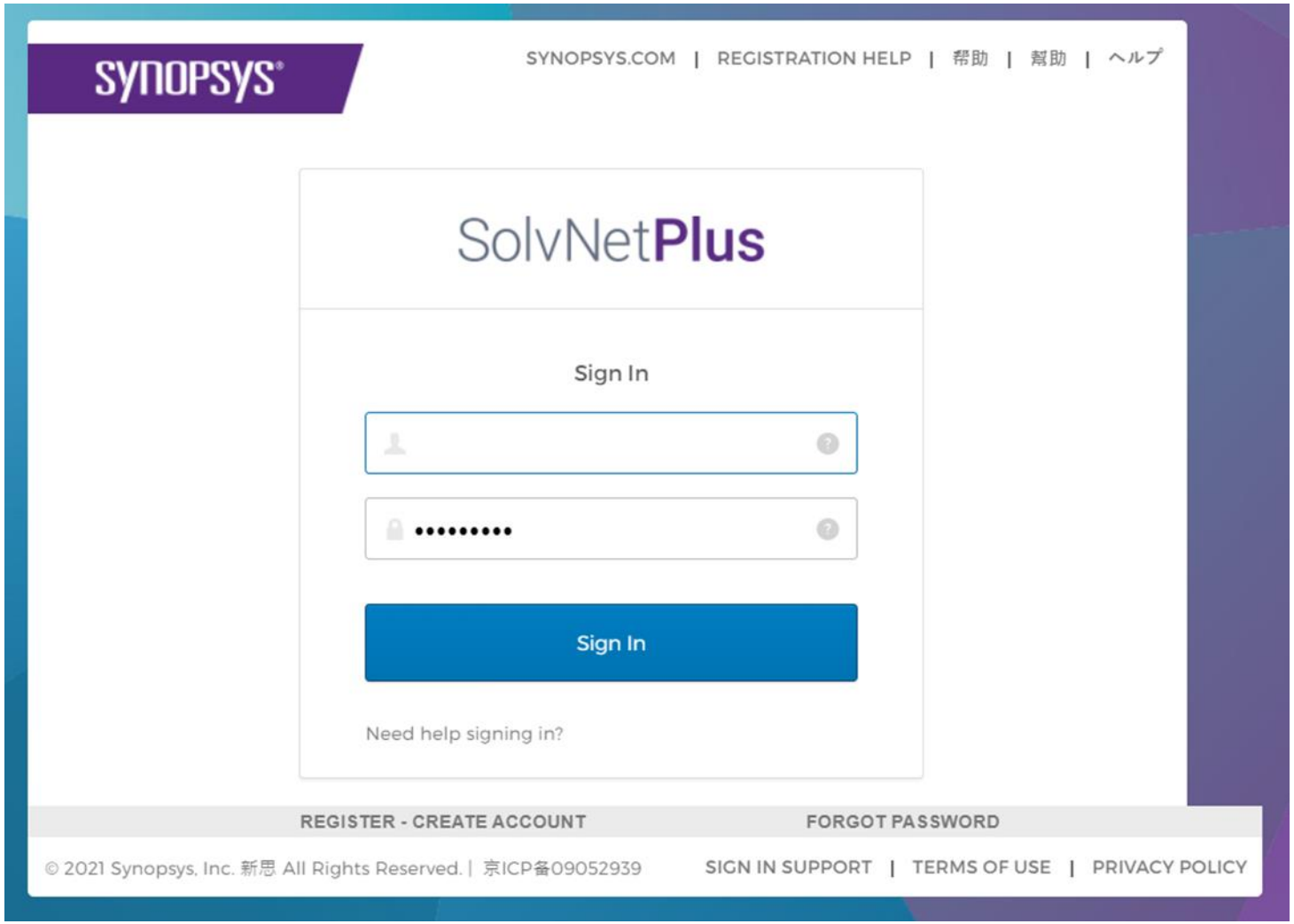
University users can access to Documentation, Training & Search ; but CANNOT use Download, EFT, Cases & STARs.



Get started w/ SolvNetPlus

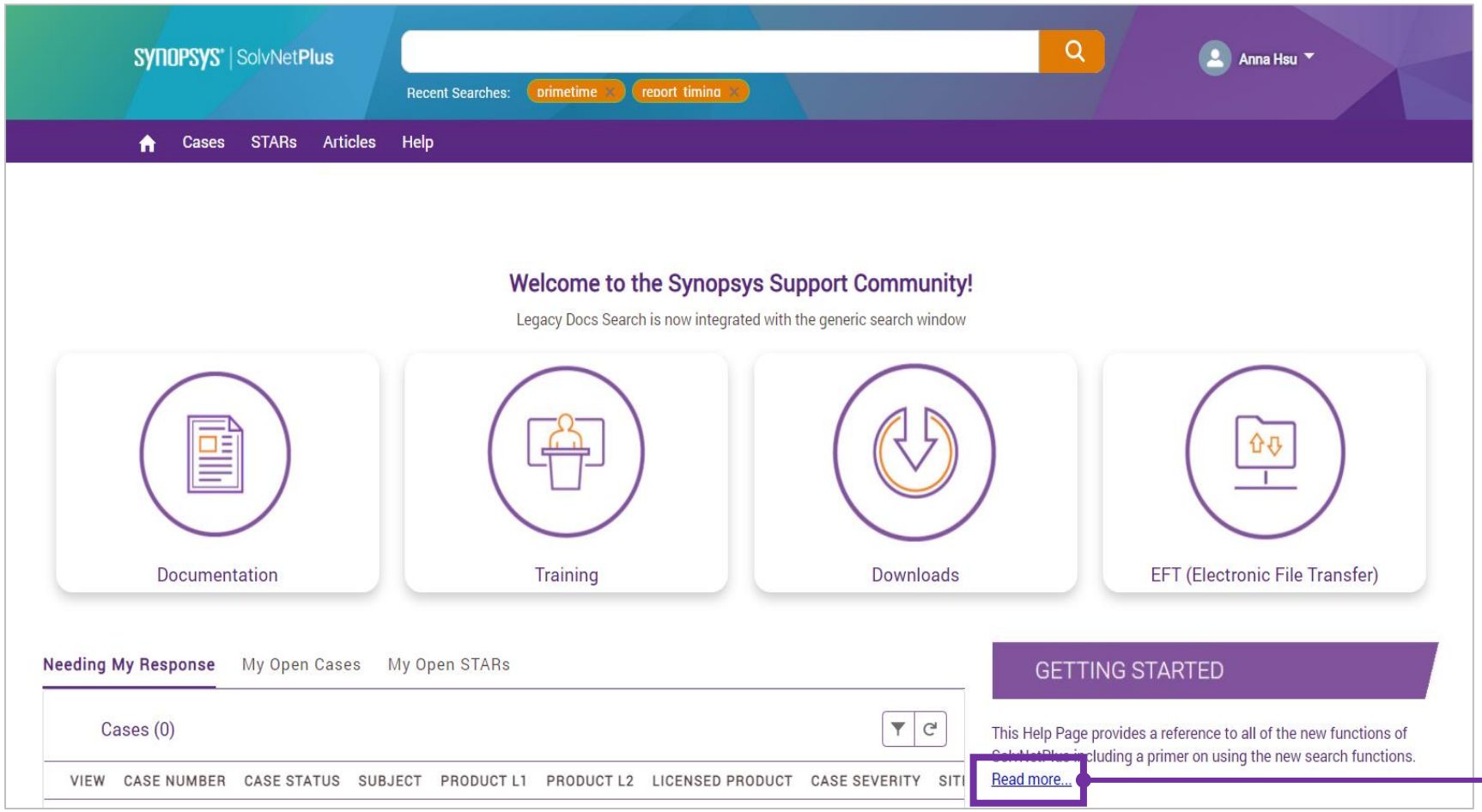
https://solvnetplus.synopsys.com/

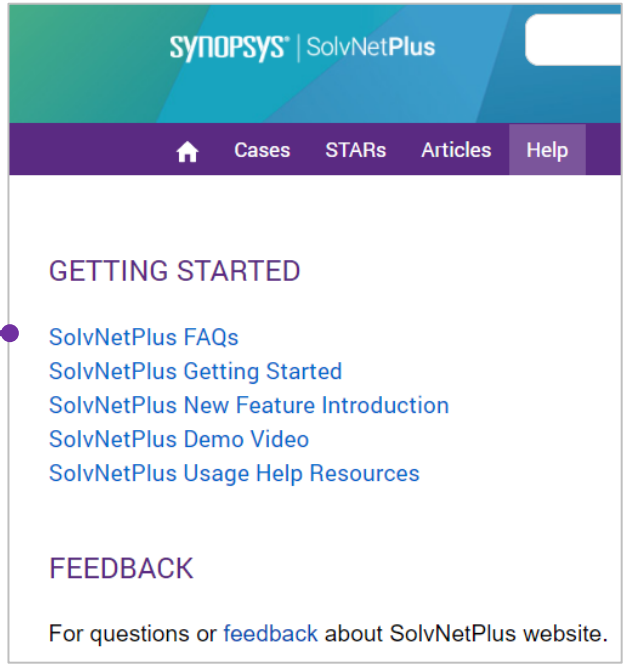
01 Log-in with Synopsys SolvNetPlus credential



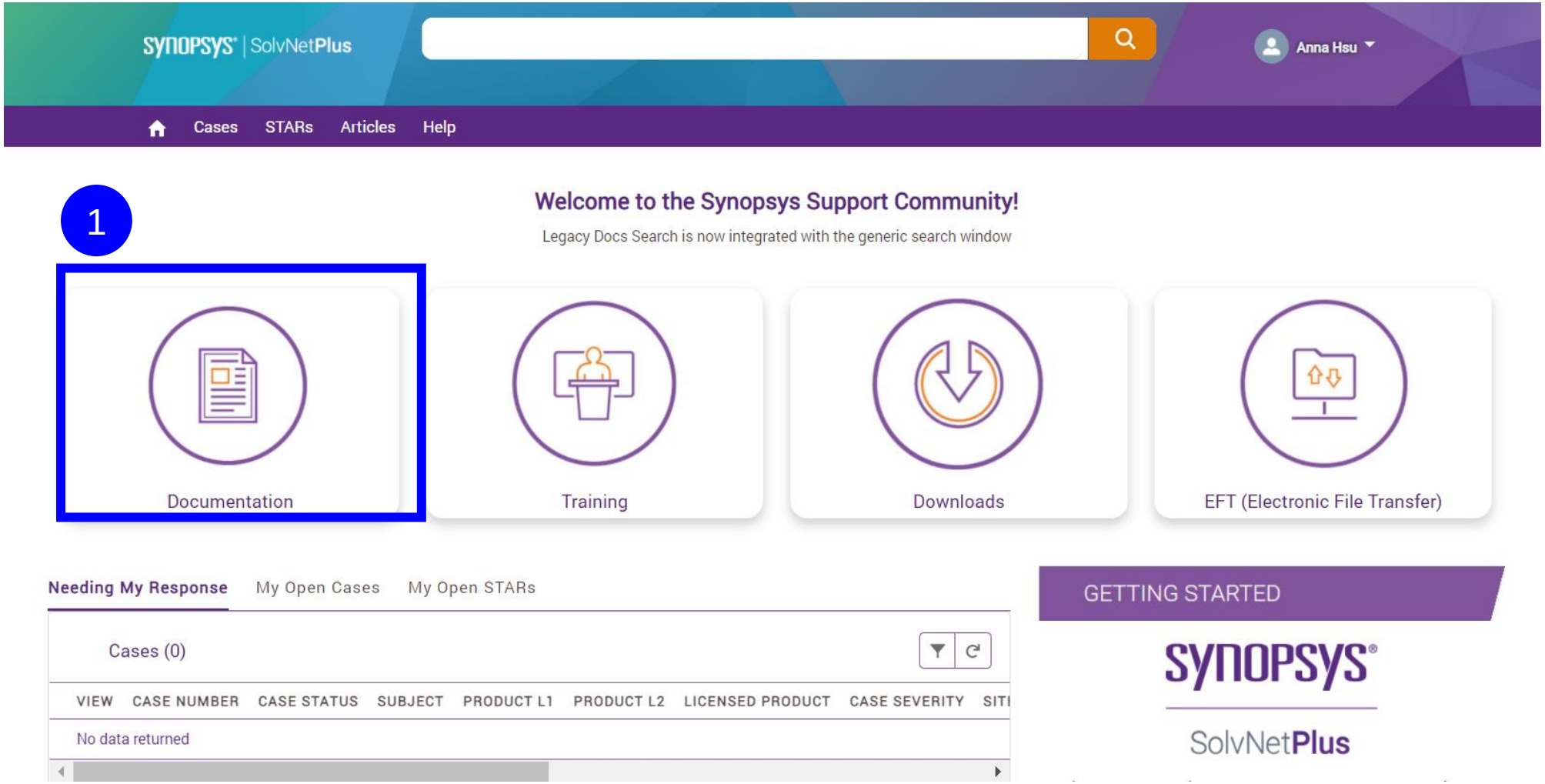
https://solvnet.synopsys.com/

02 Read “ GETTING STARTED” before use



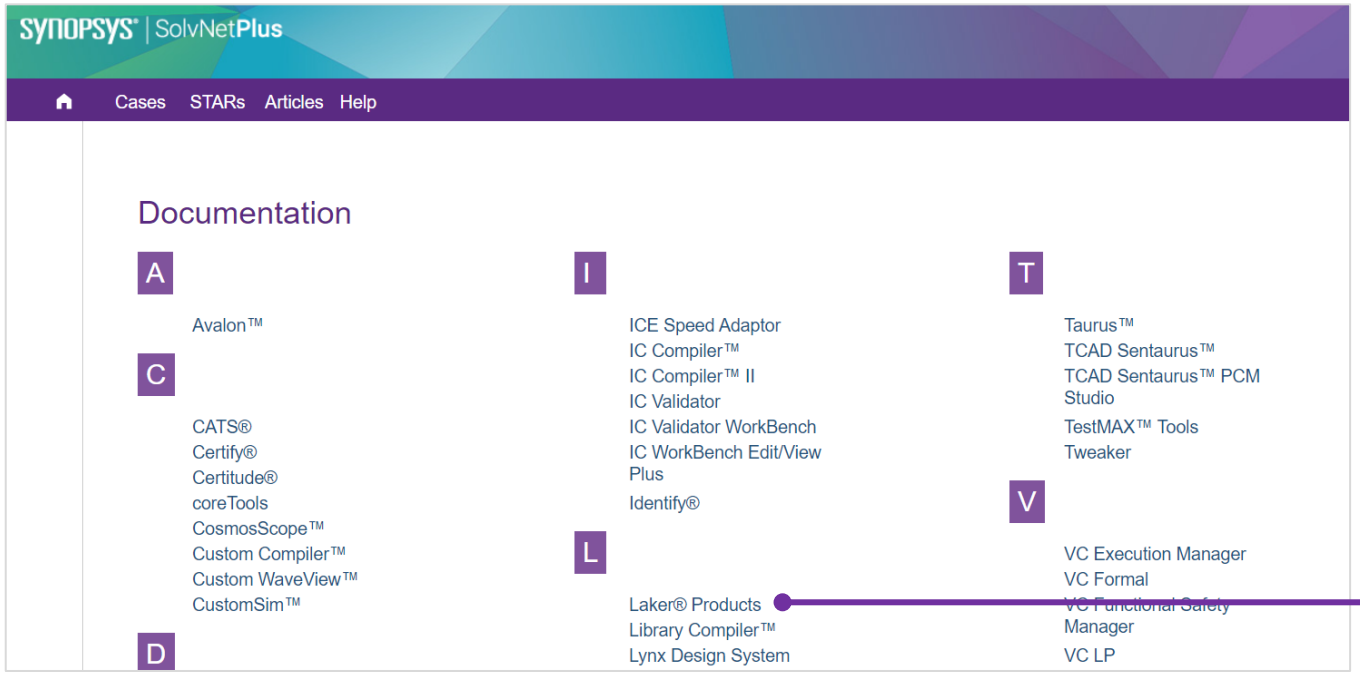


02 Click on “Documentation”



03 Search by product name to get tool documents

You can download release notes, installation guides & user guides and reference manuals from this section



Example : Laker

Laker

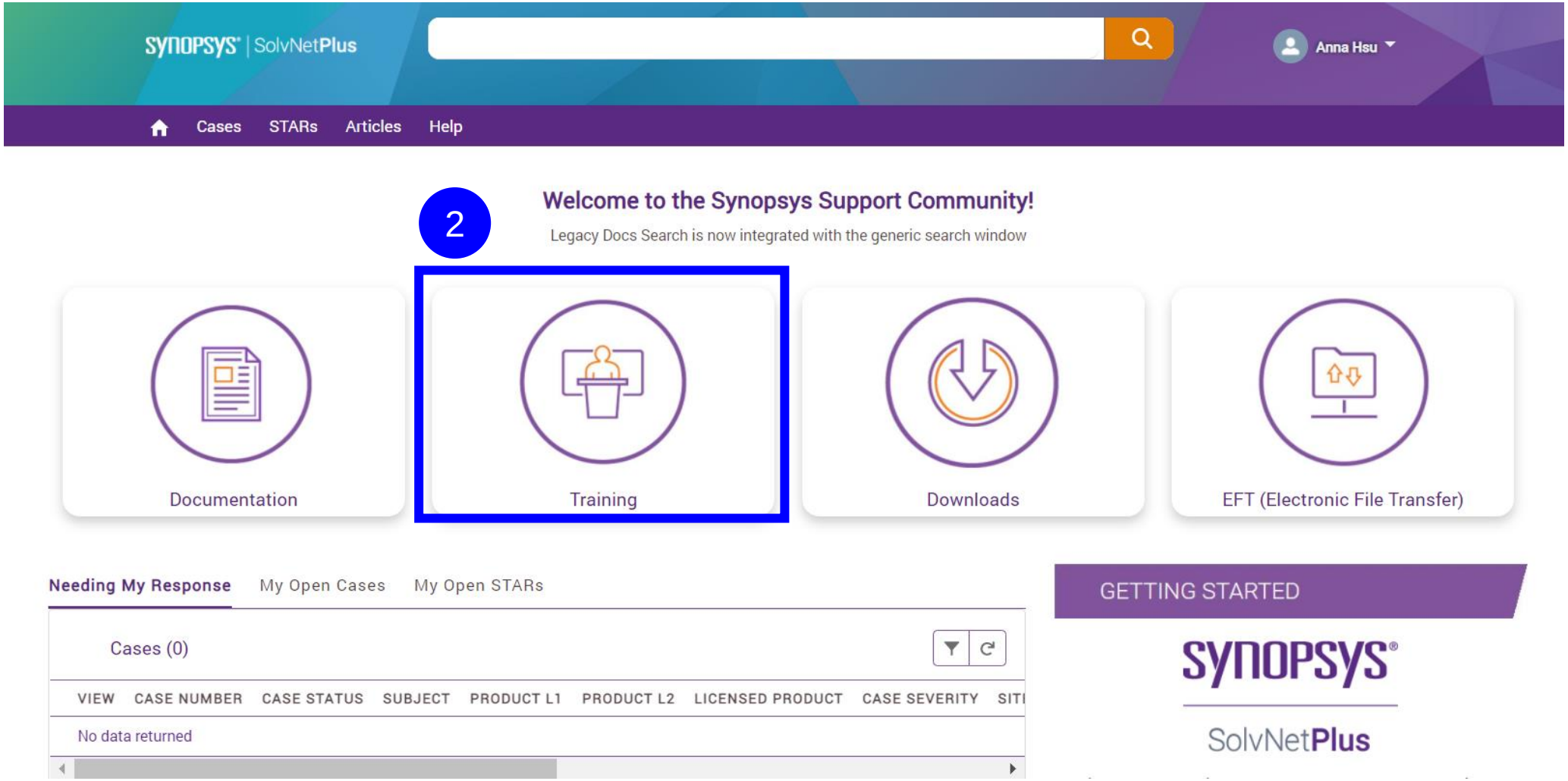
Laker3, L-2018.06, June 2018

- Laker3 Installation Guide
- Laker3 Quick Start Guide for Laker3 User Interface, K-2015.06, June 2015
- Laker3 Command Reference Manual, K-2015.06, June 2015
- Laker3 Tcl Reference Manual, K-2015.06, June 2015
- Laker3 Bind Key Summary
- Laker3 Menu Summary
- Laker DRD Tcl Command Reference, K-2015.06, June 2015
- Laker CDPR LEF/DEF Tutorial, 2013.02, February 2013
- Laker CDPR Data Preparation and SDL Tutorial, 2013.02, February 2013
- Laker3 Release Notes Version, L-2018.06-SP1 (January 2019)

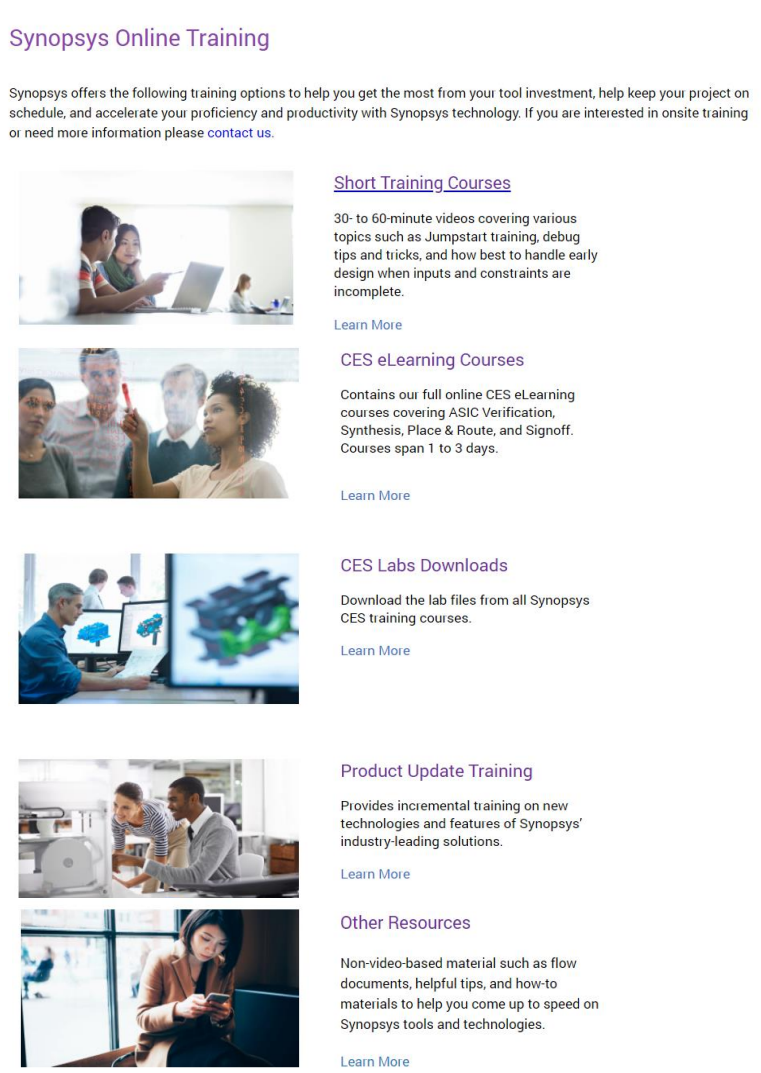
Laker, 2020.03, March 2020

- Laker User Guide and Tutorial, 2015.03
- Laker Command Reference, 2015.12
- Laker Tcl Reference, 2015.12
- Laker Bind Key Summary, 2015.12
- Laker Command Index, 2015.12

04 Click on “Training”



05 Select the training options that you need



- ***Short Training Courses –***
  - ✓ 30- to 60-minute videos
  - ✓ Covering various topics such as Jumpstart training, debug tips and tricks, and how best to handle early design when inputs and constraints are incomplete.
- ***CES eLearning Courses –***
  (*The courses are free to university users but require separate approval process. Please email chunhsu@synopsys.com if you plan to register CES courses)
  - ✓ Courses span 1 to 3 days
  - ✓ Contains full online CES eLearning courses covering ASIC Verification, Synthesis, Place & Route, and Signoff.
- ***CES Lab Downloads –***
  - ✓ Lab files from all CES training courses.
- ***Product Update Training –***
  - ✓ Incremental training on new technologies and features.
- ***Other Resources***

06 Click on “Short Training Courses”

Synopsys Online Training

Synopsys offers the following training options to help you get the most from your tool investment, help keep your project on schedule, and accelerate your proficiency and productivity with Synopsys technology. If you are interested in onsite training or need more information please contact us.

Short Training Courses

30- to 60-minute videos covering various topics such as Jumpstart training, debug tips and tricks, and how best to handle early design when inputs and constraints are incomplete.

Learn More

CES eLearning Courses

Contains our full online CES eLearning courses covering ASIC Verification, Synthesis, Place & Route, and Signoff. Courses span 1 to 3 days.

Learn More

CES Labs Downloads

Download the lab files from all Synopsys CES training courses.

Learn More

Product Update Training

Provides incremental training on new technologies and features of Synopsys' industry-leading solutions.

Learn More

Other Resources

Non-video-based material such as flow documents, helpful tips, and how-to materials to help you come up to speed on Synopsys tools and technologies.

Learn More

Title

Short Recordings

Description

Synopsys Online Training

Short Training Courses

Bitcoin Low Power Case Study

Custom Compiler Layout Editor eLearning

CustomSim – Static Circuit Check Training

Design Compiler – Jumpstart Training

Design Compiler NXT Key Features eLearning

DesignWare Cores ARC – ARC Processor Training

Formality – Jumpstart Training

Formality ECO eLearning

Formality – Ultra Training and Demonstration

Formality – Debugging Failing Verifications

Formality – Recognizing and Debugging UPF Issues

Fusion Compiler – Incomplete design handling

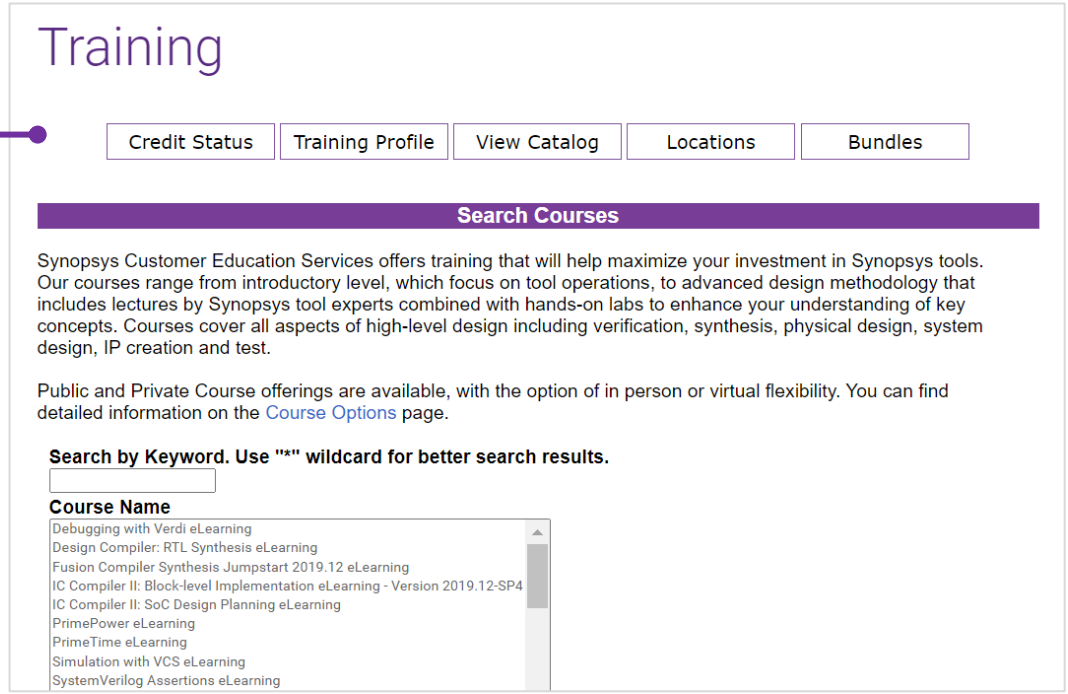
FineSim-Spice/Hspice - How simulation works?

IC Compiler II – Clock Tree Synthesis Unlocked

IC Compiler II – Jumpstart Training

07 Click on “CES eLearning Courses”

Please note that CES courses are free to university users, but to access the course, you need to submit a separate approval to Synopsys University Program. Please email chunhsu@synopsys.com if you plan to register.



08 Click on “CES Labs Downloads”

Synopsys Online Training

Synopsys offers the following training options to help you get the most from your tool investment, help keep your project on schedule, and accelerate your proficiency and productivity with Synopsys technology. If you are interested in onsite training or need more information please contact us.

Short Training Courses

30- to 60-minute videos covering various topics such as Jumpstart training, debug tips and tricks, and how best to handle early design when inputs and constraints are incomplete.

Learn More

CES eLearning Courses

Contains our full online CES eLearning courses covering ASIC Verification, Synthesis, Place & Route, and Signoff. Courses span 1 to 3 days.

Learn More

CES Labs Downloads

Download the lab files from all Synopsys CES training courses.

Learn More

Product Update Training

Provides incremental training on new technologies and features of Synopsys' industry-leading solutions.

Learn More

Other Resources

Non-video-based material such as flow documents, helpful tips, and how-to materials to help you come up to speed on Synopsys tools and technologies.

Learn More

Cases STARs Articles Help

Welcome to the Customer Education EST information page. This page has been created for workshop attendees looking to download the lab files of their recent workshop and/or for Customer System Administrators who need to download our lab files in preparation for a workshop.

Jul 24, 2020 • Knowledge

Title

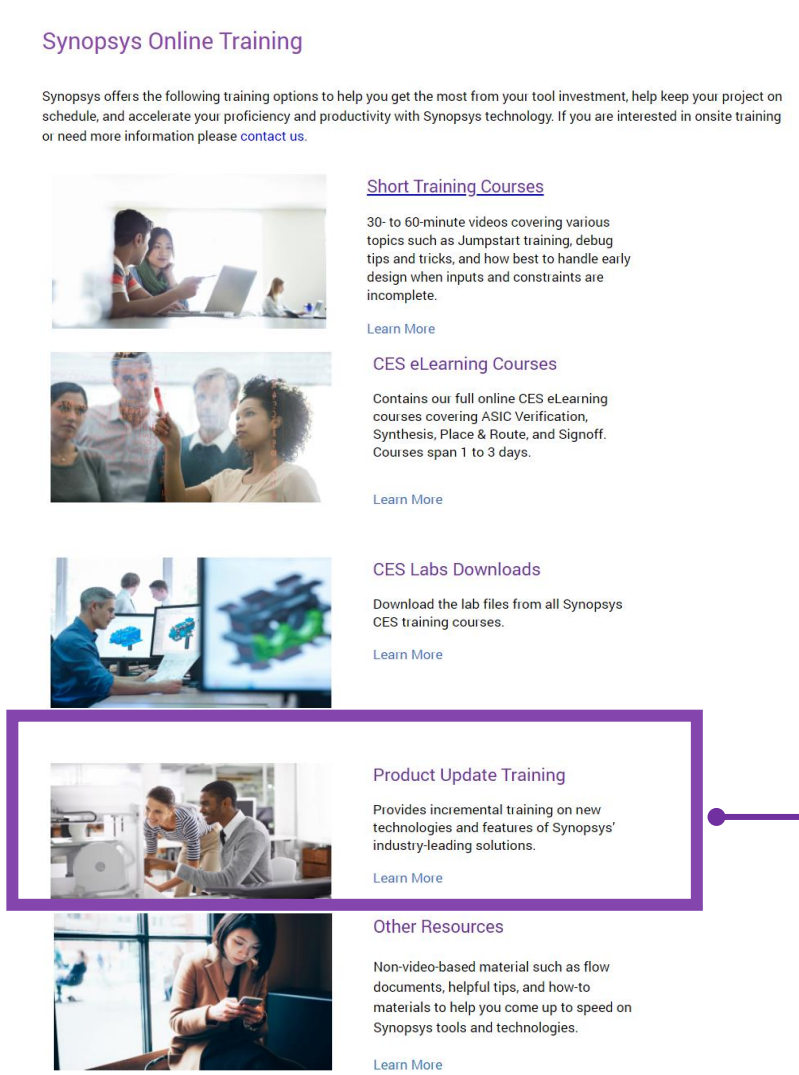
Electronic Software Transfer (EST) for Lab Files

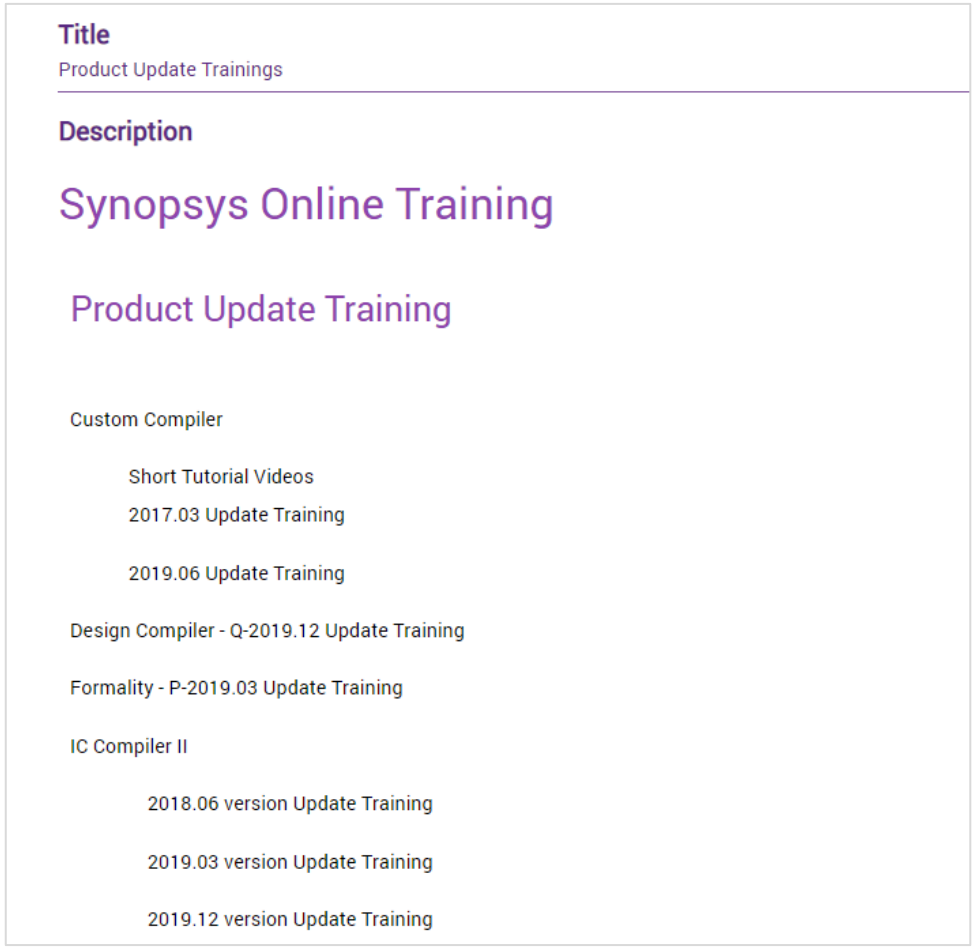
Description

These are lab script files only, they do not contain course presentation material or executable pieces of Synopsys code.

Workshop Description	Software Version	Location
Design Compiler	2016.12-SP3	Labs_DC_2016.12-SP3 Download
Design Compiler	2017.09-SP4	Labs_DC_2017.09-SP4 Download
Design Compiler NXT	2019.03-SP3	Labs_DCNXT_2019.03-SP3 Download
DFT Compiler	2017.09-SP3	Labs_DFTC_2017.09-SP3 Download
Fusion Compiler Frontend	2019.03-SP2	Labs_FC-FE_2019.03-SP2 Download
Fusion Compiler Synthesis	2019.12-SP3	Labs_FC-SYN_2019.12-SP3 Download
IC Compiler BLI	2016.03-SP1	Labs_ICC_BLI_2016.03-SP1 Download

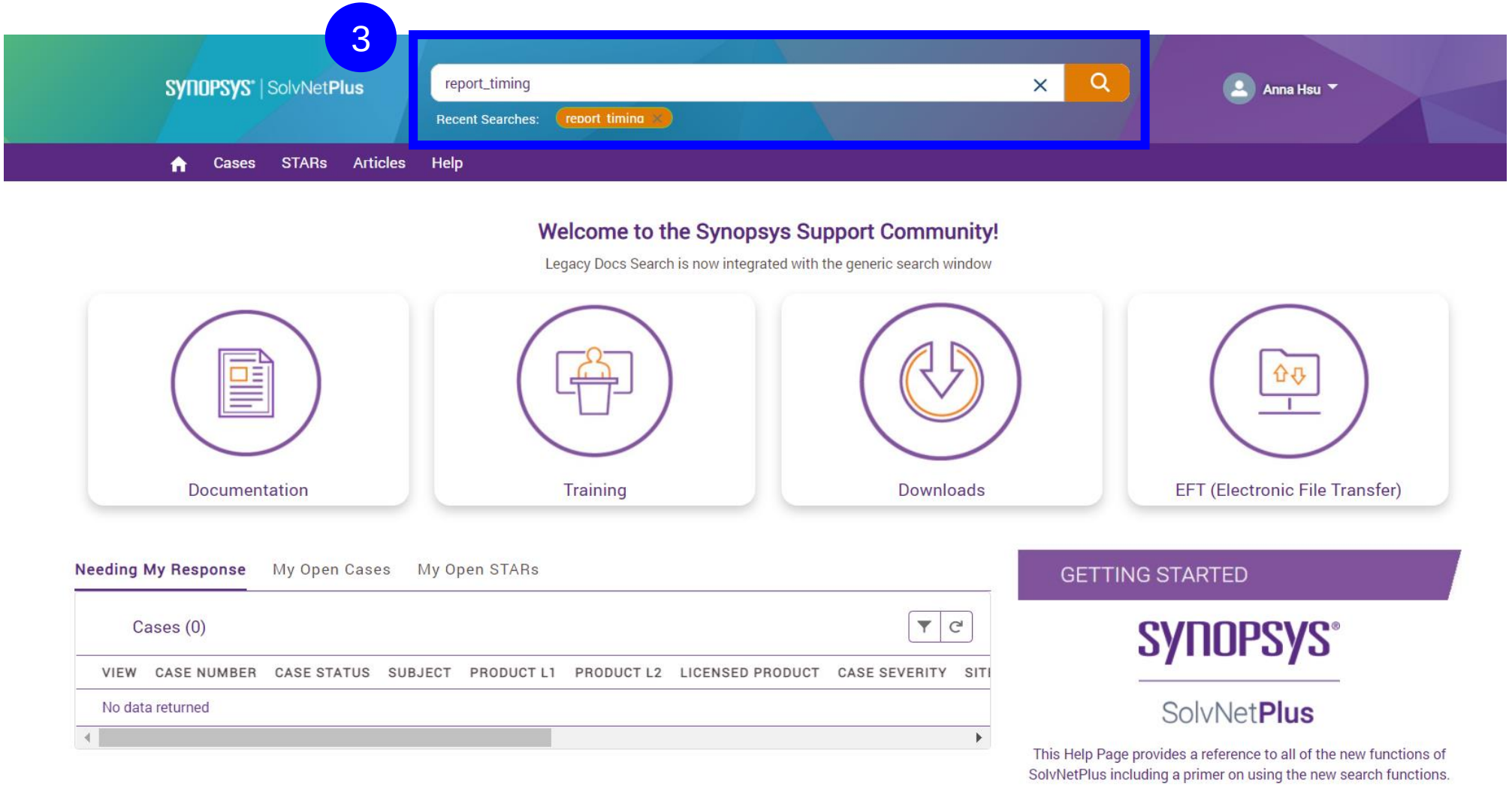
10 Click on “Product Update Training”





11 Look for information in the “Search” bar

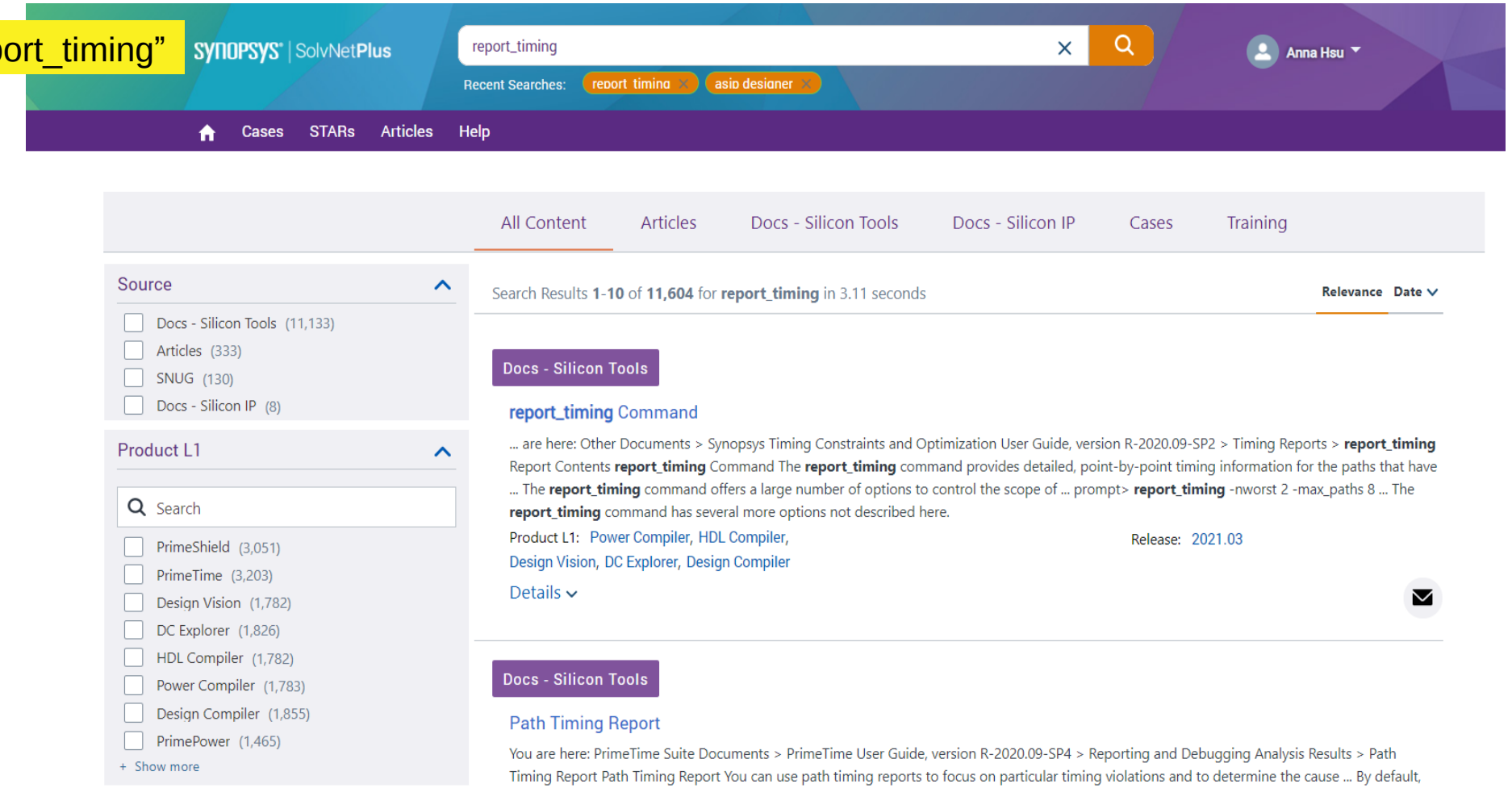
You can use search to retrieve information from various sources



12 Choose needed info from the displayed search results

The information will be displayed from various sources, such as documentation, articles, training, YouTube, and so on (but *NOT* in cases & STARs)

Example : insert “report_timing”



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Thank You

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