Quick Start Guide for testing the AD9652 Analog-to-Digital Converter (ADC) Engineering Evaluation Board Using the FPGA based Capture Board HSC-ADC-EVALCZ

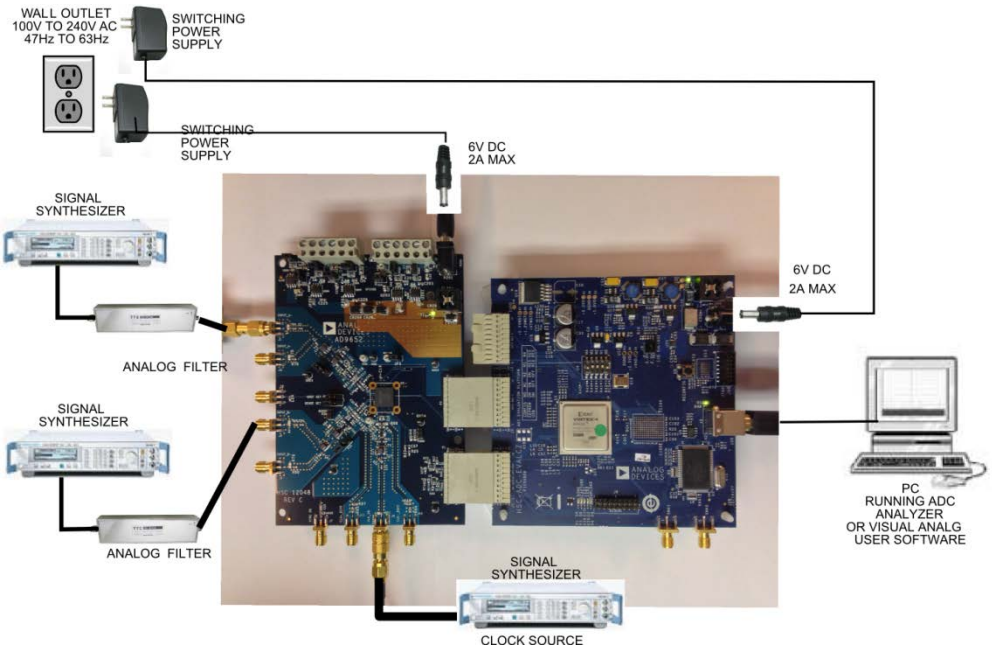


Figure 1: AD9652 Evaluation Board with HSC-ADC-EVALCZ Data Capture Board

Equipment Needed

- ► Analog signal source and anti-aliasing filter
- ► Analog Clock Source
- ► PC
- ► USB 2.0 port recommended (USB 1.1-compatible)
- ► AD9652 customer evaluation board with 6VDC, 2A AC adapter.
- ► HSC-ADC-EVALCZ FPGA Based Data Capture Board with 6VDC, 2A AC adapter.

Documents Needed

- ► AD9652 Datasheet
- ► VisualAnalog Converter Evaluation Tool User Manual, AN-905
- ► High Speed ADC SPI Control Software User Manual, AN-878
- ► Interfacing to High Speed ADCs via SPI, AN-877

Software Needed

- ► VisualAnalog
- ► SPIController

All documents and software are available at http://www.analog.com/fifo.

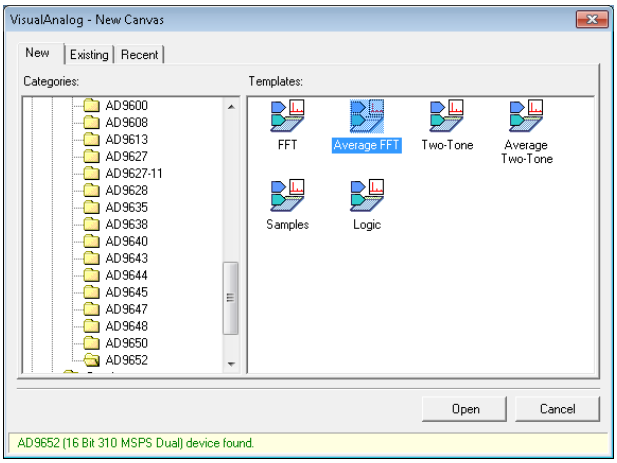
For any questions please send an email to highspeed.converters@analog.com**.**

Install software from the ADI website

1. Download and install VisualAnalog, Rev 1.9.45.21 or later.
2. Download and install SPI Control Software, Rev 4.0.4.4031 or later.

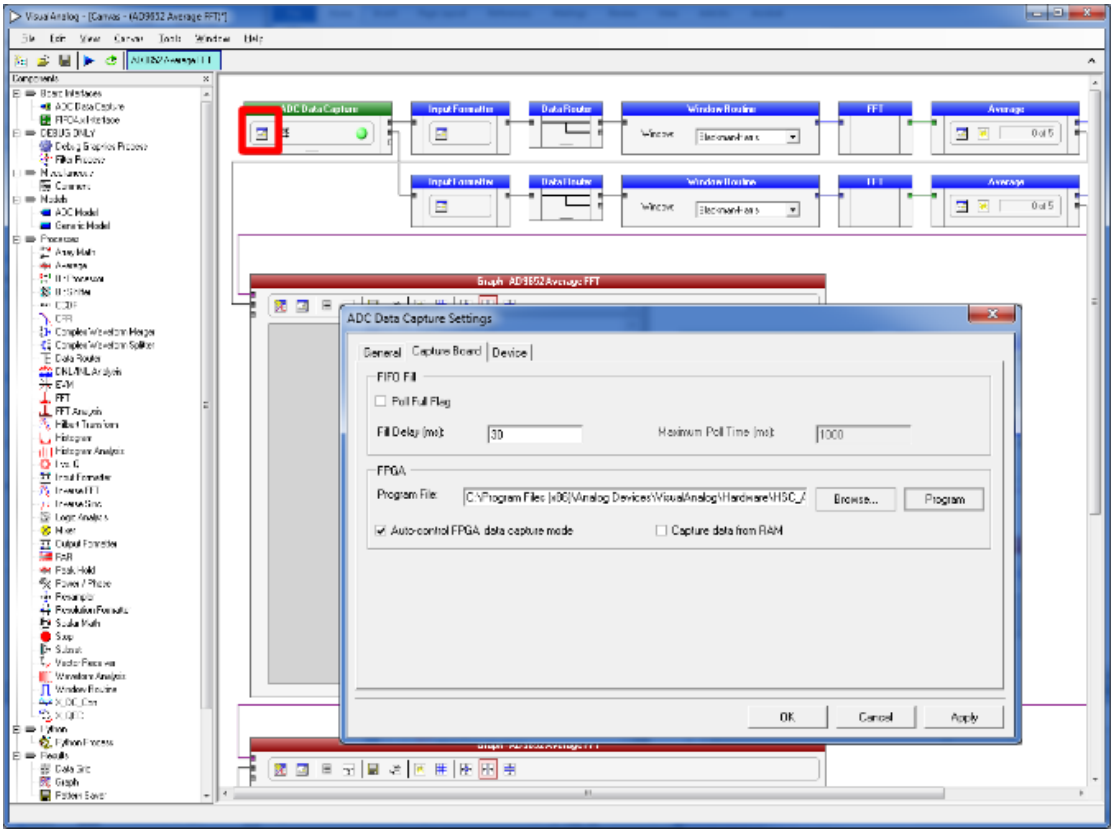
Setup hardware and software

1. Connect the AD9652 Customer evaluation board and the HSC-ADC-EVALCZ board together as shown in Figure 1. (Note these instructions are for Board HSC12048, Rev. C)
2. Connect one 6V, 2A AC Adapter to the HSC-ADC-EVALCZ board.
3. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable. (Connect to J6)
4. Verify Jumpers on the AD9652 evaluation board:
    a. Place Power supply jumpers: P204, P13, P206, P5, P205, P9, P209, P202
    b. Disable Amp: P16 and P31, jumper pins 1&2
    c. P15 jumper pins 2&3
    d. JP3 jumper should be installed
5. Connect power to the AD9652 Evaluation board using the provided 6V switching wall mount AC/DC power supply adaptor.
6. On the ADC evaluation board, provide a clean, low jitter clock source to connector J6 at the desired ADC conversion rate. Note: The AD9652 has an input clock divider circuit which allows generators to drive a higher frequency clock, for this case apply the high frequency clock to J6 and program the proper divide using SPIController when it is used in a later step. The input clock level should be between 10dBm and 16dBm.
    a. For the AD9652 evaluation board number 12048 Rev C, the Clock Duty Cycle stabilizer should be disabled when using an input clock above 620 MHz.
7. Open VisualAnalog on the PC. “AD9652” should be listed in the status bar of the “New Canvas” window. Select the template that corresponds to the type of testing that you are performing, commonly “Average FFT”.

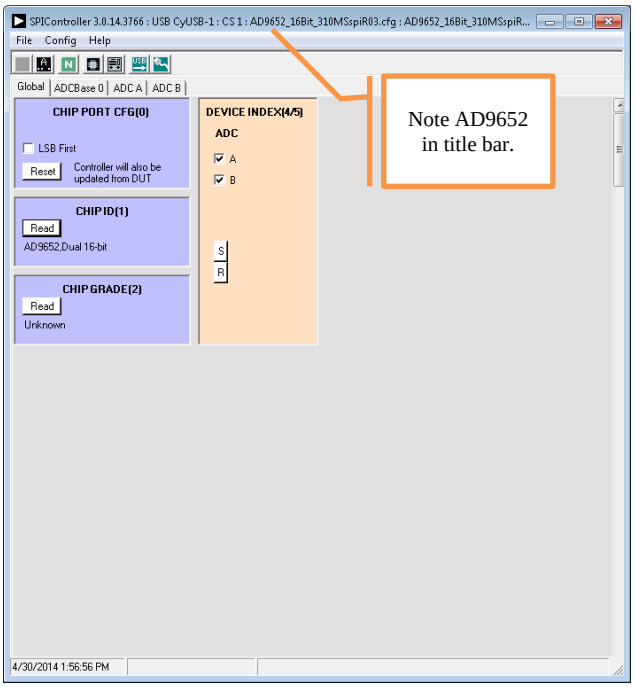


8. If an error occurs during the automatic loading of the FPGA program file, the program can be loaded manually.

a. To load the FPGA program manually, select the ADC Data Capture Settings window and click on the 'Capture Board' tab (see the red box in the figure below). In the FPGA box select the program "AD9652_fifo5.bin" to configure the FPGA. After selecting the file, click the "Program" button to download the file to the FPGA. The 'DONE' LED (D6) should illuminate on the HSC-ADC-EVALCZ board indicating that the FPGA has been correctly programmed.



9. Next open the SPI Controller software. Note that pressing the Read button in the CHIP ID(1) box, the field should report the AD9652 if it is connected properly.



10. By default the AD9652 is configured for 2.5 Vpp input of 155 MHz or less. The ADCBase 0 tabe can be used to change both of these settings.

11. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the analog input at connector J1 (Channel A) and/or J4 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (ADI uses TTE, Allen Avionics, and K&L band-pass filters.) In order for the input level to be near the ADC's full scale, the generator level should be set to around 12dBm; this level depends on the input frequency and any losses in bandpass filters.

12. Click the Run button ( ) in VisualAnalog.

13. Connect or enable the input signal and adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the "Fund Power" reading in the left panel of the VisualAnalog FFT window.)

14. If desired, click on File>Save Form as in the FFT window to save the FFT plot.

Troubleshooting

► *The FFT plot appears abnormal...*

- ✓ If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce input level if necessary.
- ✓ In VisualAnalog, Click on the Settings button in the "Input Formatter" block. Check that "Number Format" is set to the correct encoding (2's compliment by default).

► *The FFT plot appears normal, but performance is poor.*

- ✓ Make sure you are using an appropriate filter on the analog input.
- ✓ Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- ✓ If you are using non-coherent sampling, change the analog input frequency slightly.
- ✓ Make sure the SPI config file matches the product being evaluated.

► *The FFT window remains blank after the Run button is clicked.*

- ✓ Make sure the evaluation board is securely connected to the HSC-ADC-EVALDZ board
- ✓ Disconnect power from both the ADC evaluation board and the HSC-ADC-EVALDZ board, disconnect the USB cable from the HSC-ADC-EVALDZ board and begin again at Step 1.
- ✓ Make sure the FPGA has been programmed by verifying that the 'CONFIG_DONE' LED is illuminated on the HSC-ADC-EVALDZ board.
- ✓ Make sure the correct FPGA program was installed.

► *VisualAnalog indicates that the "FIFO capture timed out."*

- ✓ Make sure all power and USB connections are secure.
- ✓ Double check that the encode clock source is present at connector J505.

AD9652 Revision: 0 April 30, 2014