

Radiation Effects on Advanced Flash Memories†

D. N. Nguyen, S. M. Guertin, G. M. Swift and A. H. Johnston

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

Abstract

Radiation tests of advanced flash memories including, multi-level flash technology, are compared with results from previous generations. Total dose failure levels are comparable to or lower than those of older technologies, but are likely still caused by degradation of the internal charge pump. Small numbers of read errors were observed during single event tests of the multi-level devices that appear to be caused by shifts in the sense amplifier detection levels or cell threshold shifts and rather than loss of electrons off the floating gate.

I. INTRODUCTION

A. Basic Cell Architectures

Two basic approaches have been used to develop high-density flash memories. The NOR structure, shown in Figure 1, provides direct access to individual cells. This simplifies the overall device architecture, but increases cell area because of the need for contacts at each drain and source connection. The NOR structure is used by Intel. It requires voltages of about 12 V for erasing and writing.

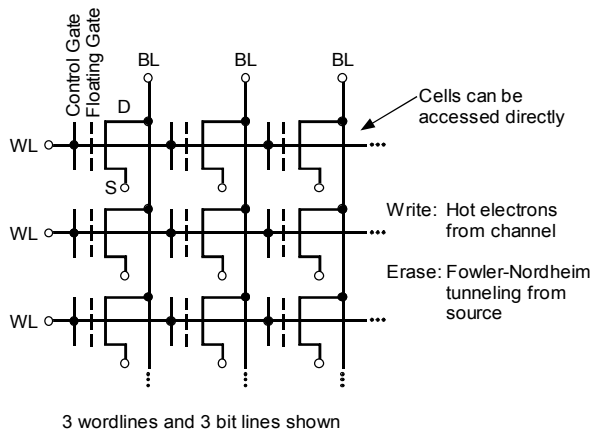


Figure 1. Cell architecture of a NOR flash memory.

The second approach uses the NAND structure, as shown in Figure 2. The NAND cell is more compact because it does not provide contacts to individual source and drain regions. However, cells in the NAND structure require reading and writing through the other cells in the stack, an architecture that results in inherently slower cell access. Cells in the NAND structure require higher voltages -- typically 20 V -- for erasing and writing than the ~12V of the NOR structure.

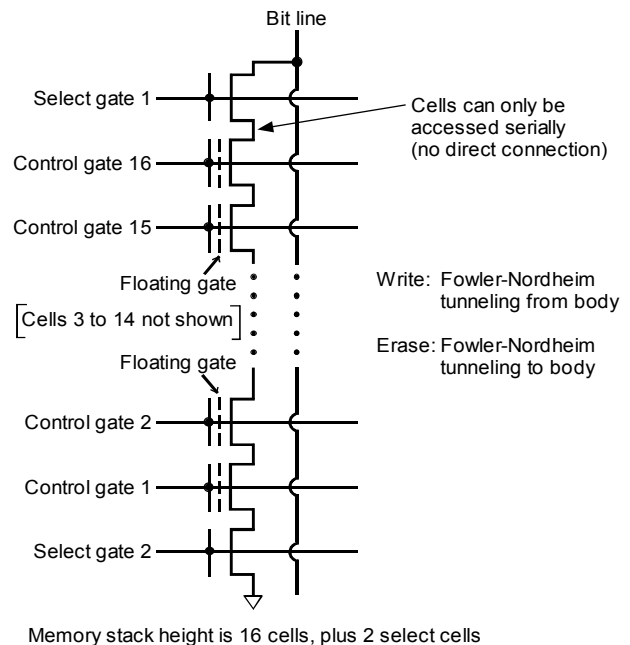


Figure 2. Cell architecture of a NAND flash memory organized in 16-bit stacks.

The overall architecture of either type of flash memory is very complex. Reading can be done relatively rapidly for either cell architecture using conventional circuitry for access and readout. However, erasing and writing are very slow operations (on the order of milliseconds) compared to conventional memories. To overcome this limitation, flash memories are subdivided into blocks, allowing erasing and writing to be done at the block level. Internal registers and buffers provide temporary storage for pages of data, allowing more transparent interface. A write state machine and a command state machine are used to control the complex sequences of operations that are needed. A charge-pump circuit is also required in order to provide the high internal voltages that are needed for erase and write operations.

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Because of this complexity, flash memories cannot be treated as simple memories. It is quite challenging to determine how they respond in radiation environments.

B. Advanced Flash Memories Considered in the Present Paper

Flash memories have evolved rapidly in recent years. New design techniques such as multilevel storage have been proposed to increase storage density in the NOR structure [1,2] and are now available commercially. Figure 3 compares threshold voltage distributions for single-level and three-level technologies [3]. To implement multi-level storage, special circuitry must be added to allow the amount of charge stored in the floating gate to be controlled within narrow limits during the writing, and also to detect the different amounts of charge during reading. This imposes tougher requirements on the analog circuitry; the sense amps must discriminate between the four threshold regimes and the programming circuits must deliver precise amounts of charge to the floating gate.

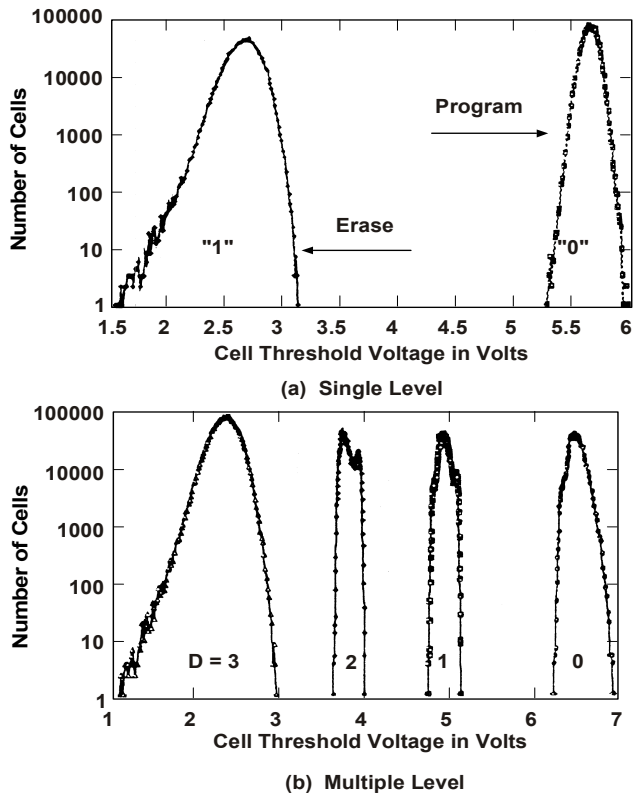


Figure 3. Comparison of cell threshold voltage distribution for single- and multi-level flash memories.

Two Intel devices that use multi-level flash architecture were selected for radiation testing: the 28F320 (32Mb) and the 28F640 (64Mb). Both parts operate with a 5-volt external power supply (although they have 3.3V I/O option). An internal charge pump is used to generate the higher voltage

required to erase and write the memory, typically 12 V for NOR flash devices.

Not all advanced flash memories use multi-level storage. The NAND architecture, which allows access only at the column level (similar to a shift register) [4], takes less area, and is easier to scale to higher densities. A Samsung 128Mb device, KM29U128, was also selected for radiation testing to compare the two architectures. The Samsung device uses a 3.3V power supply. It also uses an internal charge pump. Higher voltages are required for erasing and writing (20V). Note that the cell “stack” in this technology contains 18 transistors, which greatly increases the sensitivity of the circuit to small changes in threshold voltage.

Comparing the selected test devices specifications is revealing. As shown in Table 1, the Intel NOR devices have a much larger erase granularity and time. Indeed, the Intel 64Mb device requires 45 seconds to erase all the bits (using “typical” specifications), but the Samsung 128Mb requires only two seconds. Further, the Samsung specification allows an order of magnitude more cycles, although it may start with some bad blocks. The Intel NOR devices boast a much faster random read cycle time of 150 and 100 ns for the 64Mb and 32Mb, respectively, versus over 10 μ s for Samsung. In fairness, reading sequentially at maximum speed through an entire device takes about the same time, approximately 1.2 s, and Intel sequential writing speeds are about six times slower at 6.1 μ s per byte. It is understandable that the lower internal voltage in the Intel devices makes erasing and writing slower. It also appears to require more current, specifying 70, 60, and 55 mA for erase, write, and read for the Intel’s versus 20 mA for all modes for the Samsung.

Table 1.

Comparison of Block Characteristics

	# of Blocks	Block Size (bytes)	Block Erase Time	Max. Erase Cycles	Initial Bad Blocks
Intel 64Mb *	64	128k	0.7 s	10^5	none
Samsung 128Mb	1024	16.5k	2 ms	10^6	≤ 20

* Intel 32Mb identical, except half the blocks.

Total dose studies of earlier devices implicated the charge pump circuitry as usually responsible for device failures in both technologies [5]. This was clearly demonstrated for the 16Mb Intel NOR device where the erase/programming voltage could be externally supplied; much higher dose levels were achieved when the internal charge pump was not used. It is less clear that the charge pump is also the weakest link for the 16Mb Samsung NAND device, but it is the most likely possibility, given the even higher required voltages for erasing and programming.

Interpretation of heavy ion tests in modern flash memories is rather difficult because of the very involved architecture and internal state machine. Heavy ion tests in earlier studies

found no fundamental cell upsets; however, apparent upsets in the most complicated device were attributed to buffer and register upset [6]. Upset in both technologies occurred in the microcontroller and register regions, causing complex errors at the block level, as well as address errors. These errors are very difficult to categorize because of the many different internal operating conditions. Some types of single-event errors produced internal conditions that require power cycling in order for the memory to resume normal operation. Some high current modes, occasionally destructive were seen in Intel devices. Interestingly, a few stuck bits (19) were detected in a Samsung 16Mb device, but none occurred in the 32Mb; these “stucks” could not be erased or written over, but did anneal and rebound. Single-event tests in the present study were more limited in scope, and concentrated on determining whether the same general types of functional errors occurred in newer flash memories as well as investigating the possibility of stuck bits or other permanent types of errors.

II. TOTAL DOSE TESTING

A. Experimental Procedure

In evaluating flash memories for use in space, it is important to recognize how they will be used. Read mostly applications such as code storage (replacing PROMs) are natural fits because of the very slow write and erase time. In these applications they might not be powered except for brief periods when it is necessary to read their contents. Although many different bias and use conditions are possible (including continuous erase-write-read modes), the devices in this work were irradiated in either of two bias conditions: (1) static biased, where the device is powered, but no address cycling or data access operations are used; and (2) unbiased (all pins grounded). If the radiation tolerance is deemed acceptable by NASA flight projects, additional irradiations with more severe operational conditions (erasing and programming) will be undertaken at a later time.

Total dose tests were done using the JPL cobalt-60 test facility at either of two dose rates: 25 rad(Si)/s and 0.012 rad(Si)/s using a series of stepped irradiations.

Measurements were made after each irradiation step with an Advantest test system. For some devices post-irradiation measurements were limited to the “read” mode, making no attempt to verify operation of either the erase or write function of the memory. That simplified evaluation condition was selected because many applications require very infrequent writing, and are more concerned with how stored patterns in the memory can be read out after irradiation.

Other devices were tested more completely after each irradiation level, subjecting each device to a complete erase-write-read cycle (note that in the flash technology is necessary to first erase the memory array before writing it). This tests the full functional capability of the memory, and requires that the charge pump and verification circuitry function correctly.

Parts were programmed with a non-repeating pattern generated by a linear congruential pseudo-random generator with a slight modification: discarding every 31st number. The algorithm produces a reproducible random sequence of states, starting with a “seed” number. Two seeds were used, 31 and 59, which are both prime numbers. When the second seed is used, the pattern developed by the algorithm produces the opposite state in 1/2 the bits used with the first seed. This tests the ability to program the opposite state in 1/2 of the bit locations after each irradiation. These complex patterns are the basis of a more comprehensive functionality check which is capable of detecting address or decoding errors, unlike simple patterns (such as a checkerboard pattern).

Before the first irradiation, the devices were written with a random pattern (seed-31). The pattern was verified by reading the contents of flash devices before and after each irradiation level for all parts that were evaluated in the “read” mode. Stand-by current tests were also measured after each radiation step.

For full functional mode (EWR tests), the devices were erased and a new random pattern (seed-59) was written to the memory after the first level. After the second level the original pattern (seed 31) was used, interchanging each pattern after each irradiation step in order to verify that a different pattern could be written into each storage location.

The results presented in the following figures show the response of only one representative test sample for each irradiation condition. Many of the conditions were repeated with negligible differences in the results; one was repeated for six samples from two date codes. As one might suspect for a necessarily tightly controlled commercial process, part-to-part differences in total dose response are small. Only one ‘maverick’ failure mode was ever encountered at a slightly lower dose level: one 128Mb device (of 23 tested) demonstrated a large increase in block reading time from seconds to minutes.

B. Intel Multi-Level Flash Devices

1) Results for Read Mode

Figure 4 shows test results for the 32-Mb Intel multi-level flash memory for statically biased and unbiased conditions. With bias applied, the standby current increased slightly during irradiation. The device would no longer function after the second irradiation level [12 krad(Si)]. When tested without bias, the device continued to operate at somewhat higher levels. After 16 krad(Si) approximately 3,500 bits failed (a small fraction of the total number of bits). Thus, the first versions of the multi-level flash technology failed at lower levels than the earlier generation devices (16 Mb at about 25 krad(Si) in EWR mode) that did not use the multi-level technology [5].

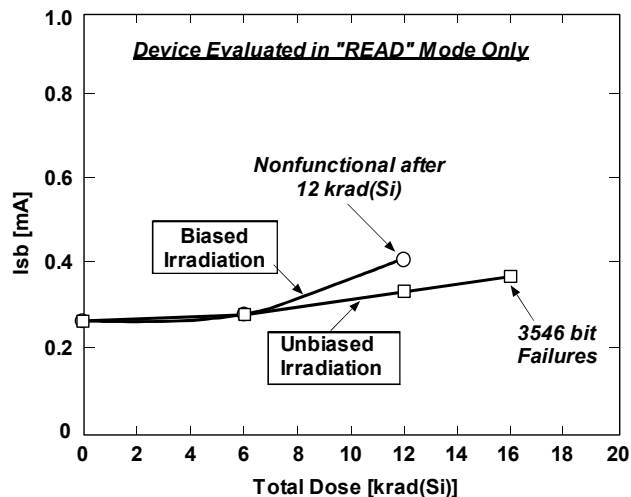


Figure 4. Total dose test results for the Intel 32Mb flash memory evaluated in read mode (I_{sb} spec limit is 0.9 mA).

The 64-Mb multi-level flash memory behaved somewhat differently. The standby current increased much more rapidly with increasing radiation levels when bias was applied compared to results for the 32-Mb devices in Figure 4. The 64-Mb devices typically operated to levels well above 20 krad(Si). Failure occurred in only a small number of cell locations even though the power supply current increased by more than an order of magnitude. These results are shown in Figure 5.

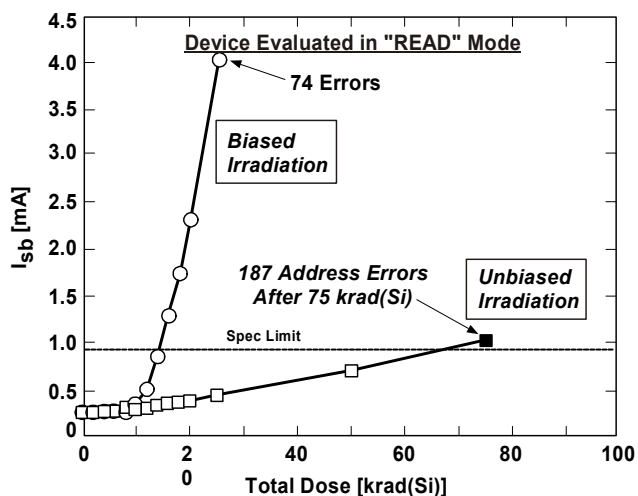


Figure 5. Total dose results for the Intel 64-Mb flash devices evaluated in read mode.

When tested without bias, the 64-Mb devices passed read functionality up to 50 krad(Si) and showed only slight increases in standby current. However, at 75 krad(Si) a large number of addressing errors occurred. These were severe enough to make the device unusable.

2) Results for Erase-Write-Read Mode

Test results for the 64-Mb Intel device in the fully operational mode (EWR) are shown in Figure 6. When irradiations were carried out under bias, the device became fully nonfunctional at 11 krad(Si), in contrast to the tests in "read" mode where the device continued to operate with only a few errors to levels almost twice as great (see Figure 5). Without bias, the device also failed at much lower levels when fully operational tests were done between irradiations. Small numbers of write errors occurred between 30 and 40 krad(Si). Three write errors were also observed at 15 krad(Si), but were not present at the next irradiation level.

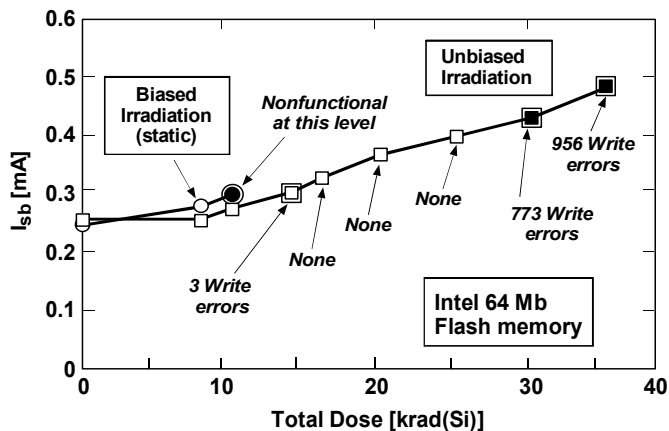


Figure 6. Total dose test results for the Intel 64Mb flash memory evaluated in full functional mode.

C. Samsung NAND Technology

1) Results for Read Mode

Test results for the 128-Mb Samsung devices in the "read" mode are shown in Figure 7. With biased irradiation, the standby current increased by several order of magnitude at about 20 krad(Si). When tested without bias the device functioned to levels above 100 krad(Si) with only a small number of "read" errors. Errors of this type could be easily accommodated in most applications with basic error-detection-and-correction techniques.

2) Results for Erase-Write-Read Mode

With full functionality tests between successive irradiation levels, erase-mode failures were observed at 8 krad(Si) under bias irradiation as shown in Figure 8. Older technology devices from Samsung behaved quite similar when tested in this mode, failing in E/W/R mode at approximately 10 krad(Si) [5]. This corresponded closely with the total dose level where the standby current started to increase. When fully functional tests were done on devices that were unbiased during irradiation, erase failures occurred at 45 krad(Si).

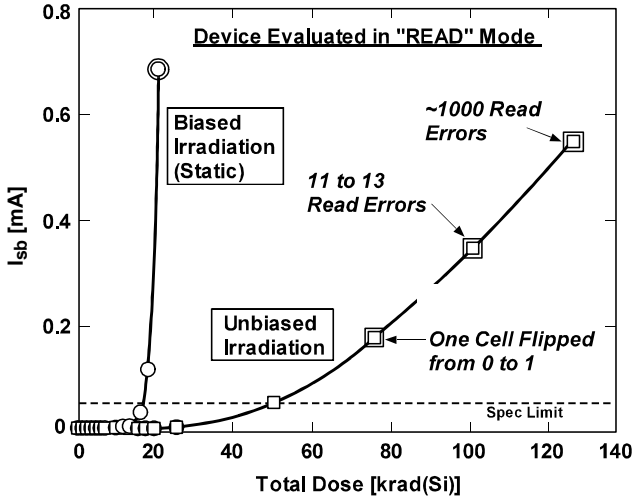


Figure 7. Total dose test results for the 128Mb Samsung flash device, tested in read mode.

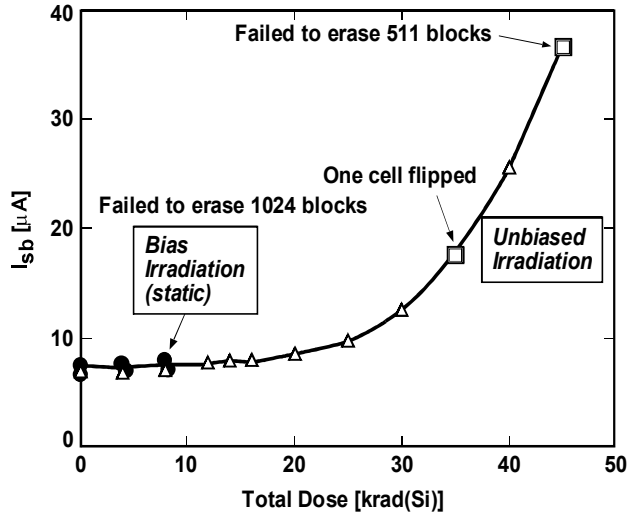


Figure 8. Total dose test results for the 128Mb Samsung flash memory evaluated in Erase/Write/Read mode.

D. Charge Pump Operation and TID Response

Earlier work [5] implicated the charge pump as the weak link accounting for 16Mb Intel failures. This conclusion can be bolstered by consideration of the Samsung charge pump which utilizes internal floating-well elements, shown in Figure 9, to produce the higher positive voltages needed to erase, program and read contents. Each PMOS transistor is

fabricated in a separate n-well. The open-circuit voltage can be calculated with the following equation [7]:

$$V_{out} = V_{cc} - |V_{te}| + N(\alpha V_{cc} - |V_{te}|) \quad (1)$$

Where V_{te} is the effective V_{th} of the pass transistor

α is close to 1 in practical cases

N is the number of stages

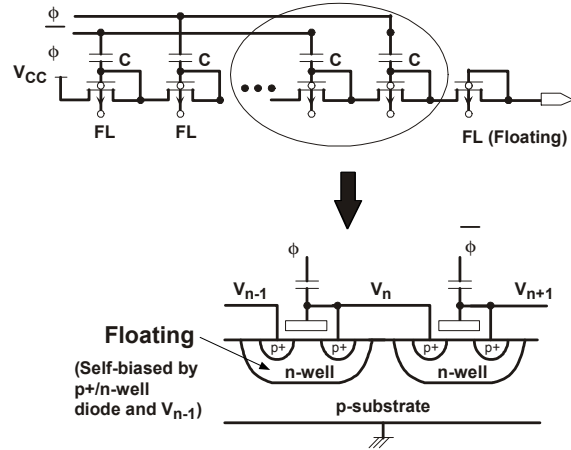


Figure 9. Samsung flash memory charge pump circuit from Ref. 7. (Intel's is likely to be similar.)

The generated output voltage is directly proportional to the number of charge pump stages and, therefore, can be generated even at a very low supply voltage. The effect of ionizing dose are to shift the threshold and reduce V_{out} . Any stage-to-stage increases in leakage would also reduce the charge pump output. Additionally, α drops rapidly as current demand increases. Note that, for NAND devices, the highest voltage is needed for erasing, then programming, then reading; this is the order in which failures are seen in the TID tests on the Samsung 128Mb flash. The Intel NOR devices tend to use the same voltage for both erasing and writing, and, in the testing, write errors are seen before erase failures. (Alternatively, the significant increases in standby current on the Intel devices may mean a different failure mechanism is dominant.)

III. SINGLE EVENT TESTING

Single event testing was done at Brookhaven National Laboratory using several different ion species. The range of the ions exceeded 38 μm in all cases (these devices have very shallow structures, so that this range should be adequate, even at incident angles of 60 degrees). Just as for the previous generation NAND flash memories from Samsung [6], errors did not occur in individual memory cells in the new 128-Mb Samsung devices. However, the heavy ions caused functional

operation that was consistent with upset in the controller or registers. The cross section for these errors was relatively small, on the order of 10^{-6} cm^2 . Additionally, address upsets were observed during sequential access.

Upsets of the page buffer were observed when reading the part during irradiation. The results are shown in Figure 10. They are somewhat dependent on the operating frequency and ion flux used for the irradiation run. In this case the device was tested by dynamically reading the contents of the memory

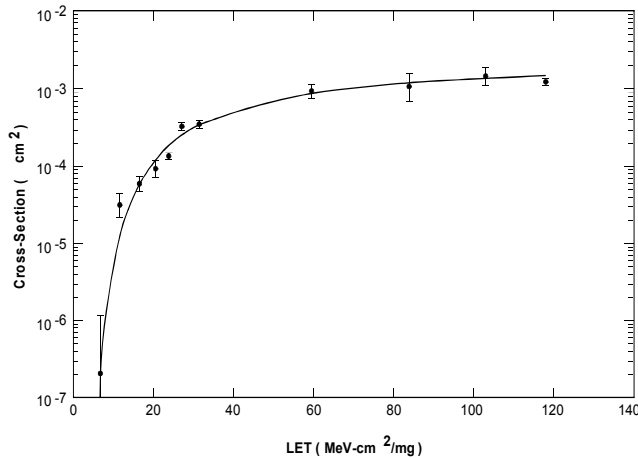


Figure 10. Single event upset cross-section for the 528-byte buffer register of the Samsung 128Mb flash memory.

at an access rate of approximately 3 MHz, with a flux of $\sim 10^4$ ions/($\text{cm}^2\text{-sec}$); these cause less than a 10% error in the measured cross sections. Note that the two-sigma error bars shown are from counting statistics. The smooth curve is a fit of diffusion-derived equation [8]. It is to be expected that the buffer would have the same cross section during writes as well; this was confirmed for $\text{LET} = 16.6$ MeV per mg/cm^2 . Only a few runs were made with irradiations while erasing or writing. During one such run with bromine with $\text{LET} = 38$, the device became unable to perform erasing. Inverting the fluence of this run give a cross section estimate of 5×10^{-4} cm^2 . This catastrophic result could be due to SEGR.

Somewhat different results occurred for the Intel multi-level flash devices. The Intels do not implement a read buffer (write buffer is optional), only latching the current data; thus, the absence of low LET errors like those of Figure 10 is not surprising. With all LETs, some functional errors were observed that were similar to the general types of errors observed for the Samsung devices as well as previous-generation flash memories from Intel. When high LET ions were used, read errors were observed. For example, with $\text{LET} = 84$ (iodine at a 45-degree angle of incidence) approximately 100 cell locations were stuck in a specific state, and could no longer be written. This could be caused by microdose errors [9, 10] that affect the sense amp detection levels slightly or shifts the cell threshold. The errors always were always from lower values to the next higher corresponding to the sense amp detection level shifting upward or the cell threshold voltage shifting downward. The arrows in Figure 11 show the

number of transitions that were observed for the 64-Mb Intel devices; the 32-Mb devices behaved similarly. Note the errors were noticeably fewer within minutes at room temperature. This apparent annealing rules out the hypothesis that the floating gate was somewhat discharged by the ion passage since there would be no mechanism to re-charge it.

Device irradiated with Iodine ($\text{LET} = 60$ MeV-cm²/mg)

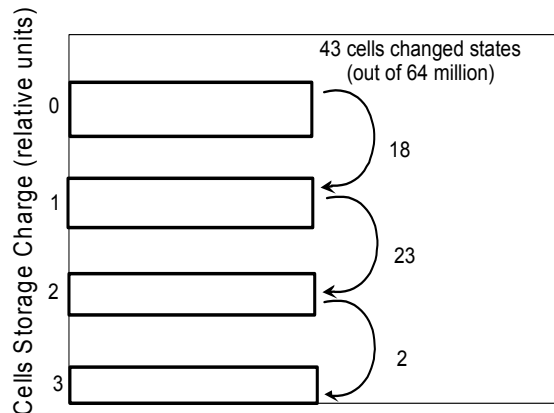


Figure 11. Single event read errors for the Intel 64Mb flash memory.

IV. DISCUSSION

Tests of multi-level flash memories have shown that they typically fail at relatively low levels, below 20 krad(Si), when biased during irradiation. The advanced devices tested in the present work demonstrate somewhat lower failure levels relative to earlier generation devices.

Just as for older devices, they undergo far less degradation when they are irradiated in an unbiased mode, and there are many applications where they can be used effectively in a mainly unpowered, read-only mode. However, they are far more vulnerable to failure in erase and write modes, which is probably caused by changes in the internal charge pump (erase and write functions required very high internal voltages, with relatively tight tolerances [1,2,4]). Charge-pump failures were identified as the cause of failure at low total dose levels in older device type [5], where external erase/write voltages could be used instead of the internal charge pump. However, the newer devices do not provide this option.

Single event upset in the newer devices appears to be similar to the older parts with some exceptions. Functional failures caused by cell upsets in the very complex control and state registers used in flash memory architecture continue to occur. Catastrophic failures have changed in detail (and moved from an Intel 16Mb device to the 128Mb Samsung) are still occurring for irradiations in EWR mode.

An important new finding is the identification of small numbers of cell transitions at high LET for multi-level flash technology devices. Although these errors only occur for ions

with very high LET, it is possible that they may occur at much lower LET values where the effect is of more practical importance as multilevel flash memory technology evolves. This is consistent with the tight threshold voltage distribution required to implement multi-level flash technology. Although the same mechanism is probably present for the Samsung devices, there is much more separation between the "0" and "1" cell threshold voltages than for multi-flash devices, providing increased margin to compensate for microdose shifts.

It is essential to know how flash memories can be used, either in read-only mode where they are not powered except when it is needed to access their contents, or in full operational mode. Recorder-type applications where reading and writing are done in equal measure are more problematic. These may be appropriate only for low dose missions with sophisticated error correction implemented. Write-mostly applications, such as scratchpad and housekeeping, will not find flash very suitable.

V. CONCLUSIONS

Several conclusions regarding trends can be drawn from this work. First, the charge pump is still the likely cause of the disappointing total dose failure levels. Although the direct test method of over-riding the charge pump output was not available with these devices, the fact that read functionality was passing at higher dose levels than erase/write implicates the charge pump. Second, the NOR architecture still demonstrates some advantage in higher failure levels relative to the NAND, although the advantage is generally less than before and in some specific cases, the NOR is worse. Third, the microdose effects seen, although not affecting many bits, may be on the verge of becoming a serious problem as transistor sizes scale and Intel pushes toward the next step in multi-level flashes, detecting seven threshold voltage levels. Finally, designing systems to effectively use flash memory while avoiding radiation problems, including destructive effects, is becoming more difficult as the devices become more attractive.

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