AD-A157 685 PORTABLE DIAGNOSTIC RADIOMETER(U) DAVID SARNOFF RESEARCH CENTER PRINCETON NJ JUL 85 N00014-83-C-0524 1/1

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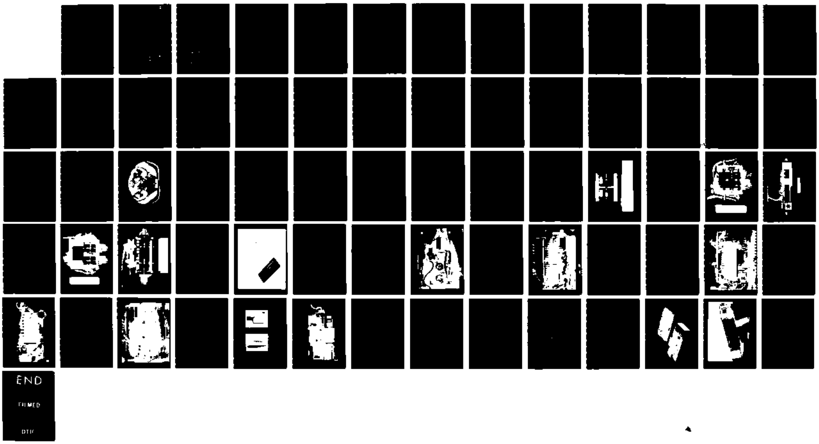

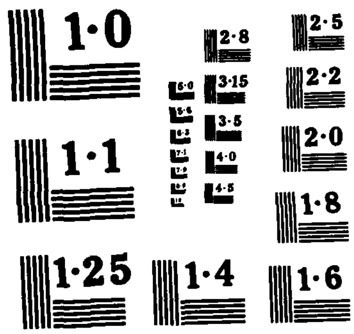

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AD-A157 685

PORTABLE DIAGNOSTIC RADIOMETER

FINAL REPORT - PHASE I

CONTRACT N00014-83-C-0524

PREPARED FOR

DEPARTMENT OF THE NAVY
NAVAL MEDICAL RESEARCH AND DEVELOPMENT COMMAND
NATIONAL NAVAL MEDICAL CENTER
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PREFACE

This Final Report for Phase I was prepared by RCA Laboratories, Princeton, New Jersey under Contract No. N00014-83-C-0524 for the Naval Medical Research and Development Command, Bethesda, Maryland. The work on Phase I was performed from October 1, 1983 through June 30, 1984 at the RCA Microwave Technology Center, Dr. Fred Sterzer, Director. The program was supervised by Markus Nowogrodzki, Head of the Microwave Subsystems and Special Projects Group. The Project Scientist was Robert W. Paglione, Member of the Technical Staff, with technical support provided by Francis J. Wozniak and Eugene C. McDermott.

The computer modeling and other software support was provided by Morris Ettenberg, Consultant.

I. INTRODUCTION

There exists a need for a portable diagnostic instrument that can noninvasively monitor and display internal body temperatures. This instrument would be extremely important on U.S. Navy ships whose complement does not include the services of competent medical professionals. In this case it would be important to determine whether a particular medical emergency does or does not exist in a patient. This would determine whether the patient should or should not be evacuated to a suitable medical facility for treatment.

The instrument would determine, by radiometric means, whether particular organs exhibit an elevated temperature. For example, this may be an aid in the diagnosis of appendicitis or nephritis.

The instrument described in this report is a dual-frequency microwave radiometer. The radiometer measures the amount of noise power being radiated from a localized tissue volume on the patient. The amplitude of this noise power over a frequency spectrum determined by the microwave components is proportional to the average temperature of the volume in question. Making this measurement at two separate frequencies can give an indication of the temperature profile over a depth as great as 6 cm.

II. TECHNICAL DISCUSSION

A. PROGRAM OBJECTIVE

The objective of Phase I of this program was to develop a "proof of concept" breadboard of a dual-frequency radiometer. The instrument should include a microprocessor, a readout, a power supply, and all circuits necessary to prove the concept of a self-balancing, multifrequency radiometer suitable for use as a diagnostic instrument by the U.S. Navy.

To meet this objective, the following tasks would be addressed:

1. Computer modeling of a multifrequency radiometer to determine the optimum frequencies that, when used with the portable radiometer, would provide temperature information at three body depths where hot-spots indicative of inflammation could be detected.

2. Adapting the self-balancing radiometer circuits to provide the multifrequency mode of operation determined from 1.

3. Construction of a breadboard instrument model.

4. Evaluation and testing of the experimental instrument of 3.

B. COMPUTER MODELING

To be able to translate the multifrequency radiometric measurements of average temperature within a tissue volume into a three-point temperature profile, a computer model of the system and the resulting heat distributions as exhibited in particular radiometric measurements is required.

The computer program that has been developed calculates the radiometric temperature at specified frequencies from a known temperature-versus-depth profile. The temperature profile is generated by assuming an arterial and ambient temperature and then calculating the heat transported due to the various heat conductivities and blood flows of the intervening tissue sections. The radiometric temperature is calculated in the following manner: The noise power, P_n, is calculated for a point on the temperature profile by multiplying the temperature, T_n, by Boltzmann's constant, k, and the receiver bandwidth, B. The amount of this power that reaches the surface is found by assuming an exponential decay with distance -- the exponential constant being the attenuation constant, , of the intervening tissues. The radiometric temperature is then the sum of all of the surface noise powers generated by all of the points on the profile divided by kB. Mathematically this is written as

$$1)\ T_{RAD} = T_1 \left\{1-\exp(-\alpha_1 x_1)\right\} + T_2 \left\{1 - \exp(-\alpha_2 x_2)\right\} \exp(-\alpha_1 x_1) + T_3 \left\{1-\exp(-\alpha_3 x_3)\right\} \exp\left\{-(\alpha_1 x_1 + \alpha_2 x_2)\right\} + \ldots T_n \left\{1-\exp(-\alpha_n x_n)\right\} \exp\left\{-\alpha_1 x_1 + \alpha_2 x_2 + \ldots \alpha_{n-1} x_{n-1})\right\}$$

where n = number of tissue sections

x = thickness of tissue section

and α = attenuation constant of tissue section.

The curve in Fig. 1 was generated by using the computer model and by assuming an arterial temperature of 37°C and an ambient temperature of 21°C. The tissue geometry used was taken from a body slice in the area of the appendix.[1] This slice, shown in Fig. 2, contains skin, fat, muscle, intestine, the appendix (processus vermiformis), and bone. The front-to-back tissue thicknesses used in the model are: 1mm-skin, 8.5mm-fat, 6.55cm-intestine, 1cm-appendix, 3.3cm-muscle, 5.1cm-bone, 1.4cm-muscle, 1.05cm-fat, and 6.5mm-skin. Typical values were used for the tissue density, thermal conductivity, specific heat, and blood flow.[2] Also, a value was used for normal surface cooling.[3] The curve in Fig. 1 is therefore a normal thermal profile in the appendix region. The radiometric temperature was calculated over the frequency range from 800 to 4000 MHz. The front surface reading is labeled TF(rad) in the figure, and only the 800 and 4000 MHz data are shown since the temperature function is linear between these two points.

In Fig. 3a, b, and c, the appendix has been given an elevated temperature of 2^{o} over normal; and the position of the appendix is varied from 4 to 8 cm. It can be seen from this data and the data in Fig. 1 that the radiometer must have an accuracy of $0.2^{o}C$ in order to detect a $2^{o}C$ elevated temperature at a depth of 6 cm.

In Fig. 4 and 5, the radiometric temperatures at 800 and 4000 MHz are plotted as a function of the surface temperature and hot-spot depth. The line representing no hot spot (NHS) is also shown in both figures. Therefore, from the measurement of the surface temperature and the radiometric temperature at 800 and 4000 MHz, it is possible to determine the depth of a typical hot spot. The temperature profile can then be extracted from the computer model. For example, if the surface and radiometric temperatures are 33.7°C, 36.7°C at 800 MHz, and 36.1°C at 4000 MHz; then the hot spot occurs at a depth of 4 cm. The temperature profile for this condition is as shown in Fig. 2b; and the three temperatures that would be displayed are 34.7°C at 0 cm depth, 37°C at 2 cm depth, and 38.7° at 4 cm depth.

C. 4 GHz SUBSYSTEM

The basic Dicke-type radiometer[4] is shown schematically in Fig. 6. In this circuit, the target noise power entering through the antenna is compared to the noise power eminating from a temperature-controlled termination. The difference between the two signal levels is displayed on the DC meter--this reading is proportional to the temperature of the target. An improvement can be made in the accuracy of this system if the reference noise signal, in this case the oven-controlled termination, was always adjusted to give a zero reading on the DC meter; then the temperature of the reference noise source would be equal to the temperature of the target. This self-balancing scheme can be realized by replacing the over-controlled termination with a diode noise source. The mixer can also be replaced with a synchronous detector to improve the system sensitivity and reduce the system noise.

The single-throw-double-pole switch is usually realized with an electronically-switched, latching ferrite circulator; however, at these frequencies, the size, weight and current drawn by these components are limiting factors when considering a portable instrument. The switch can also be designed using switched low-noise amplifiers, as shown in Fig. 7. Each amplifier is pulsed on and off asynchronously with the other, and the off-channel isolation is greater than 40 dB. The output of each amplifier is combined through a 3 dB hybrid coupler to produce a single switched output.

The amplifiers were designed around the NE13783-4 field-effect transistor--these transistors are optimized for low-noise performance at 4 GHz. The scattering parameters of these devices were measured with a computer-controlled automatic network analyzer. Input and output matching networks were designed that would produce an amplifier with a minimum gain of 13 dB from 3.7 to 4.2 GHz. The amplifiers were assembled on pallets and tested. A photograph of an amplifier pallet is shown in Fig. 8 and the measured gain of a typical amplifier is shown in Fig. 9. The assembled switch and amplifier are shown in the photographs of Figs. 10 and 11. The gain of the 3-stage amplifier with isolators is shown in Fig. 12.

D. 800 MHz SUBSYSTEM

The 800 MHz amplifier and switch were designed in a similar manner as the 4 GHz amplifiers. The solid-state devices used in this case were AT-41470 low-noise bipolar transistors. A photograph of the switch and amplifier is shown in Fig. 13 and 14. The gain response of the 2-stage amplifier is shown in Fig. 15.

E. ANTENNAS

Folded-dipole antennas were chosen for the radiometer since they can easily be made on a printed-circuit board, they can be made balanced, and they operate over a wide bandwidth.[5] A photograph of the 800 and 4000 MHz antenna assembly is shown in Fig. 16. Each antenna on the antenna board, also shown in Fig. 16, is connected to a 3.6mm coaxial line that protrudes out the back of the drawn-aluminum housing. The antenna board is mounted within the housing at a distance of 1.6mm from the open end. The 1.6mm gap is filled with a layer of neoprene rubber foam that acts as a thermal insulator. A 300K-ohm thermistor (Victory Engineering, Model 53A55) is epoxied into the antenna board so that it protrudes slightly through the foam rubber to contact the tissues being measured. The thermistor wires also come out the back of the aluminum housing.

The back of the aluminum housing also acts as the reflecting backplane for the 800 MHz antenna; a brass plate (38.1mm wide x 16.5mm high x 0.8mm thick) mounted on the coaxial line of the 4 GHz antenna at a distance of 10 cm from the rear of the antenna board acts as its reflecting backplane.

The VSWR of these antennas measured while the assembly is in contact with tissue is shown in Fig. 17.

F. LOW-FREQUENCY COMPONENTS

The schematic for the dual-frequency radiometer, including the low-frequency and digital components, is shown in Fig. 18. the low-frequency components consist of a 100 Hz modulator, a filter/amplifier, a synchronous detector and loop amplifier, a pulse-width modulator, and a switching regulator.

A photograph of the 100 Hz modulator and its associated schematic are shown in Figs. 19 and 20. This circuit produces a 200 Hz, crystal-controlled square-wave that is divided by a flipflop to achieve a 100 Hz modulation frequency. IC3 and Q5, and IC4 and Q6 produce 10 V pulses capable of driving 20 ma to the collector of each bipolar amplifier stage in the 800 MHz switch. Q3 and Q4 provide the same function for the 4000 MHz switch with 3 V pulses driving 10 ma to the drains of the FET amplifiers. Q1 and Q2 provide a slow-turn-on 3.6 V supply for Q3 and Q4.

The filter/amplifier is shown in the photograph of Fig. 21 and schematically in Fig. 22. All ICs are OP-27 low-noise operational amplifiers. The first stage is a buffer stage that provides AC coupling, transient protection, and a DC return path for the active filter. The second stage is the active filter with a gain and cutoff frequency of approximately 3 dB and 1 KHz.

The third stage is a variable-gain amplifier that provides 0 to 40 dB of gain. The filter response at full gain for the entire circuit is shown in Fig. 23.

The photograph and schematic for the synchronous detector and loop amplifier are shown in Figs. 24 and 25. The synchronous detector is built around the AD630 balanced modulator/demodulator chip, connected as an in-phase detector. In this mode the AD630 will produce a DC output voltage that is proportional to the difference between the two input signals when the two input signals are in phase with the reference signal, which in this case is the 100 Hz modulation to the switches. Therefore, any system noise that has been impressed on either or both inputs is greatly reduced and the overall detection sensitivity is greatly increased.

IC3 in Fig. 25 is the loop amplifier. The amplifier is an integrator with a time constant of approximately 3 seconds. The op-amp is connected in the inverting mode so that when the input voltage goes negative (this is indicative of an increasing target temperature), the output goes positive. A change in the output voltage of the loop amplifier causes a change in the noise power out of the noise diode which in turn brings the input voltage to zero or into a balanced loop condition.

The pulse-width modulator board is shown in the photograph of Fig. 26 and schematically in Fig. 27. The CA1524 outputs 28 V pulses at a 1 KHz repetition rate to the diode noise source. The pulse width of these pulses varies between 0 and 100% as the control voltage varies between 1 and 3.5 V. The DC average of these pulses is proportional to the target temperature, and it is this voltage that is read by the microprocessor and converted into temperature.

Most of the DC voltages required by the various components in the radiometer system are supplied by the switching regulator shown in the photograph of Fig. 28 and the schematic of Fig. 29. The power supply was designed to operate with a +12 VDC input which would be supplied by a rechargeable battery in Phase II. The FET bias voltages, that is the -5 V gate supply and +3 V drain supply, are sequenced such that on turn-on the gate voltage is on before the drain voltage and on turn-off the gate is off after the drain voltage. The turn-on and turn-off sequencing can be seen in the oscillographs of Fig. 30a and b.

G. DIGITAL PROCESSOR SUBSYSTEM

The digital processor subsystem is shown in the photograph

FIGURE CAPTIONS

Fig. 1. Temperature-versus-depth profile in tissue calculated using assumed arterial and ambient temperatures of 37 and 21°C. The tissue geometry is that of a body slice in the area of the appendix. TF(rad) is the radiometric temperature measured at a depth of 0 cm.

Fig. 2. A 2.5 cm thick body slice in the area of the appendix (12 Processus vermiformis).

Fig. 3. Temperature profile in tissue calculated using assumed arterial and ambient temperatures of 37 and 21°C. An elevated temperature of 2°C, representing an inflamed appendix, is calculated for depths of (a) 4 cm, (b) 6 cm, and (c) 8 cm.

Fig. 4. The calculated radiometric temperature as a function of surface temperature and hot-spot depth for an 800 MHz radiometer.

Fig. 5. The calculated radiometric temperature as a function of surface temperature and hot-spot depth for a 4 GHz radiometer.

Fig. 6. Basic Dicke radiometer schematic.

Fig. 7. Schematic of a single-pole-double-throw (SPDT) microwave switch using low-noise amplifiers.

Fig. 8. Photograph of the NE13783-4 low-noise amplifier pallet.

Fig. 9. Measured gain of a typical NE13783-4 amplifier pallet.

Fig. 10. Photograph of the assembled FET SPDT switch.

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```
 01B1 27                   DEC    R7
 01B2 27                   DEC    R7
 01B3 F80B                 LDI    0BH
 01B5 5F                   STR    RF
 01B6 F8CB                 LDI    0CBH
 01B8 53                   STR    R3
 01B9 F8FC                 LDI    0FCH
 01BB 59                   STR    R9
 01BC F85E                 LDI    5EH
 01BE 54                   STR    R4
 01BF F801                 LDI    01H
 01C1 55                   STR    R5
 01C2 C00056  >            LBR    LP1
 01C5 7B          CHK2     SEQ              ;IF LOOP CNTR=2
 01C6 DE                   SEP    RE        ;SET RF SWITCHES FOR 800MHZ
 01C7 27                   DEC    R7        ;CALL DELAY & RETURN
 01C8 27                   DEC    R7
 01C9 27                   DEC    R7
 01CA F806                 LDI    06H
 01CC 5F                   STR    RF
 01CD F865                 LDI    65H
 01CF 53                   STR    R3
 01D0 F8CF                 LDI    0CFH
 01D2 59                   STR    R9
 01D3 F801                 LDI    01H
 01D5 55                   STR    R5
 01D6 F822                 LDI    22H
 01D8 54                   STR    R4
 01D9 C00056  >            LBR    LP1
                  ;**
 01DC 60          EXDLY    IRX
 01DD D0                   SEP    R0
 01DE F8CF        DELAY    LDI    0CFH
 01E0 26                   DEC    R6
 01E1 56                   STR    R6
 01E2 26                   DEC    R6
 01E3 56                   STR    R6
 01E4 F801        PT1      LDI    01H
 01E6 F5                   SD
 01E7 56                   STR    R6
 01E8 60                   IRX
 01E9 F800                 LDI    00H
 01EB 75                   SDB
 01EC 56                   STR    R6
 01ED 32DC    >            BZ     EXDLY
 01EF 26                   DEC    R6
 01F0 30E4    >            BR     PT1
 01F2 DE          QUIT     SEP    RE
 01F3 DE                   SEP    RE
 01F4 C00000  >            LBR    START
```

```
0175 57              STR    R7       ;STORE 2nd DIGIT IN R7-1
0176 6E              INP    6
0177 27              DEC    R7
0178 57              STR    R7       ;STORE LS DIGIT IN R7-2
                ;**DISPLAY DIGITS
0179 F84F            LDI    4FH      ;DISABLE CDP1855, ENABLE CDP1851
017B 26              DEC    R6
017C 56              STR    R6
017D F833            LDI    33H
017F 26              DEC    R6
0180 56              STR    R6
0181 F808            LDI    08H
0183 26              DEC    R6
0184 56              STR    R6
0185 61              OUT    1
0186 62              OUT    2
0187 62              OUT    2
                ;**
0188 07              LDN    R7       ;LOAD LS THRU MS DIGIT
0189 26              DEC    R6
018A 56              STR    R6
018B 17              INC    R7
018C 07              LDN    R7
018D 26              DEC    R6
018E 56              STR    R6
018F 17              INC    R7
0190 07              LDN    R7
0191 26              DEC    R6
0192 56              STR    R6
0193 64              OUT    4
0194 26              DEC    R6
0195 63              OUT    3
0196 64              OUT    4
0197 26              DEC    R6
0198 65              OUT    5
0199 64              OUT    4
019A 26              DEC    R6
019B 67              OUT    7
019C DE              SEP    RE       ;CALL DELAY
                ;**MAIN LOOP CNTR TEST
019D 0D              LDN    RD       ;LOAD CNTR & SUBTRACT 1
019E FF01            SMI    01H
01A0 32F2    >       BZ     QUIT     ;IF LOOP CNTR=0 THEN END
01A2 5D              STR    RD
01A3 FF01            SMI    01H
01A5 3AC5    /       BNZ    CHK2     ;IF LOOP CNTR=1
01A7 F820            LDI    20H      ;SET MUX CHNL=2 & RETURN
01A9 5A              STR    RA
01AA F8A0            LDI    0A0H
01AC 5B              STR    RB
01AD F830            LDI    30H
01AF 5C              STR    RC
01B0 27              DEC    R7
```

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0139 07          LDN   R7
013A 26          DEC   R6
013B 56          STR   R6
013C F864        LDI   64H
013E 26          DEC   R6
013F 56          STR   R6
0140 F8FC        LDI   0FCH
0142 26          DEC   R6
0143 56          STR   R6
0144 67          OUT   7
0145 64          OUT   4
0146 65          OUT   5
0147 66          OUT   6
0148 67          OUT   7
0149 C4          NOP
014A C4          NOP
014B C4          NOP
014C F8F0        LDI   0F0H
014E 26          DEC   R6
014F 56          STR   R6
0150 67          OUT   7
0151 6C          INP   4
0152 6D          INP   5
0153 17          INC   R7
0154 57          STR   R7      ;STORE MS DIGIT IN R7
0155 6E          INP   6
0156 27          DEC   R7
0157 57          STR   R7      ;STORE REMAINDER IN R7-1
0158 F8F2        LDI   0F2H    ;DIVIDE REMAINDER BY 10 (0AH)
015A 26          DEC   R6
015B 56          STR   R6
015C 07          LDN   R7
015D 26          DEC   R6
015E 56          STR   R6
015F F80A        LDI   0AH
0161 26          DEC   R6
0162 56          STR   R6
0163 F8FC        LDI   0FCH
0165 26          DEC   R6
0166 56          STR   R6
0167 67          OUT   7
0168 64          OUT   4
0169 65          OUT   5
016A 67          OUT   7
016B C4          NOP
016C C4          NOP
016D C4          NOP
016E F8F0        LDI   0F0H
0170 26          DEC   R6
0171 56          STR   R6
0172 67          OUT   7
0173 6C          INP   4
0174 6D          INP   5
```

```
00FC 09                  LDN     R9
00FD 26                  DEC     R6
00FE 56                  STR     R6
00FF F8F0                LDI     0F0H
0101 26                  DEC     R6
0102 56                  STR     R6
0103 67                  OUT     7
0104 64                  OUT     4
0105 67                  OUT     7
0106 C4                  NOP
0107 C4                  NOP
0108 C4                  NOP
0109 F8F0                LDI     0F0H
010B 26                  DEC     R6
010C 56                  STR     R6
010D 67                  OUT     7
010E 26                  DEC     R6
010F 6C                  INP     4
0110 6E                  INP     6       ;INPUT BYTE TO STACK
0111 6D                  INP     5
0112 60                  IRX             ;COMPLEMENT IF NEG AT C1
0113 F800                LDI     00H
0115 56                  STR     R6
0116 26                  DEC     R6
0117 17                  INC     R7
0118 07                  LDN     R7
0119 FFFF                SMI     0FFH
011B 27                  DEC     R7
011C 3A29                BNZ     C2
011E F0                  LDX
011F FBFF                XRI     0FFH
0121 FC01                ADI     01H
0123 56                  STR     R6
0124 60                  IRX
0125 F8FF                LDI     0FFH
0127 56                  STR     R6
0128 26                  DEC     R6
0129 04           C2     LDN     R4      ;ADD CONSTANT
012A F4                  ADD
012B 57                  STR     R7
012C 60                  IRX
012D 05                  LDN     R5
012E 74                  ADC
012F 17                  INC     R7
0130 57                  STR     R7
                  ;**CONVERT TO DECIMAL DIGITS
0131 F8F2                LDI     0F2H    ;DIVIDE BY 100 (64H)
0133 26                  DEC     R6
0134 56                  STR     R6
0135 07                  LDN     R7
0136 26                  DEC     R6
0137 56                  STR     R6
0138 27                  DEC     R7
```

```
00BF 60                 IRX
                  ;**CONVERT AVERAGE TO TEMPERATURE
00C0 27                 DEC     R7      ;SUBTRACT CONSTANT FROM AVG.
00C1 07                 LDN     R7
00C2 56                 STR     R6
00C3 03                 LDN     R3
00C4 F5                 SD
00C5 57                 STR     R7
00C6 17                 INC     R7
00C7 07                 LDN     R7
00C8 56                 STR     R6
00C9 0F                 LDN     RF
00CA 75                 SDB
00CB 57                 STR     R7
00CC 07                 LDN     R7      ;COMPLEMENT IF SUBTR. GOES NEG.
00CD FFFF               SMI     0FFH
00CF 3AD9     >         BNZ     C1
00D1 27                 DEC     R7
00D2 07                 LDN     R7
00D3 FBFF               XRI     0FFH
00D5 FC01               ADI     01H
00D7 57                 STR     R7
00D8 17                 INC     R7
00D9 F8FC       C1      LDI     0FCH    ;DISABLE CDP1851, ENABLE CDP1855,
00DB 26                 DEC     R6      ;& INITIALIZE
00DC 56                 STR     R6
00DD F800               LDI     00H
00DF 26                 DEC     R6
00E0 56                 STR     R6
00E1 61                 OUT     1
00E2 67                 OUT     7
00E3 F8F9               LDI     0F9H
00E5 26                 DEC     R6
00E6 56                 STR     R6
00E7 27                 DEC     R7
00E8 07                 LDN     R7      ;LOAD X & Z REGS. & MULT. BY 93 (5DH)
00E9 26                 DEC     R6
00EA 56                 STR     R6
00EB F85D               LDI     5DH
00ED 26                 DEC     R6
00EE 56                 STR     R6
00EF 64                 OUT     4
00F0 65                 OUT     5
00F1 67                 OUT     7
00F2 C4                 NOP
00F3 C4                 NOP
00F4 C4                 NOP
00F5 6C                 INP     4
00F6 6D                 INP     5
00F7 6E                 INP     6
00F8 F8F2               LDI     0F2H    ;LOAD X REG. & DIVIDE BY CONSTANT
00FA 26                 DEC     R6
00FB 56                 STR     R6
```

```
0082 FA0F                  ANI    0FH     ;MASK OUT BITS 5-8
0084 57                    STR    R7
0085 0C                    LDN    RC      ;GIVE TOGGLE COMMAND
0086 FF10                  SMI    10H
0088 26                    DEC    R6
0089 56                    STR    R6
008A 0C                    LDN    RC
008B 26                    DEC    R6
008C 56                    STR    R6
008D 64                    OUT    4
008E 64                    OUT    4
008F 6E                    INP    6       ;INPUT A-TO-D BITS 5,6,7,8,9,10,11,12
0090 60                    IRX
0091 F4                    ADD            ;ADD PRESENT READING TO PREVIOUS
0092 56                    STR    R6
0093 60                    IRX
0094 07                    LDN    R7
0095 74                    ADC
0096 56                    STR    R6
0097 26                    DEC    R6
0098 08                    LDN    R8      ;SUBTRACT 01H FROM LOOP COUNTER (R8)
0099 FF01                  SMI    01H
009B 32A1     >            BZ     DIVN    ;CHECK IF 16 RDNGS HAVE BEEN TAKEN
009D 58                    STR    R8
009E C0006E   >            LBR    AVG
                     ;**
00A1 F0              DIVN  LDX            ;DIVIDE SUM OF 16 NOS. BY 16
00A2 F6                    SHR
00A3 F6                    SHR
00A4 F6                    SHR
00A5 F6                    SHR
00A6 56                    STR    R6
00A7 60                    IRX
00A8 F0                    LDX
00A9 FE                    SHL
00AA FE                    SHL
00AB FE                    SHL
00AC FE                    SHL
00AD 26                    DEC    R6
00AE F1                    OR
00AF FBFF                  XRI    0FFH    ;COMPLEMENT LS BYTE
00B1 27                    DEC    R7
00B2 57                    STR    R7
00B3 17                    INC    R7
00B4 60                    IRX
00B5 F0                    LDX
00B6 F6                    SHR
00B7 F6                    SHR
00B8 F6                    SHR
00B9 F6                    SHR
00BA FBFF                  XRI    0FFH    ;COMPLEMENT MS BYTE
00BC FA0F                  ANI    0FH     ;MASK OUT MS BITS
00BE 57                    STR    R7
```

```
0048 F801          LDI     01H
004A 55            STR     R5
004B F812          LDI     12H
004D 53            STR     R3
          ;**BEGIN MEASUREMENT LOOP
004E 7A            REQ             ;SET RF SWITCHES TO 4GHZ
004F F801          LDI     01H     ;SET RETURN ADDRESS
0051 BE            PHI     RE
0052 F8DE          LDI     0DEH
0054 AE            PLO     RE
0055 DE            SEP     RE      ;CALL DELAY SUBR.
          ;**
0056 F84F   LP1    LDI     4FH     ;ENABLE CDP1851
0058 26            DEC     R6      ;SET PORT B TO INPUT
0059 56            STR     R6      ;SET PORT A TO OUTPUT
005A F833          LDI     33H
005C 26            DEC     R6
005D 56            STR     R6
005E F808          LDI     08H
0060 26            DEC     R6
0061 56            STR     R6
0062 61            OUT     1
0063 62            OUT     2
0064 62            OUT     2
          ;**
0065 F800          LDI     00H     ;INITIALIZE STACK TO 0
0067 26            DEC     R6
0068 56            STR     R6
0069 26            DEC     R6
006A 56            STR     R6
006B F810          LDI     10H     ;INITIALIZE R8 TO 16
006D 58            STR     R8
          ;**
006E 0C     AVG    LDN     RC      ;SET CD4066 INPUT MUX TO
006F FF10          SMI     10H     ;INPUT CHANNEL 1 OR 2,
0071 26            DEC     R6      ;GIVE A-TO-D CONVERT COMMAND,
0072 56            STR     R6      ;RESET CD4013 TOGGLE FF
0073 0C            LDN     RC      ;GIVE TOGGLE COMMAND TO
0074 26            DEC     R6      ;CD4013 TOGGLE FF
0075 56            STR     R6
0076 0B            LDN     RB
0077 26            DEC     R6
0078 56            STR     R6
0079 0A            LDN     RA
007A 26            DEC     R6
007B 56            STR     R6
007C 64            OUT     4
007D 64            OUT     4
007E 64            OUT     4
007F 64            OUT     4
          ;**
0080 26            DEC     R6      ;INPUT A-TO-D BITS 5,6,7,8,1,2,3,4
0081 6E            INP     6       ;[MSB=BIT 1, LSB=BIT 12]
```

```
                      ;**INITIALIZE REGISTERS                  *****PROGRAM BOB*****
0000 F84F     START      LDI     4FH       ;SET MS BYTE OF RAM TO 4FH
0002 B3                  PHI     R3
0003 B4                  PHI     R4
0004 B5                  PHI     R5
0005 B6                  PHI     R6
0006 B7                  PHI     R7
0007 B8                  PHI     R8
0008 B9                  PHI     R9
0009 BA                  PHI     RA
000A BB                  PHI     RB
000B BC                  PHI     RC
000C BD                  PHI     RD
000D BF                  PHI     RF
000E F880                LDI     80H       ;R6 ADDRESS=4F80H <<STACK>>
0010 A6                  PLO     R6
0011 E6                  SEX     R6        ;SET STACK TO R6
0012 F810                LDI     10H       ;R7 ADDRESS=4F10H <<TEMP. DATA>>
0014 A7                  PLO     R7
0015 F800                LDI     00H       ;R8 ADDRESS=4F00H <<AVG. LOOP CNTR.>>
0017 A8                  PLO     R8
0018 F820                LDI     20H       ;RA ADDRESS=4F20H <<MUX CHNL COMMAND>>
001A AA                  PLO     RA
001B F830                LDI     30H       ;RB ADDRESS=4F30H <<CONVERT COMMAND>>
001D AB                  PLO     RB
001E F840                LDI     40H       ;RC ADDRESS=4F40H <<TOGGLE COMMAND>>
0020 AC                  PLO     RC
0021 F850                LDI     50H       ;RD ADDRESS=4F50H <<MAIN LOOP CNTR>>
0023 AD                  PLO     RD
0024 F860                LDI     60H       ;RF ADDRESS=4F60H <<MATH CONSTANT>>
0026 AF                  PLO     RF
0027 F861                LDI     61H       ;R9 ADDRESS=4F61H <<MATH CONSTANT>>
0029 A9                  PLO     R9
002A F862                LDI     62H       ;R5 ADDRESS=4F62H <<MATH CONSTANT>>
002C A5                  PLO     R5
002D F863                LDI     63H       ;R4 ADDRESS=4F63H <<MATH CONSTANT>>
002F A4                  PLO     R4
0030 F864                LDI     64H       ;R3 ADDRESS=4F64H <<MATH CONSTANT>>
0032 A3                  PLO     R3
0033 F800                LDI     00H       ;INITIALIZE RA TO MUX CHNL 1
0035 5A                  STR     RA
0036 F880                LDI     80H       ;INITIALIZE CONVERT COMMAND
0038 5B                  STR     RB
0039 F810                LDI     10H       ;INITIALIZE TOGGLE COMMAND
003B 5C                  STR     RC
003C F803                LDI     03H       ;INITIALIZE MAIN LOOP CNTR TO 3
003E 5D                  STR     RD
003F F807                LDI     07H
0041 5F                  STR     RF
0042 F89E                LDI     9EH
0044 59                  STR     R9
0045 F810                LDI     10H
0047 54                  STR     R4
```

J. PLANS FOR PHASE-II

The prototype unit will be delivered under Phase II of the program. A photograph of the shell of the planned prototype is shown in Fig. 38. Not shown in the photograph is the 12 volt, 3 amp-hour battery and charger unit that will connect to the pistol grip.

The display on the rear panel of the unit is a 16-character liquid-crystal display that will simultaneously display the three temperatures corresponding to the temperature of the surface and the temperature at two depths.

	4 GHz HEX	(Decimal)	800 MHz HEX	(Decimal)	Thermistor HEX	(Decimal)
C1	64	(100)	64	(100)	64	(100)
C2	959	(2393)	A77	(2679)	BF5	(3100)
C3	73	(115)	BE	(190)	F1	(241)
C4	140	(320)	140	(320)	12B	(299)

For the above constants, the 800 MHz radiometer will resolve temperatures between 18.5 and 45.4°C; the 4 GHz radiometer between 9.8 and 54.1°C; and the thermistor between 19.3 and 40.4°C.

I. RADIOMETER EVALUATION

Next Significant Digit (NSD) = $\frac{R1}{10}$ = D2+R2

Least Significant Digit (LSD) = R2.

D1, D2 and R2 are then displayed on the liquid crystal display.

The Q lines are next set to switch the latching switches into the 800 MHz position; and, with different constants in eqn. 2, a new temperature is measured and displayed. Finally the surface thermistor is interfaced to the A-to-D through a buffer amplifier and the multiplexer, and the surface temperature is calculated and displayed in a similar manner. The flow chart for the above sequence is shown in Fig. 36.

The source file that contains the assembly code for the radiometer system is listed in Appendix A.

H. BREADBOARD

The breadboard unit is shown in Fig. 37. The unit was calibrated by placing the antenna in contact with saline that was maintained at various temperatures. The antenna housing was covered with a thin layer of plastic food wrap for the calibration procedure. The saline was contained in a galvanized steel pail whose inside surfaces were lined with a 1/4 inch thick carbon-impregnated foam material. The lossy foam essentially makes the pail of saline appear as an infinite volume at a known temperature.

The radiometer and thermistor voltages were recorded for saline temperatures of 24 and 40°C. The constants of the linearizing equation (eqn. 2) are:

of Fig. 31. It consists of a power supply (±15 V and +5 V), a CDP18S601 microboard computer, a multiply/divide unit, and an interface and display board.

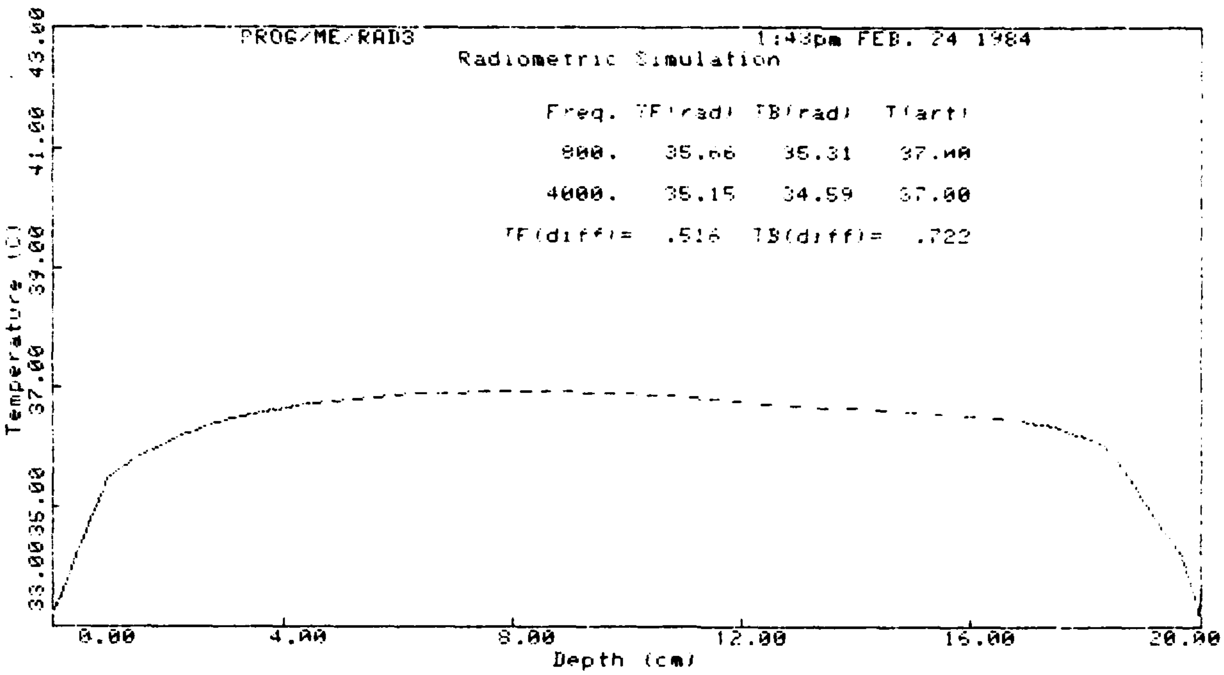
The CDP18S601 card contains a CDP1802 CPU, a 2 MHz crystal-controlled clock, read-write memory, parallel I/O ports, and sockets for up to 8 kilobytes of EPROM. The layout of the major components on this card is shown in Fig. 32. The CDP1855 multiply/divide unit is located between the CDP18S601 and the interface card. The schematic for this device is shown in Fig. 33. The schematic for the interface and display card is shown in Fig. 34, and the respective card interconnection diagram is shown in Fig. 35.

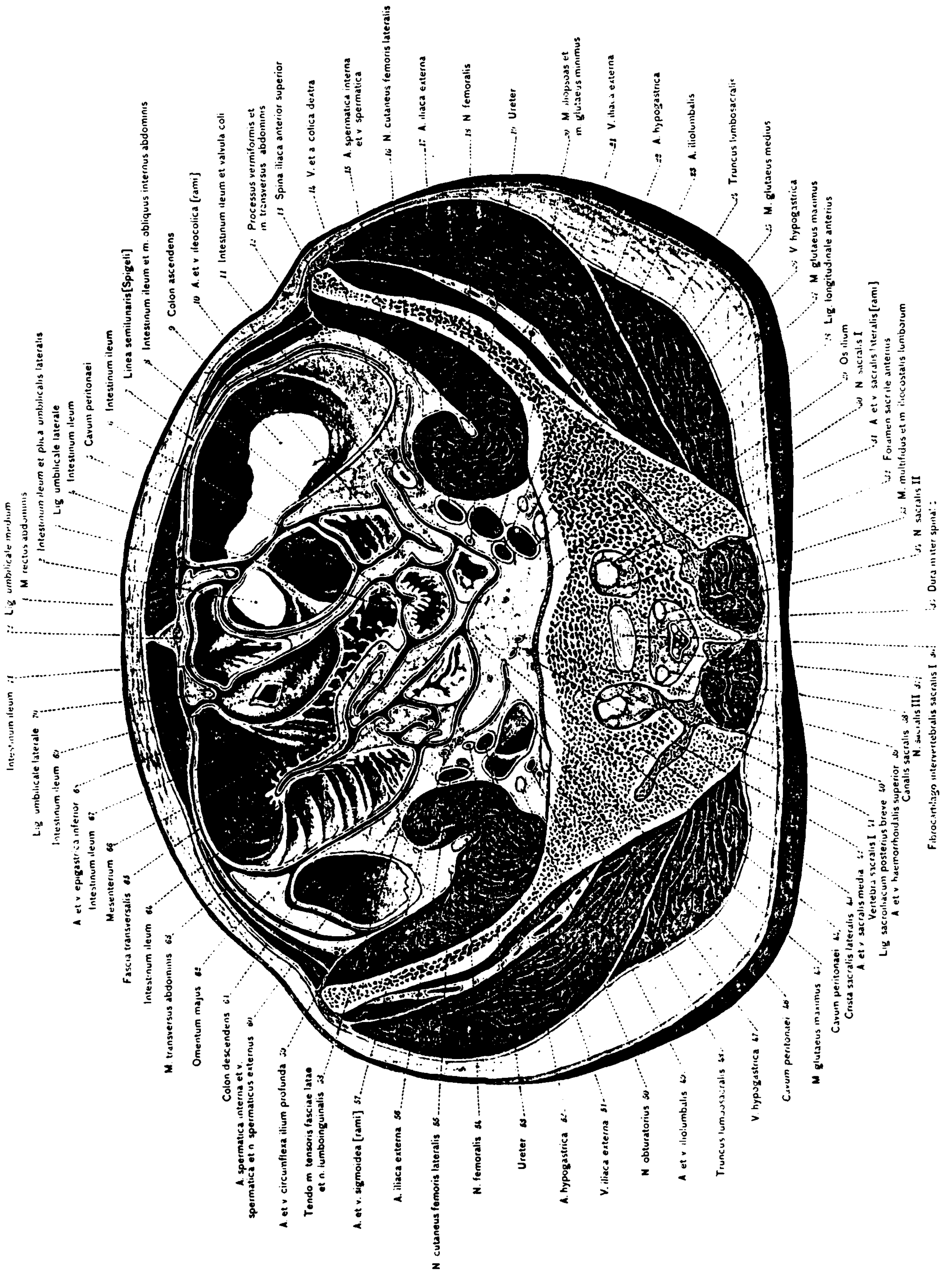
The subsystem operation is basically as follows: On start-up, the CPU resets the Q line (P1-6) which sets the latching switches (see Fig. 18) to the 4 GHz radiometer position. The radiometer output voltage is connected to the 12-bit A-to-D converter on the interface card through a buffer amplifier and the input multiplexer. The CPU converts the 12-bit digital code into a temperature using

$$2)\quad T = \frac{C1*(N-C2)}{C3} + C4$$

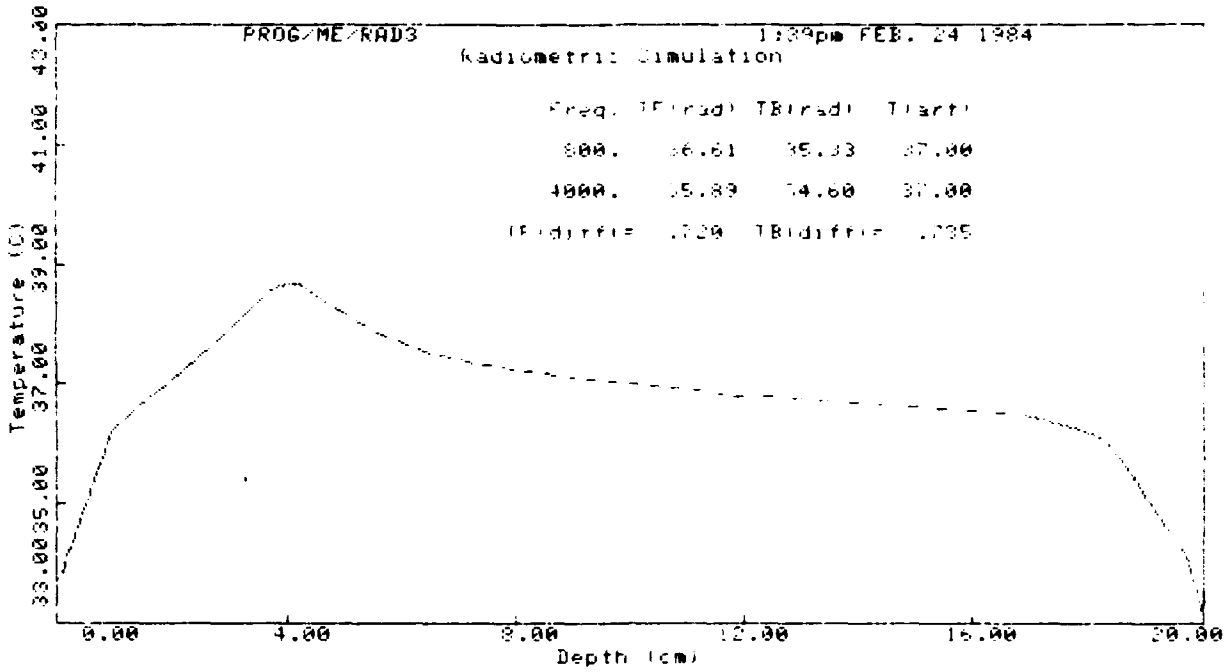
where N = 12-bit digital number in hexadecimal and C1 through C4 are constants. The temperature, T, calculated in eqn. 2 is in hexadecimal and must be converted to decimal digits for display. This is accomplished by using the following

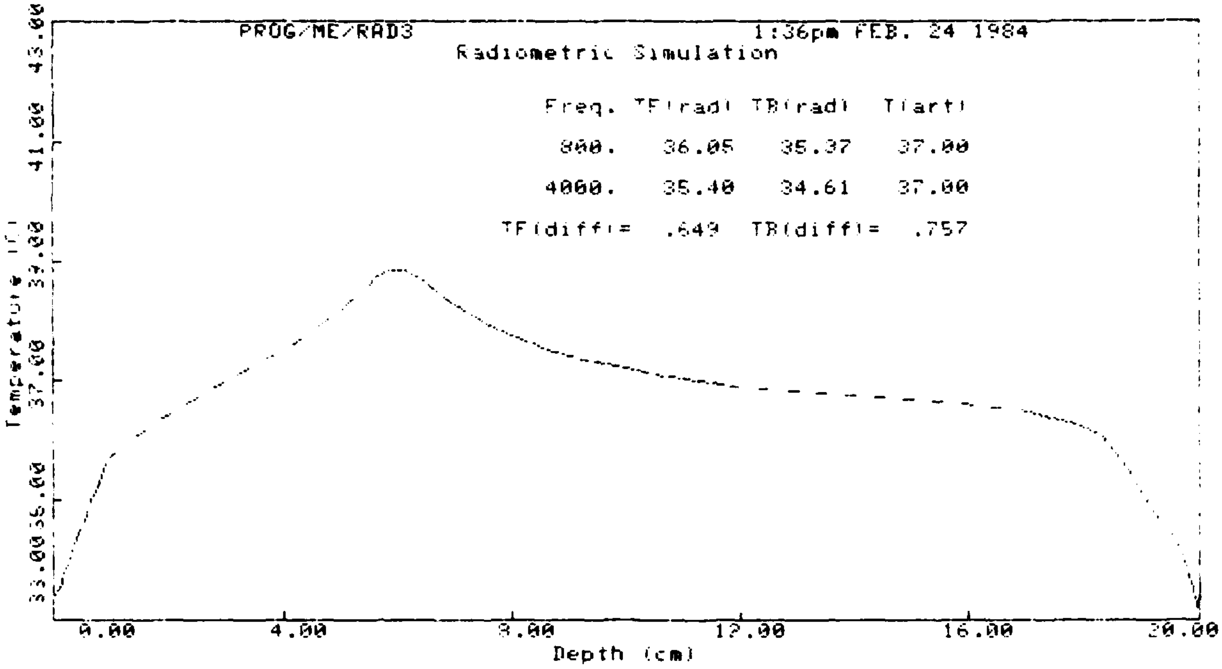
$$3)\ \text{Most Significant Digit (MSD)} = \frac{T}{100} = \text{DIGIT 1(D1)+Remainder 1 (R1)}$$

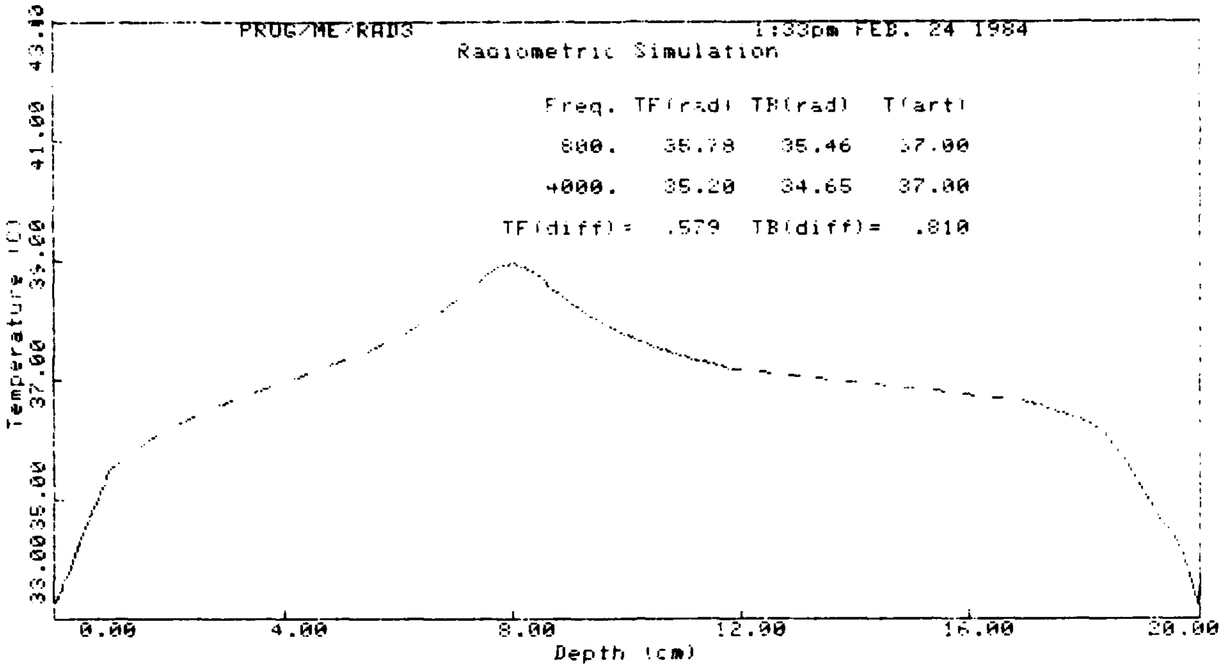

PROG/ME/RAD3
1:43pm FEB. 24 1984
Radiometric Simulation
Freq. TF(rad) TB(rad) T(art)
800. 35.66 35.31 37.00
4000. 35.15 34.59 37.00
TF(diff)= .516 TB(diff)= .722
Temperature (C)
33.00
35.00
37.00
39.00
41.00
43.00
0.00
4.00
8.00
12.00
16.00
20.00
Depth (cm)


1 M rectus abdominis
2 Intestinum ileum et plica umbilicalis lateralis
3 Lig umbilicale laterale
4 Intestinum ileum
5 Cavum peritonaei
6 Intestinum ileum
7 Linea semilunaris [Spigeli]
8 Intestinum ileum et m. obliquus internus abdominis
9 Colon ascendens
10 A. et v. ileocolica [rami]
11 Intestinum ileum et valvula coli
12 Processus vermiformis et m transversus abdominis
13 Spina iliaca anterior superior
14 V. et a colica dextra
15 A. spermatica interna et v spermatica
16 N. cutaneus femoris lateralis
17 A. iliaca externa
18 N femoralis
19 Ureter
20 M. iliopsoas et m glutaeus minimus
21 V. iliaca externa
22 A. hypogastrica
23 A. iliolumbalis
24 Truncus lumbosacralis
25 M. glutaeus medius
26 V hypogastrica
27 M glutaeus maximus
28 Lig. longitudinale anterius
29 Os ilium
30 N sacralis I
31 A et v sacralis lateralis [rami]
32 Foramen sacrale anterius
33 M. multifidus et m iliocostalis lumborum
34 N sacralis II
35 Dura mater spinalis
Fibrocartilago intervertebralis sacralis I 36
N. sacralis III 37
Canalis sacralis 38
A et v haemorrhoidalis superior 39
Lig sacroiliacum posterius breve 40
Vertebra sacralis I 41
A et v sacralis media 42
Crista sacralis lateralis 43
Cavum peritonaei 44
M glutaeus maximus 45
Cavum peritonaei 46
V. hypogastrica 47
Truncus lumbosacralis 48
A et v iliolumbalis 49
N obturatorius 50
V. iliaca externa 51
A. hypogastrica 52
Ureter 53
N. femoralis 54
N cutaneus femoris lateralis 55
A. iliaca externa 56
A. et v. sigmoidea [rami] 57
Tendo m tensoris fasciae latae et n. lumboinguinalis 58
A et v circumflexa ilium profunda 59
A. spermatica interna et v. spermatica et n spermaticus externus 60
Colon descendens 61
Omentum majus 62
M. transversus abdominis 63
Intestinum ileum 64
Fascia transversalis 65
Mesenterium 66
Intestinum ileum 67
A et v epigastrica inferior 68
Intestinum ileum 69
Lig umbilicale laterale 70
Intestinum ileum 71
Lig umbilicale medium 72

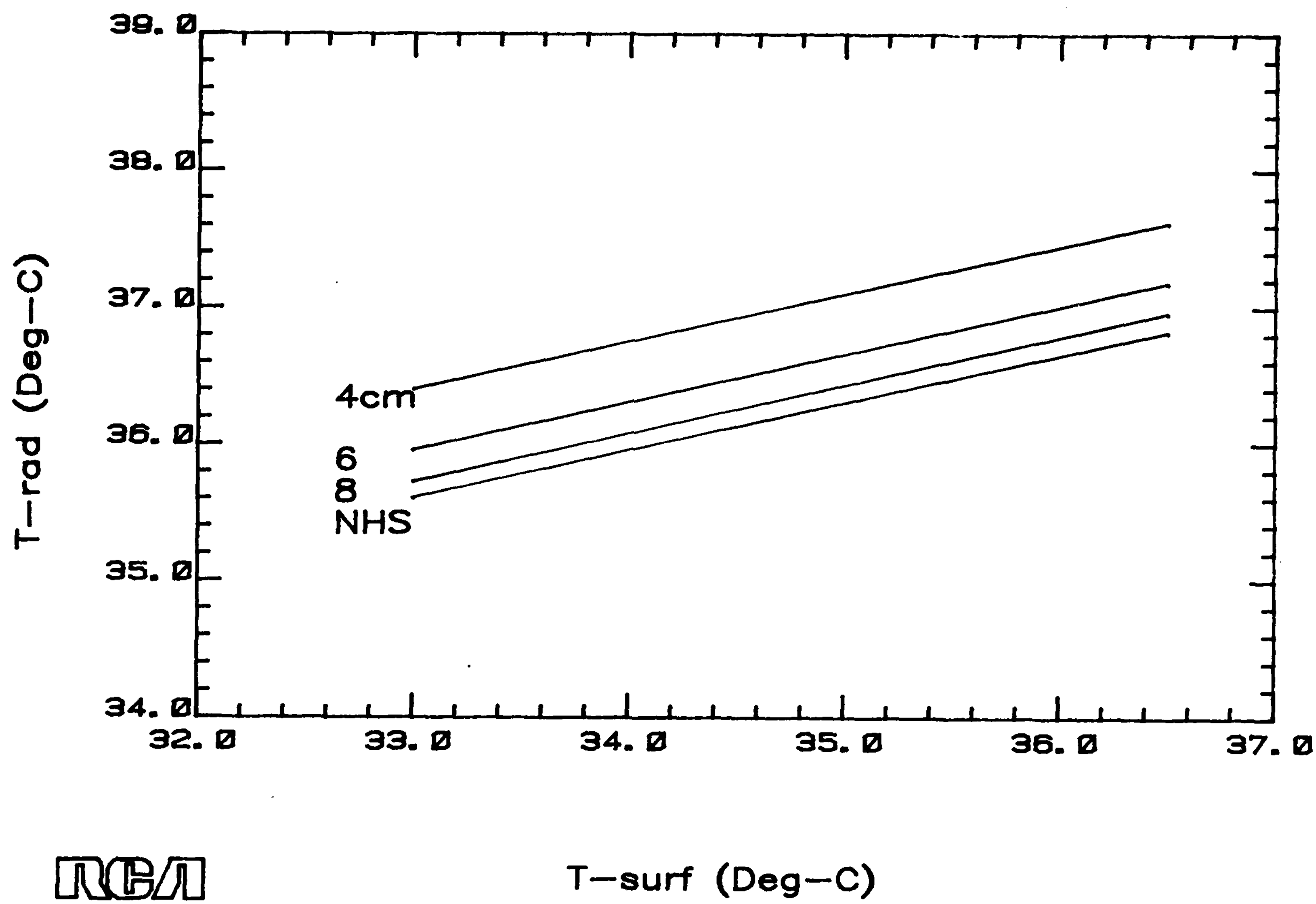
SECTION 38


PROG/ME/RAD3
1:39pm FEB. 24 1984
Radiometric Simulation
Freq. TF(rad) TB(rad) T(art)
800. 36.61 35.33 37.00
4000. 35.89 34.60 37.00
TF(diff)= .720 TB(diff)= .735
Temperature (C)
43.00
41.00
39.00
37.00
35.00
33.00
0.00
4.00
8.00
12.00
16.00
20.00
Depth (cm)

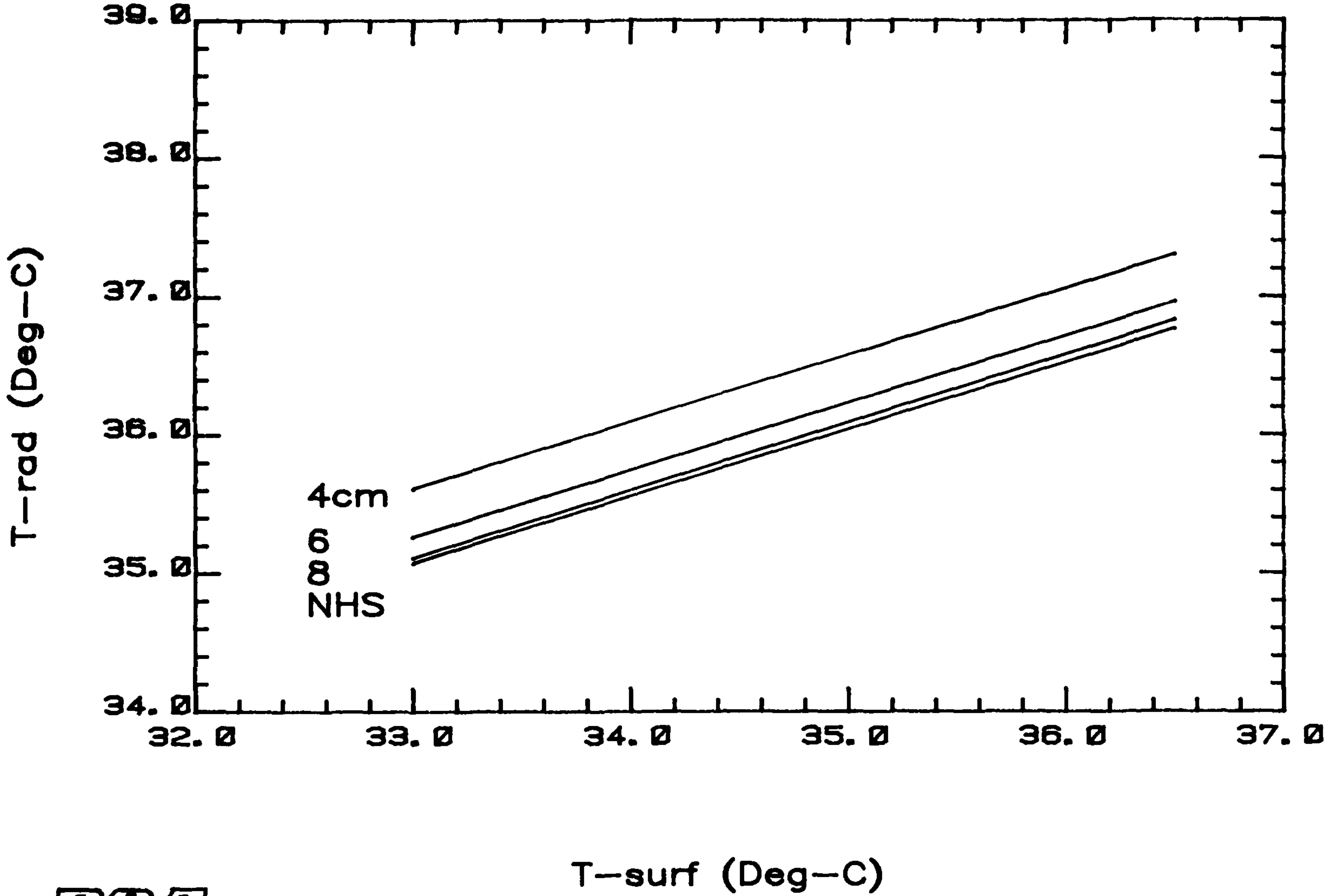

PROG/ME/RAD3
1:36pm FEB. 24 1984
Radiometric Simulation
Freq. TF(rad) TB(rad) T(art)
800. 36.05 35.37 37.00
4000. 35.40 34.61 37.00
TF(diff)= .649 TB(diff)= .757
Temperature (C)
33.00
35.00
37.00
39.00
41.00
43.00
0.00
4.00
8.00
12.00
16.00
20.00
Depth (cm)


PROG/ME/RAD3
1:33pm FEB. 24 1984
Radiometric Simulation
Freq. TF(rad) TB(rad) T(art)
800. 35.78 35.46 37.00
4000. 35.20 34.65 37.00
TF(diff)= .579 TB(diff)= .810
Temperature (C)
33.00
35.00
37.00
39.00
41.00
43.00
0.00
4.00
8.00
12.00
16.00
20.00
Depth (cm)

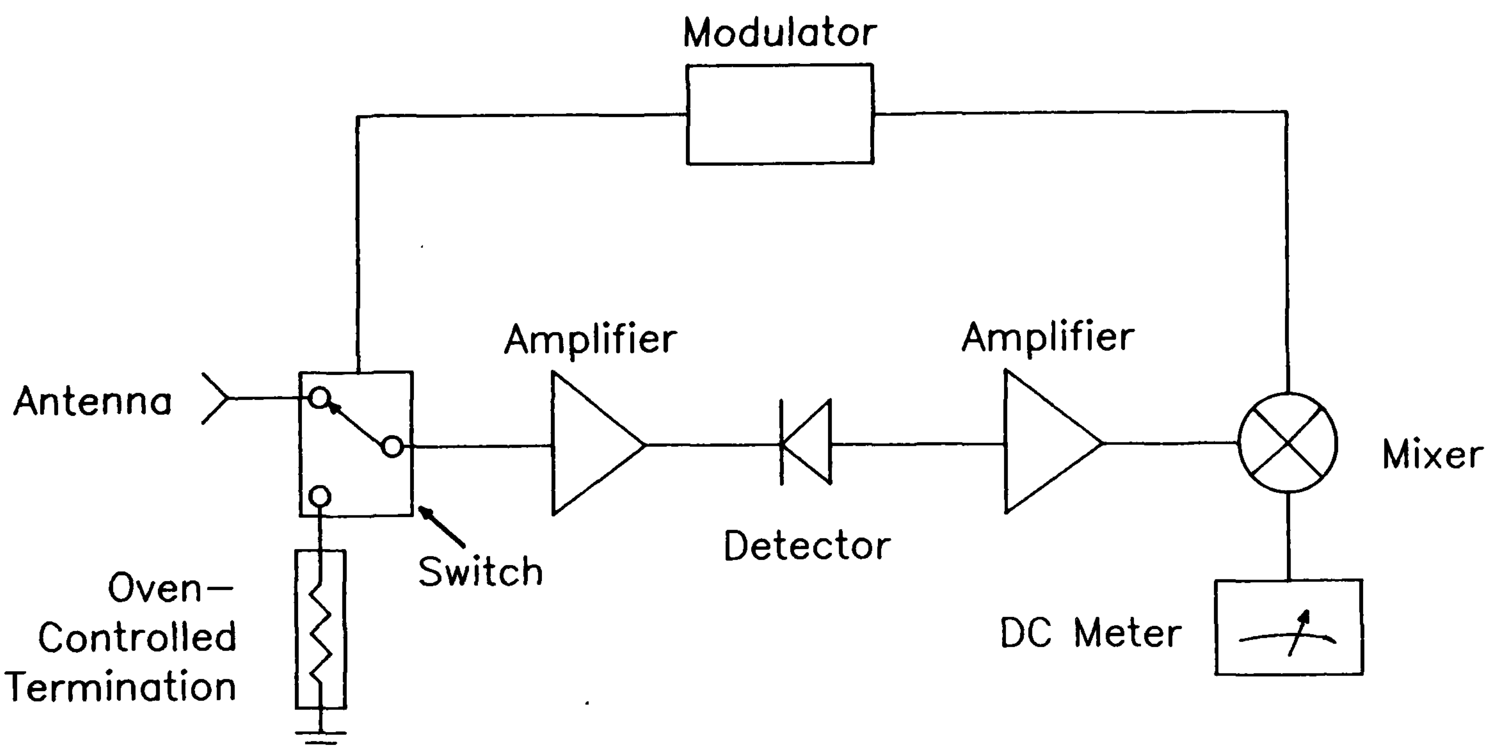
800 MHz Radiometer Simulation

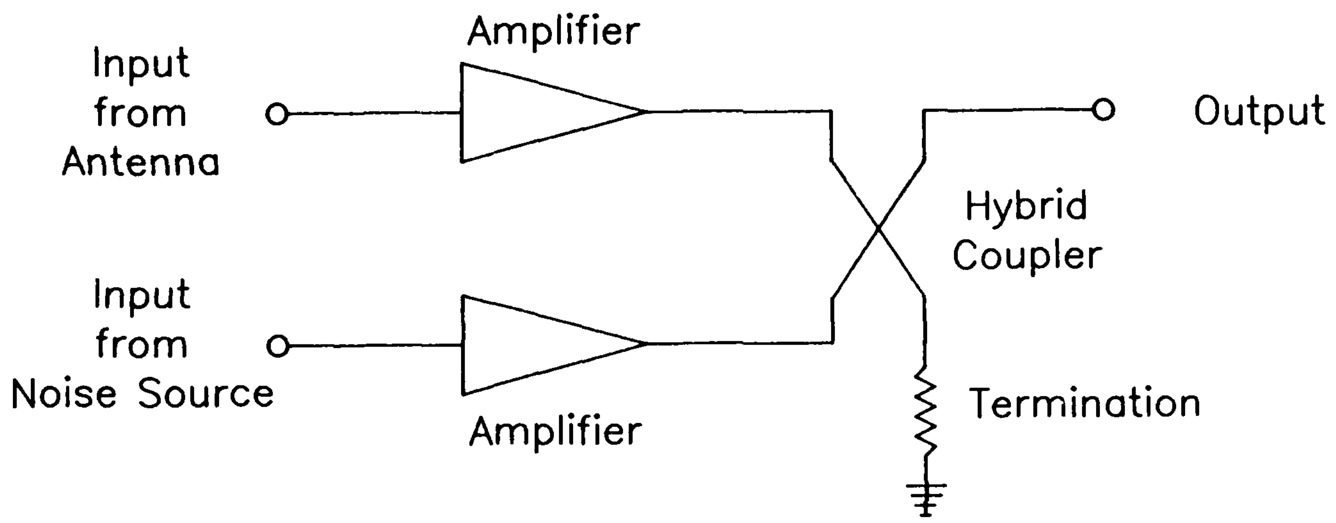


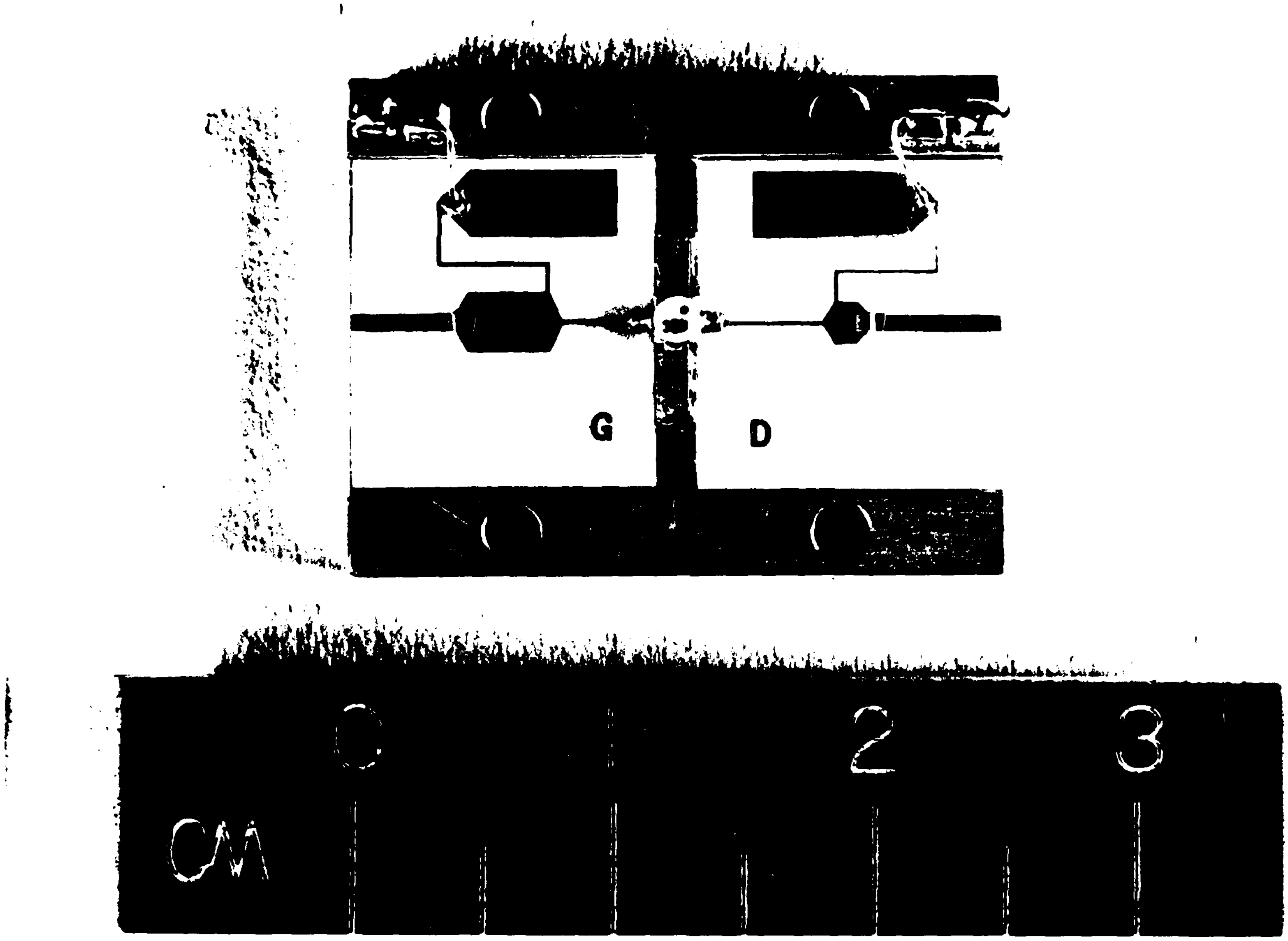
4000 MHz Radiometer Simulation

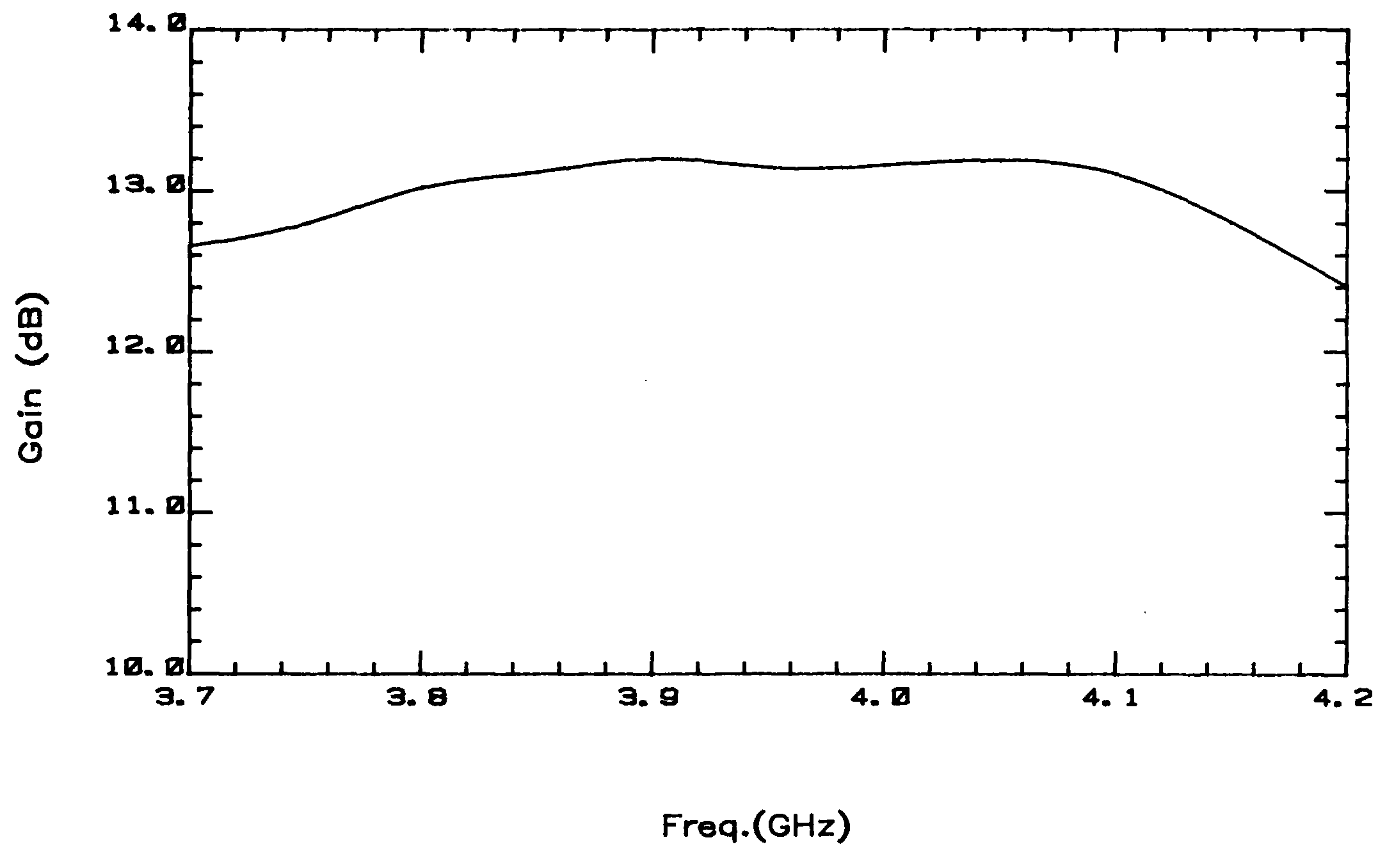


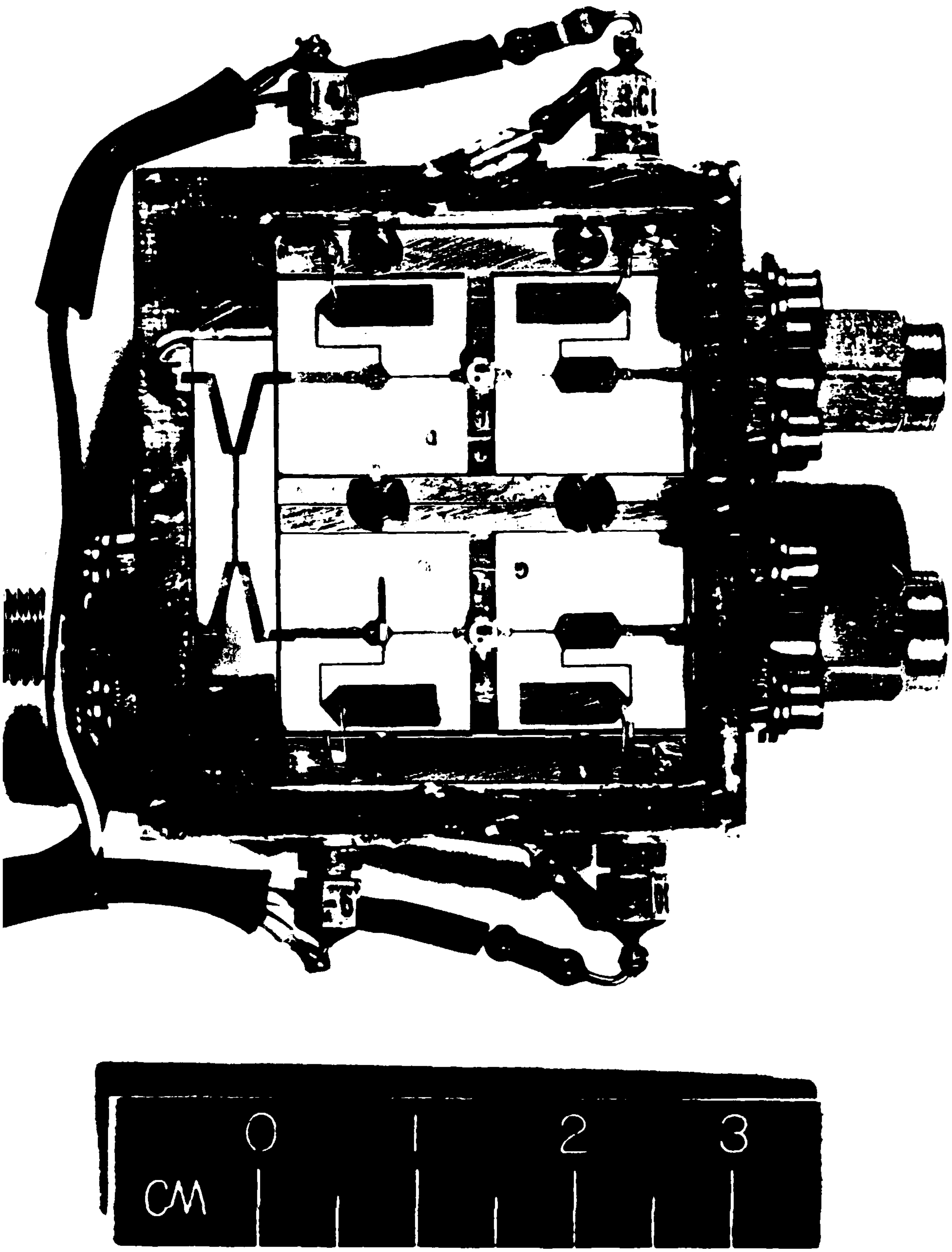
RCA

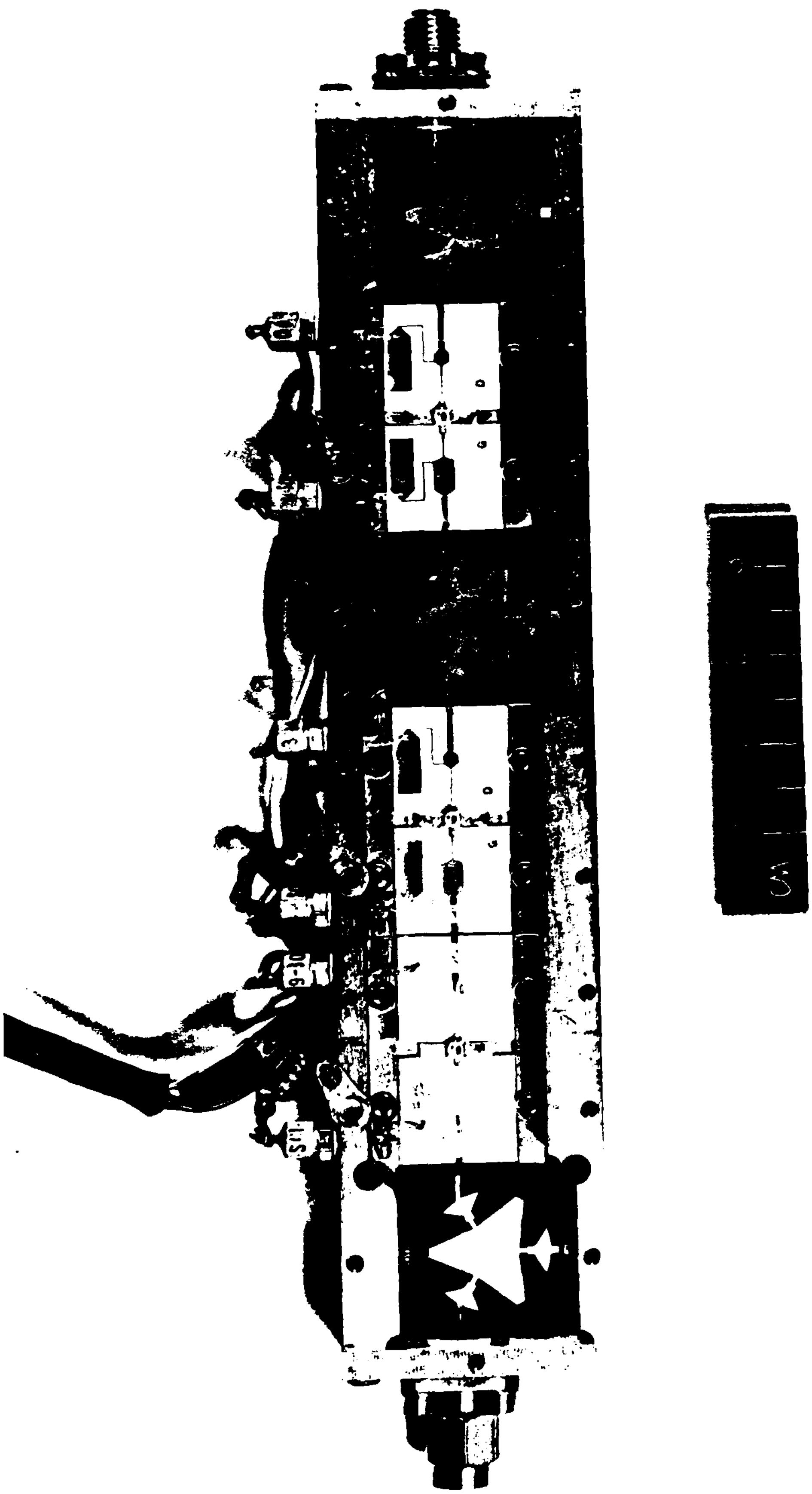

Modulator
Amplifier
Amplifier
Antenna
Mixer
Detector
Switch
Oven–
Controlled
Termination
DC Meter

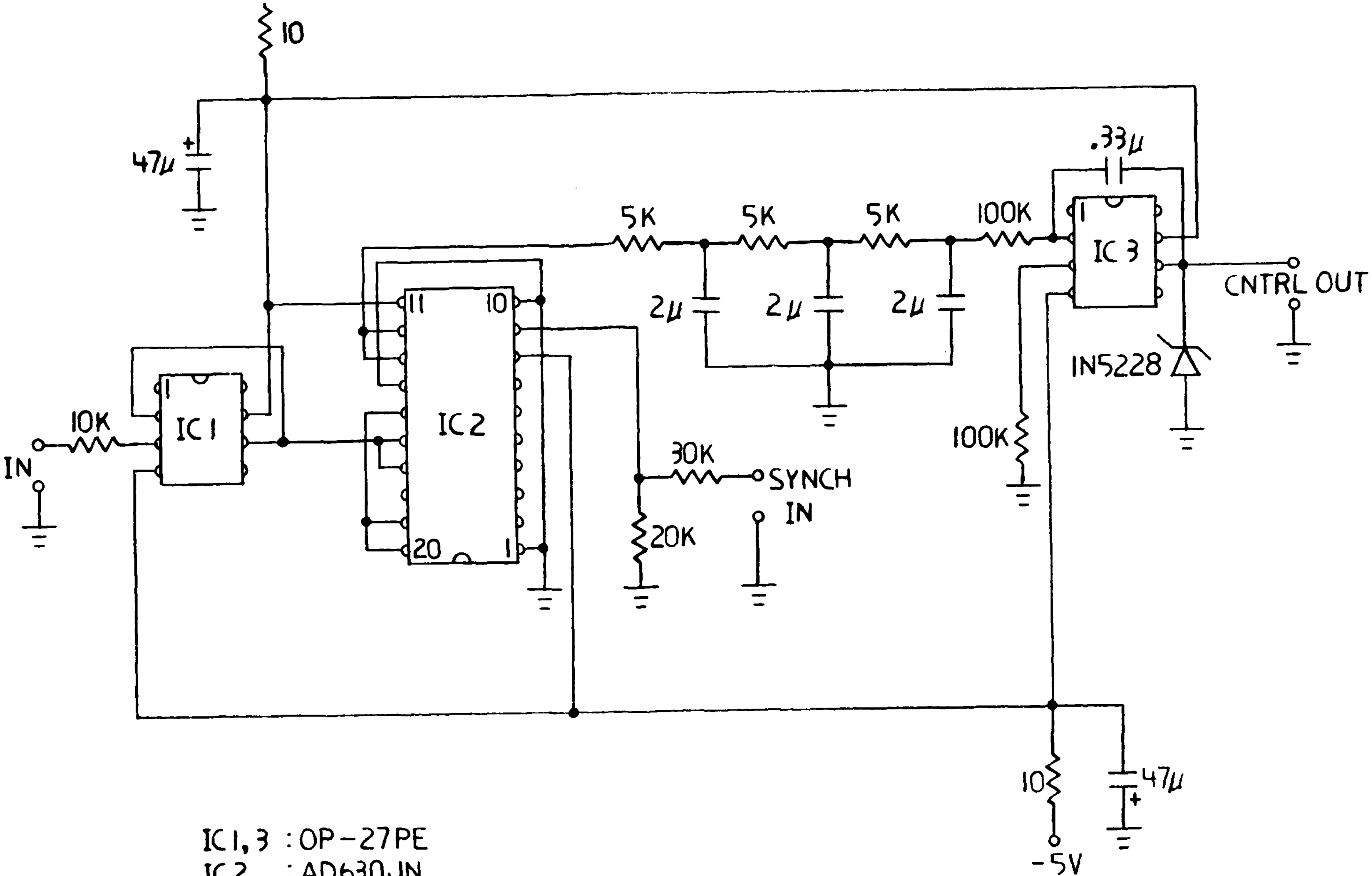

Input
from
Antenna
Amplifier
Output
Hybrid
Coupler
Input
from
Noise Source
Amplifier
Termination


G
D
CM
2
3

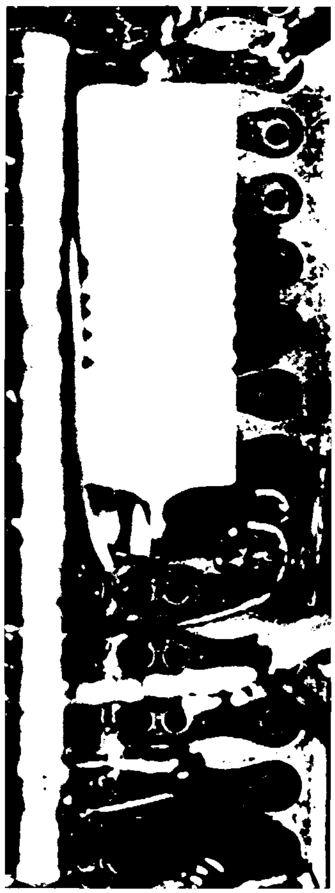

14.0
13.0
12.0
11.0
10.0
Gain (dB)
3.7
3.8
3.9
4.0
4.1
4.2
Freq.(GHz)

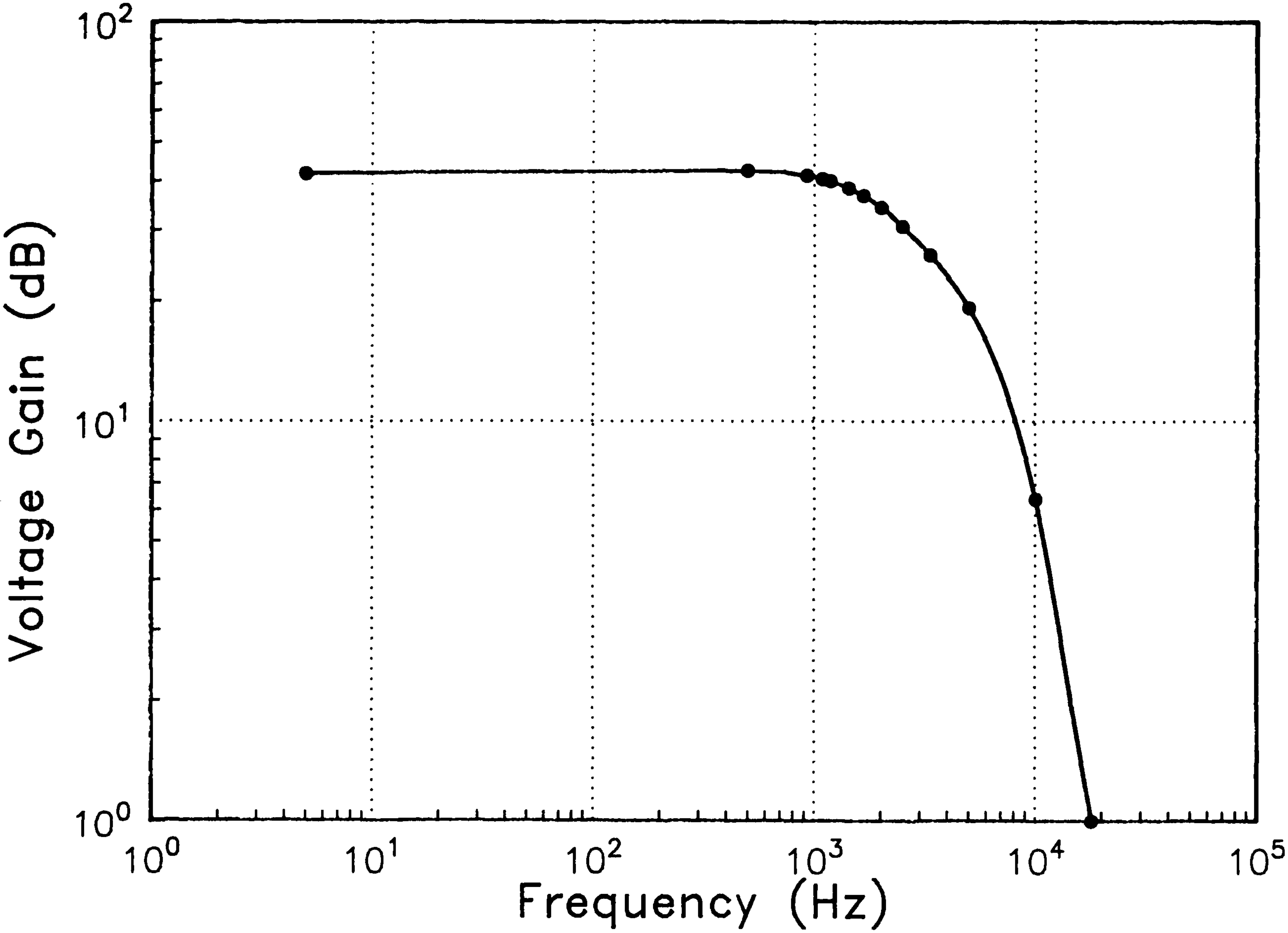

0 1 2 3
CM



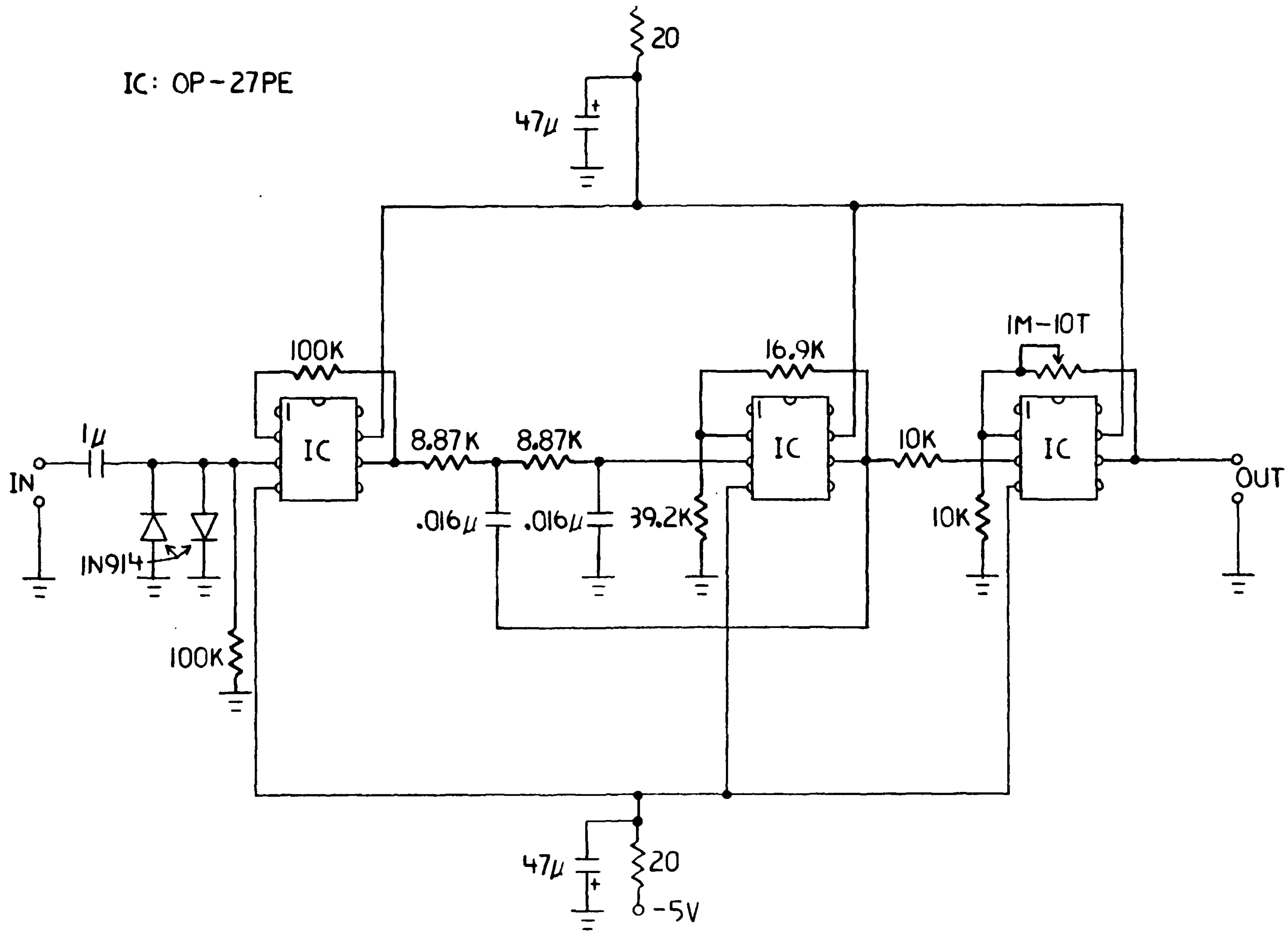


IC1, 3 : OP-27PE
IC2 : AD630JN

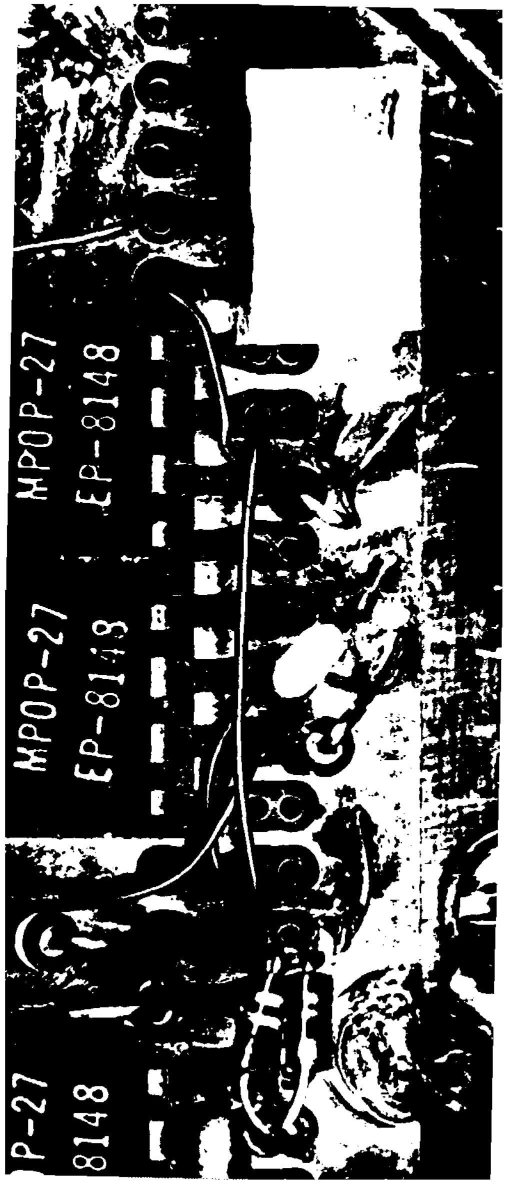




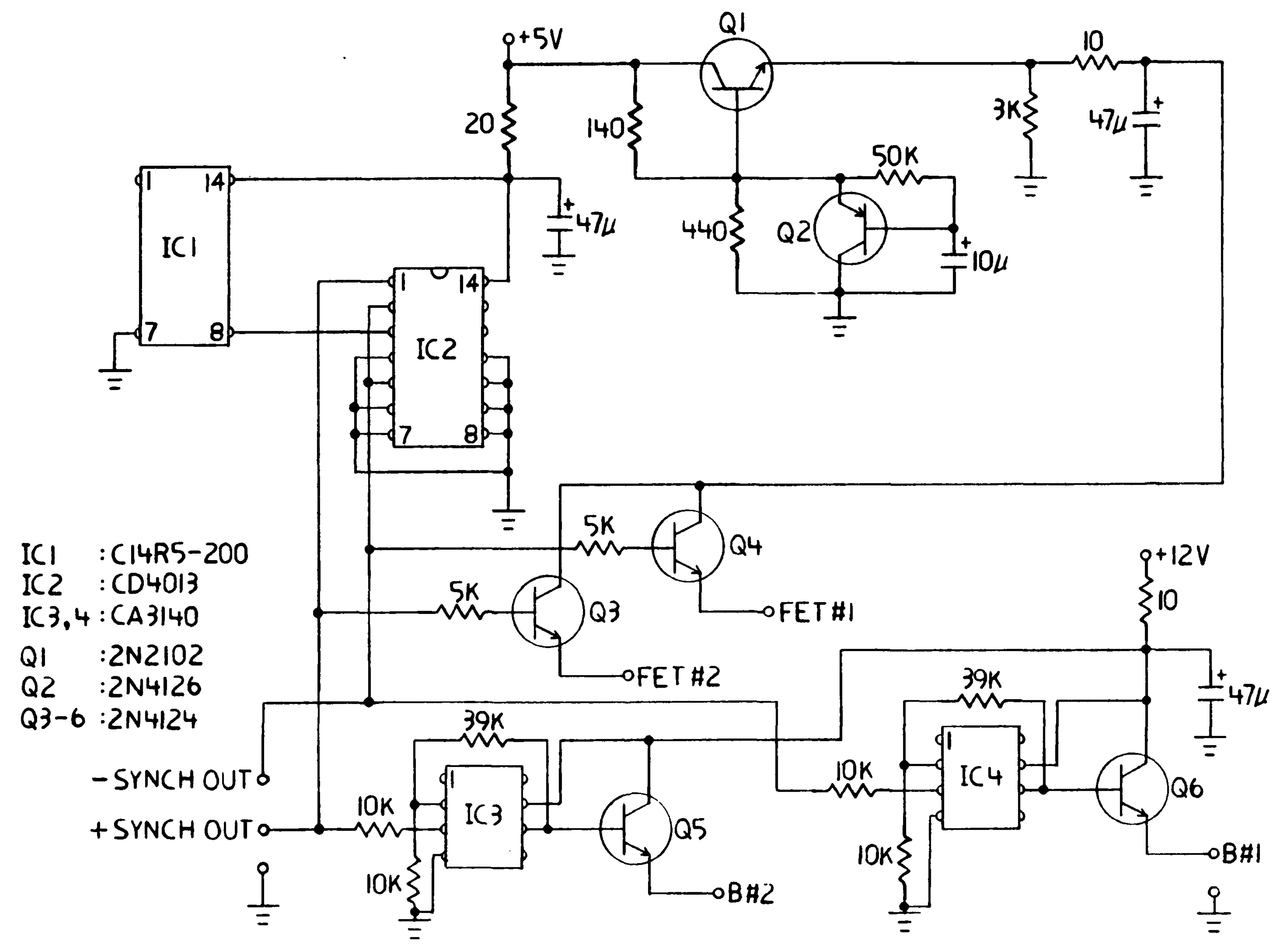
Voltage Gain (dB)
Frequency (Hz)
10^2
10^1
10^0
10^0
10^1
10^2
10^3
10^4
10^5

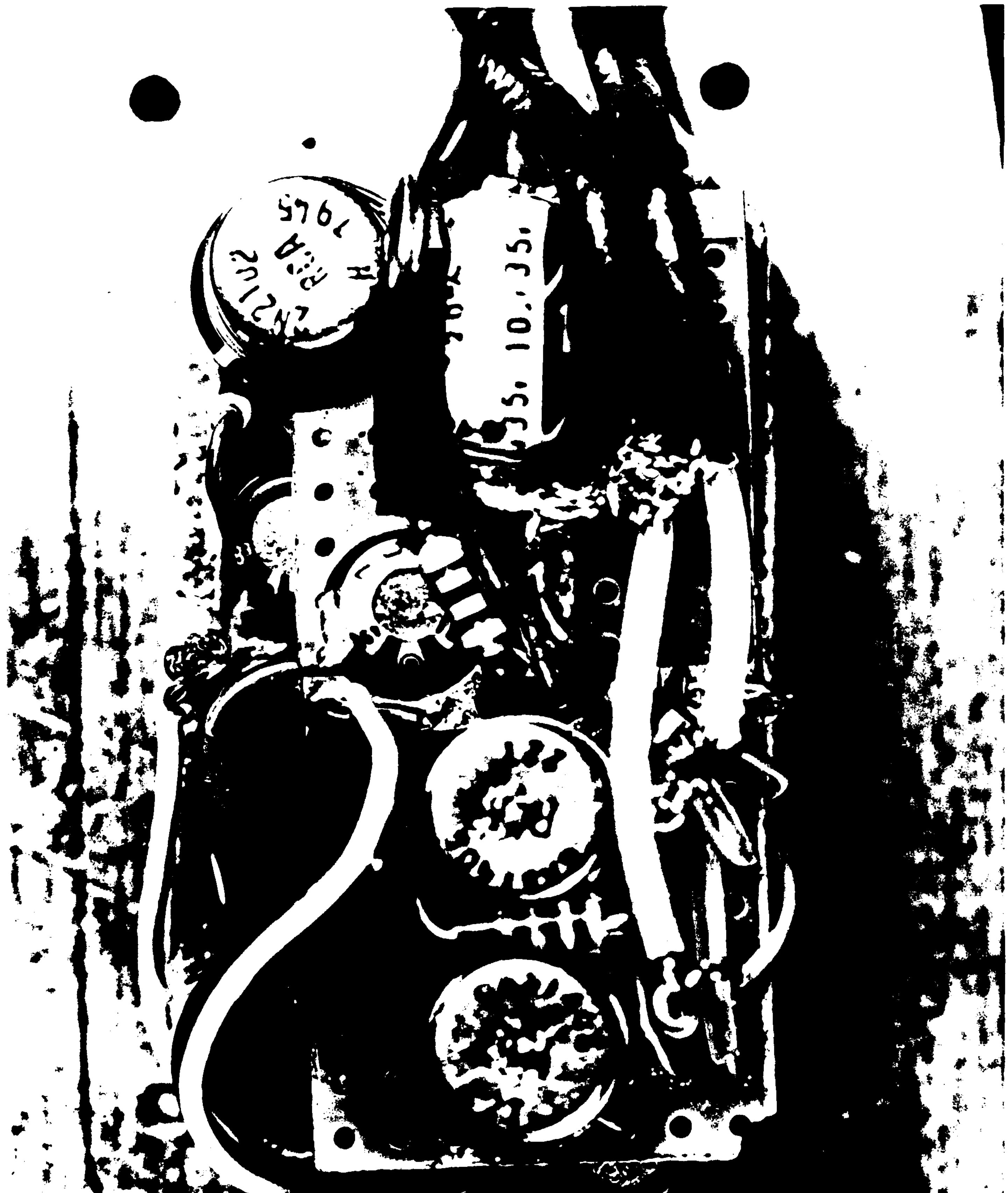


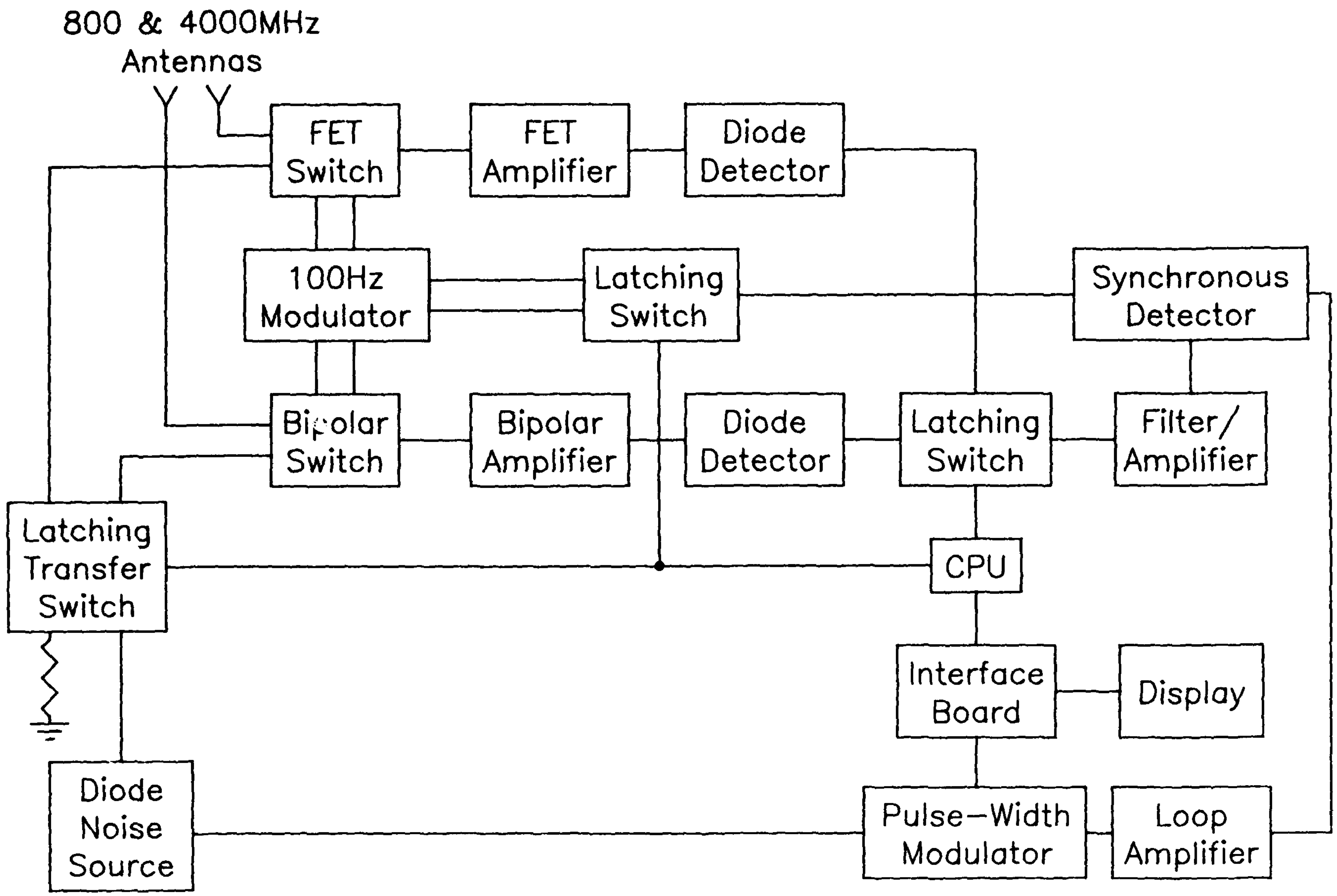
IC: OP-27PE
20
47µ
100K
16.9K
1M-10T
1µ
IN
IC
8.87K
8.87K
10K
OUT
1N914
.016µ
.016µ
39.2K
10K
100K
47µ
20
-5V

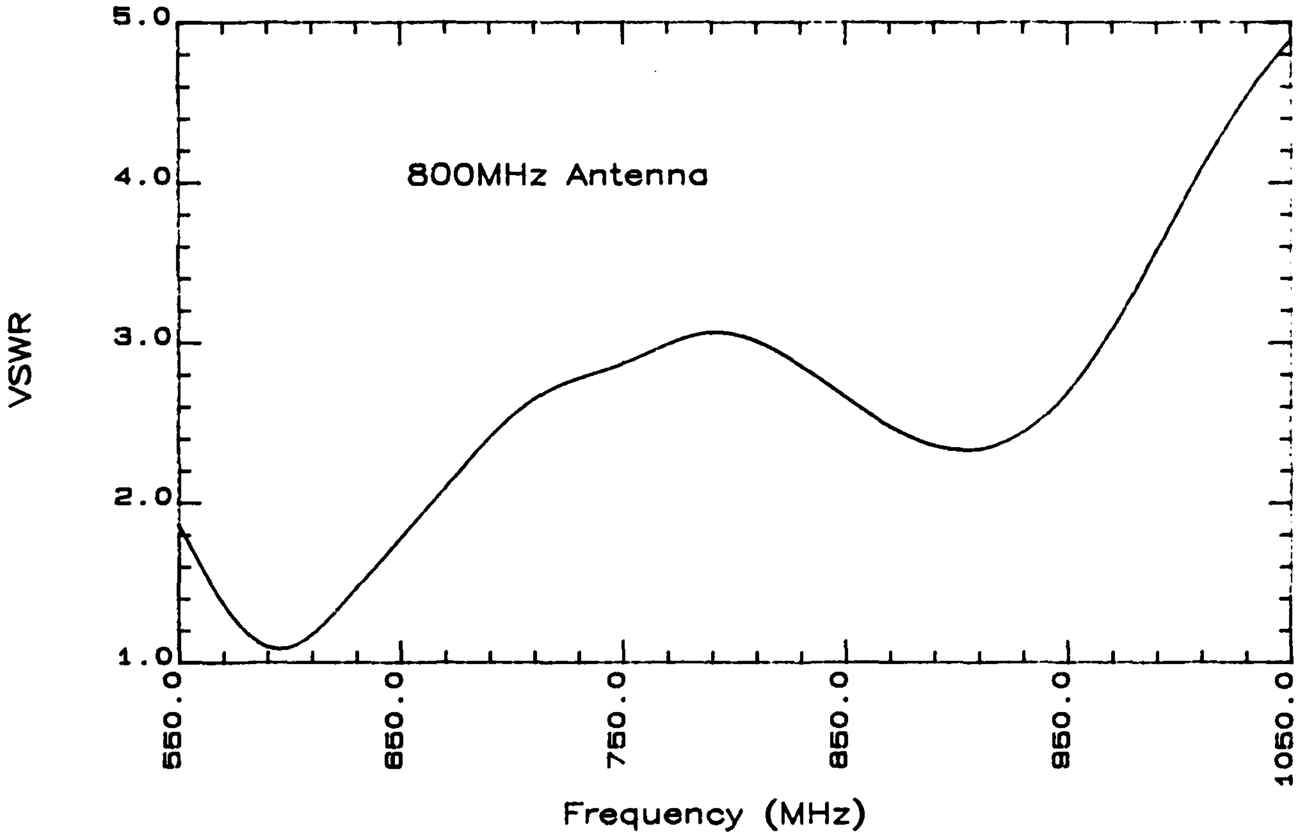


MPOP-27
EP-8148
MPOP-27
EP-8148
P-27
8148

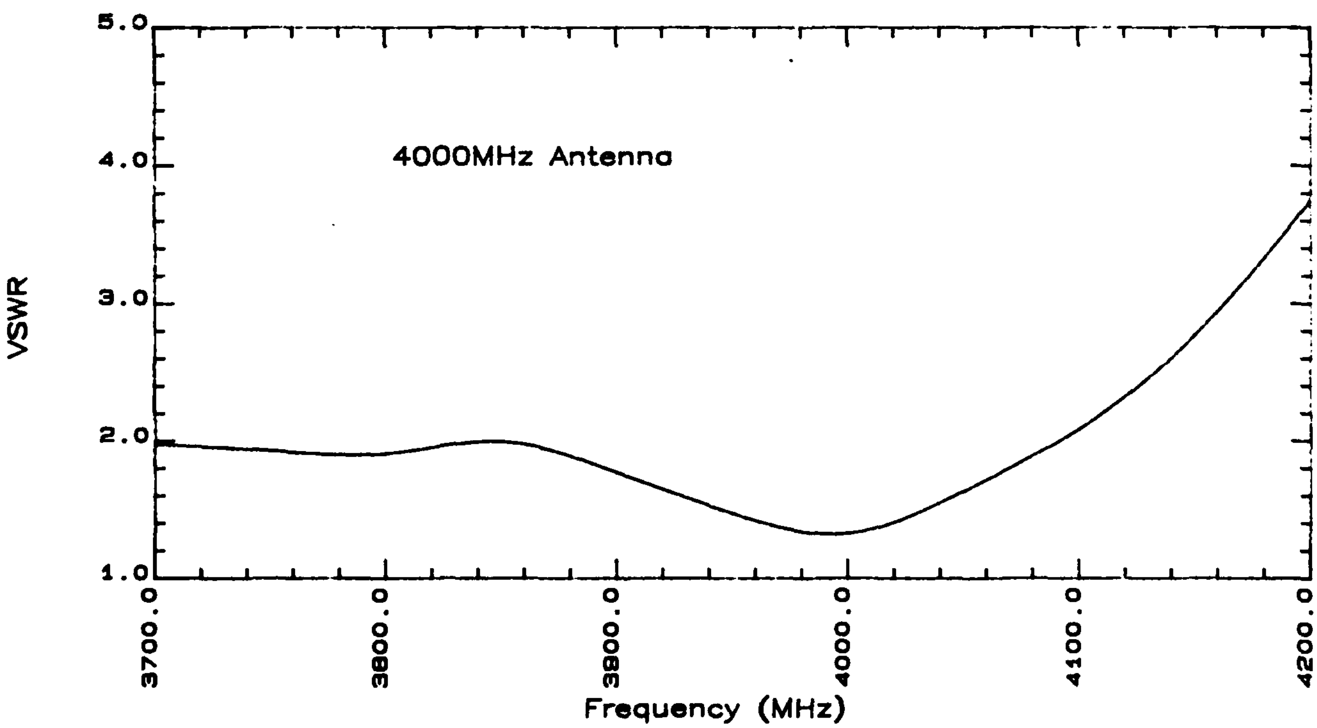

+5V
Q1
10
20
140
3K
47µ
50K
440
Q2
10µ
IC1
14
7
8
IC2
IC1 :C14R5-200
IC2 :CD4013
IC3,4 :CA3140
Q1 :2N2102
Q2 :2N4126
Q3-6 :2N4124
5K
Q4
Q3
FET#1
FET#2
+12V
39K
10K
IC3
IC4
Q5
Q6
B#1
B#2
-SYNCH OUT
+SYNCH OUT



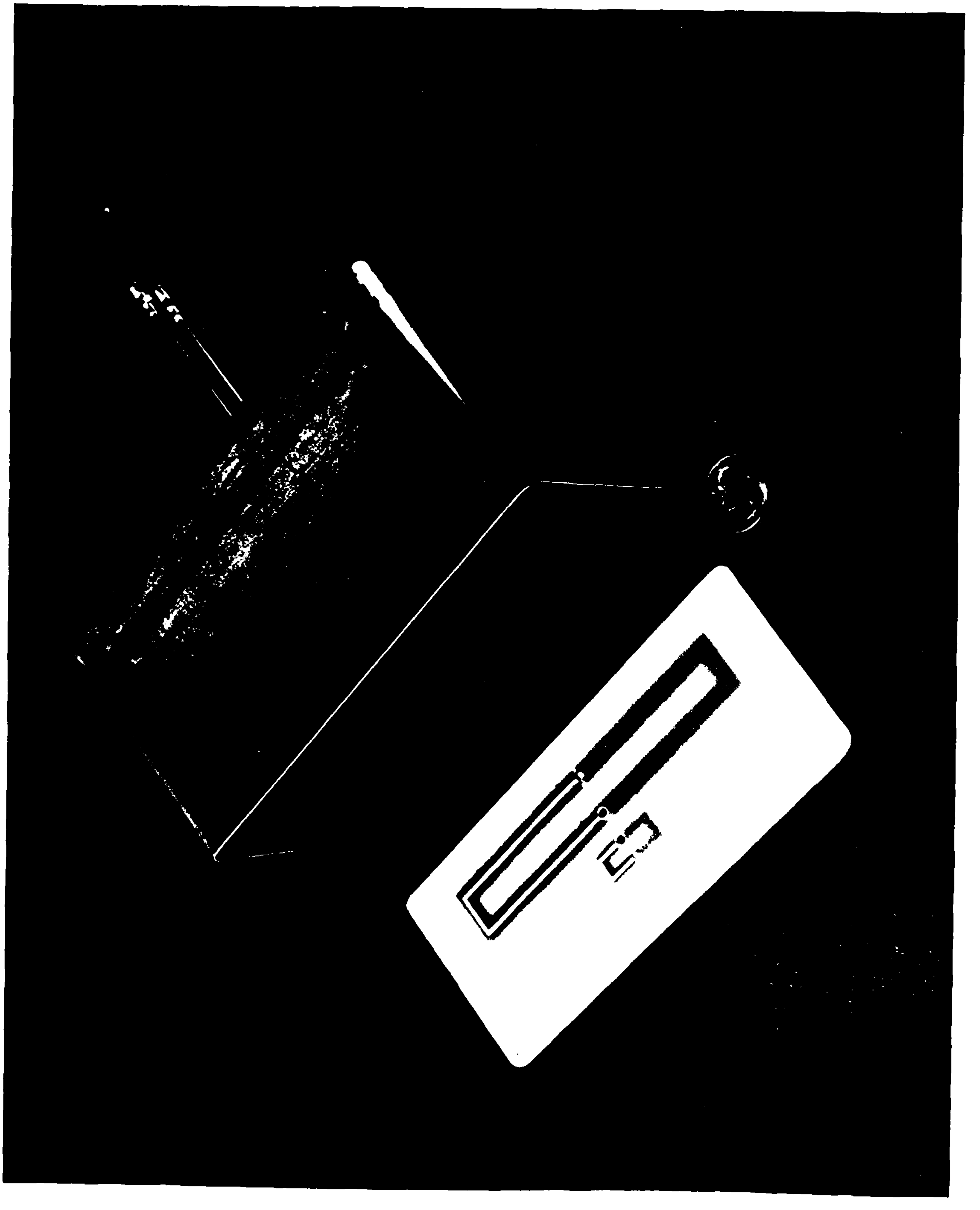

800 & 4000MHz
Antennas
FET Switch
FET Amplifier
Diode Detector
100Hz Modulator
Latching Switch
Synchronous Detector
Bipolar Switch
Bipolar Amplifier
Diode Detector
Latching Switch
Filter/ Amplifier
Latching Transfer Switch
CPU
Interface Board
Display
Diode Noise Source
Pulse-Width Modulator
Loop Amplifier

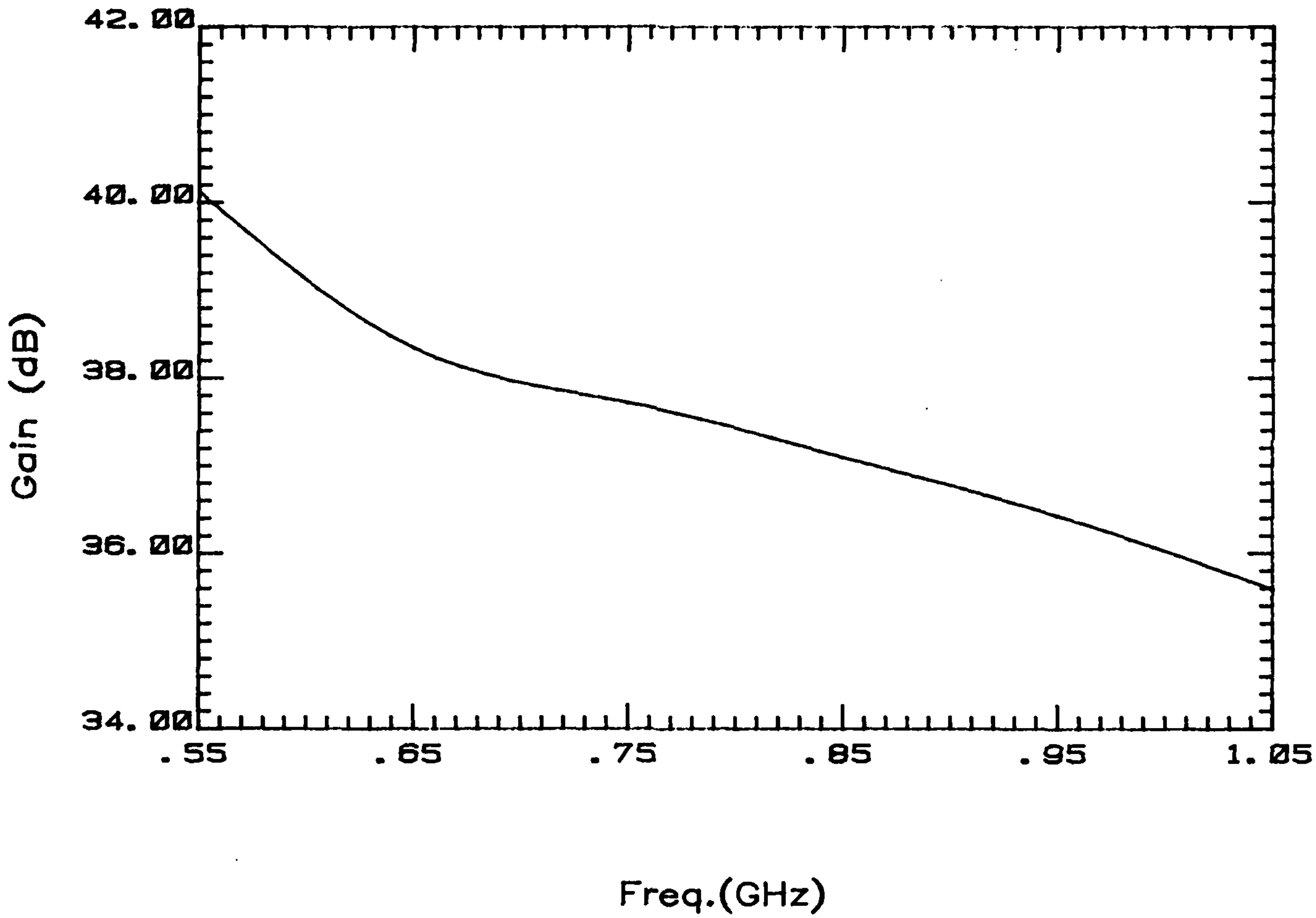


800MHz Antenna
VSWR
5.0
4.0
3.0
2.0
1.0
550.0
650.0
750.0
850.0
950.0
1050.0
Frequency (MHz)

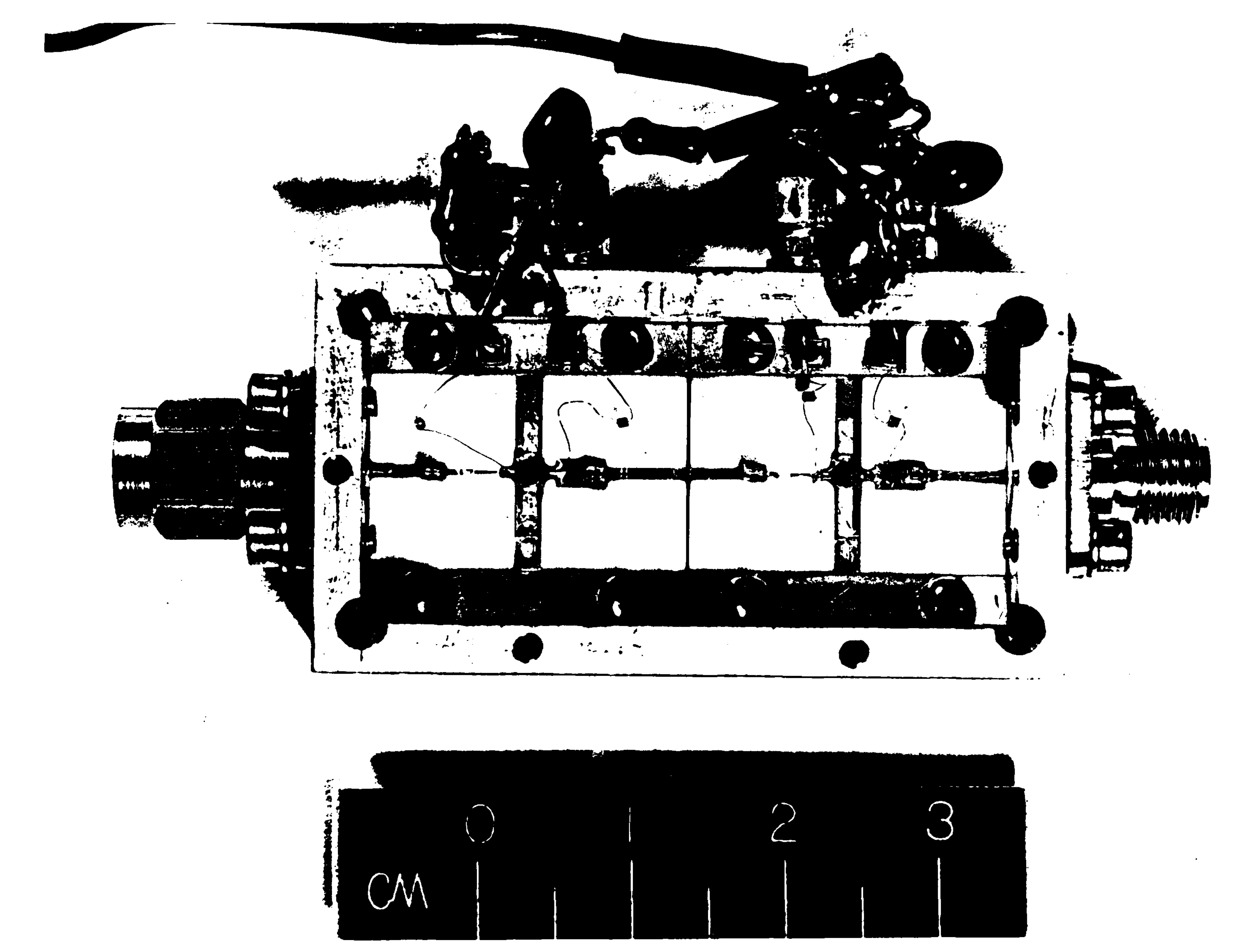


4000MHz Antenna
VSWR
5.0
4.0
3.0
2.0
1.0
3700.0
3800.0
3900.0
4000.0
4100.0
4200.0
Frequency (MHz)

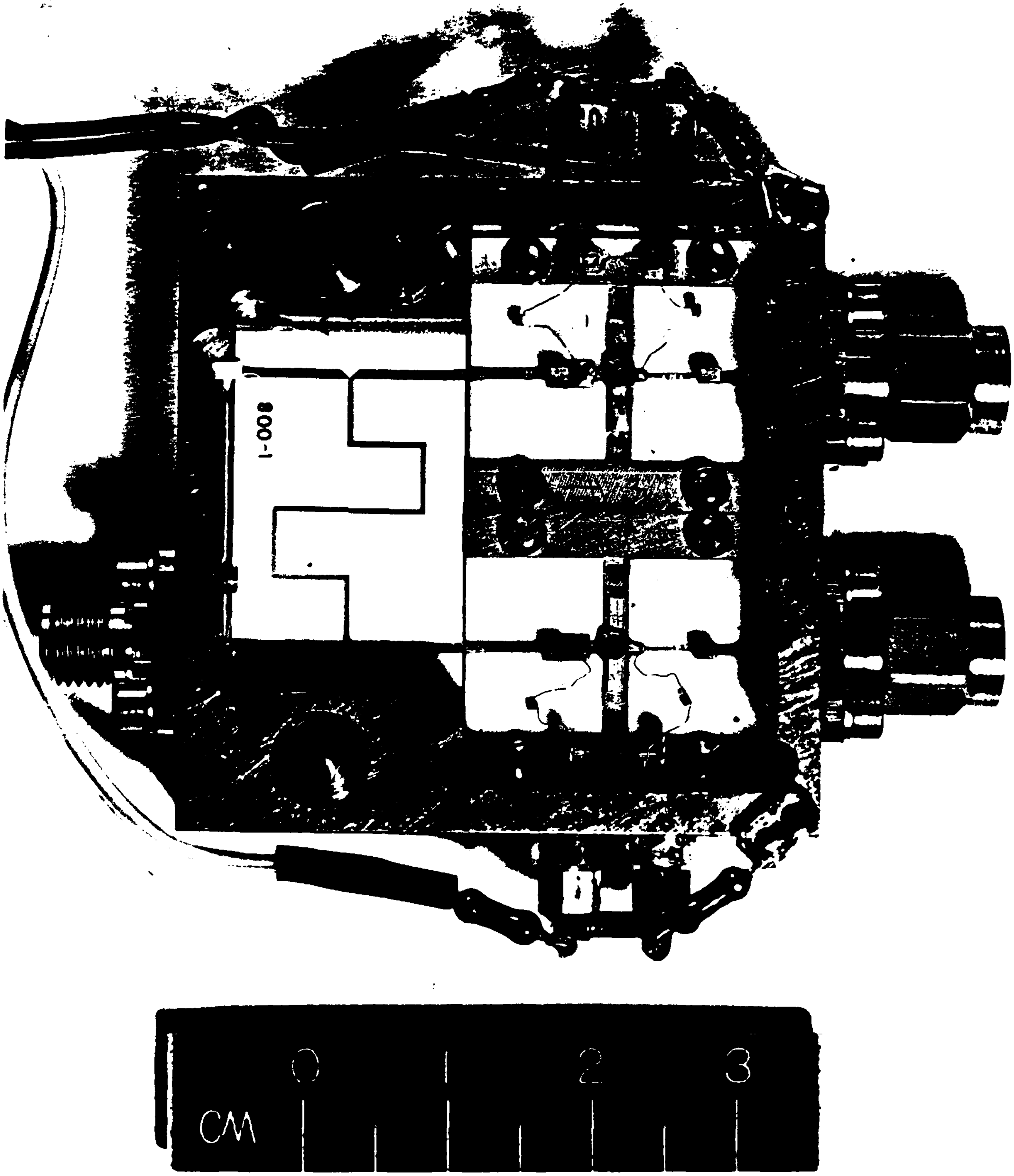


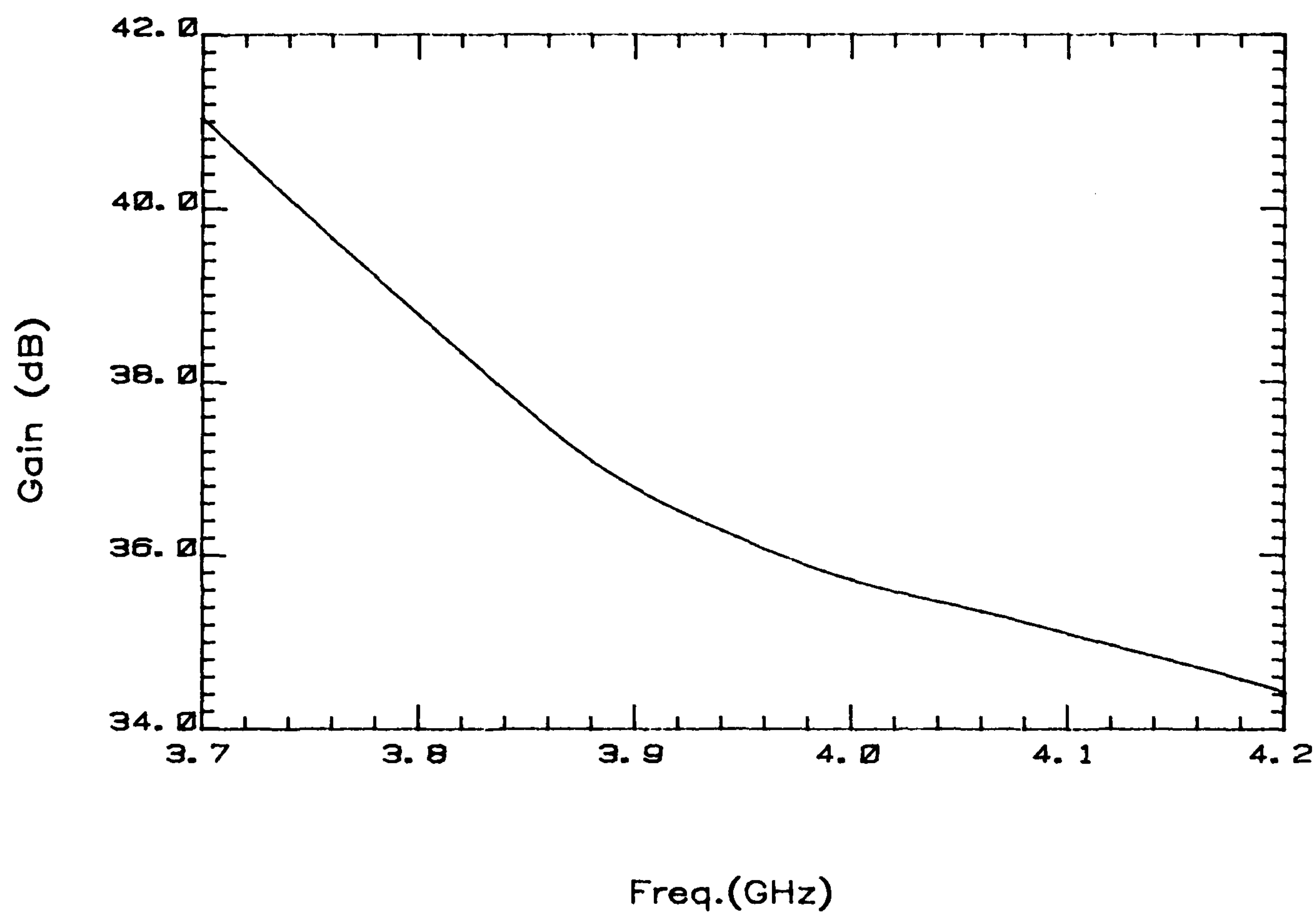


42.00
40.00
38.00
36.00
34.00
Gain (dB)
.55
.65
.75
.85
.95
1.05
Freq.(GHz)

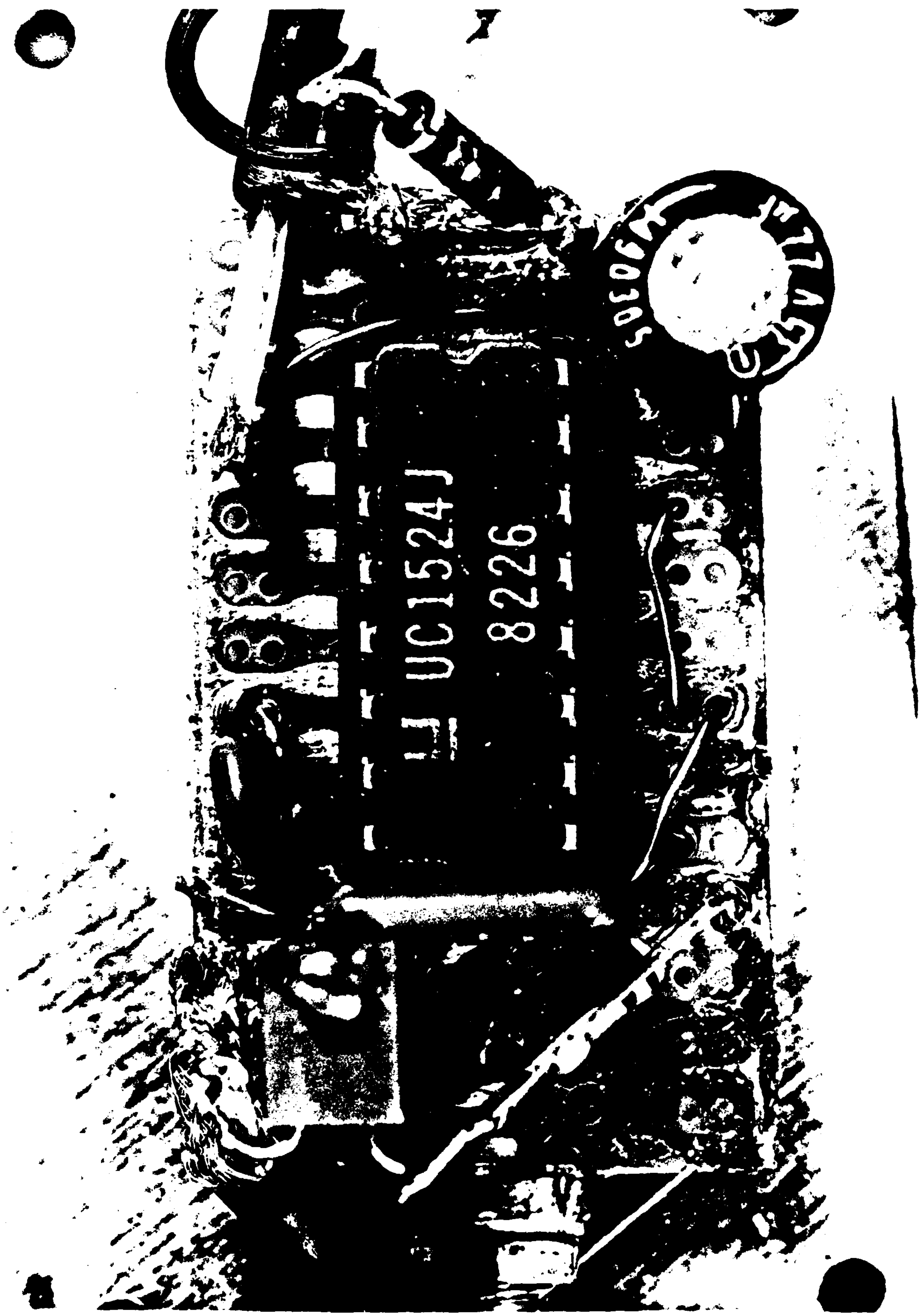


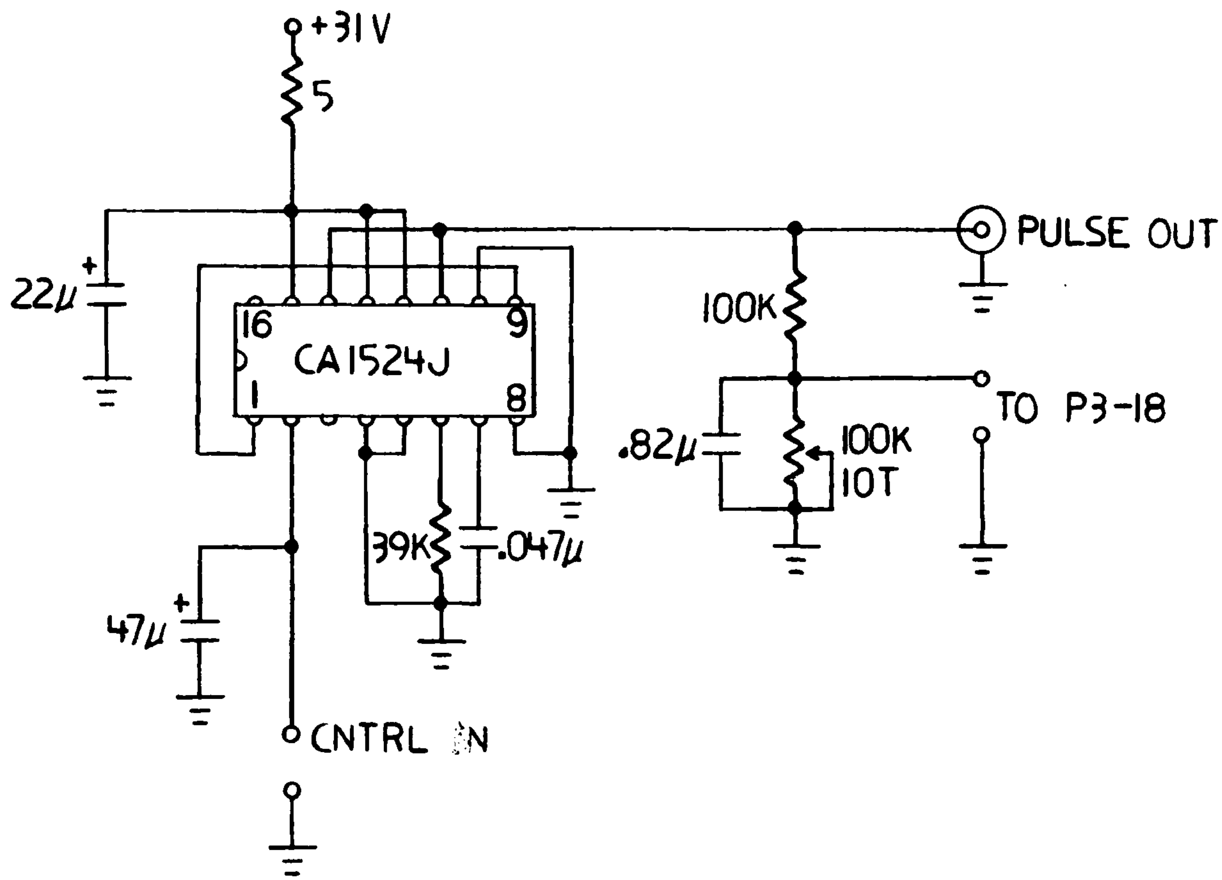
0
1
2
3
CM

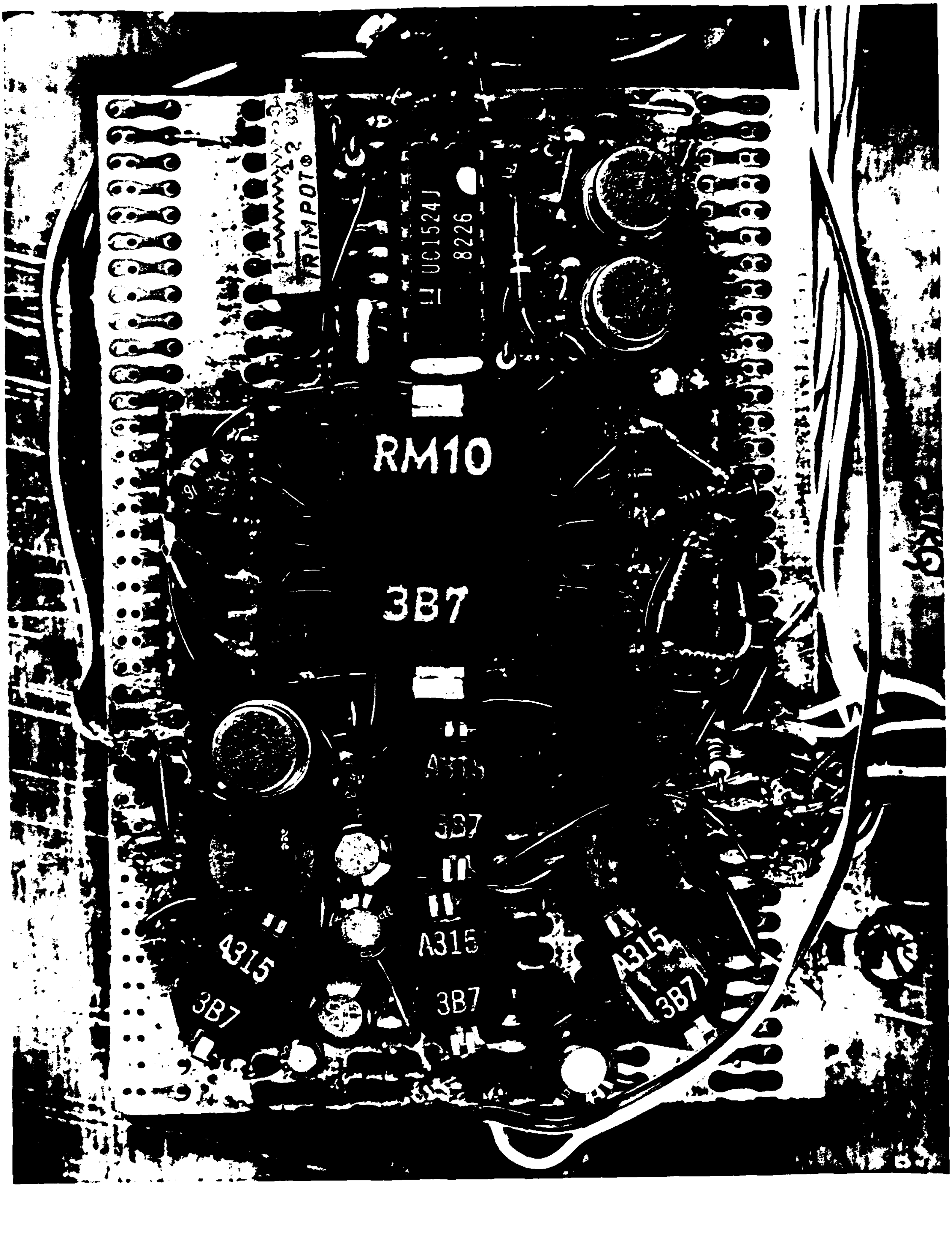

800-1
0
1
2
3
CM

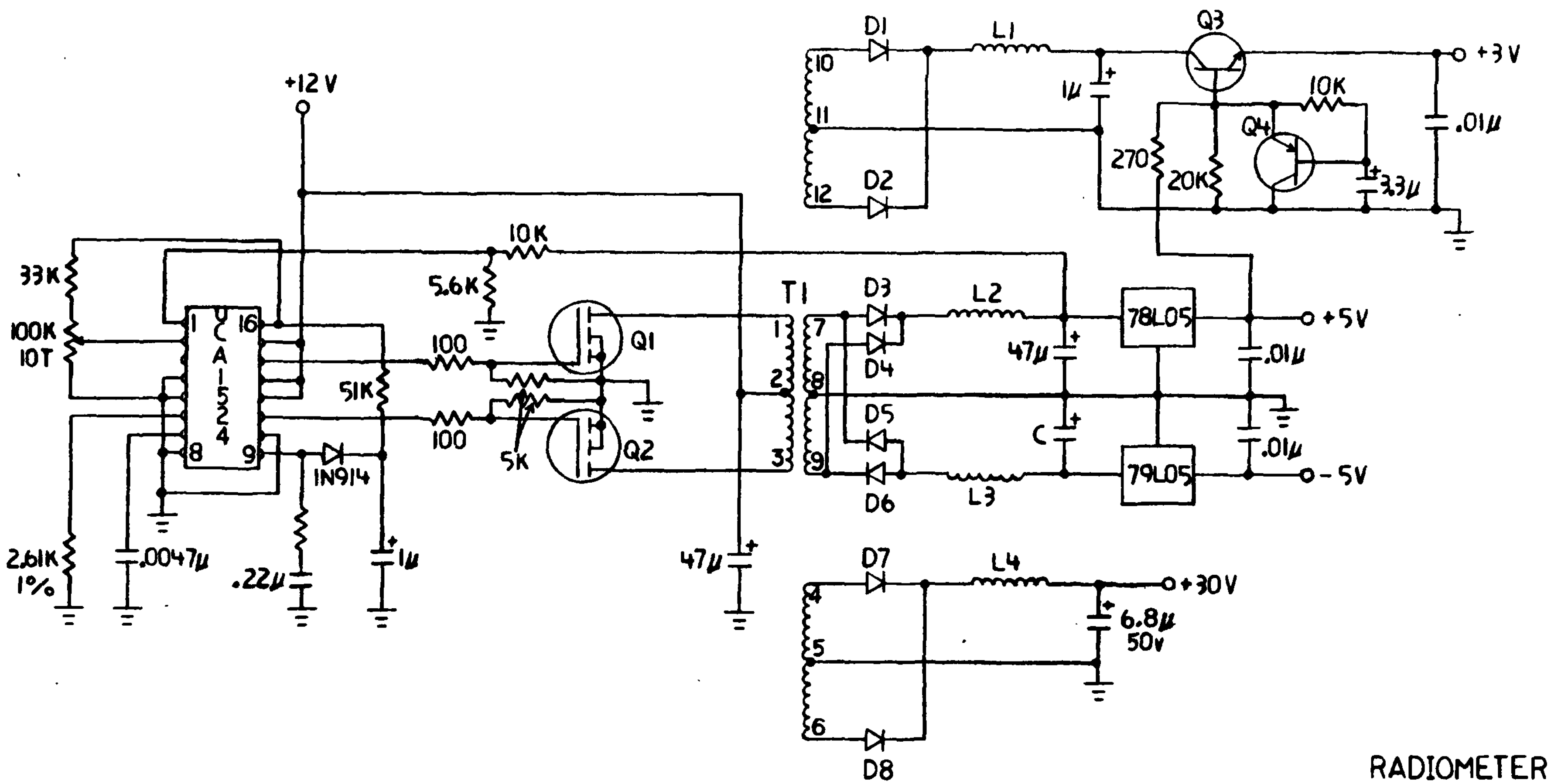


42.0
40.0
38.0
36.0
34.0
Gain (dB)
3.7
3.8
3.9
4.0
4.1
4.2
Freq.(GHz)


UC1524J
8226


+31V
5
22μ
16
9
CA1524J
1
8
47μ
39K
.047μ
CNTRL IN
PULSE OUT
100K
TO P3-18
.82μ
100K
10T


UC1524J
8226
TRIMPOT
RM10
3B7
A315
3B7
A315
3B7
A315
3B7



RADIOMETER SUPPLY

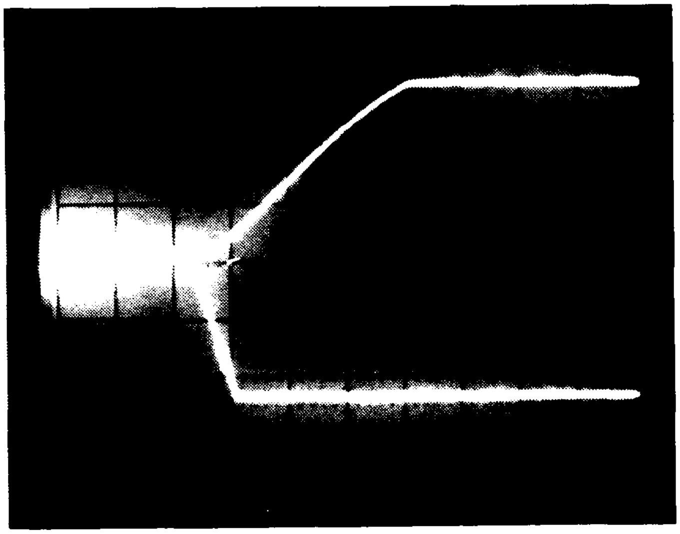
R. PAGLIONE

3-26-84

Q1, Q2 = RFL1N15
Q3 = 2N2102
Q4 = 2N4126
D1-D6 = 11DQ06
D7, D8 = UES1105
C = (2) 47µ in ‖
L1 = 1mH (56T on RM5P-A315-3B7 Core)
L3, L2 = 10mH (178T ")
L4 = 58mH (436T ")

<u>T1</u>: RM10-3B7 Core
PRIMARY = 50T (1-2 & 2-3)
SECONDARY [+3V] = 20T (10-11 & 11-12)
" ±5V = 50T (7-8 & 8-9)
" +30V = 200T (4-5 & 5-6)

(a)



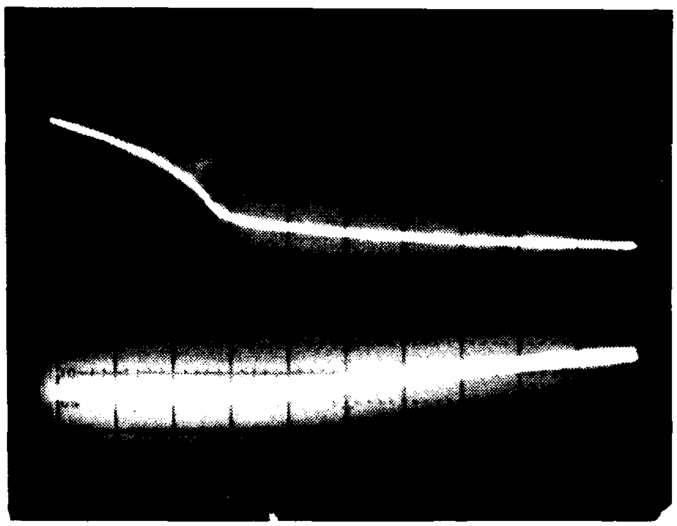
drain voltage
(1v/div)

turn-on

gate voltage
(2v/div)

time scale=20msec/div

(b)

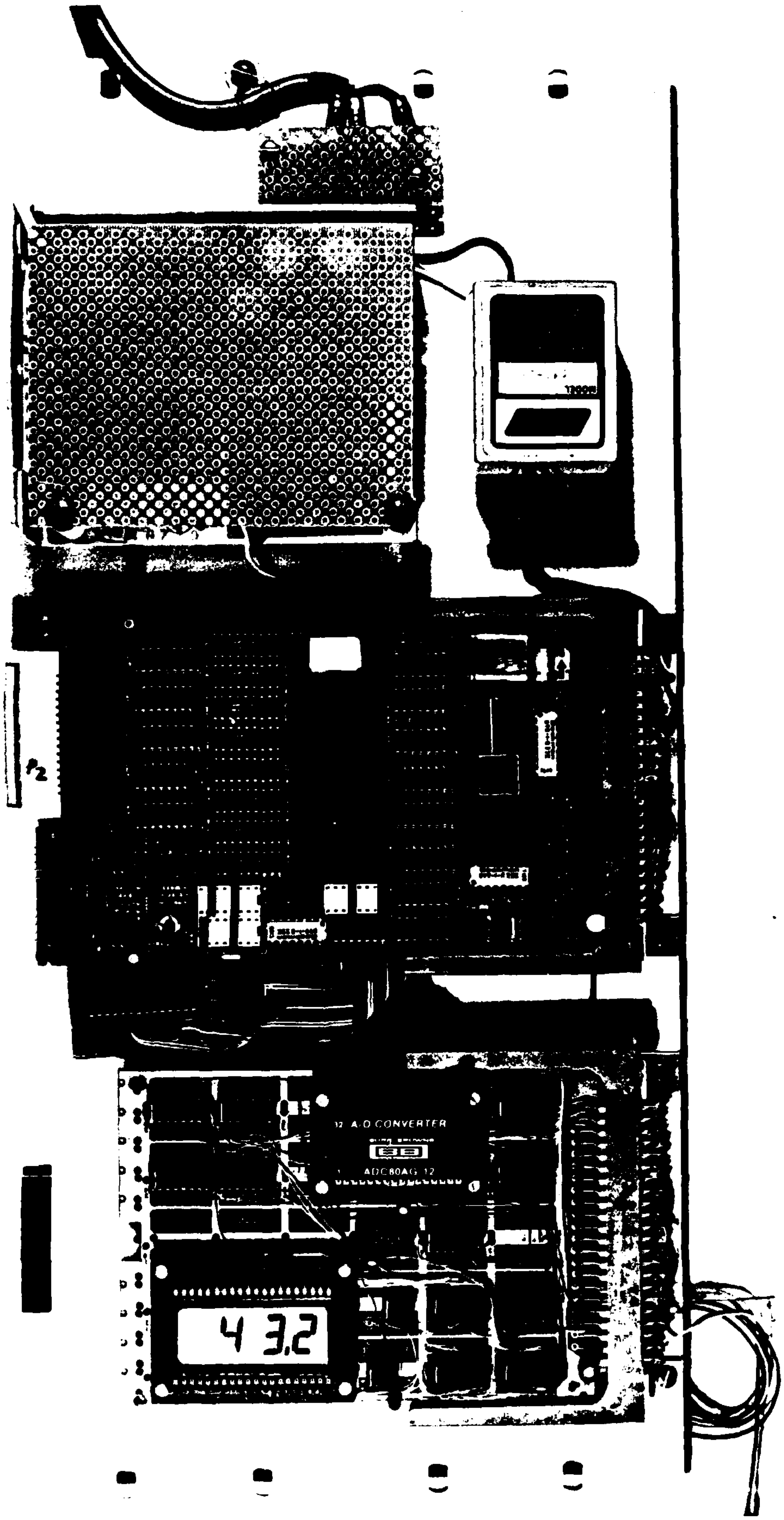


drain voltage
(1v/div)

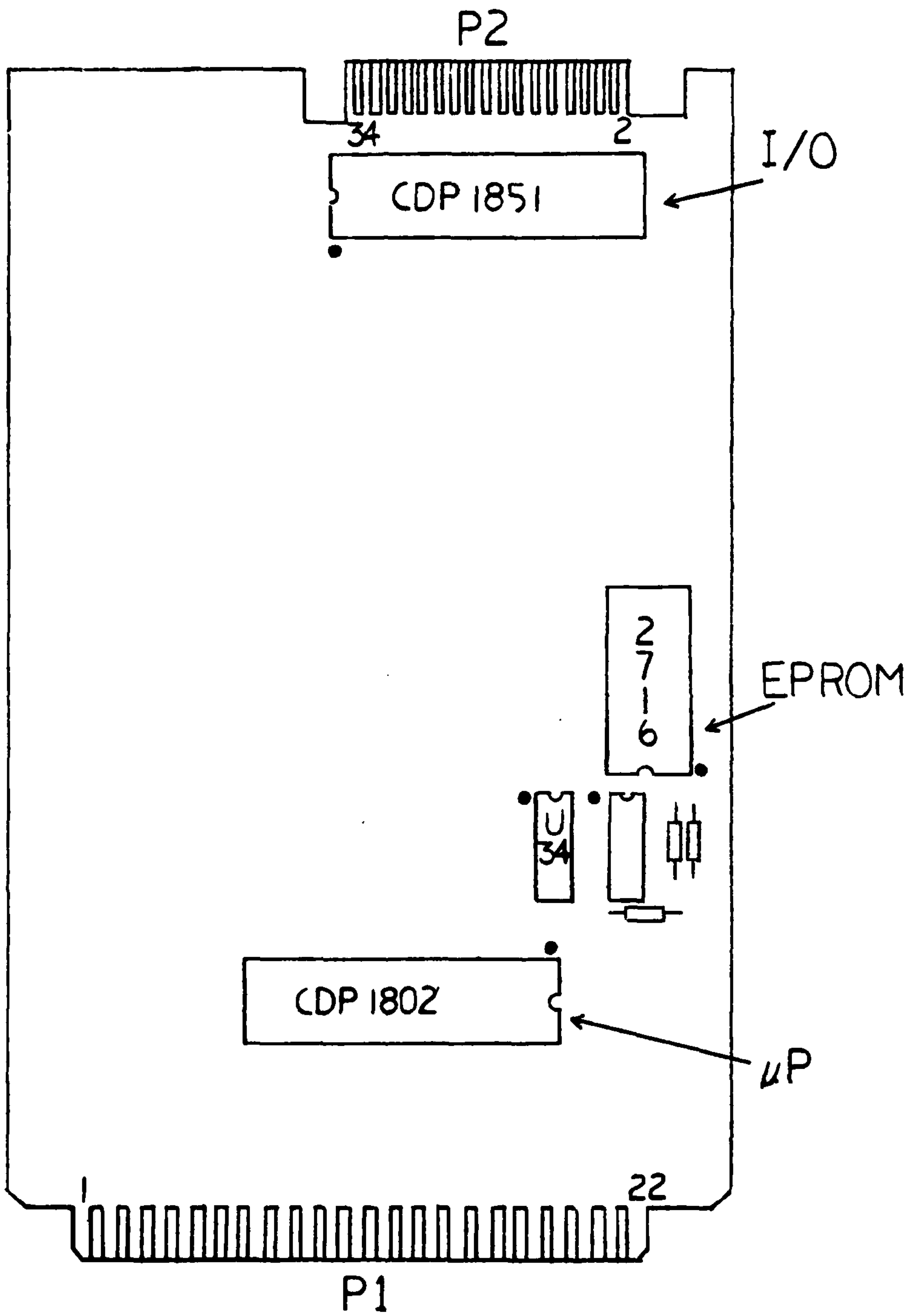
turn-off

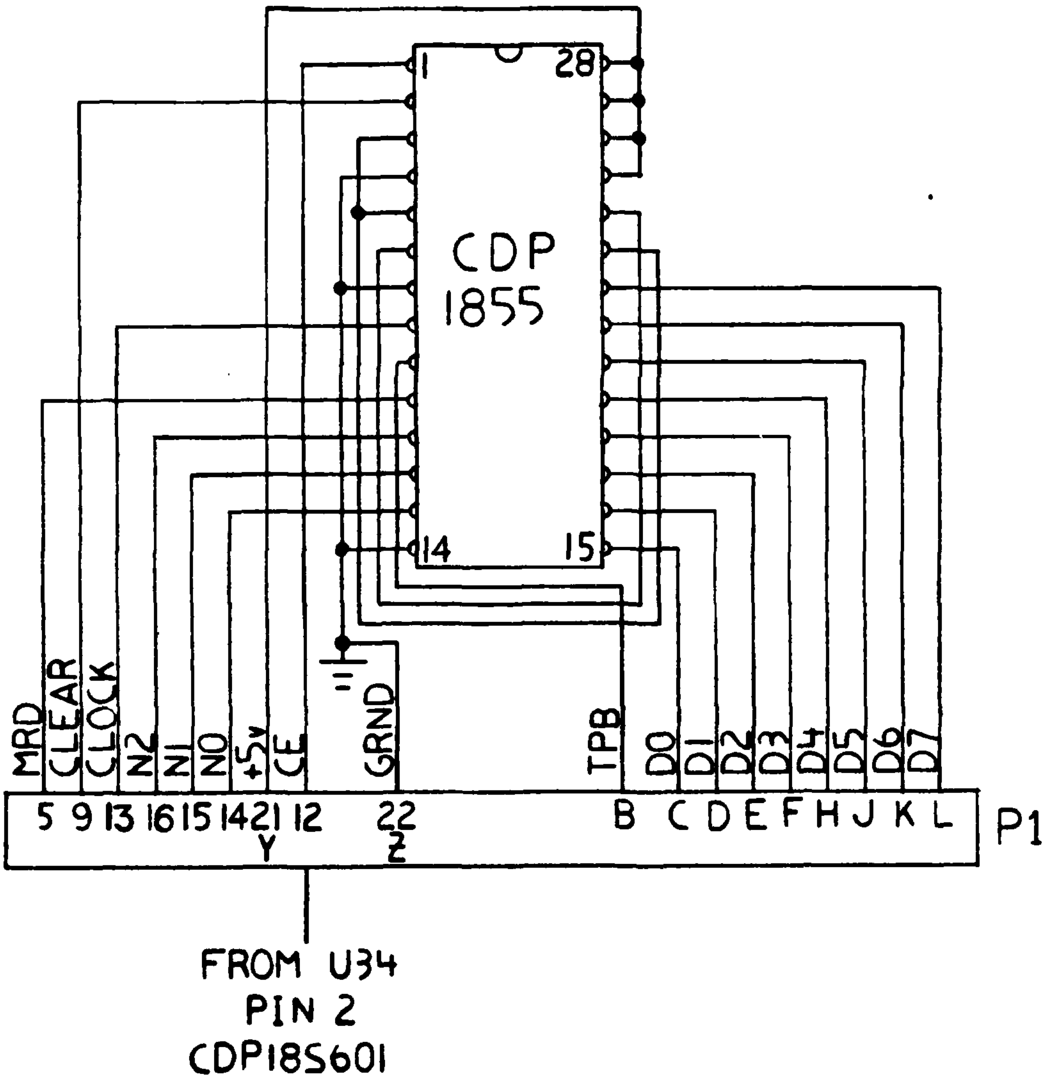
gate voltage
(2v/div)

time scale=2msec/div

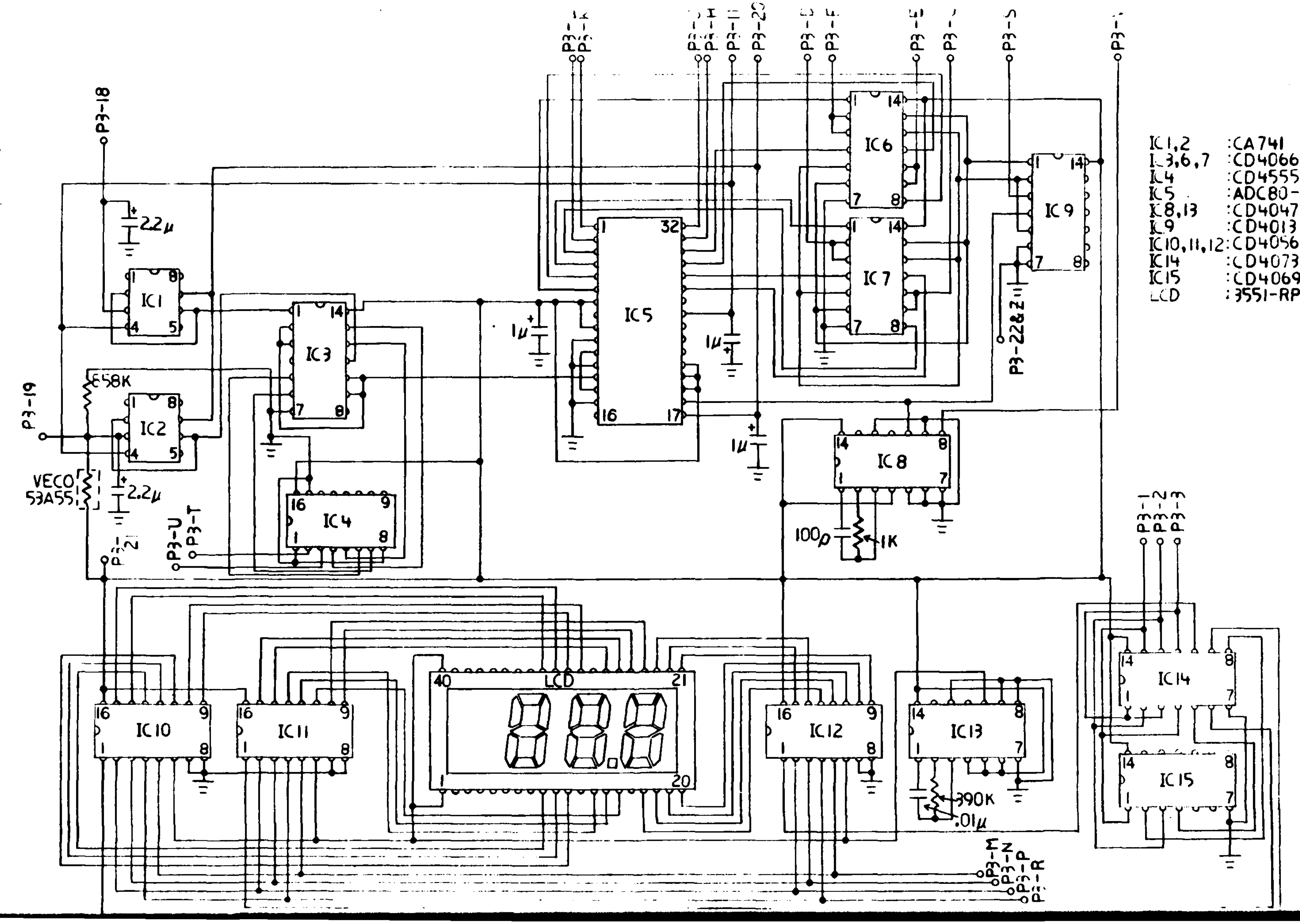


P2
12 A-D CONVERTER
ADC80AG-12
43.2

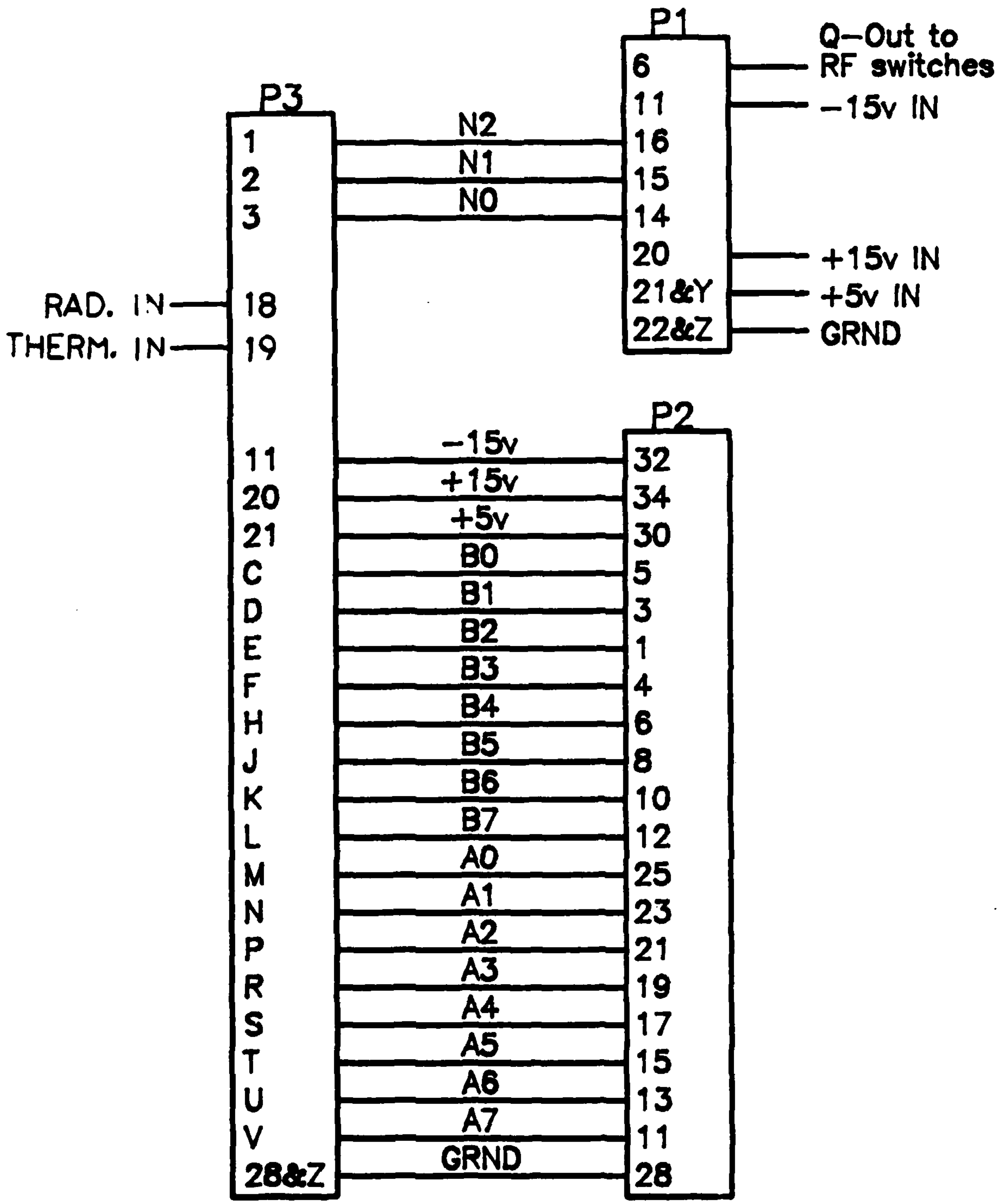

P2
34
2
I/O
CDP 1851
2
7
1
6
EPROM
U
34
CDP 1802
μP
1
22
P1

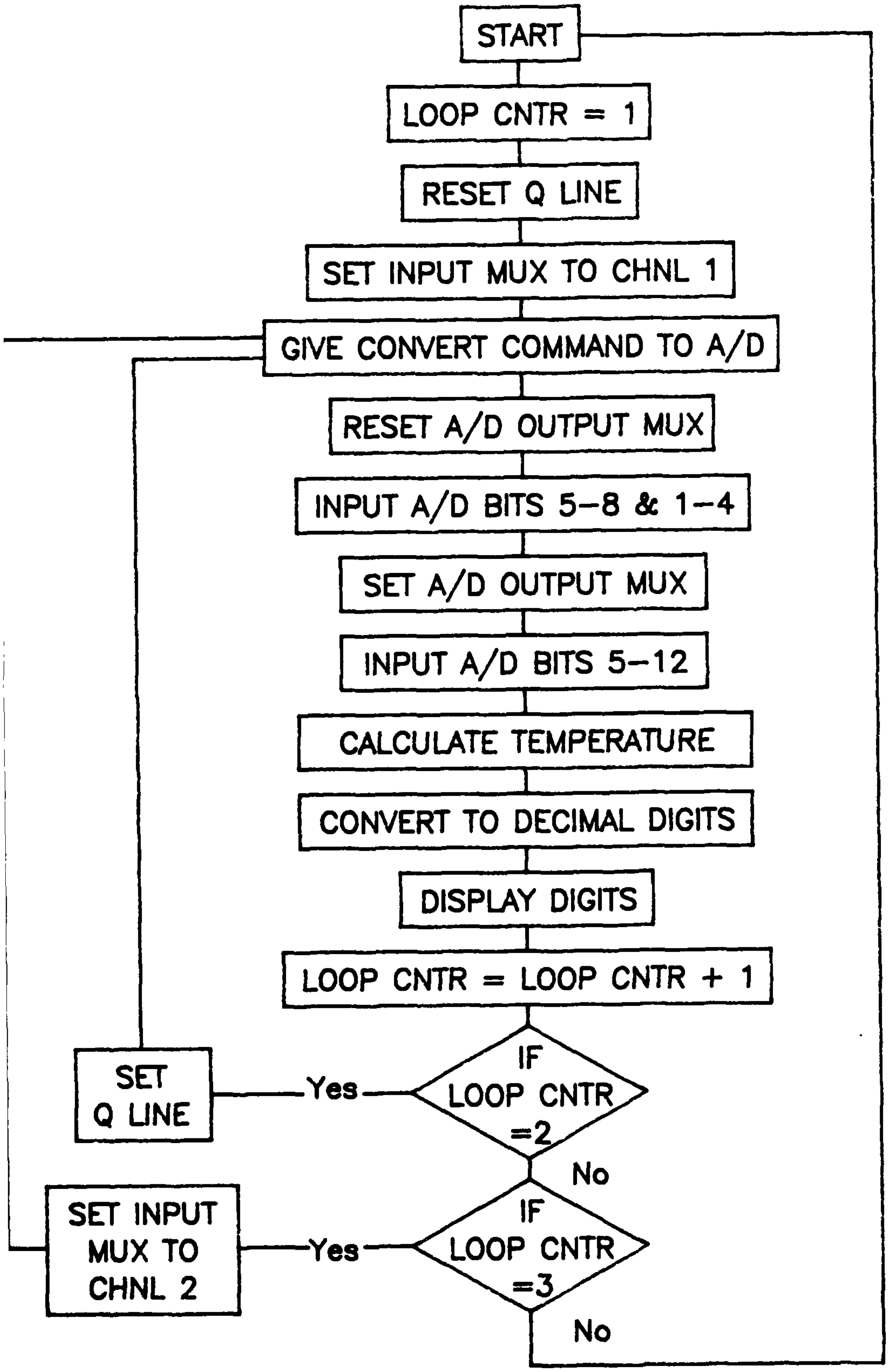


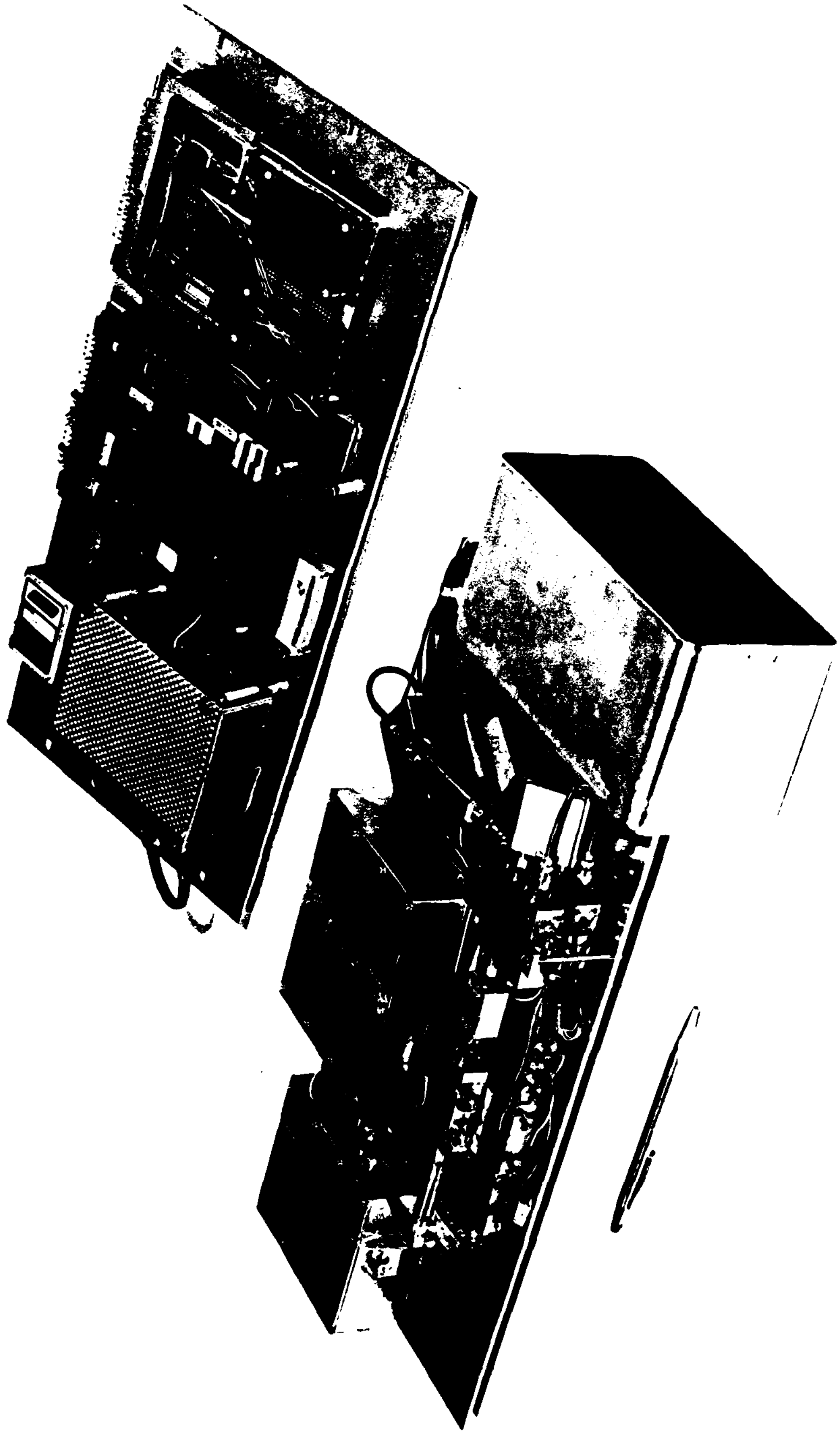
CDP 1855
1
28
14
15
MRD
CLEAR
CLOCK
N2
N1
N0
+5v
CE
GRND
TPB
D0
D1
D2
D3
D4
D5
D6
D7
5 9 13 16 15 14 21 12 22 B C D E F H J K L
Y
Z
P1
FROM U34
PIN 2
CDP18S601

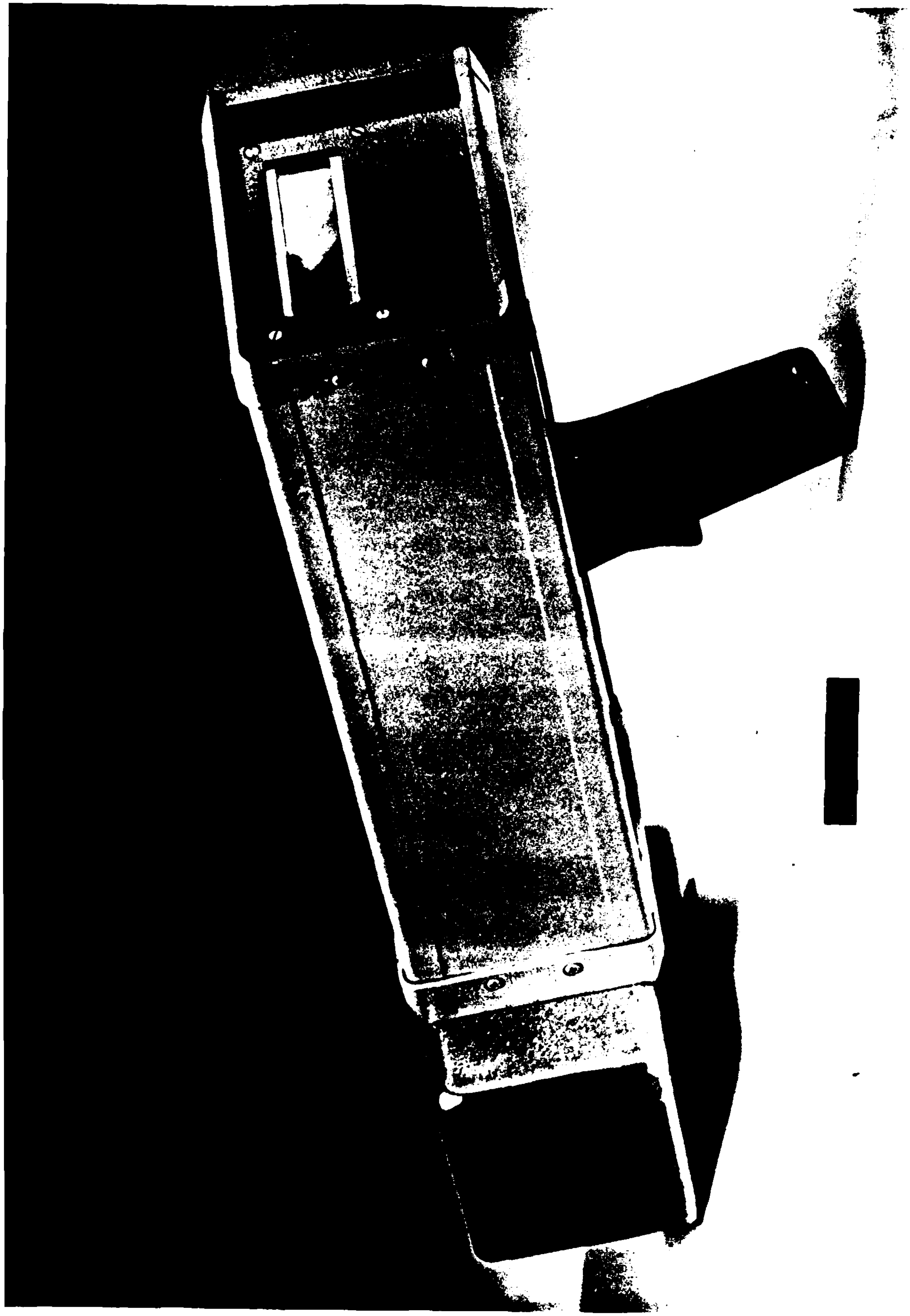


IC1,2	:CA741
IC3,6,7	:CD4066
IC4	:CD4555
IC5	:ADC80-12
IC8,13	:CD4047
IC9	:CD4013
IC10,11,12	:CD4056
IC14	:CD4073
IC15	:CD4069
LCD	:3551-RPH-0


P1
Q-Out to RF switches
-15v IN
+15v IN
+5v IN
GRND
6
11
16
15
14
20
21&Y
22&Z
P3
1
2
3
18
19
11
20
21
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
28&Z
RAD. IN
THERM. IN
N2
N1
N0
-15v
+15v
+5v
B0
B1
B2
B3
B4
B5
B6
B7
A0
A1
A2
A3
A4
A5
A6
A7
GRND
P2
32
34
30
5
3
1
4
6
8
10
12
25
23
21
19
17
15
13
11
28


START
LOOP CNTR = 1
RESET Q LINE
SET INPUT MUX TO CHNL 1
GIVE CONVERT COMMAND TO A/D
RESET A/D OUTPUT MUX
INPUT A/D BITS 5–8 & 1–4
SET A/D OUTPUT MUX
INPUT A/D BITS 5–12
CALCULATE TEMPERATURE
CONVERT TO DECIMAL DIGITS
DISPLAY DIGITS
LOOP CNTR = LOOP CNTR + 1
IF LOOP CNTR =2
Yes
SET Q LINE
No
IF LOOP CNTR =3
Yes
SET INPUT MUX TO CHNL 2
No





END

FILMED

9-85

DTIC