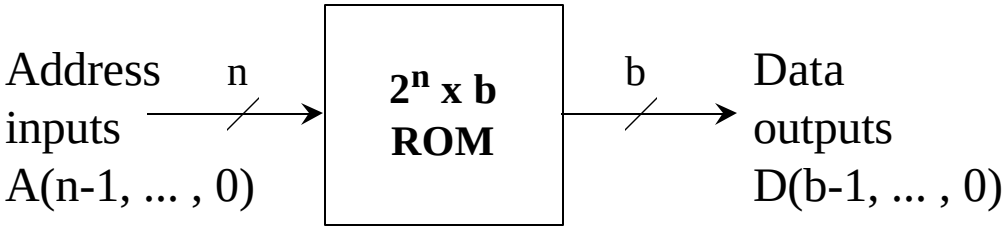
Memory Devices

- **Read Only Memory (ROM)**
  - **Structure of diode ROM**
  - **Types of ROMs.**
  - **ROM with 2-Dimensional Decoding.**
  - **Using ROMs for Combinational Logic**
- **Read/Write Memory**

  (Random Access Memory, RAM):
  - **Types of RAM:**
    - **Static RAM (SRAM)**
    - **Dynamic RAM (DRAM)**
  - **SRAM Timing**
  - **DRAM Timing**

Read-Only Memory (ROM)

- **A combinational circuit with n inputs and b outputs:**



- **Programmable ¾ values determined by user**
- **Nonvolatile ¾ contents retained without power**
- **Uniform (Random) Access ¾ delay is uniform for all addresses**

Read-Only Memory (ROM)

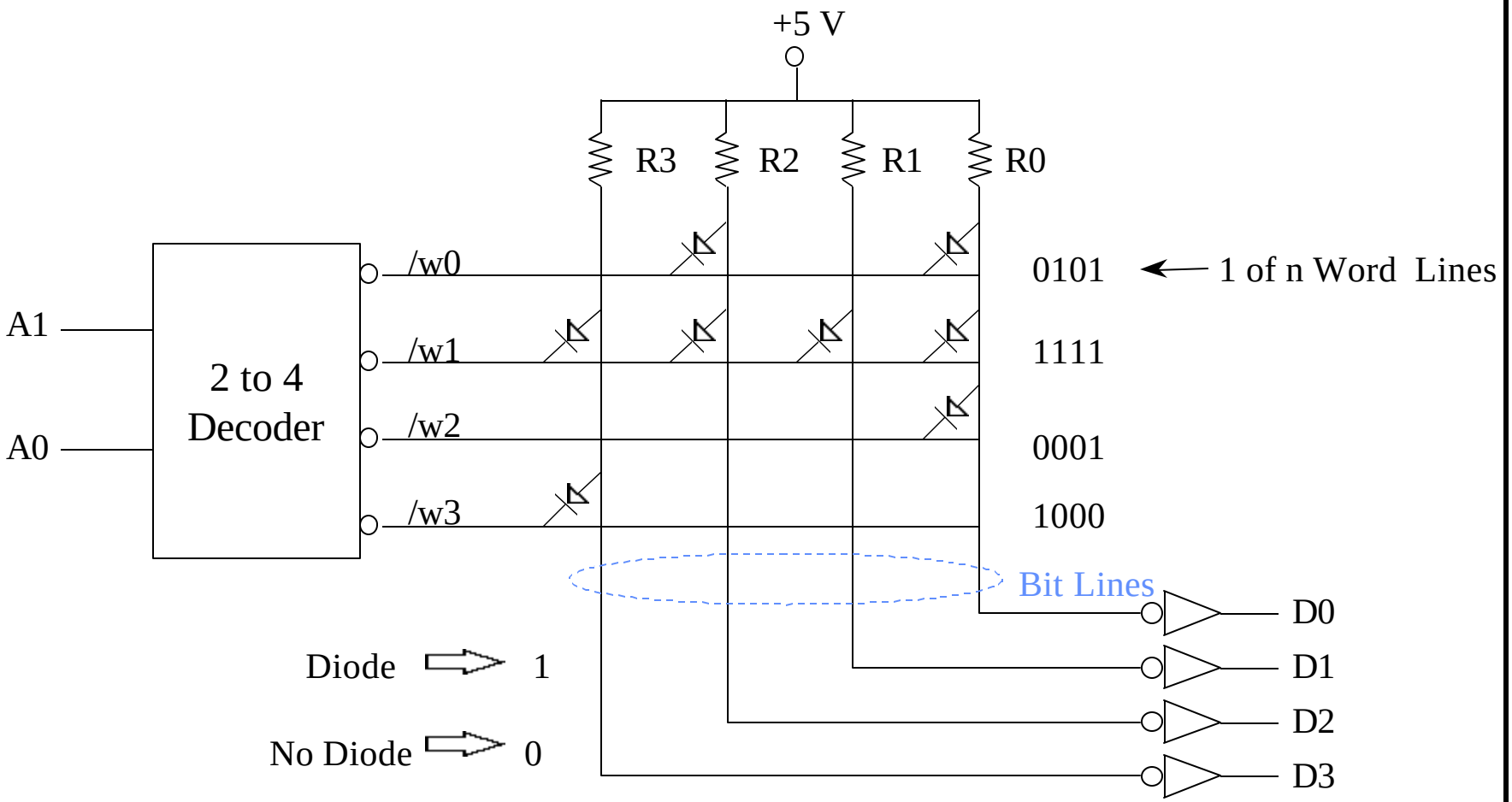
- **Two views of ROM:**
  - ROM stores 2^n words of b bits each, or
  - ROM stores an n-input, b-output truth table

Example:

n = 2		b = 4			
A1	A0	D3	D2	D1	D0
0	0	0	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	1	1	0	0	0

⇦ Stores 4 4-bit words, or stores 4 functions of 2 input variables

Internal Structure of 4´4 Diode ROM



Types Of ROMs

- **Mask ROM**
  - **Connections made by the semiconductor vendor**
  - **Expensive setup cost, Several weeks for delivery. High volume only**
  - **Bipolar or MOS technology**
- **PROM**
  - **Programmable ROM**
  - **Vaporize (blow) fusible links with PROM programmer using high voltage/current pulses**
  - **Bipolar technology**
  - **One-time programmable**
- **EPROM**
  - **Erasable Programmable ROM**
  - **Charge trapped on extra "floating gate" of MOS transistors**
  - **Exposure to UV light removes charge. Limited number of erasures (10-100)**
- **EEPROM (E^2ROM)**
  - **Electrically Erasable ROM**
  - **Not RAM (relatively slow charge/discharge)**
  - **limited number of charge/discharge cycles (10,000)**
- **Flash Memory**
  - **Electronically erasable in blocks**
  - **100,000 erase cycles**
  - **Simpler and denser than EEPROM**

ROM Type Summary

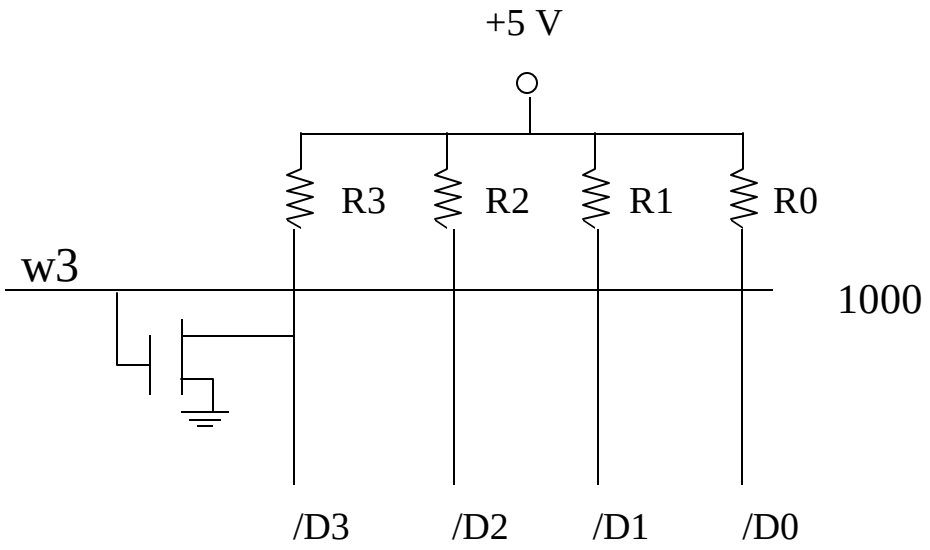
Type	Technology	Read Cycle	Write Cycle	Comments
Mask ROM	**NMOS,CMOS**	**20-200 ns**	**4 weeks**	**Write once; low power**
Mask ROM	**Bipolar**	**<100 ns**	**4 weeks**	**Write once; high power; low density**
PROM	**Bipolar**	**<100 ns**	**5 minutes**	**Write once; high power; no mask charge**
EPROM	**NMOS, CMOS**	**25-200 ns**	**5 minutes**	**Reusable; low power; no mask charge**
EEPROM	**NMOS**	**50-200 ns**	**10 ms/byte**	**10,000 writes/location limit**
FLASH	**CMOS**	**25-200 ns**	**10 ms/block**	**100,000 erase cycles**

Internal Structure of Transistor ROM

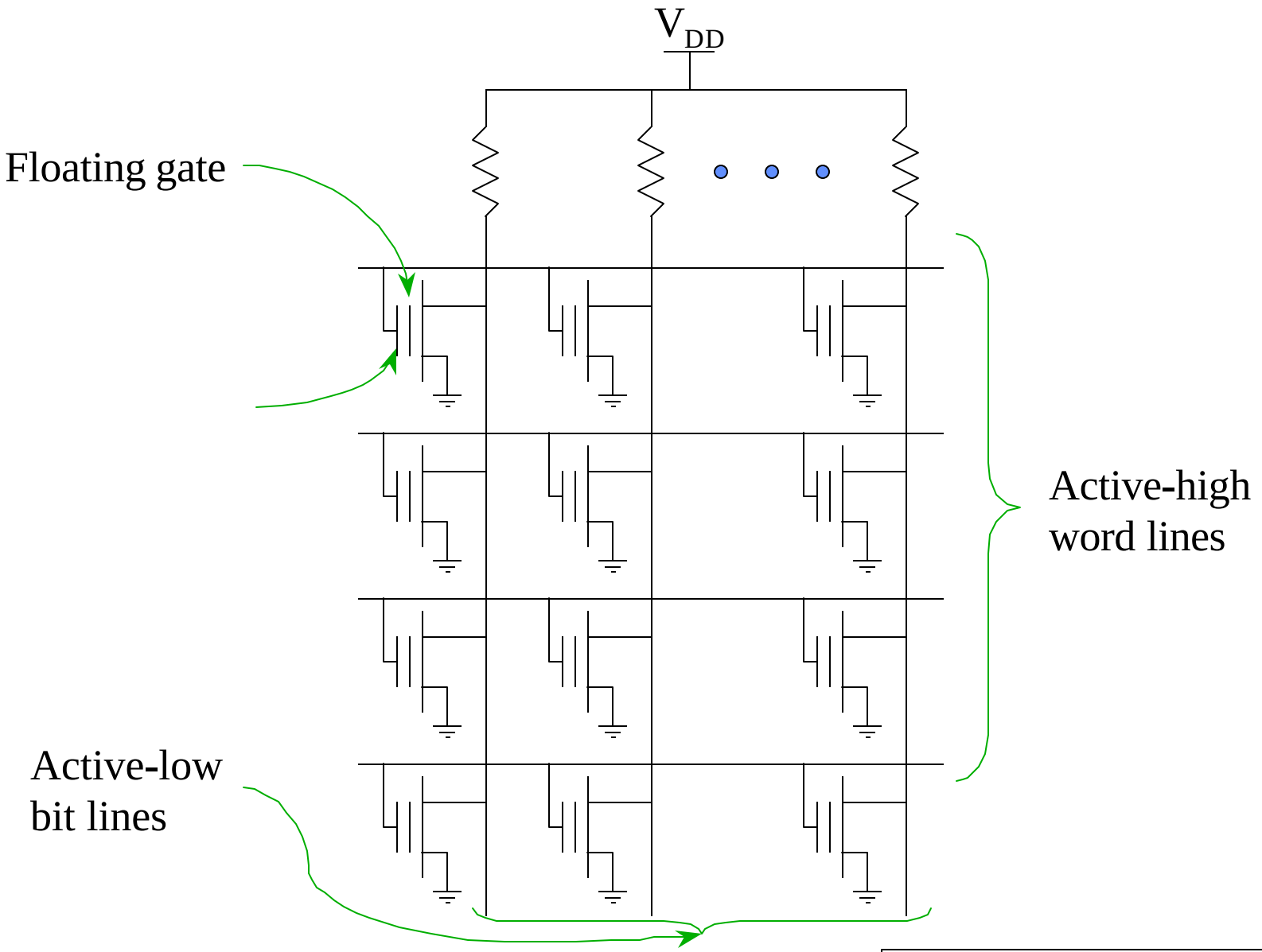
- **Replace diodes with MOS transistors**
- **Change decoder to active-high outputs**

Transistor ⇨ 1

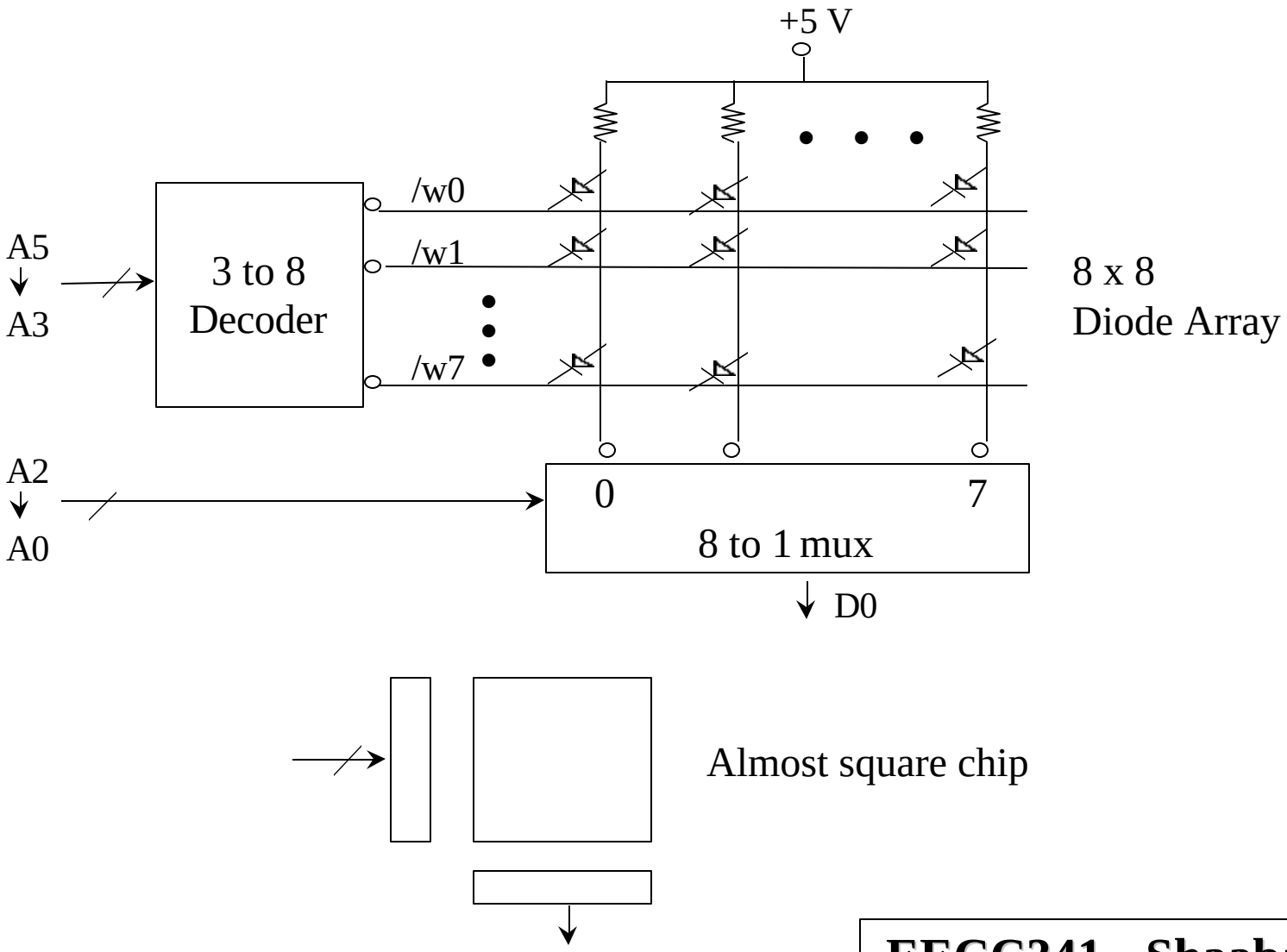
No transistor ⇨ 0

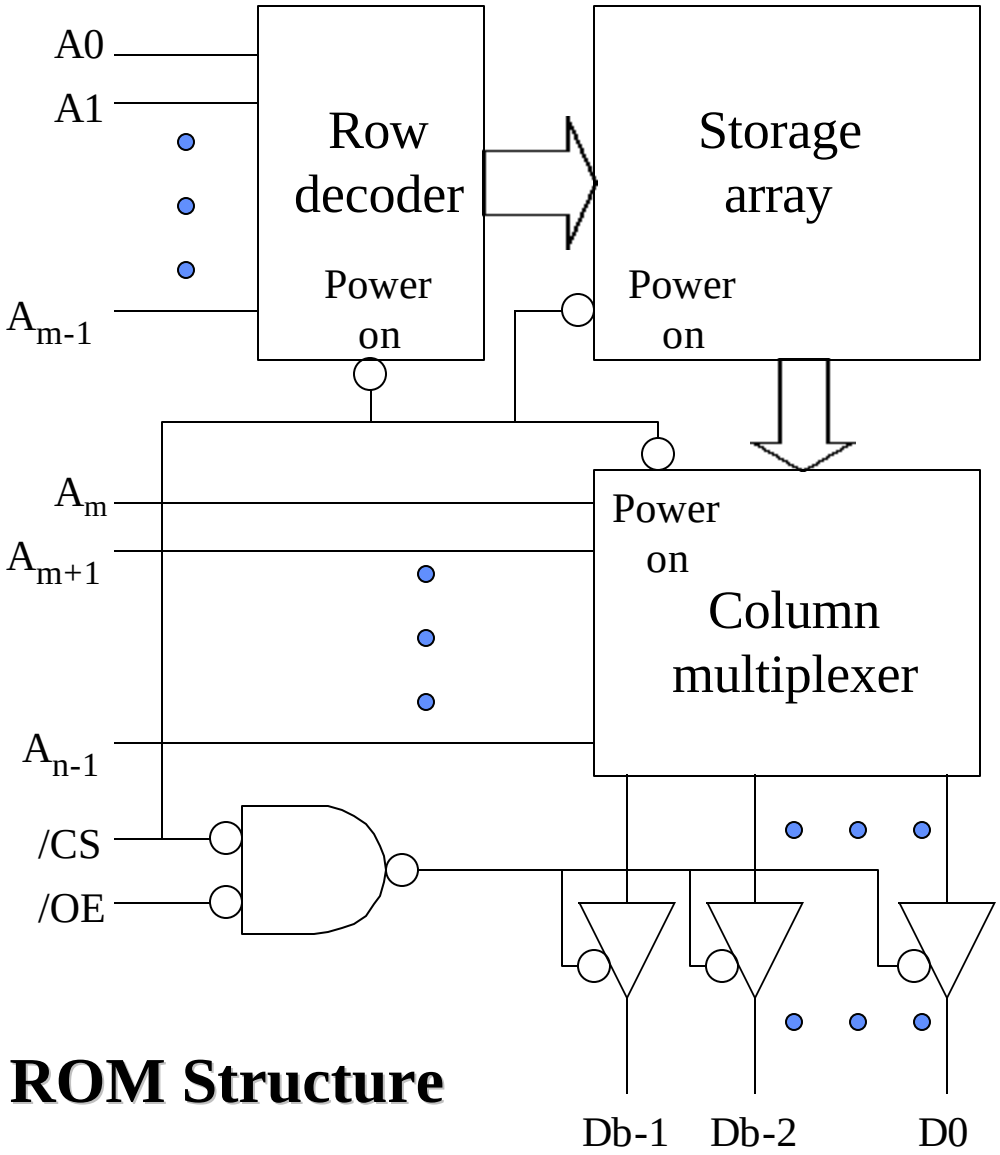


EPROM and EEPROM Structure



64 x 1 ROM with 2-Dimensional Decoding



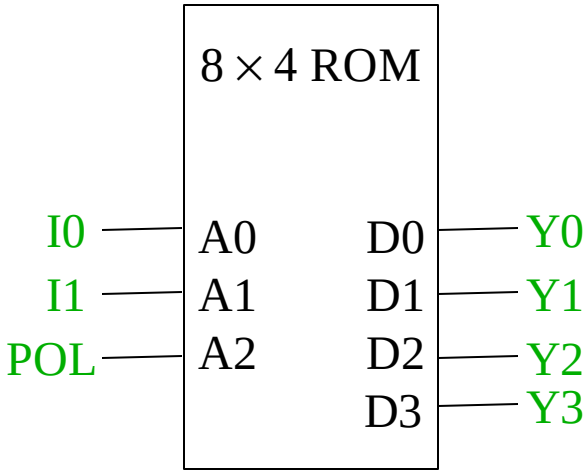


Internal 2^n x b ROM Structure

Using ROMs for Combinational Logic

Example A 3-input, 4-output combinational logic function:

Inputs			Outputs			
A2	A1	A0	D3	D2	D1	D0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0



Function: 2-to-4 Decoder with Polarity Control

A2 = Polarity (0 = active Low, 1= active High)

A1, A0 = I1, I0 (2-bit input)

D3...D0 = Y3...Y0 (4-bit decoded output)

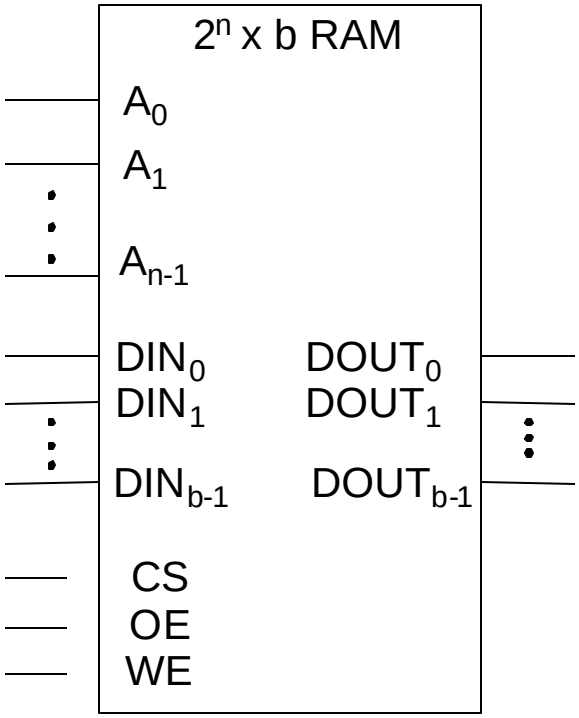
Read/Write Memory (RWM / RAM)

- **RWM = RAM (Random Access Memory)**
- **Highly structured like ROMs**
- **Can store and retrieve data at (relatively) the same speed**

- **Static RAM (SRAM) retains data in latches (while powered)**
- **Dynamic RAM (DRAM) stores data as capacitor charge; all capacitors must be recharged periodically (refresh).**

- **Volatile Memory: Both Static and Dynamic RAM**
- **Nonvolatile Memory: Data retained when power lost**
  = ROMs, NVRAM (w/battery), Flash Memory

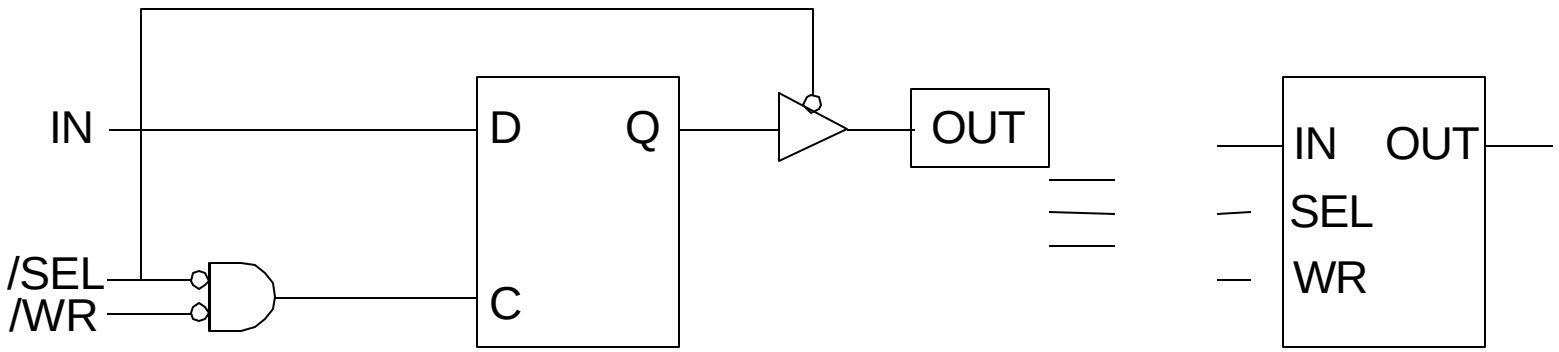
Basic Structure of SRAM



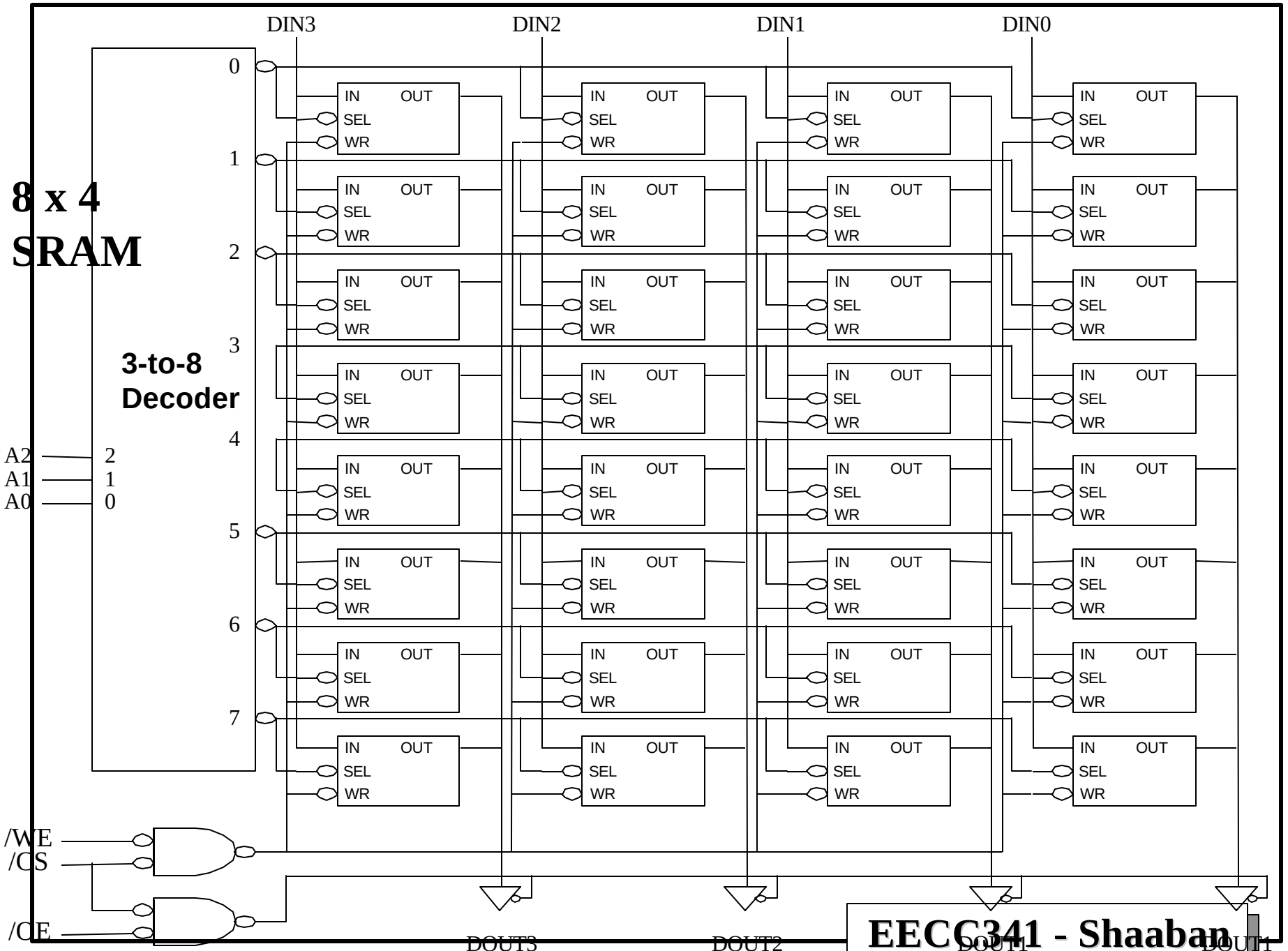
- **Address/Control/Data Out lines like a ROM (Reading)**

  + Write Enable (WE) and Data In (DIN) (Writing)

One Bit of SRAM



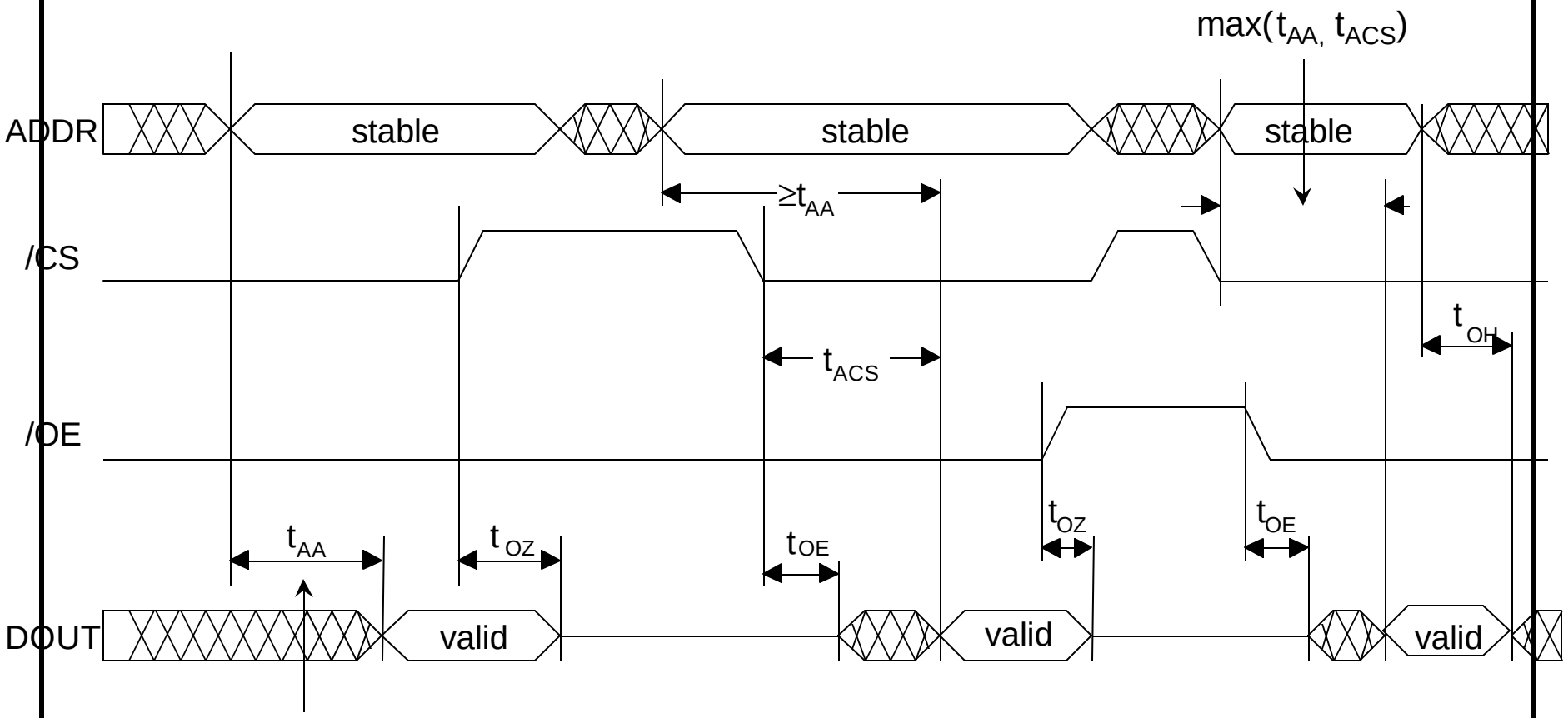
- **SEL and WR asserted ® IN data stored in D-latch (Write)**
- **SEL only asserted ® D-latch output enabled (Read)**
- **SEL not asserted ® No operation**


8 x 4
SRAM
3-to-8
Decoder
DIN3
DIN2
DIN1
DIN0
0
1
2
3
4
5
6
7
IN
OUT
SEL
WR
A2
A1
A0
2
1
0
/WE
/CS
/CE
DOUT3
DOUT2
DOUT1
DOUT1

SRAM Timing

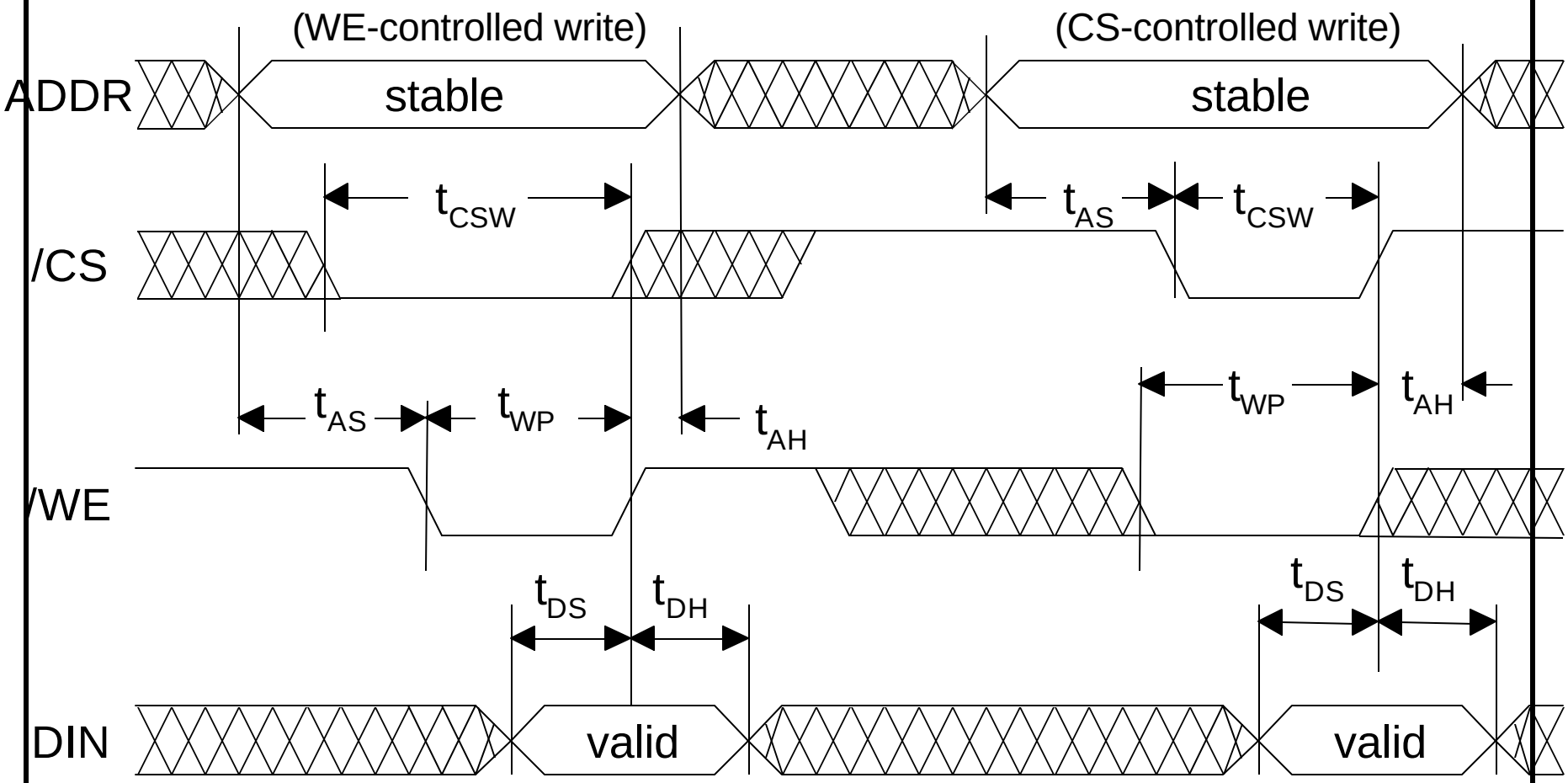
- **During READ, outputs are combinational functions of ADDR, CS, OE (like ROM)**
  - Inputs can freely change without problems (except for propagation delay from last input change to output)
- **During WRITE, data stored in latches, NOT FF's.**
  - Thus, Setup & Hold on Data IN relative to trailing edge of /WR
- **Address must be stable**
  - for setup time before /WR asserted, and
  - for hold time after /WR deasserted
    - **to prevent "spraying" data to multiple rows**
- **/WR asserted when BOTH /CS and /WE asserted**
- **/WR deasserted when EITHER /CS or /WE deasserted**

READ Timing (SRAM)

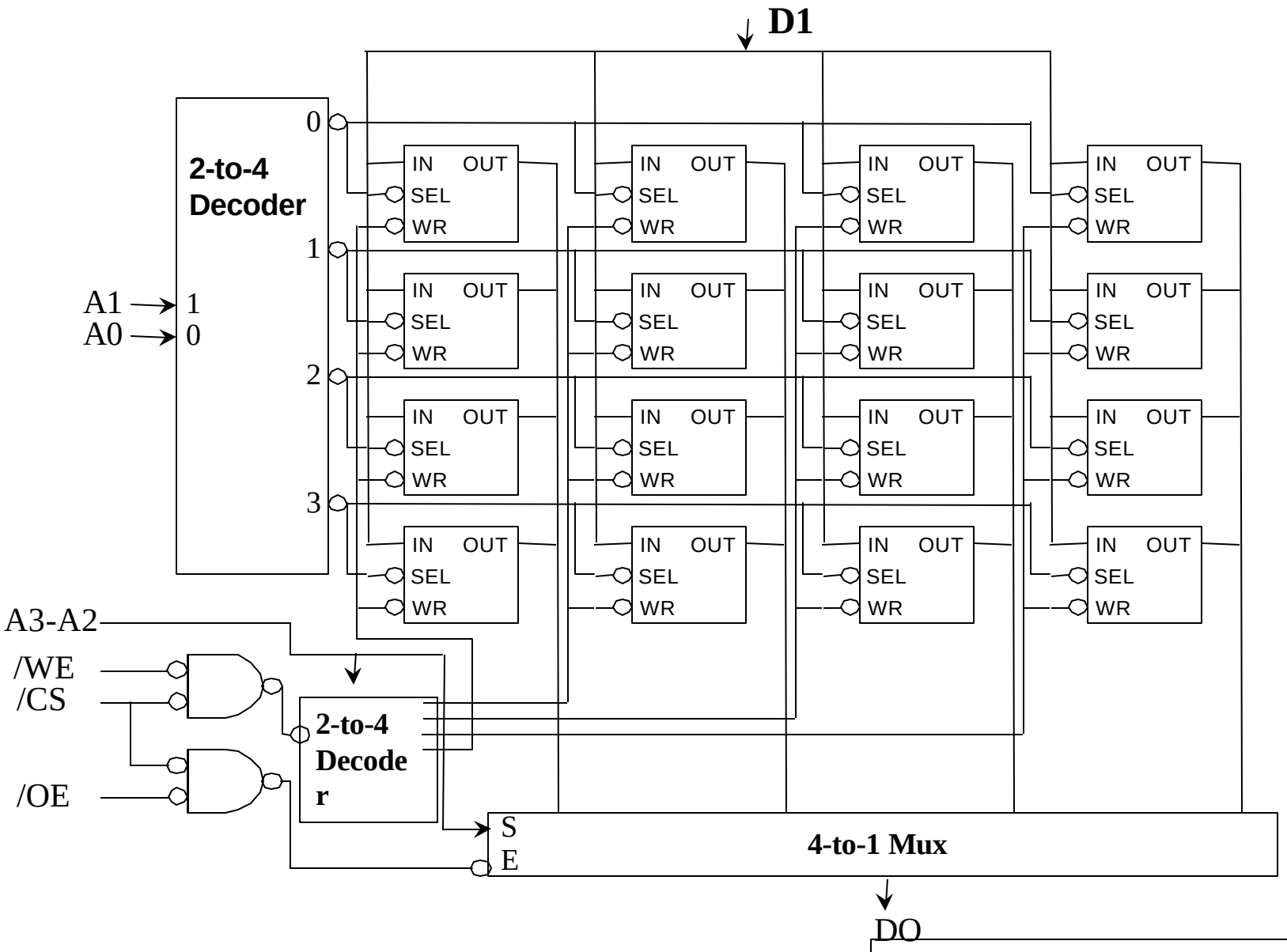


Primary Spec
for SRAMs

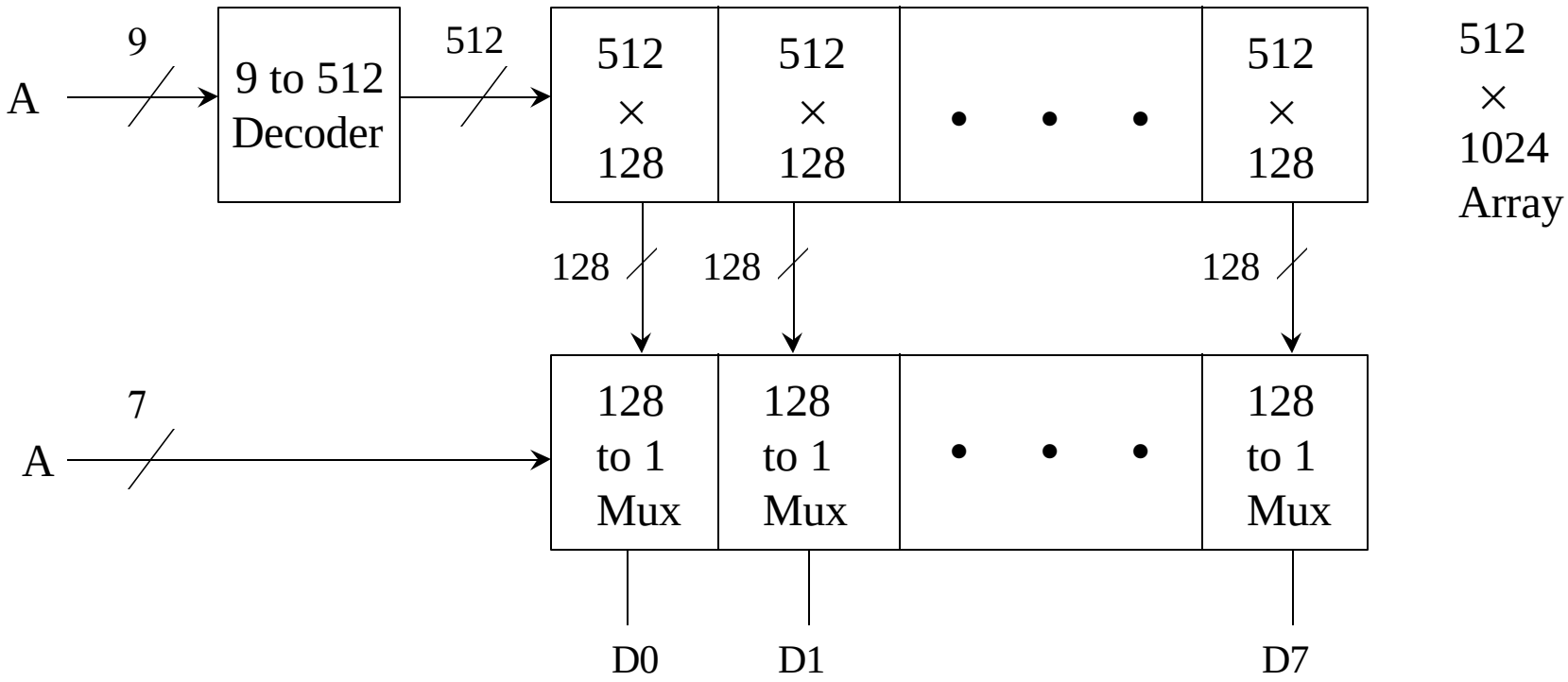
WRITE Timing (SRAM)



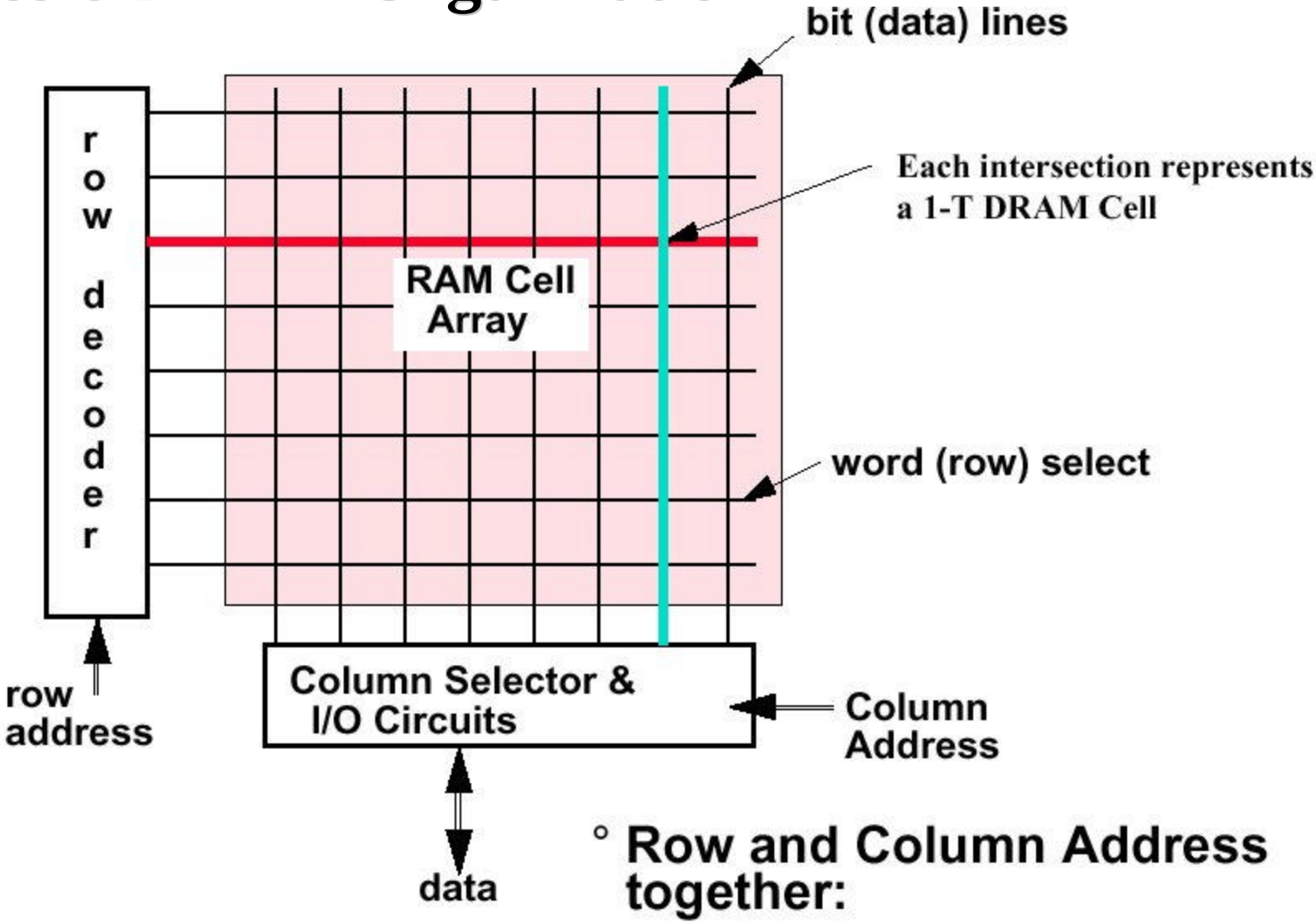
Example: 16 x 1 SRAM ® 4 x 4 Array



64K x 8 RAM with 2-D Decoding



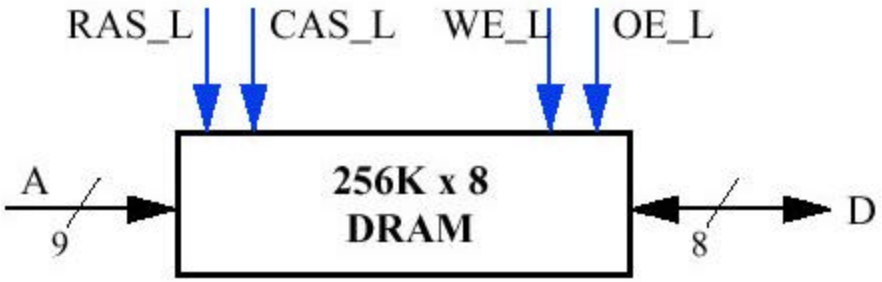
Classic DRAM Organization



° Row and Column Address together:

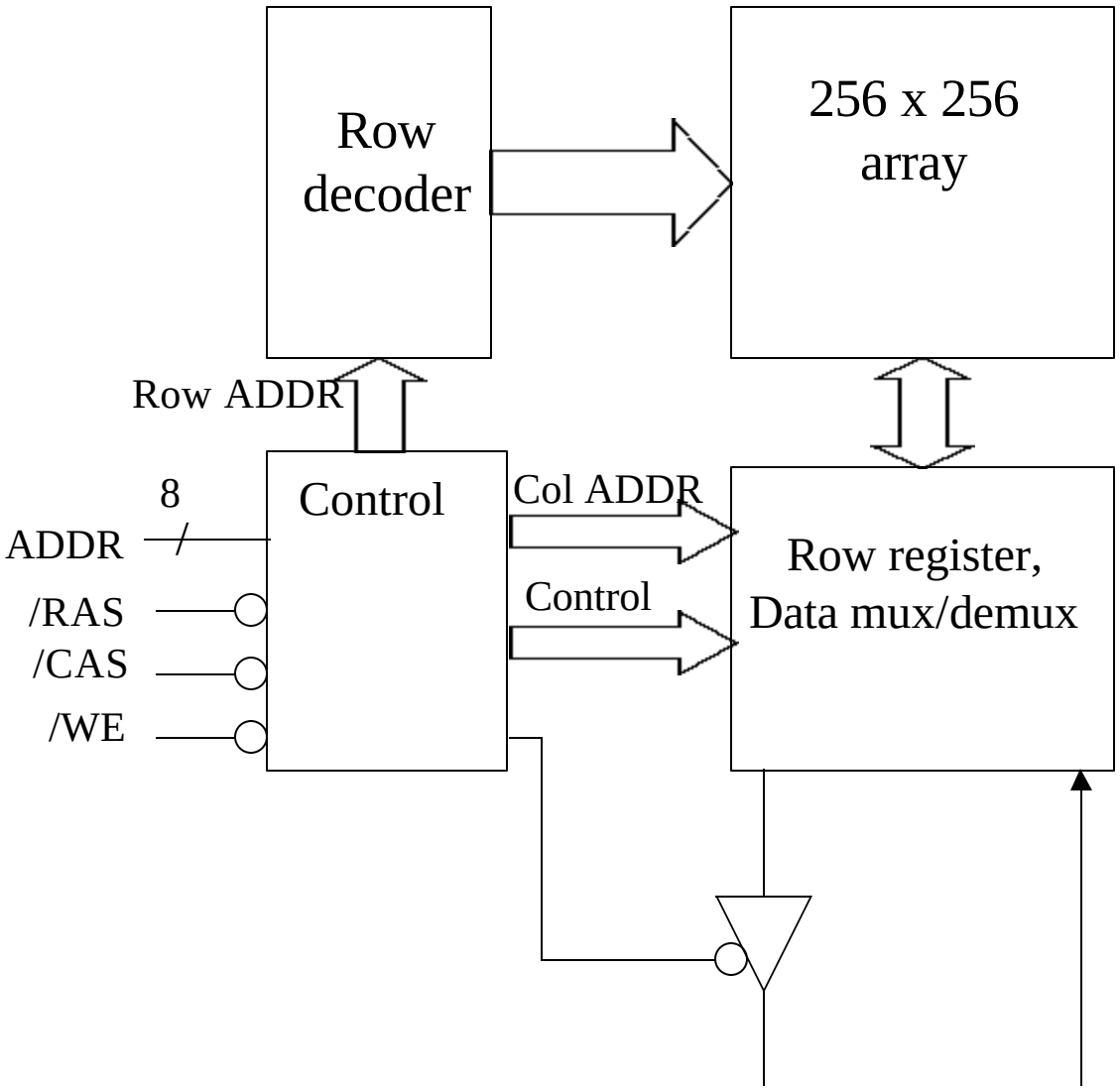
- Select 1 bit a time

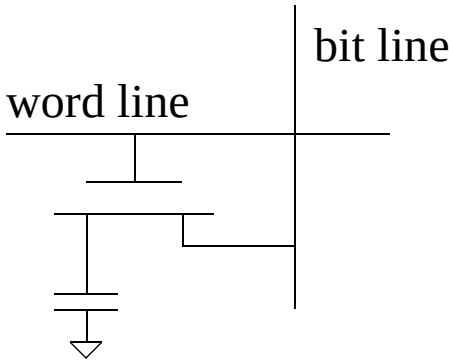
Logical Diagram of A Typical DRAM



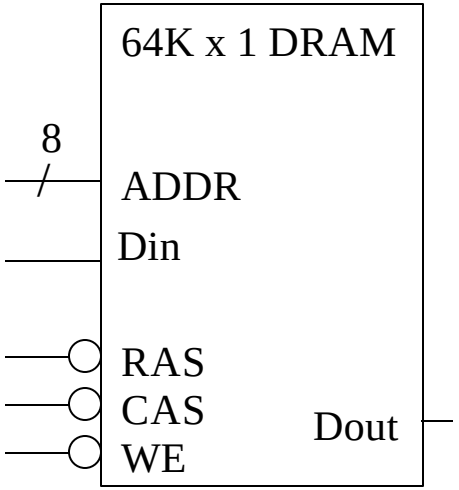
- Control Signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
- Din and Dout are combined (D):
  - WE_L is asserted (Low), OE_L is disasserted (High)
    - D serves as the data input pin
  - WE_L is disasserted (High), OE_L is asserted (Low)
    - D is the data output pin
- Row and column addresses share the same pins (A)
  - RAS_L goes low: Pins A are latched in as row address
  - CAS_L goes low: Pins A are latched in as column address

64K x 1 DRAM

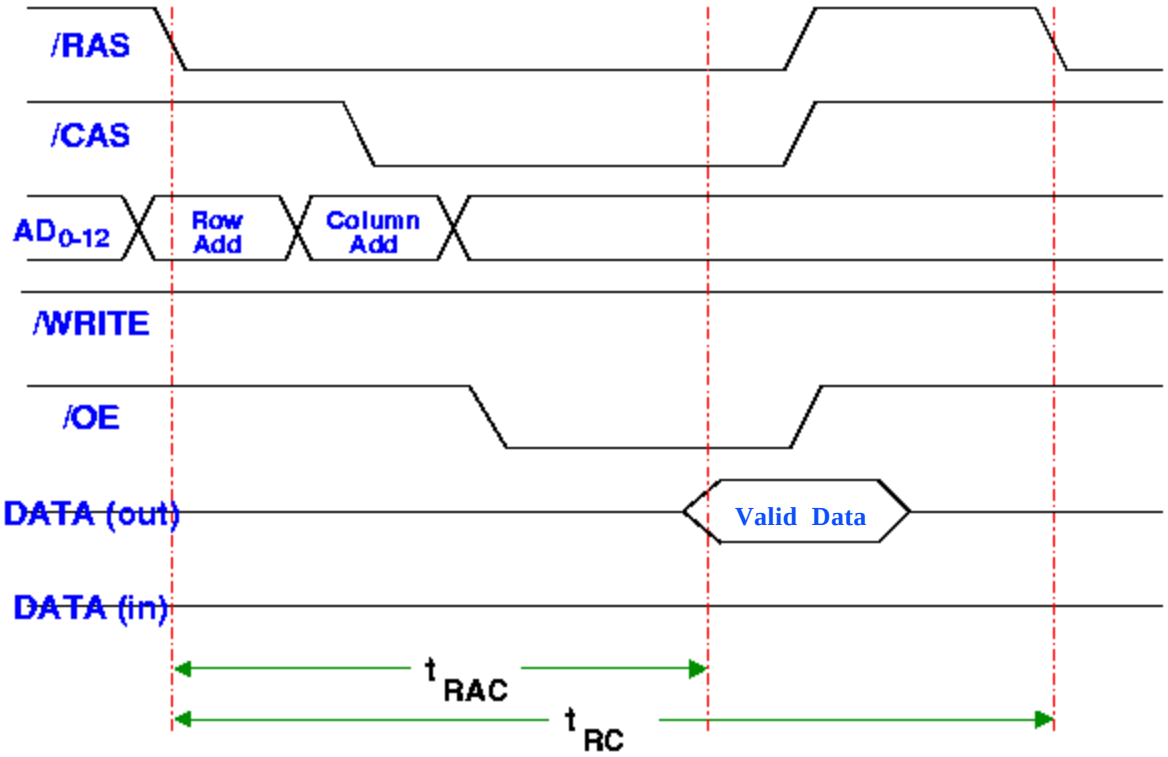




1-bit DRAM cell



Standard Asynchronous DRAM Read Timing



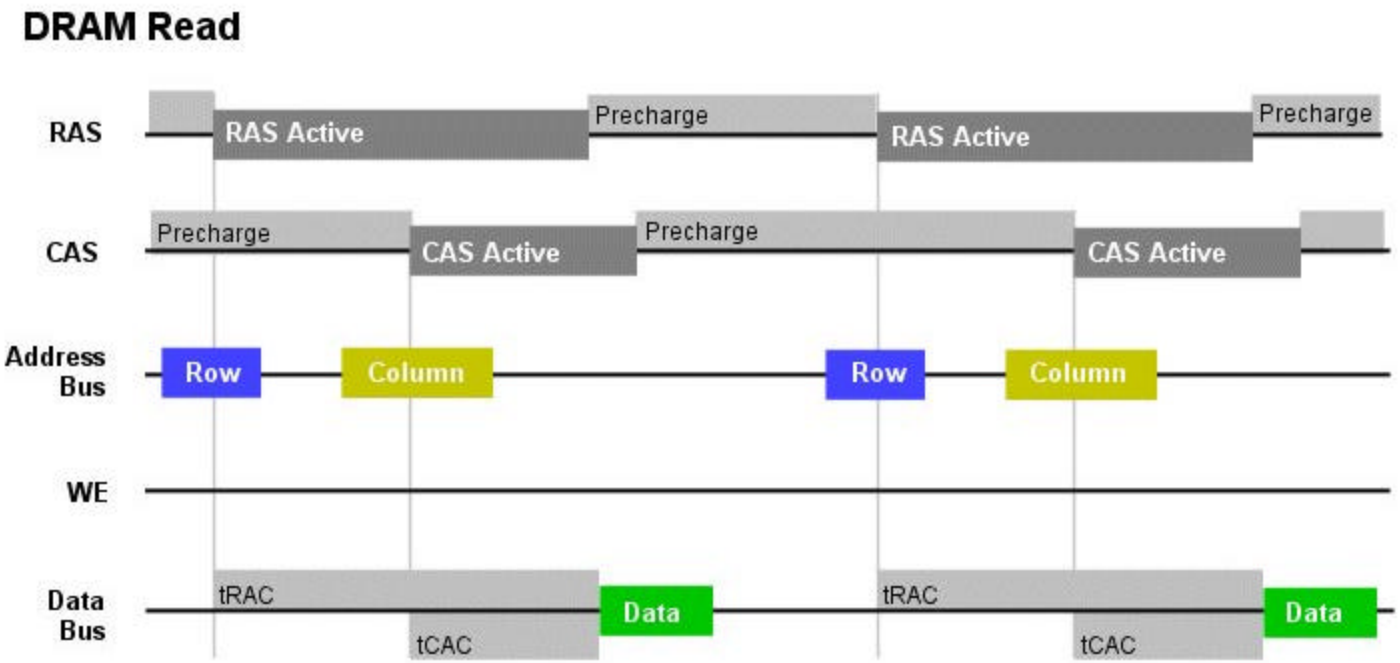
t_{RAC}: Minimum time from RAS (Row Access Strobe) line falling to the valid data output. Usually quoted as the nominal speed of a DRAM chip. For a typical 4Mb DRAM t_{RAC} = 60 ns

t_{RC}: Minimum time from the start of one row access to the start of the next.
t_{RC} = 110 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns

Four Key DRAM Timing Parameters

- t_{RAC}: Minimum time from RAS (Row Access Strobe) line falling to the valid data output.
  - Usually quoted as the nominal speed of a DRAM chip
  - For a typical 4Mb DRAM t_{RAC} = 60 ns
- t_{RC}: Minimum time from the start of one row access to the start of the next.
  - t_{RC} = 110 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns
- t_{CAC}: minimum time from CAS (Column Access Strobe) line falling to valid data output.
  - 15 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns
- t_{PC}: minimum time from the start of one column access to the start of the next.
  - About 35 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns

Simplified Asynchronous DRAM Read Timing



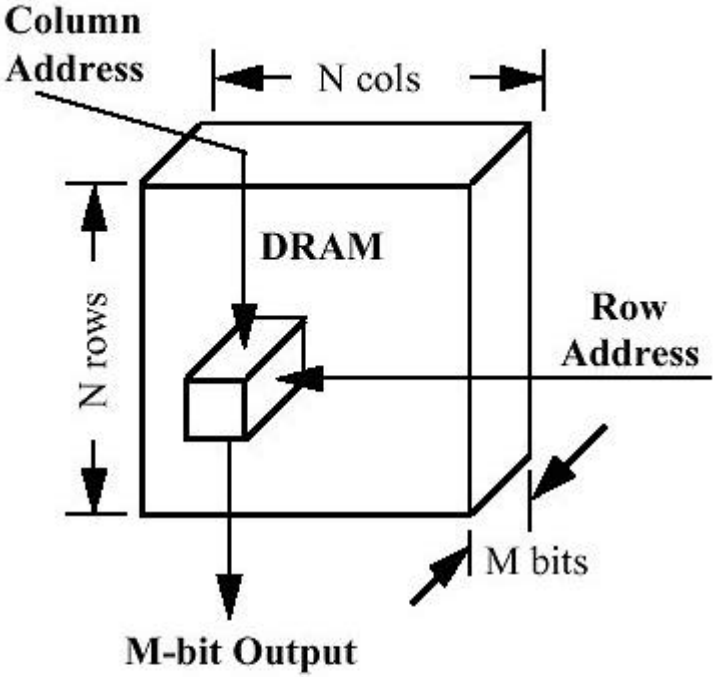
Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-1.html

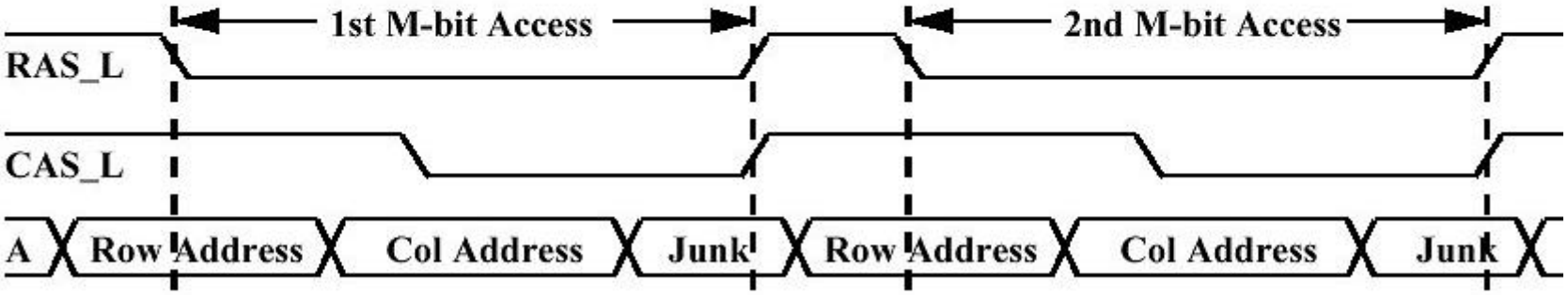
Modern DRAM Timing

- **Fast-Page Mode, FPM DRAM (One RAS, multiple CAS)**
  - Multiple bits of a row can be written before rewrite
  - Complex control, but much faster
- **Extended Data Out, EDO DRAM (One RAS, multiple CAS)**
  - Latches the column address so that the next address can be prepared *while* the output is read
  - Saves ~10ns/read, and increase of 10-15%
  - Even more complex control.
- **SDRAM - Synchronous DRAM**
  - **Unlike normal DRAM, SDRAM is clocked.**
  - **Multiple signals and banks (row-address registers) allow "pipelined" operation**

Page Mode DRAM: Motivation

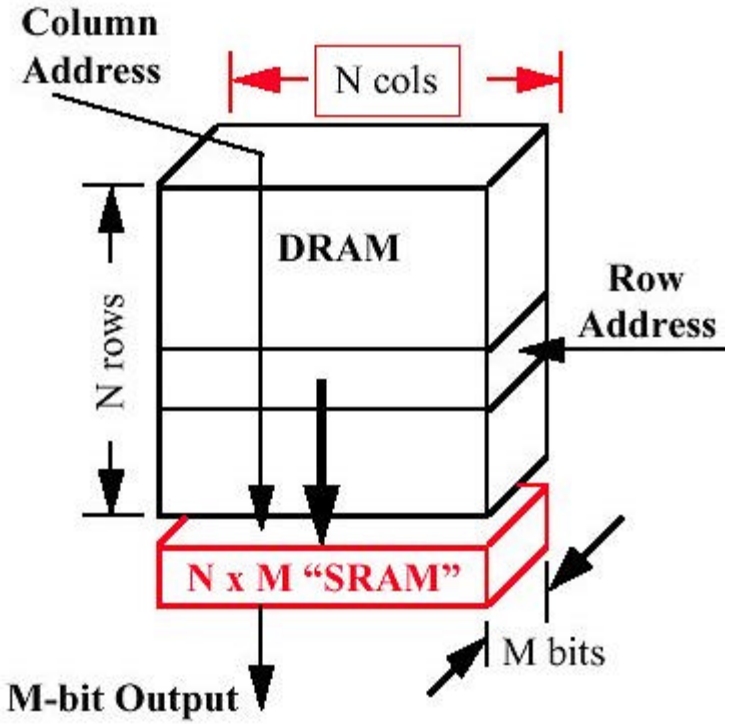
- Regular DRAM Organization:
  - N rows x N column x M-bit
  - Read & Write M-bit at a time
  - Each M-bit access requires a RAS / CAS cycle
- Fast Page Mode DRAM
  - N x M "register" to save a row

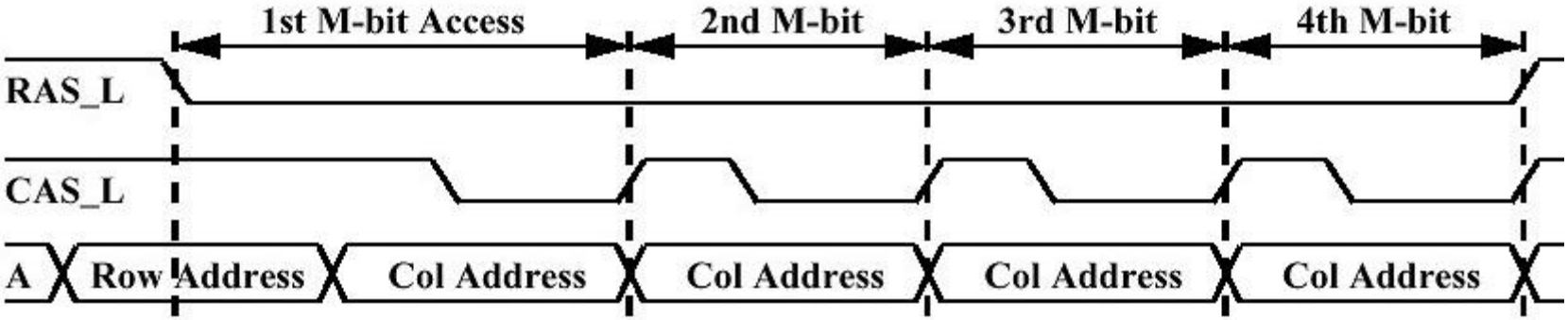




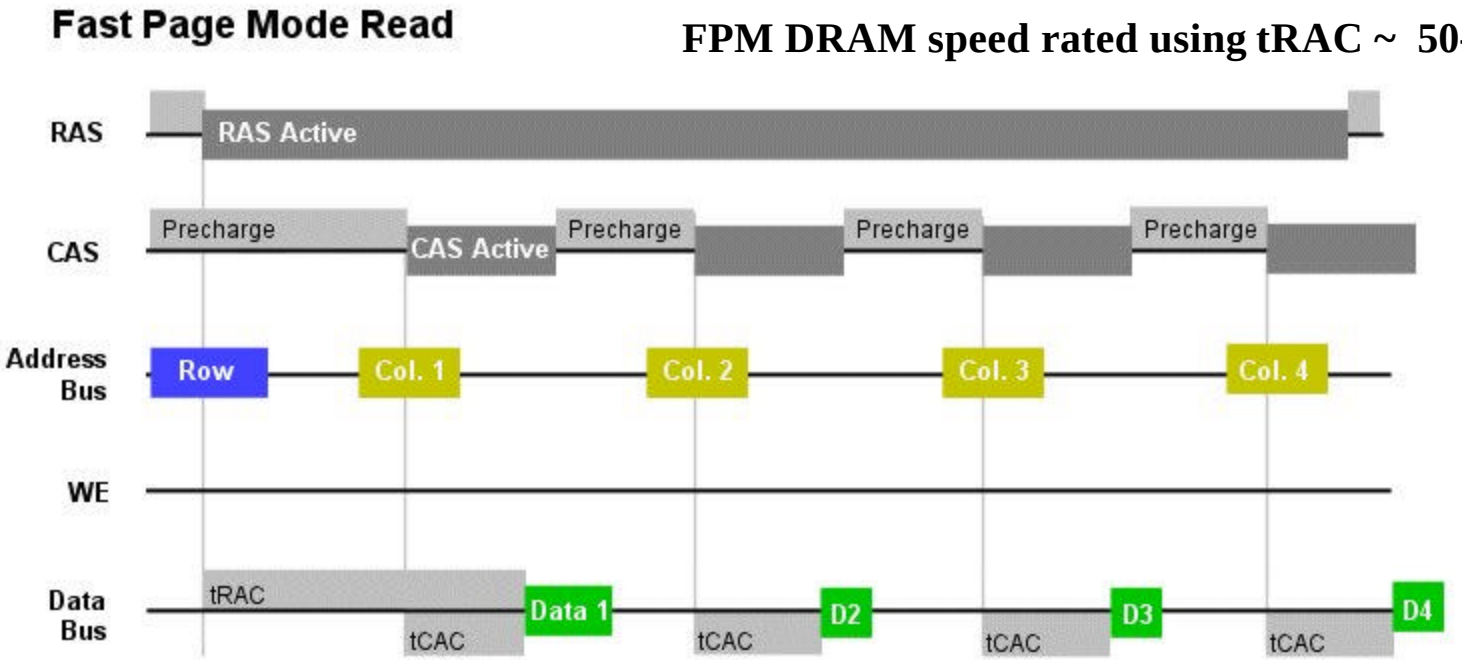
Fast Page Mode DRAM: Operation

- Fast Page Mode DRAM
  - N x M "SRAM" to save a row
- After a row is read into the register
  - Only CAS is needed to access other M-bit blocks on that row
  - RAS_L remains asserted while CAS_L is toggled





Simplified Asynchronous Fast Page Mode (FPM) DRAM Read Timing



FPM DRAM speed rated using tRAC ~ 50-70ns

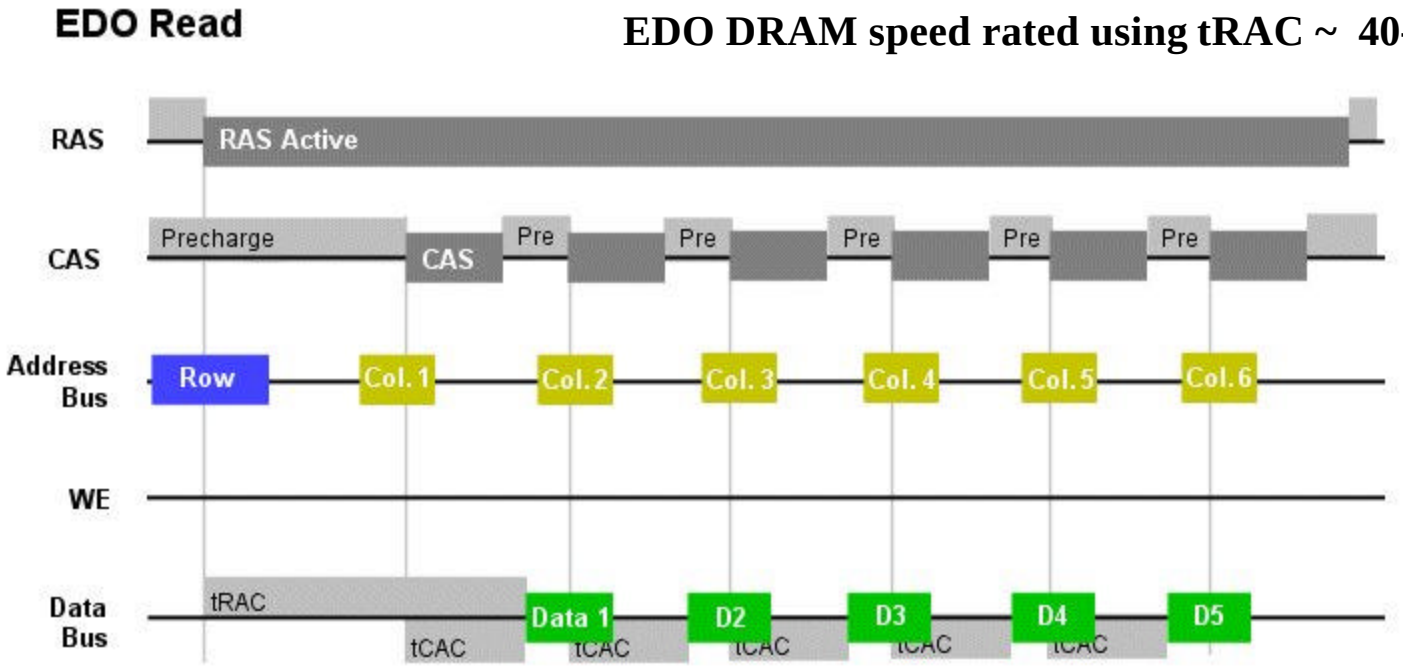
Typical timing at 66 MHZ : 5-3-3-3

For bus width = 64 bits = 8 bytes **Max. Bandwidth = 8 x 66 / 3 = 176 Mbytes/sec**

Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-1.html

Simplified Asynchronous Extended Data Out (EDO) DRAM Read Timing

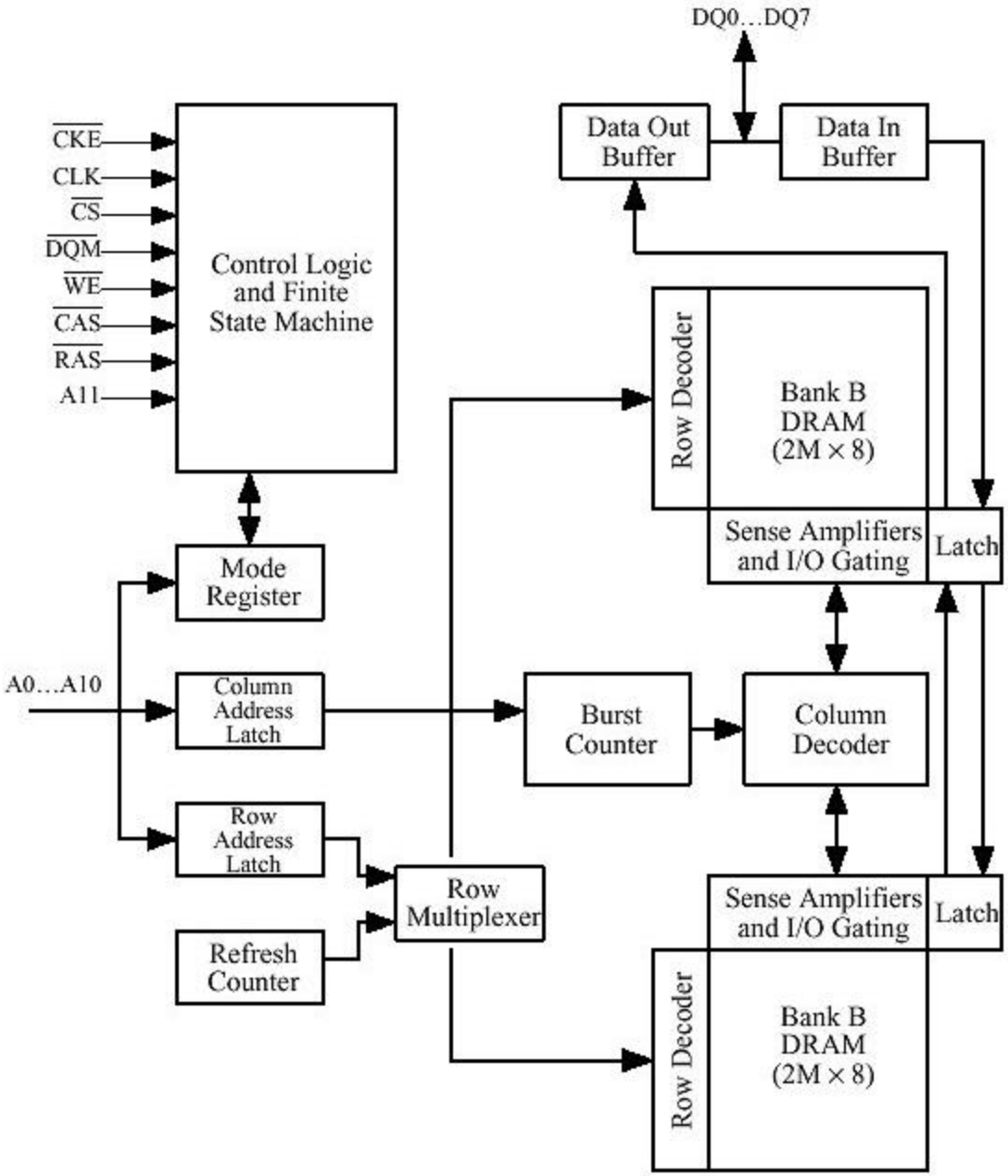
- **Extended Data Out DRAM operates in a similar fashion to Fast Page Mode DRAM except the data from one read is on the output pins at the same time the column address for the next read is being latched in.**



Typical timing at 66 MHZ : 5-2-2-2
For bus width = 64 bits = 8 bytes Max. Bandwidth = 8 x 66 / 2 = 264 Mbytes/sec

Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-1.html

Synchronous Dynamic RAM (SDRAM) Organization



SDRAM speed is rated at max. clock speed supported:

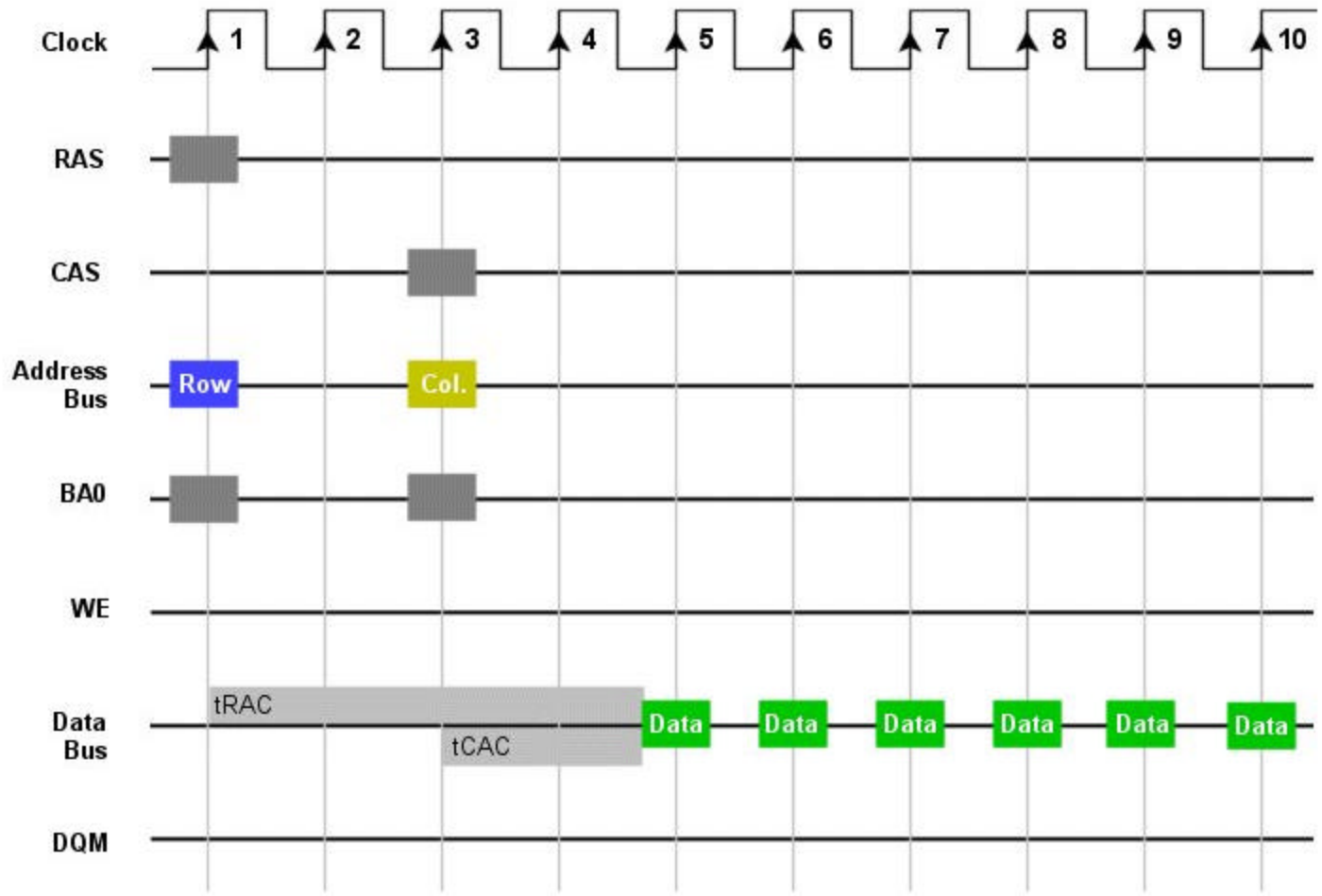
66MHZ = PC66

100MHZ = PC100

133MHZ = PC133

150MHZ = PC150

Simplified SDRAM Read Timing



Typical timing at 133 MHZ (PC133 SDRAM) : 4-1-1-1
For bus width = 64 bits = 8 bytes Max. Bandwidth = 133 x 8 = 1064 Mbytes/sec

Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-6.html

RAM Summary

SRAM:

- **Fast**
- **Simple Interface**
- **Moderate bit density (4 gates ® 4 to 6 transistors)**
- **Moderate cost/bit**

Small systems or very fast applications (cache memory)

DRAM (Dynamic RAM):

- **moderate speed**
- **complex interface**
- **High bit density (1 transistor cell)**
- **Low cost/bit**

Large Memories: PC's Mainframes