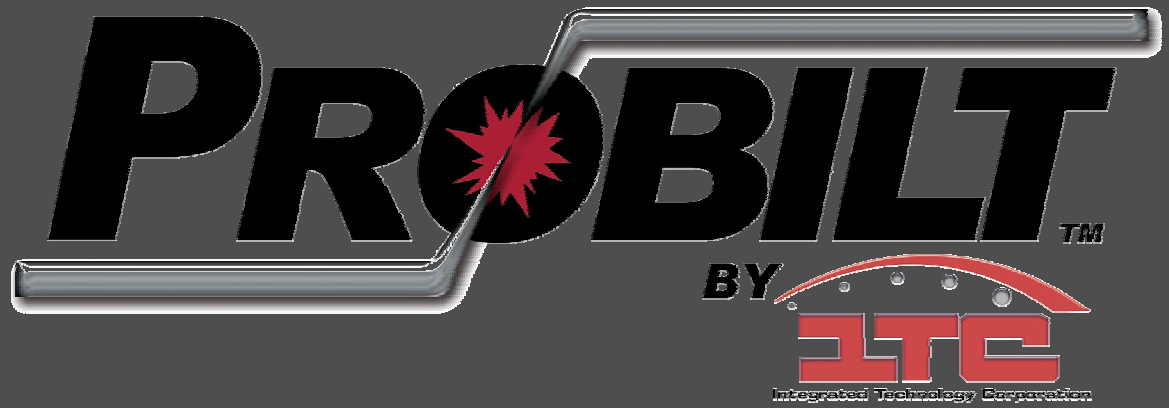


Real-World Avalanche Testing Of Single-Die, Wafers, Hybrid Modules, and Packaged Devices

Steven T. Clauter, Test Equipment Design Engineer
Integrated Technology Corporation
stevec@inttechcorp.com
www.inttechcorp.com

Taichi Ukai, President and CEO
Tiatech, Incorporated
ukai@tiatech.com
www.tiatech.com

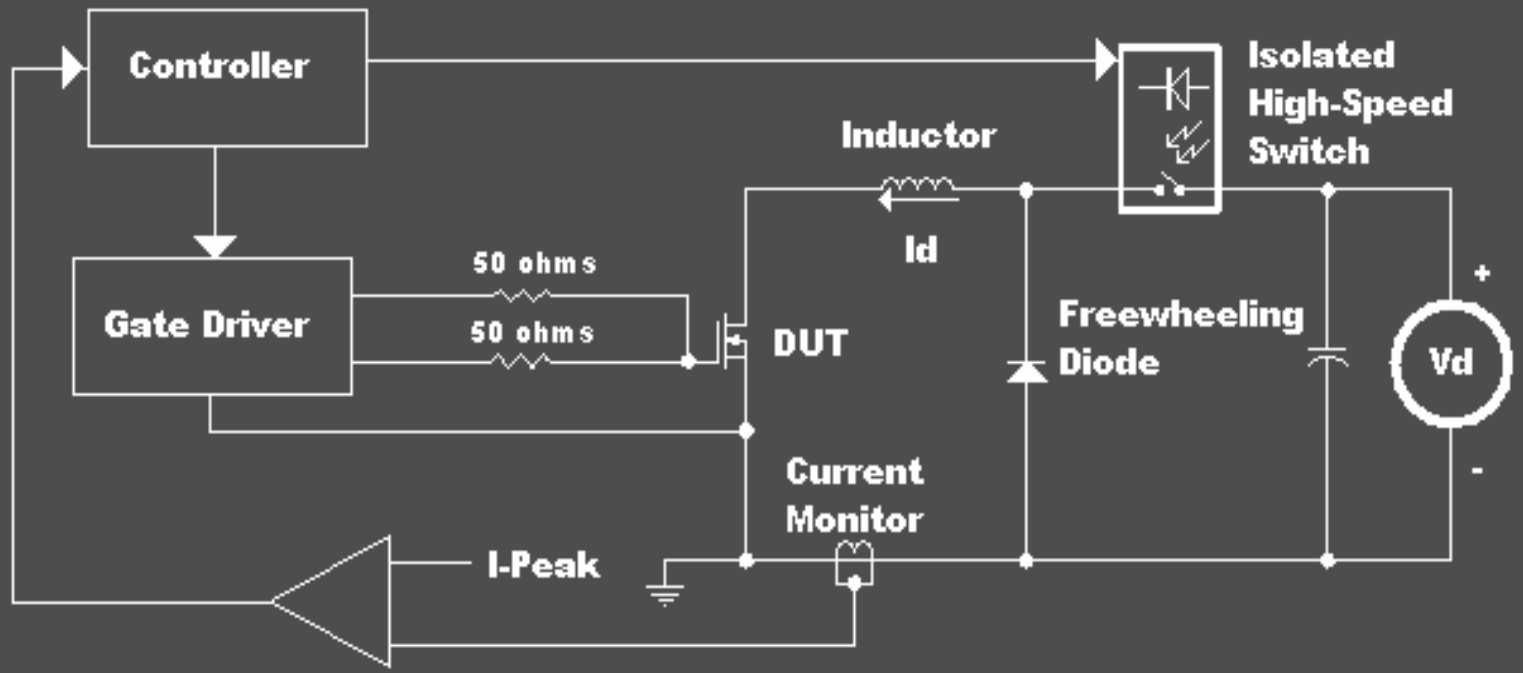
Agenda

- Background of Avalanche Testing
- Package Avalanche Testing
- Die and Wafer Testing
- Protection of Probe Tips
- Die and Wafer Full Power Testing

Avalanche Testing Background

- MOSFET Avalanche Testing - 1985
- Initially Manufacturers Disagreed
- Now Manufacturers Provide Avalanche Energy Ratings
- What Is Avalanche Mode?
- What Is Ruggedness?
- Avalanche Test Method Standards
  - MIL-STD-750 METHOD 3470.2
  - JEDEC STANDARD JESD24-5

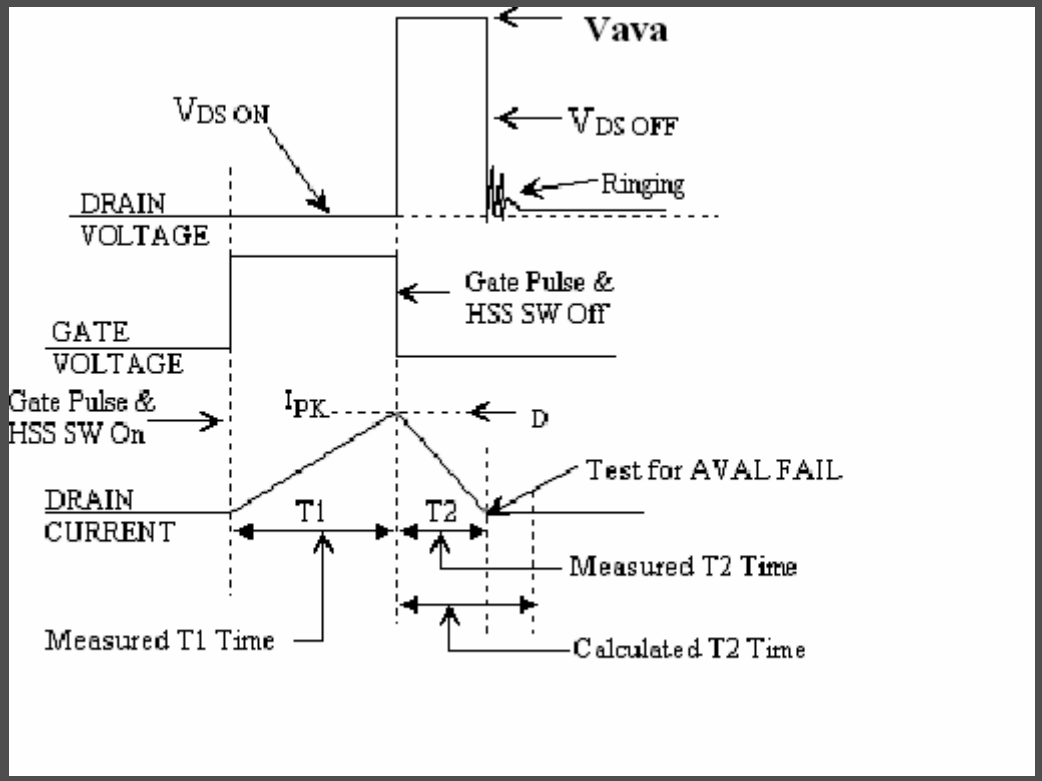
Ideal Avalanche Test Circuit



Decoupled VD UIS Method

$E_{AVA} = \frac{1}{2} L \times I^2_D$

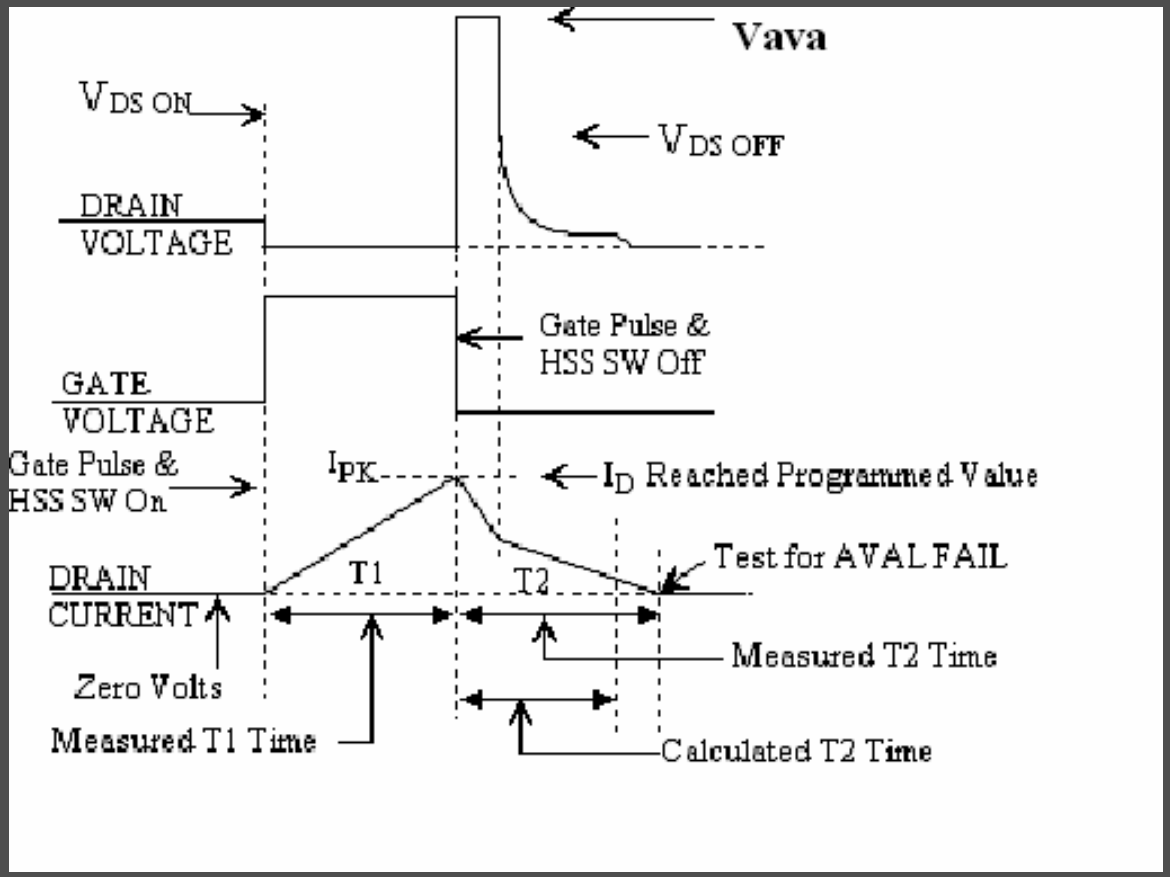
Good Avalanche Test Waveform



T1 and T2 Times
Calculated From:
- Inductance Value
- I Peak
- Rated Drain Voltage

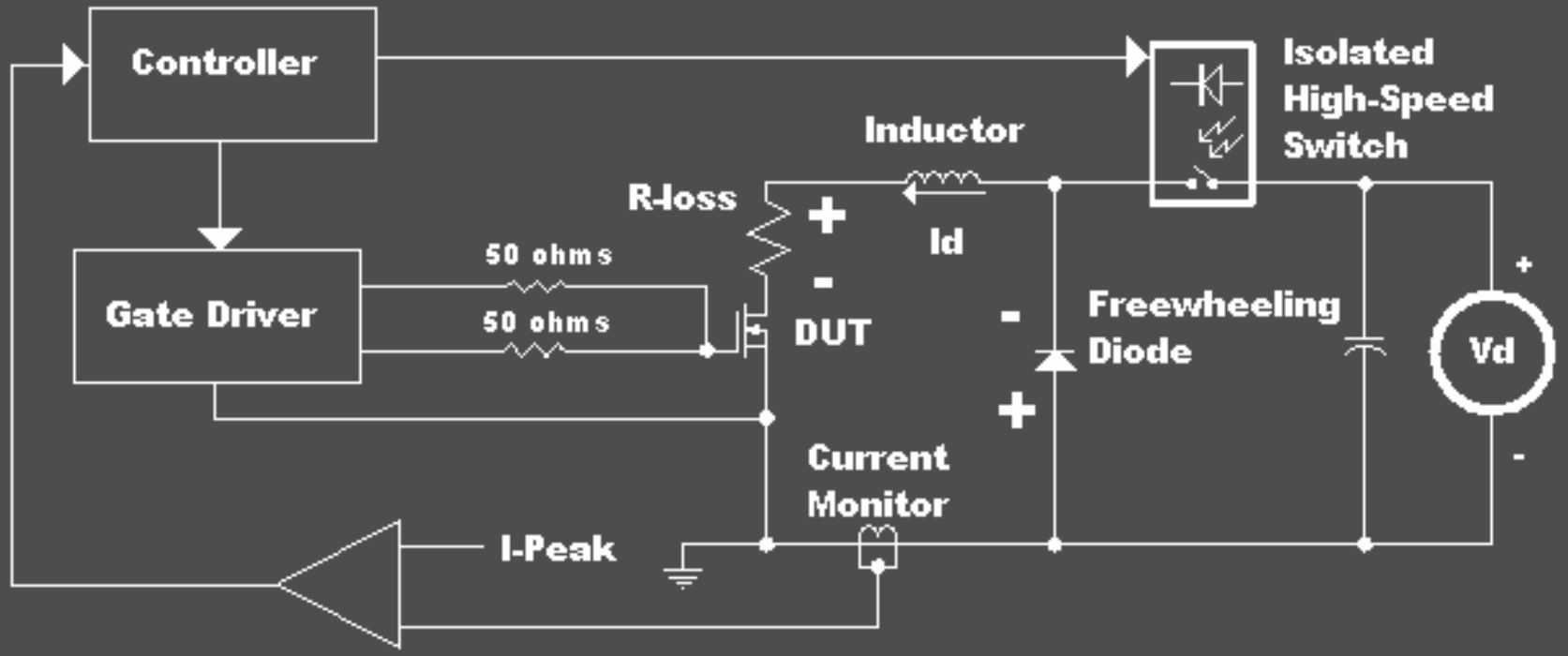
Shows DUT Passing Avalanche
Based On Measured T2 Time

Failed Avalanche Test Waveform



Shows DUT Failing Avalanche Based On Measured T2 Time

Real-World Avalanche Circuit



$R_{Loss} > 0$

$$T_1 = \frac{L}{R_{Loss}} LN\left(1 - \frac{R_{Loss} * I_P}{V_{ON}}\right)$$

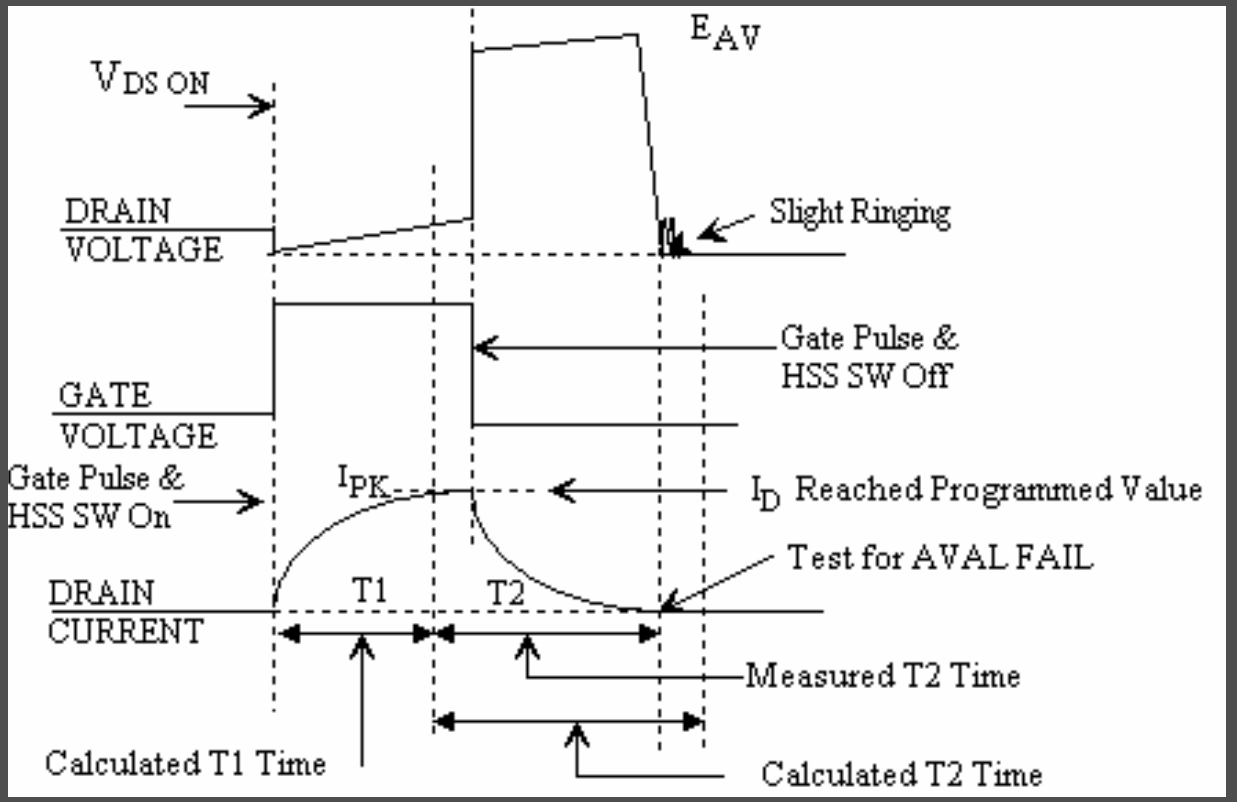
$$T_2 = \frac{L}{R_{Loss}} LN\left(1 - \frac{V_{ON}}{R_{Loss} * I_P + V_{ON}}\right)$$

$$V_{ON} = V_{Loss} + V_{DUT\ ON}$$

$$V_{OFF} = V_{Loss} + V_{DUT\ OFF}$$

$$V_{DUT\ OFF} = V_{Avalanche}$$

Real-World With Losses Waveform

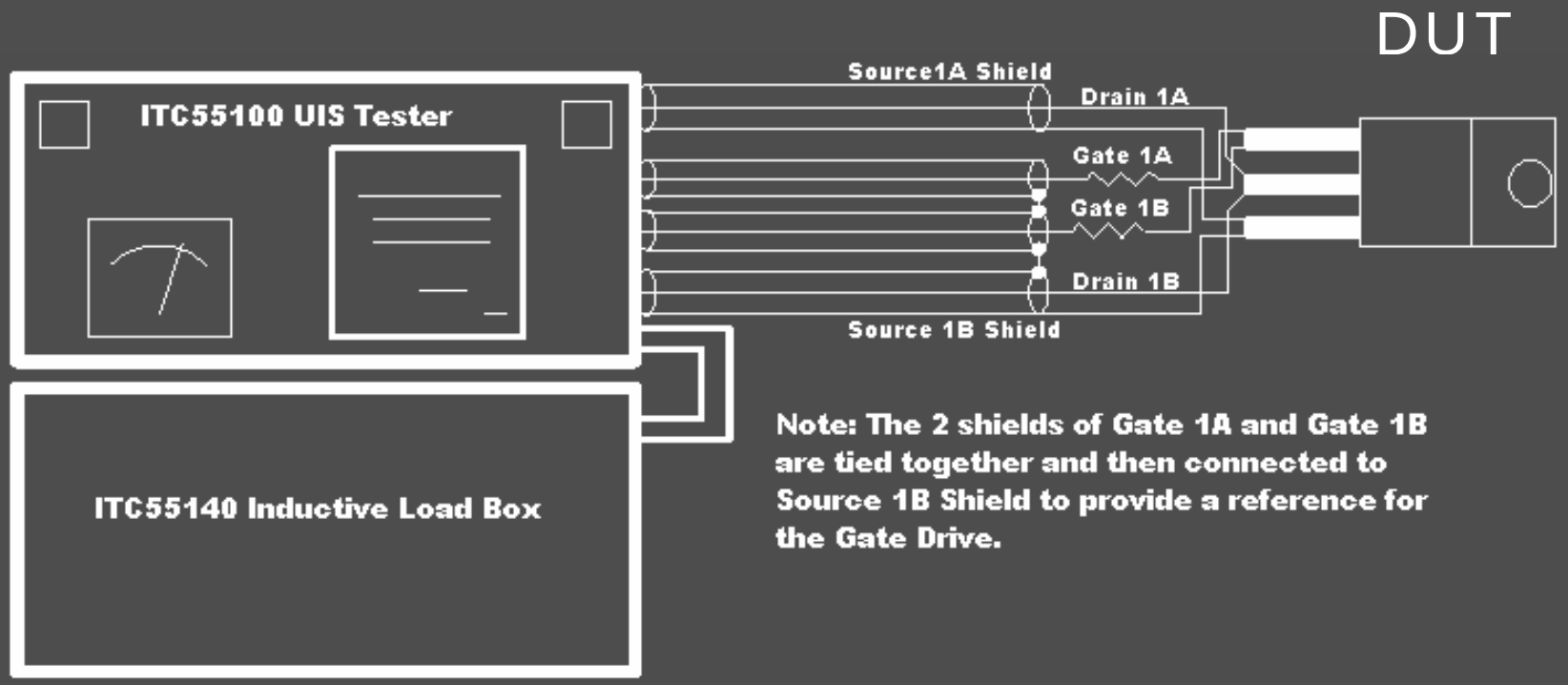


Note the “Rounded Current” Waveshape

Losses Increase T1 Time

Losses Decrease T2 Time

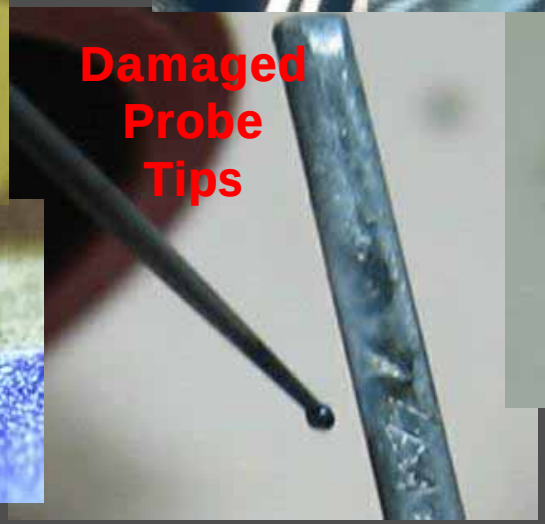
Package Level Avalanche Testing



Note: The 2 shields of Gate 1A and Gate 1B are tied together and then connected to Source 1B Shield to provide a reference for the Gate Drive.

... now to extend this same testing to Wafer and Die

High Power Testing on Probe Cards



PROBILT BY ITC

PRODUCTIVITY SOLUTIONS FOR PROBE & TEST

Wafer and Die
High Power Avalanche Testing

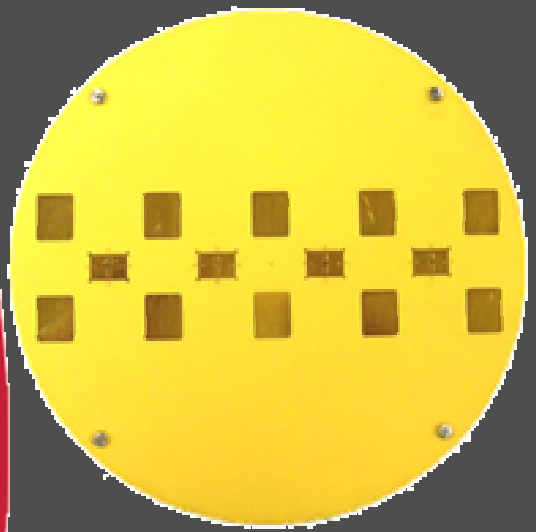
Realities:

- Probe Cards
- Probe Tips
- Testing Environment

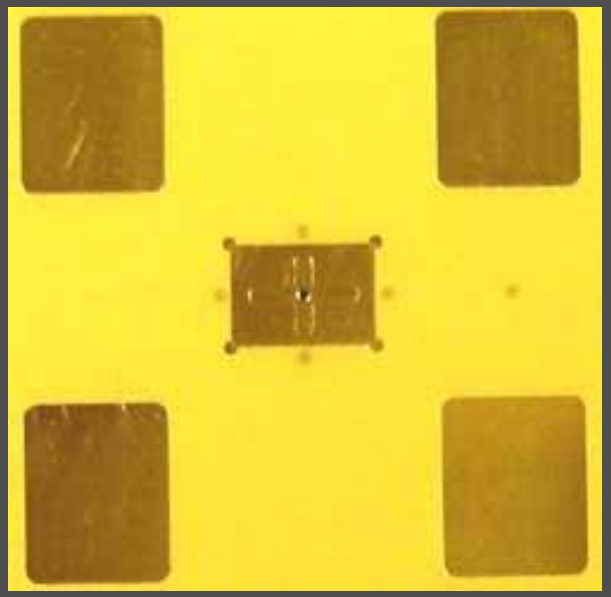
Benefits:

- Lower Cost Failures
- Faster Process Analysis
- Higher Net Yield
- Comparison with Packaged Parts

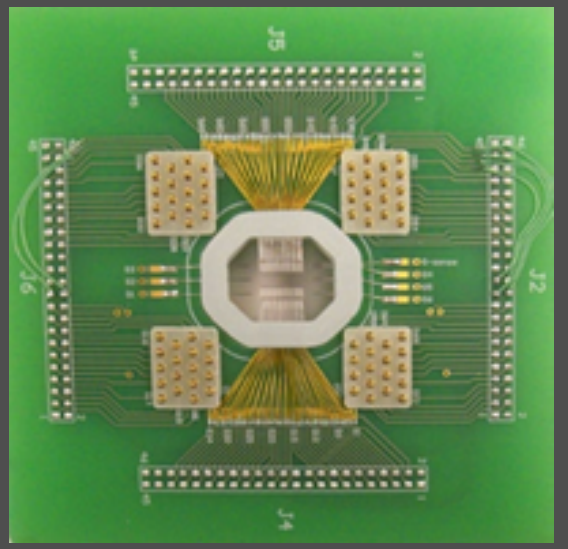
Typical Die/Chip Carrier & Probe Card



Chip Carrier



Enlarged Carrier View



Probe Card with

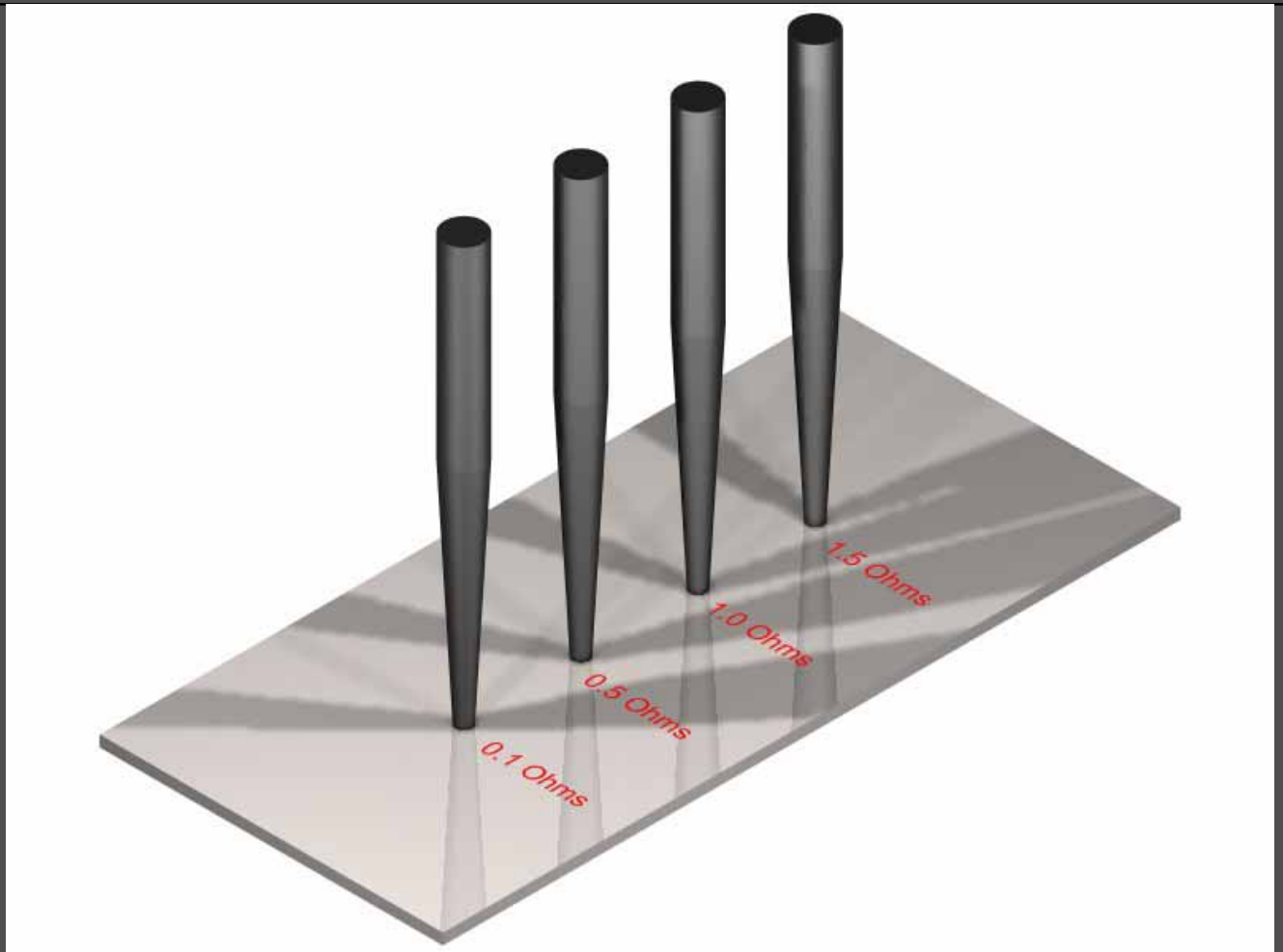
5 mil tip dia probes

and Pogo Pins

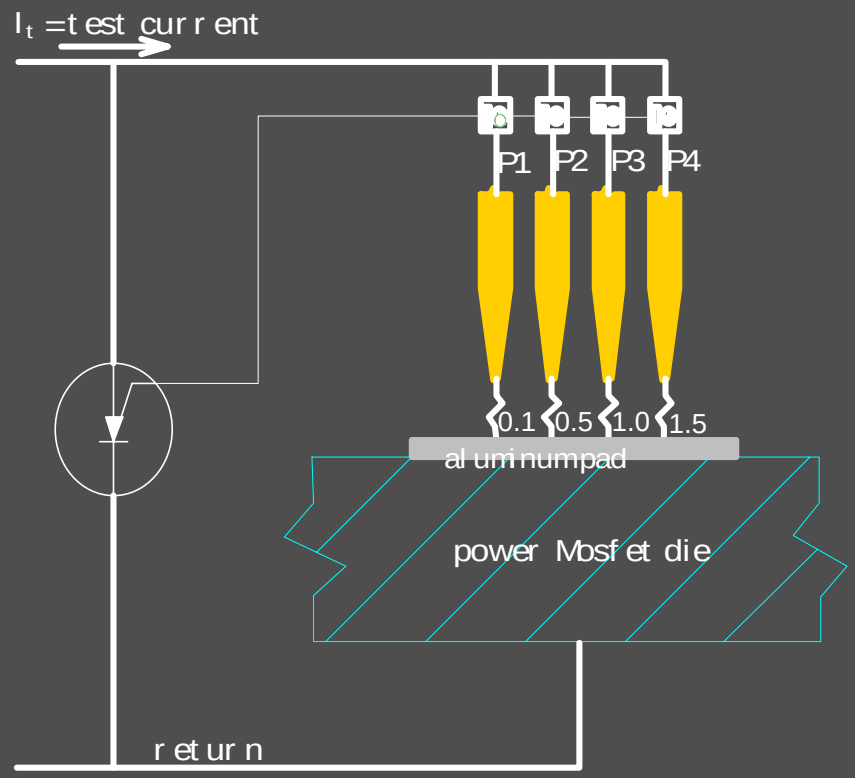
PRODUCTIVITY SOLUTIONS FOR PROBE & TEST

200 Amp, 1000V Probe Card

Probe Tips on Aluminum Pad



Probe Tip Protection Technique



It = 20 Amps

Imax = 5A/Probe, 5 mil dia

I_{P1} = 5A, V_{P1} = 0.5V

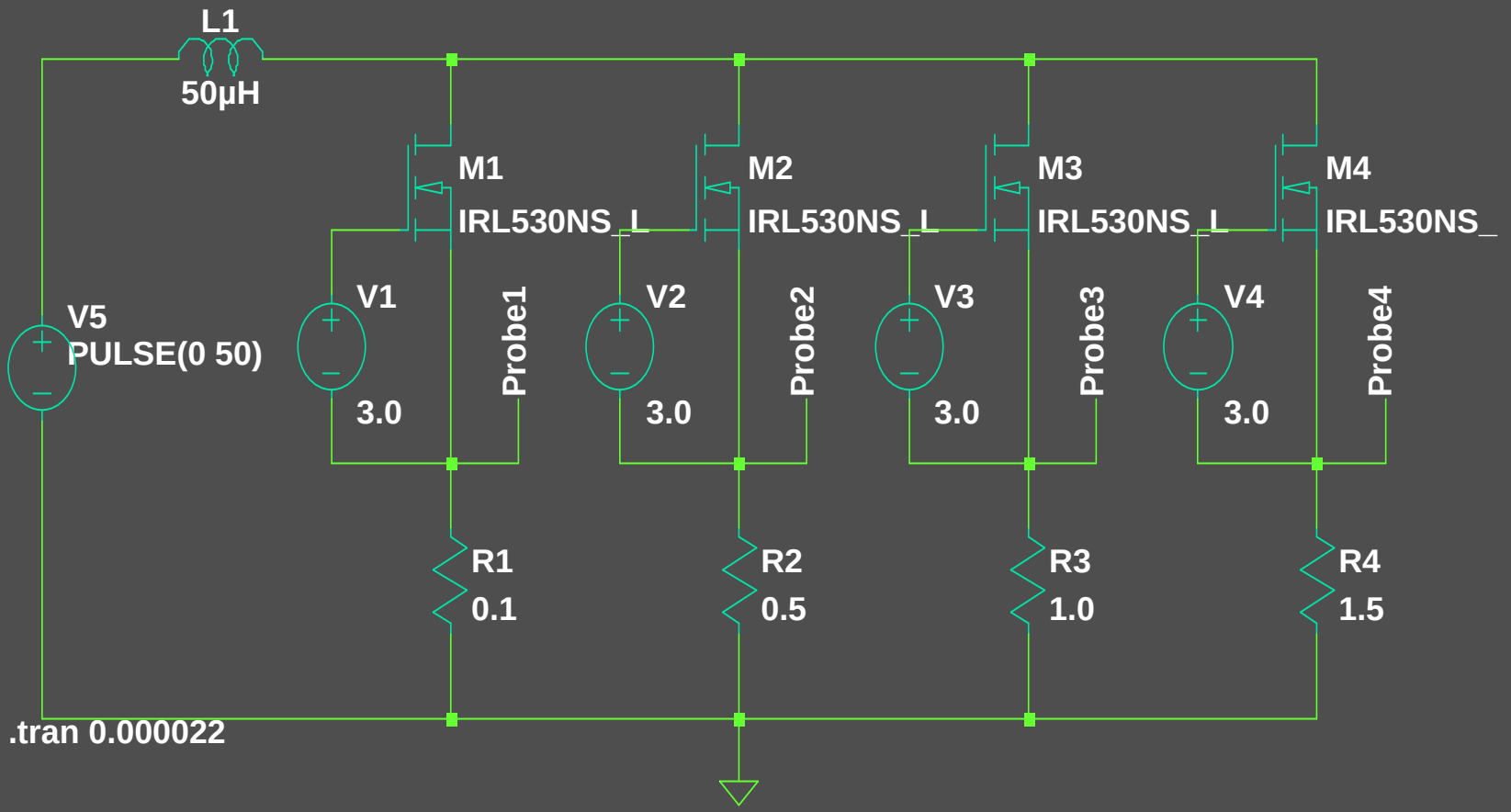
P_{P1} = 2.5W

Manage Probe Current & Voltage to keep POWER Dissipation from harming Probes

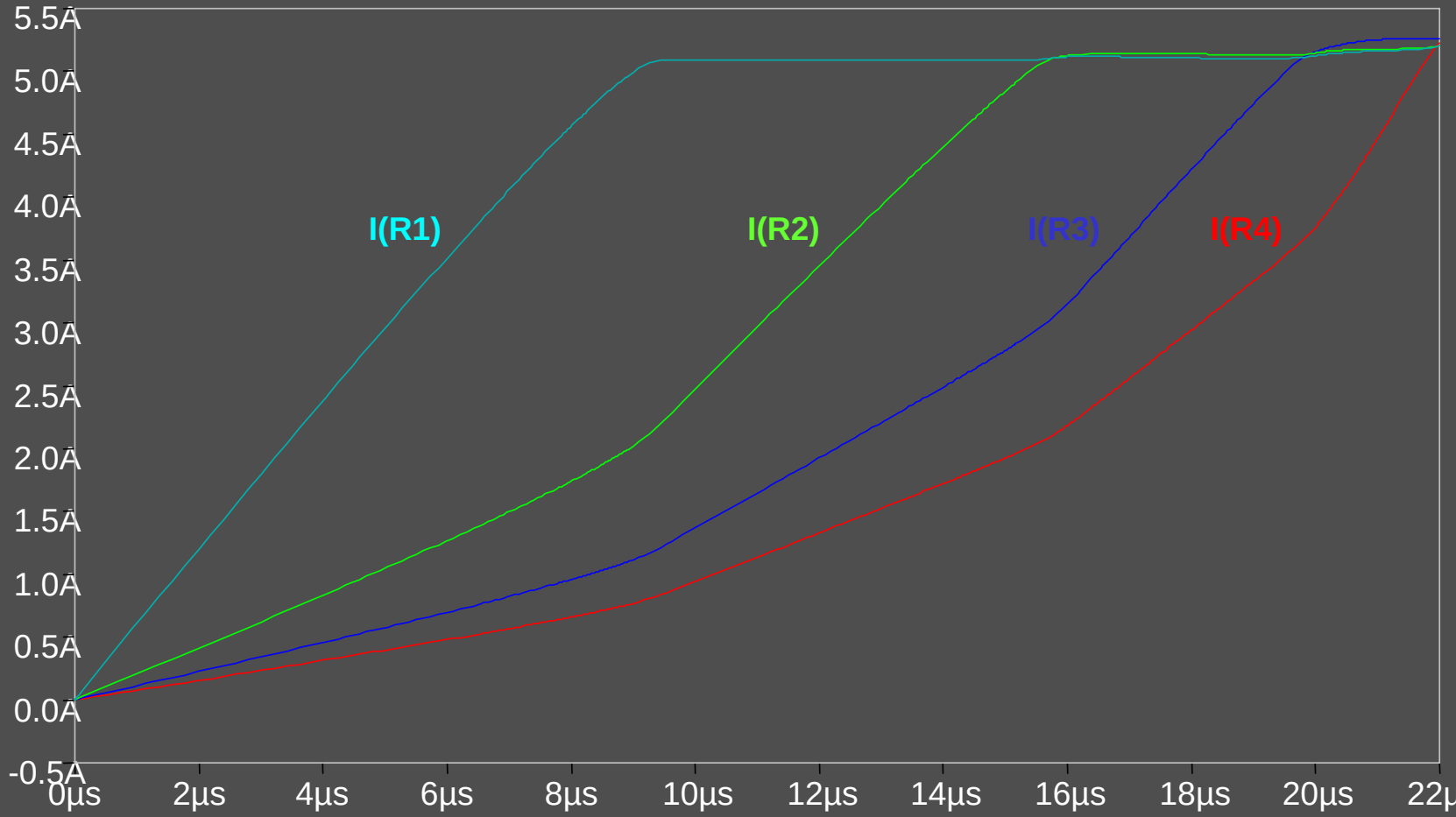
I_{P4} = 5A, V_{P4} = 7.5V

P_{P4} = 37.5W!!!!
TOO HIGH

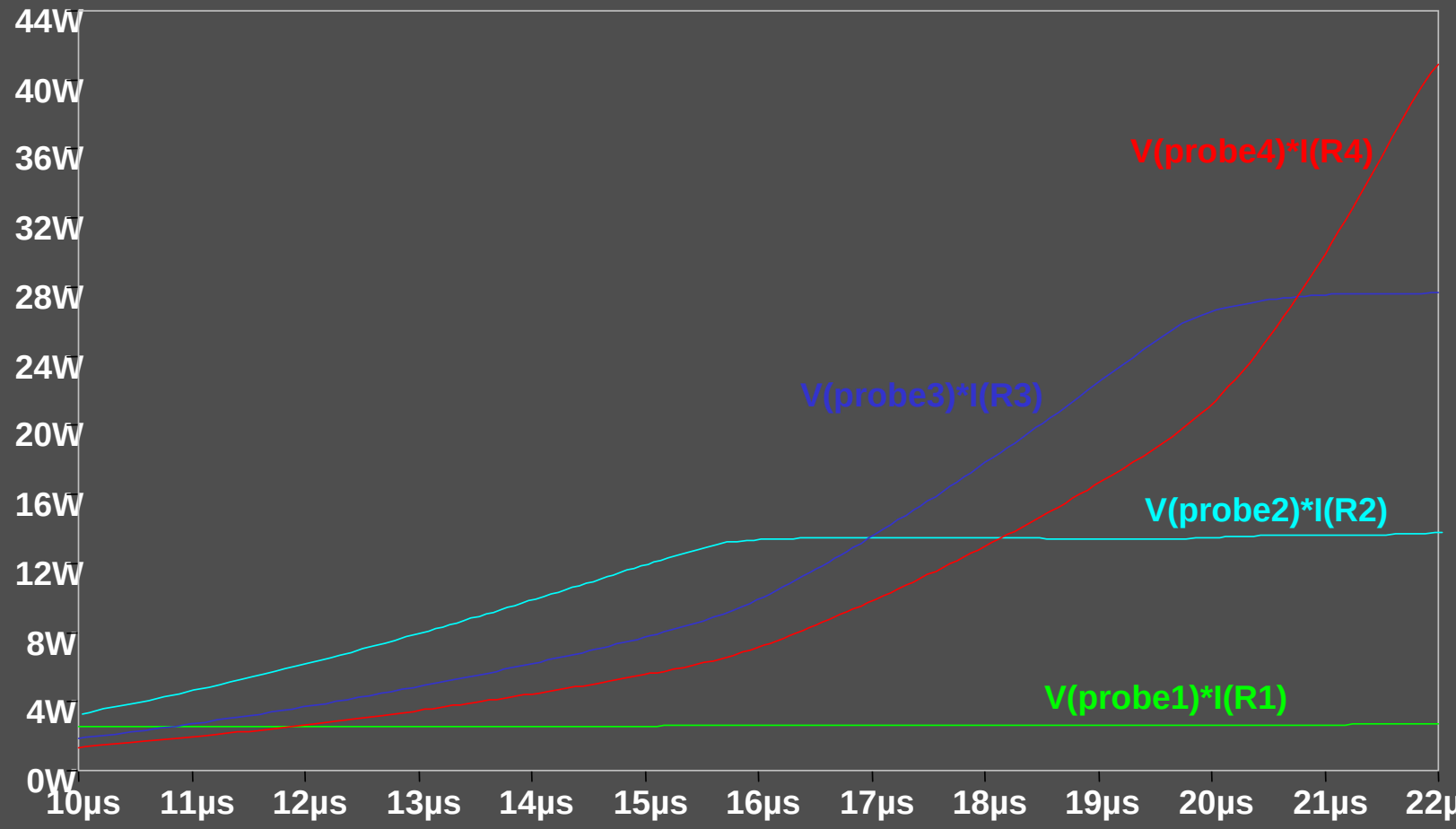
Probe Simulation Circuit



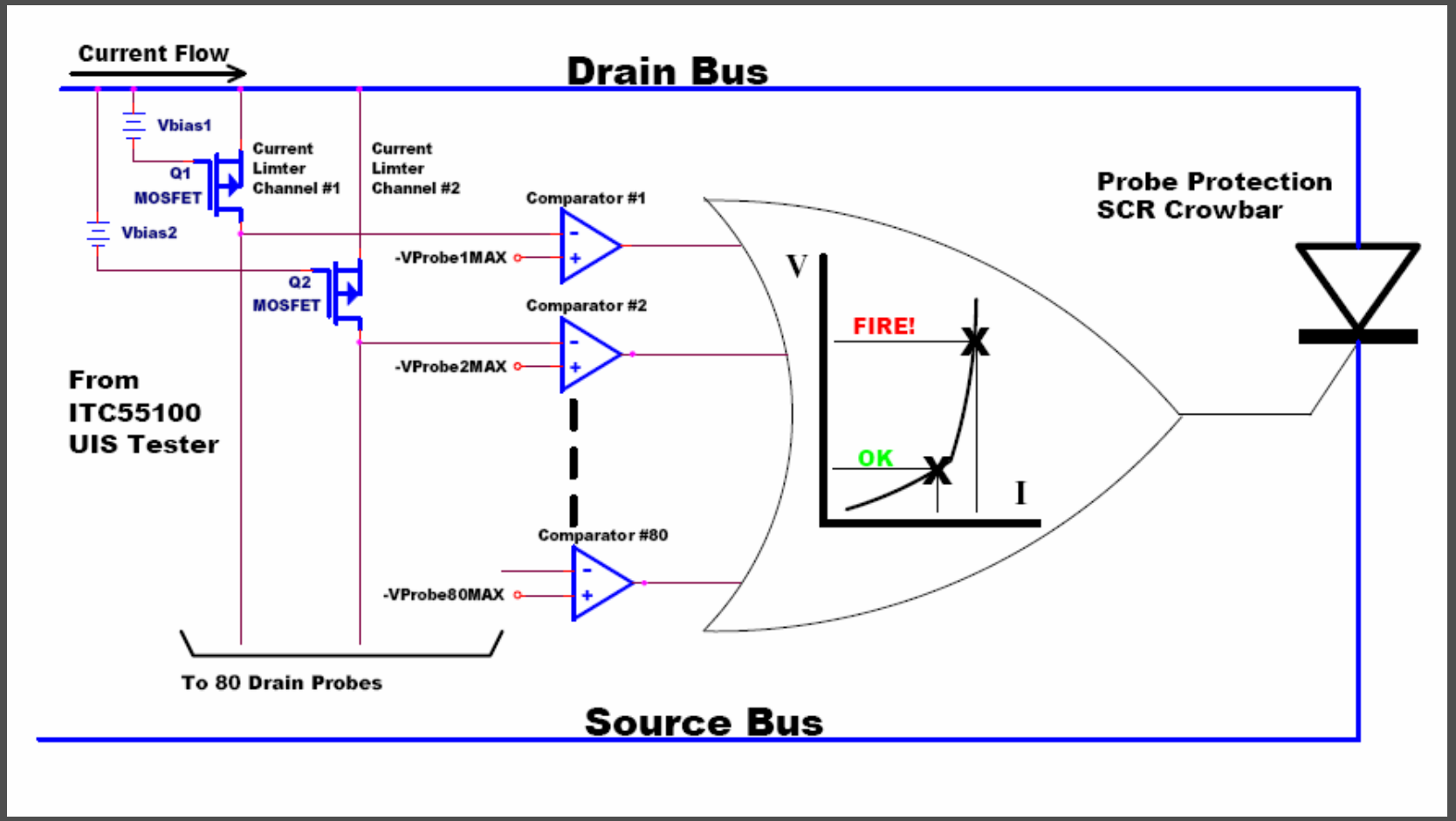
Probe Tip Currents



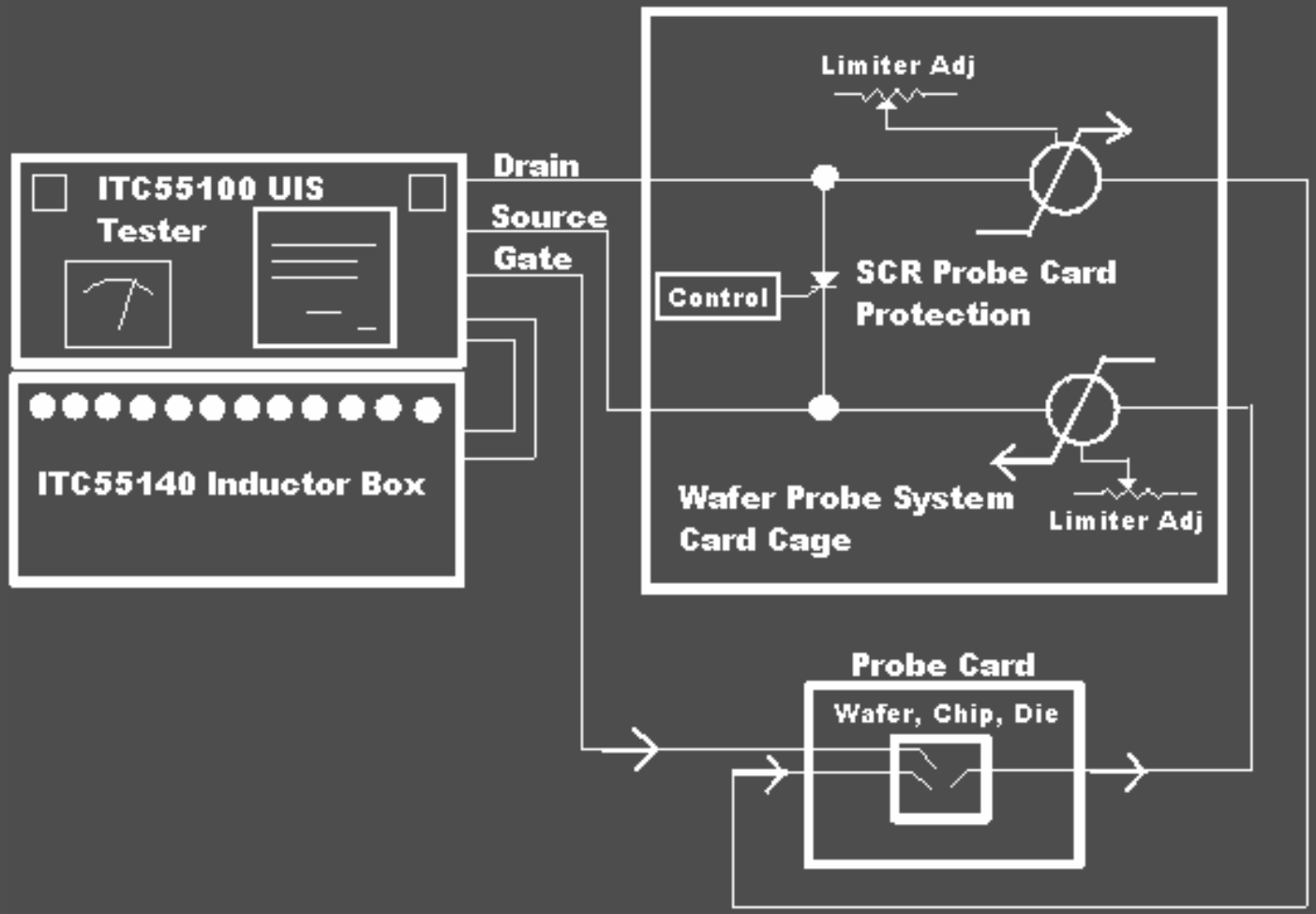
Probe Tip POWER



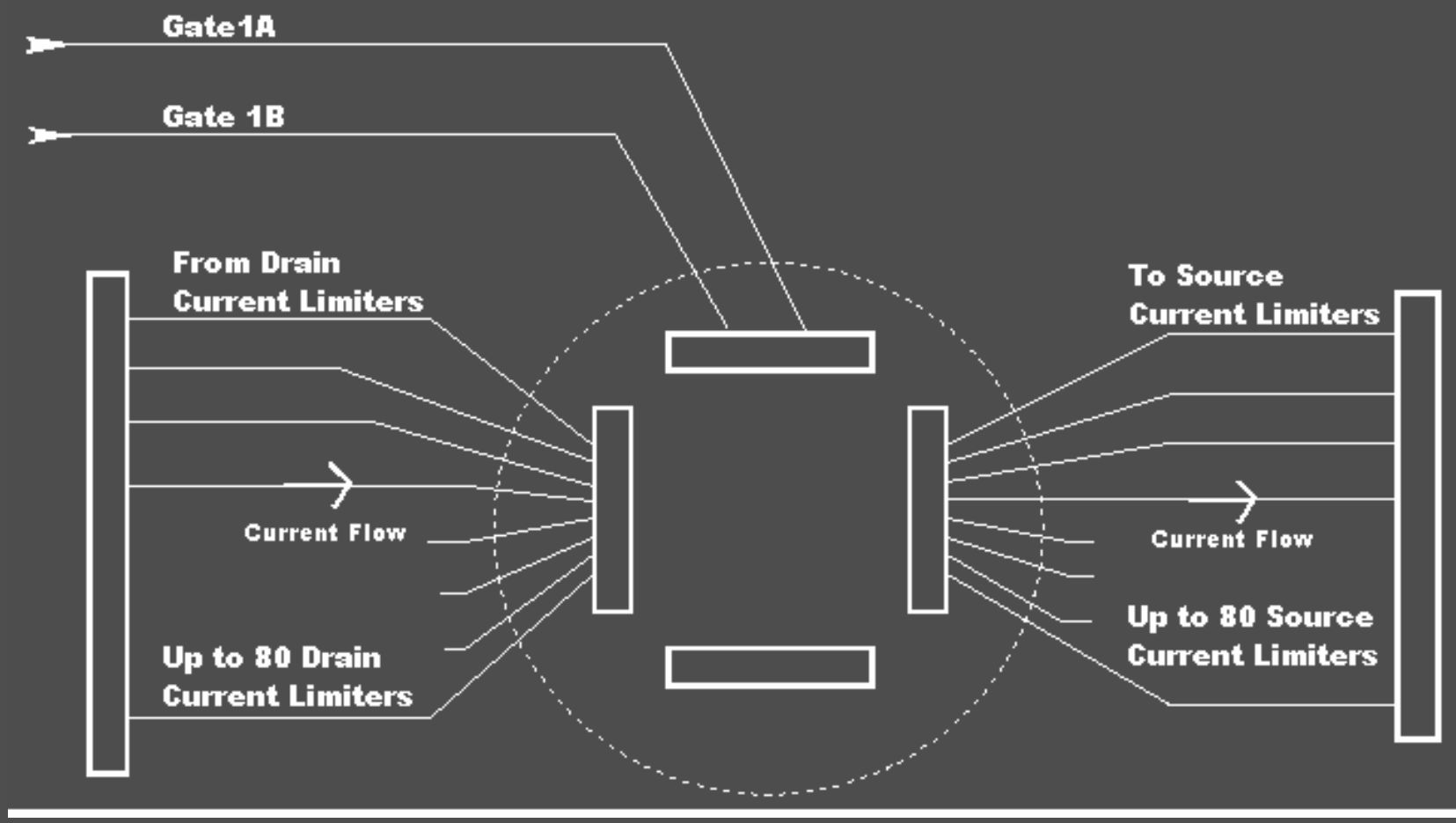
Power Limiter Showing Probe Tip Protection Concept



Production Avalanche WPS



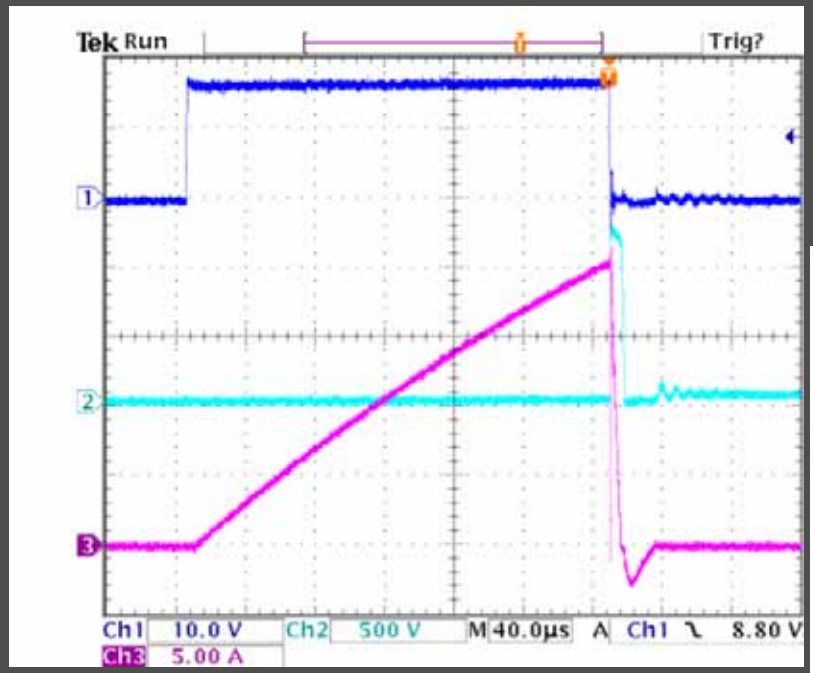
Simple Avalanche Connection Diagram

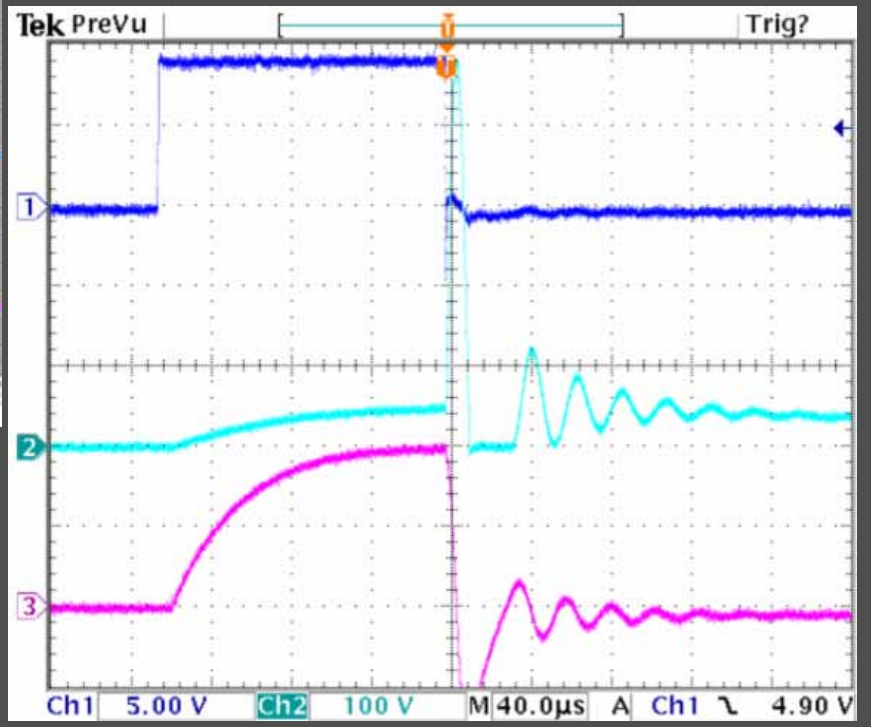


PROBILT BY ITC

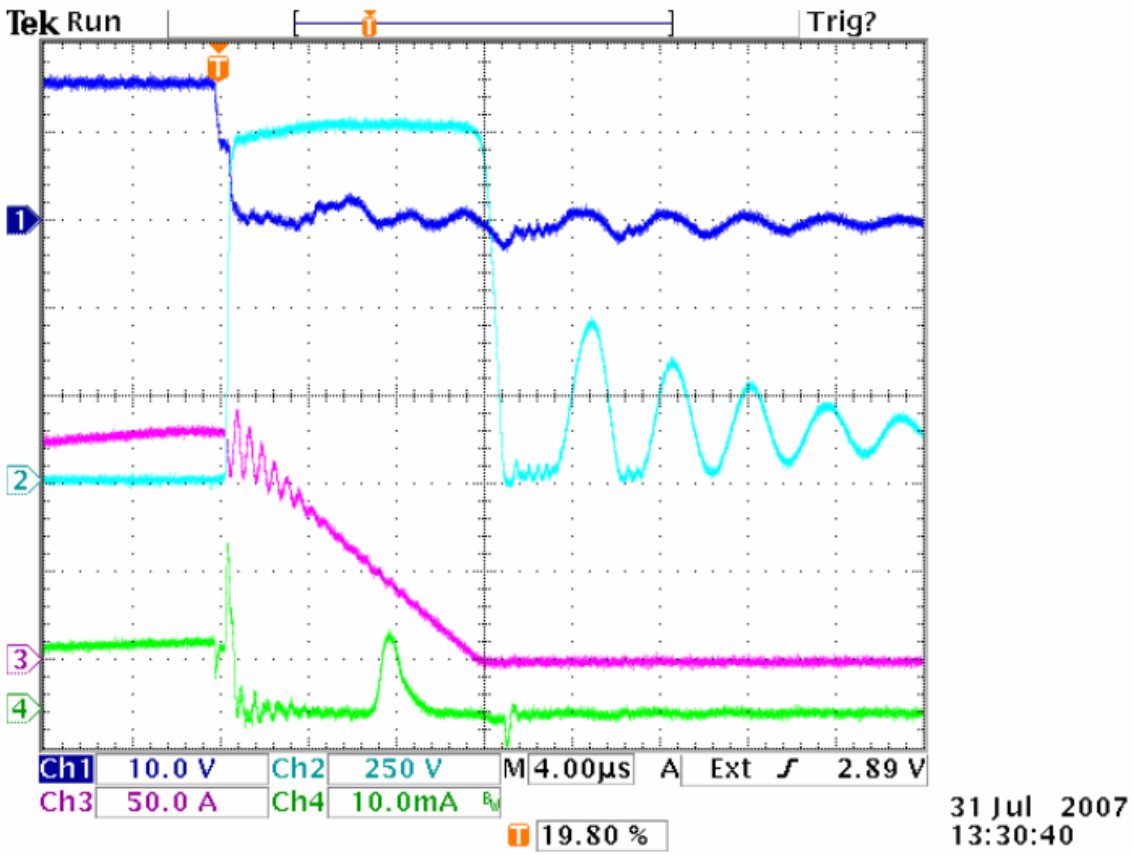
PRODUCTIVITY SOLUTIONS FOR PROBE & TEST

Realized Avalanche Waveforms





Avalanche Waveform – PASS



AVALANCHE 125A Vg = 15V

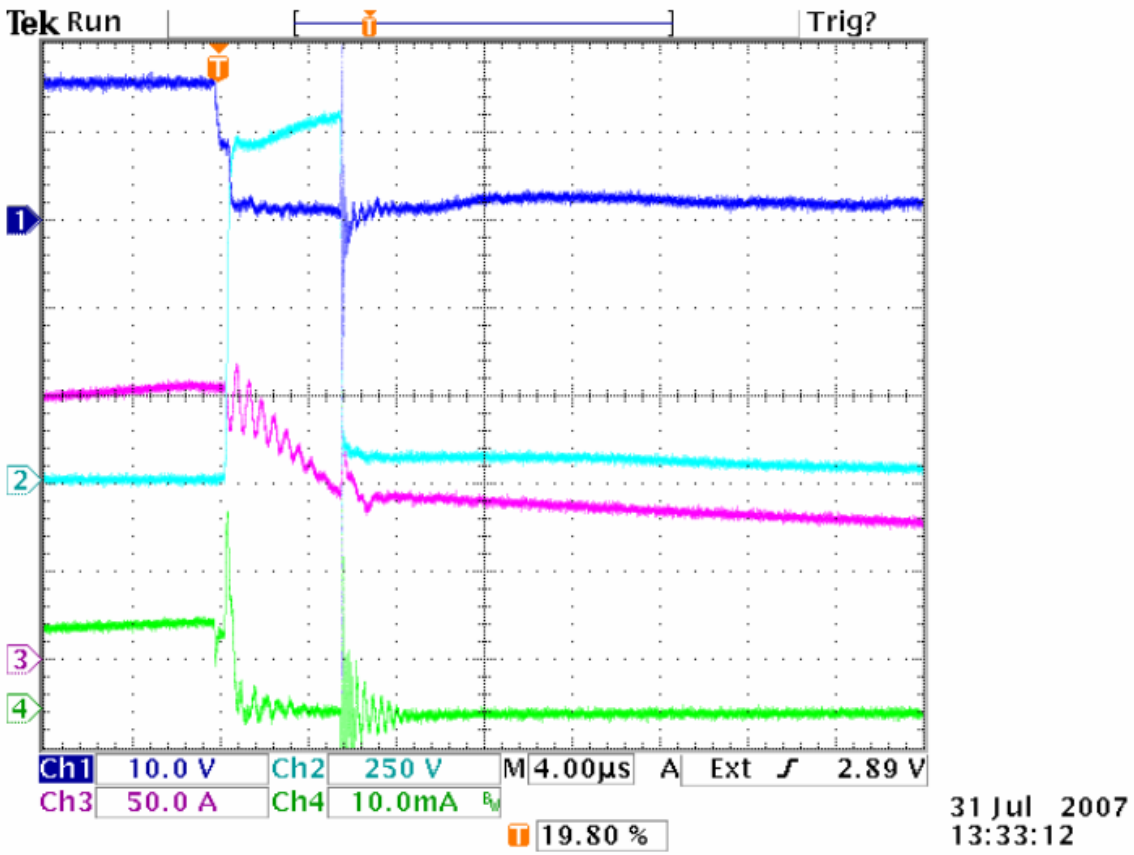
Collector Current

Collector Voltage

Gate Voltage

Sense Emitter

Avalanche Waveform – FAILURE



AVALANCHE 150A FAILURE

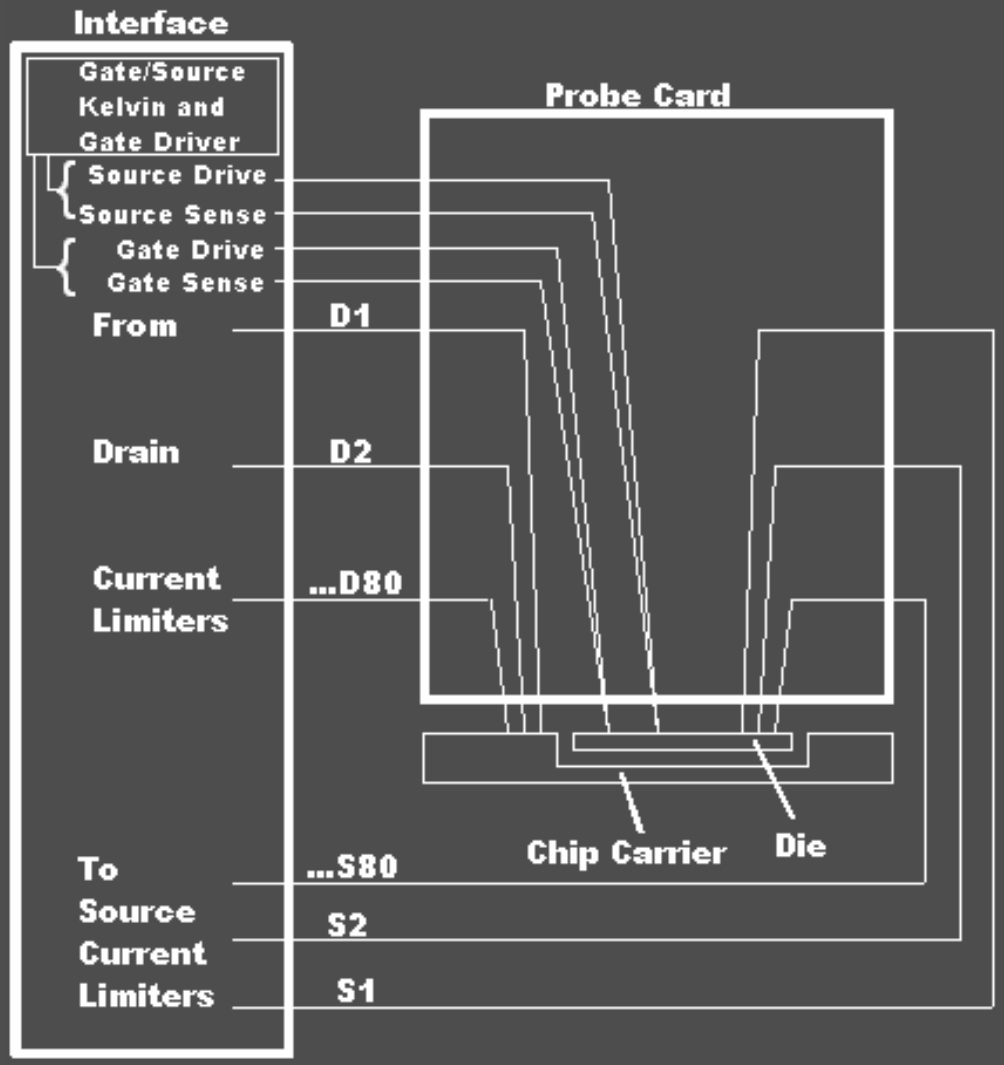
Collector Current

Collector Voltage

Gate Voltage

Sense Emitter

Advanced Chip or Die Level Avalanche Testing Connections



WPS Current Limiter Overview

- Patent-Pending Power Limiter Circuit
- Set for 5 Amps per Probe and uses Standard Probe Card Technology
- Limits Maximum Current In The BEST Probe
- Limits Maximum Power in the WORST Probe
- Voltage Across Contact Resistance Monitored for Complete Protection

Summary

- Allows for Standard Avalanche Test Methods to be used FULL Power
- Expandable to High Power and High Current Parts and Tests
- Power MOSFETs, IGBTs, Diodes, Transzorbs
- Avalanche, RB_{SOA}, V_{DSON}, R_{DSON}, V_{CEON}, $V_{F\text{-}SD}$(body diode)
- All performed with the SAME equipment at the SAME Probe Station
- Allows Correlation with Packaged Parts

References

Tim McDonald, Marco Soldano, Anthony Murry, Teodor Avram *"Power MOSFET Avalanche Design Guidelines"* IR Application Note AN-1006

Kenneth Dierberger "*Understanding The Difference Between Standard MOSFETs and Avalanche Energy Rated MOSFETs*" Advanced Power Technology Application Note

"*Power MOSFET Single-Shot And Repetitive Avalanche Ruggedness Rating*"
Philips Semiconductor Application Note AN10273-1

Warren Schultz "*Power Transistor Safe Operating Area*" ON Semiconductor
Application Note AN875/D

Michael Bairanzade "*Understanding Power Transistors Breakdown Parameters*"
ON Semiconductor Application Note AN1628/D