Reconfigurable CMOS Mixers for Radio-Frequency Applications

by

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Abstract

This thesis focuses on the design of radio-frequency (RF) mixers, including a broadband downconverter mixer, an upconverter mixer and a downconverter mixer with high linearity. The basic mixer topology used in this thesis was the Gilbert cell mixer, which is the most popular mixer topology in modern communication systems. In order to accommodate different applications, the broadband mixer and the upconverter mixer were designed to be reconfigurable.

First, a broadband downconverter mixer with variable conversion gain was designed using 0.13-μm CMOS technology. The mixer worked from 2 to 10 GHz. By changing the effective transistor size of the transconductor and the load, the mixer was able to work in three different modes with different conversion gain and power consumption.

Second, an upconverter mixer with sideband selection was demonstrated in CMOS 0.13-μm technology. The transmitted sideband could be chosen to be the upper sideband or the lower sideband. The mixer worked at 5 GHz with a 100 MHz IF. The measured voltage conversion gains were 11.2 dB at 4.9 GHz and 12.4 dB at 5.1 GHz. The best sideband rejection was around 30 dB.

Third, a modified derivative superposition (DS) technique was used to linearize a Gilbert cell mixer. Simulation results predicted an IIP3 improvement of 12.5 dB at 1 GHz. After linearization, the noise figure of the mixer increased by only 0.7 dB and the conversion gain decreased by 0.3 dB. The power consumption of the mixer increased by 0.96 mW.

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Nomenclature

Latin Symbols

A_v	Voltage Gain [V/V]
C_{gs}	Gate to Source Capacitance [F]
C_{gd}	Gate to Drain Capacitance [F]
F	Noise Factor
f	Frequency [Hz]
f_{IF}	IF Frequency [Hz]
f_{LO}	LO Frequency [Hz]
F_{min}	Minimum Noise Factor
f_{RF}	RF Frequency [Hz]
f_T	Unit Current Gain Frequency [Hz]
Δf	Bandwidth [Hz]
G	Gain
g_{d0}	Drain-Source Conductance at V_{DS}=0 [A/V]
g_m	Transconductance [A/V]
g_{mb}	Back Gate Transconductance [A/V]
$\overline{i_{nd}^2}$	Drain Current Noise Spectral Density [A^2/Hz]
$\overline{i_{ng}^2}$	Gate Current Noise Spectral Density [A^2/Hz]
k	Boltzmann's Constant [J/K]
q	Electron Charge [C]

R_L	Load Resistor [Ω]
T	Absolute Temperature [T]
V_{DD}	DC Supply Voltage [V]
V_{DS}	DC Drain to Source Voltage [V]
V_{GS}	DC Gate to Source Voltage [V]
W	Transistor Width [μm]

Greek Symbols

γ	Transistor Noise Coefficient
δ	Gate Noise Coefficient
ω	Angular Frequency [rad/s]
ω_{IF}	IF Angular Frequency [rad/s]
ω_{LO}	LO Angular Frequency [rad/s]
ω_{RF}	RF Angular Frequency [rad/s]
ω_T	Unity Current Gain Angular Frequency [rad/s]
μ_n	Electron Mobility [$cm^2/V \cdot S$]

Acronyms

CG	Voltage Conversion Gain [V/V]
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
DSB	Double Sideband
FET	Field Effect Transistor
GSG	Ground-Signal-Ground
GSGSG	Ground-Signal-Ground-Signal-Ground
IBM	International Business Machines Corporation

IC	Integrated Circuits
IEEE	Institute of Electrical and Electronics Engineering
IF	Intermediate Frequency
IIP3	Input-referred Third-order Intercept Point
IMD3	Third-order Intermodulation Distortion Products
LNA	Low Noise Amplifier
LO	Local Oscillator
MMIC	Microwave Monolithic Integrated Circuits
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-type Metal Oxide Semiconductor
NF	Noise Figure
NF_{DSB}	Double Sideband Noise Figure
NF_{SSB}	Double Sideband Noise Figure
P1dB	1-dB Compression Point
PMOS	p-type Metal Oxide Semiconductor
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
SSB	Single Sideband
UWB	Ultra-wide Band
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Introduction

The momentum for lower cost transceivers in the market is enormous, which makes CMOS the most attractive technology due to its low cost and high yield. Since the cost of CMOS transceivers is heavily weighted by the silicon area and packaging, extensive effort has been taken to reduce the chip size and improve the integration level. On one hand, CMOS continues to scale down from one generation to the next to put more transistors and functions on a certain area. On the other hand, integrating the digital baseband circuits along with the RF/analog circuits on a single chip can greatly alleviate the packaging problem and improve system integration level.

However, despite the lower cost, the design and integration of RF/analog circuits in a commercial CMOS technology are not without problems. In general, MOS field effect transistors (MOSFETs) suffer from severe trade-offs between speed and power dissipation as well as noise and power dissipation. In addition, as the supply voltage scales down with the channel length, linearity tends to degrade from one generation to the next. These problems have entailed active research on architectures, circuits, and devices in the past decades.

Figure 1.1 shows a typical superheterodyne receiver. In this architecture, the

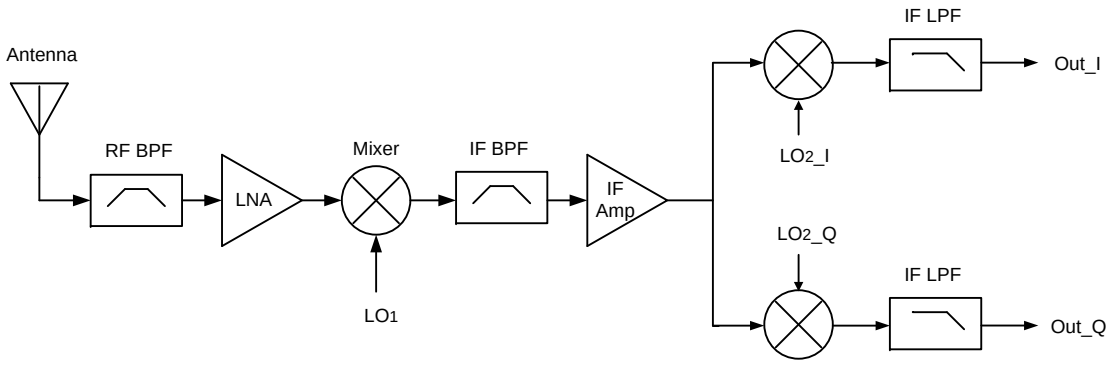

Figure 1.1: Block diagram of a superheterodyne receiver

mixer follows the low noise amplifier (LNA) and translates the amplified RF signal to the IF frequency. Recall that the noise factor (F) and third-order input intercept voltage (IIV3) of a system can be written as [5]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_n} \tag{1.1}$$

$$\frac{1}{\mathrm{IIV3}_{tot}^2} = \frac{1}{\mathrm{IIV3}_1^2} + \sum_{j=2}^{n} \left\{ \frac{1}{\mathrm{IIV3}_j^2} \prod_{i=1}^{j-1} A_{vi}^2 \right\} \tag{1.2}$$

where F_n and G_n are the noise factor and gain of the n^{th} stage of the system respectively, $\mathrm{IIV3_j}$ is the IIV3 of the j^{th} stage of the system, and A_{vi} is the voltage gain of the i^{th} stage of the system.

There are two important observations from the system noise factor and IIV3 equations. First, it is clear from Equation 1.1 that the system noise factor is in fact determined by the noise performance of the first few gain stages. In order to achieve a good overall noise factor, one needs to focus on the first few stages. Since the mixer is usually the second or third stage of the receiver front-end, its noise performance has a significant impact on the system noise factor. Second, as for the linearity, it is evident from Equation 1.2 that the later stages bear a larger burden due to the gain that precedes them. Since a typical LNA in a receiver provides power gain in

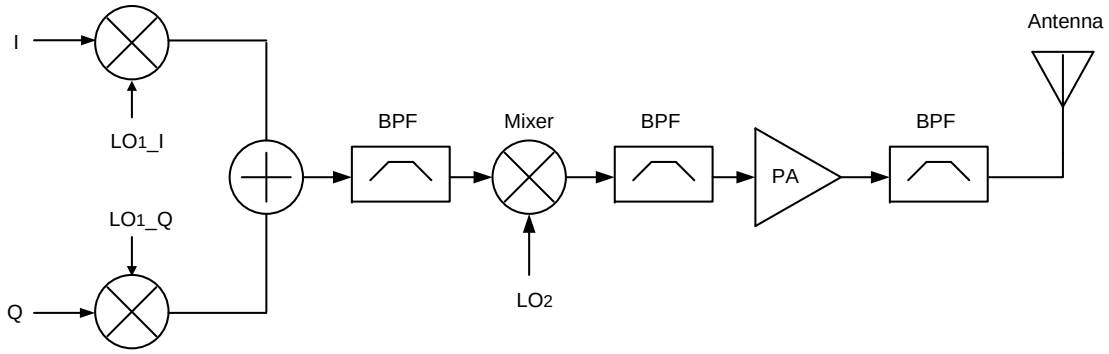

Figure 1.2: Block diagram of a superheterodyne transmitter

the range of 15-20 dB, the mixer has more stringent linearity requirement than the LNA does and hence generally determines the linearity of a receiver. Therefore, the design of low noise and high linearity mixers is of great importance to the overall performance of receivers.

In addition to frequency translation, the mixer also performs the image-rejection, which is critical in the superheterodyne architecture. The image signal can be down-converted to IF along with the desired signal, and hence degrade the signal-to-noise ratio (SNR). Although typical image-rejection ratio achieved by image-rejection mixers falls in the range of 30-35 dB, which is not enough for the requirement of a typical superheterodyne receiver (e.g. 70 dB), the use of image-rejection mixers greatly reduces the requirements for the additional on-chip or off-chip filtering that is required. In a superheterodyne transmitter, the mixer is also an important component. Figure 1.2 shows a typical superheterodyne transmitter, where the mixer translates the IF frequency to the RF frequency. Using the similar topology as in the image-rejection mixers, the mixer performs single-sideband (SSB) up-conversion which is preferred by most current communication standards.

Most of the wireless standards currently in use are narrow-band. However, driven by the ever-increasing demand for higher data rates in wireless communications, broadband standards are becoming more attractive since they usually support high data rates. For example, the ultra-wideband (UWB, 3.1 to 10.6 GHz) supports data

rates up to 480 Mb/s, which is significantly higher than the current wireless standards. In order to support standards like UWB, the design of broadband transceivers is becoming an active research area, of which one of the challenges is to design broadband circuits with reasonable performance such as LNAs and mixers.

Another active research area in transceiver design is the design of transceivers that accommodate different wireless standards [6]. The current speed of adding new modes and services is enormous. Each new mode generally requires its own radio and baseband circuit which is put into handsets using packaging. However, based on the current trend, the rate at which new services are added will soon outstrip the rate of packaging. Besides, packaging decreases the system integration level and increases the cost. Therefore, the design of transceivers that are capable of supporting different wireless standards is worthy of intensive future research. As a starting point, in this thesis, the mixers were designed to be reconfigurable.

The major contributions of this thesis are as follows:

- A broadband downconverter mixer with variable conversion gain was demonstrated. The mixer worked from 2 to 10 GHz. By changing the transconductance and the load, the mixer was able to work in three different modes. In Mode 1, the mixer had the highest conversion gain and power consumption. In Mode 2, the mixer had moderate conversion gain and power consumption. While in Mode 3, the mixer had the lowest conversion gain and power consumption.

- An upconverter mixer with sideband selection was designed in 0.13-μm CMOS technology. By setting the control voltage of the switch network, the transmitted sideband could be chosen to be the upper sideband or the lower sideband. The mixer worked at 5 GHz with a 100 MHz IF. The measured voltage conversion gain were 11.2 dB at 4.9 GHz and 12.4 dB at 5.1 GHz. The mixer achieved a best sideband rejection of 30 dB.

- A modified derivative superposition (DS) technique was proposed to linearize a Gilbert cell mixer. The advantage of the topology proposed is that it can linearize a pre-existing mixer. Post-layout simulations showed that the proposed DS technique increased the IIP3 of the mixer by 12.5 dB at 1 GHz, while the NF increased by only 0.7 dB and the conversion gain decreased by only 0.3 dB. The DC current of the mixer increased by 0.8 mA after linearization, which represented an increase of 17%.

1.2 Thesis Organization

This thesis is organized as follows:

Chapter 2 gives a general introduction to mixers. It begins with an introduction to the basic mixing concept, followed by the analysis of several mixer topologies. A brief overview on image-rejection and single-sideband (SSB) mixers are provided next. The focus of this chapter is the analysis of the Gilbert cell mixer, which is the most widely used mixer topology in modern communications [7].

In Chapter 3, a broadband mixer with variable conversion gain is presented. The chapter first introduces the mixer concept. A broadband extension technique is described in detail next, followed by the analysis of the conversion gain control technique. The chapter concludes with the measurement results.

Chapter 4 first introduces an upconverter mixer which allows the user to select the sideband of interest to be transmitted. It then describes in detail the design of the components of the proposed up-conversion mixer. Finally, the chapter concludes with simulations and measurement results of the fabricated IC.

In Chapter 5, the design of the proposed mixer using derivative superposition (DS) in 0.13-μm CMOS technology will be described step by step. It starts with the DC analysis, followed by detailed noise analysis and linearity analysis. The simulation results after post-layout extraction will be given.

Chapter 6 concludes the thesis with a summary of the performances of the circuits described in this thesis. Possible improvements and future work will also be discussed.

Chapter 2

Literature Review

In this chapter, a general introduction to mixers will be given. It starts with an introduction to the basic mixing concept, followed by the analysis of several mixer topologies. The focus of this chapter will be the analysis of the Gilbert cell mixer, which is the most widely used mixer topology in modern communications [7].

2.1 Mixer Overview

It is well known that linear, time-invariant systems are not able to produce outputs with spectral components that are not present at the input. That is, in order to perform frequency translation, the circuits used as mixers must be either nonlinear or time varying. Although the techniques used to realize mixing are quite different for different mixer topologies, the essence of all mixers lies in the concept of multiplying two signals in the time domain. Suppose that the two input signals of the mixer are $A_1cos(\omega_1 t)$ and $A_2cos(\omega_2 t)$, the multiplication can be expressed as the following equation [5]:

$$A_1cos(\omega_1 t)A_2cos(\omega_2 t) = \frac{A_1A_2}{2}\left[cos(\omega_1 t - \omega_2 t) + cos(\omega_1 t + \omega_2 t)\right] \tag{2.1}$$

It is clear that the multiplication yields the sum of the input frequencies and

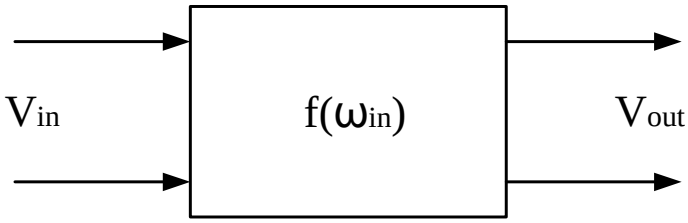

Figure 2.1: A typical nonlinear system

the difference of the input frequencies, and the amplitude of the output signal is proportional to the product of the amplitudes of the two input signals.

Thus far, many techniques have been proposed to implement the multiplication which briefly fall into two categories: nonlinearity and direct multiplication.

Figure 2.1 shows the system diagram of a typical nonlinear system, where the relationship between the input and the output can be expressed as:

$$v_{out} = \sum_{k=0}^{N} c_k (v_{in})^k \tag{2.2}$$

The output consists of three types of products, including the DC term, harmonics of the input and the intermodulation terms. Suppose that there are two frequencies at the input, namely ω_1 and ω_2. The harmonics of the input can be written as $m\omega_1$ and $n\omega_2$, where m and n refer to the m^{th} and n^{th} order of harmonics. The intermodulation terms can be expressed as $m\omega_1 \pm n\omega_2$.

The mixers based on nonlinearity have several problems. First, in a typical modern communication system, only the second-order intermodulation (IM2) term is desired. As a result, one needs to filter out the unwanted harmonics and intermodulation terms. Second, the port-to-port isolations are usually poor, which can lead to the overloading of the following stages.

The mixers based on direct multiplication, on the other hand, generally exhibit better performance. Ideally, they only generate the desired IM2 product. And since the inputs of such mixers are usually separated, the port-to-port isolations are usually much better than their nonlinearity-based counterparts. Last but not least, it is well

known that CMOS technology provides excellent switches which can be used for direct multiplication. All of the above reasons lead to the dominance of multiplication-based mixers in modern CMOS transceivers.

Below is a summary of the most important characteristics of mixers.

Conversion Gain (CG). It is defined as the ratio of the available power at the output frequency to the available power at the input frequency, which can be expressed in dB as:

$$CG = 10 \log \frac{\text{available power at the output frequency}}{\text{available power at the input frequency}} \tag{2.3}$$

If CG is smaller than 0 dB, it is called conversion loss (CL).

Up-conversion and Down-conversion. If a mixer is used to convert a signal down in frequency, which is typical in a receiver where the incoming RF is down-converted to the IF, the frequency conversion is called down-conversion. Similarly, when a mixer is used to convert a signal up in frequency as in a transmitter, the frequency conversion is called up-conversion.

Upper-sideband (USB) and Lower-sideband (LSB). It is clear from Equation 2.1 that the output of the mixer consists of two frequencies, namely, $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$. The sum frequency $\omega_1 + \omega_2$ is usually called the upper-sideband (USB), while the difference frequency $\omega_1 - \omega_2$ is referred to as the lower-sideband (LSB).

Single-sideband (SSB) and Double-sideband (DSB). If the output spectrum of a mixer consists of both the USB and the LSB, then the mixer is called a DSB mixer. Contrarily, a mixer that produces only the USB or the LSB is a SSB mixer.

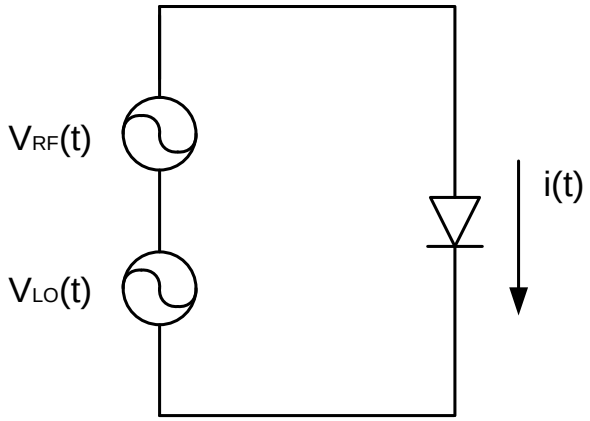

Figure 2.2: A single diode mixer

Port-to-port Isolation. The port-to-port isolation is defined as the feedthrough from one port to another. For example, the LO-to-RF isolation is defined as the ratio of the LO power that appears at the RF port to the LO power. It is often expressed in dB.

2.2 Passive Mixers

2.2.1 Diode Mixers

Diode mixers are widely used in discrete applications due to their simplicity, low noise figure and high frequency performance. Despite the conversion loss, their good characteristics have made them nearly ubiquitous in high-performance discrete equipment.

Figure 2.2 shows a basic single-ended diode mixer which uses a single diode element. The RF and LO inputs are combined at the input to drive the diode, and the bias circuits are not shown for simplicity. This mixer topology utilizes the nonlinear I-V curve of the diode. Recall that the I-V relationship of a diode can be written as:

$$i(t) = I_o \left[\exp\left(\frac{qv(t)}{nkT} - 1 \right) \right] \tag{2.4}$$

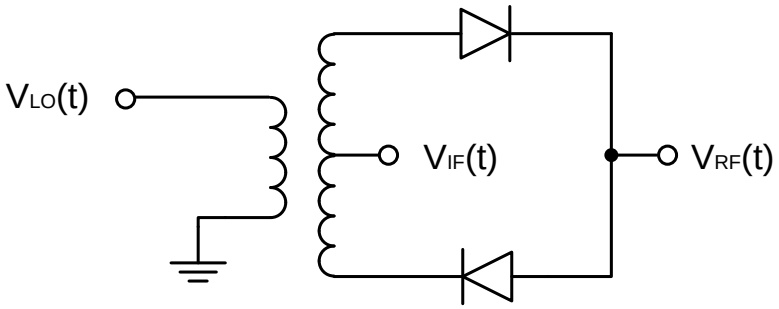

Figure 2.3: A single-balanced diode mixer

where I_o is the saturation current, q is the electron charge, k is the Boltzmann's constant, T is the absolute temperature and n is the diode ideality factor. Using the small-signal approximation, $i(t)$ can be expanded in Taylor series as:

$$i(t) = I_0 + G_d[v_{RF}(t) + v_{LO}(t)] + \frac{G_d^{'}}{2}[v_{RF}(t) + v_{LO}(t)]^2 + \cdots \tag{2.5}$$

where G_d and $G_d^{'}$ are the diode dynamic conductances. It is clear that the output current consists of many harmonics and intermodulation products. Suppose that the amplitudes of the RF and LO signals are V_{RF} and V_{LO}, the second-order intermodulation (IM2) products can be extracted from the above equation as:

$$i(t)_{IM2} = \frac{G_d^{'}}{2} V_{RF} V_{LO}[cos(\omega_{RF} - \omega_{LO})t + cos(\omega_{RF} + \omega_{LO})t] \tag{2.6}$$

The main disadvantage of the single diode mixer is that the RF-to-LO isolation is usually very poor. As a result, the two-diode mixers are used to provide a high RF-to-LO isolation, as shown in Figure 2.3. It is clear that the the RF and LO inputs are isolated. However, the RF-to-IF isolation is poor in this topology and good filtering is usually required.

In order to provide good port-to-port isolations, the double balanced diode mixer is proposed. As shown in Figure 2.4, it consists of four diodes in a bridge configuration. Suppose that the LO drive is large enough to cause the diodes to act as switches. When the LO drive is positive, the right two diodes are on and v_{IF} equals v_{RF}; when

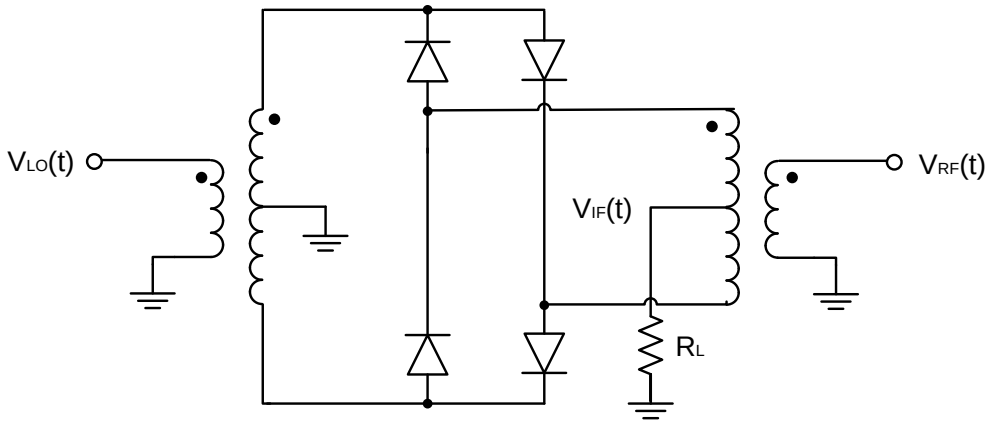

Figure 2.4: A double-balanced diode mixer

the LO drive is negative, the left two diodes are on and v_{IF} equals $-v_{RF}$.

If the circuit is well-matched, the double-balanced diode mixers can provide good isolations. It is clear from Figure 2.4 that the IF signal is connected to the virtual ground of the LO signal, which yields a high LO-to-IF isolation. Furthermore, the IF signal is also connected to the virtual ground of the RF signal. As a result, the RF-to-IF isolation is also large. Since the RF and LO signals share the virtual ground, a high RF-to-LO isolation is also achieved.

2.2.2 Passive CMOS Mixers

One of the advantages of CMOS technology is that it offers excellent switches, which can be exploited to build high-performance passive mixers. Figure 2.5 shows a double-balanced passive CMOS mixer. It switches the RF signal directly in the voltage domain without the voltage-to-current (V-I) conversion. The mixer consists of four CMOS switches in a bridge configuration. The LO signals are in anti-phase to guarantee that only one diagonal pair of transistors are on at any time. When M_1 and M_4 are on, v_{IF} equals v_{RF}; when M_2 and M_3 are on, v_{IF} equals $-v_{RF}$. The relationship between v_{IF} and v_{RF} can be written as the product of three time-varying products and a scaling factor [8]:

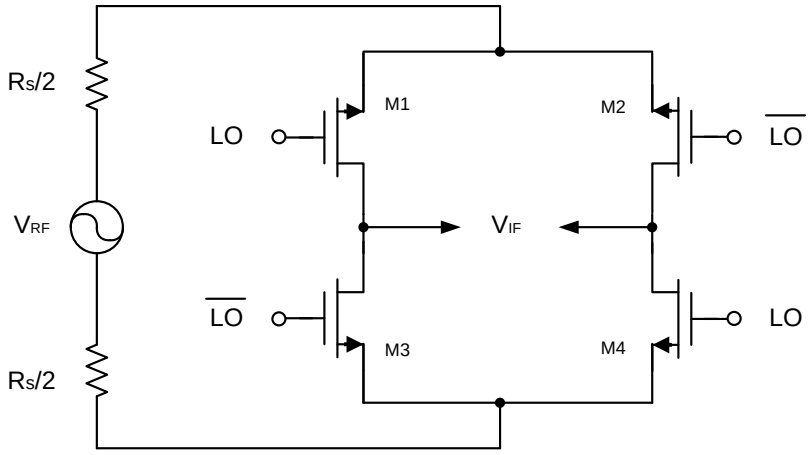

Figure 2.5: A passive CMOS mixer

$$v_{IF}(t) = v_{RF}(t)\left[\frac{g_T(t)}{g_{Tmax}}m(t)\right]\left[\frac{g_{Tmax}}{\overline{g_T}}\right] \tag{2.7}$$

The function $g_T(t)$ is the time-varying Thevenin-equivalent conductance seen from the IF port, and g_{Tmax} and $\overline{g_T}$ are the maximum and average values of $g_T(t)$. m_t is the mixing function and is defined as:

$$m(t) = \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} \tag{2.8}$$

where $g(t)$ is conductance of each switch and T_{LO} is the period of the LO drive.

The conversion gain of the mixer depends on what type of LO signal is used, namely, square wave or sinusoidal wave. The difference, however, is not significant. When a sinusoidal wave is used, the conversion gain of the mixer is $\pi/4$ or -2.1 dB, and the conversion gain drops to $2/\pi$ (-3.92 dB) when a square wave is used [5].

The most attractive properties of this mixer topology are the low power consumption, high linearity and low $1/f$ noise. Ideally, the mixer consumes no DC power, and hence has no $1/f$ noise. Typical SSB noise figure of 10 dB and IIP3 as high as 10 dBm can be achieved by using this mixer topology.

2.3 Active Mixers

2.3.1 The Single FET Mixers

The strongest nonlinearity parameters of the FET is its g_m, which can be utilized to perform mixing action. Figure 2.6(a) shows a single FET mixer. Similar to the single diode mixer, the LO and RF signals are fed into the gate of the FET. Unlike an amplifier where the FET is biased in saturation, the gate bias of the FET in Figure 2.6(a) is near the pinch-off region where g_m approaches 0. Therefore, a small variation in the gate voltage results in a large change in g_m. If the LO signal is large enough to pump g_m between the high and low states, the mixing action is achieved. The transconductance can be written as Fourier series in terms of harmonics of the LO frequency [9]:

$$g(t) = g_0 + 2\sum_{n=1}^{\infty} g_n cos\ n\omega_0(t) \tag{2.9}$$

The conversion gain (CG) of the mixer can be written as:

$$G_c = \frac{g_1^2 r_o}{4\omega_{RF}^2 C_{gs}^2 r_g} \tag{2.10}$$

where r_o is the output resistance of the FET and r_g is the gate resistance of the transistor.

The main problem of the single FET mixer in Figure 2.6(a) is that the isolation between the RF and LO ports is often very poor. Since the RF and LO frequencies are usually very close to each other (e.g. separated by several hundred MHz), one needs to use a filter with high Q to separate the LO and RF signals.

To solve this problem, the drain-pumped or source-pumped configuration can be used to separate the LO and RF input. Unlike the gate-pumped configuration, the FET is biased at saturation in the drain-pumped and source-pumped configurations.

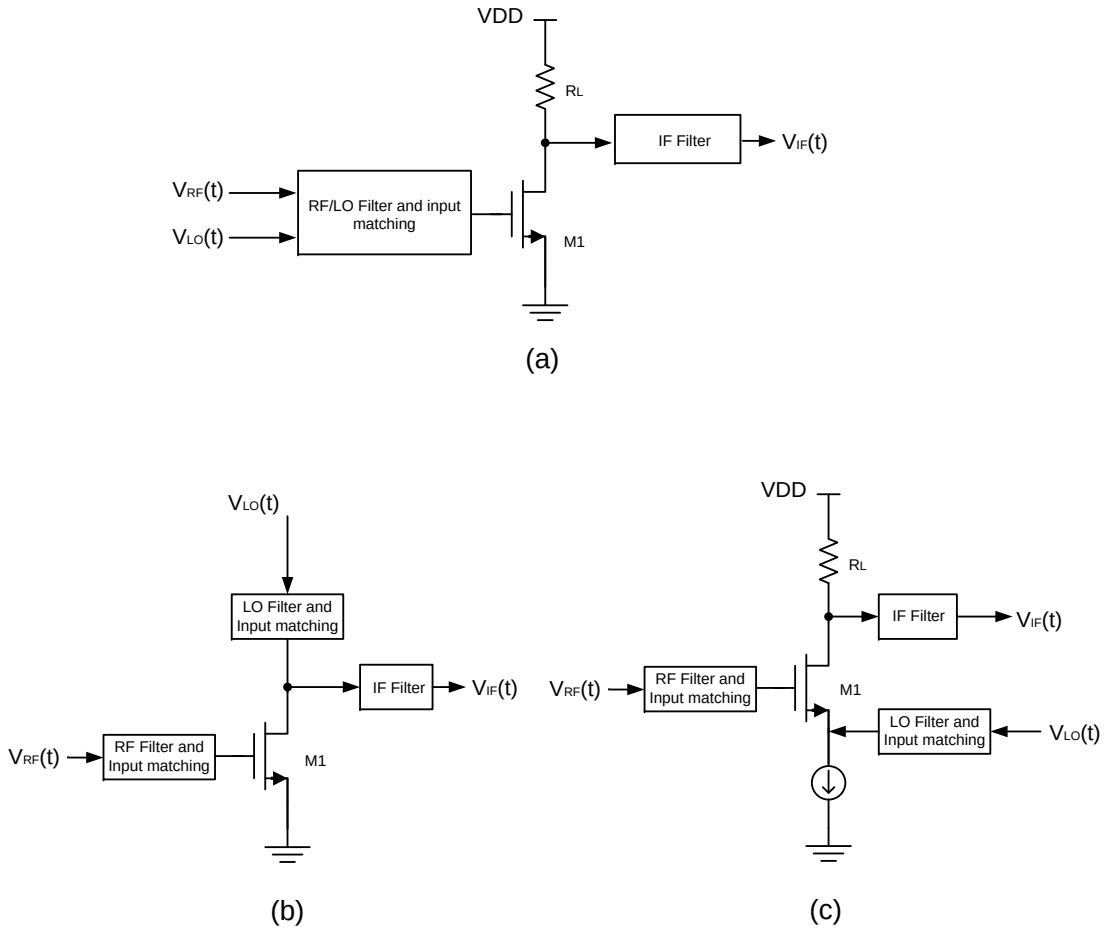

Figure 2.6: The three types of single FET mixers: (a) the gate-pumped single FET mixer; (b) the drain-pumped single FET mixer; (c) the source-pumped single FET mixer

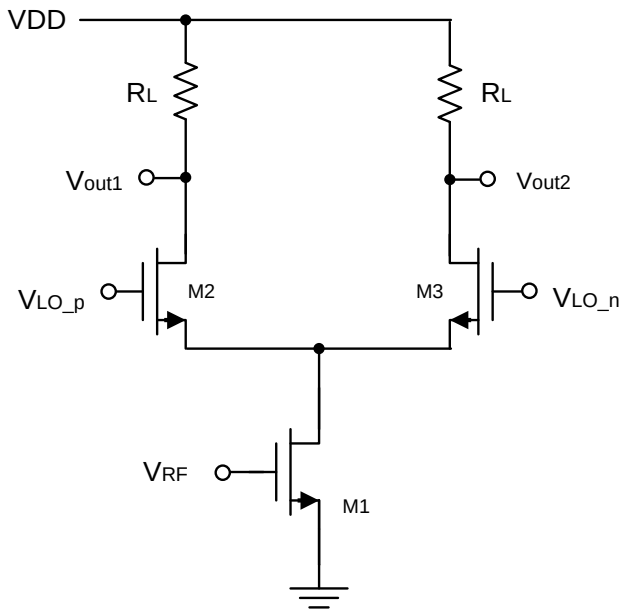

Figure 2.7: The single balanced mixer

Figure 2.6(b) shows the drain-pumped configuration where the LO signal is injected to the drain of the FET. The isolation between RF and LO is limited by the gate-to-drain capacitance C_{gd}. This configuration provides higher LO-to-RF isolation, but the LO-to-IF isolation is usually poor since the LO signal is usually large. Figure 2.6(c) shows the source-pumped configuration where the LO signal is injected into the source of the FET. Since all the three ports, namely LO, IF and RF, are separated, this configuration provides relatively high isolations.

2.3.2 The Single-Balanced Mixer

Figure 2.7 shows the single-balanced mixer. M_1 is the transconductor of the mixer which converts the incoming RF voltage into current. M_2 and M_3 serve as the switching stage of the mixer, and R_L is the resistive load. If the LO signal is large enough, M_2 and M_3 will steer all the current alternatively at the LO frequency. Therefore, the tail current is effectively multiplied by the LO signal. Suppose that the LO drive is a square wave, the output IF current can be written as [5]:

$$i_{IF}(t) = \text{sgn}[cos\omega_{LO}t](I_{DC} + I_{RF}cos\omega_{RF}t) \tag{2.11}$$

$$I_{RF} = -g_m V_{RF} \tag{2.12}$$

where g_m is the transconductance of M_1. The square wave can be expanded into the following series:

$$\text{sgn}[cos\omega_{LO}t] = \frac{4}{\pi}(cos\omega_{LO}t) - \frac{4}{3\pi}cos(3\omega_{LO}t) + \frac{4}{5\pi}cos(5\omega_{LO}t)\cdots \tag{2.13}$$

Substituting the above equation into $i_{IF}(t)$, the second-order intermodulation (IM2) products can be found as:

$$i_{IF}(t)_{IM2} = -\frac{2}{\pi}g_m V_{RF}[cos(\omega_{RF}t - \omega_{LO}t) + cos(\omega_{RF}t + \omega_{LO}t)] \tag{2.14}$$

Thus, the voltage conversion gain (CG) of the mixer is simply:

$$CG = \frac{2}{\pi}g_m R_L \tag{2.15}$$

Compared with the single FET mixers, the single-balanced mixer offers high isolation between the RF and LO port. Although two more transistors are needed, the circuit is still very compact and simple, which makes it suitable for high frequency applications. In [10], a 60-GHz single-balanced mixer was demonstrated in 0.13-μm CMOS technology. It achieved a conversion gain of 12 dB and a noise figure of 18 dB. The mixer consumed 0.9 mA of DC current under a supply voltage of 1.2 V. In [11], the single-balanced mixer built in 0.18-μm CMOS technology achieved a power conversion gain of 13 dB and a noise figure of 17.5 dB at 24 GHz, while consuming 4 mA of DC current with a 1.5 V supply.

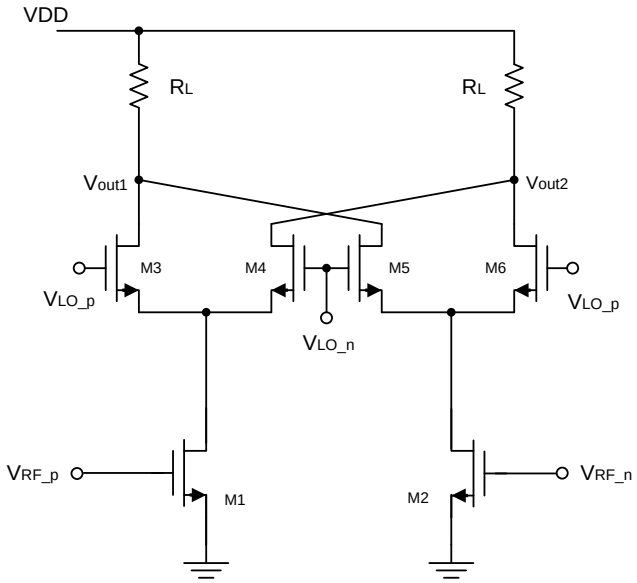

Figure 2.8: The Gilbert cell mixer

The main disadvantage of the single-balanced mixer is that it provides poor LO-to-IF isolation. From Equation 2.13, it is clear that the LO feedthrough at the IF output is $\frac{4}{\pi} I_{DC} R_L cos(\omega_{LO} t)$. Since the LO signal is usually large (e.g. 0 dBm), some filtering is required to avoid overloading the following stages.

2.3.3 The Gilbert Cell Mixer

The most popular active mixer currently in use is the Gilbert cell mixer, as shown in Figure 2.8 [7]. It consists of two single-balanced mixers with cross-coupled outputs in the current domain, and can be easily implemented monolithically using either bipolar or field-effect transistors. Although the power consumption is doubled compared to a single-balanced mixer, the Gilbert cell mixer is capable of providing excellent port-to-port isolations while maintaining reasonable conversion gain and noise performance. Therefore, it is widely used in modern communication systems.

The operation of the Gilbert cell mixer is similar to that of the single-balanced mixer. M_1 and M_2 form the transconductor stage of the mixer and convert the incoming RF signal into current. The upper two pairs of transistors (M_3 and M_4)

are cross-coupled and driven by differential LO signal, forming the switching stage of the mixer. If the LO signal is large enough, the upper two pairs act as current switches and change the polarity of the output current. Therefore, the RF current is multiplied by the LO signal. At the output, the IF signal is taken differentially between V_{out1} and V_{out2}.

The same approach can be taken to analyze the Gilbert cell mixer as in the single-balanced mixer. Suppose that the LO signal is a square wave, the currents in the two output branches can be written as:

$$i_{out1}(t) = \text{sgn}[cos\omega_{LO}t](I_{DC} + I_{RF\_p}cos\omega_{RF}t) \tag{2.16}$$

$$i_{out2}(t) = \text{sgn}[cos\omega_{LO}t](I_{DC} + I_{RF\_n}cos\omega_{RF}t) \tag{2.17}$$

$$I_{RF\_p} = -g_m V_{RF\_p} = -g_m \frac{V_{RF}}{2} \tag{2.18}$$

$$I_{RF\_n} = -g_m V_{RF\_n} = +g_m \frac{-V_{RF}}{2} \tag{2.19}$$

Using Equation 2.13, the IM2 products can be found as:

$$i_{out1}(t)_{IM2} = -\frac{2}{\pi} g_m V_{RF\_p}[cos(\omega_{RF}t - \omega_{LO}t) + cos(\omega_{RF}t + \omega_{LO}t)] \tag{2.20}$$

$$i_{out2}(t)_{IM2} = -\frac{2}{\pi} g_m V_{RF\_n}[cos(\omega_{RF}t - \omega_{LO}t) + cos(\omega_{RF}t + \omega_{LO}t)] \tag{2.21}$$

Subtracting the above two equations gives us:

$$i_{IF}(t)_{IM2} = -\frac{2}{\pi} g_m V_{RF}[cos(\omega_{RF}t - \omega_{LO}t) + cos(\omega_{RF}t + \omega_{LO}t)] \tag{2.22}$$

And the conversion gain (CG) is simply:

$$CG = \frac{2}{\pi} g_m R_L \tag{2.23}$$

which is the same as the single-balanced mixer. However, unlike the single-balanced mixer, the LO signals appear as common mode signals at the IF output and are thus canceled after subtracting. Thus, the Gilbert cell mixer provides excellent LO-to-IF isolation. If the layout is taken carefully, the Gilbert cell mixer often provides over 40 dB of LO-to-IF isolation, with values up to 60 dB possible.

Noise figure of the Gilbert cell mixer. The analysis of noise figure of the Gilbert cell mixer is difficult due to the time variance and frequency translation. In general, there are three important noise sources in a Gilbert cell mixer [12]. The first noise source is the transconductor, which sets the lower bound on the noise figure. The second noise source is the switching pair. Imperfect switching of the switching pairs attenuates the signal current and hence degrades the noise figure. In addition, if the rising edge or falling edge of the LO drive is not sharp enough, there exists a time interval when all of the switching transistors are on and conduct current. During that time interval, the switching pairs also contribute noise. The third noise source is the resistive load (R_L), which contributes noise directly to the IF output. In practice, reactive loads (e.g. an LC tank) can be used to get rid of this noise source.

A number of general methods have been proposed to minimize the noise figure [12]. High bias current can improve the transconductance of the mixer and thus improves the conversion gain and noise figure. A large enough LO drive is also preferred since it helps increase the conversion gain and reduce the noise contribution of the switching pairs. In addition, minimum channel length is often desirable for both the switching transistors and the transconductors as it improves the conversion gain. Upon the usage of the above methods, a practical Gilbert cell mixer still exhibits a SSB noise figure of at least 10 dB.

Linearity of the Gilbert cell mixer. The linearity of the Gilbert cell mixer

is primarily constrained by the transconductor [13]. In addition, the switching pairs affect the linearity if the switching action is imperfect. In order to provide good switching, a large LO drive is usually required. However, although a large LO drive is necessary, an excessive one actually degrades linearity. According to [5], a spike results from the over-drive LO signal through the gate-to-source capacitance (C_{gs}) of switching transistors, which causes the transistors to enter their linear region.

The Gilbert cell mixer has been used for several decades, and has proven to work very well in wireless communication systems thus far [7]. In addition, start of the art designs have shown that it can also provide reasonably high frequency and broadband performance. In [14], the Gilbert cell mixer built in 0.18-μm CMOS technology achieved 11 dB of conversion gain from 0.3 to 25 GHz. The port-to-port isolations were better than 20 dB over the entire frequency range. In [15], a Gilbert cell mixer using 0.13-μm CMOS technology was designed for millimeter-wave (MMW) applications. It worked from 9 to 50 GHz and the conversion gain achieved was better than 5 dB. The LO/RF-to-IF isolation was better than 40 dB, while the LO-to-RF isolation was better than 20 dB.

2.3.4 Folded Mixers

As the CMOS technology scales down, the supply voltage also scales down from one generation to the next. In a conventional Gilbert cell mixer, the switching transistors are usually stacked on top of the transconductors. Furthermore, the load resistor R_L is placed on top of the switching stage. Since the current flows through the transconductor stage, the switching stage and the load stage and introduces voltage drops at all the three stages, it becomes difficult to guarantee that all the transistors work in saturation as the supply voltage drops. Therefore, the traditional Gilbert cell configuration is not suitable for low voltage applications [16].

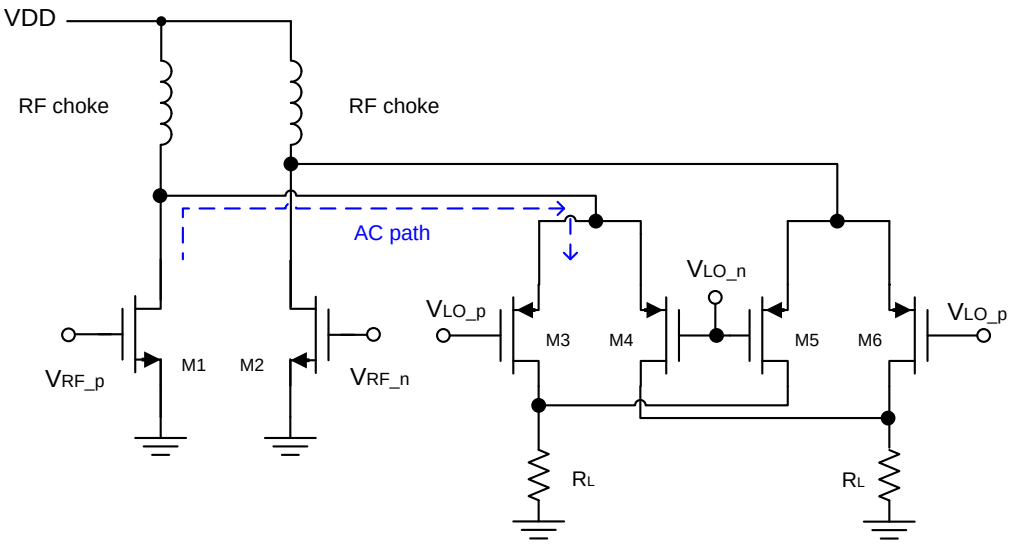

Figure 2.9: The folded Gilbert cell mixer

In order to alleviate the stringent requirements on the supply voltage, a folded configuration can be used. The key idea lies in the concept of decoupling the AC and DC paths of the circuit, as shown in Figure 2.9 [17]. Transistors M_1 and M_2 are the transconductors of the mixer, and transistors M_3-M_6 are the switching transistors of the mixer. The two resistors (R_L) serve as the resistive loads. If the RF chokes are sufficiently large to block all RF frequencies of interest, then the AC path of the folded mixer shown in Figure 2.9 is exactly the same as a conventional Gilbert cell mixer.

With careful design considerations, reasonably high frequency performance can be achieved using folded mixers. In [18], a folded mixer using 0.13-μm CMOS technology was designed for ultra-wideband (UWB) applications. It worked from 3 to 7 GHz and the conversion gain achieved was from 5.3 dB to 8.2 dB. The IIP3 of the mixer was approximately 0 dBm. The power consumption was 5 mW under a supply voltage of 1.2 V. In [19], a folded mixer using 0.18-μm CMOS technology was designed to operate at 2.4 GHz. It achieved 11.9 dB of conversion gain, 14 dB of noise figure and -3 dBm of IIP3, all under a supply voltage of 1 V and a power consumption of 3.2 mW.

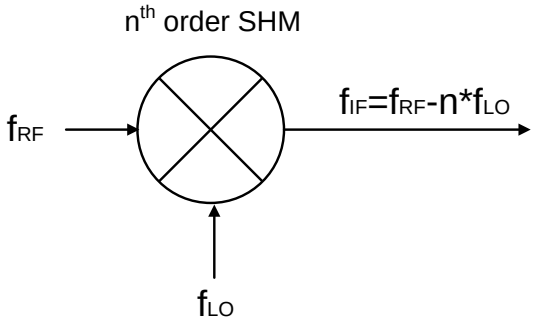

Figure 2.10: The subharmonic mixer concept

2.3.5 Subharmonic Mixers

One of the challenges in the direct-conversion receivers (DCRs) design is the LO self-mixing problem. It results from the LO feedthrough to the RF input, and can cause DC offsets which interfere with the desired signal and degrade the signal-to-noise ratio (SNR) after mixed with the LO itself [20]. In order to alleviate this problem, the subharmonic mixers (SHMs) can be used. In a SHM, the LO frequency is internally multiplied, producing mixing components from the RF frequency and an integer multiple of the LO frequency, as shown in Figure 2.10 [1]. The reduction in LO frequency greatly alleviates the LO self-mixing problem since the frequency of feedthrough from the LO is n times lower than the actual LO frequency for mixing. In addition, it simplifies the LO design and improves the phase noise performance of the LO.

Figure 2.11 shows the 4x subharmonic mixer reported in [1]. It is very similar to a Gilbert cell mixer, except that the two transistors at the bottom have been replaced by two sets of four transistors that will generate the fourth harmonic of the LO signal, thus allowing the mixer to operate as a 4x SHM. The inputs to the transistors are octet-phase LO signals, namely 0°, 90°, 180°, 270° for the first set of four transistors and 45°, 135°, 225°, 315° for the second set of four transistors. The proposed 4x SHM worked with a RF frequency of 12.1 GHz and an LO frequency of 3 GHz, producing an IF frequency of 100 MHz. It obtained 6 dB of conversion gain and -12 dBm of

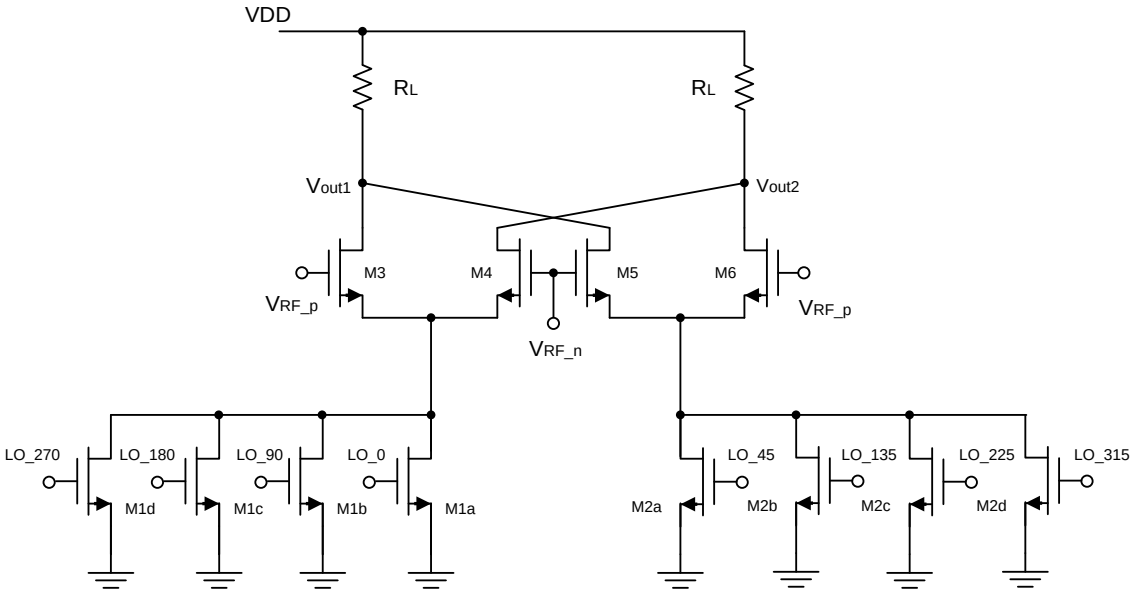

Figure 2.11: The 4x subharmonic mixer proposed in [1]

P1dB. The measured LO-to-RF isolation was 71 dB. The 2LO-to-RF and 4LO-to-RF isolation were 52 and 59 dB respectively.

2.4 Image-rejection Mixers and SSB Mixers

2.4.1 Image-rejection Mixers

The superheterodyne architecture is widely used for receivers in modern communications due to its ability to provide relatively high and stable performance. Despite its popularity, its implementation is not without difficulties. One of the problems that the superheterodyne architecture faces is the image-rejection problem. The image signal can be down-converted to IF along with the desired signal, and hence degrade the signal-to-noise ratio (SNR). Thus, proper filtering is required to remove the image signal, which is usually performed by the off-chip surface-acoustic wave (SAW) filters. However, the off-chip SAW filters are usually large and expensive, which limit the level of integration and increase the cost [21].

To overcome the image problem, image-rejection mixers can be used to alleviate

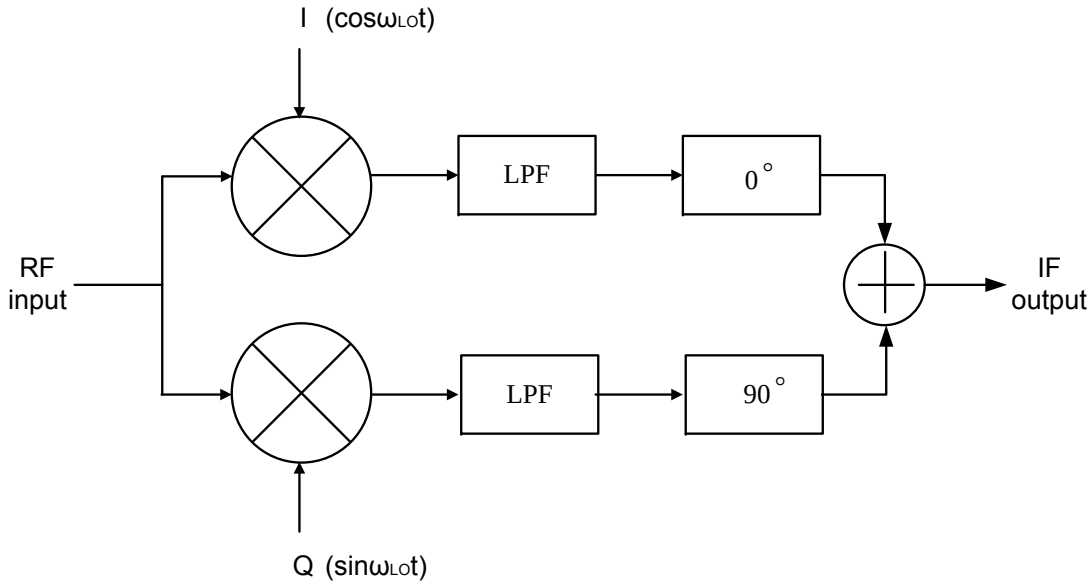

Figure 2.12: The Hartley architecture [2]

the external filtering. The basic idea is that since a signal and its image may be distinguished by their differing phase, cancellation of the image signal while passing the desired RF signal is possible. Thus far, several architectures have been proposed to realize image-rejection mixers, of which the most popular two are the Hartley Architecture and the Weaver Architecture.

The Hartley Architecture

Figure 2.12 shows the Hartley Architecture [2]. It mixes the RF input with the quadrature LO signals and low-pass filters the outputs of the mixers. Before adding the outputs together, it employs a 90° phase shifter to shift one of the outputs of the two low-pass filters. It can be proved that the desired signal is added at the output while the image signal is rejected.

Suppose that the RF input signal consists of the desire RF signal which is $cos(\omega_{RF}t)$ and the image signal which is $cos(\omega_{IM}t)$, and $f_{RF} - f_{LO} = f_{LO} - f_{IM} = f_{IF}$. For the simplicity of analysis, the amplitude of all the signals are assumed to be unity. Therefore, the output of the I mixer will be:

$$\frac{1}{2}[cos(\omega_{RF}t + \omega_{LO}t) + cos(\omega_{RF}t - \omega_{LO}t)] + \frac{1}{2}[cos(\omega_{LO}t + \omega_{IM}t) + cos(\omega_{LO}t - \omega_{IM}t)] \tag{2.24}$$

Similarly, the output of the Q mixer will be:

$$\frac{1}{2}[sin(\omega_{RF}t + \omega_{LO}t) - sin(\omega_{RF}t - \omega_{LO}t)] + \frac{1}{2}[sin(\omega_{LO}t + \omega_{IM}t) + sin(\omega_{LO}t - \omega_{IM}t)] \tag{2.25}$$

The output of the Q mixer then passes through a 90° phase shifter and becomes:

$$\frac{1}{2}[-cos(\omega_{RF}t + \omega_{LO}t) + cos(\omega_{RF}t - \omega_{LO}t)] + \frac{1}{2}[-cos(\omega_{LO}t + \omega_{IM}t) - cos(\omega_{LO}t - \omega_{IM}t)] \tag{2.26}$$

It is clear that by adding Equation 2.24 and Equation 2.26, the IF signals caused by the image (IM) signal at the I and Q paths will cancel each other, and the output is simply $cos(\omega_{RF}t - \omega_{LO}t) = cos(\omega_{IF}t)$.

However, similar to any systems that rely on cancellations, a high image rejection depends on the matching of gain and phase through the receiver chain. In order to quantify the image rejection, a parameter named image-rejection ratio (IRR) is introduced, which is defined as the power ratio of the signal to the image. If the radian phase-matching error ϵ and fractional gain mismatch θ are both small, the IRR may be expressed as [22]:

$$IRR \approx \frac{4}{\epsilon^2 + \theta^2} \tag{2.27}$$

It is difficult to achieve better than 0.1% of gain error and 1° of phase error, which corresponds to an IRR of 41 dB. At high frequencies, the IRR tends to be worse. For example, at 5 GHz, the IRR achieved generally lies in the range of 25-35 dB. However,

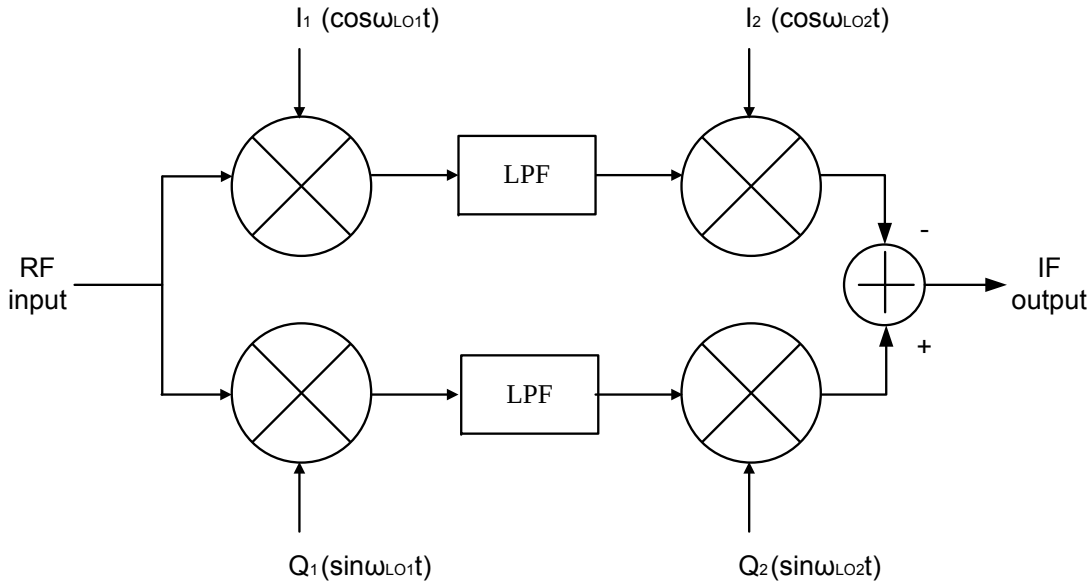

Figure 2.13: The Weaver architecture [3]

the typical IRR requirement of a superheterodyne receiver is as high as 80 dB [21]. Therefore, additional filtering is usually required.

Weaver Architecture

One of the problems of the Hartley architecture is that it is difficult to generate broadband 90° phase shifts, which hinders its applications in broadband receivers. To overcome this problem, the Weaver architecture can be used, as shown in Figure 2.13 [3]. The Weaver architecture performs two consecutive quadrature down-conversion operations on the desired RF signal and the image signal. It can be shown that at the output, the desired signal is added while the image signal is canceled after subtraction. The detailed analysis is very similar to the Hartley architecture and is hence not repeated.

Not surprisingly, the Weaver architecture is also very sensitive to mismatches. But since it does not need a 90° phase shifter which is usually a *RC-CR* network, the IRR achieved is slightly better than the Hartley architecture because on-chip resistors often exhibit large variations up to 20%. However, even so, the IRR is rarely better

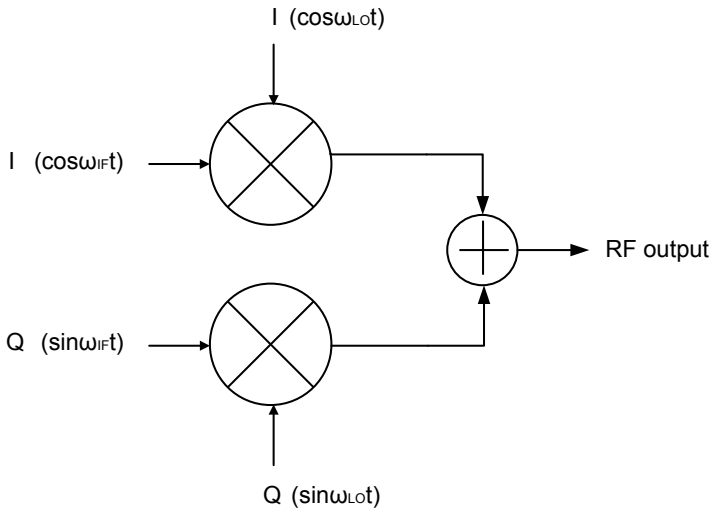

Figure 2.14: The SSB mixer [4]

than 40 dB which still falls short of the requirement of a typical superheterodyne receiver.

2.4.2 Single-sideband (SSB) Mixers

A typical up-conversion mixer produces both the upper sideband (USB) signal and the lower sideband (LSB) signal, which carry the same information. Therefore, it is a waste of power to transmit both the sidebands since power consumption is one of the primary concerns in wireless communications. That is the reason why most modern transmitters employ single-sideband (SSB) up-conversion, which is realized by SSB mixers.

The principle of SSB mixers is very similar to that of the image-rejection mixers. In fact, both the Hartley and Weaver architectures can be used for SSB mixers. The only difference is that in image-rejection mixers, the input frequency is the RF frequency and hence down-conversion is performed; while in SSB mixers, the input frequency is the IF frequency and up-conversion is performed.

Since in most transmitters the baseband provides quadrature outputs, the SSB mixers used in these transmitters can as be shown in Figure 2.14. This topology can

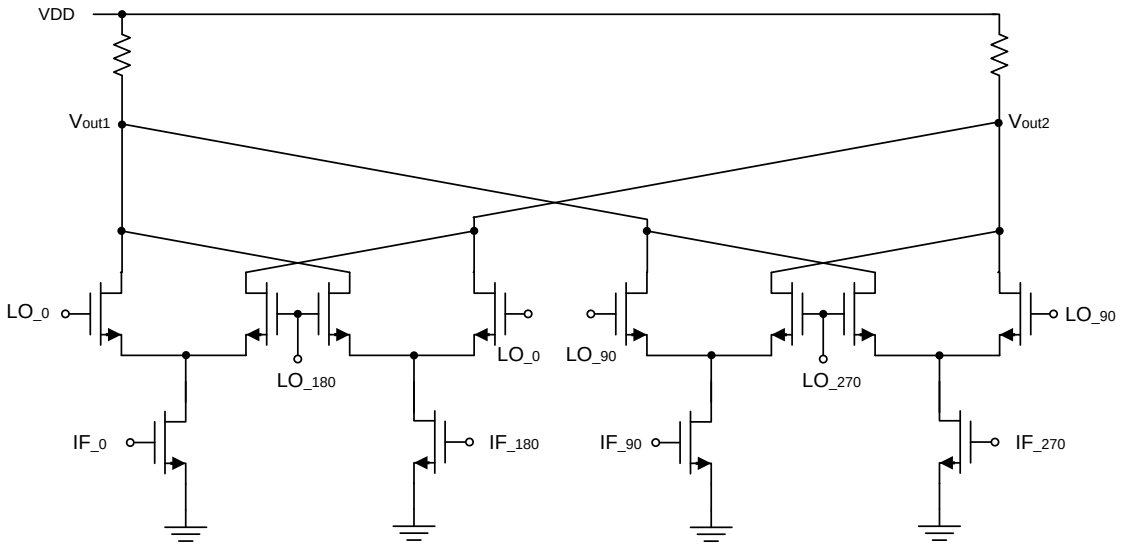

Figure 2.15: The SSB mixer realized by two Gilbert cell mixers [4]

be easily realized by two Gilbert cell mixers with their outputs added in the current domain, as shown in Figure 2.15 [4].

The matching is also very crucial to SSB mixers. Similar to the image-rejection mixers, the mismatches degrade the sideband rejection, which leads to cross-talk between the two data streams modulated on the quadrature phases of the carrier. In practice, a sideband rejection of 30 dB is required to guarantee that the cross talk between the two data streams is negligible [23].

2.5 Conclusion

This chapter gives a general introduction to mixers. It begins with the introduction to the basic mixing concept, followed by the analysis of several mixer topologies. It then gives a brief overview on the image-rejection mixers and the single-sideband (SSB) mixers. The focus of this chapter is the analysis of the Gilbert cell mixer, which is the most widely used mixer topology in modern communications.

Chapter 3

A Mixer with Variable Conversion Gain

3.1 Introduction

A number of broadband receivers and transceivers have been demonstrated in recent years [24] [25] [26] [27] [28]. However, the design of broadband transceivers is still a work in progress. Many open problems remain, and are worthy of intensive research.

One of the major issues that the design of broadband transceivers faces is the need for broadband circuits, including LNAs and mixers. Recently, broadband circuits with bandwidths as high as several tens of GHz have been demonstrated in CMOS technologies. In [29] [30], distributed amplification was used to provide good impedance matching, flat gain over a wide range of frequencies and high IIP3. However, it occupied a large die area due to the need for high quality transmission lines which made it unattractive in a low cost design. In [31] [32], recursive down-conversion mixers with wide bandwidth were demonstrated using multiband feedback and gain-reuse. While they had the advantages of large conversion gains and low DC power consumption, stability and distortion issues needed to be carefully considered. In [33] [34] [35], the resistive shunt feedback technique was used to provide wideband input matching

and low noise figure (with large loop gain). However, they suffered from large power dissipation and stability problems.

Another issue is how to distribute the automatic gain control (AGC) over the receive path of the broadband transceiver. Take the UWB transceiver design for example, a total AGC of around 60 dB is required in the receive path [24]. In [24], the 60 dB AGC was distributed as 16 dB in the LNA, 30 dB at the output of the mixers and 14 dB at baseband. In [28], a total variable gain from 25 dB to 80 dB was implemented, out of which 12 dB was realized by the LNA and the rest was from the baseband VGA.

Finally, to ensure the widest possible usage, especially in portable applications, the power consumption of a broadband transceiver should be kept as small as possible [27]. As the gain of the receive path varies, the power consumption of the broadband transceiver needs to be adjusted accordingly to save power. For example, when the input signal is weak, the transceiver needs a high gain in the receive path to amplify the input signal to achieve an optimal full-scale voltage for the ADC. Thus, the power consumption will be large when the input signal is weak. Contrarily, if the input signal is strong, a small amplification is needed and the corresponding power consumption in this case will be much smaller.

Based on the design considerations above, this chapter introduces a broadband downconverter mixer with variable conversion gain. The proposed broadband mixer worked between 2 GHz and 10 GHz. It was able to work in three different modes with different conversion gains to reduce power consumption. The circuit design was performed in Cadence while the simulations were performed in Agilent ADS. The mixer chip was fabricated using the IBM 0.13-μm CMOS technology.

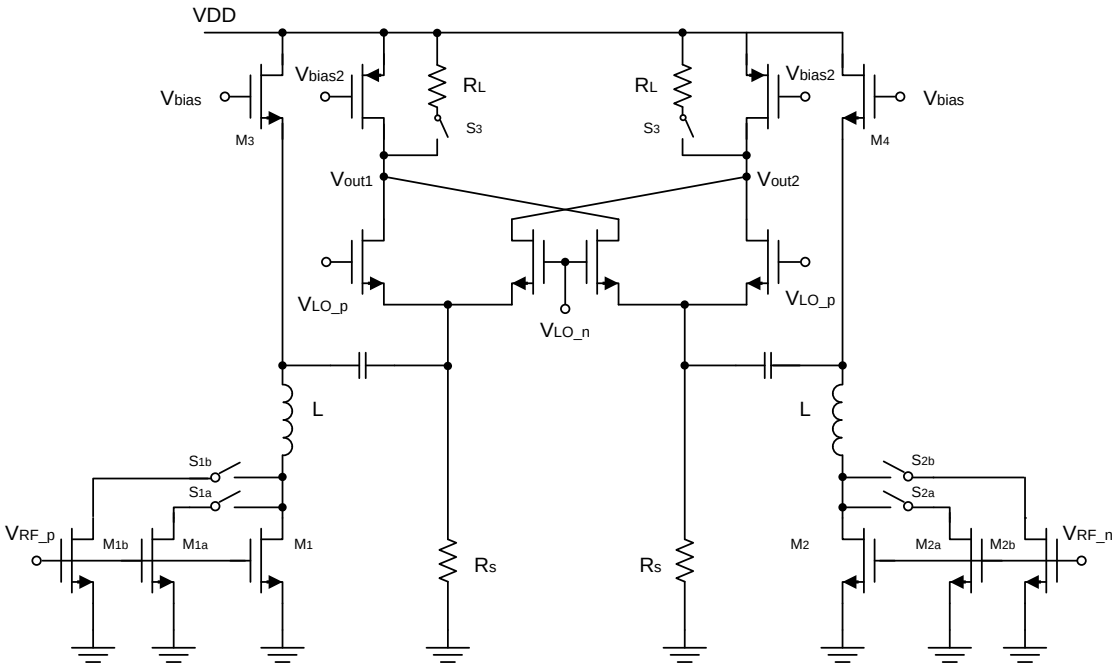

Figure 3.1: The proposed broadband mixer circuit

3.2 Mixer Concept

Figure 3.1 shows the proposed broadband mixer where capacitive coupling is used between the transconductor stage and the LO switches. To cover a wide bandwidth, the mixer employs a bandwidth extension technique known as inductive peaking. As illustrated in Figure 3.1, the inductors are placed between the transconductors and the current sources (M_3 and M_4) to increase the bandwidth of the mixer.

The conversion gain and power consumption of the mixer are controlled by the switches connected to the transconductors and the mixer load. Take the left half of the circuit in Figure 3.1 for example, by turning the switches connected to the transconductors on and off (S_{1a} and S_{1b}), the mixer can work in three different modes with different power consumption, namely mode 1, mode 2 and mode 3. Within each mode, the conversion gain of the mixer can be further controlled by the load switch S_3.

In mode 1, S_{1a} and S_{1b} are both turned on, and the mixer works in the high

Table 3.1: Summary of the Mixer Performance in Different Modes

Mode	Power Consumption	Conversion Gain	Noise Figure	Linearity
1	High	High	Low	Low
2	Moderate	Moderate	Moderate	Moderate
3	Low	Low	High	High

conversion gain mode. By turning on S_3, the conversion gain can be reduced. In this mode, the mixer consumes the largest DC power. The details of the circuit operation will be described in Section 3.3.3.

In mode 2, S_{1a} is off while S_{1b} is on, and the mixer works in the moderate conversion gain mode. Similarly, within this mode, the conversion gain can be reduced by turning on S_3. In this mode, the mixer consumes the moderate DC power.

In mode 3, both S_{1a} and S_{1b} are off, and the mixer works in the low conversion gain mode. Again, by turning on S_3, the conversion gain can be reduced. In this mode, the mixer consumes the lowest DC power.

The performance of the mixer in different modes is summarized in Table 3.1, and the states of the switches in different modes are shown in Table 3.2.

Table 3.2: Summary of Switch States in Different Modes

	Mode 1		**Mode 2**		**Mode 3**	
Conversion Gain	**High**	**Low**	**High**	**Low**	**High**	**Low**
S_{1a}	**On**	**On**	**Off**	**Off**	**Off**	**Off**
S_{1b}	**On**	**On**	**On**	**On**	**Off**	**Off**
S_3	**Off**	**On**	**Off**	**On**	**Off**	**On**

3.3 Circuit Implementation

In this section, the design of the proposed broadband mixer in 0.13-μm CMOS technology will be described in detail, including the mixer topology, the bandwidth extension technique and the conversion gain control technique.

3.3.1 Mixer Topology

The basic mixer topology used in this design is shown in Figure 3.2. It utilizes capacitive coupling between the transconductor and the switching stage. Compared with traditional stacked current-commutating mixers, one of the advantages of this topology is the relatively high LO-to-RF isolation [36]. This is important especially in direct conversion receivers where the LO leakage to the RF port may cause DC offsets at the IF output and thus degrade the SNR [28].

Another advantage is that this topology allows the separate bias of the transconductor and the LO switching stage. On one hand, it is well known that in order to meet the gain and dynamic range requirements, the transconductor stage usually needs a large DC current to provide high gain while suppressing the thermal noise [31] [12]. On the other hand, the LO switching stage requires a relatively small DC current to achieve a high switch speed and low 1/f noise [37] [38] [39]. Since the DC current requirements of the two stages do not coincide, a separate bias for each stage is preferred. And by choosing the DC current of the switching stage much smaller than that of the transconductor stage, the total bias current can be made similar to that of a conventional stacked current-commutating mixer.

As shown in Figure 3.2, the transconductor stage and the LO switching stage of the proposed mixer are biased by I_1 and I_2 respectively. In this design, I_2 was set to be smaller than 10% of I_1 in all the three different modes. Therefore, the power consumption of the mixer is mainly determined by the transconductor stage.

3.3.2 Bandwidth Extension Technique

In order to analyze the bandwidth of the proposed mixer topology, we first draw the small signal model of the transconductor stage which is illustrated in Figure 3.3, where C and R represent the total capacitance and resistance seen at the drain of transistor M_1 respectively. For the simplicity of analysis, we ignore C_{gs} and C_{gd}. The

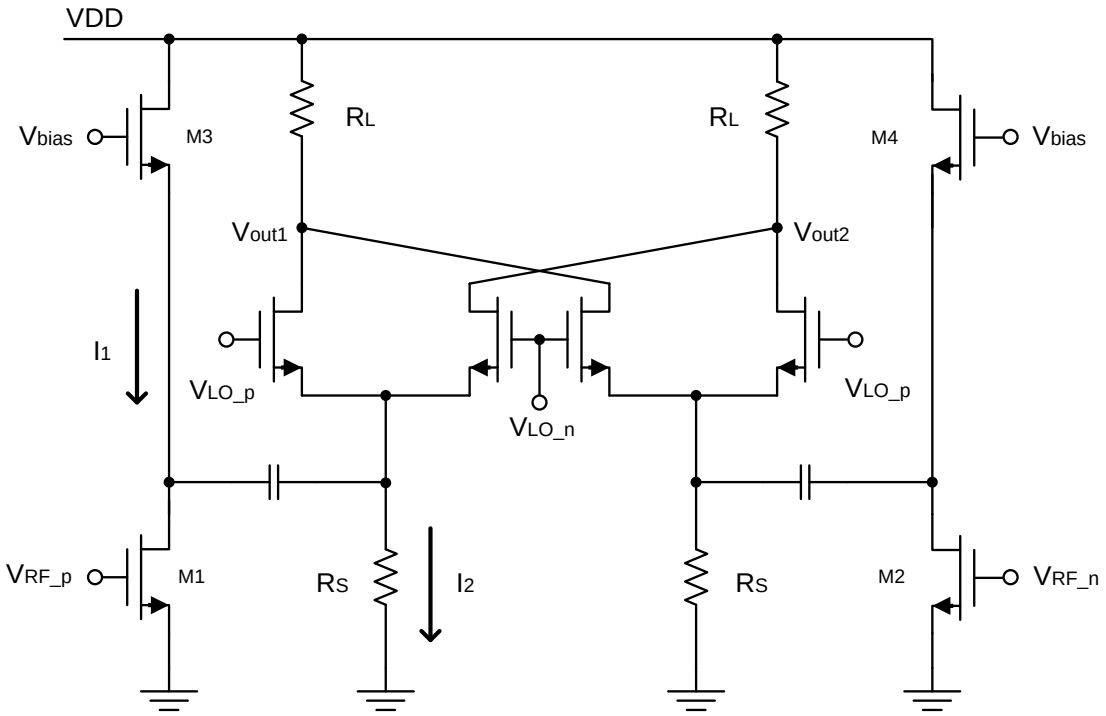

Figure 3.2: The basic mixer topology used in this design

transfer function from V_{in} to V_{out} can be written as:

$$Av_1 = \frac{V_{out}}{V_{in}} = -g_{m1}\frac{R\dfrac{1}{j\omega C}}{R + \dfrac{1}{j\omega C}} \tag{3.1}$$

$$= -g_{m1}\frac{R}{1 + j\omega RC} \tag{3.2}$$

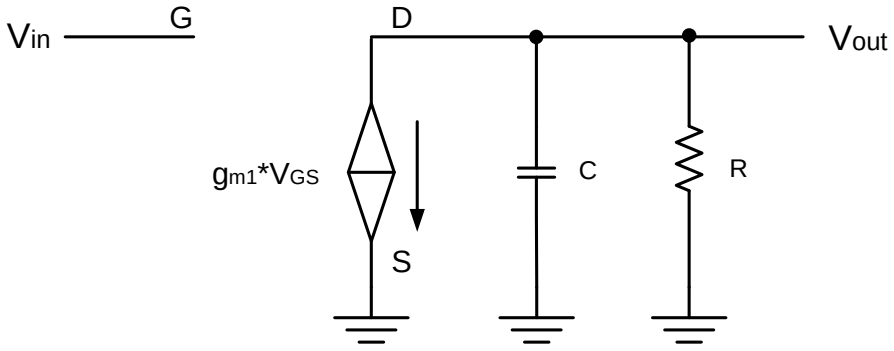

Figure 3.3: Small signal model of the transconductor stage

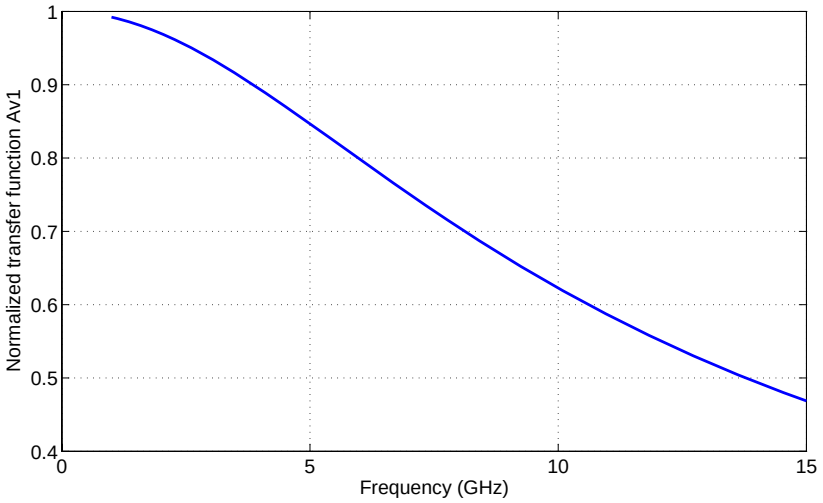

Figure 3.4: The normalized frequency response of the transfer function Av_1

where g_{m1} represents the transconductance of M_1. For R=100 Ω and C=0.2 pF, the normalized frequency response of the transfer function Av_1 is shown in Figure 3.4. It is clear that the transfer function drops quickly at high frequencies and the 3-dB bandwidth is approximately 8 GHz. Furthermore, this result is too optimistic since we ignore various intrinsic capacitances in the above analysis. Thus, for broadband applications such as UWB where the spectrum spans from 3.1 GHz to 10.6 GHz, bandwidth extension techniques need to be used.

In this design, a modified shunt peaking technique was used where the peaking inductor was placed at the drain of the transconductor instead of in series with the load, as shown in Figure 3.5. Again, we draw the small signal model of the mixer with shunt peaking in Figure 3.6. The transfer function from V_{in} to V_{outa} can be written as:

$$Av_2' = \frac{V_{outa}}{V_{in}} = -g_m(\frac{1}{j\omega C}//(j\omega L + R)) \tag{3.3}$$

$$= -g_m \frac{j\omega L + R}{1 + j\omega C(j\omega L + R)} \tag{3.4}$$

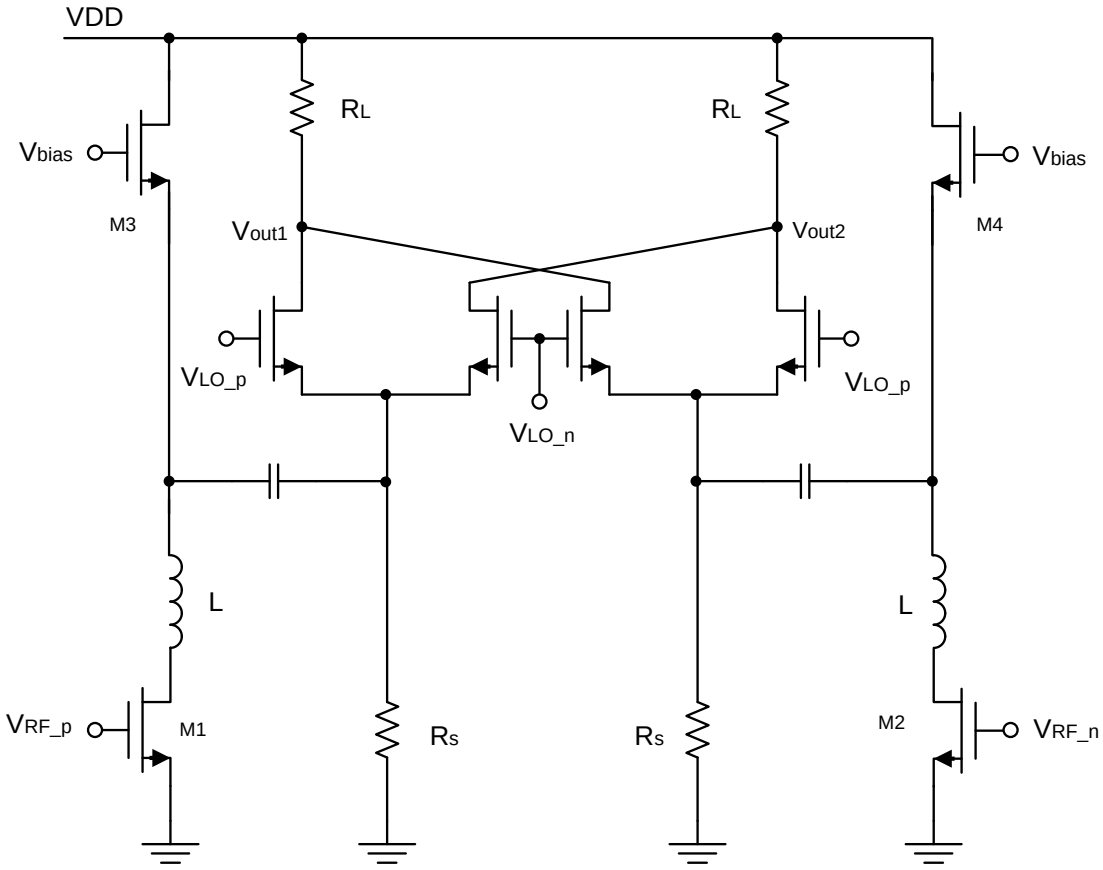

Figure 3.5: The mixer with modified shunt peaking technique

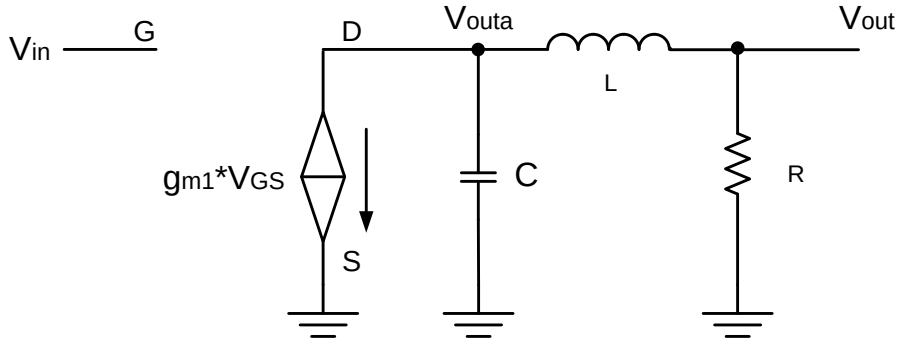

Figure 3.6: The small signal model of the mixer with modified shunt peaking technique

Then the transfer function from the V_{in} to the output V_{out} can be calculated as:

$$Av_2 = Av_2' \frac{R}{R + j\omega L} \tag{3.5}$$

$$= -g_m \frac{R}{1 + j\omega CR - \omega^2 CL} \tag{3.6}$$

Thus, the equivalent impedance of the RLC network can be written as:

$$Z(s) = \frac{R}{1 + j\omega CR - \omega^2 CL} \tag{3.7}$$

Similar to the analysis of the traditional shunt peaking technique [5], we introduce a factor m which is defined as the ratio of the RC and L/R time constants:

$$m = \frac{RC}{L/R} \tag{3.8}$$

Then we can rewrite the impedance of the RLC network as:

$$Z(s) = \frac{R}{s^2\tau^2 m + s\tau m + 1} \tag{3.9}$$

where $\tau = L/R$. The magnitude of the impedance is then normalized to the DC value (=R) as a function of frequency:

$$\frac{|Z(j\omega)|}{R} = \sqrt{\frac{1}{(1 - \omega^2\tau^2 m)^2 + (\omega\tau m)^2}} \tag{3.10}$$

We then continue to calculate the bandwidth extension of the proposed shunt peaking technique. The 3-dB bandwidth of the mixer without shunt peaking is simply:

$$\omega_0 = \frac{1}{RC} = \frac{1}{m\tau} \tag{3.11}$$

The 3-dB bandwidth of the mixer with modified shunt peaking is calculated by setting the normalized magnitude of impedance to $1/\sqrt{2}$:

$$\frac{|Z(j\omega)|}{R} = \sqrt{\frac{1}{(1-\omega^2\tau^2 m)^2 + (\omega\tau m)^2}} = \frac{1}{\sqrt{2}} \tag{3.12}$$

Solving the above equation for ω gives us:

$$\omega = \sqrt{\frac{-(m^2-2m) + \sqrt{(m^2-2m)^2 + 4m^2}}{2\tau^2 m^2}} \tag{3.13}$$

We then define a normalized 3-dB bandwidth extension which is calculated as the ratio of the compensated 3-dB bandwidth of the mixer to the uncompensated one:

$$\frac{\omega}{\omega_0} = \frac{\sqrt{\dfrac{-(m^2-2m) + \sqrt{(m^2-2m)^2 + 4m^2}}{2\tau^2 m^2}}}{\dfrac{1}{m\tau}} \tag{3.14}$$

$$= \sqrt{(-\frac{m^2}{2} + m) + \sqrt{(-\frac{m^2}{2} + m)^2 + m^2}} \tag{3.15}$$

The above result is very similar to that of the traditional shunt peaking technique. Figure 3.7 shows the normalized 3-dB bandwidth extension of the modified shunt peaking technique as a function of m. It is clear that a bandwidth extension of more than 40% can be achieved by setting m to 2.

In order to verify the bandwidth extension, we use the same parameters as in the 3-dB bandwidth calculation of the uncompensated mixer where $R = 100\ \Omega$ and $C = 0.2$ pF. Based on the definition of m, we can calculate the required inductance L that yields the most bandwidth extension:

$$L = \frac{R^2 C}{m} \approx 1\ nH \tag{3.16}$$

The transfer functions Av_1 and Av_2, which represent the transfer function of the uncompensated mixer and the compensated mixer respectively, are plotted in Figure 3.8. It is clear that after compensation, the 3-dB bandwidth of the mixer

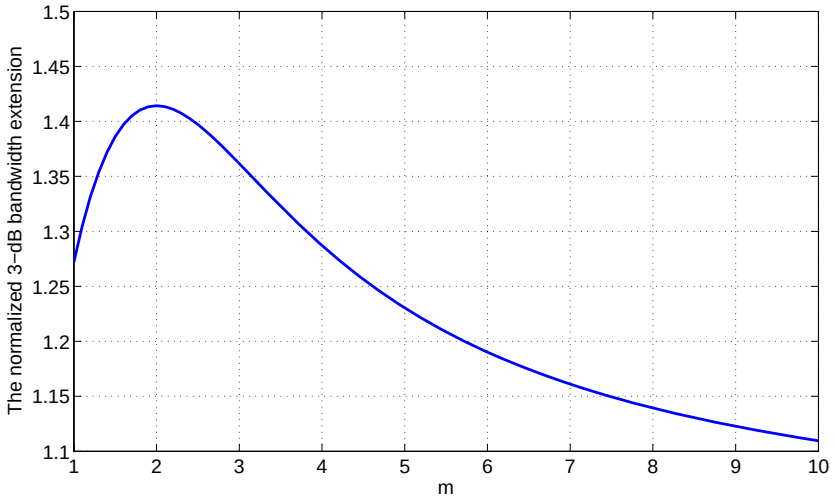

Figure 3.7: The normalized 3-dB bandwidth extension of the modified shunt peaking technique as a function of m

increases from 8 GHz to 11.3 GHz, yielding a bandwidth extension of 41%. Unlike the traditional shunt peaking technique where there is a 20% of peak (also known as ripple) in the frequency response when the bandwidth extension is maximized, the modified shunt peaking technique has a frequency response completely free of ripple.

3.3.3 Conversion Gain Control Technique

There are a number of techniques for controlling the gain of an amplifier or a mixer, including variable feedback, bias control, current steering, attenuation switching and transistor size switching.

Figure 3.9 (a) shows the variable feedback technique, where the gain is controlled by altering the feedback resistance which can be implemented as an NMOS transistor. While this technique provides a potentially high IIP3, its disadvantages are possible stability problems and a limited gain control range [40].

Figure 3.9 (b) shows the bias control technique which incorporates a variable bias network to control the bias current of the transconductor. The main advantage of this technique is the low noise figure. However, since the linearity of the amplifier or

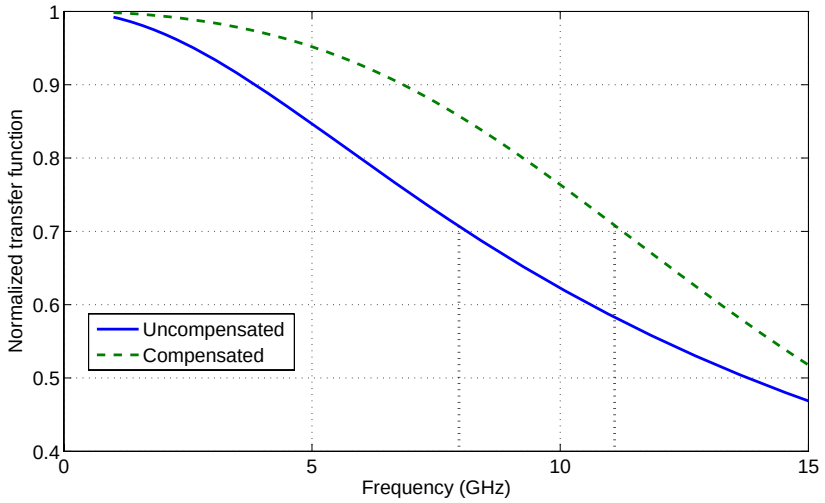

Figure 3.8: The transfer function Av_1 (uncompensated) and Av_2 (compensated)

mixer is highly dependent on the bias condition, the bias control technique needs to be carefully considered before implementation [41].

Figure 3.9 (c) shows the current steering technique where an additional transistor is used to steer current to or from the load [42] [43]. This technique has a high gain control range, but often suffers from high noise and low power efficiency.

Figure 3.9 (d) shows the transistor size switching technique. The transconductor stage consists of a number of NMOS transistors in parallel. The gain tuning is performed by switching on and off the transistors. The basic idea is to change the overall transconductance of the transconductor ($g_{m,tot}$) by changing the effective transistor size. This technique has the advantage of having a large tuning range and high power efficiency since the power consumption decreases as the gain decreases. However, since the transistors which are turned off can still contribute noise, this approach suffers from relatively high noise figure [44].

In this design, the transistor size switching technique was used to control the conversion gain of the mixer. As is shown in Figure 3.1, the transconductor stage of the mixer consists of three NMOS transistors in parallel. In the following analysis, we will take the left half of the mixer for example. The transistors M_{1a} and M_{1b} are

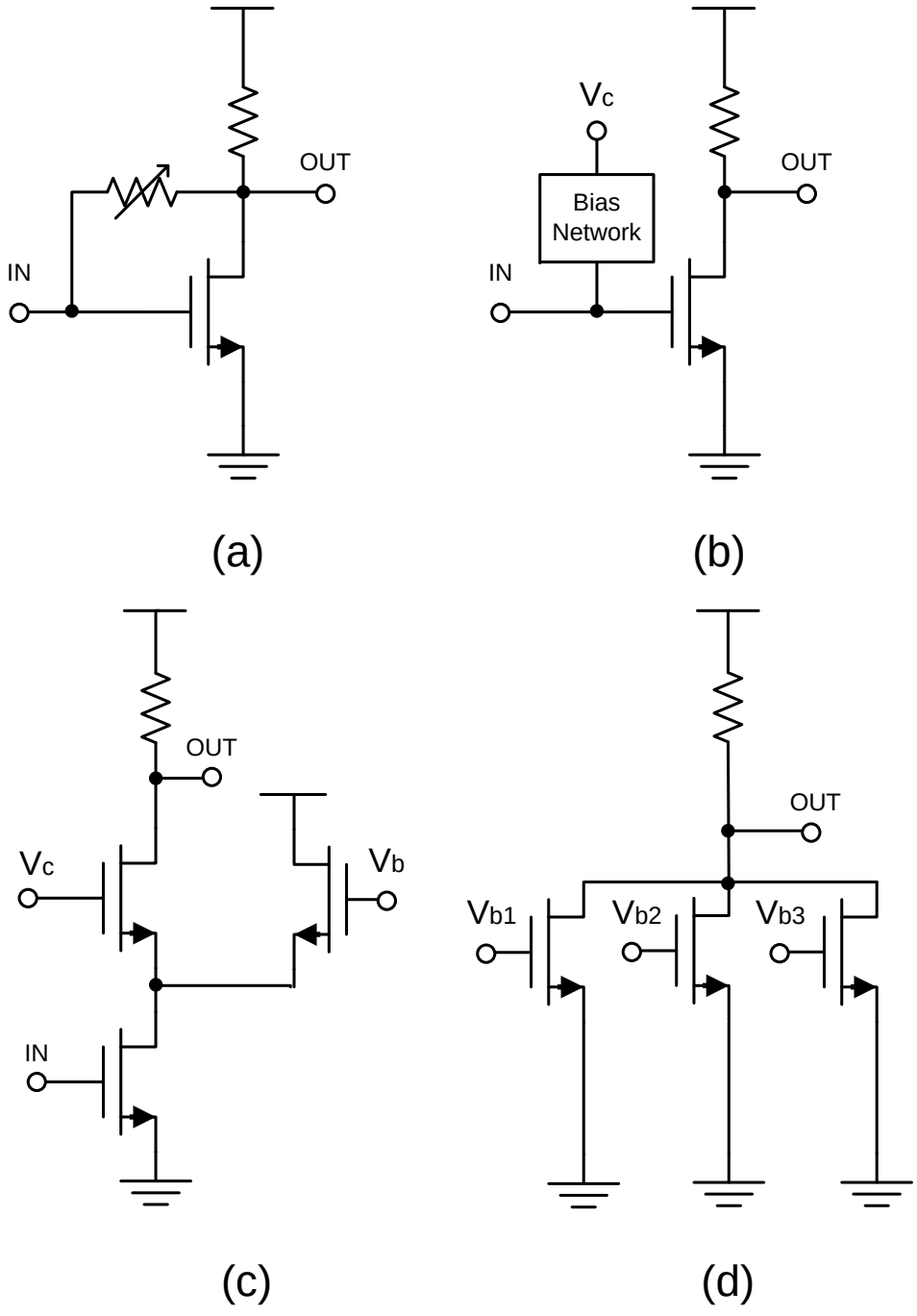

Figure 3.9: Gain control techniques: (a) variable feedback; (b) bias control; (c) current steering; (d) transistor size switching.

connected to two switches S_{1a} and S_{1b}, while transistor M_1 is not connected to any switch and hence is always on. By turning the switches S_{1a} and S_{1b} on and off, the mixer can work at three different modes with different DC power consumption.

In mode 1, S_{1a} and S_{1b} are both turned on. The total transconductance of the transconductor stage of the mixer ($g_{m,tot}$) can be written as:

$$g_{m,tot} = g_{m1} + g_{m,1a} + g_{m,1b} \tag{3.17}$$

where $g_{m,1a}$ and $g_{m,1b}$ are the transconductance of M_{1a} and M_{1b} respectively. It is clear that in Mode 1, the transconductor stage of the mixer has the largest transconductance, and hence the highest conversion gain and DC power consumption.

In mode 2, S_{1a} is off while S_{1b} is on and $g_{m,tot}$ can be written as:

$$g_{m,tot} = g_{m1} + g_{m,1b} \tag{3.18}$$

Thus, in this mode, the mixer has a lower conversion gain as well as DC power consumption than in Mode 1.

In mode 3, both S_{1a} and S_{1b} are off and $g_{m,tot}$ can be written as:

$$g_{m,tot} = g_{m1} \tag{3.19}$$

Therefore, in this mode, the mixer has the lowest conversion gain and DC power consumption.

As illustrated in Figure 3.1, the load of the mixer includes a PMOS transistor as an active load and a resistor R_L controlled by the switch S_3. When S_3 is off, the load of the mixer only consists of the PMOS active load which is usually in the kΩ range while introducing only a small DC voltage drop. The conversion gain (CG) of the mixer can be written as in Equation 3.20, where r_o is the output resistance of the active load. And when S_3 is on, the load impedance decreases with R_L in parallel

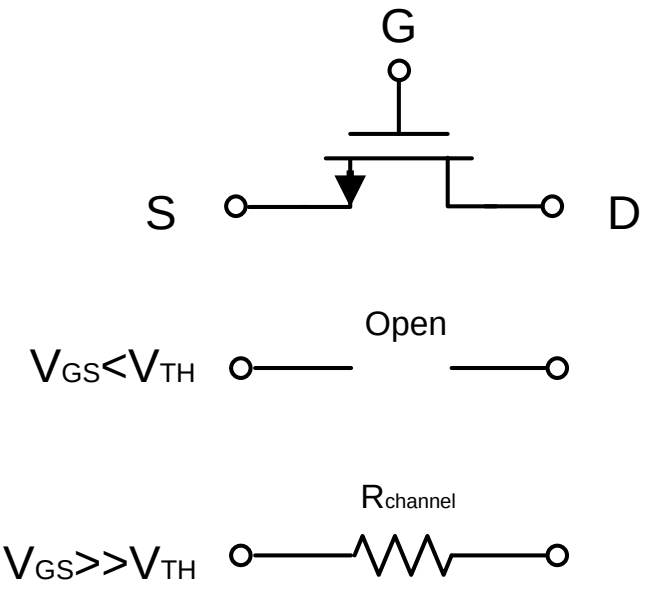

Figure 3.10: NMOS switch model

with the PMOS active load. The CG of the mixer can be written as in Equation Equation 3.21. Thus, by turning the switch S_3 on and off, the conversion gain of the mixer can be further controlled within each mode.

$$\mathrm{CG} = g_{m,tot} \times r_o \tag{3.20}$$

$$\mathrm{CG} = g_{m,tot} \times (r_o // R_L) \tag{3.21}$$

The switches in this design are implemented by NMOS transistors. Figure 3.10 shows the operation of NMOS switches [45]. It is clear that when the NMOS switch is $'$on$'$, a channel resistance $R_{channel}$ connects the drain and source of the transistor. This resistance will introduce loss to the signal and should be kept as small as possible. Since the drain-to-source voltage (V_{DS}) is small, the channel resistance in the short-channel model can be simplified as [45]:

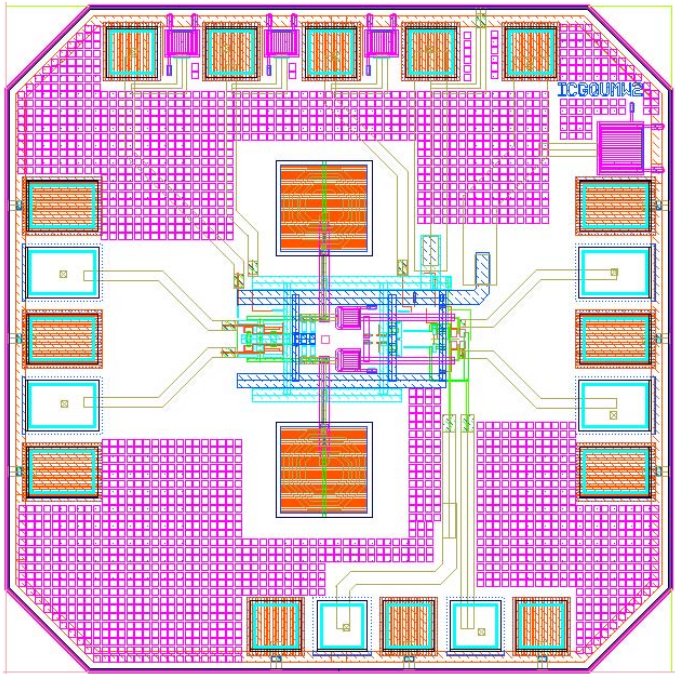

Figure 3.11: The layout of the chip in Virtuoso

$$R_{channel} \approx \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})} \tag{3.22}$$

According to the above equation, we need to increase the transistor width W to decrease $R_{channel}$. In this design, a large transistor width of 80 μm was used to minimize the channel resistance of the switches.

3.4 Measurement Results

The layout of the chip in Cadence Virtuoso is shown in Figure 3.11. The mixer was fabricated using IBM 0.13-μm CMOS technology, which has 8 metal levels including 3 thin metal layers, 2 thick metal layers and 3 RF metal layers. The mixer occupied a die area of 0.35 mm $\times$ 0.54 mm without bonding pads and 1 mm $\times$ 1 mm with bonding pads. The voltage supply used for testing was 1.2 V. Figure 3.12 shows the photograph of the fabricated mixer chip.

A direct on-wafer measurement was performed using Cascade Microtech coplanar

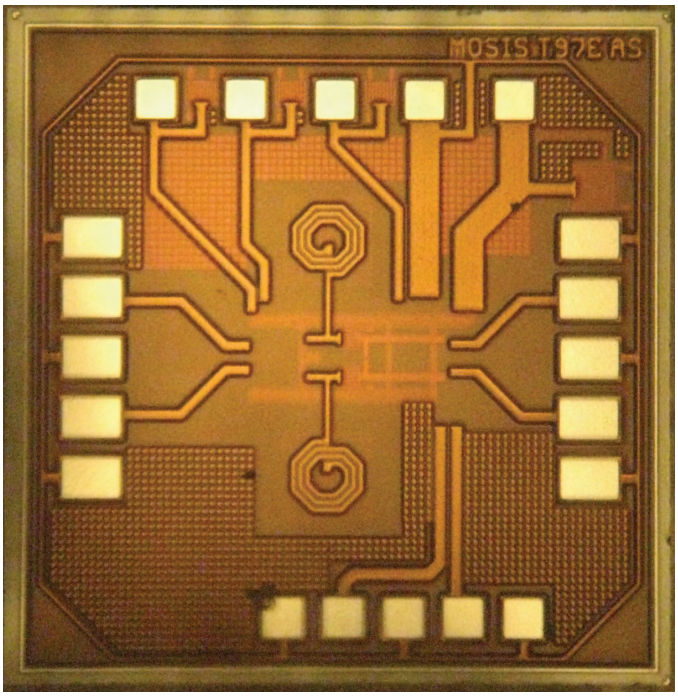

Figure 3.12: Photograph of the fabricated chip

waveguide (CPW) probes and DC probes on a probe station. The RF and LO signals were generated by two Anritsu MG3694 signal generators. An Agilent E4446A spectrum analyzer was used to examine the spectrum of the output signal.

Since all three ports (RF, LO and IF) of the mixer are fully differential, three GSGSG CPW probes with pitch size of 100 μm were used. In order to generate fully differential RF signals, an external 180° hybrid was used to convert the single input signal into differential signals. To generate differential LO signals, a power splitter was first used to split the LO input signal into two in-phase branches, followed by two identical phase shifters to generate a 180° phase difference. The IF frequency was chosen to be 200 MHz. At the IF output, an output buffer was used to convert the differential output signals into a single output signal.

Mode 1. Figure 3.13 shows the measured conversion gain of the mixer in Mode 1. It is clear that from 2 to 10 GHz, the measured conversion gain was around 24 dB and was relatively flat over the entire bandwidth. By turning on S_3, the conversion gain could be reduced by around 3.5 dB.

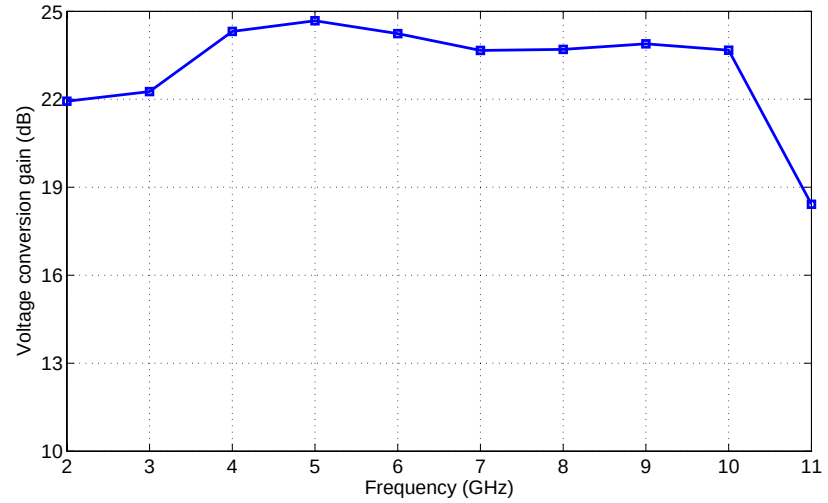

Figure 3.13: The measured conversion gain of the mixer in Mode 1

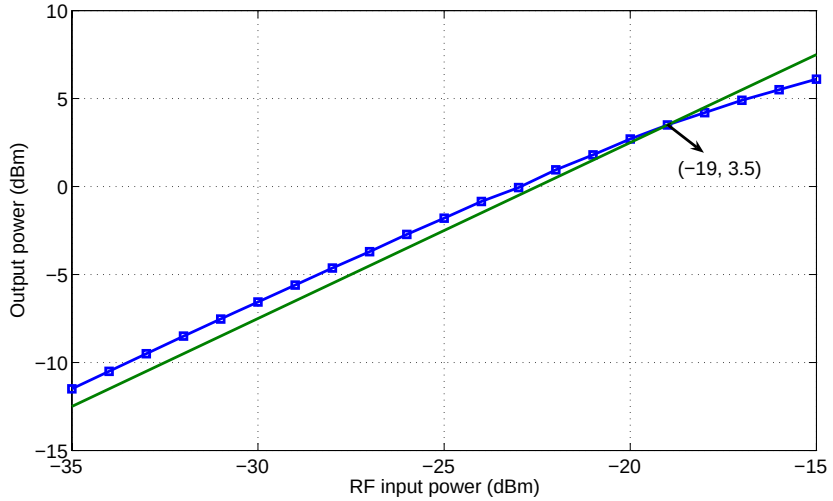

Figure 3.14: The measured P1dB of the mixer in Mode 1 at 7 GHz

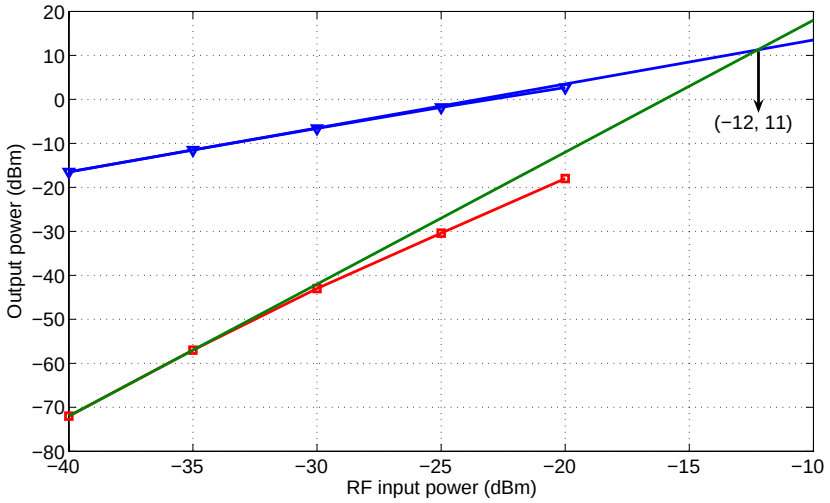

Figure 3.15: The measured IP3 of the mixer in Mode 1 at 7 GHz

The P1dB, IIP3 and noise figure of the mixer were measured at 7 GHz when S_3 was off. In order to test the IIP3 of the mixer, a two-tone test was performed. The two RF input frequencies were set to 7000.5 MHz and 6999.5 MHz. Figure 3.14 shows the measured P1dB of the mixer. As we can see, the P1dB of the mixer was -19 dBm and the corresponding output P1dB was 3.5 dBm. From Figure 3.15, we can see that the measured IIP3 of the mixer was -12 dBm and the corresponding OIP3 was around 11 dBm. Measurement result showed a double-sideband noise figure of 8 dB at 7 GHz.

In Mode 1, the mixer consumed a DC current of 15 mA under a 1.2 V supply.

Mode 2. The measured conversion gain of the mixer in Mode 2 is shown in Figure 3.16. From 2 to 10 GHz, the measured conversion gain was around 17 dB and was relatively flat over the entire bandwidth. By turning on S_3, the conversion gain could be reduced by approximately 3 dB.

The P1dB, IIP3 and noise figure of the mixer were measured at 7 GHz when S_3 was off. Figure 3.17 shows the measured P1dB of the mixer. As we can see, the P1dB of the mixer was -11.5 dBm and the corresponding output P1dB was around 3.5 dBm. From Figure 3.18, we can see that the measured IIP3 of the mixer was -3.5

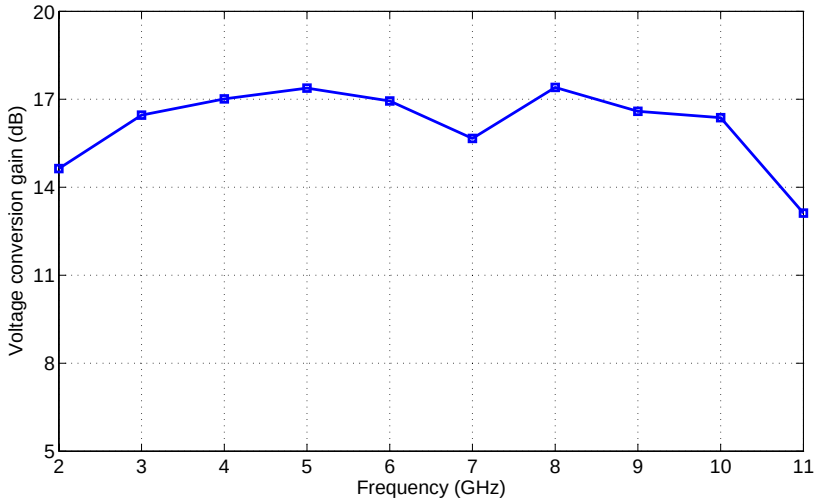

Figure 3.16: The measured conversion gain of the mixer in Mode 2

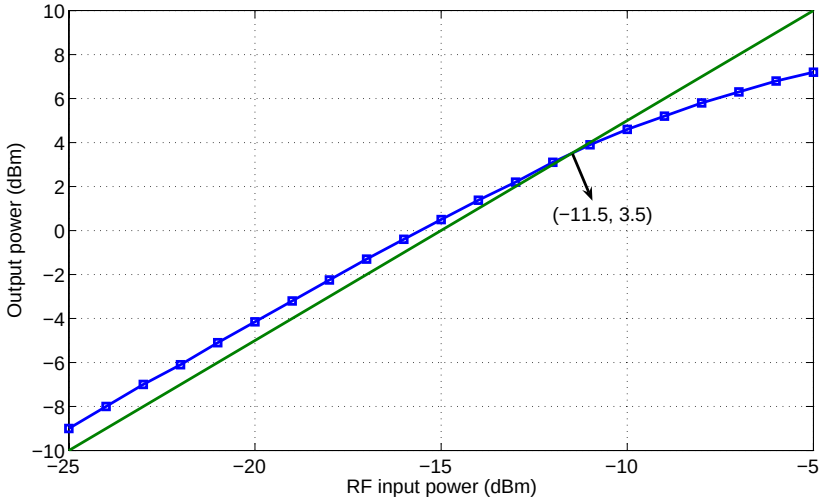

Figure 3.17: The measured P1dB of the mixer in Mode 2 at 7 GHz

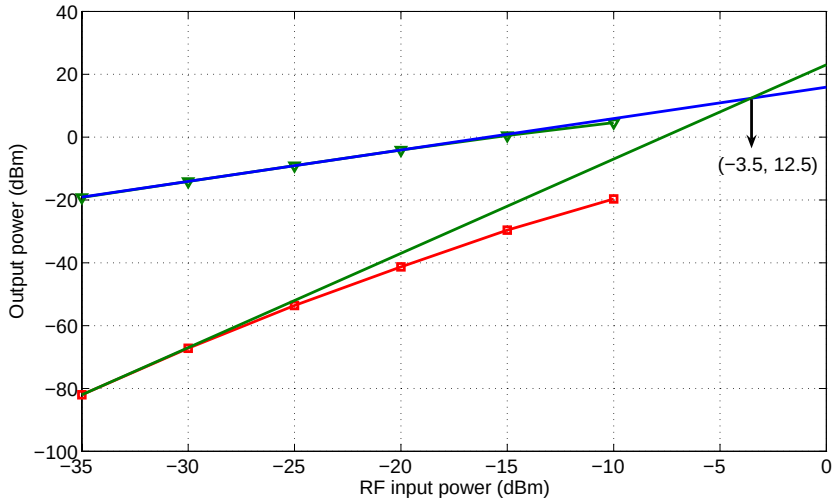

Figure 3.18: The measured IP3 of the mixer in Mode 2 at 7 GHz

dBm and the corresponding OIP3 was around 12.5 dBm. Measurement result showed a double-sideband noise figure of 16 dB at 7 GHz.

In Mode 2, the mixer consumed a DC current of 10 mA under a 1.2 V supply.

Mode 3. The measured conversion gain of the mixer in Mode 3 is shown in Figure 3.19. From 2 to 10 GHz, the measured conversion gain was around 9 dB and was relatively flat over the entire bandwidth. By turning on S_3, the conversion gain could be reduced by around 4 dB.

The P1dB, IIP3 and noise figure of the mixer were measured at 7 GHz when S_3 was off. Figure 3.20 shows the measured P1dB of the mixer. As we can see, the P1dB of the mixer was -4 dBm and the corresponding output P1dB was 3 dBm. From Figure 3.21, we can see that the measured IIP3 of the mixer was 3.5 dBm and the corresponding OIP3 was around 11.5 dBm. Measurement result showed a double-sideband noise figure of 23 dB at 7 GHz.

In Mode 3, the mixer consumed a DC current of 2 mA under a 1.2 V supply.

The port-to-port isolations of the mixer were measured in Mode 1 and the results were shown in Figure 3.22. The LO-to-IF isolation was better than 40 dB from 2 to 11 GHz, while the LO-to-RF and RF-to-IF were better than 60 dB.

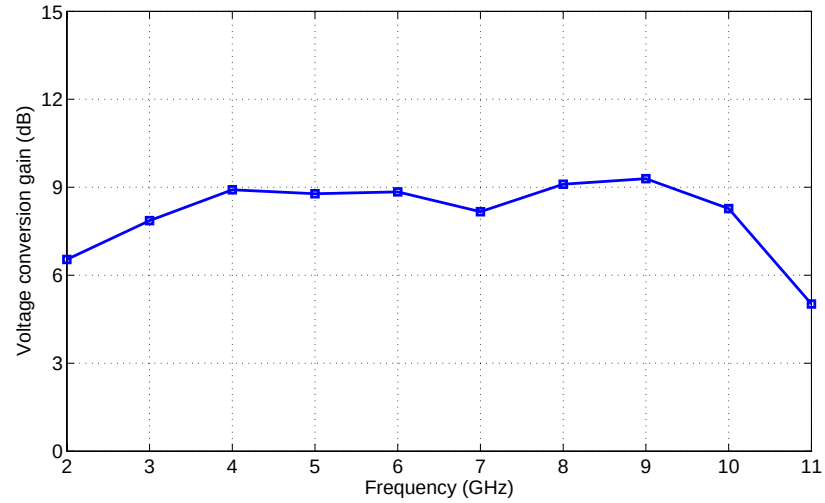

Figure 3.19: The measured conversion gain of the mixer in Mode 3

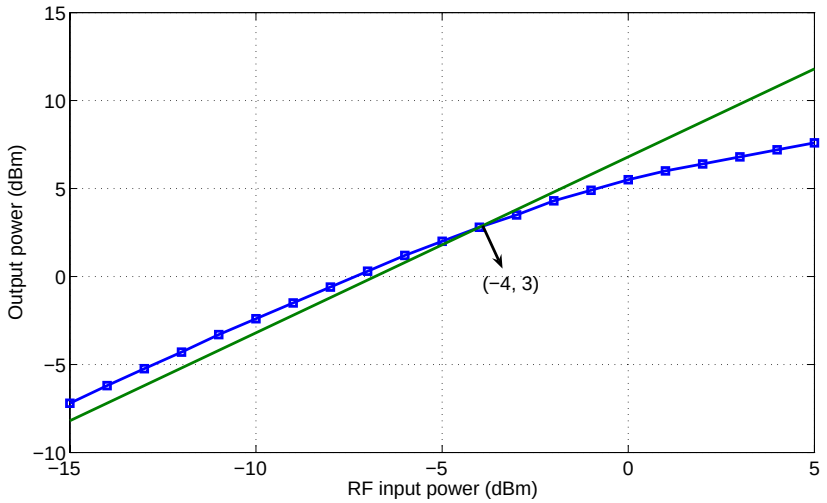

Figure 3.20: The measured P1dB of the mixer in Mode 3 at 7 GHz

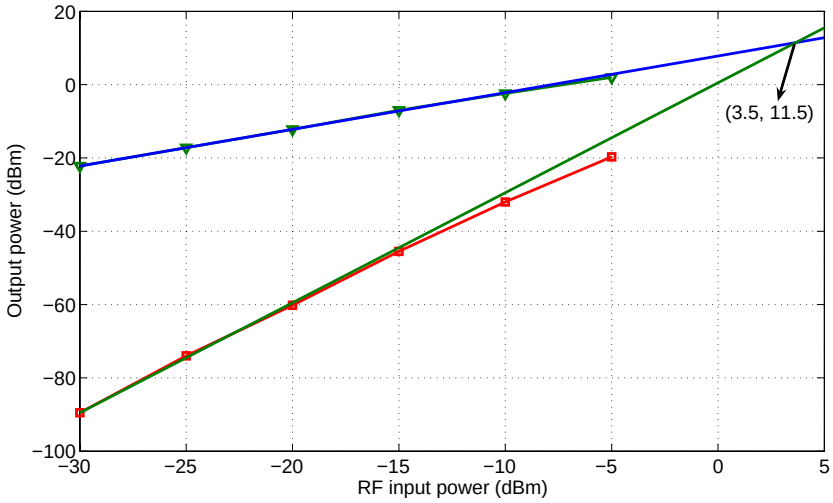

Figure 3.21: The measured IP3 of the mixer in Mode 3 at 7 GHz

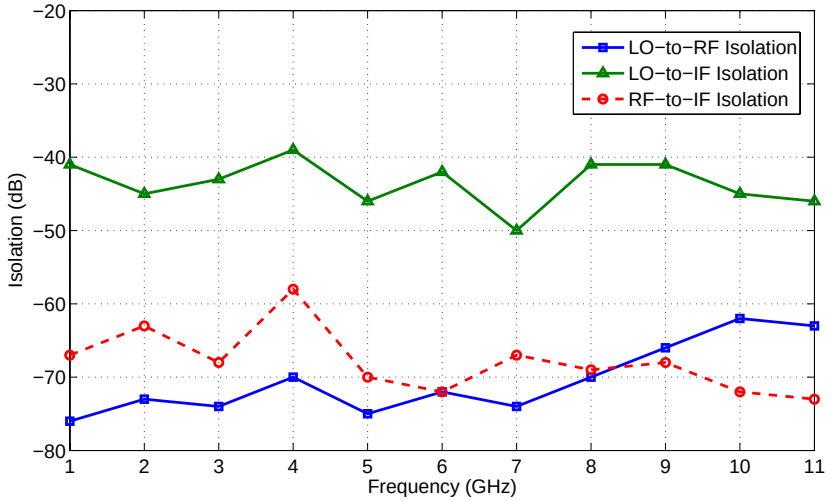

Figure 3.22: The port-to-port isolations of the mixer (measured in Mode 1)

Table 3.3: Broadband Mixer Performance Summary and Comparison Table

	This Work	[46]	[47]	[48]	[24]
Technology	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Frequency (GHz)	2-10	1.6	2.4	5.25	3.1-4.7
Conversion Gain (dB)	5-24	-50-5	15-24	-28-6	-20-10
LO-to-RF Isolation (dB)	70	N/A	30	53	N/A
Supply Voltage (V)	1.2	1.8	0.8	1.8	1.5
DC Power (mW)	2.4-18	4.2	2	7.2	2.5
Chip Area (mm^2)	0.19	0.025	0.931	N/A	N/A

A comparison of the measured results with other current state-of-art works is shown in Table 3.3.

3.5 Conclusion

In this chapter, a broadband downconverter mixer with variable conversion gain was demonstrated in 0.13-μm CMOS technology. The mixer worked from 2 to 10 GHz. By changing the effective transistor size of the transconductor and the load, the mixer was able to work in three different modes with different conversion gain and power consumption. In Mode 1, the conversion gain of the mixer was around 24 dB and could be reduced by 3.5 dB by changing the load. The power consumption in this mode was also the highest which was 18 mW under a supply voltage of 1.2 V. In Mode 2, the conversion gain of the mixer was 17 dB and could be reduced by 3 dB. The power consumption in this mode was 12 mW under a supply voltage of 1.2 V. In Mode 3, the conversion gain of the mixer was 9 dB and could be reduced by around 4 dB. The DC power consumption was 2.4 mW under a 1.2 V voltage supply. The mixer occupied a die area of 0.35 mm $\times$ 0.54 mm without bonding pads.

Chapter 4

A SSB Mixer with Sideband Selection

4.1 Introduction

This chapter introduces a single-sideband (SSB) upconverter mixer which allows the user to select the sideband of interest to be transmitted, namely, the upper sideband (USB) or the lower sideband (LSB). The detailed description of the sideband selection concept will be shown in Section 4.2. This chapter then describes in detail the design of the components of the proposed upconverter mixer. Finally, the chapter concludes with simulations and measurement results of the fabricated IC.

4.2 Sideband Selection Concept

As discussed in Chapter 2, a conventional SSB mixer employs quadrature LO and IF signals to realize sideband rejection. Figure 4.1 shows the SSB mixer structure which is commonly used in a transceiver. It consists of two Gilbert cell mixers with their outputs added in the current domain [23]. If we suppose that the mixers act as ideal

components, the output currents at A and B can be written as:

$$I_{outA} = I * cos\omega_{IF}t * cos\omega_{LO}t \tag{4.1}$$

$$I_{outB} = -I * cos\omega_{IF}t * cos\omega_{LO}t \tag{4.2}$$

where I equals to $\frac{2}{\pi}g_m V_{RF}$, and g_m is the transconductance of the mixer and V_{RF} is the amplitude of the RF input signals. Similarly, the output currents at C and D are:

$$I_{outC} = I * sin\omega_{IF}t * sin\omega_{LO}t \tag{4.3}$$

$$I_{outD} = -I * sin\omega_{IF}t * sin\omega_{LO}t \tag{4.4}$$

Thus, the output currents at I_{out1} and I_{out2} are:

$$I_{out1} = I * (cos\omega_{IF}t * cos\omega_{LO}t + sin\omega_{IF}t * sin\omega_{LO}t) \tag{4.5}$$

$$= I * cos(\omega_{LO}t - \omega_{IF}t) \tag{4.6}$$

$$I_{out2} = -I * (cos\omega_{IF}t * cos\omega_{LO}t + sin\omega_{IF}t * sin\omega_{LO}t) \tag{4.7}$$

$$= -I * cos(\omega_{LO}t - \omega_{IF}t) \tag{4.8}$$

In the ideal case, when the input quadrature signals and the two mixers are perfectly matched, the output frequency will only consist of the lower sideband $f_{LO} - f_{IF}$ while the upper sideband $f_{LO} + f_{IF}$ is completely rejected. However, if we invert the polarity of the differential IF input signals at the I path (port 1 and port2), as shown in Figure 4.2 where $cos\omega_{IF}t$ and $-cos\omega_{IF}t$ are exchanged, the output currents at A and B will become:

$$I'_{outA} = -I * cos\omega_{IF}t * cos\omega_{LO}t = I_{outB} \tag{4.9}$$

$$I'_{outB} = I * cos\omega_{IF}t * cos\omega_{LO}t = I_{outA} \tag{4.10}$$

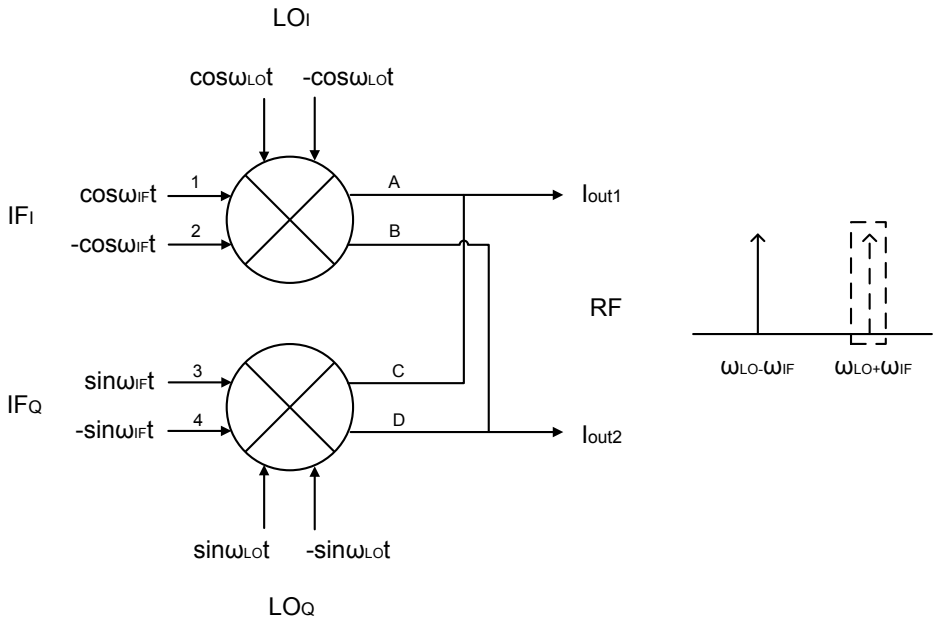

Figure 4.1: SSB mixer commonly used in transmitters

It is clear that the polarity of the output currents at A and B are inverted accordingly. Since the Q path remains the same, the output currents at I_{out1} and I_{out2} can be written as:

$$I'_{out1} = -I * (cos\omega_{IF}t * cos\omega_{LO}t - sin\omega_{IF}t * sin\omega_{LO}t) \tag{4.11}$$

$$= -I * cos(\omega_{LO}t + \omega_{IF}t) \tag{4.12}$$

$$I'_{out2} = I * (cos\omega_{IF}t * cos\omega_{LO}t - sin\omega_{IF}t * sin\omega_{LO}t) \tag{4.13}$$

$$= I * cos(\omega_{LO}t + \omega_{IF}t) \tag{4.14}$$

We can see that the upper sideband $f_{LO} + f_{IF}$ remains while the lower sideband $f_{LO} - f_{IF}$ is rejected. The same analysis can be performed if we invert the polarity of the LO differential input signals instead. Thus, by inverting the polarity of the differential input signals at one path (I or Q), regardless of IF or LO, we will be able to choose the sideband of interest to be transmitted.

The unwanted sideband can be completely rejected provided that the signals and circuits are perfectly matched. However, mismatches always exist in reality and they

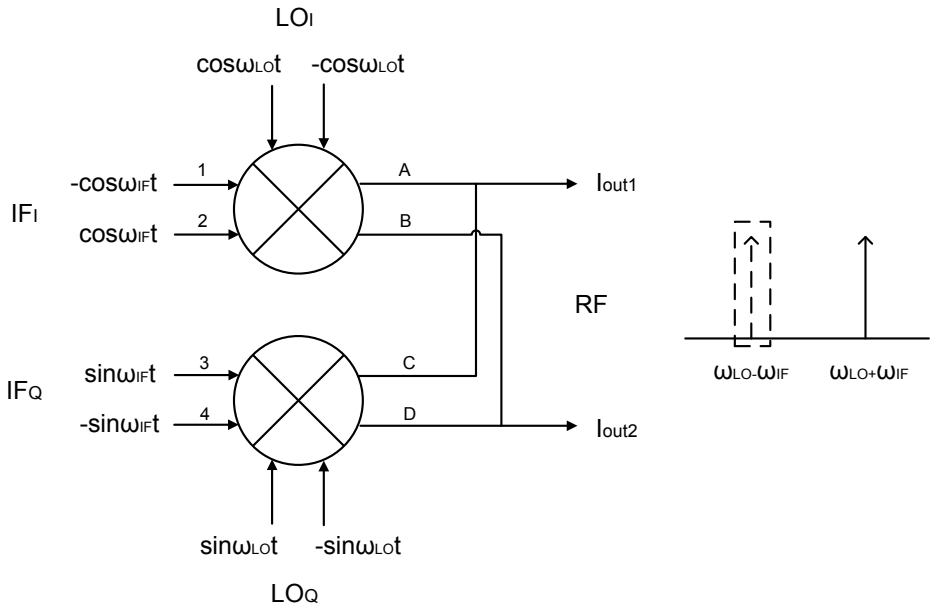

Figure 4.2: SSB mixer with switched IF signal (at the I path, input 1 and 2)

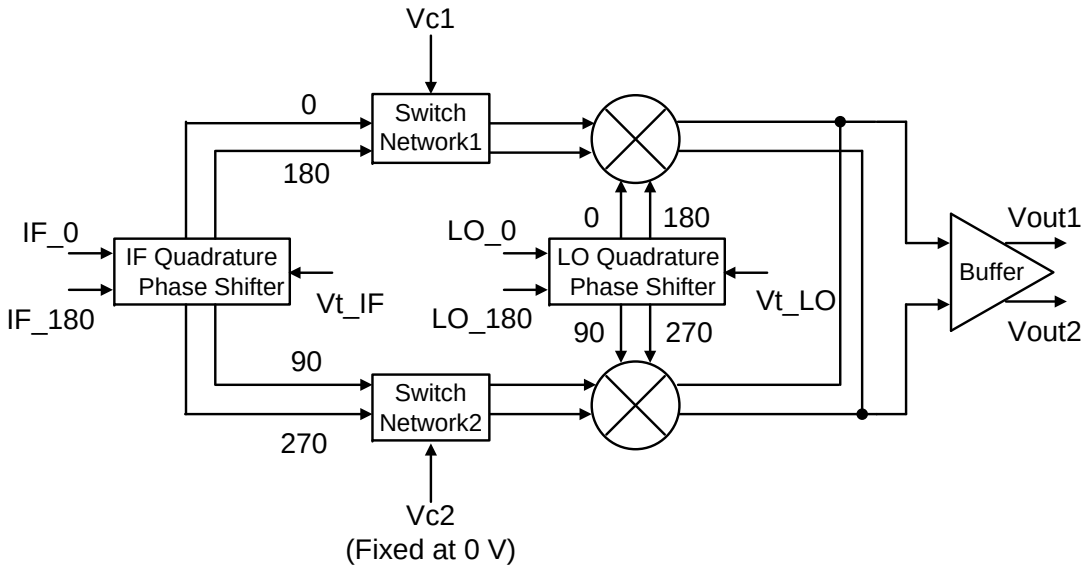

Figure 4.3: System digram of the proposed SSB mixer

decrease the amount of sideband rejection. In practice, the crosstalk between the two data streams becomes negligible if the desired signal is 30 dB above the unwanted sideband [23].

The reversal of the polarity of the differential input signals can be realized by a switch network which consists of a group of NMOS transistors in parallel. We can choose to switch either the LO or IF signal in order to choose sidebands. However, since the LO frequency is usually much higher than the IF frequency, the losses incurred by the LO switches would be significant due to the intrinsic parasitics of NMOS transistors at high frequencies. As a result, it is more desirable to switch IF signals.

Figure 4.3 shows the system digram of the proposed SSB mixer. It consists of five components: 1) an IF quadrature phase shifter; 2) an LO quadrature phase shifter; 3) two switch networks; 4) the mixer core; 5) an on-chip RF output buffer. The IF and LO quadrature phase shifters, both of which are RC polyphase networks, generate the quadrature signals required for sideband rejection. The quadrature IF signals then pass through the two switch networks before entering the mixer core. At the output, there is an on-chip RF output buffer which is used for impedance scaling for the measurements.

As shown in Figure 4.3, there are two switch networks that follow the IF quadrature phase shifter. According to the analysis above, we only need to switch either the I path or the Q path to choose the sideband. Thus, ideally, only one switch network is required. However, since the quadrature phase shifter is very sensitive to load and parasitics, another switch network is added to ensure that the four outputs of the IF quadrature phase shifter have identical load. As illustrated in Figure 4.3, the control voltage of the second switch network (V_{c2}) was fixed to be 0 V.

The IF frequency and LO frequency in this design were chosen to be 100 MHz and 5 GHz respectively. The upper sideband is then $f_{LO} + f_{IF} = 5.1$ GHz while the

lower sideband is $f_{LO} - f_{IF} = 4.9$ GHz.

4.3 Circuit Implementation

In this section, the design of the proposed mixer in 0.13-μm CMOS will be described with detailed analysis of its various components including the quadrature phase shifters, switch networks, mixer core and on-chip RF output buffer.

4.3.1 IF and LO Quadrature Phase Shifters

Several methods have been proposed to generate accurate quadrature signals, including 1) RC-CR network [1]; 2) frequency divide-by-two circuits [49] [50]; 3) inductor-capacitor (LC) high and low pass filters [51] [52]; and 4) RC ploy phase network [53] [54]. The RC-CR network has a relatively high loss, while the LC high and low filters occupy a large chip area. The frequency divide-by-two circuits could produce excellent quadrature waves, but they require the frequency of the clock signal to be twice that of the output signal. In this particular design where the LO frequency is 5 GHz, the clock frequency required will be 10 GHz. The resistor-capacitor (RC) polyphase network, however, can generate good quadrature signals with moderate loss while occupying a small chip area. Thus, in this design, the RC polyphase network is chosen as quadrature phase shifter for both IF and LO signals.

Figure 4.4 shows the RC polyphase network. It is well known that on-chip resistors generally exhibit large tolerances. For example, for the IBM 0.13-μm CMOS technology used for this design, the tolerances of resistors are usually above 10%. Tolerances are critical since they would change the cutoff frequency of the network, introducing considerable phase errors at the desired frequency. Therefore, a tunable resistor is preferred. As shown in Figure 4.4, an NMOS transistor biased in the triode region is used as a tunable resistor to allow fine-tuning for the lowest possible phase

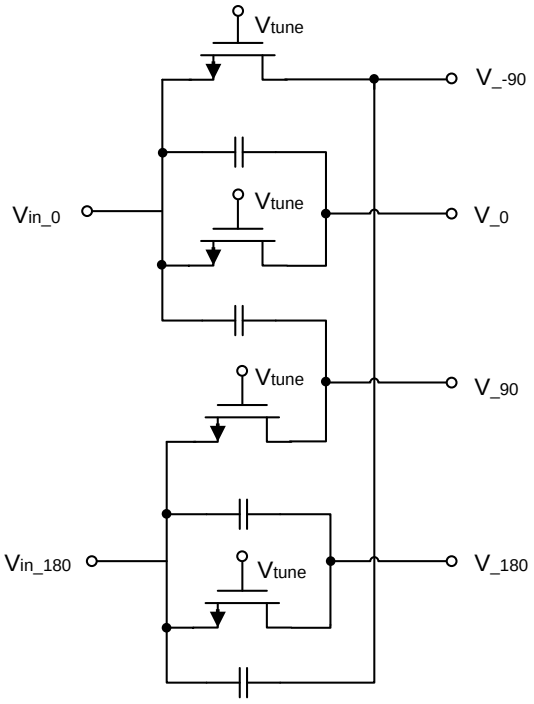

Figure 4.4: RC polyphase network

and gain errors after process variations.

The drain-to-source current-voltage characteristic (I-V) of the NMOS transistor in the triode region can be written as [55]:

$$I_{DS} = \frac{\mu_n C_{OX}}{1 + V_{DS}/(LE_{sat})} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{4.15}$$

where E_{sat} is the velocity saturation electric field. Since V_{DS} (≈ 0 V in this design) is significantly smaller than the gate overdrive voltage ($V_{GS} - V_{TH}$) and the velocity saturation voltage (LE_{sat}), this equation can be simplified as [45]:

$$I_{DS} \approx \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \tag{4.16}$$

The resistance R_{DS} is then simply the inverse of the derivative of I_{DS}:

$$R_{DS} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1} = \frac{1}{\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})} \tag{4.17}$$

where V_{GS} is the applied gate-to-source voltage which is equal to the tuning voltage V_{tune} in this design:

$$R_{DS} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{tune} - V_{TH})} \tag{4.18}$$

Thus, the require tuning voltage V_{tune} can be calculated as:

$$V_{tune} = \frac{1}{\mu_n C_{OX} \frac{W}{L} R_{DS}} + V_{TH} \tag{4.19}$$

In IBM 0.13-μm CMOS technology, the device parameters are as follows [56]:

$$K' = \frac{\mu_n C_{OX}}{2} = 270 \sim 290 \ uA/V^2 \tag{4.20}$$

$$V_{TH} = 0.4 \sim 0.44 \ V \tag{4.21}$$

In the following analysis, we will use $K' = 280 \ uA/V^2$ and $V_{TH} = 0.4 \ V$.

4.3.1.1 IF Polyphase Network

For the IF polyphase network, the cutoff frequency was chosen to be 100 MHz which is the frequency of the IF signal. Since the cutoff frequency is relatively small, large capacitors and resistors are required. In this design, the capacitor in the polyphase network was set to 5 pF. With C=5 pF, the resistance R needed to yield a cutoff frequency of 100 MHz will be:

$$R = \frac{1}{2\pi f C} = 330 \ \Omega \tag{4.22}$$

In 0.13-μm CMOS technology, this is a relatively large resistance to realize since the channel length is small. To solve this problem, there are two possible approaches. First, from Equation 4.18, we can see that in order to get a large resistance, we can

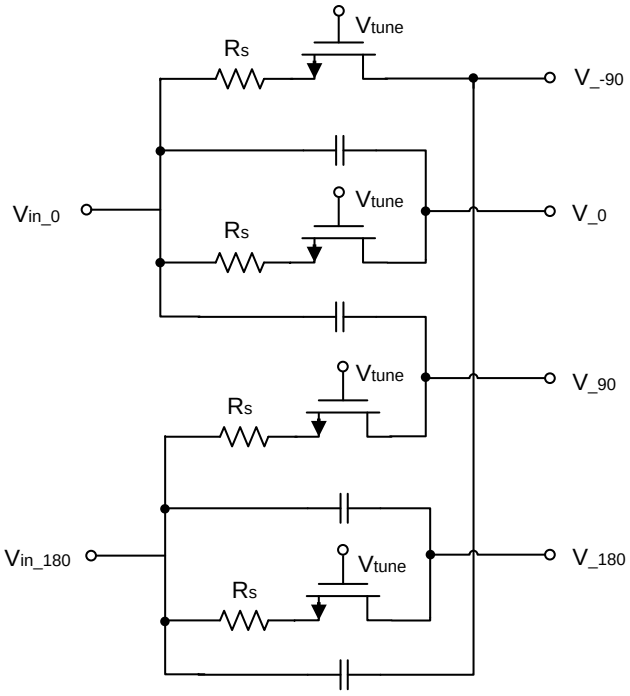

Figure 4.5: RC polyphase network with serial resistors

either increase the channel length or decrease the width of the transistor. Second, a resistor can be put in series with the transistor so that the required variable resistance of the transistor can be much smaller, as shown in Figure 4.5.

In this design, the series resistor R_s was chosen to be 280 Ω, which reduces the required variable resistance to 50 Ω. The channel length of the transistor was set to be 1 μm, and the total width of the transistor was 60 μm. With all the parameters above, the tuning voltage $V_{tune,IF}$ can be calculated as:

$$V_{tune,IF} = \frac{1}{\mu_n C_{OX} \frac{W}{L} R} + V_{TH} = 1\ V \tag{4.23}$$

The simulation of the IF polyphase network was performed in Agilent ADS. Figure 4.6 shows the phase of the outputs of the IF polyphase network. As we can see, at the calculated IF tuning voltage (1 V), the phase imbalance was around 5°. The best IF tuning voltage was 0.8 V where the corresponding phase imbalance was within 1°. The simulated gain imbalance was within 0.5 dB over the entire IF tuning range.

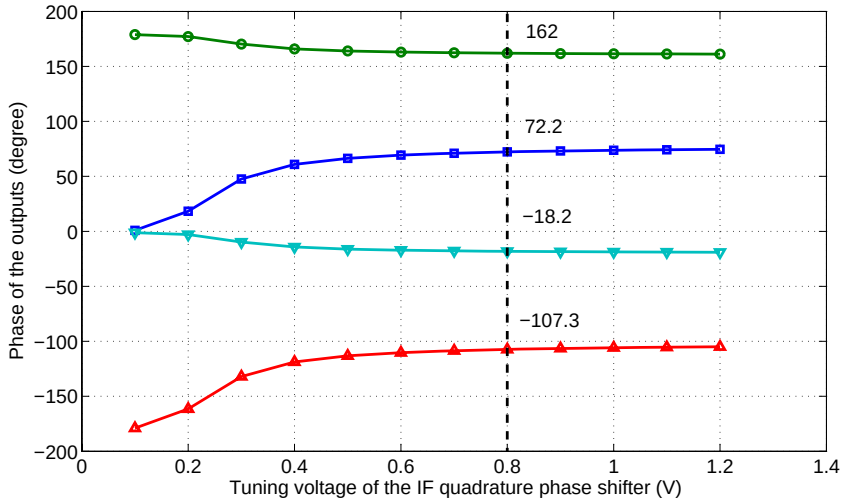

Figure 4.6: Phase of the outputs of the IF quadrature phase shifter

Simulation results showed that the loss of the IF polyphase network was around -1 dB at the calculated IF tuning voltage. Loss here is defined as power of each of the quadrature outputs minus power of each of the differential inputs.

4.3.1.2 LO Polyphase Network

For the LO polyphase network, the cutoff frequency was chosen to be 5 GHz. The capacitance was set to be 0.7 pF, yielding a resistance of 50 Ω which eliminates the need of a series resistor. Since the cutoff frequency is much higher than the IF frequency, if we choose the same channel length (1 μm) and the same tuning voltage (1 V), the total width of the transistor will be as large as 80 μm, which would introduce considerable parasitics. As a result, a channel length of 0.18 μm was chosen and the resulting total width was 30 μm. The tuning voltage $V_{tune,LO}$ is then:

$$V_{tune,LO} = \frac{1}{\mu_n C_{OX} \frac{W'}{L'} R'} + V_{TH} = 0.63\ V \tag{4.24}$$

The simulation of the LO polyphase network was also performed in Agilent ADS. Figure 4.7 shows the phase of the outputs of the LO polyphase network. At the

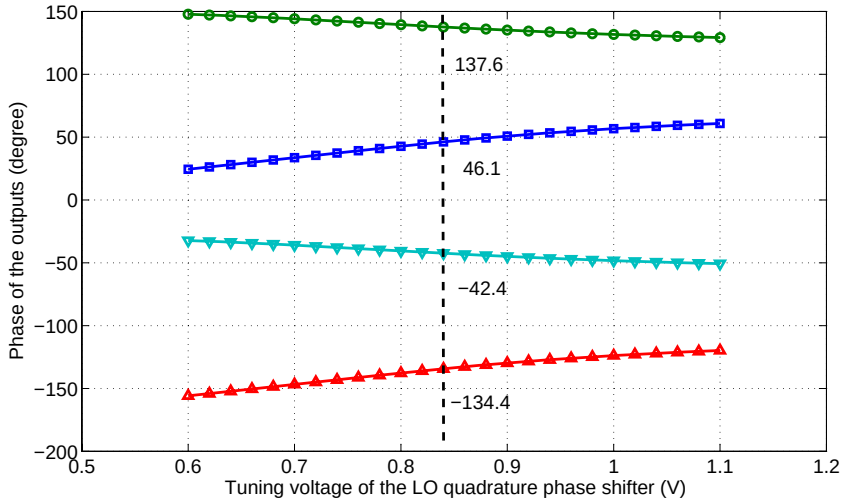

Figure 4.7: Phase of the outputs of the LO quadrature phase shifter

calculated LO tuning voltage, the phase imbalance was over 20°. This is because at 5 GHz, the high frequency transistor model needs to be used for calculation and intrinsic capacitances cannot be neglected (as shown in Figure 4.10). The best LO tuning voltage was 0.84 V where the corresponding phase imbalance was within 2°. The simulated gain imbalance was within 0.8 dB over the entire LO tuning range.

Simulation results showed that the loss of the LO polyphase network was around -1 dB at the calculated LO tuning voltage. Loss here is defined the same way as in the IF polyphase network.

4.3.2 Switch Network

As discussed in the system concept section, the function of the switch network is to invert the polarity of the differential input signals. Figure 4.8 shows the switch network used in this design. It consists of four NMOS switches in parallel. The control voltage V_c has two states, namely the 'high' state and the 'low' state, in which V_c equals 1.2 V and 0 V correspondingly. The $\overline{V_c}$ is generated by a inverter. If we suppose that the NMOS transistors act as perfect switches, the network works as follows:

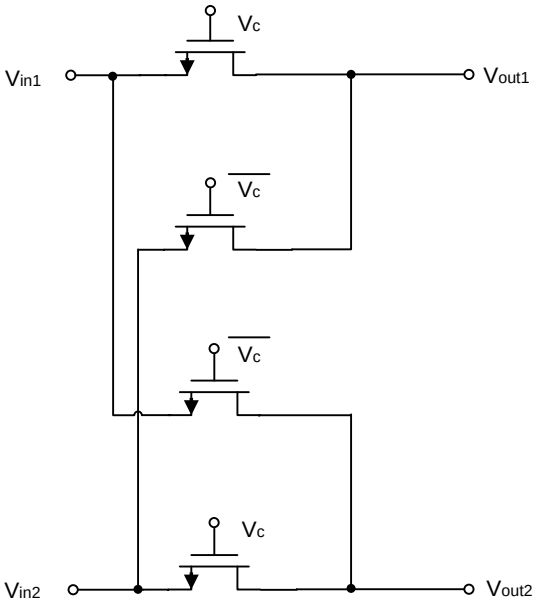

Figure 4.8: The switch network

When the control voltage V_c is high (1.2 V) and $\overline{V_c}$ is low (0 V), the output signals are:

$$V_{out1} = V_{in1} \tag{4.25}$$

$$V_{out2} = V_{in2} \tag{4.26}$$

Similarly, when the control voltage V_c is low (0 V), the $\overline{V_c}$ becomes high (1.2 V), the output signals would be:

$$V_{out1}^{'} = V_{in2} = V_{out2} \tag{4.27}$$

$$V_{out2}^{'} = V_{in1} = V_{out1} \tag{4.28}$$

Therefore, it is clear that by controlling V_c we can invert the polarity of the differential input signals.

As shown in Figure 4.3, there are two switch networks in the system. Since V_{c2} is fixed to 0 V, the sideband selection is realized by controlling V_{c1}. In this design, when

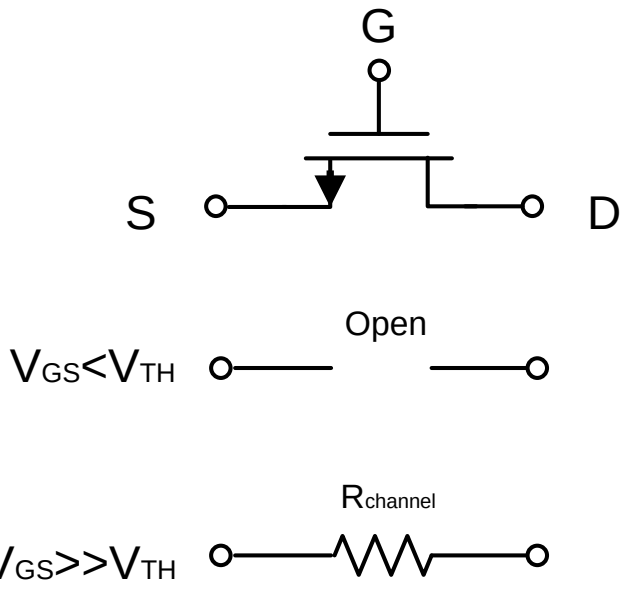

Figure 4.9: Switch model of NMOS transistor at low frequencies

V_{c1} equals 0 V, the upper sideband 5.1 GHz is selected while the lower sideband 4.9 GHz is suppressed. Similarly, when V_{c1} equals 1.2 V, the lower sideband 4.9 GHz is selected instead while the upper sideband 5.1 GHz is suppressed, as summarized in Table 4.1.

Table 4.1: Frequency Selection

Control Voltage (V_{c1})	0 V	1.2 V
Selected Sideband	5.1 GHz	4.9 GHz

The above analysis is based on the assumption that the transistors act as ideal switches. In reality, however, NMOS transistors cannot be treated as perfect switches due to the channel resistance and parasitics. Figure 4.9 shows the operation of NMOS switches at low frequencies [45]. It is clear that when the NMOS switch is $'$on$'$, a channel resistance $R_{channel}$ connects the drain and source of the transistor. This resistance will introduce loss to the signal and should be kept as small as possible. Similar to the analysis of R_{DS} in the last section, the channel resistance can be written as:

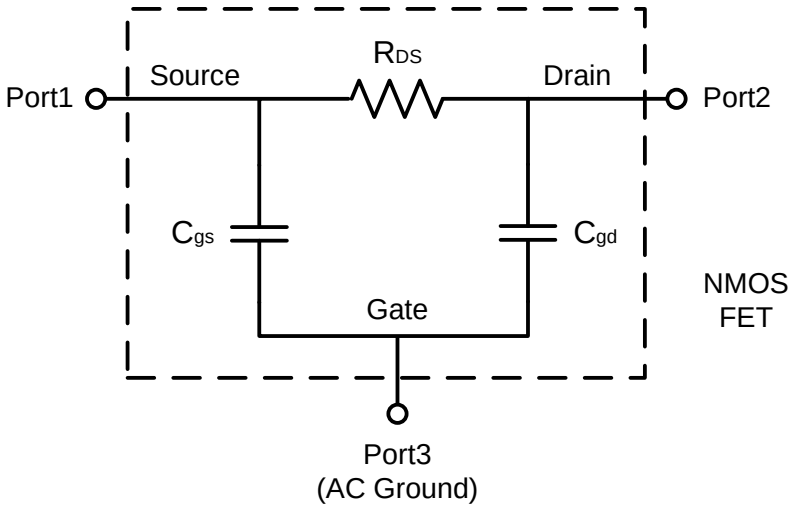

Figure 4.10: Switch model of NMOS transistor at high frequencies

$$R_{channel} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_c - V_{TH})} \tag{4.29}$$

At high frequencies (in the GHz range for example), a more careful analysis is needed due to the important intrinsic parasitic capacitances of NMOS transistors. Figure 4.10 shows the high frequency model of the NMOS switches [57], where the gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} are given by [45]:

$$C_{gs} = C_{gd} = \frac{1}{2}C_{gc} + C_{ov} \approx \frac{1}{2}C_{OX}WL_{eff} + C_{OX}WL_D \tag{4.30}$$

where C_{gc} denotes the gate-to-channel capacitance, C_{ov} represents the overlap capacitance of the gate oxide with the drain or source and L_{eff} is the effective channel length. L_D is the diffusion overlap length which becomes more significant as the device length scales down.

It is clear from Equation 4.29 that if we increase the transistor width W, the resistance $R_{channel}$ decreases. On the other hand, according to Equation 4.30, C_{gs} increases as we increase the transistor width W. As a result, a careful trade-off needs to be made to yield a small loss.

In this design, a moderate transistor width of 20 μm was chosen with a channel

length of 0.13 μm. Simulation results showed that the proposed switch network had a loss of 0.2 dB at 100 MHz.

4.3.3 SSB Mixer Core

As discussed in Chapter 2, the upconverter mixer in a transmitter can be realized by two Gilbert cell mixers with their outputs added in the current domain [23]. As device length L scales down from one technology generation to the next, the supply voltage scales down at the same time. In sub-micron technologies such as 0.13-μm CMOS, the supply voltage is typically 1.2 V. Since the DC currents of the two Gilbert cell mixers are added together, the voltage drop at the load resistors would be large enough to drive the switches and transconductors into the linear region.

In this design, an inductor was used instead as a load to provide enough conversion gain while avoiding a DC voltage drop across the load, as shown in Figure 4.11. The inductor used in this design was a parallel stacked spiral inductor which consisted of a symmetric spiral at the top levels of the metal (MA) and crossovers at alternating top level metals ($E1$) [58]. The composite structure was realized over an M1 ground plane to maximize the quality factor (Q) [58]. The value of the inductor was carefully chosen to provide maximum conversion gain at the desired frequency of 5 GHz.

The simulation of the proposed mixer core circuit was performed in Agilent ADS. Simulation results showed that the mixer consumed 14 mA of DC current with a 1.2 V voltage supply. At 5 GHz, the voltage conversion gain of the mixer was around 15 dB.

4.3.4 Output Buffer

The most typically used on-chip buffer structures are source followers and differential amplifiers with a resistive load. However, they usually consume large amounts of DC power, resulting in poor power efficiency. Besides, due to body effects, NMOS source

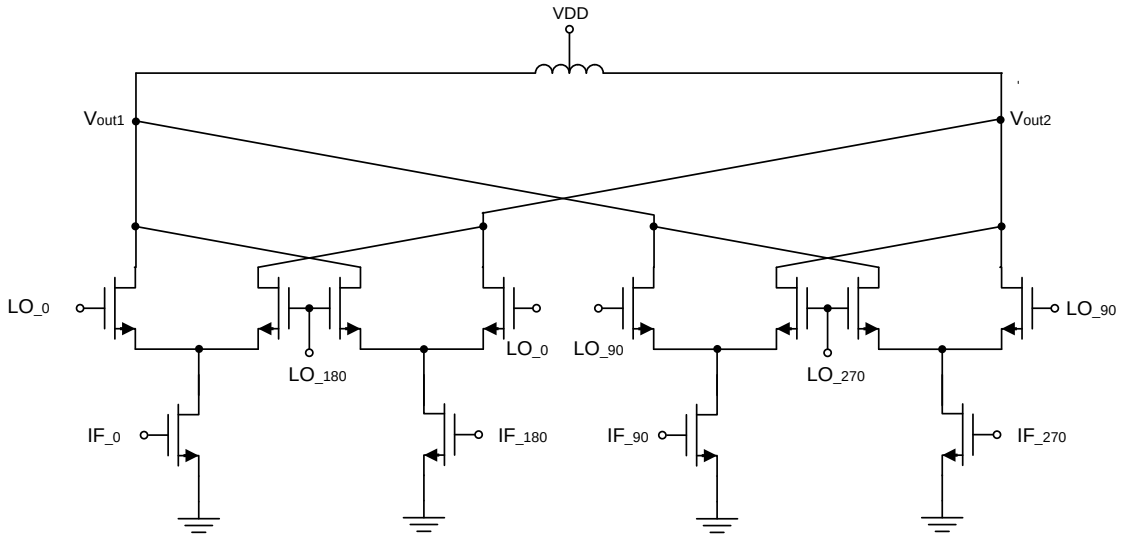

Figure 4.11: SSB mixer core with inductor load

followers suffer from high insertion loss [59].

In this design, a modified source follower was used as the on-chip buffer, as shown in Figure 4.12. The outputs of the mixer are fed into the source followers (M_3 and M_4). With opposite polarity, they are also capacitively coupled to the current sources (M_1 and M_2) [60]. For the simplicity of analysis, we ignore the output conductance of the transistors and reactive effects, then the voltage gain of the buffer can be calculated as [33]:

$$A_v = \frac{g_{m3} + g_{m2}}{g_{m3} + g_{mb3} + \dfrac{1}{R_L}} \tag{4.31}$$

where R_L refers to the load impedance which is 50 Ω in a typical RFIC design and g_{mb3} is the back-gate transconductance. From the above equation, we can conclude that for a unity gain we need to meet the following equation:

$$g_{m2} = g_{mb3} + \frac{1}{R_L} \tag{4.32}$$

The main advantage of the modified source follower is that it increases the voltage gain by 6 dB. Suppose that a traditional source follower is used, then Equation 4.31

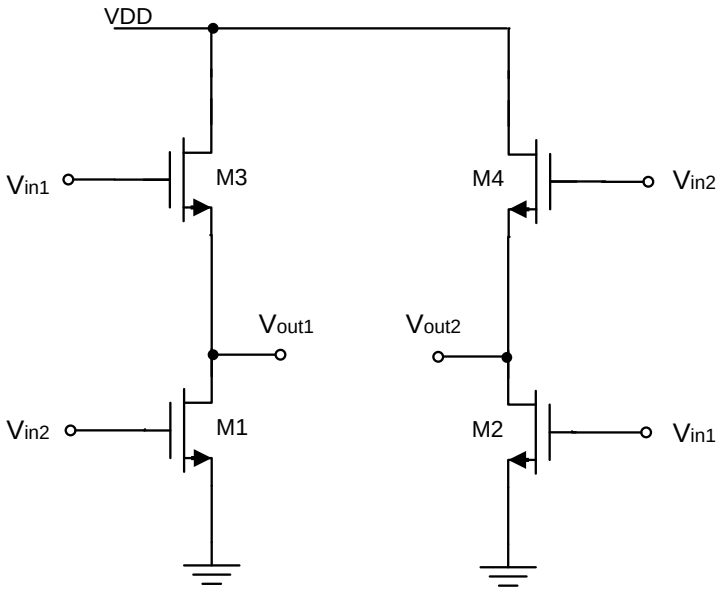

Figure 4.12: Modified source follower

will become:

$$A_v^{'} \approx \frac{g_{m3}}{g_{m3} + g_{mb3} + \frac{1}{R_L}} \approx \frac{1}{2} A_v \tag{4.33}$$

Other advantages include that compared to traditional source followers, there is no additional increase in DC current or the output impedance, and the noise figure and linearity are not degraded. Furthermore, the operating frequency range of the buffer could be a large fraction of f_T [33].

In this design, all the transistor widths were set to 50 μm. As a result, the drain-to-source voltage (V_{DS}) of the four transistors would be the same which was 0.6 V. The gate-to-source voltage (V_{GS}) was also set to 0.6 V. The device parameters are the same as in Equation 4.21. A summary of parameters can be listed as follows:

$$K^{'} = \frac{\mu_n C_{OX}}{2} = 270 \sim 290 \ uA/V^2 \tag{4.34}$$

$$V_{TH} = 0.4 \sim 0.44 \ V \tag{4.35}$$

$$V_{GS} = V_{DS} = 0.6 \ V \tag{4.36}$$

In order to simplify the calculations, we still use the long-channel transistor model. The transconductance of a transistor in saturation could be written as [5]:

$$g_m = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) \tag{4.37}$$

Substituting all the parameters into the above equation gives us:

$$g_m = 560 \times 10^{-6} \times \frac{50}{0.13} \times (0.6 - 0.4) = 0.043\ S \tag{4.38}$$

The voltage gain of the buffer can be calculated from Equation 4.31. The back-gate transconductance (g_{mb}) is typically 30% of the main transconductance (g_m) [5]. Thus, the voltage gain of the buffer in this design is:

$$A_v = \frac{g_{m3} + g_{m2}}{g_{m3} + g_{mb3} + \frac{1}{R_L}} = \frac{0.043 + 0.043}{0.043 + 0.043 \times 0.3 + \frac{1}{50}} = 1.13 \tag{4.39}$$

which is very close to unit gain.

The simulation of the buffer circuit was performed in ADS. Two 50 Ω load resistors were connected to the output of the buffer. Simulation results showed that the buffer consumed 7.1 mA of DC current with a 1.2 V voltage supply. At 5 GHz, the voltage gain of the buffer was around -0.5 dB which was close to the calculation result above. The input P1dB of the buffer was around 1 dBm while the corresponding output P1dB was 0 dBm.

4.4 Measurement Results

Figure 4.13 shows the layout of the chip in Cadence Virtuoso. The proposed mixer was fabricated using IBM 0.13-μm CMOS technology, which had 8 metal levels including 3 thin metal layers, 2 thick metal layers and 3 RF metal layers. It occupied a die area of 0.7 mm × 0.7 mm without bonding pads and 1 mm × 1 mm with bonding

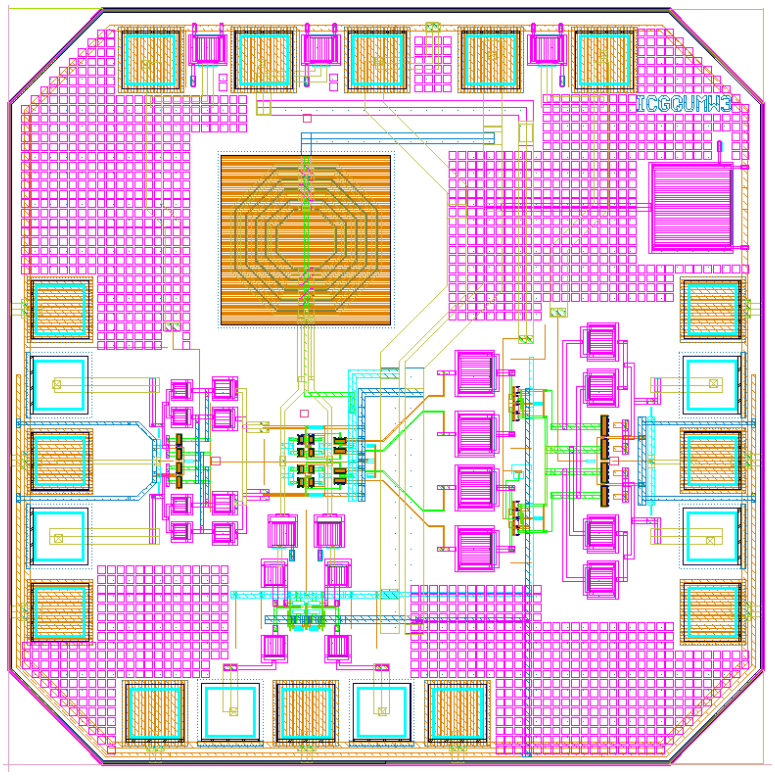

Figure 4.13: The layout of the chip in Virtuoso

pads. The whole circuit consumed 22 mA of DC current from a 1.2 V voltage supply. Figure 4.14 shows the photograph of the fabricated mixer chip.

In order to test the fabricated IC, a direct on-wafer measurement was performed using Cascade Microtech coplanar waveguide (CPW) probes and DC probes on a probe station. The LO and IF signals were generated by two Anritsu MG3694 signal generators. An Agilent E4446A spectrum analyzer was used to examine the spectrum of the output signal.

Since all three ports (IF, RF and LO) of the mixer were fully differential, three GSGSG CPW probes with pitch size of 100 μm were used. In order to generate fully differential IF signals, an external 180° hybrid was used to convert the single input signal into differential signals. To generate differential LO signals, a power splitter was first used to split the LO input signal into two in-phase branches, followed by two identical phase shifters to generate a 180° phase difference. At the RF output,

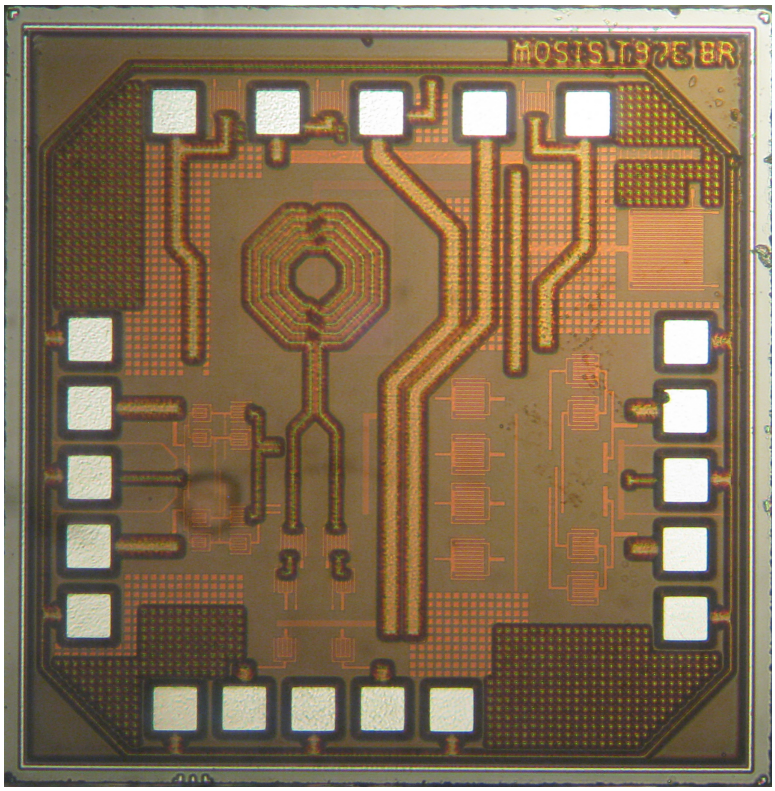

Figure 4.14: Photograph of the fabricated chip

another external 180° hybrid was used to convert the differential output signals into a single output signal.

As discussed in the system concept, the control voltage V_{c1} determines the sideband to be selected while V_{c2} is fixed to 0 V, as summarized in Table 4.1.

Upper Sideband Mode Measurements (5.1 GHz)

First, the control voltage V_{c1} was set to 0 V and the mixer worked in the upper sideband mode. Figure 4.15 shows the mixer's simulated and measured voltage conversion gain versus the tuning voltage of the IF quadrature phase shifter. As we can see, the voltage conversion gain of the upper sideband (5.1 GHz) was almost the same over the entire IF tuning range. However, the voltage conversion gain of the lower sideband (4.9 GHz) changed over the IF tuning range and reached a dip when IF tuning voltage was 0.8 V, where the sideband rejection came to a maximum of 30.4

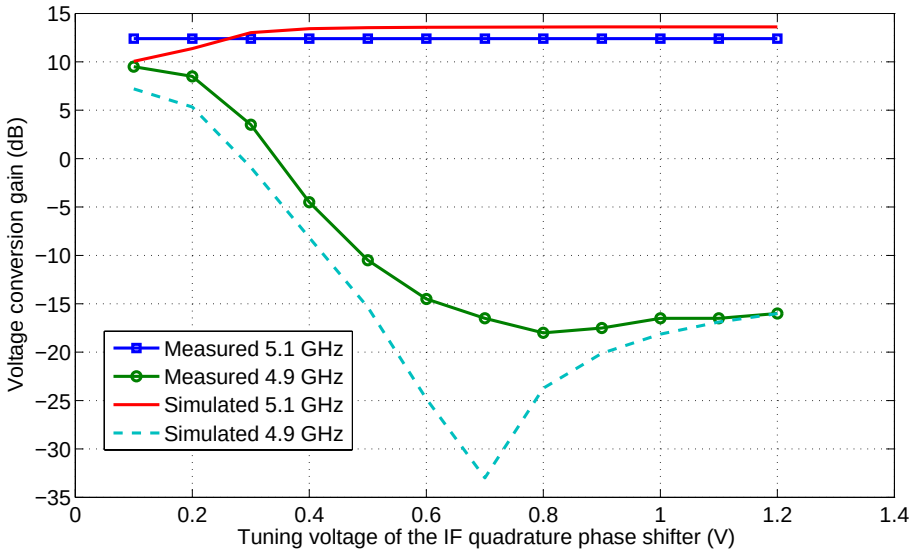

Figure 4.15: The mixer's simulated and measured voltage conversion gain versus the IF tuning voltage in the upper sideband mode

dB. The difference between the simulated and measured dip positions is due to the parasitics after fabrication.

Similarly, Figure 4.16 shows the mixer's simulated and measured voltage conversion gain versus the tuning voltage of the LO quadrature phase shifter. It was clear that the simulated result and measured result were very close to each other. The voltage conversion gain of the upper sideband (5.1 GHz) decreased slightly as the LO tuning voltage increased. The voltage conversion gain of the lower sideband (4.9 GHz) reached a dip when LO tuning voltage was 0.8 V, leading to a best sideband rejection of over 30.7 dB.

Figure 4.17 shows the spectrum of the output signal in the upper sideband mode.

Lower Sideband Mode Measurements (4.9 GHz)

Second, the control voltage V_{c1} was set to 1.2 V which selected the lower sideband (4.9 GHz) while suppressing the upper sideband (5.1 GHz). Figure 4.18 shows the mixer's simulated and measured voltage conversion gain versus the tuning voltage of the IF quadrature phase shifter. Similar to the results in upper sideband mode, the

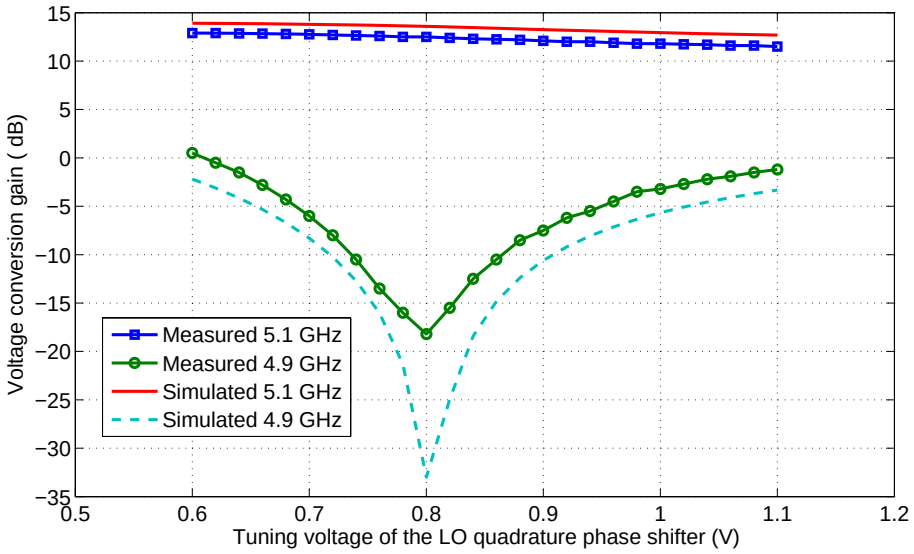

Figure 4.16: The mixer's simulated and measured voltage conversion gain versus the LO tuning voltage in the upper sideband mode

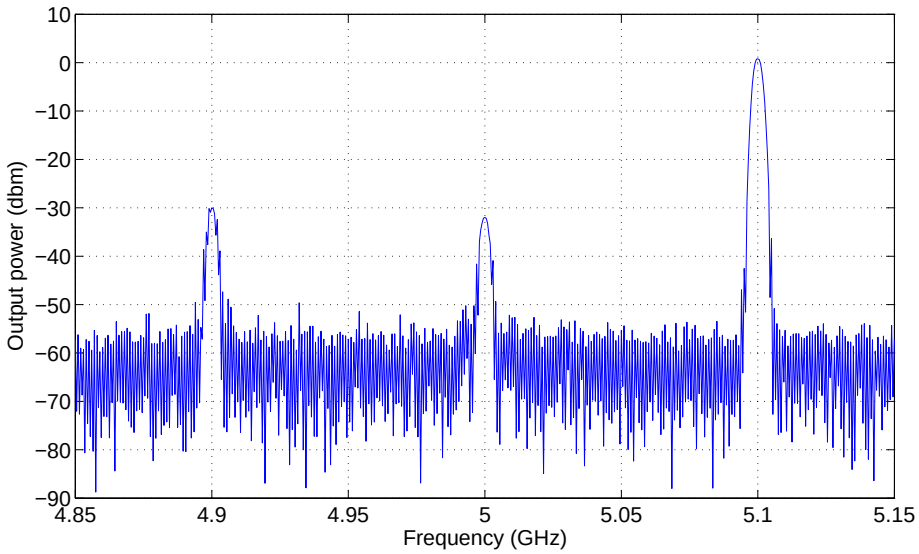

Figure 4.17: The output spectrum of the upper sideband mode

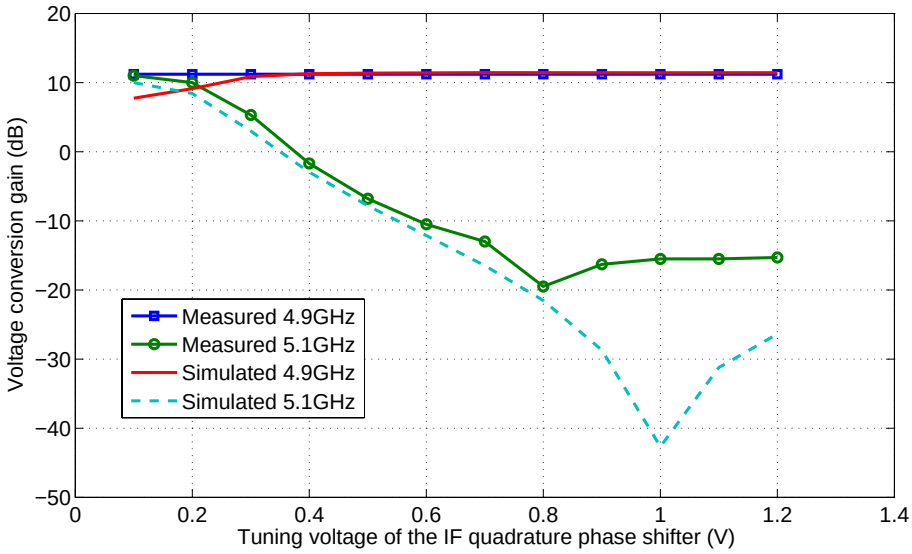

Figure 4.18: The mixer's simulated and measured voltage conversion gain versus the IF tuning voltage in the lower sideband mode

voltage conversion gain of the lower sideband (4.9 GHz) was nearly constant over the entire IF tuning range. The voltage conversion gain of the upper sideband (5.1 GHz), however, changed over the IF tuning range and reached a dip when IF tuning voltage was 0.8 V, where the sideband rejection came to the maximum (31 dB). Again, the difference between the simulated and measured dip positions is due to the parasitics after fabrication.

Figure 4.19 shows the mixer's simulated and measured voltage conversion gain versus the tuning voltage of the LO quadrature phase shifter. Again, the simulated result and measured result were very close to each other. The voltage conversion gain of the lower sideband (4.9 GHz) decreased slightly as the LO tuning voltage increased. While the voltage conversion gain of the upper sideband (5.1 GHz) reached a dip when LO tuning voltage was 0.82 V, leading to a best sideband rejection of 29.7 dB.

The spectrum of the output signal in the lower sideband mode is shown in Figure 4.20.

The input P1dB of the mixer was measured when the mixer worked in upper

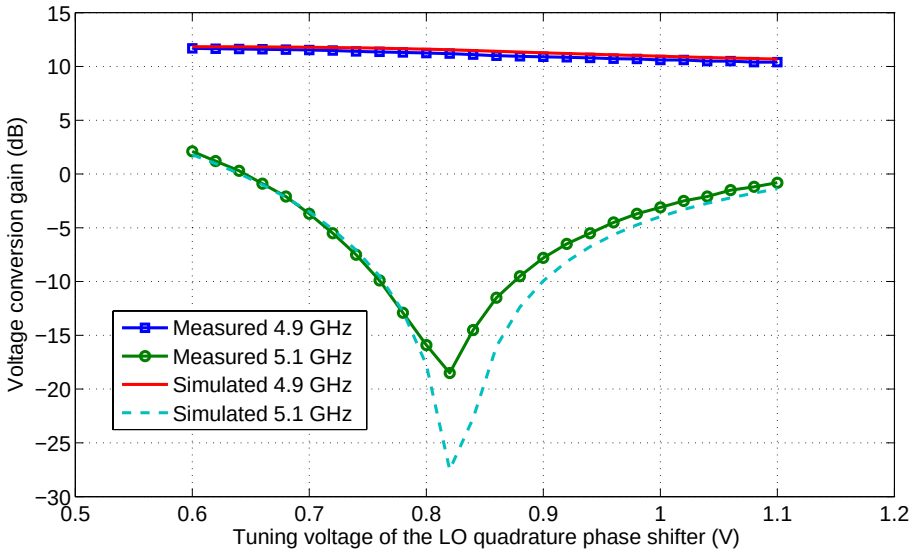

Figure 4.19: The mixer's simulated and measured voltage conversion gain versus the LO tuning voltage in the lower sideband mode

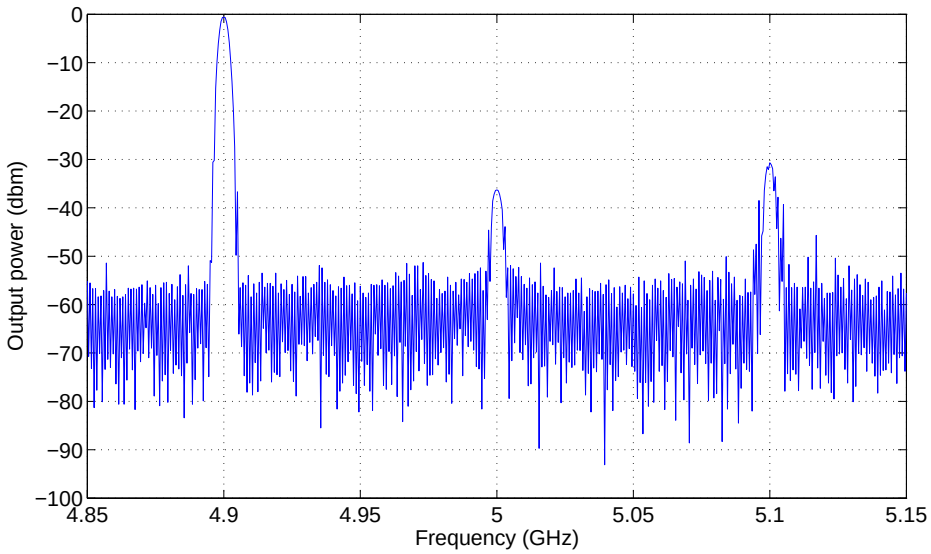

Figure 4.20: The output spectrum of the lower sideband mode

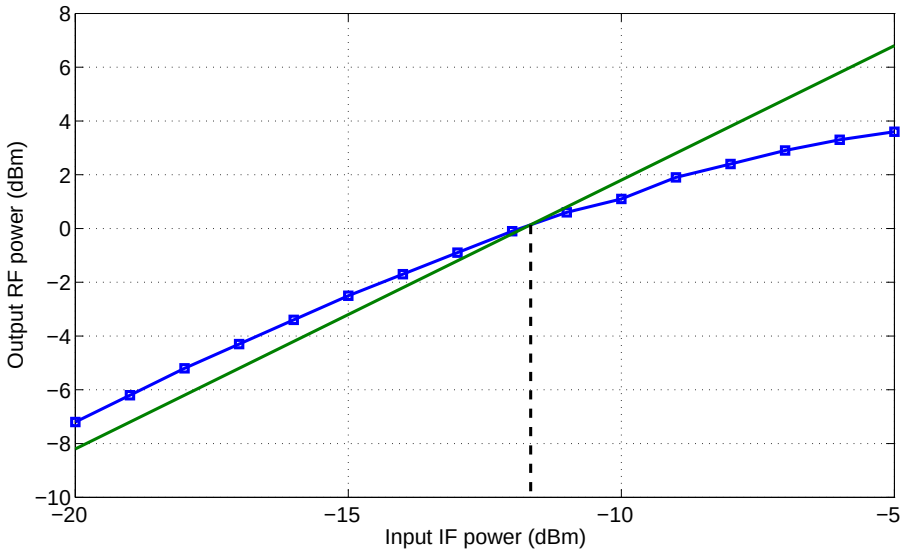

Figure 4.21: The measured P1dB of the proposed mixer

sideband mode (5.1 GHz). The tuning voltages of the IF and LO phase shifters were both set to 0.8 V. The measured result is shown in Figure 4.21. As we can see, the input P1dB was around -12 dBm while the corresponding output P1dB was 0 dBm.

A comparison of the measured results with other current state-of-art works is shown in Table 4.2. As we can see, the mixer fabricated using CMOS technology provides overall performance that is comparable to the mixers fabricated using other technologies.

Table 4.2: SSB Upconverter Performance Summary and Comparison Table

	This Work	[61]	[62]	[63]
Technology	0.13-μm CMOS	0.15-μm pHEMT	0.18-μm SiGe	0.35-μm SiGe
RF Frequency (GHz)	5.0	15	41–44	2.7 & 5.4
Conversion Gain (dB)	12.4 (max)	5	18.3	0.5
Sideband Rejection (dB)	31	63	12	62.9
Selectable Sideband?	Yes	No	No	No
Output P_{1dB} (dBm)	0	-6	-1.7 (max)	-7
LO – RF isolation (dB)	30	31	5	24
DC Power (mW)	26	86	786	36
Chip Area (mm^2)	0.49 (core)	1.26	0.66 (core)	1.0

4.5 Conclusions

In this chapter, a single-sideband (SSB) upconverter mixer with sideband selection was designed in 0.13-μm CMOS technology. Detailed design analysis and calculations were given. By setting the control voltage of the switch network, the transmitted sideband of the upconverter mixer could be chosen to be the upper sideband (USB) or the lower sideband (LSB). The mixer worked at 5 GHz with an IF frequency of 100 MHz. The measured voltage conversion gains were 11.2 dB at 4.9 GHz and 12.4 dB at 5.1 GHz. The best sideband rejection was around 30 dB. The mixer consumed 22 mA of DC current from a 1.2 V voltage supply with an on-chip buffer which consumed 7 mA of DC current.

Chapter 5

A Mixer with High Linearity

5.1 Introduction

Linearity is important to keep intra-band and inter-band intermodulations low [64]. However, in spite of the growing demand for low power and high performance in state-of-art transceiver design, linearity is becoming more and more challenging as the supply voltage scales down from one generation to the next [65]. Generally speaking, the linearity of a receiver is dominated by the mixers, while the linearity of a transmitter is mainly limited by the power amplifiers [66]. Therefore, the design of mixers with high linearity and low power consumption is crucial for low power and high performance transceivers.

One of the most widely used mixer topologies in communication systems is the Gilbert cell mixer [7]. In modern communications, it is used for both down-conversion and up-conversion. On one hand, it has the advantages of high port-to-port isolation, good broadband performance and large conversion gain. On the other hand, it consumes relatively large DC power and has moderate noise and linearity performance. Thus, in modern transceiver design where high linearity is usually required, linearization techniques need to be used to improve the linearity of Gilbert cell mixers.

Thus far, many linearization techniques have been proposed, which can improve

the linearity by various degrees at the cost of additional DC power consumption, noise degradation and die area. Although most of the linearization techniques were initially proposed to improve the linearity of LNAs, they can also be used for mixers. In [67], feed-forward distortion cancellation was used to achieve a very high IIP3 of a CMOS LNA. This technique relied on accurate scaling between the input signals of the main and auxiliary gain stages and their transfer functions, and the addition of the auxiliary stage increased the power consumption of the circuit significantly. In [68], active feedback was proposed to linearize an LNA, but the noise figure could be severely degraded in some cases using this technique. In [69], the linearity of a Si bipolar junction transistor (BJT) or a SiGe HBT could be readily improved using a simple technique based on low-frequency low-impedance base termination without degrading gain or NF. Unfortunately, this technique was not applicable for linearizing filed-effect transistors (FETs). In [5], a linearization technique known as piecewise approximation was introduced. It was based on the observation that virtually any system is linear over sufficiently small range. It divided the responsibility for linearity among several systems, each of which was active over a small enough range. The composite could exhibit high linearity over an extended range at the cost of large power consumption. In [70] [71], the optimal biasing technique was used to improve the IIP3 of an LNA by biasing the FET at a gate-source voltage (V_{GS}) at which the third-order derivative of its DC transfer characteristic was zero. Although a high IIP3 was achieved, it peaked in a very narrow range of V_{GS} and was very sensitive to bias variations. In [72] [73] [74], the derivative superposition (DS) method was used to improve the IIP3 while reducing the sensivity to bias voltage (V_{GS}). It used two or more parallel transistors of different widths and V_{GS} to achieve a composite DC transfer characteristic with an increased V_{GS} range in which the third-order derivative was close to zero. This technique achieved IIP3 improvement up to 20 dBm (in [72]) with little degradation in noise figure, gain and power consumption, all at the cost of

moderately increased die area.

In this work, the derivative superposition (DS) technique was used to improve the IIP3 of a double-balanced Gilbert cell mixer. Compared with the linearization techniques above, the topology proposed in this design had the advantage of linearizing a pre-existing mixer without modifying it. The proposed mixer was designed to operate at 1 GHz. The circuit design was performed in Cadence while the simulations were performed in Agilent ADS. The mixer chip was fabricated using IBM 0.13-μm CMOS technology.

5.2 Mixer Concept

Figure 5.1 shows the proposed mixer circuit. It consists of a mixer core without linearization which is in the dotted box, and the proposed derivative superposition (DS) circuit which is outside the dotted box. The mixer core is a typical double-balanced Gilbert cell mixer with resistive loads. Transistors M_1 and M_2 are the transconductors of the mixer, while transistors M_{1a} and M_{2a} are the transconductors of the DS circuit. The output of the DS circuit is capacitively coupled to the mixer through a large capacitor. Transistors M_5 and M_6 serve as the current source for the DS circuit.

Compared with traditional DS techniques where the DS circuit is embedded in the mixer and shares the DC bias with the mixer core, this topology has two advantages. First of all, this topology allows us to linearize the mixer core without modifying it. This is especially important when some parameters of the mixer core have already been optimized for certain applications [73]. For example, if the DC bias of the mixer core has been set to the optimal value to achieve the lowest noise figure, adding a DS circuit will force us to optimize the mixer again since noise figure is sensitive to bias conditions. Another advantage, as will be discussed in detail later, is that this kind of topology can reduce the third-order intermodulation distortion (IMD3) introduced

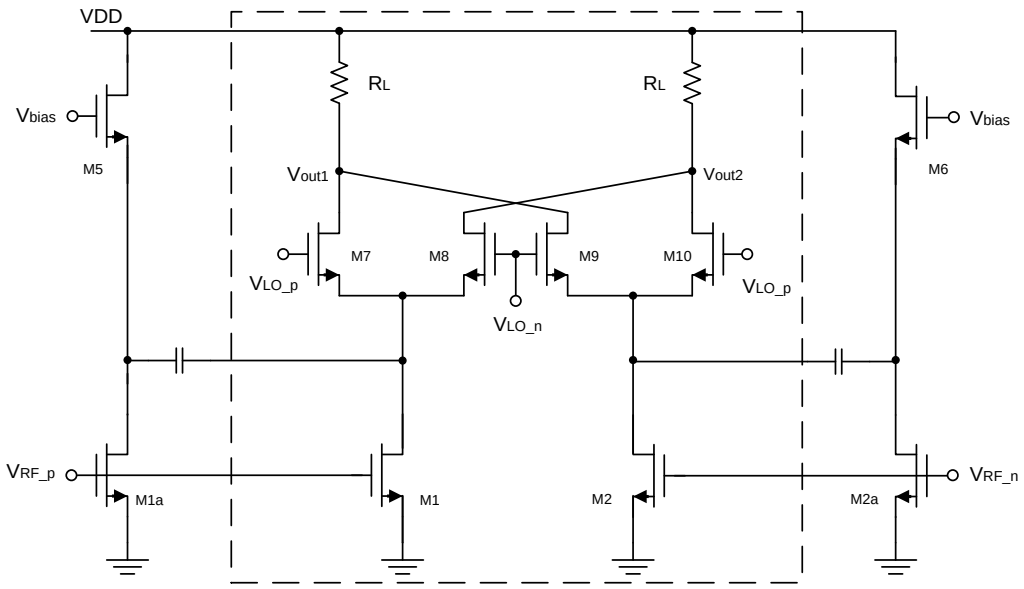

Figure 5.1: The proposed mixer circuit which consists of a mixer core without linearization which is in the dotted box, and the proposed derivative superposition (DS) circuit which is outside the dotted box.

by second-order transconductance g_2 and harmonic feedback.

5.3 Design Considerations and Circuit Implementation

In this section, the design of the proposed mixer in 0.13-μm CMOS technology will be described step by step. We start with the DC analysis, followed by detailed noise analysis and linearity analysis.

5.3.1 DC Analysis of the Transconductor Stage

Figure 5.2 shows the mixer core to be linearized in this design. It is a typical double-balanced Gilbert cell mixer. M_1 and M_2 serve as the transconductor stage of the mixer and are also the targets of linearization. M_7-M_{10} are the switches of the mixer, and R_L serves as the resistive load.

We start our design with the DC analysis of the transconductor stage of the mixer

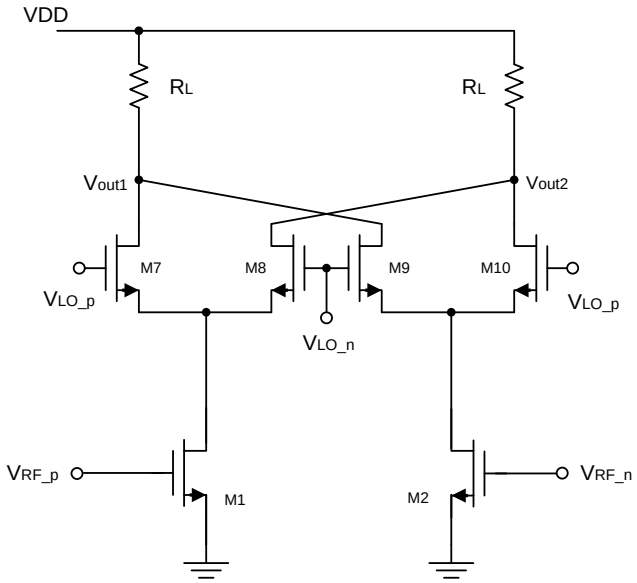

Figure 5.2: The mixer core

core. Take M_1 for example, the small-signal output current of M_1 biased in saturation can be expanded into the following power series in terms of the small-signal gate-to-source voltage v_{gs} [71]:

$$i_{d,1}(v_{gs}) = g_{1,1}v_{gs} + g_{2,1}v_{gs}^2 + g_{3,1}v_{gs}^3 + \cdots \tag{5.1}$$

where $g_{n,1}$ is the n^{th}-order small signal transconductance of M_1. The higher-order coefficients ($g_{2,1}$, $g_{3,1}$ etc.) define the strengths of the corresponding nonlinearities. Among these coefficients, $g_{3,1}$ is the most important parameter since it mainly controls the third-order intermodulation distortion (IMD3) at low signal levels. The coefficients generally depend on the DC gate-to-source voltage V_{GS} and can be written as:

$$g_{1,1}(V_{GS}) = \frac{\partial I_D}{\partial V_{GS}} \tag{5.2}$$

$$g_{2,1}(V_{GS}) = \frac{1}{2}\frac{\partial^2 I_D}{\partial^2 V_{GS}} \tag{5.3}$$

$$g_{3,1}(V_{GS}) = \frac{1}{6}\frac{\partial^3 I_D}{\partial^3 V_{GS}} \tag{5.4}$$

The IIP3 can then be calculated in voltage (V) as [5]:

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{1,1}}{g_{3,1}}\right|} \tag{5.5}$$

When the input impedance is matched to 50 Ω, the IIP3 can be written in dBm as [73]:

$$IIP3 = 10\log\left(\frac{40}{3}\left|\frac{g_{1,1}}{g_{3,1}}\right|\right) \tag{5.6}$$

Therefore, in order to get a high IIP3, we need to make $g_{3,1}$ as small as possible. Ideally, when $g_{3,1}$ equals 0, IIP3 goes to infinity. However, when $g_{3,1}$ is completely canceled, IMD3 will be dominated by the fifth order or higher odd-order nonlinearities. As a result, IMD3 will increase with the input power with a slope greater than 3, which makes IIP3 meaningless [72].

The derivative superposition (DS) technique reduces g_3 of a transistor by putting another transistor in parallel with a negative g_3, yielding a composite g_3 of 0. It is well known that the polarity of g_3 changes with the bias conditions (V_{GS}) of the FET. When the FET works in saturation, or strong inversion, it has a negative g_3. When the FET works in weak inversion, g_3 becomes positive. To verify this claim, we can simulate the g_3 of M_1 as a function of the gate-to-source voltage V_{GS}. In this design, the channel length of M_1 was set to 0.13 μm and the width of the transistor was set to 60 μm. By setting V_{DS} to 360 mV, the g_3 of M_1 as a function of V_{GS} can be

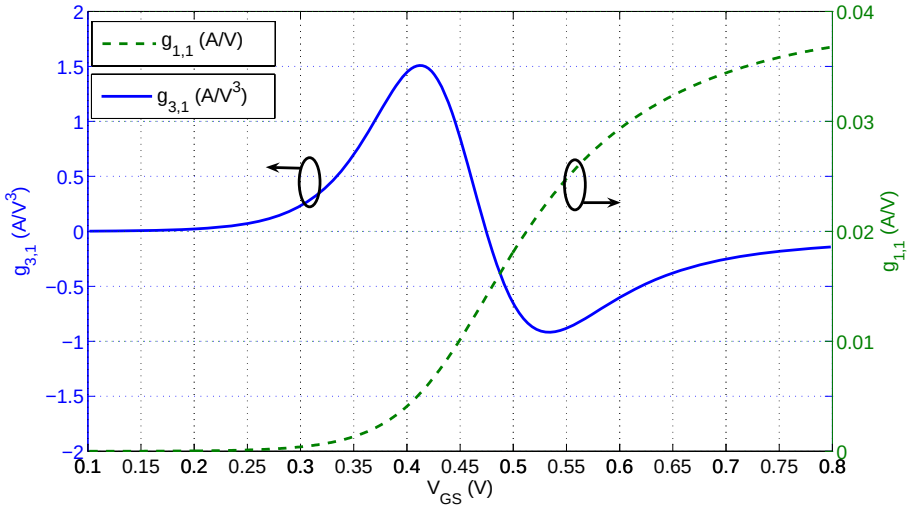

Figure 5.3: The $g_{1,1}$ and $g_{3,1}$ of M_1

shown in Figure 5.3. It is clear that as V_{GS} increases, $g_{3,1}$ changes from positive (weak inversion) to negative (strong inversion). Therefore, in order to improve the IIP3 of M_1, we can put a transistor in weak inversion (M_{1a}) in parallel, as shown in Figure 5.4. By setting the magnitude of g_3 of the two transistors equal, namely $g_{3,1}$+$g_{3,1a}$=0, a significant improvement in IIP3 can be achieved as g_3 of the two transistors cancel each other.

In this design, the V_{GS} of M_1 was set to 0.55 V. From the solid line in Figure 5.3, we can see that $g_{3,1}$ equals -0.883 A/V^3. To the first-order, we only need to set $g_{3,1a}$ equals +0.883 A/V^3 to get a composite g_3 of 0. However, there are infinite numbers of combinations of V_{GS} and transistor size that will give us the required $g_{3,1a}$. In other words, we need to find another parameter (i.e., noise figure, power consumption) to limit the number of combinations of V_{GS} and transistor size that we can choose from. Since noise figure is usually very important in receiver design, we proceed to find the optimal V_{GS} and transistor size of M_{1a} that yields the best noise performance.

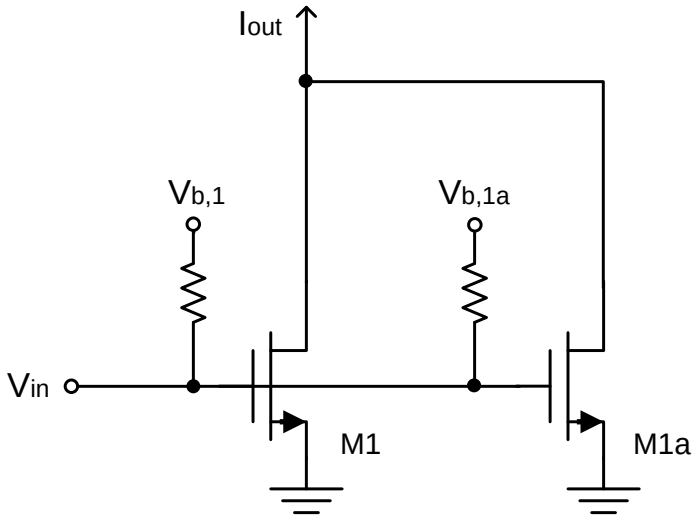

Figure 5.4: This graph shows the derivative superposition with two FETs in parallel. M_1 works in saturation with a negative g_3 while M_{1a} works in weak inversion with a positive g_3. By making $g_{3,1a}$=$-g_{3,1}$, g_3 of the composite structure will be 0.

5.3.2 Noise Analysis of Derivative Superposition Method

In this section, we analyze the noise degradation introduced by the derivative superposition method. Since the DC biases of the mixer core and the DS circuit are separated, the DS circuit has little influence on the noise performance of the mixer core's switch stage. Therefore, in order to find out the noise contribution of the DS circuit, we only need to analyze the noise performance of the composite structure as shown in Figure 5.4.

Figure 5.5 shows the small signal noise model. In the following analysis, we will use first-order approximations of the drain current noise ($\overline{i_{nd}^2}$) and gate induced noise ($\overline{i_{ng}^2}$). The results calculated may not be accurate for predicting the absolute values of the noise figure (NF), but they can show us the trend and thus give us insights into circuit design.

In order to facilitate our analysis, we first introduce a parameter called Noise Degradation (ND) which is defined as the increase of minimum noise factor (F_{min}) after the DS circuit is added:

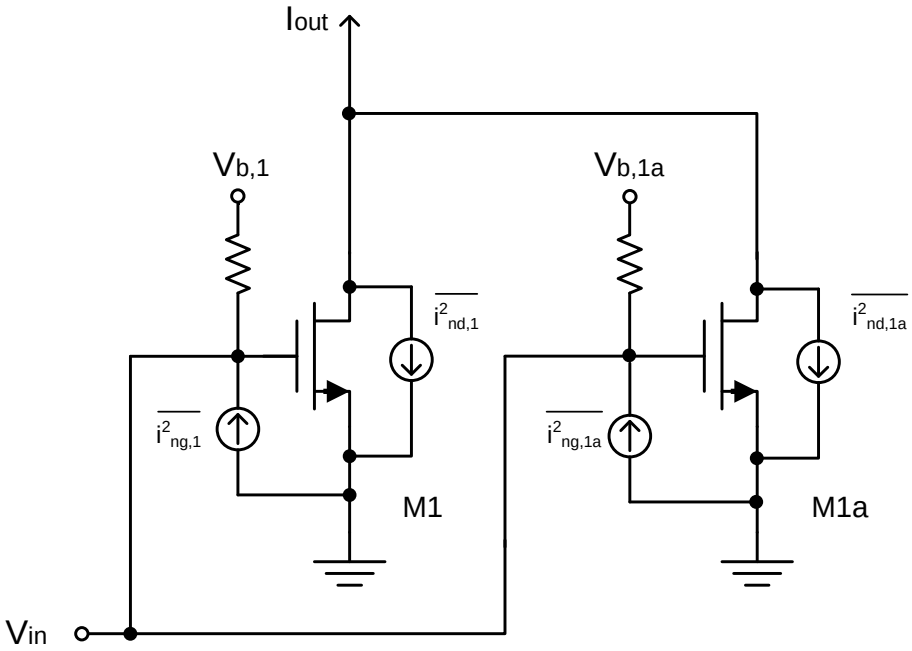

Figure 5.5: The noise model of the DS circuit

$$ND = 10\ \log F'_{min} - 10\ \log F_{min} = 10\ \log\left(\frac{F'_{min}}{F_{min}}\right) \tag{5.7}$$

We first calculate the F_{min} of transistor M_1. Van der Ziel has shown that the drain current noise ($\overline{i^2_{nd,1}}$) and induced gate noise ($\overline{i^2_{ng,1}}$) can be expressed as [75]:

$$\overline{i^2_{nd,1}} = 4kT\gamma g_{d0,1}\Delta f \tag{5.8}$$

$$\overline{i^2_{ng,1}} = 4kT\delta g_{g,1}\Delta f \tag{5.9}$$

$$g_{g,1} = \frac{\omega^2 C^2_{gs,1}}{5g_{d0,1}} \tag{5.10}$$

where $g_{d0,1}$ is the drain-to-source conductance of M_1 at zero V_{DS}, γ and δ are the bias-dependent noise coefficients, k is the Boltzmann's constant, T is the absolute temperature and Δf is the noise bandwidth in Hertz over which the measurement is made. According to the classical two-port noise theory, the minimum noise factor F_{min} of M_1 biased in saturation (without power match) can be written as [5]:

$$F_{min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{5.11}$$

where ω_T is the frequency at which the current gain of a FET drops to unity and c is the correlation coefficient. Assume that $g_{d0,1}$ is approximately equal to $g_{1,1}$, then we have:

$$\omega_T = \frac{g_{1,1}}{C_{gs,1}} \tag{5.12}$$

Using Equation 5.10 and $g_{d0,1} = g_{1,1}$, we have:

$$g_{g,1} = \frac{g_{1,1}}{5} \left(\frac{\omega}{\omega_T} \right)^2 \tag{5.13}$$

$$\frac{\omega}{\omega_T} = \sqrt{\frac{5 g_{g,1}}{g_{1,1}}} \tag{5.14}$$

Substituting ω/ω_T into Equation 5.11, the F_{min} of M_1 can be written as:

$$F_{min} \approx 1 + \frac{2}{g_{1,1}} \sqrt{\gamma\delta g_{d0,1} g_{g,1} (1 - |c|^2)} \tag{5.15}$$

Now we start to analyze the noise factor of the composite structure in Figure 5.5. Van der Ziel's noise model can also be used for M_{1a} which is in weak inversion, where $g_{d0,1a}$ can be written as [72]:

$$g_{d0,1a} = \frac{I_D}{\Phi_T} \tag{5.16}$$

where I_D is the drain current of M_{1a} in weak inversion and Φ_T is the thermal voltage kT/q. The boundary between weak and strong inversion for M_{1a} is defined as [5]:

$$V_{GS,1a} = V_{ON} = V_{TH,1a} + \frac{nkT}{q} \tag{5.17}$$

which means that $V_{GS,1a}$ needs to be nkT/q larger than $V_{TH,1a}$ for M_{1a} to work in strong inversion, where n is a value in the range of 2-4. The drain current of M_{1a} at V_{ON} is usually called I_{ON}. With the definition of I_{ON}, the drain current of M_{1a} in weak inversion can be readily written as [5]:

$$I_D = I_{ON}\left[\exp\left(\frac{qV_{od,1a}}{nkT} - 1\right)\right] \tag{5.18}$$

where $V_{od,1a}$ is the gate overdrive voltage of M_{1a} which equals to $V_{GS,1a} - V_{TH,1a}$.

As we can see, since M_{1a} works in weak inversion, its DC current I_D is usually much smaller than that of M_1. Therefore, in order to simplify our analysis, we can make a few assumptions. First, we can ignore $\overline{i^2_{nd,1a}}$ since it is proportional to I_D. Second, since $g_{1,1a}$ is much smaller than $g_{1,1}$, we can assume that the transconductance of the composite structure equals $g_{1,1}$. However, we must take $\overline{i^2_{ng,1a}}$ into consideration because it is inversely proportional to I_D. The induced gate noise of M_{1a} increases the portion of the total induced gate noise and it is unrelated to the drain current noise of the composite structure. Thus, the unrelated induced gate noise current of the composite structure can be written as [72]:

$$\overline{i^2_{nu}} = 4kT\Delta f\delta g_g(1 - |c|^2) \tag{5.19}$$

$$= 4kT\Delta f\delta_{1a} g_{g,1a} + 4kT\Delta f\delta_1 g_{g,1}(1 - |c|^2) \tag{5.20}$$

$$\delta g_g(1 - |c|^2) = \delta_{1a} g_{g,1a} + \delta_1 g_{g,1}(1 - |c|^2) \tag{5.21}$$

where δ and g_g represent the corresponding parameters of the composite structure. Suppose that M_1 and M_{1a} have the same γ and δ, the minimum noise factor of the composite structure (F'_{min}) can be calculated as:

$$F'_{min} \approx 1 + \frac{2}{g_{1,1}}\sqrt{\gamma\delta g_{d0,1}\left[g_{g,1a} + g_{g,1}(1 - |c|^2)\right]} \tag{5.22}$$

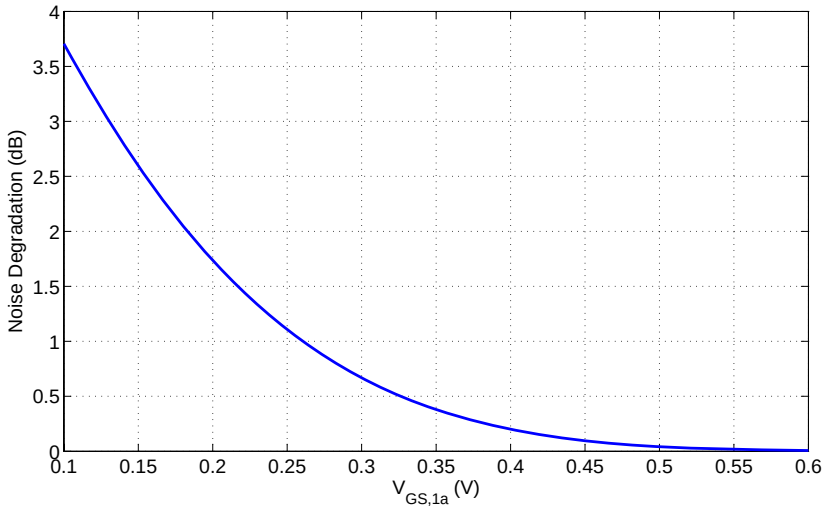

Figure 5.6: The Noise Degradation as a function of $V_{GS,1a}$

where $g_{g,1a}$ can be written as:

$$g_{g,1a} = \frac{\omega^2 C_{gs,1a}^2}{5g_{d0,1a}} = \frac{\omega^2 C_{gs,1a}^2 \Phi_T}{5I_{ON}\left[\exp\left(\frac{qV_{od,1a}}{nkT} - 1\right)\right]} \tag{5.23}$$

Based on Equation 5.7, we can calculate the Noise Degradation (ND). From Figure 5.3, we can see that $g_{1,1}$ equals 0.025 A/V. Suppose that M_1 and M_{1a} are of identical sizes and $g_{d0,1}$=$g_{1,1}$, we can plot ND as a function of the gate-to-source voltage of M_{1a} ($V_{GS,1a}$), as shown in Figure 5.6. It is clear that as $V_{GS,1a}$ decreases, ND increases rapidly. Therefore, we need to choose a relatively large $V_{GS,1a}$ which ensures that M_{1a} works in weak inversion ($V_{GS,1a} \leq V_{TH,1a}$=0.43 V), while introducing a small Noise Degradation. For example, in this particular case, we are able to keep the ND below 0.5 dB by choosing $V_{GS,1a}$ larger than 0.35 V.

5.3.3 Effect of Out-of-Band Terminations

As discussed in Section 5.3.1, a significant improvement of IIP3 can be achieved by setting $g_{3,1} = -g_{3,1a}$ so that g_3 of the composite structure in Figure 5.4 will be 0. However, the third-order intermodulation distortion (IMD3) introduced by the

combination of g_2 and harmonic feedback then becomes dominant when g_3 is small. The second-order transconductance g_2 generates the second-order product, which is then mixed with the fundamental tones to produce the third-order products [74]. Thus, in order to further increase IIP3, we need to consider the role of g_2 and harmonic feedback.

Meanwhile, g_2 is also critical in direct-conversion receivers (DCRs) and low-IF receivers. In addition to 1/f noise and DC offset, one of the major design issues in DCRs is the second-order intermodulation distortion (IMD2). For wireless systems where a direct-conversion receiver or a low-IF receiver is used, a high IIP2 (and hence a small g_2) is required [76].

In the ideal case when the circuits and signals are perfectly matched, IMD2 should not be present in a double-balanced Gilbert cell mixer. However, all asymmetries and nonlinearities in the RF input signal, the LO signal and the mixer itself in practical applications do generate IMD2 even in a double-balanced mixer [77]. The asymmetries in the mixer may include the differential input pair, the switch transistors and the load resistors. For simplicity, we only consider the mismatches of g_2 of the differential input transistors in this section, namely the mismatches between $g_{2,1}$ and $g_{2,2}$ as in Figure 5.2.

Suppose that we do a two-tone test with two slightly different input frequencies ω_1 and ω_2. The effect of out-of-band terminations on third-order intermodulation distortion (IMD3) can be expressed as follows [78]:

$$IIP3(2\omega_1 - \omega_2) = \frac{1}{6Re[Z_s(\omega)]\,|H(\omega)|\,|A_1(\omega)|^3\,|\epsilon(\Delta\omega, 2\omega)|} \tag{5.24}$$

$$\Delta\omega = \omega_1 - \omega_2 \tag{5.25}$$

where $\epsilon(\Delta\omega, 2\omega)$ can be written as:

$$\epsilon(\Delta\omega, 2\omega) = g_3 - g_{\prime} \tag{5.26}$$

and $g_{\prime}$ can be written as:

$$g_{\prime} = \frac{2g_2^2}{3}\left[\frac{2}{g_1 + g(\Delta\omega)} + \frac{1}{g_1 + g(2\omega)}\right] \tag{5.27}$$

where Z_s represents the source impedance, and $g(\Delta\omega)$ and $g(2\omega)$ are the conductance functions to be defined at the subharmonic frequency of $\Delta\omega$ and the second-order harmonic frequency of 2ω. $H(\omega)$ is related to equivalent IMD3 voltage to the IMD3 response of the drain current nonlinear term, and $A_1(\omega)$ is the linear transfer function for the input voltage of v_{gs}. $\epsilon(\Delta\omega, 2\omega)$ shows how the second-order nonlinearities contribute to the IMD3 response. And $g_{\prime}$ comes from the multiple feedbacks in the circuit mainly by the gate-drain capacitance C_{gd}.

From Equation 5.26, we can see that by making g_3 of the composite structure equal 0, we can indeed improve IIP3. However, as g_3 becomes small, $g_{\prime}$ dominates $\epsilon(\Delta\omega, 2\omega)$ and is proportional to the square of g_2. As a result, we cannot get a significant improvement of IIP3 by further reducing g_3.

According to Equation 5.27, we can reduce $g_{\prime}$ by increasing $g(\Delta\omega)$ and $g(2\omega)$. Since $g(\Delta\omega)$ is usually much larger than $g(2\omega)$, it is more desirable to increase $g(2\omega)$. In a common-source configured FET, $g(2\omega)$ is given by [74]:

$$g(2\omega) = g_1\frac{1 + 2j\omega C_{gs}Z_1 + 2j\omega C_{gd}Z_2}{1 + \omega_T C_{gd}Z_2} \tag{5.28}$$

where Z_1 is the impedance looking into the signal source and is usually on the order of $1/(\omega C_{gs})$, and Z_2 is the impedance looking into the load. For our particular design, g_1=0.025 A/V, ω=$2\pi \times 1$ GHz, ω_T=$2\pi \times 100$ GHz. Suppose that C_{gd} equals 0.1 pF, we can plot the magnitude of $g(2\omega)$ as a function of Z_2 (Ω) as shown in Figure 5.7.

It is clear that as Z_2 decreases, $g(2\omega)$ increases rapidly. Therefore, a small load

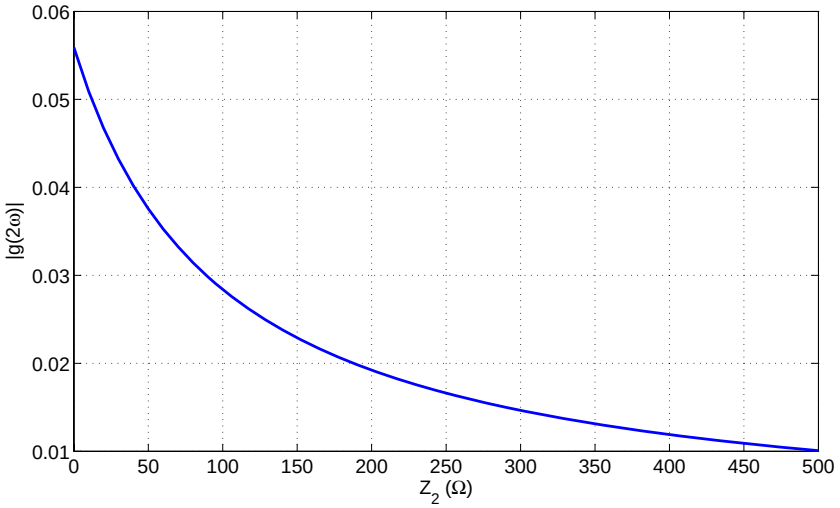

Figure 5.7: $|g(2\omega)|$ as a function of Z_2

impedance Z_2 is desired to achieve a high IIP3. A number of ways have been proposed to create a low impedance at the drain node of M_1 and M_{1a}. In [78], the author used harmonic tuning to reduce Z_2. In [74], a cascade transistor M_c was put at the drain node, which reduced Z_2 to $1/g_{1,c}$. By increasing the size of M_c, a relatively small Z_2 was achieved.

In our design, since our target is to linearize a pre-existing mixer, we cannot change Z_2 by modifying the mixer core. But we have the freedom of making use of the impedance looking into the source node of the current sources (M_5 and M_6) in the DS circuit, as shown in Figure 5.1. By increasing the size of M_5 and M_6, we can effectively reduce Z_2 in our design. However, as the impedance looking into the source of M_5 and M_6 decreases, more loss is introduced and the conversion gain of the mixer will decrease. Therefore, we need to find a balance between conversion gain degradation and IIP3 improvement.

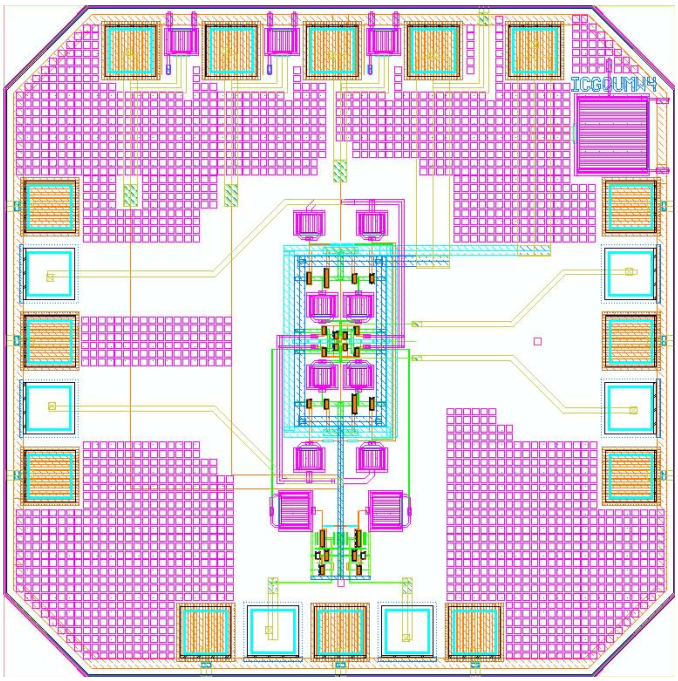

Figure 5.8: The layout of the chip in Virtuoso

5.4 Simulation Results

In this section, the simulation results of the mixer chip after post-layout extraction will be given. The layout and extraction of the chip were performed in Cadence, while the simulations were performed in Agilent ADS. Figure 5.8 shows the layout of the chip in Cadence Virtuoso.

The proposed mixer in Figure 5.1 was fabricated using IBM 0.13-μm CMOS technology, which has 8 metal levels including 3 thin metal layers, 2 thick metal layers and 3 RF metal layers. It occupied a die area of 0.2 mm $\times$ 0.5 mm without bonding pads and 1 mm $\times$ 1 mm with bonding pads.

In order to verify the effectiveness of the proposed DS technique, we simulated the circuit as shown in Figure 5.1. By turning the DS circuit on (normal bias) and off (set $V_{GS,1a}$ and V_{bias} to 0 V), we could compare the performance of the mixer with and without linearization.

The DC simulations were first performed in Aglient ADS. Simulation results

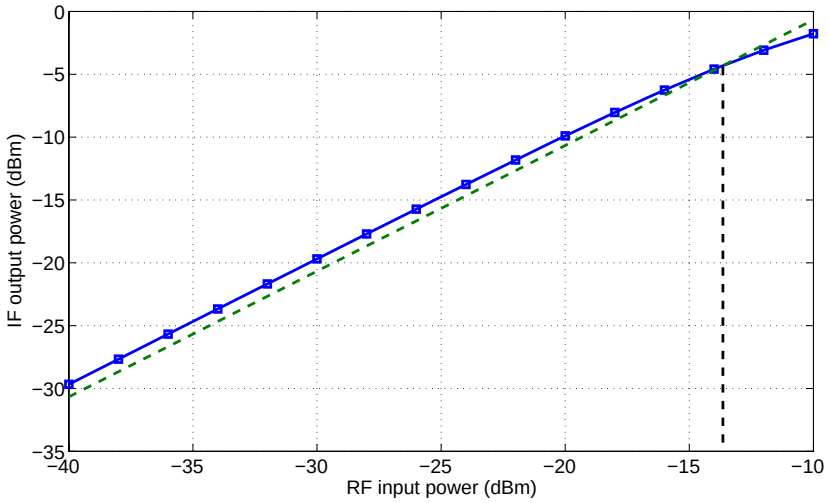

Figure 5.9: The P1dB of the linearized mixer

showed that the mixer consumed a DC current of 4.6 mA with a 1.2 V voltage supply when the DS circuit was turned off, while the mixer consumed a DC current of 5.4 mA with the same voltage supply when the DS circuit was on. Thus, the additional power consumption introduced by the DS circuit was only 17.4%.

To simulate the conversion gain of the mixer, the RF frequency was set to 1 GHz, and the LO frequency was set to 800 MHz. The simulated conversion gain of the mixer was 10.7 dB when the DS circuit was off, and reduced to 10.4 dB when the DS circuit was on. The P1dB of the mixer with linearization was -13.5 dBm, as shown in Figure 5.9.

In order to test the IIP3 of the mixer, a two-tone test was performed also in Agilent ADS. The two RF input frequencies f_1 and f_2 were set to 1000.5 MHz and 999.5 MHz. The LO frequency was set to 800 MHz. The simulated IIP3 of the mixer when the DS circuit was off is shown in Figure 5.10, and the simulated IIP3 of the mixer when the DS circuit was on is shown in Figure 5.11. It is clear that the modified DS technique improved the IIP3 of the mixer by 12.5 dB. At higher input power levels, the slope of the measured IMD3 is larger than 3:1, which indicates that IMD3 is dominated by the higher odd-odder nonlinearities (e.g. the fifth-order nonlinearity). If the third-order

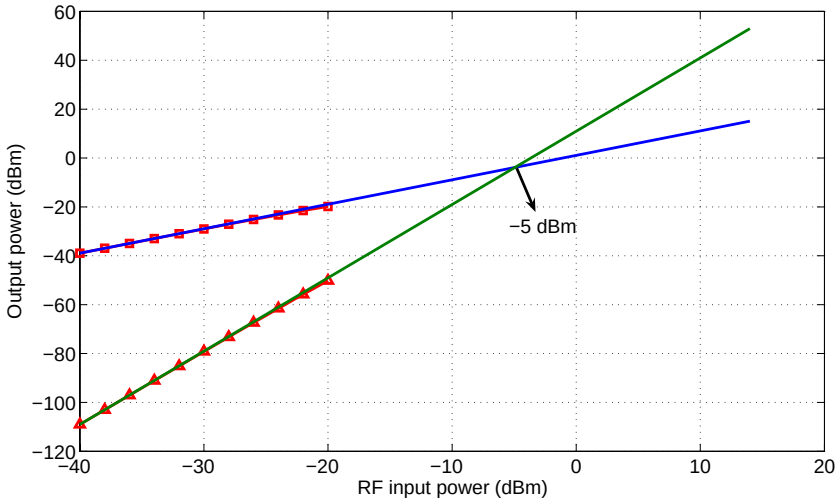

Figure 5.10: The measured IP3 of the mixer when the DS circuit was off

nonlinearity was completely canceled, the slope 3:1 would not exist and IIP3 would be meaningless [72].

Figure 5.12 shows the IIP3 improvement introduced by the DS technique as a function of the gate-to-source voltage of M_{1a} ($V_{GS,1a}$). As we can see, the IIP3 improvement was sensitive to bias conditions. Thus, in practical applications, a bias circuit with calibration techniques might have to be used.

Figure 5.13 shows the simulated isolations of the mixer when the DS circuit was on. As we can see, when the RF input power increased from -40 dBm to -10 dBm, the RF-to-IF isolation was approximately 70 dB and the LO-to-IF isolation was approximately 60 dB. The LO-to-RF isolation, which is important in direct conversion receivers (DCRs) and low IF receivers, was larger than 80 dB.

To check the Noise Degradation (ND) introduced by the DS circuit, a noise figure (NF) simulation was performed. Simulation results showed that the double sideband noise figure (DSB NF) of the mixer was 10 dB when the DS circuit was off, while the DSB NF of the mixer when the DS circuit was on was 10.7 dB. Therefore, the DS circuit introduced a ND of 0.7 dB. Since in a typical receiver, there is an LNA proceeding the mixer which usually has a voltage gain in the range of 10-20 dB, the

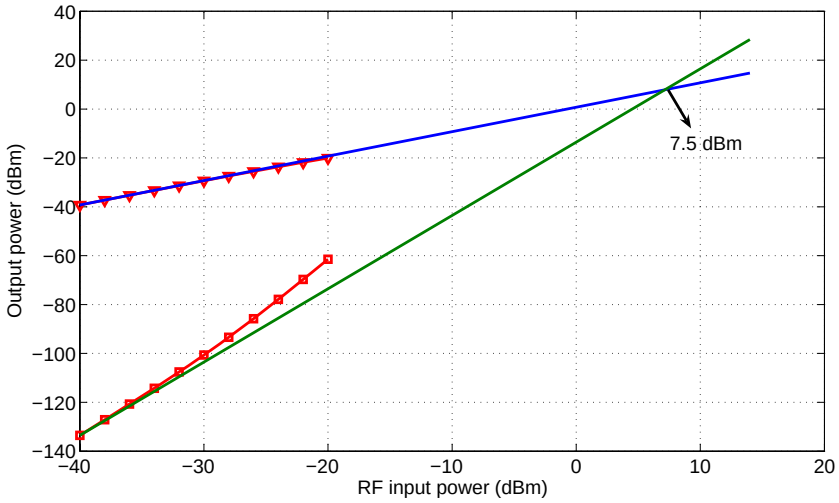

Figure 5.11: The measured IP3 of the mixer when the DS circuit was on

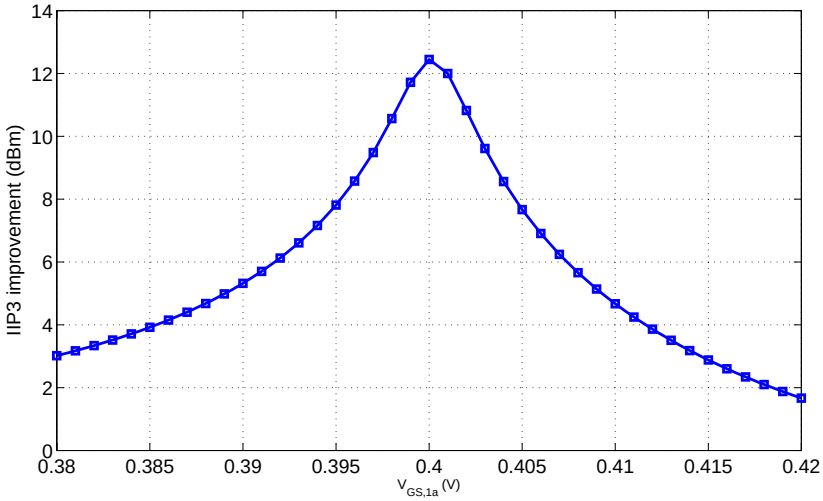

Figure 5.12: The IIP3 improvement as a function of $V_{GS,1a}$

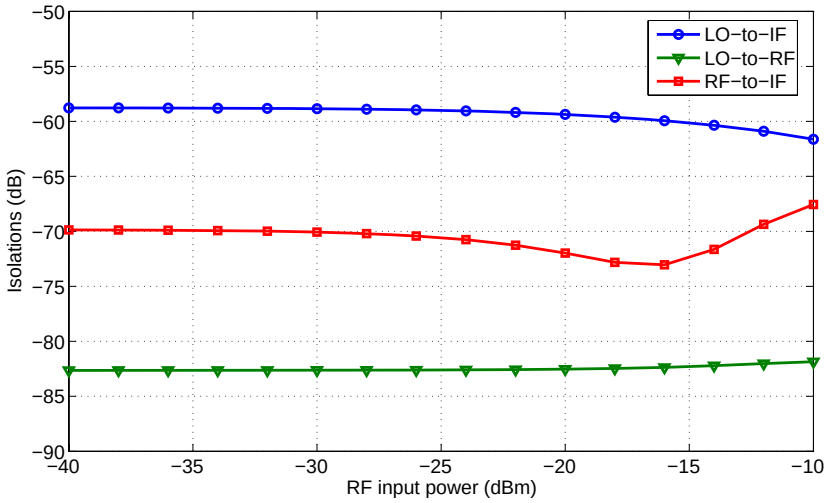

Figure 5.13: The isolations of the mixer

ND of the receiver will be much smaller than 0.7 dB.

5.5 Conclusions and Future Work

In this chapter, a modified derivative superposition (DS) technique was used to linearize a Gilbert cell mixer. Compared with traditional DS techniques, the advantage of the topology proposed in this chapter is that it can linearize a pre-existing mixer without significantly changing it. Post-layout simulations showed that the proposed DS technique increased the IIP3 of the mixer by 12.5 dB at 1 GHz, while the NF increased by only 0.7 dB and the conversion gain decreased by only 0.3 dB. The mixer consumed a DC current of 4.6 mA without the DS circuit and 5.4 mA with the DS circuit, both under a supply voltage of 1.2 V. The mixer occupied an active area of 0.2 mm $\times$ 0.5 mm.

The future work will concentrate on two areas. First, we will try to implement this technique on higher frequencies, such as the 5 GHz band. Second, we will try to make the circuit less sensitive to bias conditions.

Chapter 6

Conclusions and Future Work

6.1 Summary

The mixer is one of the essential components in a transceiver. It performs the frequency translation both in the receiver and in the transmitter. In a typical receiver, it basically determines the linearity of the system and also has a big impact on the noise performance of the system. Still in a receiver, the image-rejection mixer performs the image-rejection and greatly alleviates the need for additional on-chip or off-chip filtering. While in a transmitter, the mixer performs the frequency up-conversion and single-sideband modulation at the same time. Therefore, the design of high-performance mixers is crucial to modern transceivers.

In this thesis, three different types of mixers were designed, which focused on different applications of mixers in modern transceivers, including a broadband down-converter mixer with variable conversion gain, an upconverter mixer with sideband selection and a downconverter mixer with high linearity.

The first chip demonstrated in this thesis was a broadband downconverter mixer with variable conversion gain. A modified shunt peaking technique was used which extended the bandwidth of the mixer to 8 GHz (from 2 to 10 GHz). In order to control the conversion gain of the mixer, the transistor size switching technique was

employed. By changing the effective transistor size of the transconductor stage, the mixer was able to work in three different modes with different conversion gain and power consumption, namely, Mode 1, Mode 2 and Mode 3. In Mode 1, the mixer had the highest conversion gain and power consumption; while in Mode 3, the mixer had the lowest conversion gain and power consumption. Within each mode, the conversion gain could be further controlled by changing the load of the mixer.

The second chip designed in this thesis was an upconverter mixer with sideband selection (Chapter 4). Compared with conventional upconverter mixers in a transmitter which generate only one sideband, the mixer in Chapter 4 allowed the user to select the sideband of interest to be transmitted, namely, the upper sideband (USB) or the lower sideband (LSB). The mixer chip was fabricated in 0.13-μm CMOS technology. It occupied a small chip area (0.5 mm^2) and had a low DC power consumption, while achieving a relatively high conversion gain and linearity. The best sideband rejection was 30 dB, which is comparable to other upconverter mixers. To further improve the sideband rejection, there are several possible approaches. First of all, since the sideband rejection is directly related to the mismatches of quadrature signals, more polyphase shifters can be put in cascade to provide more accurate quadrature IF and LO signals. Alternatively, on-chip quadrature oscillators can be used to generate LO signals. Second, more careful layout can yield a better sideband rejection because the sideband rejection is also related to mismatches of circuits.

Chapter 5 presents the last chip designed in this thesis which was a downconverter mixer with high linearity. It used a modified derivative superposition (DS) technique to linearize a Gilbert cell mixer. Unlike the conventional DS technique where the DS circuit is embedded in the mixer circuit itself, the modified DS technique proposed in Chapter 5 utilized capacitive coupling between the DS circuit and the mixer transconductor. Therefore, it had the advantage of linearizing a pre-existing mixer without changing its bias conditions. Post-layout simulation results suggested an

IIP3 improvement of 12.5 dB, at the cost of very small degradation in conversion gain, noise figure and power consumption. The resulting chip was very compact (0.2 mm $\times$ 0.5 mm). Although a large improvement in IIP3 was achieved using the modified DS technique, the result was relatively sensitive to the gate-to-source voltage (V_{GS}). Therefore, further work needs to be done to decrease the sensitivity to bias conditions.

6.2 Future Work

The future work will concentrate on two areas:

First, the DS technique used in Chapter 5 was at relatively low frequency (1 GHz). To make this technique more attractive, we will try to implement this technique at higher frequencies (such as the 5 GHz band) or even broadband. In addition, as the simulation results suggested, the DS technique was very sensitive to bias voltages which hinders its practical applications. Therefore, another direction of future work will be to reduce the sensitivity of the DS technique to bias conditions.

Second, the design of low voltage mixers with high linearity is another concentration of future work. The demand for high-performance broadband transceivers is increasing. However, as the supply voltage scales down from one generation to the next, it is becoming more and more challenging to design mixers with high linearity and low power consumption. Since mixers usually determine the linearity of the receiver chain, it is of great value to design low voltage mixers with reasonably high linearity.

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