Reliability Evaluation of Fully Depleted SOI (FDSOI) Technology for Space Applications.

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Table of Contents

		page no.
1.0	Introduction	5
2.0	SOI Technology	6
2.1	SOI Materials and Processes	6
2.2	SOI Lateral Isolation	7
2.3	SOI Defects and Issues	8
2.4	SOI MOSFET Transistors	9
3.0	SOI Reliability Issues	11
3.1	Self-Heating Effects	12
3.2	Hot Electron Effects	14
3.3	Radiation Effects	14
4.0	FD SOI Technology	15
4.1	MIT/LL SOI Process	15
4.2	MIT/LL Multiprojects Achievements	16
5.0	SOI Reliability Test Structures	17
5.1	MIT/LL Test Structures for FDSOI Technology and Process Controls	18

5.2 MIT/LL MOS Technology Testing 22

6.0 MIT/LL FD FET Reliability Characterization Test Results 24

6.1 Hot Carrier Effects Test Results 24

6.2 Radiation Effects Testing 25

6.3 Effects of Temperature 25

7.0 Conclusions 26

References 27

Listing of Tables

Table 1 MIT/LL SOI CMOS Multiproject Fabrication Runs 15

Table 2 Reticles Used in SOI FD CMOS Fabrication 16

Table 3 Groups and Types of Reliability Testing Using Test Structures 18

Table 4 Snake-Comb Ladder Structures Available 19

Table 5 Contact/Via Chain Test Structures 20

Table 6 P- and N- Channel Transistors Available 21

Table 7 Sidewalk Edge Measurement MOS Transistors 22

Table 8 MOS Transistor Parameter Measurements 23

Listing of Figures/Schematics

Figure 1 Design comparison: SOI (left) and bulk-Si (right) CMOS transistors 29

Figure 2 Design comparison: PD (left) and FD (right) SOI CMOS transistors 29

Figure 3 FD SOI FET cross section, SEM view 30

Figure 4 Subthreshold characteristics of the FDSOI FET 30

Figure 5 Layout (top) and an optical view (bottom) of the MIT/LL test chip matrix 31

Figure 6 Schematic and optical view (~ 100X) of a snake-comb-ladder test chip. Insert shows close-up of the corner area (~ 1000X) 31

Figure 7 Schematic (a) and optical views (b, c, d) of different contact/via chain test chips 32

Figure 8 Schematic (a) and optical views of a sheet resistance and line width test chip (b, c) 32

Figure 9 Schematic and optical views of two FDSOI MOS transistors with different channel widths 33

Figure 10 FDSOI transistors with H-gate (a, b) and circular gate (c, d) for sidewall effect testing 34

1.0 Introduction.

In a conventional, bulk-Si microcircuits, the active elements are located in a thin surface layer (less than 0.5 μm of thickness) and are isolated from the silicon body with a depletion layer of a P-N junction. The leakage current of this P-N junction exponentially increases with temperature, and is responsible for several serious reliability problems. Excessive leakage currents and high power dissipation limits operation of the microcircuits at high temperatures. Parasitic n-p-n and p-n-p transistors formed in neighboring insulating tubs can cause latch-up failures and significantly degrade circuit performance.

Silicon-on-insulator (SOI) technology employs a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick (hundreds of nanometers) layer of silicon oxide. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures. Figure 1 shows schematic cross sections of the bulk-Si and SOI CMOS transistors.

SOI technology simplifies manufacturing process by eliminating well and field implantation steps and allows fabrication of smaller, denser, and faster microcircuits, with reduced interconnect cross-talk. These features make SOI technology particularly attractive in emerging system-on-chip microcircuits, micro-electromechanical systems (MEMS), and integrated optics applications. Dielectric isolation in SOI also helps in decoupling the analog and digital components in mixed-signal microcircuits by reducing the substrate cross-talk [1]. Another appealing aspect of SOI technology is its compatibility with the standard semiconductor fabrication.

Some examples of the VLSI devices successfully manufactured on SOI materials are: fully functional 16 Mbit DRAMs (16 million transistors), 4 Mbit SRAMs (24 million transistors) and 533 MHz microprocessor (3 million transistors, BICMOS) [2]. Recently, models for circuit simulation (SPICE-like models) have been developed for partially depleted (PD) SOI technology, and several high-performance RISC microprocessors have been designed and built by IBM to commercial specifications [3]. IBM S400 machine, which began shipping this year, utilizes microprocessor manufactured in 0.22 μm process SOI technology.

In spite of more than 20-year history and promising benefits, SOI technology has not captured any substantial portion of the commercial market. However, it does remain an emerging technology with a high future potential. There are several factors that have impeded the introduction of SOI technology into the mainstream. One of them has been the availability, cost, and quality of SOI materials. These materials should have a thin, defect-free silicon layer with high thickness uniformity and a high quality of buried oxide. Wafer supply was a limiting factor several years ago, but this is becoming less of an issue with the advent of several companies that specialize in offering different types of SOI wafers.

Another problem with SOI has been the circuit design, which requires new approaches from the engineering point of view [4]. The SOI circuit designer must have better understanding of the underlying device physics and processes, which were not mandatory when designing with the bulk-Si devices. Simulation models and CAD tools for SOI design that take into consideration the floating body effects, and at the same time take full advantage of the packing density and electrical characteristics are still under development. Also, fabrication and metrology issues make the task of processing on SOI materials more difficult than on the regular bulk-Si wafers [5].

The primary motivation for developing SOI technologies was the need for radiation-hardened ICs as an alternative to expensive silicon on sapphire (SOS) technology that uses a thin film of silicon grown on an insulating Al_2O_2 substrate. A potentially high radiation tolerance of the SOI devices makes them very attractive for space applications.

A major objective of this task was to gain some experience with fully depleted SOI technology and the reliability test structures developed by Massachusetts Institute of Technology, Lincoln Laboratory (MIT/LL).

2.0 SOI Technology

Some of the major manufacturing/processing of SOI wafers related concerns such as lateral isolation, defects, and MOSFET characteristics are described below.

2.1. SOI Materials and Processes

SOI process starts with manufacturing wafers, containing a thin silicon layer above a relatively thick layer of silicon oxide. There are several approaches to manufacturing SOI substrates, and their major features are briefly described below [1],[3],[4]:

- Separation by implantation of oxygen (SIMOX) injects a high concentration of oxygen beneath the surface of a silicon wafer, typically using a dose of 2×10^{18} atoms/cm^2 at 200 keV. The implantation receives a high-temperature anneal to restore crystalline quality of the silicon layer over the buried oxide (BOX), which forms during the same heat treatment.
- A latest trend with SIMOX fabrication is to use a lower oxygen implant dose to obtain an improved, low-cost SOI material. This new approach has drastically improved the top silicon film crystalline quality, but also yields much thinner silicon and SiO_2 layers. For example, the internal thermal (ITOX) SIMOX process uses a high-energy, smaller-dose oxygen implant to produce a thick silicon layer and a thin BOX layer (~300 nm and 80 nm respectively). A subsequent anneal in oxygen oxidizes some of the superficial silicon layer and increases the thickness of the BOX.
- Separation by plasma implantation of oxygen (SPIMOX) is another potentially low-cost process for fabricating SOI substrates. In this modification of SIMOX process, oxygen is implanted by plasma immersion. The whole wafer is implanted at once, resulting in a

high wafer throughput. A potential drawback of this technique is the lack of ion beam selection and possible contamination.

- Bond and etch-back SOI (BESOI) is used to manufacture relatively thick films of both oxide and silicon. Two silicon wafers, one with an oxide layer, are bonded together using Van der Waals forces. A subsequent anneal increases the bonding strength. Finally, one side of the bonded substrate is thinned to roughly 1µm by mechanical grinding and polishing. Typically, the bonded wafers have thicker, yet better-quality, silicon and buried oxide layers compared to the SIMOX process. Analog Devices widely uses a high-speed complementary bipolar process, called XFCB (eXtra-Fast Complementary Bipolar), which is a variation of the BESOI technology, for production of commercial mixed-signal microcircuits.
- Smart Cut Technology combines ion implantation and wafer-bonding technologies. A wafer is oxidized to form the buried oxide layer of the SOI structure. A high-dose (5 x 10^{16} ions/cm^2) hydrogen ion implantation through the oxide forms cavities or microbubbles at the implantation range. This wafer is then bonded to another wafer using Van der Waals forces. A 500°C thermal activation nucleates, coercing hydrogen into the cavities and merging them, causing delamination of the top section of the wafer. The use of ion implantation for the layer separation improves the layer thickness uniformity.
- Epitaxial layer transfer (ELTRAN) produces SOI wafers with a relatively defect-free silicon film. It is formed by growing an epitaxial layer on a layer of porous silicon. This wafer is then bonded to a "handle" wafer and is either ground down or separated at the porous layer.

SIMOX is considered to be the most promising among the various SOI technologies. In spite of a seemingly destructive process, the SIMOX does result in stress-free silicon film, which enables manufacturing device-grade SOI structures. The thin silicon layer formed by this technology is a wafer-scale monocrystal with high quality and excellent electrical properties [6].

In a regular-quality SIMOX wafers, the buried oxide interfaces are sharp and uniform. However, physical properties of the buried oxides are different compared to the thermal oxide. The buried oxide is silicon-rich, which results in a high density of electron traps (strained Si-Si bonds) and E' centers (acting as traps for holes). The breakdown electrical field in good-quality BOX exceeds 8 MV/cm, which is still below the values typical for thermal oxides (in the range of 10 to 16 MV/cm).

2.2. SOI Lateral Isolation

Traditionally, lateral isolation between SOI devices is obtained by the formation of a mesa structure or by producing a thick field oxide using LOCOS (local oxidation of silicon) process.

In mesa isolation, the active device regions are masked to etch the field device areas (see Figure 1). The SOI oxide helps as the etch-stop layer, while anisotropic etching allows for an efficient isolation scaling. The weak point of this isolation technique is the sharpness of the sidewall and its potential impact on gate oxide integrity and the device subthreshold characteristics [1]. Besides, a special care should be taken to prevent the possibility of etching through a thin BOX (in some cases 100 nm), when a mesa isolation with a Si-island sidewall spacer is formed.

LOCOS isolation in SOI is much the same as the LOCOS in bulk silicon. However, the oxidation kinetics in SOI is somewhat different, particularly when the growing oxide reaches the buried oxide. The oxidation times to consume the entire silicon film can be long, resulting in transistor-width loss. It is also possible that LOCOS isolation may introduce mechanical stresses in the active region of the MOSFET, causing device leakage.

Most manufacturers of the SOI devices use the trench isolation process (or shallow trench isolation, STI) as a prime choice for lateral isolation. Shallow trench isolation needs to be modified compared to conventional bulk-Si process for shallower, selective to oxide etch, thinner deposited oxide and shorter chemical-mechanical polishing (CMP) cycles.

2.3. SOI Defects and Issues

The dominant defects detected in the SIMOX are threading dislocations, small stacking faults, which are frequently observed at the bottom of the Si overlay, and the BOX defects, which can lead to leakage currents [2].

These BOX defects are typically silicon inclusions, bridging defects (or "pipes") and interface undulations in the SIMOX material. Two factors contribute to these defects: (1) the presence of particles on the wafer surface, locally masking oxygen ion implant, and (2) local kinetics of BOX formation during the implantation and annealing process. Crystalline silicon inclusions and islands are often encountered at the bottom of the oxide (see Figure 3), reducing its effective thickness and hardness.

A thin SOI film has several characteristic defects: stacking faults, inclusions, and threading dislocations. The dislocations are not known to pose a performance or reliability risk in CMOS devices on SOI. The stacking faults are usually small, comparable to those found below the BOX, and located near the SOI/BOX interface. They are unlikely to have serious impact on the devices; however, they have been found to contribute to the transistor leakage when their size encroaches on the junction area. The inclusions, manifesting themselves as, so-called HF defects, when their size spans the full thickness of the SOI film, are considered killer defects when located under the gate area. Their origin is related to large oxygen precipitates, or BOX "upwelling" to the top of the wafer. These defects could be caused by particles locally masking oxygen implant, or heavy precipitation of metal contamination during high temperature processing that forms the HF-soluble silicides.

Dopant diffusion in thin SOI film can be different than in the bulk-Si process. This factor, as well as some implant dose loss into the BOX for very thin SOI films, and dopant segregation into the buried oxide may require modification of the implantation regimes and the thermal processes.

Silicidation of very thin SOI film (typical for fully depleted SOI technology) with large amounts of refractive metal may lead to over-consumption of silicon and form voids at the source/drain and channel boundary, which may also result in the formation of silicide under the gate area.

Therefore, extreme precautions have to be taken during the front-end processing because of the limited amount of silicon on the top surface of an SOI substrate. This thin silicon layer can be easily removed by extensive wet or dry etches or oxidation.

2.4. SOI MOSFET Transistors

The major difference between a bulk-Si MOS transistor and a SOI MOS transistor from the circuit designer point of view is that the later has smaller junction capacitance and has a floating body [4]. These are some other effects and characteristics associated with SOI MOSFETs:

- **Floating-Body Effects**

Floating body effect (FBE) is the major parasitic effect in SOI-MOSFETs and is a consequence of the complete isolation of the transistor from the substrate. The effect is related to the built-up of a positive charge in the silicon body of the transistor, originating from the holes created by impact ionization. This charge can not be removed rapidly enough, primarily because no contact with the Si film (body) is available.

There are various consequences of this built-up charge, which are generally referred to as the floating-body effects, such as [5]: kink-effect; negative conductance and transconductance; hysteresis and instabilities, single transistor latch (the transistor cannot be turned off by reducing gate voltage), bipolar transistor action, and premature breakdown. The FBE can lead to circuit instabilities, frequency-dependent delay time, and pulse stretching. Many of the negative consequences of the FBE could be eliminated by using a body contact for every MOSFET, but this is generally not an optimum solution.

It should be noted that these typical SOI effects can be observed even in the bulk-Si MOSFETs at low temperatures when the substrate becomes semi-insulating and if the substrate contact is left floating.

- **Edge Effects**

The lateral edges of the SOI MOSFETs represent a parasitic conduction path between the source and the drain. This sidewall transistor operates in parallel with the main transistor, and strong coupling and charge sharing between the front, back, and the edge channels dictate its threshold voltage. Special edgeless devices (e.g. H-gate transistor, which has two p+ body contacts that inhibit any conduction path along the sidewalls may be designed, but this is a space-consuming alternative [5].

■ Partially Depleted and Fully Depleted SOI FETs

Depending on the thickness of the silicon layer, MOSFETs will operate in fully depleted (FD) or partially depleted (PD) regimes. When the channel depletion region extends through the entire thickness of the silicon layer, the transistor operates in a FD mode. PD transistors are built on relatively thick silicon layers with the depletion depths of the fully powered MOS channel shallower than the thickness of the silicon layer. Figure 2 illustrates the difference between these two types of transistors [8].

The FD devices have several advantages compared to the PD devices; however, there are some drawbacks also. These are some of the tradeoffs in use of the FD versus PD SOI MOSFETs:

- Fully-depleted SOI devices are naturally free from kink effect, because the majority carriers can penetrate more easily into the source; thus, preventing the excess carriers accumulation [5].
- FD SOI has an enhanced subthreshold swing, S (see Figure 4). For the bulk and PD devices, 1/S = 85 to 90 mV/decade, and for FD SOI, 1/S = 65 to 70 mV/decade, which is close to an ideal characteristic of a MOS transistor at room temperature (1/S = 60 mV/decade) [8].
- Fully-depleted SOI devices have the highest gains in circuit speed, reduced power requirements and highest level of soft-error immunity [7]. FD devices operate faster because of a sharper subthreshold slope, and a reduced threshold voltage that allows for faster switching of the MOS transistors. These transistors also have increased drive currents at relatively low voltages.
- Several drawbacks of the FD SOI design and process come along with their benefits: Although FD MOSFETS are naturally free from the kink effect, the interface coupling effect affects their operation [5],[9]. The interface coupling is inherent to fully depleted SOI devices, where all parameters (threshold voltage, transconductance, interface-trap response etc.) of one channel are insidiously affected by the opposite gate voltage (at the buried oxide).
- While FD SOI MOSFETs offer a reduced body effect and a nearly ideal g_m/I_d ratio when biased in the weak or moderate inversion region, a weak (not fully eliminated) current-voltage kink still exists in the strong inversion region. Therefore, additional technology optimization is required to use these transistors for baseband analog applications [10].

Besides, accumulation at the back interface can lower the breakdown voltage and introduce the kink effect.

- The threshold voltage fluctuation due to SOI thickness variation is one of the most serious problems in FD SOI MOSFETs. In comparison, partially depleted SOI devices are built on a thicker silicon layer and are simpler to manufacture.
- Most design features for developing PD devices can be imported from the bulk silicon devices and used in the SOI environment with only modest changes. This makes circuit redesign for the PD devices simpler than for the FD microcircuits.

3.0 Reliability Issues in SOI Technology

3.1 Self-Heating Effects

In general, many of the reliability issues related to bulk devices such as dielectric related, conductor and metallization, hot carrier related degradation and failures are applicable to SOI technology, as well. Most new reliability issues in SOI devices, which are not known in the traditional bulk-Si devices are related to the presence of the buried oxide. In the bulk technologies, heat generated by charge transfer in the transistor is readily transferred out of the chip backside through silicon substrate. This transfer of heat is quick enough so that local device transconductance changes due to self-heating are negligible. For bulk devices with six or more layers of interconnect, the stacked inter-layer dielectrics (ILDs) present substantial thermal resistance. However, in the current generation of submicron technology bulk devices, these thermal issues are being addressed with the use of reduced dielectric constant dielectrics and higher conductivity metallization based on copper interconnect.

In SOI technology, silicon dioxide, comprises the BOX layer, so that the SOI transistor is encased in a perfect little insulated region of its own. As a result, the average junction temperature of SOI devices can be somewhat higher than for an identical bulk device, reducing the device transconductance. Since SOI transistors are thermally insulated from the substrate by the buried insulator, the removal of excess hear generated by the Joule Effect, within the device is less efficient than in the bulk devices. The excess heat has several conduction paths, diffusing vertically through the buried oxide and laterally through the silicon island into the contacts and the metallization.

Thus, SOI MOSFETs are susceptible to the local thermal heating generated in the channel due to less thermal conductivity of the buried oxide, which is approximately 100 times lower than thermal conductivity of silicon [6]. The self-heating causes a reduction of the carrier mobility, shifts the threshold voltage, and results in a negative differential conductance at high gate and drain voltages. The negative resistance, which can be seen in the output characteristics of SOI MOSFETs is due to a mobility reduction effect caused by device self-heating. This effect can compromise reliability of the part when the part is operating at low and ultra low temperatures due to thermo-mechanical stresses and possible formation of structural defects and microcracks.

In SOI devices, self-heating effect can be minimized by using a thin buried oxide film; thus, decreasing the bottom layer thermal resistance. Another advantage of this approach is the reduction of short channel effect for the back transistor. However, the back channel transistor threshold voltage is reduced if the doping level at the back channel interface is not increased. This, in combination with a floating body effect, can lead to a worst case behavior.

The self-heating effect is more pronounced in fully-depleted structures due to thinner silicon films, which means a thinner buried oxide will be required to minimize it. The limitation for thinning the buried oxide is imposed by the variations of the threshold voltage with the backgate bias. Fully depleted devices exhibit a different electrical behavior from the partially depleted devices. The threshold voltage varies with the backgate bias for enhancement mode and accumulation mode devices due to the coupling effect between the front and the back gates when the silicon film is fully depleted. As a result of this coupling effect, the threshold voltage of fully depleted devices becomes a function of the silicon and buried oxide thicknesses.

3.2 Hot Electron Effects

The vulnerability of submicron devices to hot carrier injection is well known and understood phenomenon. In a high electrical field of a short-channel transistor, carriers may gain enough energy to either be trapped at the gate oxide interface (or in the bulk of oxide) or they may create electron-hole pairs by impact ionization. Then, the generated carriers can be injected into the oxide region where they may create defects or get trapped, causing a shift in threshold voltage and degradation in transconductance and saturation current [11]-[12]. Usually, degradation of FETs is caused by several field-dependent mechanisms, which are simultaneously involved in the process of defect formation: filling of preexisting traps, generation of new oxide traps, and interface-trap production. The degradation of p-MOSFET due to hot carrier effect is less severe than that for n-channel transistors, simply because the mobility, mean-free path, energy, and ionization rate (e.g. substrate current) are substantially lower for holes than for electrons. Moreover, the oxide barrier for hole injection (4.5 eV) is much higher, so most of the degradation is still due to hot electron injection [5].

For SOI transistors, not only the gate oxide but also the buried oxide may be degraded. The BOX is more subject to degradation than the gate oxide because the high density of electron traps is an intrinsic feature of SIMOX oxides. These defects may change parameters of the back channel in FET and affect the performance of CMOS circuit through the coupling effect. Thus, the hot carrier induced degradation in SOI devices is more complex than that in bulk devices because of the thin Si- film effects and the existence of two interfaces (two oxides and two channels). It has been reported in the literature [11] that (a) the front channel of the FD transistor degrades less than that of the PD ones [12]-[13]; (b) the back channel of the FD transistors degrades much more than the front ones [14]; (c) for both the PD and FD transistors, stressing one channel may also damage the opposite channel [15]-[16]; SOI MOSFETs degrade less [12]-[13], or more [15]-[16] than their bulk counterparts. These results may appear contradictory, partly because it is difficult to establish meaningful procedures for such comparisons.

The basic concept to the understanding of hot carrier effects in SOI MOSFETs (as in bulk ones) is the impact ionization that generates e-h pairs near the drain of a device under stress, and the resulting gate and substrate currents [17]. Any of these two currents can be used as hot carrier stress monitors for NMOS devices, but the gate current is more appropriate for pMOS devices [18]. Several studies have been performed for hot carrier stress testing in PD SOI devices to investigate degradation of both channels.

A hot carrier effects study was conducted on lightly doped drain (LDD) FD SOI devices with channel length down to 0.8 μm [19], and the following process parameters:
t_{ox1} = 15 nm; t_{ox2} = 400 nm; t_{Si} = 140 nm; and $N_A = 4 \times 10^{16} cm^{-3}$. These devices were subjected to 10^4 s stresses consisting of various combinations of bias voltages V_D, V_{G2} and V_{G1}, and the degradation of both channels was measured. Following the front channel stress, the front channel showed very little degradation (delta V_{T1} = 2 mV, delta g_{mi} < 1 %), and there was no change in the back channel. After various back channel stresses, the back channel degraded significantly (delta V_{T2} = 0.5 to 2 V), but much less for PD devices, and there was no change in the front channel.

A detailed study was also conducted on FD non-LDD devices with channel length 0.25 μm upward [20], and following process parameters:
t_{Si} = 70, 100 and 180 nm
$N_A = 5 \times 10^{16}$, 1×10^{17}, and 3×10^{17} cm^{-3}
t_{ox1} = 10.8 nm
$_{tox2}$ = 360 nm
The gate current was measured to monitor the electric field. It was observed that the worst case degradation occurred when stressing at $V_G – V_T$ = 0.15 V, and not at $V_G = V_D/2$, as is the case for bulk devices. It was also found that the extent of degradation depends upon the state of the back channel (i.e., accumulation, depletion) during stress. A significantly reduced gate current was observed for all SOI devices in comparison to the bulk, with the thinnest FD device exhibiting the least gate current.

A new approach was used for hot carrier reliability evaluation in FD SOI devices fabricated on SIMOX substrate [21]. Measurements were made of the front gate threshold voltage shift, and dc-coupled front and back gate threshold voltage shifts by accumulating the opposite interface. Experimental results were used to analyze the effect of floating body, bipolar breakdown and series parasitic source/drain resistance (R_{ds}) debiasing on hot carrier degradation. In this study, NMOS transistors with n^+ poly gates fabricated on SIMOX substrate were used. These devices had front gate oxide (t_{fox}) and buried oxide thickness (t_{box}) of 12 nm and 400 nm, respectively. SOI film thicknesses were 75 nm. Effective channel length and R_{ds} were 1.2 μm and 37 ohm, respectively. The drain bias was varied from 3.5 V to 5.5 V to include effects such as floating body, bipolar turn-on and series parasitic source/drain resistance effects. The devices were stressed at each drain bias for 6 hours.

The test results showed that at low V_{ds}, device degradation is due to the coupling of back interface degradation to the front interface with low front interface trap generation. At moderate V_{ds}, floating

body induced shift in threshold voltage is dominant, despite moderate front interface states generation. At high V_{ds}, interface state generation at the back interface, and the competing hole trapping and interface state generation at front interface are observed. However, due to floating body effect, back interface degradation is weakly coupled to the front interface.

The PD transistors under hot carrier stressing appear to degrade more than the FD ones, which in turn degrade more if the back channel is kept accumulated during stress. The worst case stress condition in FD devices occur at the gate voltages just above threshold. It is expected that thinner FD transistors with carefully engineered drains should exhibit improved resistance hot carriers down to very short channel lengths. However, abnormally high degradation has been predicted and observed when the channel length goes into 0.1 μm range.

For FD SOI devices, stressing the front channel may also stress the back interface, and the threshold voltage shift can be affected by the charges trapped in the opposite oxide due to interface coupling effect [22]. It has been reported that the back interface of FD P-channel SIMOX transistor degrades much more than the front one [23], due to the poor electrical properties of the buried oxide (BOX) formed by oxygen implantation. A new SOI material technology "Smart Cut" has been recently developed for the fabrication of Unibond wafers, which combines hydrogen implantation and wafer bonding [24]. A good uniformity of silicon layer without any defects and a very sharp bonded interface have been obtained from this technology.

3.3 Radiation Effects

SOI devices have excellent tolerance to the transient radiation effects (far better than bulk-Si parts). A still unsolved problem is the permanent radiation damage related to the cumulative dose effects.

Experiments on SOIFETs show that in most cases the gate oxide under radiation conditions behaves normally. If properly made and free of defects, gate oxides for SOI devices tend to have a level of reliability similar to that of bulk-Si.

However, buried oxides usually are much more vulnerable to electron trapping [5]. Typically, the SIMOX is an ultra-dry oxide where the traps are presumably related to the high density of oxygen vacations. Since most of the defects are accumulated into the buried oxide (because it is thicker and has more initial structural defects compared to the gate oxide), this oxide usually decreases radiation tolerance of the device.

4.0 FD SOI Technology

4.1 MIT/LL SOI Process

The MIT/LL SOI process was designed to manufacture fully depleted SOI CMOS microcircuits. The development of this technology was funded mostly by DAPRA, initiated on April 1995 and was realized during three Mutiproject fabrication runs. More than 29 different circuit design groups from 19 different organizations participated in these projects (see Table 1).

The purpose of these Multiprojects was to make the product available for non-competitive research, low-power-circuit design community. Additional objectives of this Multiprojects funding were [8],[25]:

- Development of design rules and extraction of SPICE models;
- Integration of designs onto common reticle set;
- Development and characterization of process monitors;
- Distribution of test data and dissemination of fabricated chips to researchers.

Table 1. MIT/LL SOI CMOS Multiproject Fabrication Runs

Run	Fab Comp. Date	Participants		
		Industry	Government Laboratories	Universities and Nonprofits
I	September 1996	Boeing, DEC, Honeywell, Irvine Sensors, Lucent, Rockwell	Lincoln Laboratory, NASA JPL, NIST, and Phillips Laboratory	ASU, Georgia Tech, Mayo, MIT, UC Berkeley, Stanford
II	July 1998	Boeing, DEC, Honeywell, Irvine Sensors, Lucent, Nortel, and Rockwell	Lincoln Laboratory, NIST, NASA/JPL, NSA, and Phillips Laboratory	ASU, Berkeley, Cal Tech, CMU, MIT, Northeastern, Mayo Foundation
III	April 99	AIL, Boeing, Honeywell, Lucent, Raytheon	Lincoln Laboratory, NASA/JPL	ASU, Berkeley, Cal Tech, Notre Dame, OSU, USC, Mayo Foundation

During the second and third design/fabrication runs, the process was optimized and a variety of different devices were fabricated for different customers/participants.

The developed baseline process was designed to manufacture microcircuits for low power, high performance applications and features the following characteristics:

- 0.25 μm fully depleted silicon-on-insulator (FDSOI) process with no body contacts;
- 50 nm thick active silicon layer with mesa isolation;
- 0.25 um drawn, dual-doped polysilicon gates with 25 nm Ti-capped cobalt salicide process;

- 100-200 nm buried oxide;
- Aluminum damascene stacked contact and via plugs;
- Fully planar 3-level metal interconnect;
- 150 mm wafer diameter.

The developed process employs 11 steps of photolithography and 8 reticles listed in Table 2.

Table 2. Reticles Used in SOI FD CMOS Fabrication

Level	Reticle	Description
1	Active Area	Defines n and p Transistor Islands
2	p-Channel Mask	Implant n-Channel Island Sidewalls
3	n-Channel Mask	Implant p-Channel Island Sidewalls
4	p-Channel Mask	n-Channel Threshold Adjust Implant
5	n-Channel Mask	p-Channel Threshold Adjust Implant
6	Polysilicon Gate	Define Polysilicon Gates and Interconnect
7	n+ Implant	Implant n+ Source and Drains
8	p+ Implant	Implant p-Channel Drift Regions (Sidewall Spacer Formation)
9	p+ Implant	Implant p+ Source and Drains
10	Contact Cuts	Define Source, Drain, and Gate Contacts
11	Metal 1	Defines First-Level Metal Interconnect

Figure 3 shows a cross-section of a FD SOI transistor manufactured in the MIT Lincoln Laboratory in 1998. These transistors had subthreshold characteristics with a slope of 65-70 mV/decade (see Figure 4) which is close to a theoretically expected slope of 60 mV/decade.

4.2 MIT/LL Multiprojects Achievements

The feedback of the participants after testing the Multiproject-I devices can be summarized as follows:

- Boeing. 8051A Microcontroller with 2k SRAM, operated at the limit of their tester (300 MHz) at 2 volts. The microcircuit was functional down to 0.6 volt of power supply.
- LUCENT. A digital signal processing macro circuits for wireless communication systems was operational in the range from 0.6 to 2.0 V of power supply.
- Irvine Sensors. Functional low noise mixed-mode analog and neural circuits had a speed which was limited by the test board design.
- Rockwell (Boeing). A low power (80 μW) 12 bit analog-to-digital converter had demonstrated key characteristic elements.
- Arizona State. A current mode 450 μW, 5 bit digital-to-analog converter was functional at 40 MHz with the resolution limited by power supply decoupling.
- MIT. Functional 32 bit linear feedback shift register and 8-bit array multiplier were operational at frequency of more than 100 MHz at 1 volt.

One of the results of the second multiprojects was fabrication of a fully functional data generation/acquisition circuit (DGAC) containing approximately 14,000 transistors (Mayo Foundation). The circuit was used to provide process technology benchmarking for NSA and had similar performance to Vitesse GaAs foundry (950 MHz vs. 1 GHz). However, the 0.25 µm FDSOI CMOS circuit had significantly (45 times) lower power consumption. The part was operating at V_{DD} = 2 V and the input frequency up to 1.15 GHz.

The MIT/LL 0.25 µm FDSOI CMOS compressive receiver test chip, which was also developed during the Multiproject II, contained 5000 transistors and operated at frequency of more than 1 GHz and V_{DD} = 2 V. Devices demonstrated an enhanced radiation performance for space applications.

More than 92 circuits were fabricated for 27 different government, industry and academic organizations as a part of the third DAPRA-sponsored Multiproject runs. The manufactured devices are currently under testing.

MIT/LL is planning transitioning from 0.25 µm to 0.175 µm design rules (for Multiproject IV) and is starting research on developing a 100 nm process. The developed 0.25 µm process is being transferring to a commercial DOD fabrication facility.

5.0 SOI Reliability Tests Structures

Test structures are widely used in the present day microelectronics fabrication for wafer process control, die assembly, and reliability evaluation. These structures are one of the major elements in the quality control system. They allow verification of lot-to-lot reproducibility, identify defects in the major fabrication steps to allow implementation of corrective actions.

The number and types of test structures used vary with the maturity of a given process and usually is much larger for a developing process. For example, IBM products have approximately 10% of their wafer area dedicated to “drop-in” test sites, when it is initially introduced into the manufacturing flow [26]. As the technology matures, the wafer area with test structures is reduced to about 5%.

Many test structures and test techniques for process control, such as line width measurements, contact resistance, transistor characterization, and even some reliability tests have reached the point where standards exist for these measurements [27].

Testing of the test structures is often considered as an alternative approach to the costly and time consuming standard high-reliability-assurance procedure. It allows direct monitoring of the quality of the device during manufacturing. The test chip for these purposes have to be carefully designed to identify individual failure modes and minimize the potential misinterpretation of the data.

Typical groups of test structures used to evaluate quality and reliability of the devices on the wafer level during manufacturing are shown in Table 3.

Table 3. Groups and Types of Reliability Testing using Test Structures.

Group	Reliability Testing Type
Interconnect Reliability Tests	Electromigration
	Stress migration
	Passivation integrity
Hot Carrier Injection Tests	DC HCI
	AC HCI
I/O Reliability Tests	Electrostatic discharge
	Latchup
Junction Integrity Tests	Junction leakage
Gate Oxide Integrity	Plasma process-induced damage
	Charge to breakdown
	Time-dependent dielectric breakdown
	Ionic contamination

The usage of the wafer level reliability (WLR) test structures and techniques is probably especially effective for the ASIC microcircuits designed for space applications [28]. A new ASIC design for high reliability applications can not be qualified by gathering large amounts of statistical information from field applications or from the accelerated life testing when the total number of parts to be used for the life of a spacecraft is in the order of a few hundred devices. Therefore it is essential that each individual major process step involved in the design and fabrication of the ASICs is qualified.

There are two categories of wafer level testable mechanisms. The first group has some fairly well defined test structures and test procedures, while the second group comprises mechanisms that possibly can be tested at wafer level based upon some research experience. Typical wafer level established testable mechanisms are: time dependent dielectric breakdown (TDDB); electromigration (metal and contact); hot carrier effect; ion drift; and radiation hardness. A well-designed rapid wafer level reliability test method can be a good indicator of changes in the manufacturing process and/or in used material wear-out characteristics, varying from wafer-to-wafer or from lot-to-lot.

5.1. MIT/LL Test Structures for FD SOI Technology and Process Control

One of the approaches to quality control of manufacturing highly scaled microcircuits is to use a matrix of equally spaced pads with the test devices constructed around them [29]. Several process control chips can be incorporated in the wafer and used for manufacturing

control. A probe card applied to the wafer can be then used to test any structure on the matrix.

Similar approach was used in the MIT/LL during the third Multiproject Fabrication run [30] for FD SOI CMOS technology control. A schematic and an overall view of the test matrix are shown in Figure 5. Rows and columns identify location of the test structure on the die. All test structures can be classified into six large groups, based upon their design goals and functions. These test structures are described below.

■ Snake-Comb-Ladder

Each of these test structures consists of a snake jammed between two combs. This device is used to detect metal shorts and/or voids by measuring the snake continuity and leakage between the snake and the combs. A schematic and an optical view of the test structure are shown in Figure 6.

Twelve types of these structures, which differ by size, used conductive materials, interlayer insulators, and topology of the surface, are available (see Table 4 below).

Table 4. Snake-Comb Ladder Structures Available

Location row/column	Snake	Comb	Width/Spacing, μm
1/1	N+ Island	N+ Island	0.5/0.4, 0.6/0.5
1/2	P+ Island	P+ Island	0.5/0.4, 0.6/0.5
1/3	N+ Poly	N+ Poly	0.25/0.35, 0.2/0.3
1/4	P+ Poly	P+ Poly	0.25/0.35, 0.2/0.3
1/5	N+ Poly	N+ Poly over island	0.25/0.35, 0.25/1.0
1/6	P+ Poly	P+ Poly over island	0.25/0.35, 0.25/1.0
1/7	Metal 1	Metal 1	0.75/0.75, 0.6/0.6
1/10	Metal 1	Metal 1 over Poly	0.6/0.6, 0.5/0.5
1/12	Metal 2	Metal 2	0.75/0.75, 0.6/0.6
1/13	Metal 2	Metal 2 over Metal 1	0.75/0.75, 0.6/0.6
1/14	Metal 3	Metal 3	1.0/1.0, 0.8/0.8
1/15	Metal 3	Metal 3 over Metal 2	1.0/1.0, 0.8/0.8

■ Contact/Via Chain Test Structures

This test structure consists of 2021 contacts of different sizes between different conductive layers connected in sequence (see Figure 7). Resistance of the chain reflects the quality of the contacts. Seven variants of this type of test structures are available (see Table 5 below).

Table 5. Contact/Via Chain Test Structures

Location Row/Column	Layer 1	Layer 2	Contact Sizes/Surround (µm)
2/3	Metal 1	N+ Island	0.5/0.25, 0.5/0.15, 0.5/0.05, 0.4/0.25
2/4	Metal 1	P+ Island	0.5/0.25, 0.5/0.15, 0.5/0.05, 0.4/0.25
2/5	Metal 1	N+ Island over N+ Island contact Chain	0.5/0.25, 0.5/0.15, 0.5/0.05, 0.4/0.25
2/6	Metal 1	P+ Island over P+ Island contact Chain	0.5/0.25, 0.5/0.15, 0.5/0.05, 0.4/0.25
2/9	Metal 1	Metal 2 (via chain)	0.5, 0.75, 0.6, 0.4
2/10	Metal 2	Metal 3 (via chain)	0.5, 0.75, 0.6, 0.4
2/11	Metal 2/3	Poly/Metal 1 (via chain)	various

These structure can be also used for wafer level reliability evaluation, in particular, for interconnect electromigration tests.

■ Sheet Resistance and Line Width Test Structures

These measurements are based on the Van der Pauw theory, which allows calculation of the resistivity of a conductive layer of arbitrary shape. The Greek cross structure is usually employed for this purpose. The line width measurements can be done by employing the cross-bridge (or double-cross bridge) structures. The Greek cross at one end of the structure is used to evaluate the resistivity of the conducting layer and then the resistance of the bridge (long line) is measured, allowing calculation of the line width.

Figure 8 shows a schematic and an optical view of a test structure of this type. The test is used to measure sheet resistance of different metal or polysilicon layers, to calculate changes in the line width (compared to the drawn line width), and to estimate contact resistances. Ten variants of this type of test structures are available:

- Metal 1 sheet resistance and delta Line Width (location Row 7/Column 1);
- Metal 2 sheet resistance and delta Line Width (location Row 7/Column 2);
- Metal 3 sheet resistance and delta Line Width, and Metal 3-to-Metal 2 via resistance (location Row 7/Column 3);

- N+ island sheet resistance and delta Line Width, and Metal 1-to-N+ island contact resistance (location Row 7/Column 4);
- P+ island sheet resistance and delta Line Width, and Metal 1-to-P+ island contact resistance (location: Row 7/Column 5);
- Undoped Poly sheet resistance and delta Line Width, and Metal 1-to-Poly contact resistance (location: Row 8/Column 1);
- N+ Poly sheet resistance and delta Line Width, and Metal 1-to-N+ Poly contact resistance (location: Row 8/Column 2);
- P+ Poly sheet resistance and delta Line Width, and Metal 1-to-P+ Poly contact resistance (location: Row 8/Column 3);
- N+ Poly sheet resistance and delta Line Width, and Metal 1-to-N+ Poly contact resistance (location: Row 8/Column 4);
- P+ Poly sheet resistance and delta Line Width, and Metal 1-to-P+ Poly contact resistance (location: Row 8/Column 5).

■ **Substrate Leakage Test Structures**

This test is performed on test structures, which are similar to the contact/via chain structures described above. A leakage current to substrate is measured by applying 2V to contact pads 1, 3, 5, and 7. Four variants of the test devices are used:

- Metal 1 to N+ island contact chain (location 2/3);
- Metal 1 to P+ island contact chain (location 2/4);
- Metal 1 to N+ island over N+ island contact chain (location 2/5);
- Metal 1 to P+ island over N+ island contact chain (location 2/6).

■ **MOS Transistors**

A schematic and optical views of the test transistors are shown in Figure 9. Tests procedures to characterize these transistors were developed at MIT/LL and are described in Section 4.2. A variety of widths and lengths of P- and N-channel transistors are available (see Table 6 below).

Table 6. P- and N- Channel Transistors Available

Location row/column	Channel	Width, µm	Length, µm	Gate
3/2 L	N	8	0.2	
3/2 R	N	8	0.25	
3/3 L	N	8	0.3	
¾ L	N	8	0.5	
3/5 L	N	8	2.0	
3/7 L	N	1	0.25	
3/5 R	N	8	8.0	
4/9 L	N	6	0.25	Circular
5/2 L	P	8	0.2	
5/2 R	P	8	0.25	

5/3 L	P	8	0.3	
5/4 L	P	8	0.5	
5/5 L	P	8	2.0	
5/5 R	P	8	8.0	
6/9 L	P	6	0.25	Circular
3/9 L	N	100	0.25	
3/9 R	N	100	0.5	
4/7 L	N	1	0.25 X 100 in parallel	
4/7 R	N	1	0.5 X 100 in parallel	
5/9 L	P	100	0.25	
5/9 R	P	100	0.5	
6/7 L	P	1	0.25 X 100 in parallel	
6/7 R	P	1	0.5 X 100 in parallel	
4/1 L	N	0.5	0.25	
6/1 R	P	0.5	0.25	

Test structures of this type can be used for wafer level reliability evaluation, in particular, for hot carrier effect measurements, gate oxide integrity, radiation hardness, and mobile ions.

- **Sidewall Edge Effect Measurement Test Structures**

This test is designed to evaluate the edge effect and employs MOS transistors with different gate configuration. A schematic and optical views of these transistors is shown in Figure 10. Location and types of these transistors are listed in the Table 7 below.

Table 7. Sidewall Edge Effect Measurement MOS Transistors

Location Row/Column	Type of Transistor	Width (µm)	Length (µm)	Gate Type
3/4 L	N	8	0.5	
3/4 R	N	8	0.5	Hgate
4/9 R	N	6	0.5	Circular
5/4 L	P	8	0.5	
6/8 R	P	8	0.5	Hgate
6/9 R	P	6	0.5	Circular

5.2. MIT/LL MOS Transistors Testing

Fourteen automatic parametric tests were developed to characterize MOS transistors [30]. Table 8 shows the measured parameters and respective test conditions.

Table 8. MOS Transistors Parameter Measurements

Test	Parameter	Conditions
Test A	Vtlow	Force 50 mV on Drain; Sweep Gate from 0.0 V to 2.0 V; Differentiate data set; Find Max Slope; Find index of max slope in slope array; Test – A = (Y-intercept + Vds/2.) as Vtlow; Test – K = Slope as gm.
Test B	Vtlow with substrate bias voltage applied	Same as Test-A with substrate biased
Test C	Vthigh	Calculate target current (Itarg) as 0.1 uA * (W/L); · Force 1.0 V on Drain; Execute binary search on Gate (-0.5 V to 2.0 V); · Test-C = Gate voltage which produces a Drain-Source current of (Itarg).
Test D	DIBL	Calculate DIBL = (Vtlow (Test A) – Vthigh (Test C))/0.95 (*difference in drain voltage).
Test E	Subthreshold swing	· Force 50 mV on Drain; Sweep Gate from O.OV to Vtiow; Store Vgs in ARRAYL; Store Ids in ARRAY2; · If Ids at the start of the sweep (LEAKI) is greater than 1 nA, abort the test; · Search the Ids current array (ARRAY2) for a current close I OnA, retrieve array index as INDEX1; · Search the Ids current array (ARRAY2) for a current close 0. 1 nA, retrieve array index as INDEX2; · VGSI = ARRAYI(INDEX1); · VGS2 = ARRAYI(INDEX2); Force 50 mV on Drain; Sweep Gate from VGS1 to VGS2; Store Vgs in ARRAY3; Store Ids in ARRAY4; · Calculate ARRAY5 as log(abs(ARRAY4)); Perform linear least squares fit to x,y dataset where x=ARRAY3, y=ARRAY5, to get SLOPE; · Subthreshold swing(mv/decade) = (1.0/SLOPE) *1000.
Test F	Drain-Source Leakagel	Force 1.0V on Drain; Force 0.0V on Gate; measure Ids
Test G	Drain-Source Leakage2	Force 2.0 V on Drain; Force 0.0 V on Gate; measure Ids
Test H	Drain-Source Leakage3	Force 2.0 V on Drain; Force –0.5V on Gate; measure Ids
Test I	Ddve Current 1-	Force 1.0 V on Drain; Force 1.0 V on Gate; measure Ids
Test J	Ddve Current 2	Force 2.0 V on Drain; Force 2.0 V on Gate; measure Ids
Test K	Linear transconductanc e (gm)	see Test A
Test L	Saturation transconductanc e (gsat)	Force 1.0 V on Drain; Force 0.9V on Gate; measure current as I1; · Force 1.0 V on Drain; Force 1.1 V on Gate; measure current as 12; Gsat = (11-12)/.2.
Test M	Output conductance (gds)	· Force 1.0V on Gate; Force 0.9V on Drain; measure current as I1; · Force 1.0V on Gate; Force 1. 1 V on Drain; measure current as 12; · Gds = (11-12)/.2.

Test N	Back channel threshold	· Calculate target current (Itarg) as 0.1 uA * (W/L); · Force 1.0 V on Drain; Ground Gate; Execute binary search on Wafer (-0.5 V to 20.0 V); Test-N = Wafer voltage which produces a Drain-Source current of (Itarg).

Test measurement details: *reverse voltage polarities for p-channel FETs; the source is grounded for all tests.

6.0 MIT/LL FD FET Reliability Characterization Test Results

6.1 Hot Carriers Effects Test Results

The hot-carrier induced degradation in SOI MOS transistors fabricated at Lincoln Laboratory was investigated at JPL [31]. Experiments were performed on several fully depleted 0.25-μm SOI n-channel MOS transistors, which had a gate oxide thickness of 7.3 nm, a silicon layer thickness of 50 nm and a buried oxide thickness of 195 nm.

Initial measurements showed a relatively poor reproducibility of the I_d vs. V_g characteristics from one chip to another. The transistors had breakdown voltages (at $V_g = 1.5$ V) of 2.88 V, 3.10 V, and 3.28 V for channel lengths of 0.25, 0.3 and 0.35 μm, respectively.

These transistors were stressed at three different drain voltages ($V_{d,stress}$) below the breakdown voltage, with front gate voltage $V_{g,stress} = V_{d,stress} / 2$ and the backgate grounded. The I_d versus V_g characteristics at $V_d = 50$ mV and $V_{g2} = 0$ V were recorded versus stress time up to 100,000 sec (approx. 27 hours).

The lifetime, τ, is often defined as a 100-mV or 10-mV shift in V_{th} or a 10% degradation of $g_{m,max}$, and exhibits usually an exponential dependence on the drain voltage bias that can be expressed by following relationship:

$$\tau \propto \exp(a / V_d).$$

The test results showed that the observed degradation did not follow simple power time dependence with a constant index, but rather the index decreased with time after 100 sec. Experiments performed at $V_{d,stress}$ more than 2.5 V showed that a different degradation mechanism was involved at these stresses. This indicates that particular care should be taken in future experiments to stress the transistors in conditions representative of normal operating conditions.

Analysis showed that degradation of the NMOS transistors was caused by negative injected charges and resulted in an increase of the threshold voltage and in a decrease of maximum transconductance. It is quite possible that this degradation was caused by the hot carriers

effect at the back (silicon-buried oxide) interface. For additional details, consult reference [31]- Final Report for FY00, Dated 12/8/2000.

Due to the limited number of devices available (3 transistors), only preliminary results on the lifetime estimations were obtained. Although these results looked promising for applications below 2 V, more data are needed around 2.5 V to verify the trend. GSFC/JPL are planning to procure some additional test chips from MIT/LL to perform more extensive characterization including testing at extreme temperatures.

6.2 Radiation Effects Testing

Radiation testing was performed during the second Multiproject fabrication run and employed FD SOI N-channel MOS transistors, which were designed for low power, high performance operation without any optimization for radiation performance [8]. The transistors had a channel width of 8.0 μm and a length of 0.25 μm.

An X-ray source with the dose rate of 10 krad(Si) per minute for 0-200 krad and 130 krad(Si) per minute for 200-1000 krad was used for this testing. The devices were biased with 1 V on the gate and 0 V on the source, drain and substrate.

No changes in the threshold voltage were observed at –30 V on the wafer (creates accumulation at the buried oxide-Si interface), whereas at 0 V the threshold shift was 140 mV after a dose of 1 Mrad (Si). Preliminary results showed relatively minor changes in the transistor characteristics, which were most likely due to degradation at the buried oxide interface.

6.3. Effects of Temperature

Conventional bulk-Si MOSFET devices operate at moderate temperatures up to 150 - 200 °C. At higher temperatures, these devices usually fail due to increased junction leakage, thermally induced latch-up and threshold voltage shifts. With proper dielectric isolation, this high–temperature limit can be extended well above 200 °C, up to 500 °C [2]. In the range from 0 °C to 300 °C, the threshold in a p-channel SOI transistor tend to increase with temperature at a rate of 3 mV/°C and to decrease at a rate of 2.5 mV/°C for an NMOS transistor [32].

Preliminary results on the behavior of the FDSOI transistors at cryogenic temperatures (60 K, 50 K and 40 K) have also been reported [33]. The measured n- and p- channel MOS transistors were manufactured by MIT/LL, had 0.25 μm gate length and the widths in the range from1 to 100 μm and operated at 2 V.

Experiments have demonstrated normal operation of the transistors at cryogenic temperatures. The threshold voltage increased from 0.43 V at room temperature to 0.64 V at

40 K. The key parameters of the transistors such as the subthreshold slope and the drive current, increased at low temperatures in accordance with expected theoretical predictions.

7.0 Conclusions

The finding of this study on reliability evaluation of FD SOI technology for space applications are summarized below.

- Analysis of the present state of the art of SOI technology and reliability has shown that SOI technology has relatively matured over last several years and become a good candidates for aerospace applications. A number of companies are currently testing and evaluating custom designed SOI devices for high volume, commercial manufacturing product lines.

- MIT/LL has completed development of the 0.25 µm FDSOI process. A variety of microcircuit elements and custom designed analog and digital devices were manufactured and successfully tested during the three Multiproject Fabrication runs. Preliminary results showed that the FD SOI CMOS has promising performance characteristics, good radiation radiation tolerance and low temperature characteristics.

- MIT/LL has developed a test chip matrix, which includes more than a hundred of different test structures. This matrix can provide adequate process control of all major steps of the microcircuits manufacturing. However, the wafer level reliability system for quality control has not yet been developed. Test structures available on the test chip matrix most likely could be used to develop similar system in the near future. Therefore, hot electrons degradation effects are an area of concern, especially at low temperature operation. Additional testing is necessary to characterize these degradation effects and provide the data to NASA designers that would enable them to take those effects into consideration. GSFC/JPL are planning to perform this additional testing.

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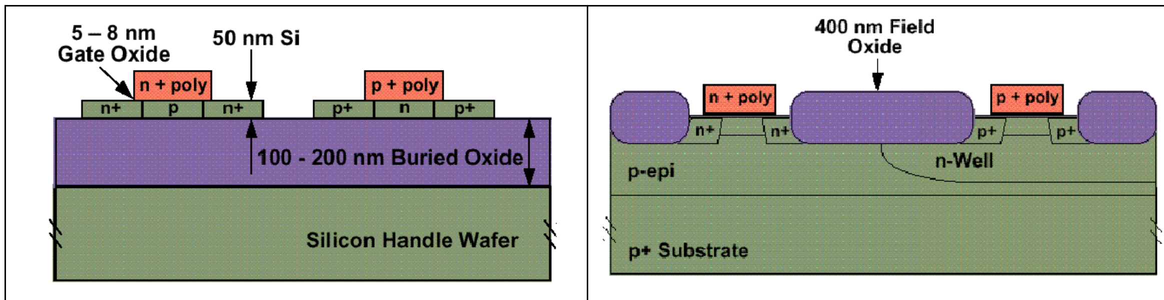


Figure 1. Design comparison: SOI (left) and bulk-Si (right) CMOS transistors [25].

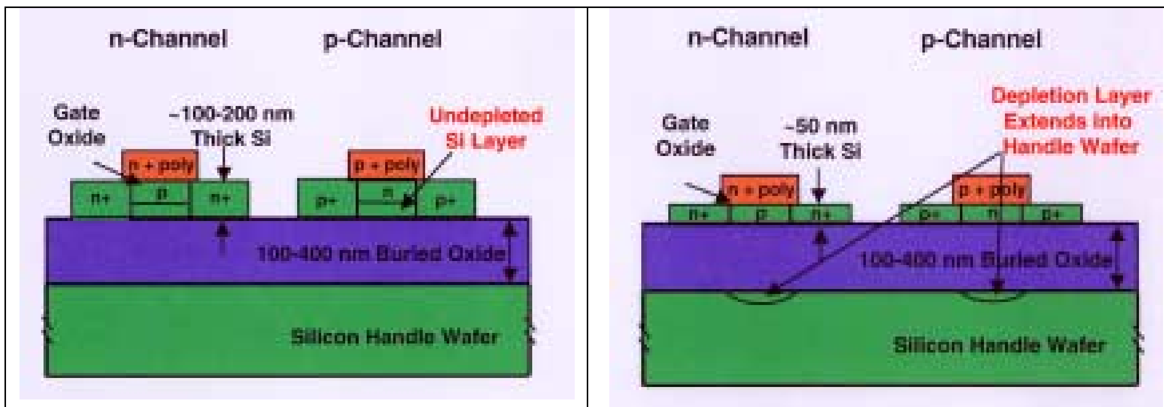


Figure 2. Design comparison: PD (left) and FD (right) SOI CMOS transistors [8].

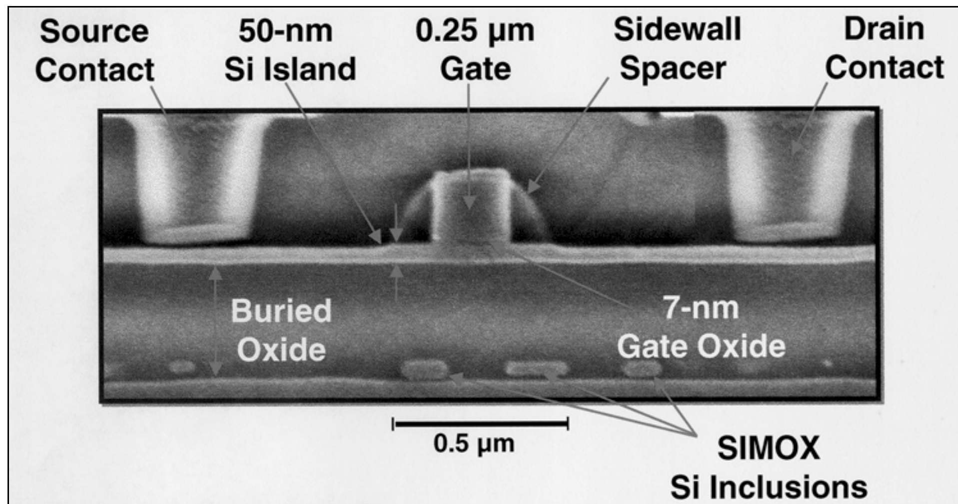


Figure 3. FD SOI FET cross section, SEM view [8].

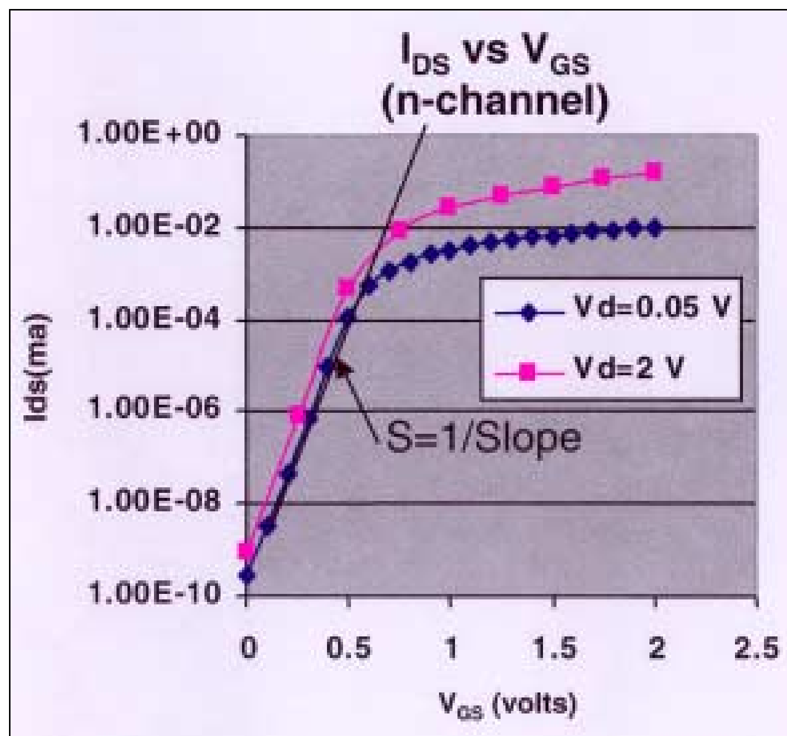


Figure 4. Subthreshold characteristics of the FDSOI FET [8].

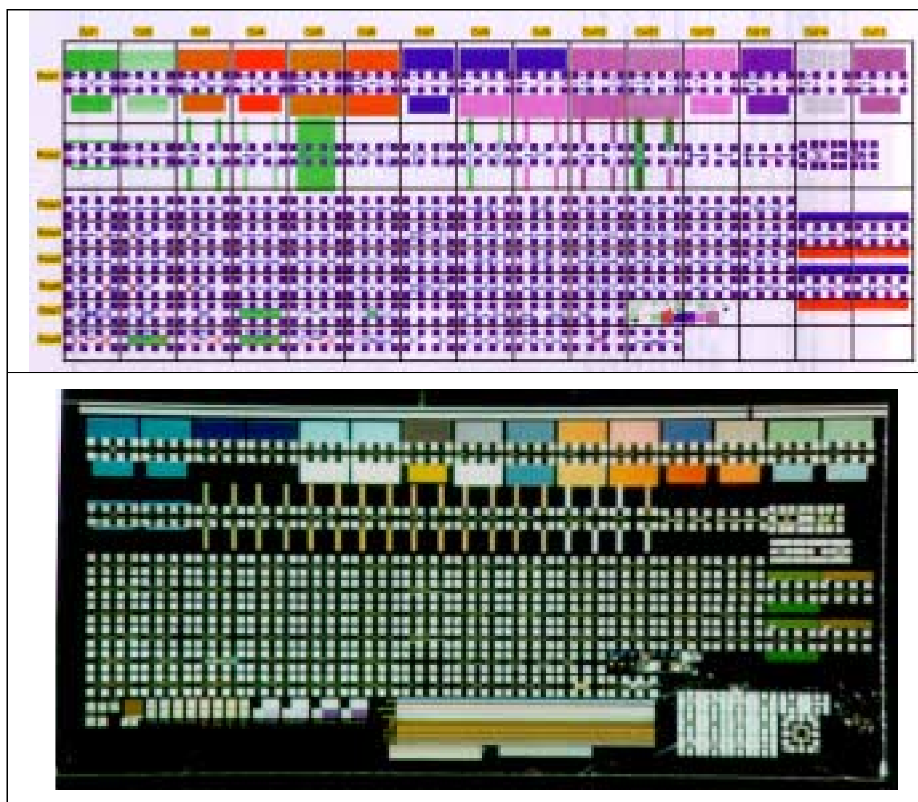


Figure 5. Layout (top) [30] and an optical view (bottom) of the MIT/LL test chip matrix.

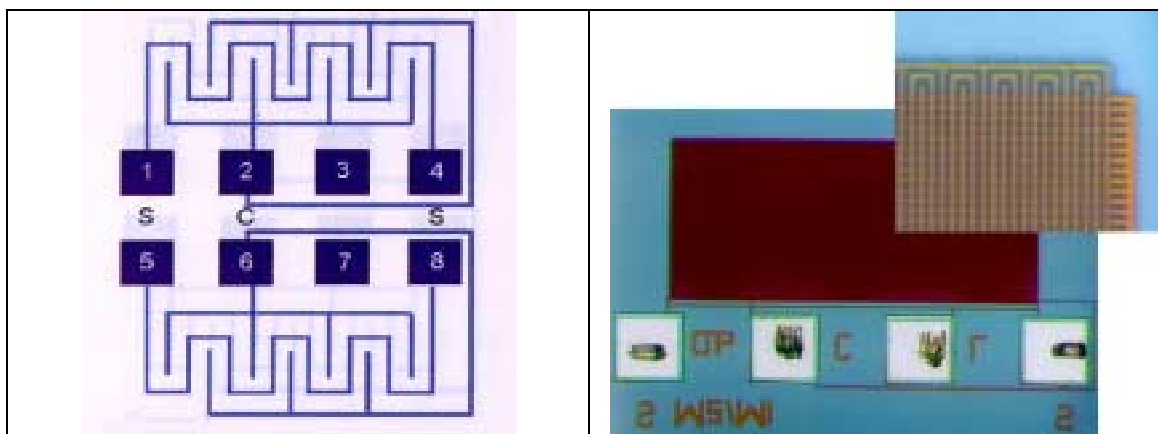


Figure 6. Schematic [8] and optical view (≈100X) of a Snake-Comb-Ladder test chip. Insert shows close-up of the corner area. (≈1000X)

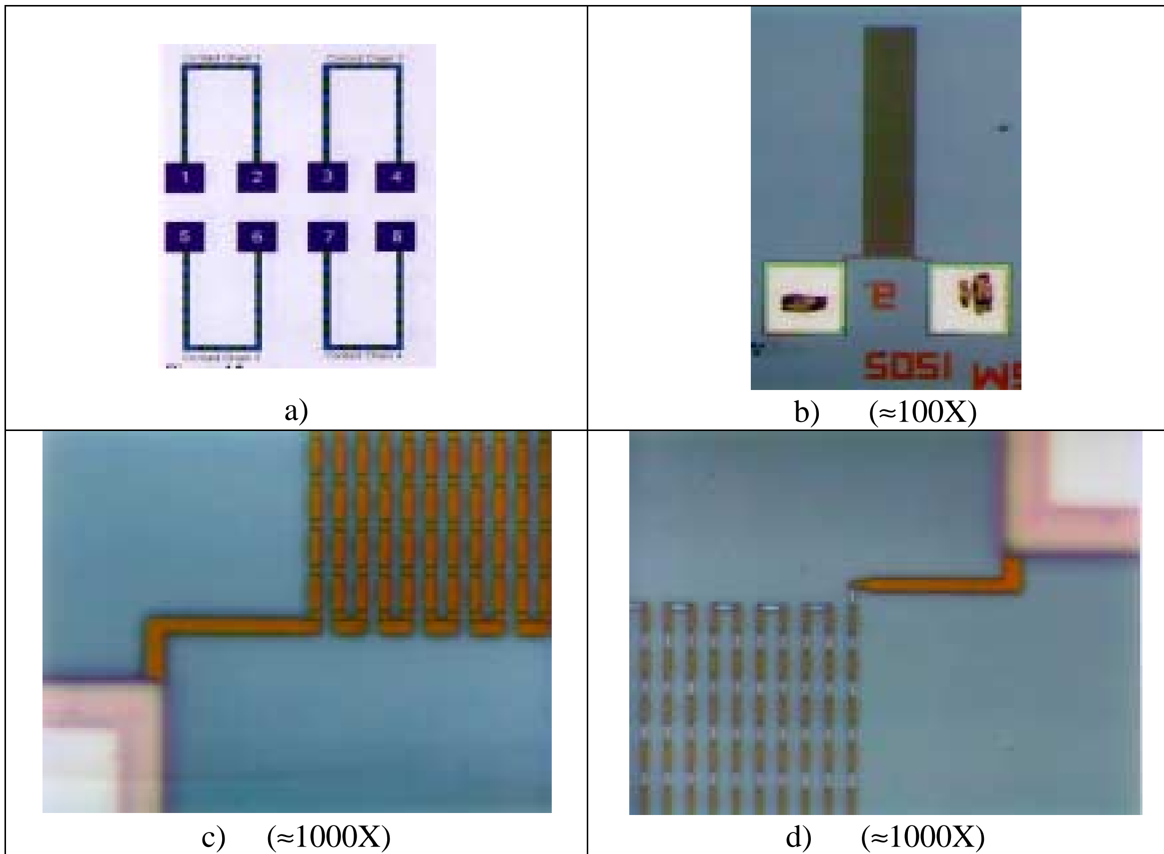


Figure 7. Schematic (a) and optical views (b, c, d) of different Contact/Via chain test chips.

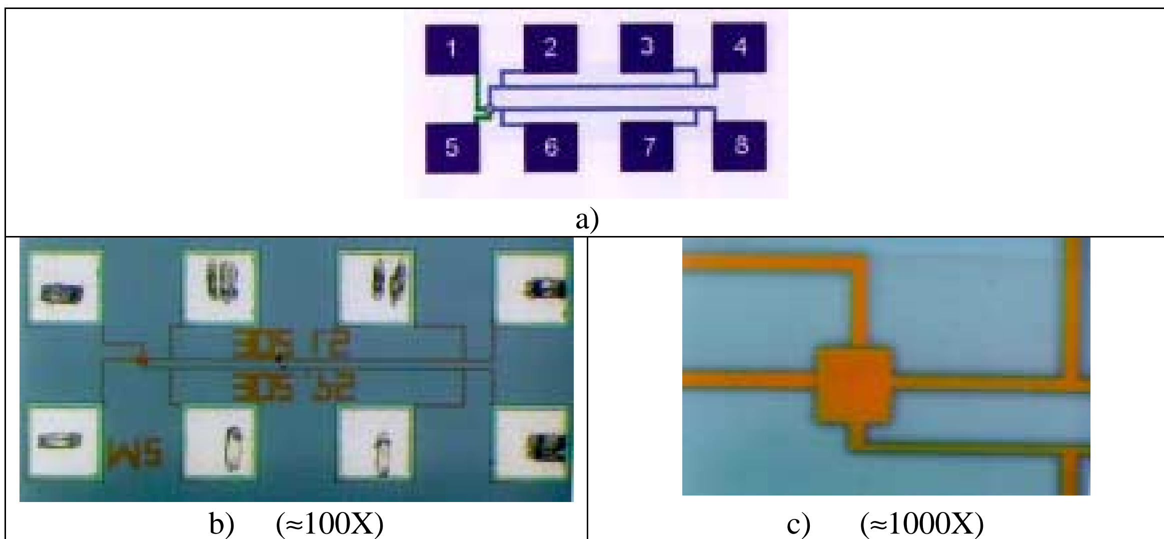


Figure 8. Schematic (a) and optical views of a sheet resistance and line width test chip (b, c).

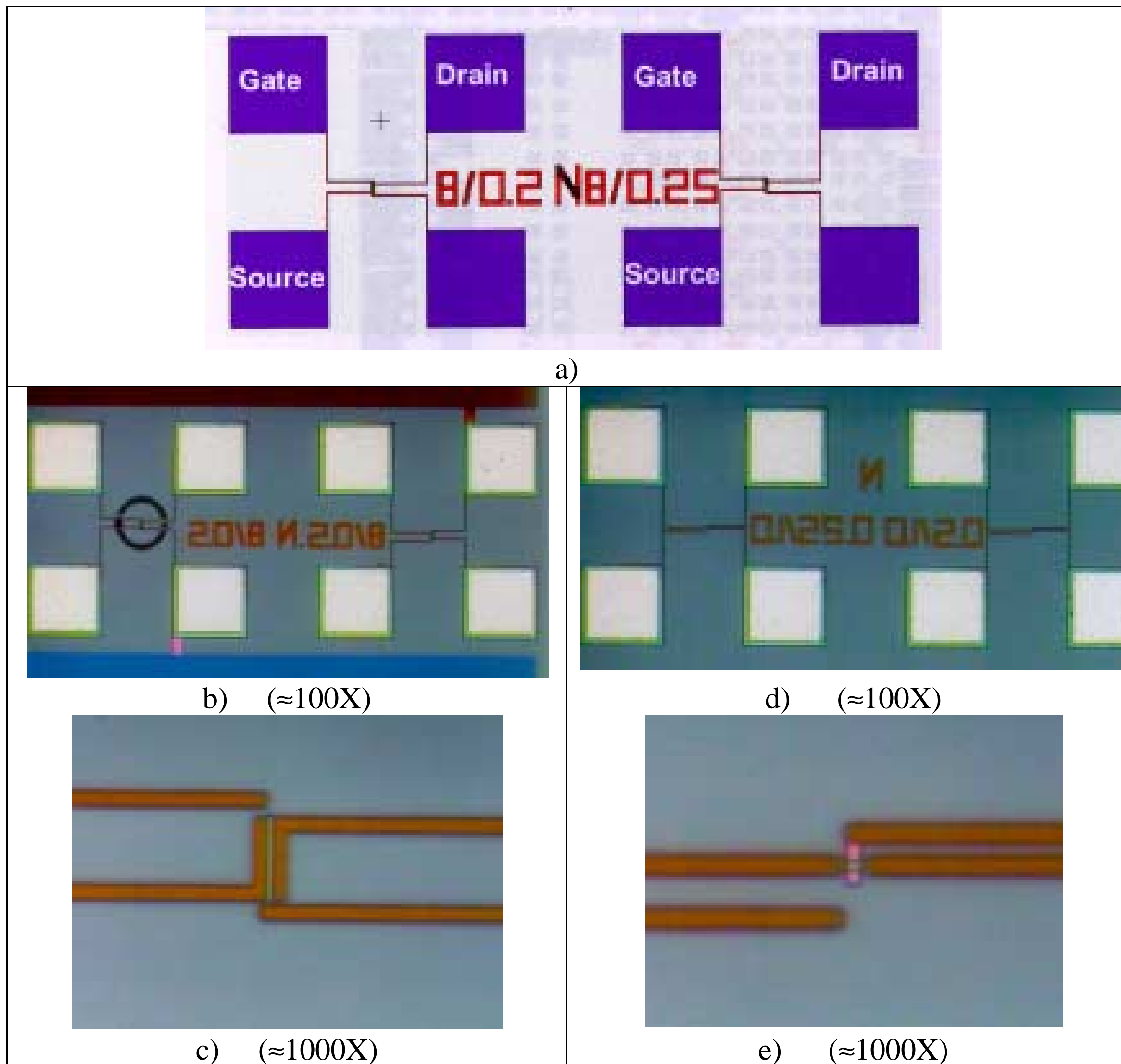
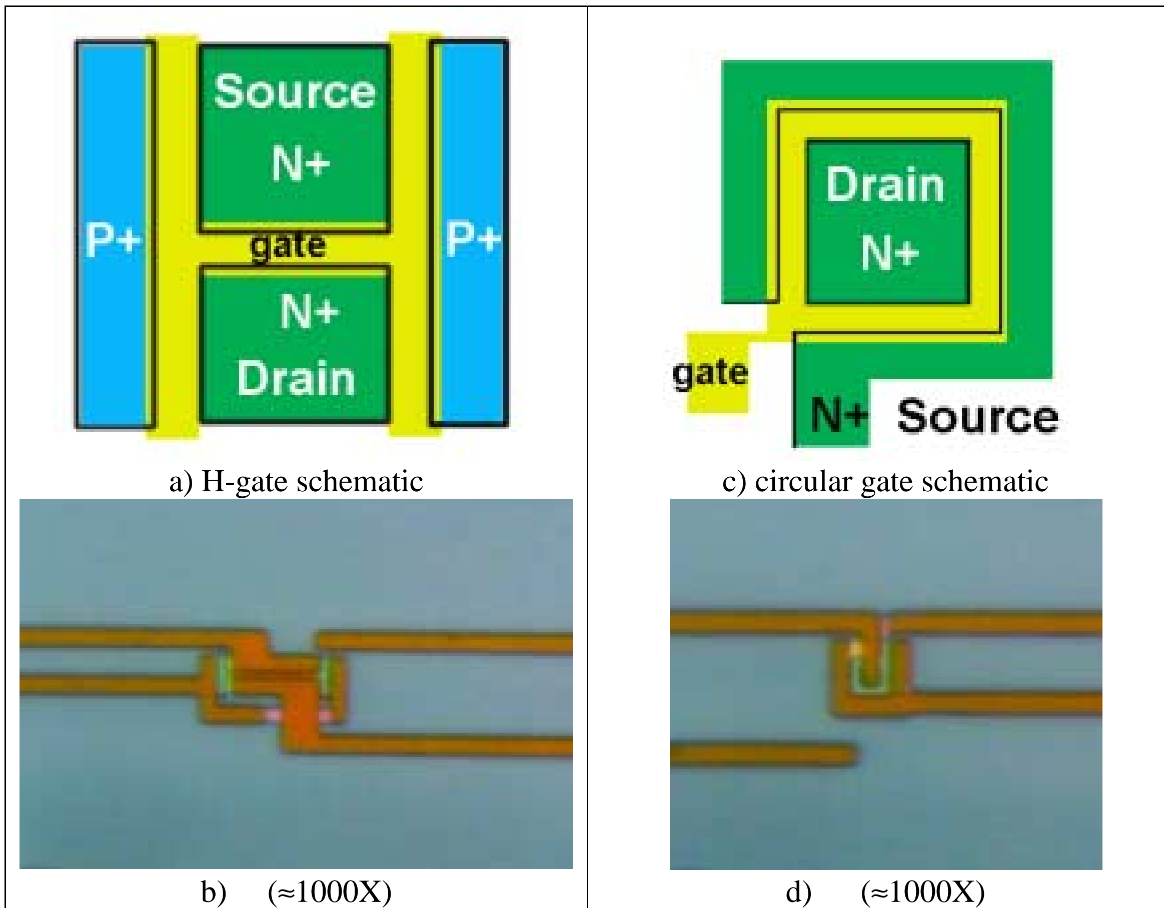


Figure 9. Schematic and optical views of two FDSOI MOS transistors with different channel widths.



a) H-gate schematic c) circular gate schematic

b) (≈1000X) d) (≈1000X)

Figure 10. FDSOI transistors with H-gate (a, b) and circular gate (c, d) for sidewall effect testing.