Reliability of Lead-free and Tin-Lead Solders for PBGA Assemblies

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IPC 97xx covering surface mount assembly reliability for both thermal and mechanical testing requirements are now well adopted by industry and widely referenced. Specifically, IPC-9701 specification addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. Since release of its new revision that includes Pb-free solder, additional data have been gathered to determine the impact of various thermal cycle parameters on accelerated test results. Industry/Celestica/JPL test data for a high I/O plastic package assembled using Pb-free and tin-lead solder alloys are presented. Effect of various parameters including type of solder materials, reflow maximum temperature, dwell time, and monitoring techniques are discussed in details. Results of JPL data performed under three different thermal cycles one cool down to -130° C also presented. The Celestica's most recent data generated for the same package/assembly using preferred thermal cycle profile recommended by IPC 9701 is also presented.

1. Introduction

Ball grid arrays (BGAs) and chip scale packages (CSPs) are now widely used for many electronic applications, including portable and telecommunication products. The BGA version is now extensively implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. The plastic BGA version of the area array package, introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid 1990s to the CSP (also known as fine pitch BGA) having a much finer pitch from 0.4 mm to 0.3 mm. Because of these developments, it is becoming even more difficult to distinguish different array packages by size and pitch.

Extensive work has been carried in understanding technology implementation of area array packages for high reliability applications using tin-lead solder alloy⁽¹⁻⁵⁾. Commercial industry moves to use of various lead-free solder alloys requires understanding of many reliability aspects before its use in high reliability applications. Co-authors and their team have been active in evaluating various lead-free solder alloys and published their results⁽⁶⁻⁷⁾. This paper review IPC 9701 for lead-free solder alloy and compare industry test data for assembly of a full array PBGA package with 676 I/Os. Thermal cycle data for the same package using the same test vehicle performed in two facilities are also presented.

2. IPC Standard for Thermal Cycle Performance Requirement for SMT Assemblies

The IPC-9701 specification⁽⁸⁾ addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to compare solder joint reliability for different package technologies, numerous materials and process parameters were specified, including the following:

- Specifies 0.093 inch for the PWB (e.g., FR-4) thickness in order to minimize bending and to achieve conservative values on cycles-to-failure data.
- Limits surface finish choices to OSP (organic solder preservative) and HASL (hot air solder level) in order to eliminate the potential of interfacial failure
- Limits pad configuration to NSMD (non-solder mask defined or Cu defined) in order to eliminate failure due to stress risers.
- Defines PWB-pad size to be 80% to 100% of the package-pad size in order to have a more realistic failure

The newest revision, IPC-9701A, includes guidelines for Pb-free solder alloys. Appendix B of this specification provides guidelines for modifications for Pb-free solder joints. Two thermal cycle profiles were recommended for (SAC) solder attachments depending on the reliability approach and use conditions. These are:

- Condition D10 (10 minute dwell) requiring 10-minute dwells at both the hot and cold temperature extremes. This is possibly the most efficient, accelerated thermal cycle profile since it induces the most strain energy per unit of time (considering the entire cycle) or per unit dwell time. Cycles-to-failure data generated under this condition should generally be used as stand-alone only, and only when damage accumulation is understood by modeling. The test results may be used for comparison to those of lead-based solder assemblies to show theoretically whether their performance is better or worse.
- Condition D30⁺ (30 minutes or higher dwell) requiring dwells of 30 minutes and higher (i.e., 60 minutes) at the hot and cold temperature extremes in order experimentally to induce creep damage somewhat comparable to lead-based solder. Modeling in conjunction with experimental data at different dwell times may be required to better define such a comparison.

An OSP surface is recommended for the Pb-free base solder alloys even though the final version of the specification includes immersion silver (IAg) based on additional inputs by industry. For Sn-Pb, the acceptable surface finish was HASL. For Pb-free, HASL is not allowed since it is not compatible with Pb-free solder interconnections. Other surface finishes can be used for the manufacturer's internal data comparison. Electroless nickel/immersion gold (ENIG) surface finish also can be used for internal data comparison; however, there is a risk of introducing unintended immature failure as documented by industry.

In this specification, the thermal cycle (TC) test ranges, test profile, and the number of test cycles (NTC) reported were also standardized. These include the reference cycle in the range from 0° to 100°C (TC1) and the harsh military cycle condition from -55° to 125° C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22, Method A104, Revision A. The NTCs varied from a minimum value of 200 cycles to a reference value of 6000 cycles.

3. Cycles-to-failure of PBGA676 I/Os

The effects of the parameters for PBGA 676 I/O package assemblies are presented below.

3.1 Effect of Dwell Time:

A team of companies⁽⁹⁾ collaborated to evaluate the assembly and reliability of lead-free SnAgCu (SAC) PBGA676 psckages with tin-lead and lead-free SAC solder paste on a 93mil thick test vehicle. Reliability evaluations included Accelerated Thermal Cycling (ATC) from 0° to 100° C with 2 dwell time durations at the high temperature 100° C extreme: the usual short dwell duration of 10 minutes and a long dwell duration of 60 minutes recently proposed by IPC. The Weibull plots of test results for the two test conditions are shown in Figure 1. As expected, shorter dwell time resulted in higher cycles to failures.

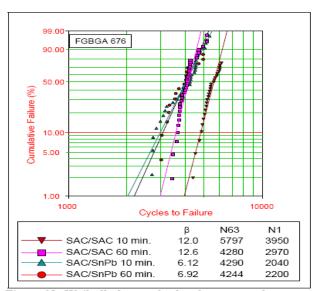
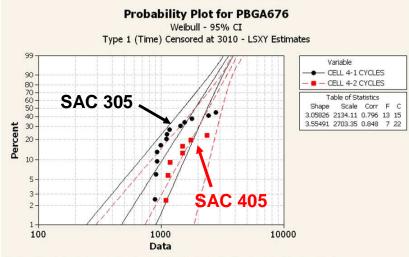


Figure 1 Effect of dwell time on lead-free 2nd level assembly (Bath, et al, SMTAI 2005)

3.2 Effect of Lead-free Solder Alloys:

Progressively improved test vehicles were built by the co-authors' team to characterize manufacturing as well solder joint reliability of various packages. The results for the PBGA 676 I/O package assembly on 93 mil board using two types of paste and thermal cycled per IPC 9701 in a harsh environmental testing are shown in Figure 2. It is clearly shows decrease in cycles-to-failure for lower silver paste alloys SAC 305 compare to SAC 405. Thermal cycle temperature range was relatively severe and was in the range of -55° to 125°C.



Note: CELL 4.1 had one component fail at thermal shock - removed from sample.

Figure 2 Effect of lead-free silver amount on solder joint reliability of PBGA676 (- 55/125°C)

3.3 Effects of solder paste alloys for preferred TC, 0°-100°C:

The co-authors' team working in an EMS facility, supporting mostly commercial OEMs, was required to perform extensive characterization of lead-free assemblies. They performed extensive testing characterization using the preferred thermal cycle profile (0°-100°C) recommended by IPC 9701A. Various conditions included in evaluation are as follows:

- Tin-lead solder paste with SAC405/305 balled 676 I/O packages (Cells 1-1 to 1-6)
- SAC305 on various surface finishes (Cells 2-1 to 2-6)
- SAC405 on various surface finishes (Cells 3-1 to 3-6)
- Thick board, primary and reworked (5-1 and 5-3)

The test results for assemblies with various boards, solder, and balls alloys are shown in Figure 3 where y axis represents various testing conditions. It is apparent that most of these assemblies showed no failures to 6,000 thermal cycles or failures were limited. Weibull's plots could not be generated because insufficient number of failed samples.

3.4 Test Results for High Reliability Applications:

In collaboration with co-authors, test vehicles built at the EMS facility was tested under thermal cycling conditions that generally are considered for high-reliability applications. The PBGA assemblies were subjected to three thermal cycle conditions. All assemblies passed 200 thermal cycles. Thermal cycle conditions and number of samples tested were:

- (-130°/85°C), 4 parts
- (-55°/125°C), 6 parts
- (-55°/100°C), 8 parts

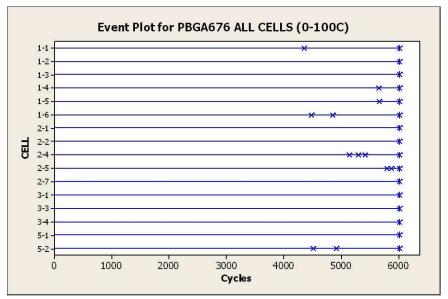


Figure 3 Effects of various assembly parameter on cycles-to-failures of SAC405/SAC305 PBGA675 subjected to 0° to 100°C)

4. Summary and Future Activities:

Figure 4 summarizes literature review and test results performed at two facilities:

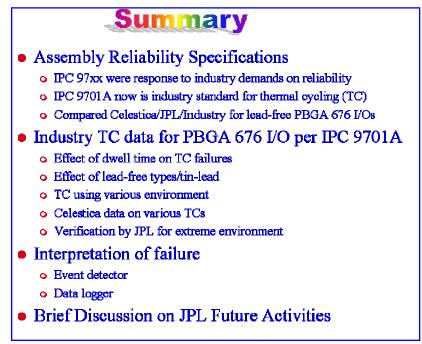


Figure 4 Summary page

5. Acknowledgements

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6. References

1. Ghaffarian, R., "Shock and Thermal Cycling Synergism Effects on Reliability of CBGA Assemblies," 2000 IEEE Aerospace Conference Proceedings (2000), p. 327

2. Fjelstad, J., Ghaffarian, R., Kim, YG., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002)

3. Ghaffarian, R., "Chip Scale Package Assembly Reliability," Chapter 23 in *Area Array Interconnect Book*, eds. K. Puttlitz, and P.Totta (Kluwer Academic Publishers, 2002)

4. Ghaffarian, R.,"Characterization and Failure Analyses of Lead-Free Solder Defects," Chapter 10 in *Lead-Free Solder Interconnect Reliability Book*, ed. D. Shangguan (ASM International, 2005

5. Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir, Editor (Springer, 2006)

6. McCormick, H., et al, "Mixing Metallurgy: Reliability of SAC Balled Area Array Packages Assembled Using SnPb Soldering," SMTA International, Sept 2006

7. Snugovovsky, P., et al, "Failure Mechanisms of SAC305 and SAC405 in Harsh Environment and Influence of Board Defects Including Black Pad," SMTA International, Sept 2006

8. IPC-9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," IPC, Association Connecting Electronics Industries, 2006

9. Jasbir, Bath, et, al, "Reliability Evaluation of lead-free SnAgCu PBGA676 Component Using Tin-lead and Lead-free SnAgCu Solder Paste" SMTAI 2005