Report from Task Force on APA Wire Printed Circuit Boards

8 June 2020

Background and context

The Preliminary (60% maturity) Design Review of the electrical design of the DUNE SP APA was held at PSL on November 18-19 2019 chaired by Jonathan Asaadi.

The DUNE/LBNF JPO Review Office released the final report on 12 February 2020.

Out of the report's 32 Comments and 6 Recommendations 18 and 5 respectively refer to the specification, design, production and QA of the wire boards.

The APA consortium leadership considers that at this point the wire boards are on the critical path of our plan to be ready for Final Design Review in summer 2020 and start APA production in the UK in Q3/20.

Task Force Membership

Terri Shaw, tshaw@fnal.gov, FNAL, Chair

Andy Laundrie, awlaundrie@wisc.edu, PSL (board designer)

Mike Eads, meads@niu.edu, NIU

Justin Evans, justin.evans@manchester.ac.uk, U. Manchester

Anthony Ezeribe, a.ezeribe@sheffield.ac.uk, U. Sheffield

Tim Jones, timjones@liverpool.ac.uk, U. Liverpool

Graham Miller, Graham.Miller@manchester.ac.uk, U. Manchester

Mitch Soderberg, msoderbe@syr.edu, Syracuse

Answers to Charge Questions

Charge questions addressed three main areas of concern: mechanical tolerances of the boards, electrical tolerances of the boards and the tolerances of the press-fit pin and socket custom parts. Three working groups were established to specifically study these areas. The reports from those groups are included as appendices to this document.

1. Mechanical tolerance on board thickness.
    a. Current mechanical tolerance is specified as low as +/-2%
    b. Industry standard is +/-10%, advanced +/-5%
    c. Review panel recommends thickness tolerance be "clearly defined as motivated by the physics requirements" – is +/-5% tolerance acceptable?

d. Review panel also recommended that commercial vendors should be found such that boards could be "done at production scale without custom modifications being done"

The task force recommends that board thickness tolerance be required to be less than or equal to +/-5%. This tolerance is stricter than industry standard of +/-10%, but is within what multiple PCB vendors can produce given advanced techniques. It is believed that transparency requirements can be met. (see Appendix A)

2. Electrical specifications of board, specifically the trace to trace spacings maintained to avoid breakdown.
    a. The differential voltage between traces dictates a certain spacing when following IPC criteria. The APA Consortia wishes to have at least a 20% overhead from nominal wire bias settings and the wire tension test will supply a differential voltage of ~500V for a short duration.
    b. Committee should advise trace to trace spacing requirements which follow the IPC criteria or are proven to be sufficient through testing.

It has been shown that all APA PCB boards can maintain the clearances required to withstand both wire bias voltages and the 500V differential required for wire tension measurement. Some minor board layout issues will be addressed and conformal coatings will be put on vias as well as some connector pins. (see Appendix B)

3. Advice on how to implement the statement in the report "Prior to declaring a design final an engineering review should be completed to ensure that either all IPC standards have been met or that tests have been performed indicating that the risk of breakdown on the boards are negligible."

The Task Force focused primarily on **IPC-2221B PCB Trace Spacing / Clearance by Voltage**. We felt that this standard addressed the main concerns of the ability of the boards to withstand the bias voltage differences on the CR board and the differential voltages applied to the wire boards during wire tension measurements. Anthony Ezeribe and Graham Miller have identified tools which allow for the verification of IPC-2221 standards with respect to breakdown voltage. All boards should be vetted with these tools. It is advisable to test prototype batches of boards using the final artwork prior to launching production.

4. All aspects of board-to-board connections including the proposed custom MillMax connectors. Hole tolerances and plating specifications should be well documented for all press-fit pins. QA procedure to ensure good electro-mechanical connection should be defined.

Andrew Laundrie has identified a drill size and plating requirements for all press-fit holes. Further tests will be done to verify the new requirements perform as required and give the expected force measurements to push a pin in and pull it out of a finished hole.

Currently all pins are pressed by hand using an arbor press. It is strongly recommended that proper tooling be designed to make this process easier to automate and give consistent results.

5. The suitability, based on manufacturers' specifications, of all components, and the procurement strategy for them.

When producing or acquiring boards and/or parts:

PCBs – suggest a single vendor for each type of PCB; this guarantees the same production process for each type of board. Some boards require precision machining. Work with vendors to discuss whether they can do this work or if a 3rd party vendor needs to be identified for precision machining. Special tooling may be required.

Pins/Sockets – These are custom precision parts. Suggest that production quantity be purchased and tested. Custom tooling for pressing pins will be required.

Components – Capacitors have a long lead time of 2-3 months. The screening process for the boards also includes measuring the leakage current to lower levels than what is allowed for in the specification. Buying all capacitors at once and asking that they come from the same lot will give a more uniform performance.

6. Production procedures, best practice, QA.

APA consortia is encouraged to work with DUNE QA professionals. Many of the recommendations above reflect best practice which we believe should be followed.

Detailed assembly and test procedures should be developed. Mechanical tolerances should be clearly identified and marked on all mechanical drawings.

APPENDIX A

PCB Mechanical Tolerances

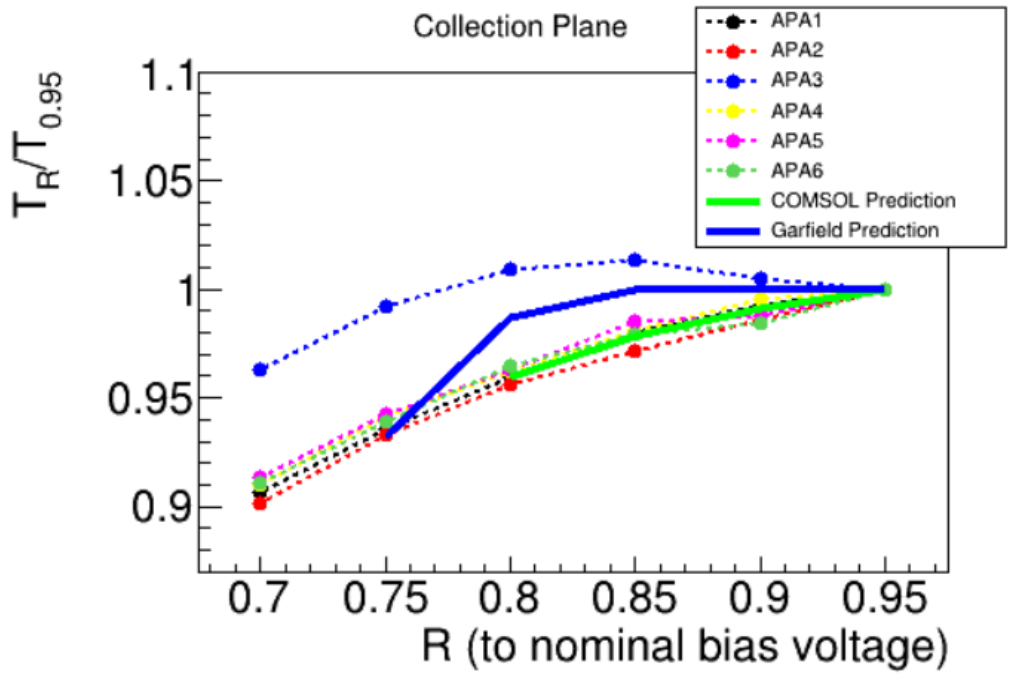
Mechanical tolerances of DUNE APA PCBs

The primary focus of the task force was to define the needed tolerance on circuit board thickness. The task force additionally looked at other dimensional tolerances on these circuit boards.

Board Thickness Specification

Circuit board thickness is what determines the spacing between wire layer on the APA. Hence, it is important to the overall performance of the APA. The key physics driver is the requirement for electron transparency.

The quality of the processing of the signals from the charge collected from the APAs relies on the assumption that the G-layer and the two induction layers (U and V) are transparent to the charge, and that all charge is collected on the collection (X) layer. This transparency is achieved if ratio of the electric field in front of and behind each induction layer matches the transparency condition (O. Bunemann *et al*., Can. J. Res. **A27**, 191), and that ratio is a function of the applied bias voltages and the layer spacing. The figure below shows a COSMOL simulation, compared to ProtoDUNE data, of how the transparency depends on bias voltage, indicating that the COSMOL simulation is trustworthy (X. Qian, https://indico.fnal.gov/event/18681/session/13/contribution/157/material/slides/0.pptx).

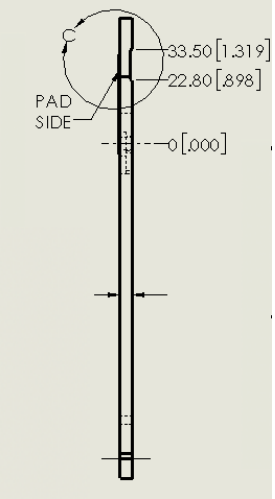


An analytical calculation determines that a 0.5 mm change in wire-layer spacing corresponds to an 11% bias-voltage change, or a 3-4% transparency loss of the affected

induction layer; this would stack up if two boards directly above and below each other were too thick or thin in a correlated way.

The design wire-layer spacing is 4.8 mm. The official APA design parameter from the TDR states a ±0.5 mm tolerance on the layer spacing, however we should not take that all up in the thickness of each board. The APA frame also has a flatness tolerance of around 0.5 mm, however frame warpings affect all layers separately rather than the layer spacing. If we can control the PCB impact on the layer-spacing tolerance to 5%, or 0.24 mm, we are a factor of two within the stated APA tolerance, and we also do not risk any part of the APA losing more than 4% transparency even if both induction layers are too close or too far apart by the full 0.25 mm.

Discussions between the UK groups and several circuit board manufacturers have indicated that a ±5% tolerance on the board thickness is likely achievable. This thickness parameter is vital for the head boards, and less critical for the wrap boards. The task force feels it may be easier to order all boards with a ±5% tolerance on thickness, but cost considerations may make it more sensible to have a ±10% tolerance for the non-critical boards.

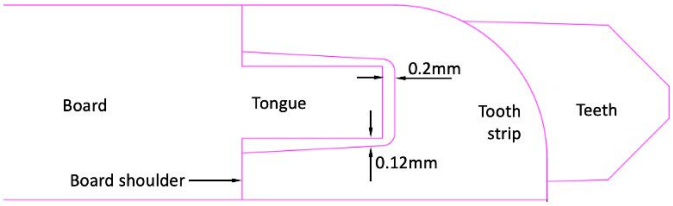


Other Mechanical Dimension Tolerances

While the focus of the charge to the task force was the board thickness specification, several other board dimensions are important. These were examined during the work of the task force and are summarized here.

There is a glue groove on head boards used for the glue when building up the board stack (see figure at left). If this groove is too shallow, the glue will overflow and the board will not sit flat. If it is too deep, the glue will not engage both boards. The recommended tolerance on the depth of the glue groove is ±0.2mm.

Additionally, there is a “tongue” on wrap boards to which a tooth strip is attached (see figure below). The dimensions of this tongue are important for proper positioning of this tooth strip, which impacts wire positioning. The recommended tolerance on the tongue dimensions is ±0.1mm.



Finally, the board width is also important to ensure that all boards will fit next to each other as the board stack is built up. The recommended tolerance on the board width is ±0.24mm.

Summary of tolerance recommendations

Head boards: Board thickness ±5% or ±0.24 mm across all parts of each board.

Edge and foot boards: Board width ±0.24 mm.
Tongue dimensions ±0.1 mm.

All boards: Glue groove dimensions: ±0.2 mm.
Board width (long dimensions): ±0.15 mm.
Board-positioning holes: ±0.15 mm.
All other features: 0.4 mm. [? not critical; we have to pick a number]

APPENDIX B

PCB Electrical Tolerances

DUNE APA Boards: Voltage Rating Review Using IPC-2221 Standards

Report prepared by:
Anthony C. Ezeribe (a.ezeribe@sheffield.ac.uk), Graham Miller (Graham.Miller@manchester.ac.uk)
for the DUNE APA board review task force
Date: 27th May 2020.

1.0 Introduction:

Printed circuit boards designed for operation of the DUNE Anode Plane Assemblies (APA) were reviewed using requirements from the IPC 2221 standards.

1.1 Geometry boards:

In total 8, 4, 7 and 10 types of the V, X, G and U geometry boards were tested, respectively. Charge readout wires on the APAs will be soldered on these geometry boards to be biased through either the G-bias filter or CR-boards (see section 1.2 for details) during operations in liquid argon. Any given set of geometry boards on the same wire plane will have a common voltage during the detector operations. However, for the electrical tension measurements, consecutive traces on the geometry boards/wire layer will be exposed to a maximum voltage of 480 V. For this, an extra 4% safety voltage was required so each of the geometry boards will be tested with a 500 V voltage rating. This 4% safety voltage margin was chosen due to the expected low trace/wire exposure times during the electrical tension measurements.

1.2 G-Bias Filter And CR Boards:

For the detector operation, G-bias filter boards are used to power the G-wire layer while CR-boards bias the U, V and X-wire layers connected through the custom-made Mill-Max pin slots. An additional 50% safety voltage margin was required in this operational mode for the respective wire layers to obtain a voltage rating of 998 V, 555 V, 0 V and 1230 V for the G, U, V and X wire layers, respectively.

2.0 Methodology:

The board design Gerber files were imported into Altium or Cuprum to extract minimum clearance between coated traces and uncoated soldering pads/signal vias on each board type. Results from these measurement were then used to calculate the maximum allowed differential voltages for the respective boards. The IPC-2221 computation tools used in these calculations were the Switched Mode Power Supply (SMPS) PCB trace spacing calculator [1] (for the G, U-geometry, G-bias filter and CR boards) and Saturn PCB Design software [2] (for the V and X-geometry boards). The reported maximum current for the G and U geometry board traces were determined using the Advanced Circuits 4PCB trace width calculator [3].

3.0 Results And Discussions:

Results of the minimum clearance measurements obtained from the G and U-geometry boards are shown on Table 1 with results from the G-bias filter board. See below for definitions of the variables used in Table 1 and 3:

Variable	Definition
Coated_T:	Minimum clearance between coated traces for a given board.
Max_V:	Maximum IPC-2221 allowed differential voltage for the clearance shown in the preceding column.
Op_V:	Expected operational voltage in LAr for the traces measured in the preceding column.
Max_I:	Maximum IPC-2221 allowed current for the traces measured in the preceding column.
Uncoated_T or UnCtd-UnCtd:	Minimum clearance between uncoated vias/soldering pads
UnCtd-Ctd:	Minimum clearance between coated traces and uncoated vias or soldering pad.
Internal_T:	Minimum clearance between internal traces.

It can be seen from Table 1 that the traces, soldering pads and signal vias on all of the tested seventeen G and U-geometry boards satisfied the IPC-2221 requirements for 500 V differential voltage as required for the electrical tension measurement. Highlighted in green and yellow are minimum clearances that can hold differential voltages that are greater than 550V and less than 550 V respectively. For the current rating, a worst cases would be an event that created about 10,000 electrons on a wire within the microsecond readout time-scale resulting in micro-amp scale signal current. This is well under the capability of trace widths in the current G and U-geometry board designs shown in Table 1 which can hold up to milli-amp scale currents.

The maximum differential voltage that can be allowed on the G-bias filter board is 300 V as shown on Table 1. This is below the IPC requirement for the electrical tension measurement. However, it can bias the G-layer wires during operation in LAr since all the G-layer wires are expected to be at the same potential during the detector operation.

Boards	S/N	Name	Ref on EDMS	Coated_T (mm)	Max_V (V)	Trace Width (mm)	Max_I (mA)	Uncoated_T (mm)	Max_V (V)	Internal_T (mm)	Max_V (V)
1	1	G Head Board Middle	8760121_revA3	1.199	630	0.305	367	2.792	557	NA	
	2	G Head Board Right-End	8760120_revA3	0.935	545	0.305	367	2.792	557	NA	
	3	G Head Board Left-End	8760122_revA3	1.065	588	0.305	367	2.792	557	NA	
2	4	G Edge Board Low Slot End	8760051_revA1	4.042	1563	0.75	705	2.589	517	NA	
	5	G Edge Board Middle	8760054_revA1	4.042	1563	0.75	705	2.589	517	NA	
	6	G Edge Board High Slot End	8760062_revA1	4.042	1563	0.75	705	2.589	517	NA	
	7	G Edge Board Position 4 and 7	8760113_revA1	4.042	1563	0.75	705	2.589	517	NA	
3	8	U Head Board Middle	8760115_revA3	1.245	648	0.305	367	2.551	510	NA	
	9	U Head Board Left End	8760119_revA3	1.245	648	0.305	367	2.552	510	NA	
	10	U Head Board Right End	8760123_revA3	1.149	615	0.305	367	2.651	530	NA	
4	11	U-Side Board End	8760038_revA2	1.354	680	0.406	452	5.965	1193	NA	
	12	U-Side Board Without Slot Mid	8760040_revA2	1.374	688	0.406	452	5.965	1193	NA	
	13	U-Side Board With Slot Middle	8760042_revA2	1.12	605	0.406	452	5.965	1193	1.12	848
5	14	U-Foot Board High Slot End	8760044_revA1	5	1878	0.75	705	3.547	710	NA	
	15	U-Foot Board Middle	8760057_revA1	5	1878	0.75	705	3.547	710	NA	
	16	U-Foot Board Low Slot End	8760059_revA1	5	1878	0.75	705	3.547	710	NA	
	17	U-Foot Board Position 4 And 7	8760111_revA1	5	1878	0.75	705	3.547	710	NA	
6	18	G-Plane Bias Filter Board	8760196_revA1	7.594	2725	0.406	452	2.2	300	NA	

Table 1: Results from the G, U-geometry and G-Bias filter boards. Green highlights **excellent** results while yellow highlights **good** results.

Table 2 shows that the minimum calculated spacing required for coated features is 0.8 mm and for uncoated features is 2.50 mm, both of these results use an input voltage rating of 500V corresponding to the requirements for the tension measurement tests. This voltage is the same for coated and uncoated features, as can be seen in the table. The calculated required trace clearance, as seen in columns J and K of Table 2 are less than the majority of the measured values shown in columns E and F signifying that most of boards meet the minimum IPC voltage clearance standard. Results from the V-Edge (middle) board (with ref. 8760028) which is highlighted in red in Table 2 almost meets the IPC requirements, however the minimum clearance on this board need to be increased by 0.1 mm.

A	B	C	D	E	F	G	H	I	J	K
Board number	Board type	Part	Number of layers	Minimum track/pad spacing based on PCB measurements (Coated – mm)	Minimum track/pad spacing based on PCB measurements (Uncoated – mm)	Specified voltage from Sebastien (V)	Input working voltage from calculator (V) (Coated – A5)	Input working voltage from calculator (V) (Uncoated – B2)	Calculated track/pad spacing mm (Coated – A5)	Calculated track/pad spacing mm (Uncoated – B2)
8760024	V	Edge	2	1.68	5.80	500.00	500.00	500.00	0.80	2.50
8760026	V	Edge	2	1.57	5.80	500.00	500.00	500.00	0.80	2.50
8760028	V	Edge	4	0.79	5.84	500.00	500.00	500.00	0.80	2.50
8760030	V	Edge	2	3.75	3.59	500.00	500.00	500.00	0.80	2.50
8760036	V	Edge	2	3.75	3.59	500.00	500.00	500.00	0.80	2.50
8760107	V	Edge	2	3.75	3.59	500.00	500.00	500.00	0.80	2.50
8760108	V	Head	2	1.20	2.80	500.00	500.00	500.00	0.80	2.50
8760116	V	Head	2	1.12	2.90	500.00	500.00	500.00	0.80	2.50
8760032	X	Edge	2	2.79	2.79	500.00	500.00	500.00	0.80	2.50
8760034	X	Edge	2	2.79	2.79	500.00	500.00	500.00	0.80	2.50
8760109	X	Edge	2	2.79	2.79	500.00	500.00	500.00	0.80	2.50
8760104	X	Head	2	1.00	2.79	500.00	500.00	500.00	0.80	2.50

Table 2: Results from the V and X geometry boards

Results from the current CR-board design is shown on the 2nd row (counting from the label row) of Table 3 while the 3rd row shows expected improvements from coating all the soldering pads and signal vias. It can be seen that the current design of the CR-boards does not satisfy the IPC-2221 requirements to allow the proposed operational voltages on the U and X-wire layers. However, the current CR- board design will meet the IPC standards (see the 3rd row) if all the vias and soldering pads are coated after the board assembly with at least a safety factor (Max_V/Op_V) of 1.3 as shown on the 3rd row of Table 3. This safety factor can be improved to 1.5, if the clearance around some identified areas on the board are increased by <0.5 mm in addition to coating of the vias and soldering pads.

A	B	C	D	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
Boards	S/N	Name	Ref on EDMS	UnCtd-Ctd (mm)	Max_V (V)	Op_V (V)	Rqd Spacing (mm)	Rqd Max_V (V)	UnCtd-UnCtd (mm)	Max_V (V)	Op_V (V)	Rqd Spacing (mm)	Rqd Max_V (V)	UnCtd-UnCtd (mm)	Max_V (V)	Op_V (V)	Rqd Spacing (mm)	Rqd Max_V (V)
11	30	CR Boards	8760144_revA2	2.764	551	820	4.59	1230	2.567	513	820	6.15	1230	2.491	450	370	2.78	555
				2.764	1144	820	3.03	1230	2.567	1081	820	3.03	1230	2.491	1054	370	0.97	555

Table 3: CR-Board results. Counting from the label row of the table: 2nd row shows the current design while the 3rd row shows expected improvements from coating the soldering pads and signal vias. **Green** highlights **excellent** results, **yellow** highlights **good** results while **red** shows areas that **failed** the tests.

4.0 Conclusion:

All the geometry boards shown in Table 1 and 2 satisfied the IPC-2221 minimum clearance requirements for the proposed electrical tension measurement except a V-Edge (middle) board (with ref. 8760028) that requires a 0.1 mm increase on its minimum trace clearance.

The G-bias filter board, also meets the IPC standards for the operational conditions but not for the differential voltage ratings needed for the electrical tension measurements hence, should

not be used in the tension measurements.

The CR-board will need some modifications before it can satisfy the IPC requirements. This can be achieved by increasing the minimum differential voltage clearance on the CR-board by <0.5 mm and coating all the vias/soldering pads. This way, the CR-board can meet the IPC standards for the operational voltages with a 1.5 safety factor.

5.0 Acknowledgment

Thanks to Andrew Laundrie (PSL) and Justin Evans (Manchester) for checking the IPC-2221 test results and reviewing this report.

6.0 References

1. https://www.smps.us/pcbtracespacing.html
2. http://saturnpcb.com/pcb_toolkit/
3. https://www.4pcb.com/trace-width-calculator.html

APPENDIX C

Press-fit Pin Tolerances

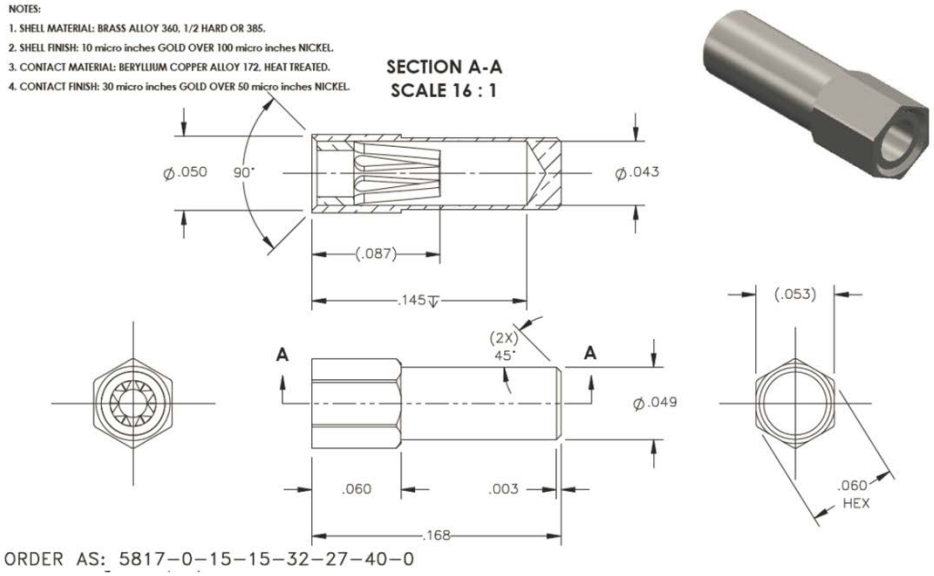
For plated through holes, Mill-Max recommends a hex or square profile along the pin barrel. The multi-faceted press-fit shape leaves a contiguous path of copper from the bottom of the hole to the top of the hole after press-fitting. The points along the diameter of the press-fit shape are intended to cut into the copper wall of plated through holes while the flats of the shape provide relief to minimize the risk of creating voids.

Hole sizes for multi-faceted press-fit pins require more consideration than standard plated through holes, with particular attention paid to the drill size used. The drill size should be slightly larger than the diameter of the points of the press-fit feature. For example, a discrete receptacle has a hexagonal across-points diameter of .109". The hole prior to plating should be Ø .1095" or 2.8mm. Finished hole diameters are typically .0005" smaller than the nominal drill size in FR-4. Thus, the nominal finished hole size with copper would be Ø .106".

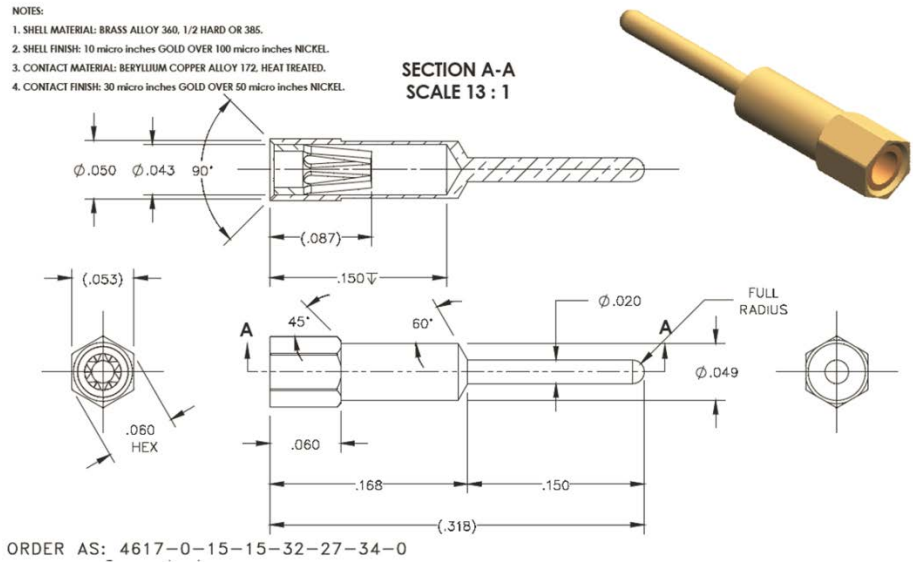
Mill-Max recommends that when specifying plated-through holes that receive multi-faceted press-fit pins, the PCB fabricator should be given the actual drill size prior to plating as well as a commercial finished hole tolerance of +/- 0.002”. The PCB manufacturer should also be instructed to mask the edges of panels in the copper plating tank to reduce excessive build-up of copper in the edge holes relative to holes in the center of the panel.

DUNE head boards and CR boards utilize custom Mill-Max receptacles both with and without “tails” which function as contact pins when the components are mated. They are hybrid designs that were developed from commercial designs already in production and adapted for the specific geometry of the APA.

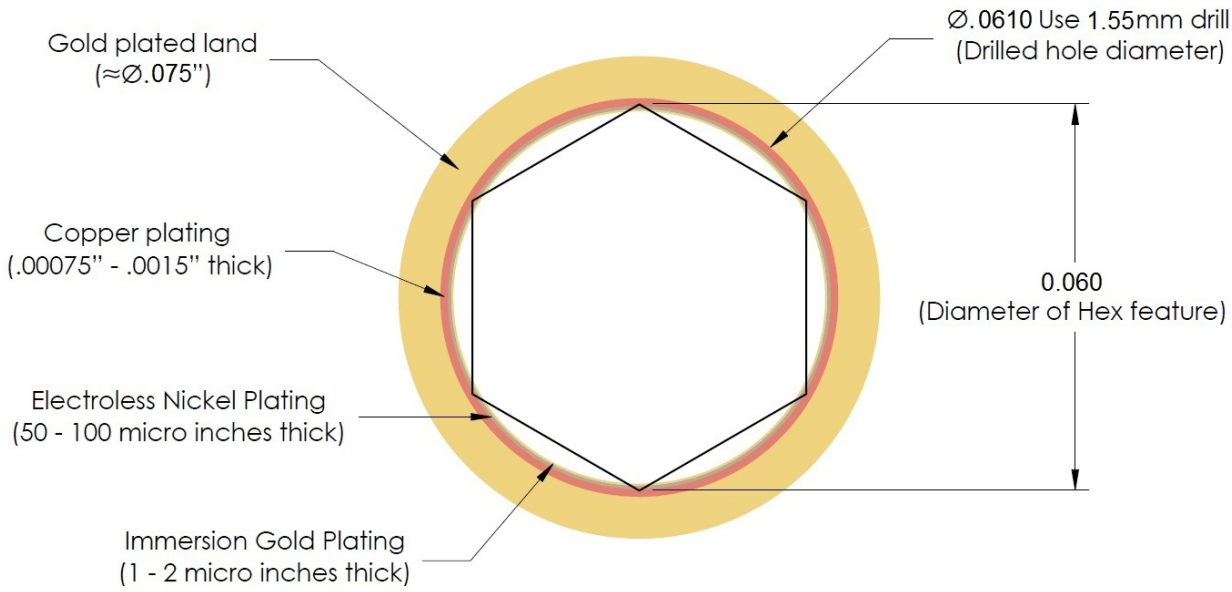
Receptacles without tails (X head boards):



Receptacles with tails (CR boards and V, U, and G head boards):



The custom components have a hexagonal across-points diameter of .060". The hole prior to plating through should be Ø .061" or 1.55 mm. The recommended copper plating thickness is 0.75 to 1.50 mils.



The required force to press each pin into place is approximately 20 lbs. Quality Assurance and Statistical Process Control measures should sample prototype and production boards to ensure that insertion forces are neither too little nor too great. Plated through holes should also be profiled to ensure that the correct drill size and plating thickness are being used.