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Research Article

Performance Analysis of Modified Drain Gating Techniques for Low Power and High Speed Arithmetic Circuits

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This paper presents several high performance and low power techniques for CMOS circuits. In these design methodologies, drain gating technique and its variations are modified by adding an additional NMOS sleep transistor at the output node which helps in faster discharge and thereby providing higher speed. In order to achieve high performance, the proposed design techniques trade power for performance in the delay critical sections of the circuit. Intensive simulations are performed using Cadence Virtuoso in a 45 nm standard CMOS technology at room temperature with supply voltage of 1.2 V. Comparative analysis of the present circuits with standard CMOS circuits shows smaller propagation delay and lesser power consumption.

1. Introduction

As we move on to finer MOSFET technologies, transistor delay has decreased remarkably which helped in achieving higher performance in CMOS VLSI processors. With technology scaling, it is required to reduce the threshold and power supply voltages. As square of power supply voltage is directly proportional to dynamic power dissipation, to achieve less consumption of power, supply voltage has to be reduced. Static power and dynamic power are two main components of total power dissipation. Static power consumption is calculated in the form of leakage current through each device. Substantial increase has been observed in subthreshold leakage current with scaling of threshold voltage [1]. Subthreshold current I_{ST} is given by [1]

$$I_{ST} = \mu_0 \mathrm{Cox} \left(\frac{W}{L}\right) (m-1) (V_T)^2 \times e^{(V_g - V_{th})/mV_T} \times \left(1 - e^{-V_{DS}/V_T}\right), \quad (1)$$

where

$$m = 1 + \frac{\mathrm{Cdm}}{\mathrm{Cox}}, \quad (2)$$

where thermal voltage, $V_T = KT/q$, μ_0 is the mobility, V_g is the gate voltage, V_{th} is the threshold voltage, V_{DS} is termed as drain to source voltage, and m is the body effect coefficient. Cdm and Cox are the depletion layer and gate oxide capacitances, respectively.

To counteract the excessive leakage in CMOS circuit, many architectural techniques have been proposed over the years. Power gating [2] and stacking effect [3] are two well-known techniques for reducing leakage power dissipation. Power gating normally makes use of sleep transistors that are connected either between the power supply and the pull-up network (PUN) or between the pull-down network (PDN) and ground. Sleep transistors are switched on when the circuit is evaluating and they are switched off in standby mode to conserve the leakage power in the logic circuit. Multi-threshold-CMOS (MTCMOS) [4] technique is also an effective way to achieve considerable decline in leakage power consumption. In MTCMOS technique, high V_{th} sleep transistors are added in the circuit whereas PUN and PDN use low V_{th} devices. In dual threshold circuits [5], low V_{th} devices are used in the delay critical sections and high V_{th} devices are used to reduce the leakage current in the circuitry.

Stacking of transistor in series reduces the subthreshold leakage current when one transistor is in the off state. Stacking effect is used in sleepy stack technique [6] and force stack technique [7]. Sleepy stack technique provides better results than forced stack technique. In forced stack, an extra sleep

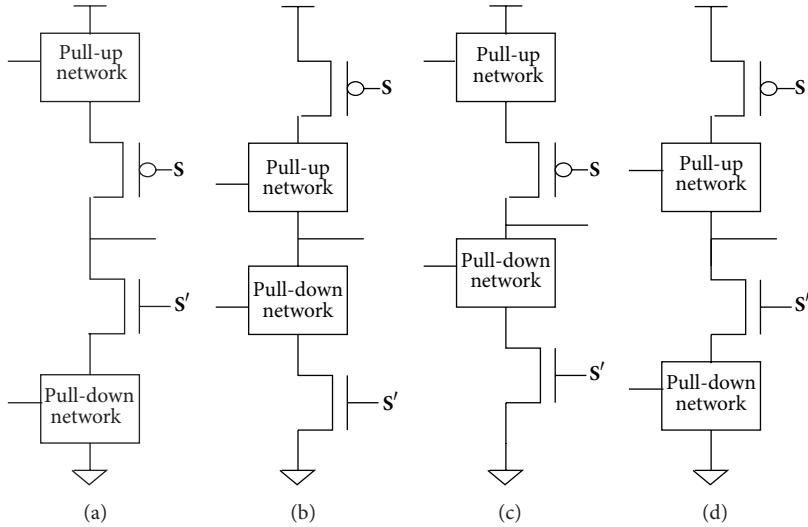

Figure 1: (a) Drain gating, (b) power gating, (c) drain-header and power-footer gating (DHPF), and (d) drain-footer and power-header gating (DFPH).

transistor is inserted for each input of the gate both in PUN and in PDN resulting in higher delay and area. In sleepy stack, an additional sleep transistor is connected in parallel with the transistor stack. This reduces the leakage current but at the same time delay in the circuit is increased.

LECTOR [8] and GALEOR [9] are also two leakage tolerant techniques. LECTOR makes use of two leakage control transistors (LCTs) that are connected between the PUN and PDN. In the same time GALEOR technique makes use of gated leakage transistors (GLTs). Both LCTs and GLTs reduce leakage by increasing the resistance between supply voltage and ground.

Another efficient technique to counter the leakage current problem is drain gating and its variation [10], explained in detail in Section 2. The modified circuits are proposed in Section 3. Simulation results taking NAND gate, 1-bit full adder, and 8-bit RCA (Ripple carry adder) as test bench circuits are enumerated in Section 4 and Section 5 provides the final conclusion.

2. Drain Gating Technique and Its Variant Circuits

In drain gating technique [10] shown in Figure 1(a), two sleep transistors are added between the PUN and PDN. PMOS transistor with sleep input **(S)** is connected between PUN and output node, whereas NMOS transistor with sleep input **(S′)** is inserted between the output node and PDN. When the circuit is in evaluation mode, the NMOS and PMOS sleep transistors are turned on resulting in low resistance conducting path. When the circuit is in standby, both transistors are switched off to reduce the standby power. Other variant circuits of drain gating are, namely, power gating, drain-header and power-footer gating (DHPF), and drain-footer and power-header gating (DFPH). In power gating technique, PMOS sleep transistor with input **(S)** is added between the power supply and the PUN, whereas NMOS sleep transistor with input **(S′)** is added between the PDN and ground as shown in Figure 1(b). The two mixed techniques DHPF and DFPH are shown in Figures 1(c) and 1(d), respectively. As the name suggests, in DHPF, a PMOS sleep switch is inserted between PUN and output node and an NMOS sleep switch is inserted between the PDN and ground rail. DFPH consists of an NMOS sleep switch between output node and PDN and a PMOS sleep switch between the power supply and the PUN. Comparative results in Section 4 indicate that power gating technique is the best leakage tolerant technique whereas drain gating technique has the least delay among the previously proposed circuits.

3. The Proposed High Speed Circuit Techniques

The proposed circuits are aimed at reducing the propagation delay incurred by drain gating technique and its variations. Four different circuit techniques, namely *high speed drain gating (HS-drain gating)*, *HS-power gating*, *HS-DHPF,* and *HS-DFPH* as shown in Figures 2(a), 2(b), 2(c), and 2(d) respectively, are proposed in this section. In *HS-drain gating* technique an additional sleep transistor with sleep input **(S)** is connected at the output node parallel to the NMOS sleep transistor **(S′)** and PDN. During the active mode, when the logic circuit evaluates the circuits output, the added NMOS sleep transistor **(S)** provides an additional discharging path in the circuit. This added transistor helps in speedy evaluation, hence providing higher speed. In a similar fashion, an additional NMOS sleep transistor with sleep input **(S)** is added to power gating, DHPF, and DFPH circuits.

The proposed cicuits have been verified by taking NAND gate, 1-bit full adder, and 8-bit RCA as test bench circuits. Experimental results in Section 4 prove that the modified HS-drain gating technique has the the least delay among

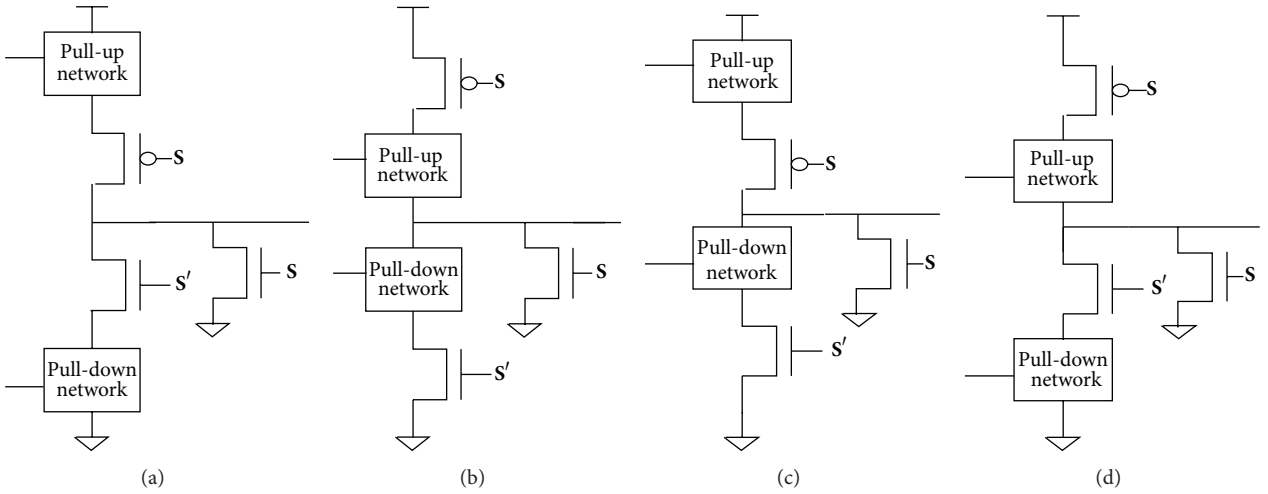

Figure 2: (a) HS-drain gating, (b) HS-power gating, (c) HS-DHPF, and (d) HS-DFPH.

Table 1: Power and delay values of NAND gate, FA, and 8-bit RCA using various techniques.

Circuit techniques	NAND gate		FA		8-bit RCA	
	Power (nW)	Delay (ps)	Power (nW)	Delay (ps)	Power (uW)	Delay (ps)
Standard CMOS	22.32	45*e*3	2.1*e*3	30*e*3	52.2	23.7*e*3
Drain gating	12.63	25*e*3	393	15*e*3	7.53	8.85*e*3
Power gating	8.73	205*e*3	238	150*e*3	2.39	20.5*e*3
DHPF	11.08	80*e*3	340	25*e*3	3.02	12*e*3
DFPH	8.71	175*e*3	245	150*e*3	4.02	15.5*e*3
HS-drain gating	18.42	2.22	250	15.08	6.97	10.3
HS-power gating	16.57	11.76	246	49.9	2.13	21.4
HS-DHPF	16.70	6.3	248	35.97	4.15	11.9
HS-DFPH	16.64	11.71	247	44.87	2.92	17

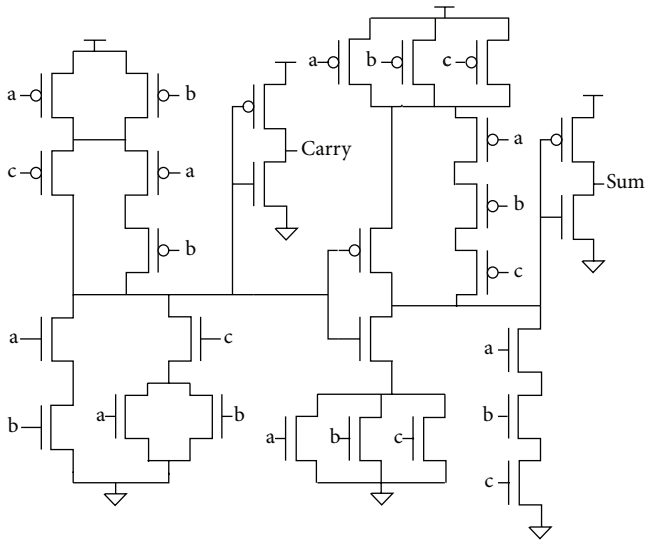

Figure 3: 1-bit CMOS full adder.

the existing and proposed architectural techniques as shown in Figure 5. Also HS-power gating technique has the lowest power as compared to standard CMOS circuit and the newly proposed circuits as shown in Table 1. The ratio of PMOS to NMOS size is set to be equal to 2.

Two-input NAND gate using HS-drain gating operates in two modes, namely, *sleep or standby mode* and *active mode*. When the circuit is in active mode, sleep input **(S)** is in low state, and output node gets charged to power supply voltage. Both NMOS and PMOS sleep transistors connected between PUN and PDN are turned on and output is evaluated. For example, if we provide input to the PUN as 0(XX) where XX stands for input vectors (00, 01, 10, 11), output will be high for the first three cases and low for the fourth case for the NAND gate. Sleep signal should be provided in the form of alternate high and low signals. When sleep signal **(S = 1)**, both PMOS and NMOS sleep transistors between PUN and PDN network turn off and additional NMOS sleep transistor is turned on, discharging the output node to ground thereby resulting in higher performance. A trade-off is achieved between power and delay so as to maintain high speed in the proposed circuits.

4. Simulations and Results

Two-input NAND gate, 1-bit full adder, and 8-bit RCA are implemented using the proposed high speed architectural techniques. The circuit diagrams for 1-bit full adder and 8-bit RCA are shown in Figures 3 and 4, respectively. Each stage in 8-bit RCA consists of a 1-bit full adder (FA). Each FA circuit consists of 28 transistors. In RCA, carry is propagated from one stage to another and final carry is obtained as C_8 shown in Figure 4.

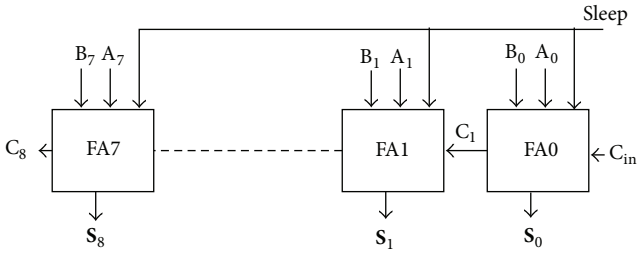

Figure 4: 8-bit RCA.

The total power consumption and propagation delay of various existing and proposed techniques for NAND gate, FA, and 8-bit RCA are compared in Table 1. HS-drain gating technique has the least delay. HS-power gating, HS-DFPH, and HS-DHPF suffer from 50%, 39%, and 13% propagation delay with respect to HS-drain gating technique. Standard drain gating and its variants circuit techniques suffer from 99% propagation delay in comparison with HS-drain gating technique. Circuits employing HS-power gating technique have very low power consumption. Power savings of nearly 85% are achieved in arithmetic architectures employing HS-power gating technique. HS-drain gating technique has the least power saving among the proposed circuits. HS-DHPF and HS-DFPH techniques optimize the power and delay in CMOS arithmetic circuits.

The corner analysis for the drain gating design and its variants is plotted along with that of the modified high speed counterparts. Figure 5 shows the temperature versus the propagation delay graph for 8-bit RCA using the existing techniques and the proposed techniques.

Similarly Figure 6 shows the plot of process corners versus the propagation delay of 8-bit RCA using the existing techniques and the proposed techniques.

On observing the comparative graph shown in Figures 5 and 6, we can infer that the designs made using the modified high speed drain gating technique and its corresponding variants have substantial reduction in the propagation delay when compared to the designs made using the CMOS, drain gating technique, and its variants.

5. Conclusions

In this paper, we have tabulated the total power consumption and the propagation delay for certain circuits using the existing low power and performance enhancing techniques and the newly proposed ones. Also we have made a comparative study of these techniques for the parameters like temperature, process corners, and propagation delay. Simulation results show that the proposed circuits work effectively even at extreme temperature and at different transistor configurations.

From the above mentioned experimental data, we can observe that, by implementing the high speed modified designs for the drain gating technique and its variants, we are able to enhance the performance of the design at lower power

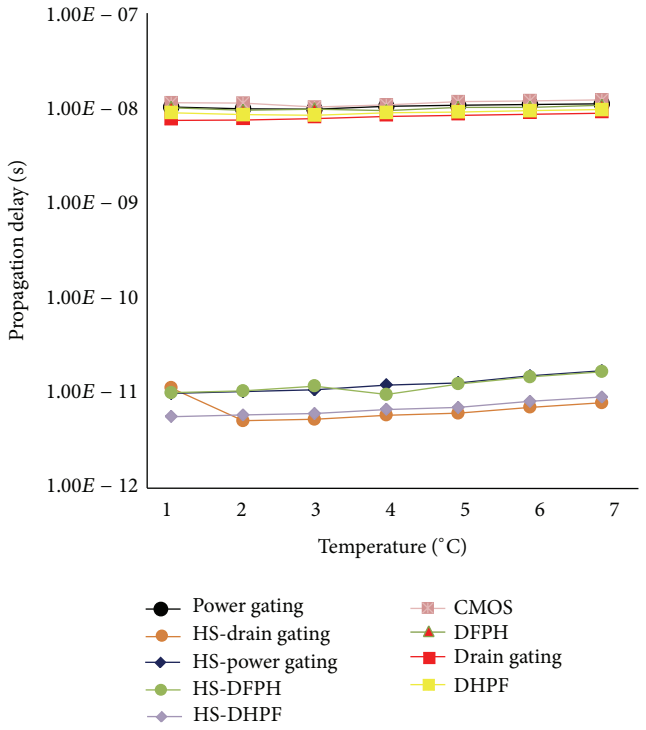

Figure 5: Temperature versus the propagation delay for the existing and the proposed techniques.

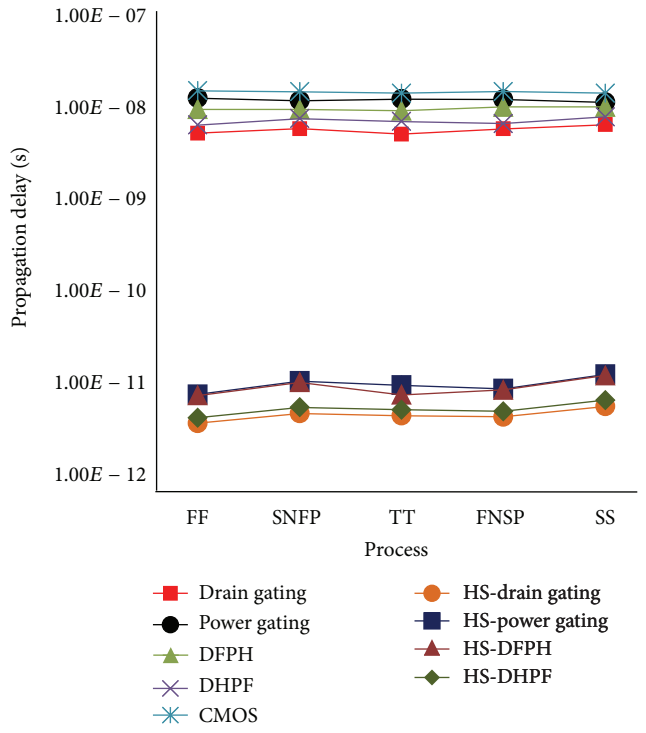

Figure 6: Process versus the propagation delay for 8-bit RCA using the existing and the proposed techniques.

consumption. Power consumption savings as observed in 8-bit RCA and 1-bit full adder are 95% and 88%, respectively, whereas propagation delay has been reduced by almost 99% in both RCA and full adder circuit.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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