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Research Article

On Improving the Performance of Dynamic DCVSL Circuits

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This contribution aims at improving the performance of Dynamic Differential Cascode Voltage Switch Logic (Dy-DCVSL) and Enhanced Dynamic Differential Cascode Voltage Switch Logic (EDCVSL) and suggests three architectures for the same. The first architecture uses transmission gates (TG) to reduce the logic tree depth and width, which results in speed improvement. As leakage is a dominant issue in lower technology nodes, the second architecture is proposed by adapting the leakage control technique (LECTOR) in Dy-DCVSL and EDCVSL. The third proposed architecture combines features of both the first and the second architectures. The operation of the proposed architectures has been verified through extensive simulations with different CMOS submicron technology nodes (90 nm, 65 nm, and 45 nm). The delay of the gates based on the first architecture remains almost the same for different functionalities. It is also observed that Dy-DCVSL gates are 1.6 to 1.4 times faster than their conventional counterpart. The gates based on the second architecture show a maximum of 74.3% leakage power reduction. Also, it is observed that the percentage of reduction in leakage power increases with technology scaling. Lastly, the gates based on the third architecture achieve similar leakage power reduction values to the second one but are not able to exhibit the same speed advantage as achieved with the first architecture.

1. Introduction

Digital design space is filled with a variety of logic styles suitable for different applications [1–6]. Conventionally static CMOS has predominance over remaining styles due to the low static power consumption. Differential Cascode Voltage Switch Logic (DCVSL) [6] is a static style which is beneficial from circuit delay, layout density, logic flexibility, and power consumption. The DCVSL has been employed to develop various circuits for fault tolerance [7], ternary logic [8], micro pipelining [9], delay cell [10], ring oscillator [11], capacitor neutralization [12], and so forth. It is well known that static logic styles suffer from high power consumption when output switches its logic state, a situation which worsens with increasing clock frequencies. The performance can be improved by using the dynamic version of DCVSL which is based on precharge-evaluation logic. Many clocked versions of DCVSL style named dynamic DCVSL (Dy-DCVSL) and enhanced DCVSL (EDCVSL) [13] are presented in the literature. As the speed of the dynamic circuit depends on logic tree depth and width [13], this paper proposes an architecture to reduce logic tree depth by employing transmission gates in logic function realization. Apart from the speed issue, leakage currents are yet another concern that shows predominance in submicron technologies. Leakage loss occurs when the output is stable (i.e., low output or high output). A new architecture incorporating the leakage control technique [14] in dynamic DCVSL circuits is put forward, which reduces leakage current. The features of the former architectures are combined to present a third architecture.

The paper is arranged in five sections including the present one. Section 2 briefly presents existing dynamic DCVSL and EDCVSL circuits. Section 3 describes the proposed dynamic DCVSL circuits. The functional verification and performance of the proposal are placed in Section 4 and conclusions are drawn in Section 5.

2. Dynamic Differential Cascode Voltage Switch Logic Family

Differential Cascode Voltage Switch Logic (DCVSL) is a differential style derived from conventional CMOS logic and

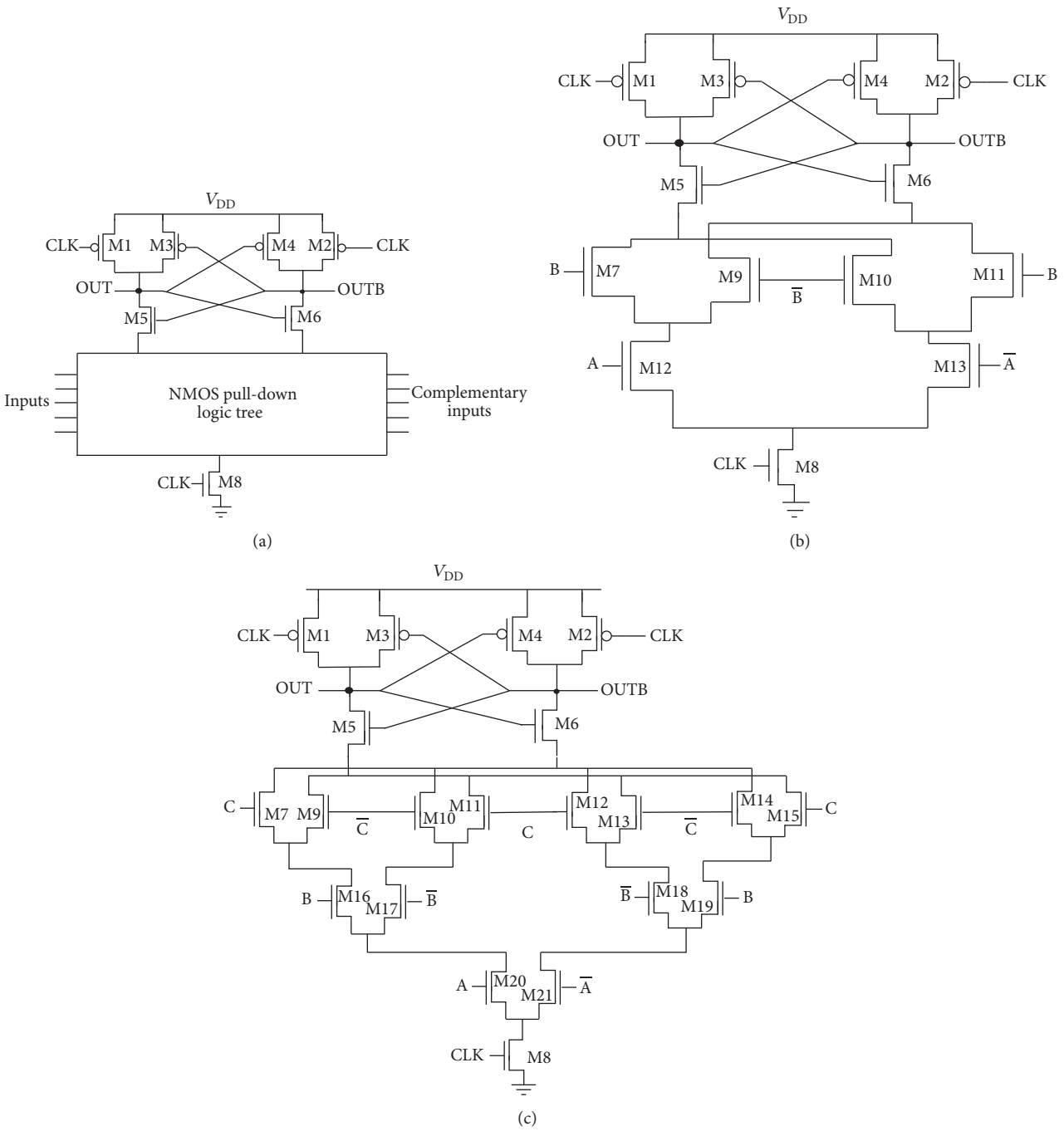

Figure 1: (a) Generic architecture of Dy-DCVSL circuit: (b) two- and (c) three-input Dy-DCVSL XOR-XNOR gate.

ratioed pseudo NMOS logic. It combines their advantages and provides a high speed, area efficient, and rail-to-rail logic design alternative. Both the static and the dynamic versions of the DCVSL style are available in open literature. This section briefly describes existing dynamic DCVSL styles (Dy-DCVSL).

2.1. Conventional Dy-DCVSL Architecture. The generic architecture of a Dy-DCVSL gate is shown in Figure 1(a). It consists of a pull-down network (PDN) that implements the logic function (OUT) as well as its complement (OUTB) using NMOS transistors only. The operation of the circuit depends on clock signal (CLK). It works in precharge phase for low CLK signal and in evaluation phase otherwise. In the precharge phase, the transistors M1 and M2 are ON and transistors M3 and M4 remain OFF, so both output nodes are precharged to high ($=V_{DD}$) logic level. Any change in the inputs during this phase will not affect the output nodes' potential as a current path from the output nodes to the ground could not be established. A high CLK signal makes

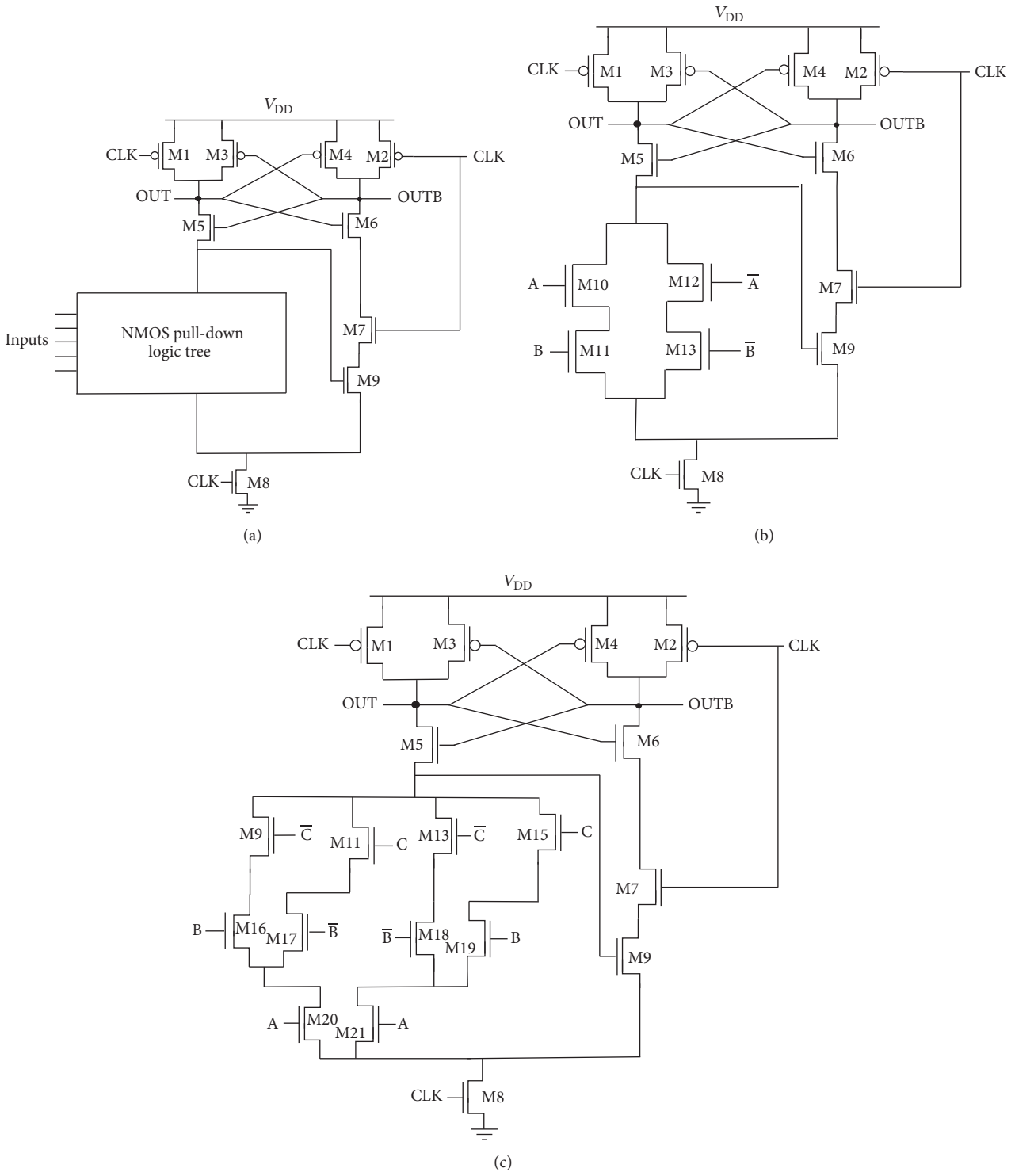

Figure 2: (a) Generic architecture of EDCVSL circuit: (b) two-input and (c) three-input EDCVSL XOR-XNOR gate.

transistors M1 and M2 OFF. One of the output nodes attains a low logic level depending on the value of inputs.

Cross-coupled transistors M3 and M4 help output to switch and transistors M5 and M6 accelerate this process [13]. The circuits of two- and three-input Dy-DCVSL XOR-XNOR gates are shown in Figures 1(b) and 1(c) as illustrations.

2.2. Conventional EDCVSL Architecture. The generic architecture of the EDCVSL circuits is drawn in Figure 2(a) and two/three-input EDCVSL XOR-XNOR gate is shown as an example in Figures 2(b) and 2(c). It is similar to Dy-DCVSL except for PDN where only one logic tree branch (OUT) is retained and the other is replaced by two stacked transistors

M7 and M9. The gate of transistor M7 is connected to CLK signal so it is activated in the evaluation phases only. The transistor M9 is connected to the output of the logic tree branch to achieve complementary operation. To elaborate the behavior, consider schematic of Figure 2(b). In the precharge phase, both outputs are precharged and the NMOS cross-coupled transistors M5 and M6 are ON but have no effect on output as M8 is OFF. In the evaluation phase, for low (high) values at both inputs, the transistors M12 and M13 (M10 and M11) are ON and therefore transistor M9 is OFF. So, OUTB remains high and M5 retains its ON state and finally OUT becomes low. For the case when one input is high and the other is low, no path exists between OUT and the ground so it remains high and OUTB goes low. The operation of three-input EDCVSL XOR-XNOR gate is similar to two-input EDCVSL XOR-XNOR gate and is omitted for the sake of brevity.

3. The Proposed Dynamic DCVSL Circuits

This section presents three new architectures to improve performance of existing Dy-DCVSL and EDCVSL. The first architecture aims at speed improvement, the second works on leakage reduction, and the third combines features of the first two architectures to see their combined effect on performance.

3.1. Proposed Architecture-1 (PA-1). Proposed architecture-1 is based on shifting the function realized by PDN logic tree to a separate block and using transmission gates (TG) logic for its implementation. The new Dy-DCVSL and EDCVSL circuits based on architecture-1 are named Dynamic TG based DCVSL (Dy-TG-DCVSL) and Dynamic TG based EDCVSL (TG-EDCVSL) circuits, respectively. A generic architecture of Dy-TG-DCVSL circuit along with two- and three-input XOR-XNOR realization is depicted in Figure 3. The PDN logic tree consists of two NMOS transistors which are controlled by the outputs of two separate blocks. The two blocks generate the complementary outputs such that either M9 or M10 is ON during evaluation.

The working of the proposed Dy-TG-DCVSL XOR2 gate can be explained for the two phases. The operation in precharge phase is the same as conventional Dy-DCVSL. Any changes in the inputs A and B may update the gate potential of M9 and M10 but will not affect the output, since M8 is OFF. Consequently, when CLK becomes high, the output gets evaluated according to the gate potential of M9 and M10. In comparison to the conventional Dy-DCVSL XOR-XNOR gate (Figure 1(b)), there is a speed advantage in terms of evaluation time due to the fact that the intermediate computation of the function is completed in the separate blocks just prior to the start of the evaluation phase. Also, a closer examination of the proposed architecture reveals a unique advantage of maintaining a constant evaluation time irrespective of the realized functionality. Similarly, placing logic functionality of EDCVSL in separate block logic leads to the proposed TG-EDCVSL architecture. Generic gate structure, two- and three-input XOR-XNOR gates are depicted in Figure 4.

3.2. Proposed Architecture-2 (PA-2). The differential nature of the DCVSL logic style has several advantages but in submicron regions it needs attention. For all input combinations, one of the two logic tree branches in the PDN will be conducting while the other would remain nonconducting. The nonconducting branch in submicron regions would have some amount of current due to OFF transistors in the path in both precharge and evaluation phases. This current can be classified as leakage current. To improve the performance in submicron region, these currents need to be minimized. Various leakage reduction techniques based on the use of sleep transistor [15] and high threshold voltage transistors [16] are available for static DCVSL circuits. These techniques require either routing of sleep signal [15] or a complex algorithm for selection of high threshold voltage transistors. A self-controlled technique named LECTOR [14] is presented for CMOS circuits, which reduces both types of currents and is adapted for dynamic DCVSL circuits, and the resulting topology is referred to as proposed architecture-2 (PA-2). LECTOR technique introduces two leakage control transistors (PMOS and NMOS) in between the PUN and the PDN of the logic gate with the gate terminal of each of the leakage control transistors (LCTs) controlled by the source of the other. This arrangement ensures that one of the LCTs is always in the "near-cut-off region" for any possible input combination. This results in an increase in the resistance of the path from the power supply to the ground, leading to a substantial drop in leakage currents through the path [14]. A further modification in achieving much more leakage control is to use high Vth LCTs. The architectures incorporating LECTOR technique in Dy-DCVSL and EDCVSL circuits are shown in Figure 5. The proposed architectures add four high Vth LCTs (LCT1–LCT4) in the basic architectures of the Dy-DCVSL (Figure 1(a)) and EDCVSL (Figure 2(a)) circuits and are called Dy-DCVSL-LCT and EDCVSL-LCT, respectively.

To understand the leakage control mechanism in Dy-DCVSL-LCT and EDCVSL-LCT circuits, the operating regions of LCTs during precharge and evaluation phases are examined. In the precharge phase, both the OUT and the OUTB are at V_{DD}. Under this condition, it can be observed that the transistor LCT2 is ON and LCT1 is in near-cut-off state. Thus, LCT1 offers more impedance along the path and reduces the leakage current. Similar behavior can be observed when a high voltage is obtained at the output in the evaluation phase.

3.3. Proposed Architecture-3 (PA-3). Proposed architecture-3 combines the features of proposed architecture-1 and proposed architecture-2. The resulting Dy-DCVSL and EDCVSL structures are called Dy-TG-DCVSL-LCT and TG-EDCVSL-LCT. The proposed architectures are shown in Figure 6.

4. Simulation Results

This section presents the simulation results for the new Dy-DCVSL circuits based on the proposed architectures. The simulations are performed using Symica tool and the PTM technology parameters for 90 nm, 65 nm, and 45 nm nodes. The frequencies of the inputs CLK, A, B, and C are 50 MHz,

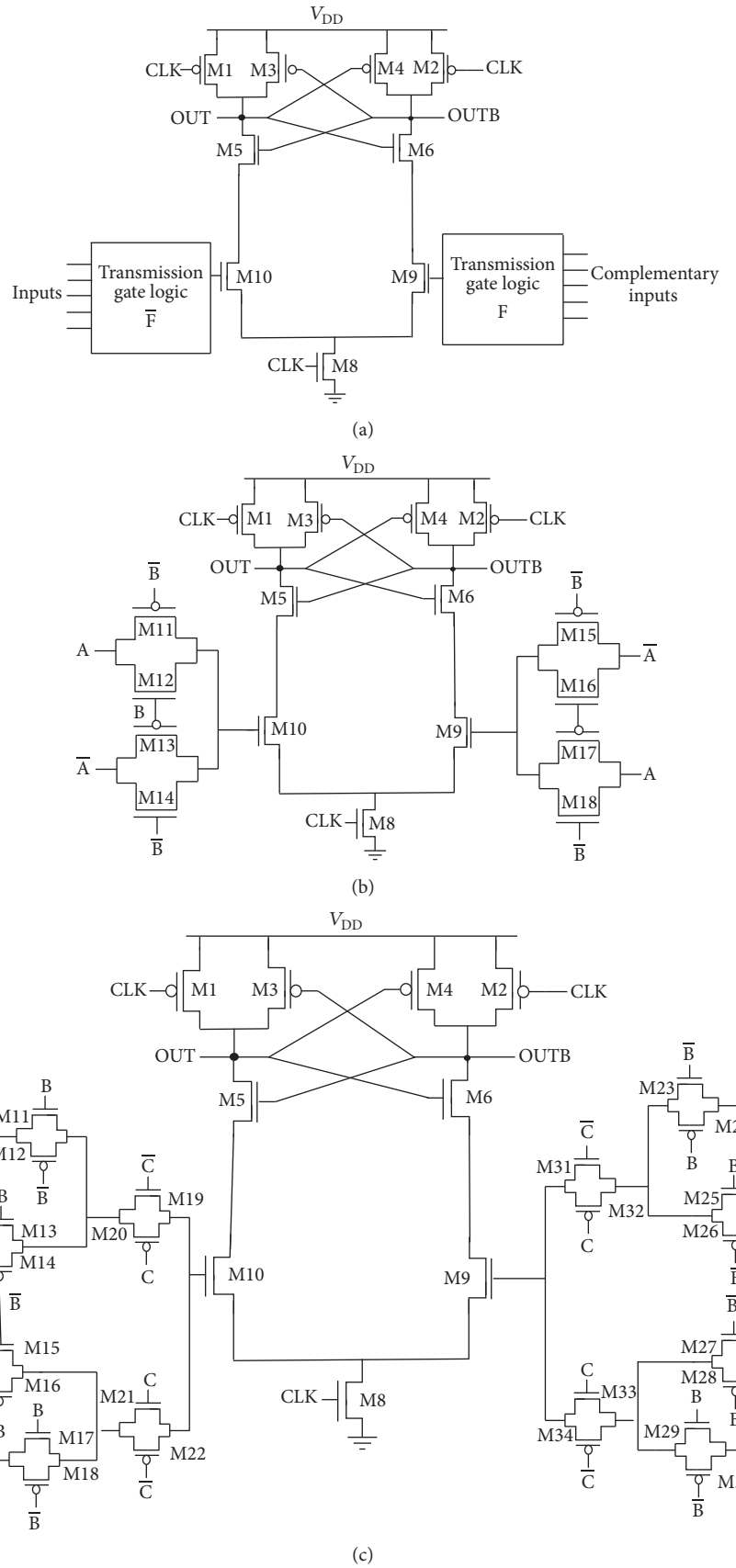

Figure 3: (a) Proposed architecture-1 for Dy-TG-DCVSL circuits. (b) Two-input and (c) three-input Dy-TG-DCVSL XOR-XNOR gate.

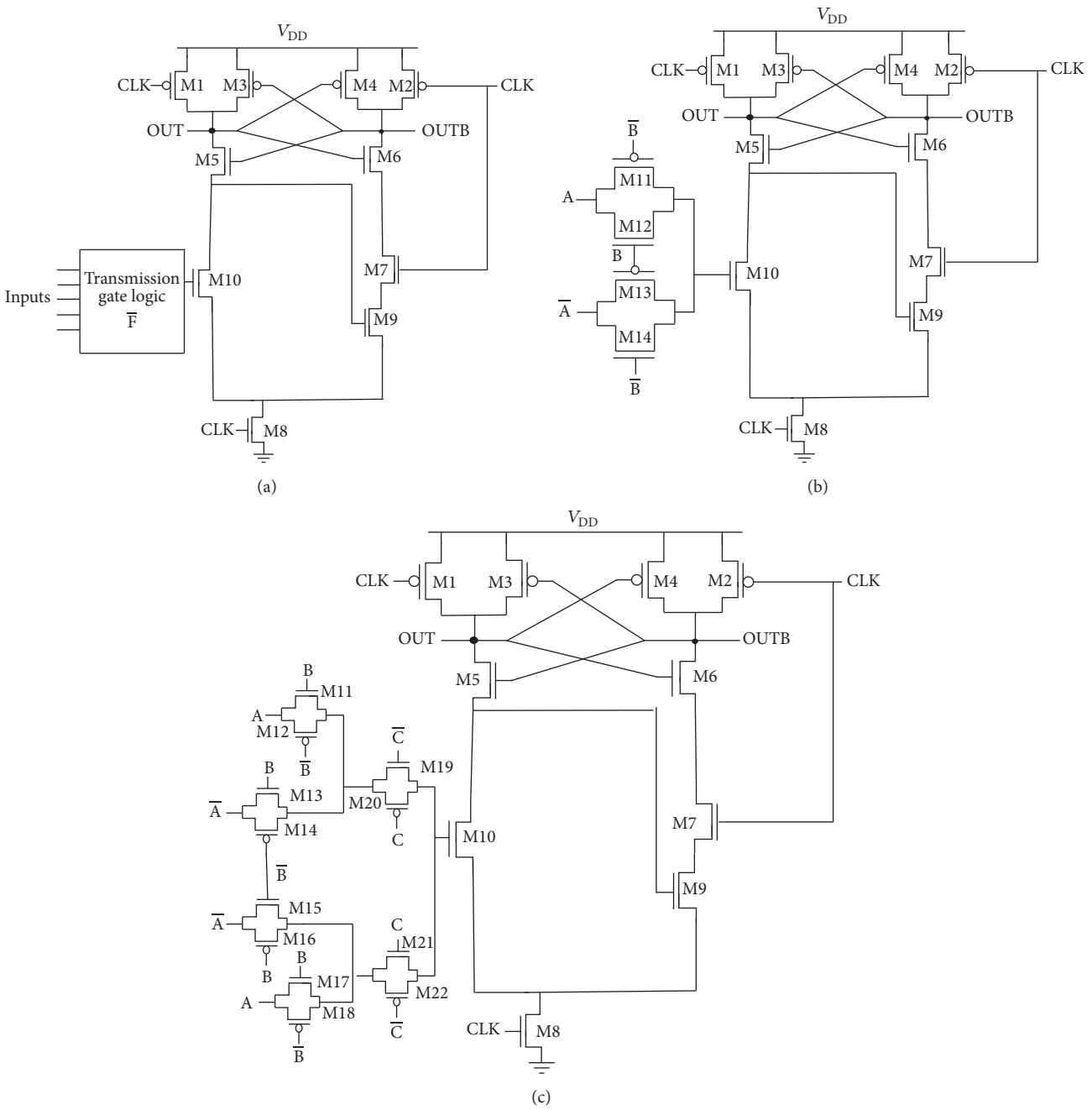

Figure 4: (a) Proposed architecture-1 for TG-EDCVSL circuits. (b) Two-input and (c) three-input TG-EDCVSL XOR-XNOR gates.

25 MHz, 12.5 MHz, and 6.25 MHz, respectively. FO4 of inverters is maintained as the load in all the gates. The results are categorized into three sections according to the proposed architectures. The leakage power is computed on the basis of leakage current and the power supply.

4.1. Simulation Results with PA-1. Dy-TG-DCVSL and TG-EDCVSL based two-input AND-NAND (AND-NAND2), three-input AND-NAND (AND-NAND3), two-input exclusive-OR (XOR-XNOR2), and three-input exclusive-OR (XOR-XNOR3) circuits are simulated using 90 nm CMOS technology parameters. The simulation waveforms of the Dy-TG-DCVSL and TG-EDCVSL XOR-XNOR2 and XOR-XNOR3 gates are shown in Figure 7. For all the gates, it can be observed that, for low value of the CLK signal, both output nodes are precharged to V_{DD} (=1.8 V). The voltage changes in the input signals A and B during this phase do not affect the potential of the output nodes. In the evaluation phase, for the same value of the inputs A and B (Figure 7(a)), the output node OUT remains low. Similarly, when the inputs differ,

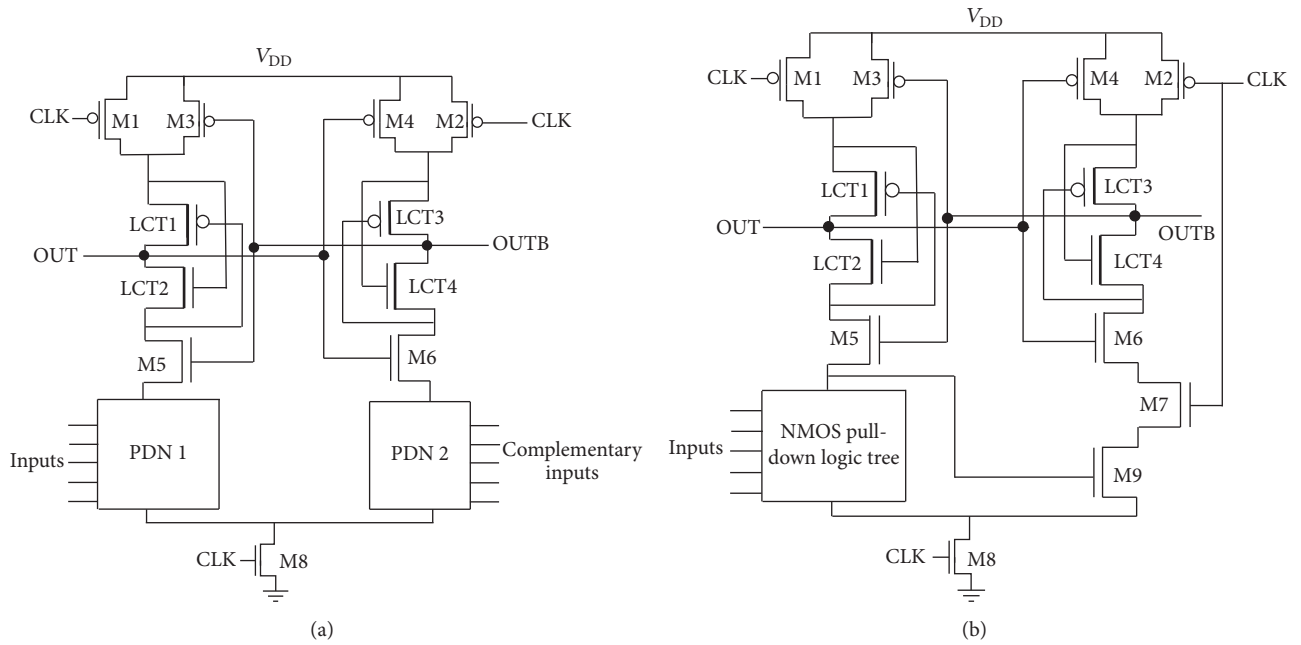

Figure 5: Proposed architecture-2 for (a) Dy-DCVSL-LCT circuits and (b) EDCVSL-LCT circuits.

a high voltage level is obtained at the output node OUT. Thus, the XOR functionality is achieved in the proposed Dy-TG-DCVSL and TG-EDCVSL XOR2 gates. The simulation waveform for Dy-TG-DCVSL and TG-EDCVSL XOR-XNOR3 gate is shown in Figure 7(b). Similar waveforms were achieved for the other gates and are omitted for the sake of brevity.

The gates are also designed in Dy-DCVSL and EDCVSL styles to analyze the speed advantage. The corresponding delay results are noted and enlisted in Table 1. The results clearly indicate the speed advantage of PA-1 based gates over the conventional counterparts. Also, the TG-EDCVSL gates are the fastest among all the logic styles. Lastly, the PA-1 based gates show almost equal delay values irrespective of the implemented functionality.

4.2. Simulation Results with PA-2. In this category, the leakage current reduction through incorporation of LECTOR technique in dynamic DCVSL circuits is demonstrated. An XOR-XNOR2 gate is chosen as the test bench due to its wide range of applications. The conventional Dy-DCVSL, EDCVSL, Dy-DCVSL-LCT, and EDCVSL-LCT XOR-XNOR2 gate circuits are simulated at various submicron technology nodes such as 90 nm, 65 nm, and 45 nm. Table 2 lists the leakage power for the conventional Dy-DCVSL, EDCVSL, Dy-DCVSL-LCT, and EDCVSL-LCT XOR-XNOR2 gate with V_{DD} = 1.2 V.

The following observations are made from Table 2:

(1) The percentage reduction ranges in the leakage power are 30.4%–56.6% for 90 nm, 32.2%–61% for 65 nm, and 33.8%–74.3% for 45 nm.

(2) Leakage power tends to follow an increasing trend with the scaling down of the technology.

(3) An increase in percentage reduction is seen as we dig down the lower technology nodes.

4.3. Simulation Results with PA-3. Dy-TG-DCVSL, TG-EDCVSL, Dy-TG-DCVSL-LCT, and TG-EDCVSL-LCT two-input XOR2 and three-input XOR3 gates are simulated at various technology nodes. Out of the two dynamic styles, the results pertaining to EDCVSL circuits are listed in Tables 3–5 for the leakage power and delay measurements. The delays reported in Table 5 are for 45 nm technology node. The findings can be summarized as follows:

(1) A percentage reduction range of 27%–64% for 90 nm, 30%–66% for 65 nm, and 38%–76% for 45 nm in leakage power is observed.

(2) The TG-EDCVSL-LCT XOR-XNOR2 gate shows less leakage power with respect to Dy-TG-DCVSL counterpart.

(3) Leakage power tends to follow an increasing trend with the scaling down of the technology.

(4) The percentage reduction in the leakage power increases with the lower technology nodes.

(5) The delay of the TG-EDCVSL-LCT XOR-XNOR2 gate is more than the Dy-TG-DCVSL due to the presence of the high resistance path for leakage current reduction, thus exhibiting a trade-off between the speed and leakage power reduction.

5. Conclusion

In this paper, three new architectures to enhance the performance of Dy-DCVSL and EDCVSL are proposed. The first

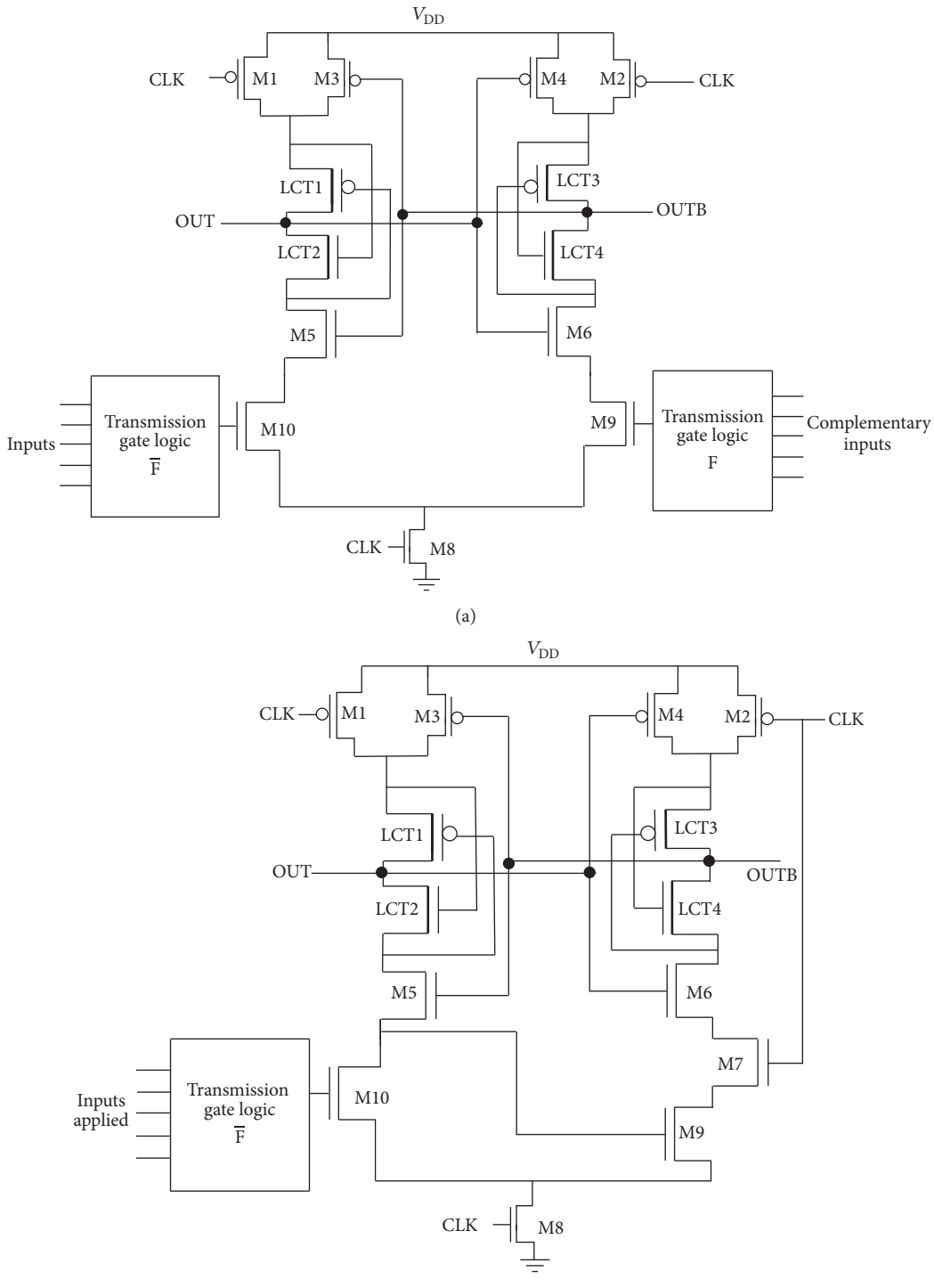

Figure 6: Proposed architecture-3 based (a) Dy-TG-DCVSL-LCT and (b) TG-EDCVSL-LCT circuits.

improves the speed by using transmission gates through logic tree depth reduction. The second architecture is derived to reduce leakage power at lower technology nodes. The incorporation of leakage control by incorporating LECTOR technique is proposed. The third architecture merges the two proposed architectural modifications to analyze their combined effect on the performance. Extensive simulations are done at various CNOS submicron technology nodes such as 90 nm, 65 nm, and 45 nm. It is observed that dynamic DCVSL gates based on the first architecture are 1.6 to 1.4 times faster than the conventional dynamic CVSL circuits. The gates based on the first architecture show almost equal delay values

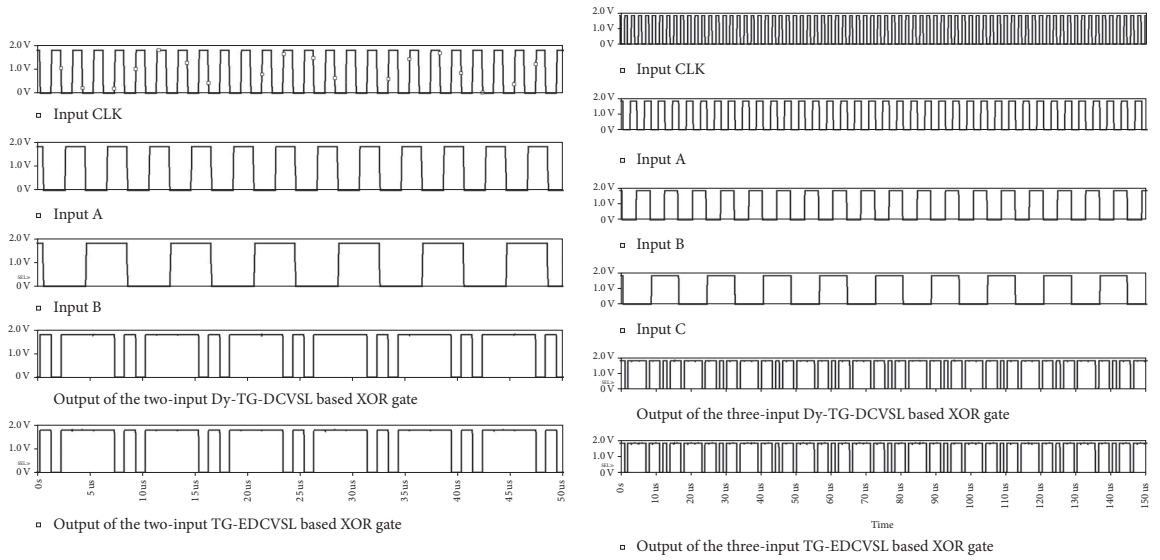

Figure 7: Simulation waveform of Dy-TG-DCVSL and TG-EDCVSL based (a) two-input XOR-XNOR gate and (b) three-input XOR-XNOR gate.

Table 1: Summary of delay results (ps).

Gate	Style			
	Dy-DCVSL	EDCVSL	Dy-TG-DCVSL	TG-EDCVSL
AND-NAND2	500	480	350	340
AND-NAND3	570	530	355	345
XOR-XNOR2	500	480	350	341
XOR-XNOR3	550	490	355	345

Table 2: Leakage power (nW) for the conventional Dy-DCVSL, EDCVSL-LCT and PA-2 Dy-DCVSL-LCT, EDCVSL-LCT based XOR-XNOR2 gate topologies.

Inputs		Architecture					
		Conventional		PA-2		Reduction with respect to conventional (%)	
A	B	Dy-DCVSL	EDCVSL	Dy-DCVSL-LCT	EDCVSL-LCT	Dy-DCVSL-LCT	EDCVSL-LCT
90 nm node							
0	0	9.27	8.9	4.02	4.06	56.6	54
0	1	0.23	0.21	0.16	0.14	30.4	33
1	0	0.23	0.21	0.16	0.14	30.4	33
1	1	9.27	8.9	4.02	4.06	56.6	54
65 nm node							
0	0	12.9	12.88	5.16	5	60	61
0	1	0.41	0.27	0.27	0.18	32.2	33.3
1	0	0.41	0.27	0.27	0.18	32.2	33.3
1	1	12.9	12.88	5.16	5	60	61
45 nm node							
0	0	22.48	22.48	5.79	5.79	74	74.3
0	1	0.41	0.28	0.28	0.18	33.8	35.7
1	0	0.41	0.28	0.28	0.18	33.8	35.7
1	1	22.48	22.48	5.79	5.79	74	74.3

Table 3: Leakage power (nW) for TG-EDCVSL and TG-EDCVSL-LCT based XOR-XNOR2 gate topologies.

Inputs		Architecture		
A	B	TG-EDCVSL	TG-EDCVSL-LCT	Reduction with respect to TG-EDCVSL (%)
		90 nm node		
0	0	8.8	4	55
0	1	0.18	0.13	27
1	0	0.18	0.13	27
1	1	8.8	4	55
		65 nm node		
0	0	12.7	5	61
0	1	0.2	0.14	30
1	0	0.2	0.14	30
1	1	12.7	5	61
		45 nm node		
0	0	22.24	5.7	74.3
0	1	0.21	0.13	38
1	0	0.21	0.13	38
1	1	22.24	5.7	74.3

Table 4: Leakage power (nW) in TG-EDCVSL and TG-EDCVSL-LCT three-input XOR-XNOR gates.

Inputs			Architecture		
A	B	C	TG-EDCVSL	TG-EDCVSL-LCT	Reduction with respect to TG-EDCVSL (%)
			90 nm node		
0	0	0	9.8	4	59
0	0	1	0.34	0.21	64
0	1	0	0.34	0.21	64
0	1	1	9.8	4	59
1	0	0	0.34	0.21	64
1	0	1	9.8	4	59
1	1	0	9.8	4	59
1	1	1	0.34	0.21	64
			65 nm node		
0	0	0	14	5.07	63
0	0	1	0.38	0.26	66
0	1	0	14	5.07	63
0	1	1	0.38	0.26	66
1	0	0	0.38	0.26	66
1	0	1	14	5.07	63
1	1	0	14	5.07	63
1	1	1	0.38	0.26	66
			45 nm node		
0	0	0	24.5	5.85	76
0	0	1	0.43	0.12	72
0	1	0	0.43	0.12	72
0	1	1	24.5	5.85	76
1	0	0	0.43	0.12	72
1	0	1	24.5	5.85	76
1	1	0	24.5	5.85	76
1	1	1	0.43	0.12	72

Table 5: Delay measurement for the PA-1 based and the PA-3 based ED-CVSL XOR/XNOR gate.

Mode of operation	A	B	Output	Delay
PA-1 based XOR gate				
Evaluation	1	1	1->0	300 ps
	0	0	1->0	299 ps
Precharge	1	1	0->1	184 ps
	0	0	0->1	187 ps
PA-3 based XOR gate				
Evaluation	1	1	1->0	355 ps
	0	0	1->0	354 ps
Precharge	1	1	0->1	598 ps
	0	0	0->1	598 ps

irrespective of the implemented functionality. A maximum leakage power reduction of 78.43% is achieved with the second architecture based DCVSL gates. An increasing trend in the leakage power with the scaling down of the technology is observed in the proposed circuits. Lastly, the third architecture achieves the same leakage power reduction values as the second one but is not able to exhibit the same speed advantage as achieved with the first architecture.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

References

[1] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, Pearson Education, 2003.

[2] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley Publishing, 2010.

[3] C. Piguet, *Low-Power CMOS Circuits*, CRC Press, 2006.

[4] L. Bisdounis, D. Gouvetas, and O. Koufopavlou, "A comparative study of CMOS circuit design styles for low-power high-speed VLSI circuits," *International Journal of Electronics*, vol. 84, no. 6, pp. 599–613, 1998.

[5] K. M. Chu and D. L. Pulfrey, "A comparison of CMOS circuit techniques: differential cascode voltage switch logic versus conventional logic," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 528–532, 1987.

[6] L. Heller, W. Griffin, J. Davis, and N. Thoma, "Cascode voltage switch logic: a differential CMOS logic family," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 16–17, San Francisco, Calif, USA, Feburary 1984.

[7] M. Stanisavljevic, A. Schmid, and Y. Leblebici, "Fault-tolerance of robust feed-forward architecture using single-ended and differential deep-submicron circuits under massive defect density," in *Proceedings of the International Joint Conference on Neural Networks (IJCNN '06)*, pp. 2771–2778, July 2006.

[8] R. Faghih Mirzaee, T. Nikoubin, K. Navi, and O. Hashemipour, "Differential Cascode Voltage Switch (DCVS) Strategies by CNTFET Technology for Standard Ternary Logic," *Microelectronics Journal*, vol. 44, no. 12, pp. 1238–1250, 2013.

[9] S. Mathew and R. Sridhar, "Data-driven micropipeline structure using DSDCVSL," in *Proceedings of the 21st IEEE Annual Custom Integrated Circuits Conference (CICC '99)*, pp. 295–298, May 1999.

[10] D. Z. Turker, S. P. Khatri, and E. Sánchez-Sinencio, "A DCVSL delay cell for fast low power frequency synthesis applications," *IEEE Transactions on Circuits and Systems. I. Regular Papers*, vol. 58, no. 6, pp. 1225–1238, 2011.

[11] Priyanka and A. K. Singh, "A low voltage high speed DCVSL based ring oscillator," in *Proceedings of the Annual IEEE India Conference (INDICON '15)*, pp. 1–5, New Delhi, India, December 2015.

[12] W. Y. Choi, "Miller effect suppression of tunnel field-effect transistors (TFETs) using capacitor neutralisation," *Electronics Letters*, vol. 52, no. 8, pp. 659–661, 2016.

[13] D. W. Kang and Y.-B. Kim, "Design of enhanced differential cascode voltage switch logic (EDCVSL) circuits for high fan-in gate," in *Proceedings of the 15th Annual IEEE International ASIC/SOC Conference (ASIC/SOC '02)*, pp. 309–313, September 2002.

[14] N. Hanchate and N. Ranganathan, "LECTOR: a technique for leakage reduction in CMOS circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 2, pp. 196–205, 2004.

[15] P. Lakshmikanthan and A. Nuñez, "A novel methodology to reduce leakage power in differential cascode voltage switch logic circuits," in *Proceedings of the 3rd International Conference on Electrical and Electronics Engineering*, pp. 1–4, Veracruz, Mexico, September 2006.

[16] W. Chen, W. Hwang, P. Kudva, G. D. Gristede, S. Kosonocky, and R. V. Joshi, "Mixed multi-threshold differential cascode voltage switch (MT-DCVS) circuit styles and strategies for low power VLSI design," in *Proceedings of the International Symposium on Low Electronics and Design (ISLPED '01)*, pp. 263–266, August 2001.