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Application of a Tiled Radiation-Hardened Commercial DSP toward Advanced Spaceborne Computing

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Agenda

- The Spaceborne Payload Processing Dilemma
- RADSPEED DSP Architecture and Implementation
- RADSPEED Performance in Payload Applications
- RADSPEED Board
- Scaling the Architecture
- RADSPEED DSP Software Development Kit and Remote Login

For an existing need, an emerging solution

- Many payloads already on orbit and in development require both high power/performance and excellent resistance to radiation
- Some examples of high performance payload applications:
  - Radar processing: high throughput required for both Space-Time Adaptive Processing (STAP) and Synthetic Aperture Radar (SAR) algorithms
  - Hyperspectral imaging: simultaneous processing of images across a number of frequency bands, fusing data for analysis
  - Spectral analysis: simultaneous assessment of data across a number of frequency bands
  - Image processing: distribution of a high resolution image across a series of parallel processing elements
- Currently available solutions all involve some level of compromise
  - Commercial digital signal processors: offer high performance, but without good radiation resistance and often with high power dissipation
  - Radiation-hardened general purpose processors: can address moderate payload requirements, but typically do not have sufficient throughput for these payloads
  - Space capable FPGAs: offer fast programming / turnaround but typically with comparatively poor power/performance, only moderate radiation resistance and additional configuration memory requirements
  - Radiation-hardened ASICs: can achieve excellent power/performance and radiation hardness, but require long lead times and high NRE

For space payloads requiring high throughput with both strong resistance to the space environment and excellent power/performance, a better solution was needed

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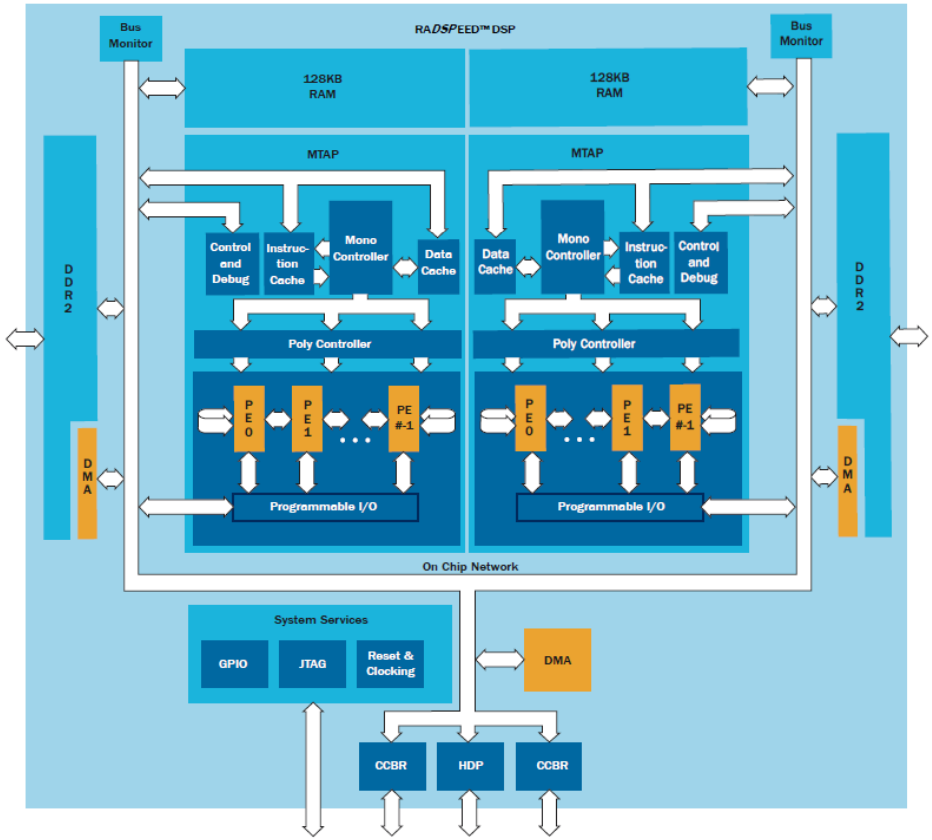
RA*DSP*EED™ DSP SIMD processor architecture

- The RA*DSP*EED DSP is a radiation hardened variant of the CSX700 digital signal processor (DSP) from ClearSpeed Technology
- RA*DSP*EED™ DSP features
  - 160 processing elements (2x76 + 8 spares) called "PEs" in two multi-threaded array processors called "MTAPs"
  - Each PE incorporates double precision floating point hardware as well as integer processing
  - Single instruction, multiple data (SIMD) architecture
  - Dual ClearConnect™ bridges (CCBR)
    - Each with ~ 30 Gb/s throughput
    - Supports direct connection between DSPs or to a backplane using a bridge
  - Dual DDR2 DRAM interfaces
    - A DDR2 interface is dedicated to each MTAP, avoiding bottlenecks
    - Throughput: ~30 Gb/s each
- Supported by mature commercial software development kit
- Software prototyping hardware available now



RA*DSP*EED DSP block diagram

The RA*DSP*EED DSP chip includes two independent cores, each with 76 parallel processing engines, and dual high performance memory and I/O ports

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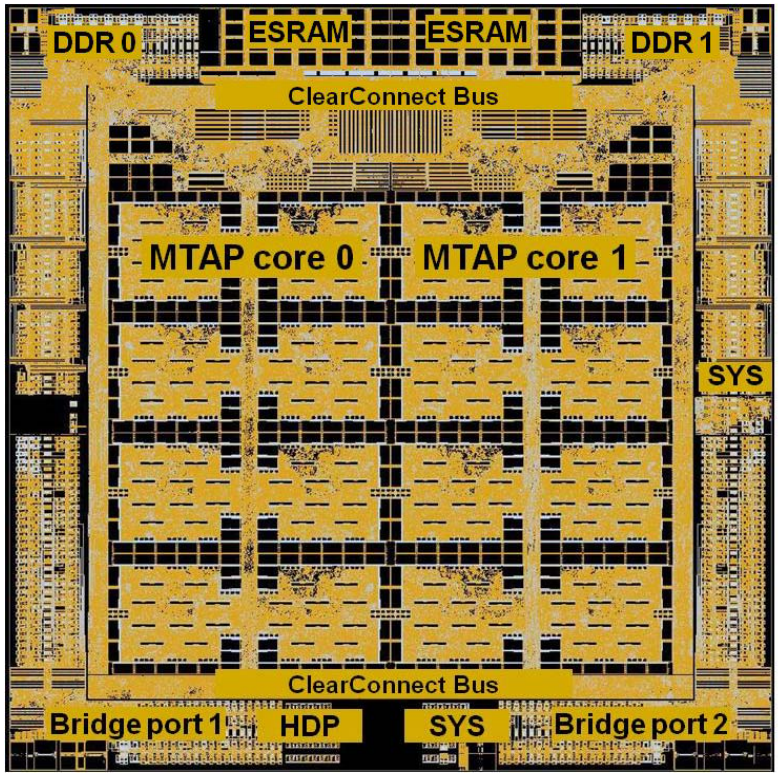
RA*DSP*EED DSP implementation

- RA***DSP***EED™ DSP technology
  - 90 nm bulk CMOS technology
  - 400 mm^2 die size
  - Incorporation of advanced radiation hardened design techniques
- Technical metrics
  - Radiation
    - Total Ionizing Dose: est. 1 Mrad (Si)
    - Single Event Upset*: est. 1E-5 upsets/device-day
    - Latchup: immune
  - Performance
    - 233 MHz clock speed
    - 70 GFLOPS peak throughput
  - Power dissipation
    - Approx. 15 W @ 233 MHz in heavy stress applications
    - Unused PEs are clock gated to further reduce power dissipation
- Development schedule
  - Prototypes: estimated 1Q12
  - Production: planned for 4Q12



RA***DSP***EED DSP die screen shot

*** SEU @ worst case 90% GEO**

Implemented in a 90 nm process, the radiation hardened RA*DSP*EED DSP chip provides throughput as high as 70 GFLOPS while dissipating only 15 Watts (4.7 GFLOPS/W)

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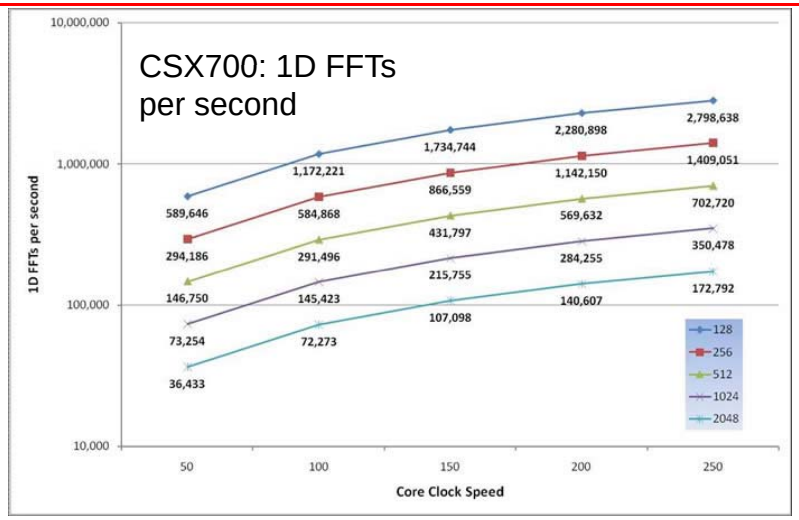
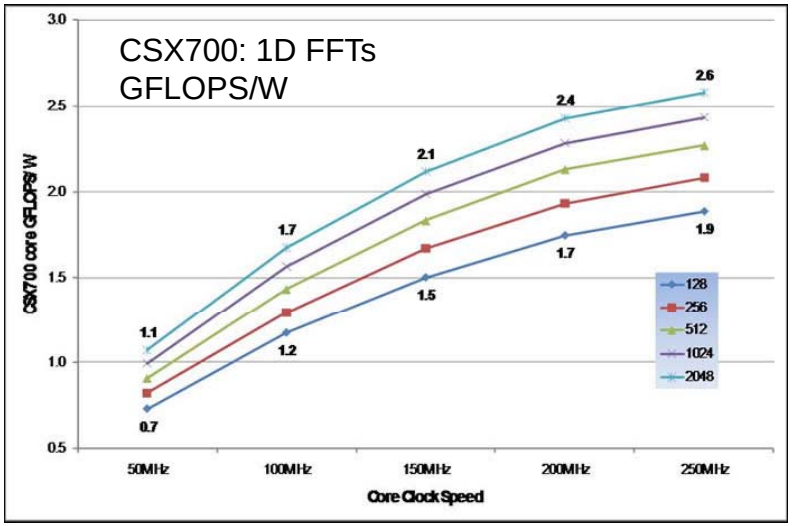
SAR processing application example*

- As part of the Software Development Kit, an FFT library is provided that includes a 1024x1024 point single precision complex 2D FFT
- The1024x1024 point 2D FFT is executed with the following three steps:
  1. Perform 1024 1D FFTs across the rows, each on 1024 samples
  2. Transpose the 2D array of 1024x1024 samples
  3. Perform 1024 1D FFTs down the columns, each on 1024 samples
- Programmed I/O (PIO) DMA engines within the PEs read the data from the DDR2 memory, then perform the 1D FFTs all in parallel
- Twiddle factors are pre-computed and left in PE memory for the duration of the entire 2D FFT
- Rather than perform the transpose as a completely separate phase, the transpose is merged as part of the write back to DDR2 memory at the end of the first phase of 1D FFT processing across the rows
- Following 1D FFT computation across the rows and transposition, 1D FFTs are performed down the columns





*From "Synthetic Aperture Radar on CSX700 Technical Notes", 02-WP-1633, May 2009, and FFT performance benchmarks, ClearSpeed Technology Limited

The SIMD architecture efficiently executes the 2D FFT kernel required for SAR applications

RA*DSP*EED DSP image processing application example*

- Fijany and Hosseini have recently studied four classes of image processing applications on CSX700
  - Harris Corner Detector (feature detection)
  - SSD-based Stereo vision (depth map)
  - RANdom Sample Consensus (mathematical model generation from data set with outliers)
  - Histogram of Oriented Gradient (object detection)
- **Absolute processing performance is very high compared to results reported on other engines including FPGA, ASIC and GPU** for all but HOG application
- HOG performance using one CSX700 is about 54.2% less than the best reported GPU. However,
  - Performance scales linearly with added CSX700s
  - 3 CSX700s would outperform GPU by 37%
  - **3 CSX700s use only 8% of the power per frame of a GPU**
- These applications cover a wide range of granularity, data dependency, and pattern of communication illustrating wide applicability of CSX700 architecture
- RA*DSP*EED DSP performance is >70% that of CSX700
  - 152 versus 192 processing elements
  - 233 MHz versus 250 MHz

Table 2. Comparison of HCD Implementation on CSX With Other Implementations in the Literature

Image Resolution	fps reported in [ref]	CSX700 fps achieved by our approach
128x128	1367 (ASIC) [13]	4464
352x288	60 (FPGA) [14]	819
640x480	99 (GPU) [15]	304

Table 4. Comparison of Stereo Vision implementation on CSX and Conventional Architecture

Algorithm	MPDs reported in [3]	CSX700 MPDs reported in [25]
SSD	143	1032
SSD_MW5	75	442
SSD_LR	114	501

Table 7. Comparison of HOG implementation on CSX Architecture with Other Implementations in the Literature

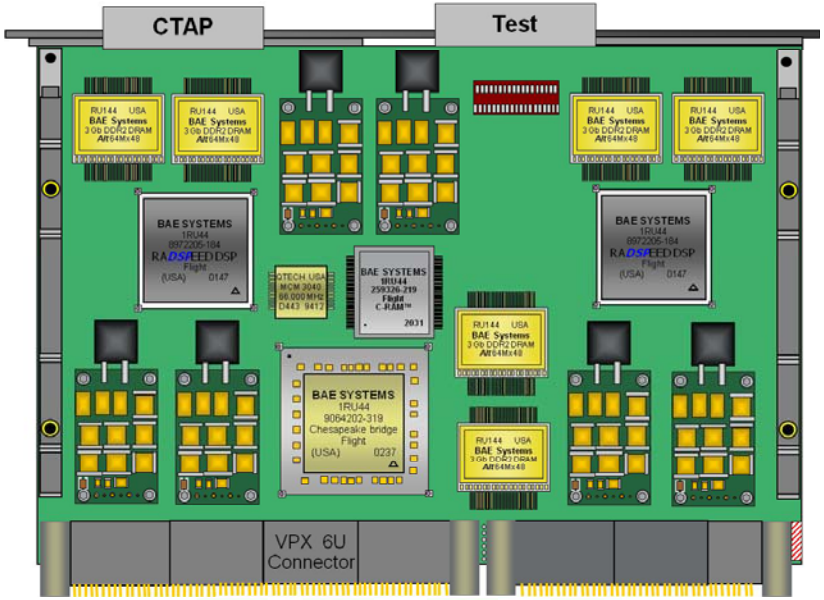
	Latency (ms)	Peak Performance (GFLOPS)	fps / watt
CSX [41]	146.23	96	.75
GPU [39]	99	384	.06
GPU [40]	67	1788.48	.05

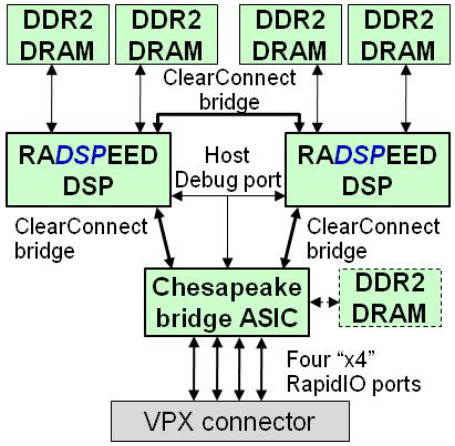
*Amir Finjany and Fouzhan Hosseini, "Image Processing Applications on a Low Power Highly Parallel SIMD Architecture," published at the 2011 IEEE Aerospace Conference (March 2011). Used with permission.

Image processing performance is similarly impressive, especially compared to alternatives

RA*DSP*EED card implementation

- Either two or four RADSPEED DSP chips would be placed on a card, combined with a backplane interface chip called the “Chesapeake Bridge ASIC”
  - Dual DSP version uses 6U-160 card format with VPX (Vita 46) connector standard
  - A quad DSP version of the card will require the use of advanced thermal management techniques and would fit on 6U-220 card format
  - DDR2 SDRAM shown in multichip modules for shielding, density, and improved ruggedness
- A minimum of 1 GB of DDR2 SDRAM is dedicated to each DSP
- Chesapeake bridge ASIC features:
  - Four “x4” serial RapidIO interfaces plus a spare (40 Gb/s in total)
  - Dual CCBR interfaces to RA*DSP*EED DSP chips
  - DDR2 SDRAM memory controller with SECDED ECC
  - Controller processor core





At the card level, interfaces for the RA*DSP*EED DSP are focused on very high rates of data transfer between DSP chips, to the backplane, and to on-card memory

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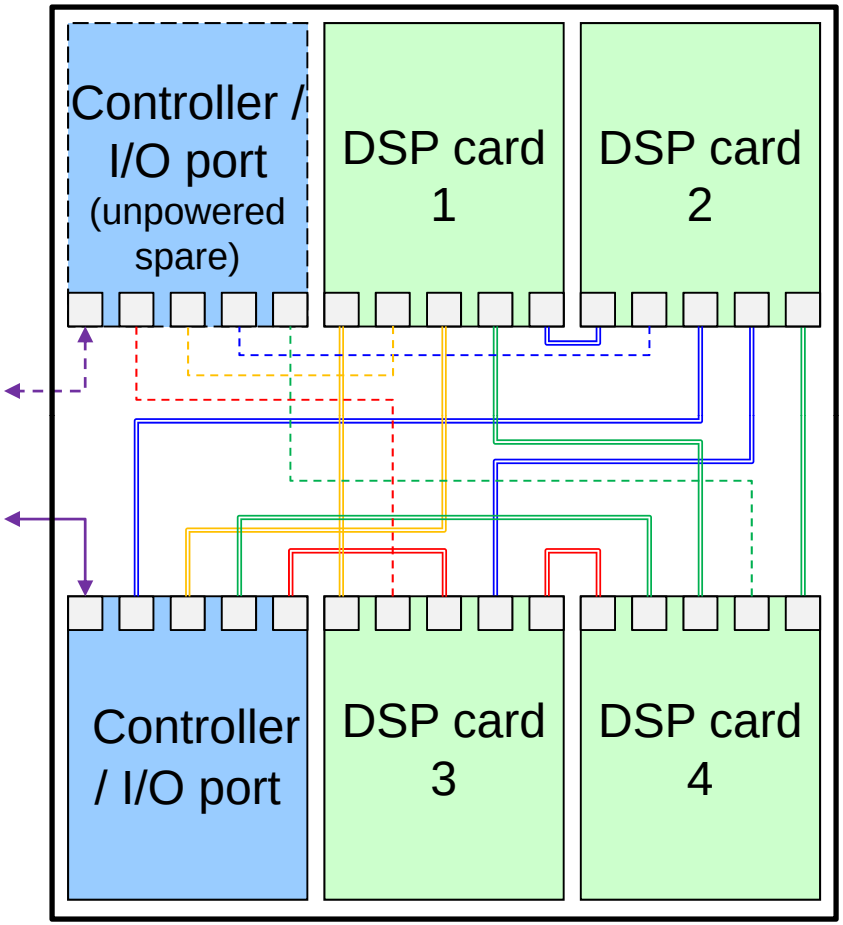
Small subsystem implementation

- Small subsystem configuration
  - A small subsystem includes up to four DSP cards (or 3 with a redundant spare) and a redundant I/O and subsystem controller interface card
  - Using the four active RapidIO ports, all connection can be made directly, requiring no central RapidIO switch ASIC
  - The spare interfaces on the DSP cards would go to the redundant I/O card
- Performance
  - At 70 GFLOPS peak per DSP, a four card system with dual DSPs per card would achieve a peak throughput of 560 GFLOPS
  - With quad DSP cards, that would double to achieve peak throughput of > 1 TFLOPS



A subsystem based on the RA*DSP*EED DSP can be variably sized, where smaller implementations do not require a central RapidIO switch

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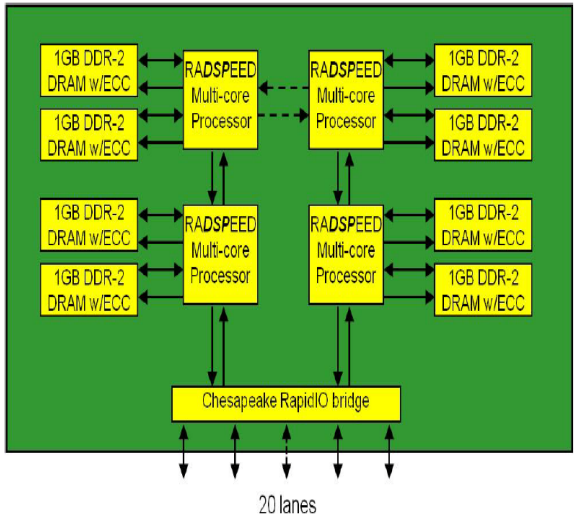
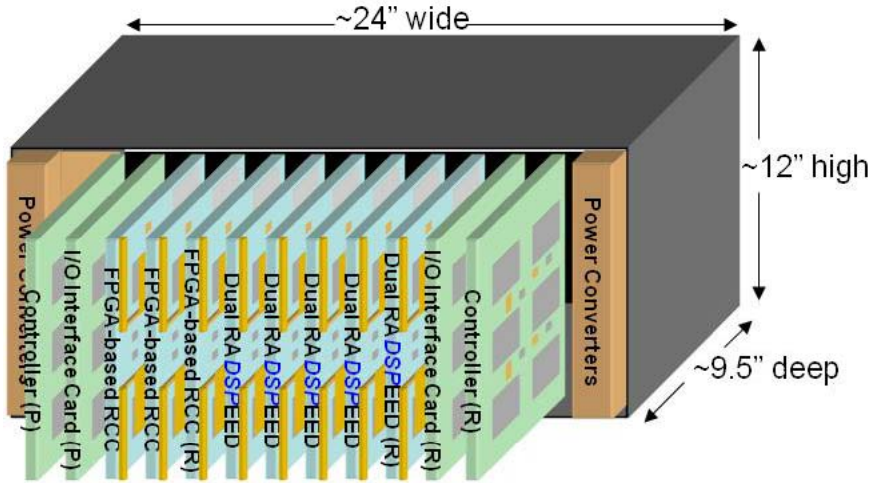
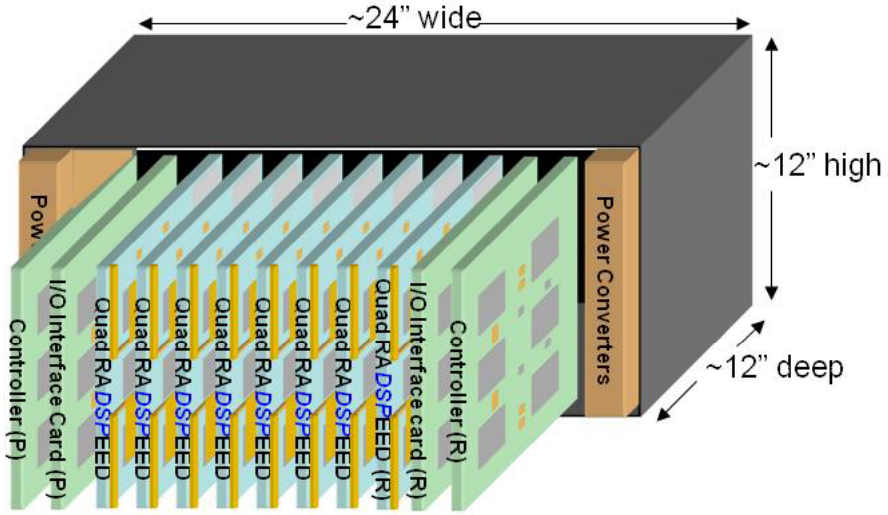
Scaling the architecture

- Dual or quad DSP board variants are achievable
- Multiple card implementation scales and addresses increasing and more varied processing requirements







Heterogeneous subsystem with:

- Four dual DSP cards plus a spare
- Two reconfigurable FPGA cards plus a spare
- Redundant controller cards
- Redundant I/O cards
- Redundant central RapidIO switch ASICs

Large RADSPEED subsystem with:

- Seven quad DSP cards plus a spare
- Redundant controller cards
- Redundant I/O cards
- Redundant central RapidIO switch ASICs

The RADSPEED DSP system architecture can easily be scaled to support 2 TFLOPS of total throughput

RA*DSP*EED DSP software development kit (SDK) support

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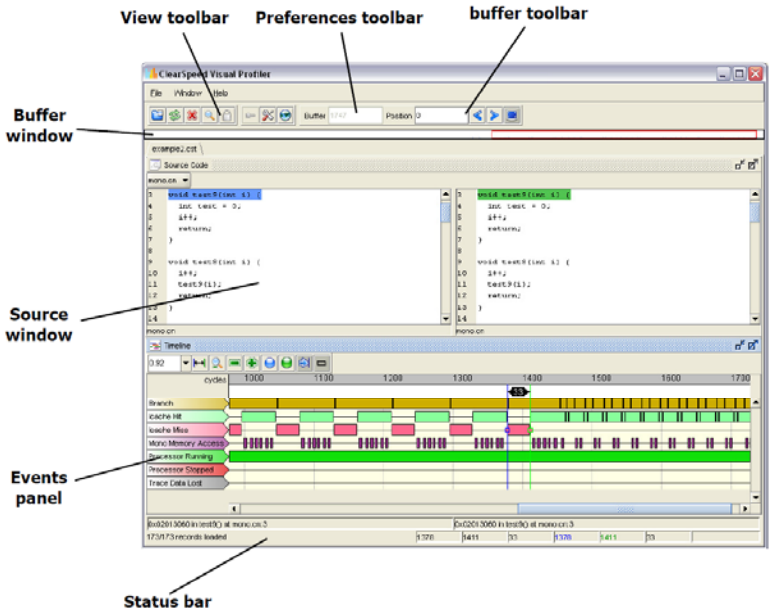
- **Cⁿ language and compiler**
  - Cⁿ extends C language with “poly” commands for SIMD program control / execution
  - Cⁿ optimizing compiler
- **CSXL vector math libraries**
  - Accelerated versions of mathematical functions
    - Includes Basic Linear Algebra Subroutines (BLAS)
    - Includes Linear Algebra Package (LAPACK)
  - Supports a single DSP per process
- **Development environment**
  - GDB-based source level debugger
    - GNU freeware with ClearSpeed additions
    - Provided by DSP supplier
    - Instruction set and cycle-accurate simulators
  - **Profiler**
    - GUI interface
    - Visualizes DSP performance, integrating with debugger
    - Allows trace of RADSPEED pipelines



Visual Profiler GUI

The RADSPEED DSP includes specialized software provided in a software development kit (SDK)

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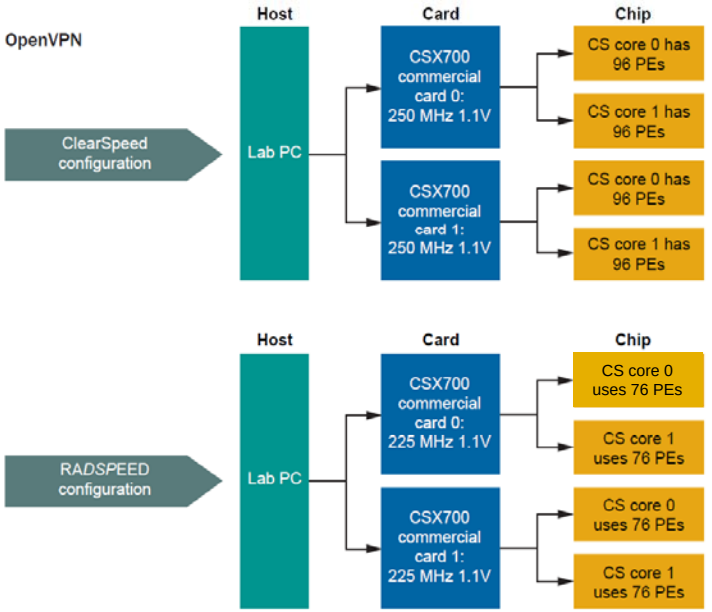
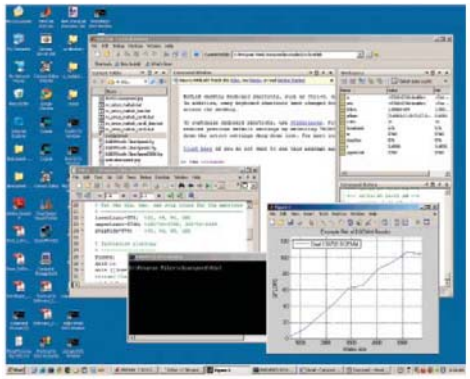
Remote login for RA*DSP*EED DSP benchmarking

- The RA***DSP***EED DSP mission application lab is fully compatible with the commercial CSX700 SDK which includes the following features:
  - ANSI C-based optimizing compiler
  - Data-parallel extensions
  - Full-featured debug and profiling tools
  - ECLIPSE-based IDE
  - Standard C libraries
  - Optimized library functions available featuring:
    - FFT
    - BLAS
    - LAPACK
  - High-level host interface API (CSPX)
- Lab hardware includes two ClearSpeed e710 cards installed in workstations
- Remote login is available through OpenVPN





Users interested in benchmarking their applications can obtain remote login access to our lab run on an emulated RADSPEED configuration using the commercial cards

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Summary

- The RA***DSP***EED DSP will open up significant high performance payload applications especially when an FPGA or GPP is not the best solution
- Components focus on achieving the best possible power/performance and I/O bandwidth, while achieving SEU resistance combining circuit hardening with error correction and scrubbing of internal arrays
- Card-level level products are focused on fast memory with high capacity and extreme I/O throughput to prevent “starvation” of the processing elements
- A software development kit matched to the processor hardware is provided by BAE Systems
- Early benchmarking with equipment in the BAE Systems lab is available to potential users via remote login
- Scalability and flexibility has been considered in the development of the RA***DSP***EED DSP solution

The RADSPEED DSP will provide a powerful and scalable solution for on-board digital signal processing