Aviral Shrivastava

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OVERVIEW

Aviral Shrivastava is currently an Assistant Professor in the School of Computing Informatics and Decision Systems Engineering at the Arizona State University. He received his Ph.D. from University California, Irvine in 2006.

Dr. Shrivastava's research interests lie at the intersection of compilers and architectures of embedded and multi-core systems. He is well known for his work in compilation for processors with scratch pads, compiler and microarchitectural techniques to reduce the impact of soft errors, and compiler-assisted processor design.

Dr. Shrivastava is co-author of the book "Power-Efficient System Design," published by Springer, and has contributed chapters to two others. He has published 19 journals, and 51 conference papers in all the top embedded system journals and conferences. His works have received several "best paper award" nominations.

Dr. Shrivastava's research efforts have been supported from national and state foundations as well as from the industry. Most noticeably, he has been awarded the *2010 NSF CAREER Award* to support his efforts on protecting computation from soft errors. His research on compilation for limited local memory multi-core architectures has been funded by NSF and SFAZ. Industry, through the Consortium of Embedded Systems (CES) has been supportive of his research on power-efficient computing. Industry has also valued the consultancy of Dr. Shrivastava for their R&D efforts. In the past five years, Dr. Shrivastava has been a key participant in $3.4 million of research, with his contribution valued at $1.5 million.

Dr. Shrivastava primarily teaches undergraduate and graduate level courses on computer architecture, and compilers, and has excellent teaching record with student evaluations averaging 4.30/5.00. He has revamped the computer organization course to shift the focus towards processor design instead of assembly language programming, and revamped the contents of the computer architecture course to including information about the new multi-core architectures.

Dr. Shrivastava serves on the technical program committees of top conferences in the area of embedded systems, including CODES+ISSS, CASES, and LCTES, and is organizing the workshop on "Compiler Assisted SoC Assembly" in 2011. He has been invited to present his work at several prominent universities and industry.

Dr. Shrivastava's first Ph.D. student is graduating in fall 2011. He has graduated 7 Master students, who are all very well placed in the industries, like Microsoft, Intel, Nvidia, Qualcomm etc. He mentored a post-doc, who is now an Assistant Professor at UNIST, South Korea. Currently he is supervising 4 Ph.D. students and 7 Masters students.

BACKGROUND

Academic Preparation

Ph.D. **University of California, Irvine, Information and Computer Science,** **June 2006**
Thesis: Compiler-in-the-Loop Exploration of Programmable Embedded Systems
Advisors: Profs. Nikil Dutt (chair), Alex Nicolau, and Alex Veidenbaum

M.S. University of California, Irvine, Information and Computer Science May 2002

B.Tech Indian Institute of Technology, Delhi, Computer Science and Engineering May 1999
Thesis: Hardware Software Partitioning and Synthesis targeted towards FPGA based implementation
Advisor: Prof. M. Balakrishnan

Academic Experience

2006 - present Assistant Professor, School of Computing, Informatics and Decision Systems Engineering, Arizona State University.

2002 - 2006 Graduate Research Assistant, Information and Computer Science, University of California, Irvine.

2000 - 2002 Teaching Assistant, Information and Computer Science, University of California, Irvine.

Industrial Experience

July 2003 – Dec. 2003 Research Intern at Strategic CAD Labs in Intel Shrewsbury, MA.

July 2002 – Sept. 2002 Internship at HP Labs in PICO Group.

Sept. 1999 – June 2000 CAD Engineer at Philips Semiconductors, Nijmegen, Netherlands.

Research Interests

Compilation for modern multi-core and embedded architectures, Temperature and Power-Aware Computing, Extremely high-performance, low-power Computing, Reliable Computing on Unreliable Hardware, Coarse Grain Reconfigurable Architectures, and Soft error resilience.

Teaching Interests

Computer Organization, Computer Architecture, Multi-core Architectures and Programming, and Low-Power Computing

AWARDS AND HONORS

- **2010 NSF CAREER Award** for "Compiler Techniques for Power-Efficient Protection from Soft Errors."
  The Faculty Early Career Development (CAREER) is the National Science Foundation's most prestigious awards in support of junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education and the integration of education and research within the context of the mission of their organizations.
  - Source: NSF website: http://www.nsf.gov/funding/pgm_summ.jsp?pims_id=503214

- **IEEE Senior Member**

- **2010 SCIDSE Outstanding Master's Thesis**, awarded to my student Seung-chul Jung for "Dynamic Code Mapping for Limited Local Memory Architectures"

- **Invited Speaker at CASA** (Compiler-Assisted SoC Assembly Workshop) 2005, 2006, 2008, and 2010.

- **Second Highest Ranked Paper**, "*Cache Vulnerability Equations for Protecting Data in Processor Caches from Soft Errors*" at Languages Compilers and Architectures for Embedded Systems, LCTES 2010.

- **Best Paper Candidate,** "*SPKM: A Novel Graph Drawing based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architecture*" at Asia South Pacific Design Automation Conference, ASPDAC 2008.

- **Best Paper Candidate**, "*Bypass Aware Instruction Scheduling for Register File Power Reduction*" at Languages Compilers and Architectures for Embedded Systems LCTES 2006.

- **Spring 2005 Dissertation Fellowship,** University of California, Irvine.

- **Intel-SRC Funded Ph.D. Student** 2003-2005 (Semiconductor Research Corporation).

- **102 Rank Nation-wide in JEE 1995**
  The **Indian Institute of Technology Joint Entrance Examination** (popularly known as **IIT-JEE** or just **JEE**). It is one of the toughest engineering entrance exams in the world with a success rate of around 1 in 45. More than 450,000 students compete in the examination.
  Source: http://en.wikipedia.org/wiki/Indian_Institute_of_Technology_Joint_Entrance_Examination

- **National Talent Search Scholarship,** 1993-1995.
  The National Talent Search Examination (NTSE) is a national level scholarship program in India to identify and nurture talented students. It is widely regarded as the toughest and most prestigious examination at high school level in the country with typical acceptance rate of 0.33%
  Source: http://en.wikipedia.org/wiki/National_Talent_Search_Examination

RESEARCH SUPPORT

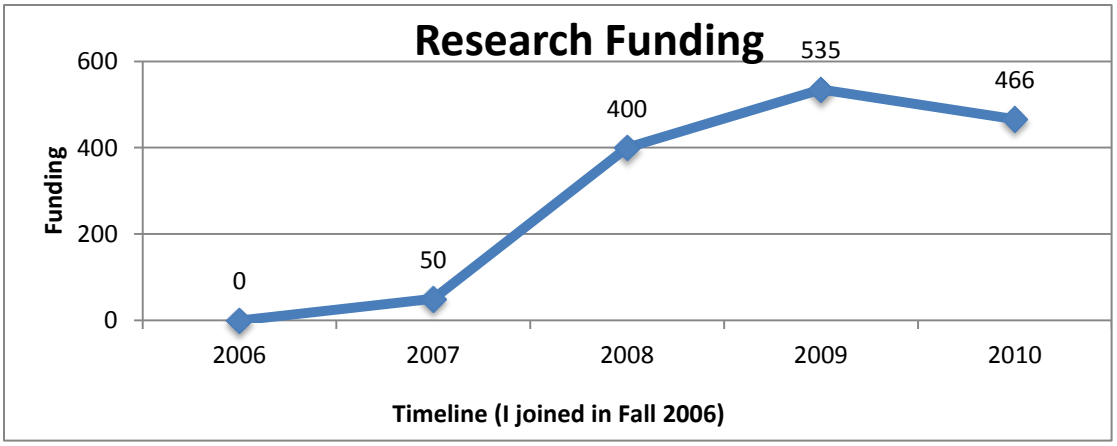
Summary of Sponsored Research and Consultation

	Sponsor	Years	Account	Recognition	RID	IIA	Total Award $	My Award $
1	NSF-REU	2011	CRS 0262	100%	100%	100%	$8K	$8K
2	NSF-CAREER	2011-16	CRS 0285	100%	100%	100%	$401K	$401K
3	NSF	2009-12	CRS 0212	100%	100%	100%	$500K	$500K
4	NSF	2009-12	AQS 0014	0%	0%	0%	$300K	$0K
5	NSF-REU	2010	CRS 0262	100%	100%	100%	$16K	$16K
6	SFAZ	2008-11	AQS 0012	20%	20%	20%	$2,000K	$400K
7	CES	2011	TBD	100%	100%	100%	$35K	$35K
8	CES	2010	AQS-0236	100%	100%	100%	$35K	$35K
9	CES	2009	AQS-0236	100%	100%	100%	$35K	$35K
10	AZ Security	2010	CRS 0260	100%	100%	100%	$12K	$12K
11	AZ Security	2010	JS5 1050	100%	100%	100%	$2K	$2K
12	Microsoft Research	2007	JX9 1015	100%	100%	100%	$50K	$50K
						Total	**$3,394K**	**$1,494K**

- **Sponsor**: the sponsor funding the grant/contract.
- **Account**: the account number at Arizona State University associated with the grant/contract.
- **Recognition**: Recognition refers to the percentage of the project for which I receive credit on annual reports of proposal and award dollars.
- **RID**: Research incentive distribution
- **IIA**: Investigator incentive award.
- **Total Award $**: The total of the award in dollars
- **My Award $**: Of the total award, the award dollars attributed to me.
- **NSF:** National Science Foundation
- **REU:** Research Experience for Undergraduates
- **SFAZ:** Science Foundation of Arizona
- **CES:** Consortium for Embedded Systems*

***** *Consortium for Embedded Systems (CES)* is an Industry-University partnership at ASU, of which several companies, including Intel, Raytheon Missile Systems, Qualcomm, and Marvel Inc. are members. Research proposals are solicited by the member companies, competitively evaluated and then funded by the member companies. For more information, please visit: http://embedded.asu.edu.

Funding Timeline



External Research Funding from Federal and State Agencies

- **$401K,** *Sole Principal Investigator,* National Science Foundation **CAREER Award** for "Compiler Techniques for Power-Efficient Protection from Soft Errors," 08/01/2011 – 07/31/2016.
- **$500K,** *Sole Principal Investigator*, National Science Foundation: "Compilation for Multi-core Processors with Limited Local Memories," 08/01/2009 – 07/31/2012.
- **$16K**, *Sole Principal Investigator*, National Science Foundation, "NSF-REU: Compilation for Multi-core Processors with Limited Local Memories," 08/01/2010 – 07/31/2011.
- **$0K**, *Co-Principal Investigator*, National Science Foundation, "NSF-ENG: Collaborative Research: Consortium for Embedded Systems" Total award: $300K, 03/01/2009 – 02/28/2014, Principal Investigator: Sarma Vrudhula.
- **8K**, *Sole Principal Investigator*, National Science Foundation, "NSF-REU: Compilation for Multi-core Processors with Limited Local Memories," 08/01/2011 – 07/31/2012.
- **$400K**, *Co-Principal Investigator*, Science Foundation of Arizona: "An Integrated Design Framework for Application Development on Multi-Core Processors." Total Award: $2000K, 08/01/2007 – 07/31/2011. Principal Investigator: Sarma Vrudhula.

External Research Funding from Industry

- **$34K,** Sole Principal Investigator, "Programming Non-Coherent Cache Architectures," Consortium for Embedded Systems*, 2011.
- **$35K,** Sole Principal Investigator, "Memory Optimizations for Limited Local Memory Multi-core Systems," Consortium for Embedded Systems*, 2010.
- **$2K,** Sole Principal Investigator, for **"**Multi-core programming," from **Arizona Security Technologies**, Phoenix, AZ, USA, 2010.
- **$35K,** Sole Principal Investigator, for "Memory-Aware Compilation for multi-core Systems," from Consortium for Embedded Systems*, 2009.
- **$50K,** Sole Principal Investigator, for "Low-Power Compilation using Phoenix," from **Microsoft Research**, Redmond, WA, USA, 2007.

Industry Consultation

- **$12K,** Arizona Security Technologies, Phoenix, USA, for consultation in "Acoustic Signature Recognition in Software."

Equipment Support from Industry

- **Nvidia Corporation**, Santa Clara, California: 3 Fermi GTX480 GPUs for GP-GPU computing, 2011.
- **Intel Corporation,** Santa Clara, California: Access to the new Intel 48-core processor for "Coarse-Grain Memory Management for many-core Computing," 2011.
- **Nvidia Corporation**, Santa Clara, California: 2 Tesla C1060 GPUs for GP-GPU computing, 2009.

Pending Proposals

- Co-Principal Investigator, NSF: "CPS: Medium: Collaborative Research: An Adaptive, Power-Sustainable, Intelligent-Sensor Ecosystem Design for Monitoring Stroke Patients," Principal Investigator: Hari Sundaram, $1500K, submitted 03/20/2011.

- Co-Principal Investigator, NSF: "SI2-SSE: An Integrated Approach to Reliability in Exascale Systems," Principal Investigator: Rida Bazzi, $500K, submitted 07/18/2011.

Recently Declined Proposals

- Co-Principal Investigator, NSF, "CSR: Large: Collaborative Research - An Adaptive and Zero Maintenance Intelligent-Sensor System Design for Monitoring Stroke Patients"
  PI: Hari Sundaram. Co-PIs: Jeffrey Kleim, Selcuk Candan, Thenasis Rekasis, ASU.
  Amount: $1900K, Declined 07/04/2010.
  - *Was rated "Highly Competitive," but was declined for scarcity of funds.*

- Principal Investigator, NSF, "CSR: Medium: Collaborative Research: Enabling High Performance at High Power Efficiency using Coarse Grain Reconfigurable Arrays"
  Co-PIs: Sarma Vrudhula, ASU, and David Blaauw, UMich Ann Arbor.
  Amount: $800K, Declined 01/27/2011.

- Sole Principal Investigator, DOE, "HCPA: Hierarchy of Cores and Programmable Accelerators - A Novel Processor Architecture for Exascale Computing,"
  Amount: $401K, declined 06/30/2011.

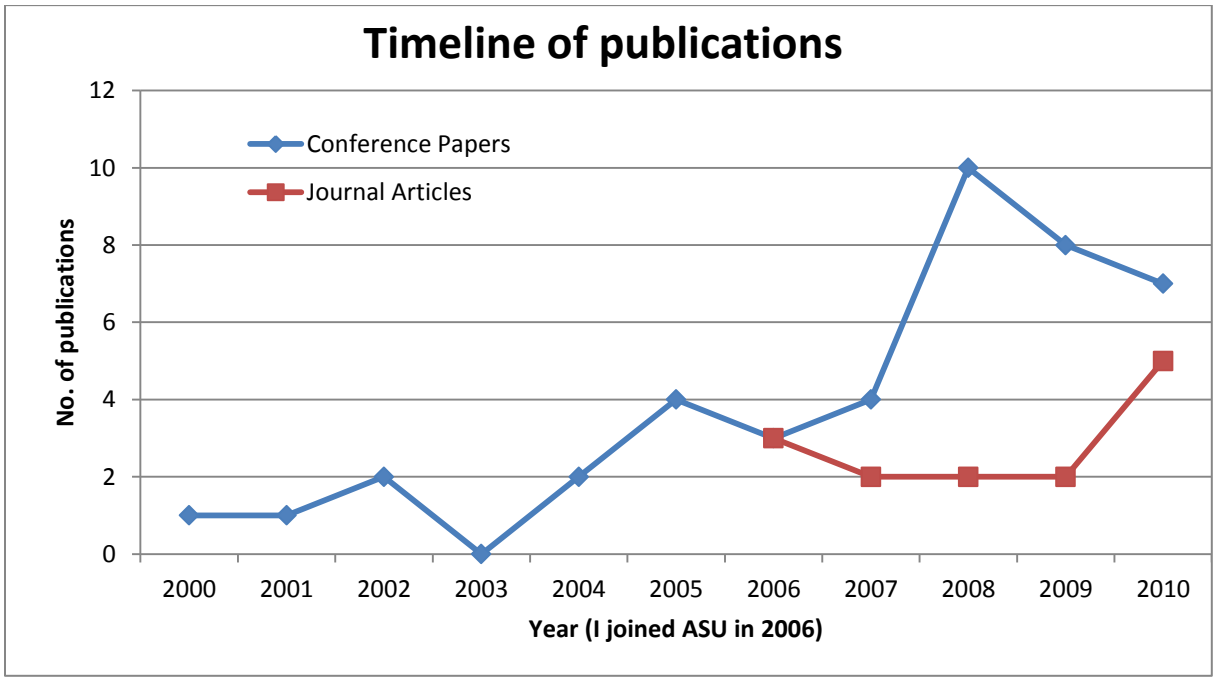
RESEARCH PUBLICATIONS

Summary of Publication Record

My field of research is at the intersection of compilers, microarchitectures, and design automation of embedded systems, with a particular focus on "Compilers for Embedded Systems." I am the co-author of a book titled, "Power-Efficient System Design" by Springer, and have contributed chapters in 2 books. I have published 19 journal articles and 51 conference papers in almost all top venues in the field of embedded systems. Top journals in my field include ACM Transactions on Embedded Computing Systems (ACM TECS), ACM Transactions on Design Automation of Embedded Systems (ACM TODAES), IEEE Transactions on Computed Aided Design (IEEE TCAD), and IEEE Transactions on VLSI Design (IEEE TVLSI). The most important embedded system conferences are International Conference on Languages Compilers and Architectures of Embedded Systems (LCTES) (25-30% acceptance rates), International Conference on Hardware Software Co-design and System Synthesis CODES+ISSS (25-30% acceptance rates), Design Automation Conference (DAC) (20-25% acceptance rates), International Conference on Design Automation and Test in Europe (DATE) (25-30% acceptance rates), International Conference on Compilers Architectures and Synthesis of Embedded Systems (CASES) (30-40% acceptance rates).

Important Note: Due to the cutting-edge and fast-changing nature of research in computer science, conferences are much more selective, prestigious, and higher impact than journals. This is especially true in my field of embedded systems.

Timeline of Publications



Summary of Student Involvement:

During the last 5 years, I have worked and published extensively with several ASU students. I have guided and worked with students in several capacities: i) students that I have directly supervised, ii) students with whom I have worked in collaboration with other faculty in SCIDSE and SECEE, iii) students who have taken my course, and have done course projects that resulted in papers and journals.

Below is the list of ASU that I have collaborated with. This list does not consider students in other universities that I have collaborated with.

- Reiley Jeyapaul is my Ph.D. student, expected graduation Fall 2011.

- Amit Pabalkar was my MS student, graduated Spring 2008, now at nVIDIA, Santa Clara, CA.
- Arun Kannan was my MS student, graduated Spring 2008, now at Intel, Portland, OR.
- Rooju Chokshi was my MS student, graduated Spring 2008, now at Microsoft, Redmond, WA.
- Sai Mylavarapu was my MS student, graduated Fall 2008, now at Qualcomm, San Diego, CA.
- Saleel Kudchadker was my MS student, graduated Spring 2010, now at AMD, Austin, TX.
- Seung-chul Jung was my MS student, graduated Spring 2010, now an entrepreneur in CA.
- Fei Hong was my MS student, graduated Spring 2011, now at Allied Telesis, San Jose, CA.

- Ke Bai is my Ph.D. student, expected graduation Fall 2012.
- Yooseong Kim is my Ph.D. student, expected graduation Fall 2013.
- Jing Lu is my Ph.D. student, expected graduation Fall 2014.
- Mahdi Hamzeh is Ph.D. student of myself and Prof. Sarma Vrudhula.

- Abhishek Rhisheekesan is my MS student.
- Jared Pager is my MS student.

- Deepa Kannan was a MS student in SECEE, now at Intel, Portland, OR.
- Vipin Mohan was a MS student in the SECEE.

- Aarul Jain was MS student of Prof. Chaitali Chakrabarti (SECEE), graduated Fall 2010.
- Jeffery Boyd is a Ph.D. student of Prof. Hari Sundaram.
- Michael A. Baker was a Ph.D. student of Prof. Karam Chatha, graduated Spring 2011.
- Sarvesh Bharadwaj was Ph.D. student of Prof. Sarma Vrudhula, graduated Fall 2007.
- Satyajayant Mishra was a Ph.D. student of Prof. Guoliang Xue, graduated Spring 2008.

Books Published

B1. Book Title: Power-Efficient System Design

Authors: Preeti Ranjan Panda, **Aviral Shrivastava**, B.V.N. Silpa, and Krishnaiah Gummidipudi

Publisher: Springer

Year: 2010

ISBN: 978-1-4419-6387-1

Book Chapters

BC2. Chapter Title: ADL-Driven Methodologies for Design Automation of Programmable Architectures

Authors: Prabhat Mishra and **Aviral Shrivastava**

Book title: Processor Description Languages: Applications and Methodologies,

Publisher: Morgan Kaufman

Year: 2007

ISBN: 978-0-12-374287-2

BC1. Chapter Title: Compiler Aided Design of Embedded Computers

Authors: **Aviral Shrivastava** and Nikil Dutt

Book title: The Compiler Design Handbook: Optimizations and Machine Code Generation, Second Edition,

Publisher: CRC Press

Year: 2007

ISBN: 978-1-4200-4382-2

Journal Publications (refereed and archived)

*ASU student names are underlined

J19. [IEEE TCAD] IEEE Transactions on Computer Aided Design
High Throughput Data Mapping for Coarse-Grained Reconfigurable Architectures
Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, and Yunheung Paek
Accepted for publication

J18. [ACM TECS] ACM Transactions on Embedded Computing Systems
PICA: Processor Idle Cycle Aggregation for Energy Efficient Embedded Systems
Jongeun Lee and **Aviral Shrivastava**
Accepted for publication

J17. [ACM TODAES] ACM Transactions on Design Automation of Embedded Systems
Memory Access Optimization in compilation for Coarse Grain Reconfigurable Architectures
Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, and Yunheung Paek
Accepted for publication

J16. [IEEE TVLSI] IEEE Transactions on VLSI
Return Data Interleaving for Multi-channel Embedded CMPs
Fei Hong and **Aviral Shrivastava**
Accepted for publication

J15. [IEEE TVLSI] IEEE Transactions on VLSI
Static Analysis of Register File Vulnerability
Jongeun Lee and **Aviral Shrivastava**
vol. 30, issue 4, pages 606-616, April 2010

J14. [IEEE TCAD] IEEE Transactions on CAD
A Compiler-Microarchitecture Hybrid Approach to Soft Error Reduction for Register Files
Jongeun Lee and **Aviral Shrivastava**
vol. 29, issue 7, pages 1018-1027, July 2010

J13. [ACM TODAES] ACM Transactions on Design Automation of Embedded Systems
Partitioning Techniques for Partially Protected Caches for Resource-Constrained Embedded Systems
Kyoungwoo Lee, **Aviral Shrivastava**, Ilya Issenin, Nikil Dutt, and Nalini Venkatasubramanian
vol. 15, issue 4, pages 30:1-30:30, Oct 2010.

J12. [Springer IJPP] International Journal on Parallel Programming

Code Transformations for TLB Power Reduction

Reiley Jeyapaul and **Aviral Shrivastava**

vol. 38, issue 3, pages 254-276, March 2010.

J11. [IEEE TVLSI] IEEE Transactions on VLSI

Reducing Functional Unit Power Consumption and its Variation using Leakage Sensors

Aviral Shrivastava, Deepa Kannan, Sarvesh Bhardwaj, and Sarma Vrudhula

vol. 18, number 6, pages 988-997, June 2010.

J10. [IEEE TCAD] IEEE Transactions on Computer Aided Design

A Software-only solution to use Scratch Pads for Stack Data

Aviral Shrivastava, Arun Kannan, and Jongeun Lee

vol. 28, number 11, pages 1719-1728, Nov 2009.

J9. [IEEE TCAD] IEEE Transactions on Computer Aided Design

Compiler-in-the-Loop Design Space Exploration Framework for Energy Reduction in Horizontally Partitioned Cache Architectures

Aviral Shrivastava, Ilya Issenin, Nikil Dutt, Sanghyun Park, and Yunheung Paek

vol. 28, number 3, pages 461-466, March 2009.

J8. [IEEE TVLSI] IEEE Transactions on VLSI

A Graph Drawing Based Spatial Mapping Algorithm for Coarse-Grained Reconfigurable Architectures

Jonghee W. Yoon, **Aviral Shrivastava**, Sanghyun Park, Minwook Ahn, and Yunheung Paek

vol. 17, number 11, pages 1565-1579, Nov 2009.

J7. [IEEE TVLSI] IEEE Transactions on VLSI

Partially Protected Caches to Reduce Failures due to Soft Errors in Multimedia Applications

Kyoungwoo Lee, **Aviral Shrivastava**, Ilya Issenin, Nikil Dutt, and Nalini Venkatasubramanian

vol. 17, number 9, pages 1343-1348, Sept 2009.

J6. [IFIP DES] IFIP Distributed Embedded Systems

Data Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures

Kyoungwoo Lee, **Aviral Shrivastava**, Nikil Dutt, and Nalini Venkatasubramanian

vol. 271, pages 213-225, 2008.

J5. **[IEEE TCAD] IEEE Transactions on Computer Aided Design**
Register File Power Reduction using Bypass Sensitive Compiler
Sanghyun Park, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek
vol. 27, number 6, pages 1155-1159, June 2008.

J4. **[IEEE TCAD] IEEE Transactions on Computer Aided Design**
Automatic Design Space Exploration of Register Bypasses in Embedded Processors
Aviral Shrivastava, Sanghyun Park, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek
vol. 26, number 12, pages 2102-2115, Nov. 2007.

J3. **[ACM TODAES] ACM Transactions on Design Automation of Electronic Systems**
Architecture Description Language (ADL)-driven Software Toolkit Generation for Architectural Exploration of Programmable SOCs
Prabhat Mishra, **Aviral Shrivastava**, and Nikil Dutt
vol. 11, number 3, pages 626-658, March 2006.

J2. **[IEEE TVLSI] IEEE Transactions on VLSI**
Retargetable Pipeline Hazard Detection for Partially Bypassed Processors
Aviral Shrivastava, Nikil Dutt, Alex Nicolau, and Eugene Earlie
vol. 14, issue 8, pages 791-801, Sept 2006.

J1. **[ACM TODAES] ACM Transactions on Design Automation of Electronic Systems**
Compilation Framework for Code Size Reduction using Reduced Bit-width ISAs
Aviral Shrivastava, Partha Biswas, Ashok Halambi, Nikil Dutt and Alex Nicolau
vol. 11, number 1, pages 123-146, Jan 2006.

International Conferences Proceedings (Refereed, Achieved, and Premier)

*ASU M.S. and Ph.D. student names are underlined

* Conference acceptance rates are mentioned in "Summary of Publications," page 10.

C51. [CODES+ISSS 2011] International Conference on Hardware/Software Codesign and System Synthesis

Branch Penalty Reduction on IBM Cell SPUs via Software Branch Hinting

Jing Lu, Yooseong Kim, and **Aviral Shrivastava**

C50. [ICPP 2011] International Conference on Parallel Processing

UnSync: A Soft Error Resilient Redundant Multicore Architecture

Reiley Jeyapaul, **Aviral Shrivastava**, Fei Hong, Abhishek Rhisheekesan, and Kyoungwoo Lee

Nominated for Best Paper Award

C49. [ICPP 2011] International Conference on Parallel Processing

Enabling Multi-threading on CGRAs

Aviral Shrivastava, Jared Pager, Reiley Jeyapaul, Mahdi Hamzeh, and Sarma Vrudhula

Nominated for Best Paper Award

C48. [CASES 2011] International Conference on Compilers, Architectures and Synthesis for Embedded Systems

Smart Cache Cleaning: Energy-Efficient Vulnerability Reduction in Embedded Processors

Reiley Jeyapaul and **Aviral Shrivastava**

C47. [CASES 2011] International Conference on Compilers, Architectures and Synthesis for Embedded Systems

Vector Class on Limited Local Memory (LLM) Multi-core Processors

Ke Bai, Di Lu, and **Aviral Shrivastava**

C46. [ASAP 2011] International Conference on Application Specific Systems, Architectures and Processors

Stack Data Management for Limited Local Memory (LLM) Multi-core Processors

Ke Bai, **Aviral Shrivastava,** and Saleel Kudchadker

C45. [DAC 2011] Design Automation Conference

CuMAPz: A Tool to Analyze Memory Access Patterns in CUDA

Yooseong Kim and **Aviral Shrivastava**

C44. **[ISLPED 2011] International Symposium on Low Power Electronics and Design**
Fast and Energy-Efficient Constant-Coefficient FIR Filters Using Residue Number System
Piotr Patronik, Krzysztof Berezowski, Stanislaw Piestrak, Janusz Biernat and **Aviral Shrivastava**

C43. **[VLSI 2011] International Conference on VLSI Design**
LA-LRU: A Latency-Aware Replacement Policy for Variation Tolerant Caches
Aarul Jain, **Aviral Shrivastava**, and Chaitali Chakrabarti

C42. **[CODES+ISSS 2010] International Conference on Hardware/Software Codesign and System Synthesis**
Heap Data Management for Limited Local Memory (LLM) Multi-core Processors
Ke Bai and **Aviral Shrivastava**

C41. **[ASAP 2010] International Conference on Application-specific Systems, Architectures and Processors**
Dynamic Code Mapping for Limited Local Memory Systems
Seung chul Jung, **Aviral Shrivastava**, and Ke Bai

C40. **[SCOPES 2010] International Conference on Software and Compilers for Embedded Systems**
B2P2: Bounds Based Procedure Placement for Instruction TLB Power Reduction in Embedded Systems
Reiley Jeyapaul and **Aviral Shrivastava**

C39. **[LCTES 2010] International Conference on Languages, Compilers and Tool support for Embedded Systems**
Cache Vulnerability Equations for Protecting Data in Processor Caches from Soft Errors
Aviral Shrivastava, Jongeun Lee, and Reiley Jeyapaul
Second Highest Rated Paper

C38. **[LCTES 2010] International Conference on Languages, Compilers and Tool support for Embedded Systems**
Operation and Data Mapping for CGRAs with Multi-bank Memory
Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, Jonghee Yoon, and Yunheung Paek

C37. **[DATE 2010] International Conference on Design Automation and Test in Europe**
Power-Accuracy Tradeoffs in Human Activity Detection
Jeffrey Boyd, Hari Sundaram, and **Aviral Shrivastava**

C36. [HIPEAC 2009] International Conference on High-Performance Embedded Architectures and Compilers

Memory-Aware Application Mapping on Coarse Grain Reconfigurable Arrays

Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, Jonghee Yoon, and Yunheung Paek

C35. [CASES 2009] International Conference on Compilers, Architectures and Synthesis for Embedded Systems

Exploiting Residue Number System for Power-Efficient Digital Signal Processing in Embedded Processors

Rooju Chokshi, Krzysztof Berezowski, and **Aviral Shrivastava**

C34. [LCTES 2009] Languages, Compilers and Tool support for Embedded Systems

A Compiler Optimization to Reduce Soft Errors in Register Files

Jongeun Lee and **Aviral Shrivastava**

C33. [VLSI-SOC 2009] International Conference on Very Large Scale Integration

Adaptive Recuced Bit-width Instruction Set Architecture (adapt-RISA)

Sandro Neves Soares, Ashok Halambi, **Aviral Shrivastava**, Flavio Rech Wagner, and Nikil Dutt

C32. [DATE 2009] International Conference on Design Automation and Test in Europe

Static Analysis to Mitigate Soft Errors in Register Files

Jongeun Lee and **Aviral Shrivastava**

C31. [DATE 2009] International Conference on Design Automation and Test in Europe

FSAF: File System Aware Flash Translation Layer for NAND Flash Memories

Sai Mylavarapu, **Aviral Shrivastava**, and Jongeun Lee

C30. [ASPDAC 2009] Asia and South Pacific Design Automation Conference

A Software Solution for Dynamic Stack Management on Scratch Pad Memory

Arun Kannan, **Aviral Shrivastava**, Amit Pabalkar and Jong-eun Lee

C29. [ASPDAC 2009] Asia and South Pacific Design Automation Conference

Compiler-Managed Register File Protection for Energy-Efficient Soft Error Reduction

Jongeun Lee and **Aviral Shrivastava**

C28. [VLSI 2009] International Conference on VLSI Design

Code Transformations for TLB Power Reduction

Reiley Jeyapaul and **Aviral Shrivastava**

C27. **[CODES+ISSS 2008] International Conference on Hardware/Software Codesign and System Synthesis**

Static Analysis of Processor Stall Cycle Aggregation

Jongeun Lee and **Aviral Shrivastava**

C26. **[HIPC 2008] International Conference on High Performance Computing**

SDRM: Simultaneous Determination of Regions and Function-to-Region Mapping for Scratchpad Memories

Amit Pabalkar, **Aviral Shrivastava**, Arun Kannan, and Jongeun Lee

C25. **[ACM MM] ACM International Conference on Multimedia**

Mitigating the Impact of Hardware Failures on Multimedia Applications - A Cross-Layer Approach

Kyoungwoo Lee, **Aviral Shrivastava**, Minyoung Kim, Nikil Dutt and Nalini Venkatasubramanian

C24. **[DIPES 2008] IFIP Conference on Distributed and Parallel Embedded Systems**

Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures

Sanghyun Park, Kyoungwoo Lee, **Aviral Shrivastava**, Nikil Dutt and Nalini Venkatasubramanian

C23. **[DATE 2008] International Conference on Design Automation and Test in Europe**

Hiding Cache Miss Penalty Using Priority-based Execution for Embedded Processors

Sanghyun Park, **Aviral Shrivastava**, and Yunheung Paek

C22. **[ASPDAC 2008] Asia and South Pacific Design Automation Conference**

SPKM: A Novel Graph Drawing based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architecture

Jonghee W. Yoon, **Aviral Shrivastava**, Sanghyun Park, Minwook Ahn, and Yunheung Paek

Best Paper Candidate

C21. **[ASPDAC 2008] Asia and South Pacific Design Automation Conference**

A Compiler-in-the-Loop Framework for Exploration of Horizontally Partitioned Caches

Aviral Shrivastava, Ilya Issenin, and Nikil Dutt

C20. **[VLSI 2008] International Conference on VLSI Design**

PTSMT: A Tool for Cross-Level Power, Performance and Thermal Exploration

Deepa Kannan, Aseem Gupta, **Aviral Shrivastava**, Fadi Kurdahi, and Nikil Dutt

C19. **[VLSI 2008] International Conference on VLSI Design**

Temperature and Process Variations aware Power Gating of Functional Units

Deepa Kannan, Vipin Mohan, Sarvesh Bhardwaj, **Aviral Shrivastava** and Sarma Vrudhula

C18. **[VLSI 2008] International Conference on VLSI Design**

Power Reduction of Functional Units considering Temperature and Process Variations

Deepa Kannan, Sarvesh Bhardwaj, **Aviral Shrivastava** and Sarma Vrudhula

C17. **[CODES+ISSS 2007] International Conference on Hardware - Software Codesign and System Synthesis**

Smart Driver for Power Reduction in Next Generation Bi-Stable Electrophoretic Display Technology

Michael A. Baker, **Aviral Shrivastava** and Karamvir Chatha

C16. **[WASP 2007] Workshop on Application-Specific Processors**

Power Conscious Mapping onto Coarse-Grained Reconfigurable Architectures using Graph Drawing based Algorithm

Jonghee W. Yoon, **Aviral Shrivastava**, Sanghyun Park, Minwook Ahn and Yunheung Paek

C15. **[DATE 2007] International Conference on Design Automation and Test in Europe**

Functional and Timing Validation of Partially Bypassed Processors

Qiang Zhu, **Aviral Shrivastava** and Nikil Dutt

C14. **[ICC 2007] International Conference on Communications**

Robust Localization in Wireless Sensor Networks through the Revocation of Malicious Anchors

Satyajayant Mishra, Guoliang Xue and **Aviral Shrivastava**

C13. **[CASES 2006] International Conference on Compiler Architecture and Synthesis for Embedded Systems**

Mitigating Soft Error Failures for Multimedia Applications by Selective Data Protection

Kyoungwoo Lee, **Aviral Shrivastava**, Ilya Issenin, Nikil Dutt, and Nalini Venkatasubramanium

C12. **[LCTES 2006] Language, compilers and tool support for embedded systems**

Bypass Aware Instruction Scheduling for Register File Power Reduction

Sanghyun Park, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek.

Best Paper Candidate

C11. **[DATE 2006] International Conference on Design Automation and Test in Europe**

Automatic Generation of Operation Tables for Fast Exploration of Bypasses in Embedded Processors

Sanghyun Park, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek.

C10. [CASES 2005] International Conference on Compiler Architecture and Synthesis for Embedded Systems

Compilation Techniques for Energy Reduction in Horizontally Partitioned Cache Architectures

Aviral Shrivastava, Ilya Issenin, and Nikil Dutt.

C9. [CODES+ISSS 2005] International Conference on Hardware - Software Codesign and System Synthesis

Aggregating Processor Free Time for Energy Reduction

Aviral Shrivastava, Eugene Earlie, Nikil Dutt and Alex Nicolau.

C8. [DATE 2005] International Conference on Design Automation and Test in Europe

PBExplore: A Framework for Compiler-in-the-Loop Exploration of Partial Bypassing in Embedded Processors

Aviral Shrivastava, Nikil Dutt, Alex Nicolau and Eugene Earlie

C7. [TechCon 2005] Semiconductor Research Corporation, TechCON

Compiler-in-the-Loop, ADL-driven Early Architectural Exploration

Aviral Shrivastava, Nikil Dutt, Alex Nicolau and Eugene Earlie.

C6. [CODES+ISSS 2004] International Conference on Hardware - Software Codesign and System Synthesis

Operation Tables for Scheduling in the Presence of Incomplete Bypassing

Aviral Shrivastava, Eugene Earlie, Nikil Dutt, Alex Nicolau.

C5. [ASPDAC 2004] Asia South-Pacific Design Automation Conference

Energy Efficient Code Generation using rISA

Aviral Shrivastava, Nikil Dutt.

C4. [ISSS 2002] International Symposium on System Synthesis

A Design Space Exploration Framework for Reduced Bit-width Instruction Set Architecture (rISA) Design

Ashok Halambi, **Aviral Shrivastava**, Partha Biswas, Nikil Dutt, Alex Nicolau.

C3. [DATE 2002] International Conference on Design Automation and Test in Europe

An Efficient Compiler Technique for Code Size Reduction using Reduced Bit-width ISAs

Ashok Halambi, **Aviral Shrivastava**, Partha Biswas, Nikil Dutt, Alex Nicolau.

C2. [SCOPES 2001] International Workshop on Software and Compilers for Embedded Systems

A Customizable Compiler Framework for Embedded Systems

Ashok Halambi, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau.

C1. [VLSI 2000] International Conference on VLSI Design

Optimal Hardware-Software Partitioning of Concurrent Sequence Flow Graphs

Aviral Shrivastava, Mohit Kumar, Sanjiv Kapoor, Shashi Kumar, M. Balakrishnan

Invited Talks

T33. **[University of California, Los Angeles] Los Angeles, CA, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T32. **[Purdue University] West Lafayette, IN, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T31. **[University of Pennsylvania] Philadelphia, PA, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T30. **[University of California, San Diego] San Diego, CA, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T29. **[Georgia Institute of Technology] Atlanta, GA, March 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T28. **[University of Texas at Austin] Austin, TX, March 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T27. **[Columbia University] New York, NY, March 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T26. **[IIT Ropar] Ropar, India, 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T25. **[IIT Delhi] New Delhi, India, 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T24. **[Texas Instruments] Houston, TX, 2010**
Compilation for Hybrid Cache and SPM Memory Hierarchy

T23. **[Marvell Semiconductors] Chandler, AZ, 2010**
Research on Low-Power Compilation

T22. **[Rainbow Studios] Phoenix, AZ, 2010**
Compilation for IBM Cell

T21. **[Professional Course] Tempe, AZ 2009**
Multi-core Programming - A 2-day Professional Course

T20. **[Caltech Center for Advanced Computing Research] Pasadena, California, 2009**
Compiler-Aided Soft Error Protection of Register File

T19. **[Space Mission Challenges SMC-IT] Pasadena, CA, 2009**
Compiler-enabled Power-Efficient Register File Protection

T18. **[Texas Instruments] Houston, TX 2009**
Multi-core Computing Challenge: Missing Memory Virtualization

T17. **[IBM Research Labs] New Delhi, India 2009**
Multi-core Computing Challenge: Missing Memory Virtualization

T16. **[Sagar Institute of Technology] Bhopal, India 2008**
The Growth of Computing and the Multi-core challenges

T15. **[Compiler Assisted SoC Assembly Workshop] Atlanta, GA, 2008**
Scratch Pad Memories: Life beyond Embedded Systems

T14. **[BK21 Workshop] Seoul, South Korea, 2008**
Compiler and Microarchitectural Techniques for Leakage Reduction

T13. **[ETRI] Seoul South Korea, 2008**
Application Mapping onto Coarse-Grain Reconfigurable Architectures

T12. **[Microsoft Research] Redmond, WA, 2007**
Compiler and Microarchitectural Techniques for Low Leakage

T11. **[LSI Systems] San Jose, 2007**
Compiler and Microarchitectural Techniques for Low Leakage

T10. **[NSF IUCRC Workshop] ASU, Tempe, AZ, 2007**
Compiler Techniques for Power Reduction in Embedded Processors

T9. **[Coware Inc.] Noida, India, 2007**
Architecture-Sensitive Compiler Techniques for Energy Reduction

T8. **[IIT Delhi] New Delhi, India, 2007**
Compiler-in-the-Loop Exploration of Embedded Systems

T7. **[Indian Institute of Sciences] Bangalore, India, 2007**
Compiler-in-the-Loop Exploration of Embedded Systems

T6. **[Workshop on Compiler Assisted SoC Assembly] Seoul National University, South Korea, 2006**
Compiler-assisted Processor Exploration and Design

T5. **[Apple Inc.] Cupertino, CA, 2006**
Architecture Sensitive Compilation Techniques for Energy Reduction

T4. **[Seoul National University] South Korea, 2006**
Architecture Sensitive Compilation Techniques for Energy Reduction

T3. **[Optimizing Compiler Assisted SoC Assembly Workshop] Seoul, South Korea, 2005**
Compiler-in-the-Loop Exploration of Programmable SoCs

T2. **[VSSAD, Intel] Hudson, MA, 2005**
Compiler-in-the-loop Design Space Exploration of XScale Microarchitectures using EXPRESSION ADL

T1. **[Strategic CAD Labs, Intel] Shrewsbury, MA, 2003**
Compiler Optimizations for Performance and Energy Improvements in Simple In-order Processors

PROFESSIONAL AND SCIENTIFIC SERVICE

Conference/Workshop Organization

- 2011
    a. **[CASA]** Organizer of the Workshop on Compiler Aided System-on-Chip Assembly
    b. **[ESWEEK]** Web Chair of Embedded Systems Week, the top embedded systems event.
- 2010
    a. **[ESWEEK]** Web Chair of Embedded Systems Week, the top embedded systems event.
    b. **[LCTES]** Organized Poster Session and Works-in-Progress session, at Languages Compilers and Tools for Embedded Systems.
- 2009
    a. **[LCTES]** Organize Poster Session and Works-in-Progress session, at the International Conference on Languages Compilers and Tools for Embedded Systems.

Technical Program Committee Membership

- 2011
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems
    d. **[RTCSA]** International Conference on Embedded and Real-Time Computing Systems and Applications
    e. **[DSD]** Euromicro Conference on Digital System Design
    f. **[VLSI]** International Conference on VLSI Design
- 2010
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems
    d. **[RTCSA]** International Conference on Embedded and Real-Time Computing Systems and Applications
    e. **[DSD]** Euromicro Conference on Digital System Design
    f. **[VLSI]** International Conference on VLSI Design

- 2009
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems
    d. **[RTCSA]** International Conference on Embedded and Real-Time Computing Systems and Applications
    e. **[DSD]** Euromicro Conference on Digital System Design
- 2008
    a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    b. **[RTCSA]** International Conference on Embedded and Real-Time Computing Systems and Applications
    c. **[DSD]** Euromicro Conference on Digital System Design
- 2007
    a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems

Session Chair

- 2011
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
- 2010
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems
- 2009
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems

- 2008
    a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
- 2007
    a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    b. **[ISLPED]** International Symposium on Low Power Electronic Design
- 2006
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis

Journal Refereeing

- **[IEEE TCAD]** IEEE Transactions on Computer Aided Design
- **[IEEE TVLSI]** IEEE Transactions on Very Large Integrated Circuits
- **[ACM TECS]** ACM Transactions on Embedded Computing Systems
- **[ACM TODAES]** ACM Transactions on Design and Analysis of Embedded Systems
- **[IJPP]** Springer International Journal on Parallel Processing

Professional Society Membership

- Association of Computing Machinery (ACM)
- Institute for Electrical and Electronic Engineers (IEEE)

UNIVERSITY SERVICE

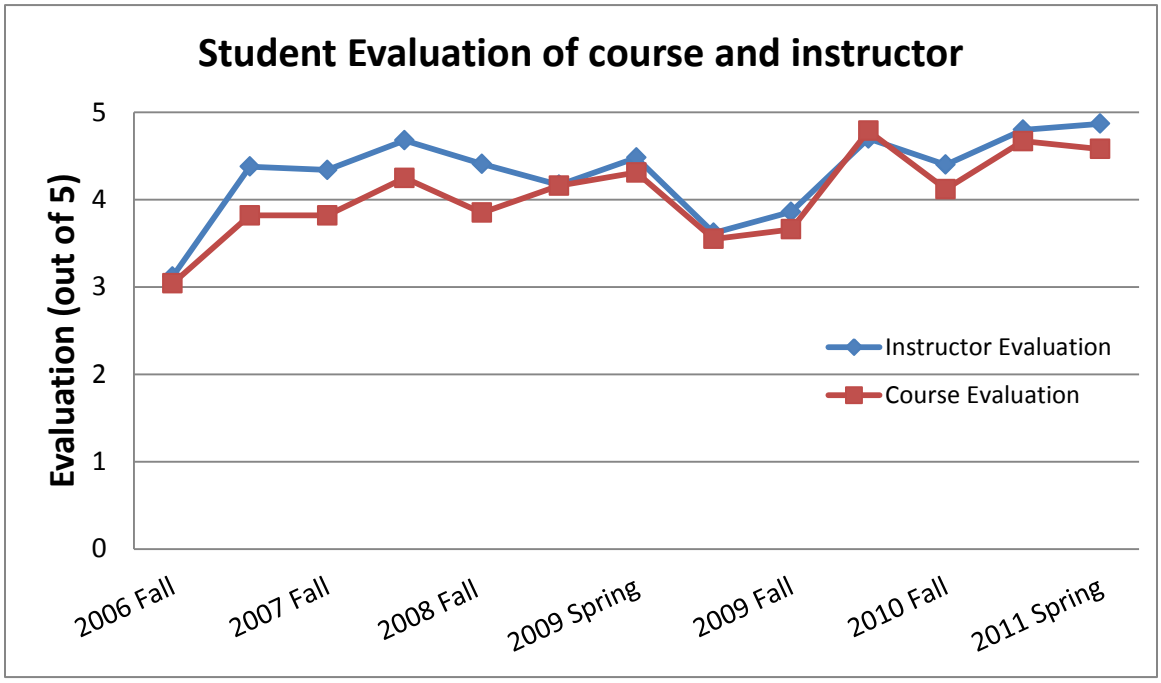
Department Committees

- 2011
    a. Computer Science and Engineering Graduate Program Committee
    b. Computer Science and Engineering Undergraduate Program Committee
- 2010
    a. Computer Science Undergraduate Program Committee
    b. Computer Science and Engineering Graduate Program Committee
- 2009
    a. Graduate Admissions Committee
- 2008
    a. Graduate Admissions Committee
    b. Computing Resources Committee
- 2007
    a. Graduate Admissions Committee
- 2006
    a. Graduate Admissions Committee

EVALUATION OF INSTRUCTION

Summary of Student Evaluations

My teaching evaluations have been steadily increasing, and have been above 4/5, except for 2006 fall (my first semester), and 2009 fall. The slightly disappointing evaluations in 2009 fall were because I was teaching two undergraduate courses, in the same semester, out of which one (CSE 420/598) was a course I was teaching for the first time. It took a lot of time and effort to prepare slides for the course, and also re-structuring the course to include new contents about modern multi-core architectures. Because of the heavy teaching load, both the courses suffered. Later when I taught CSE 420/598 again in 2010 fall, I got a very good evaluation of 4.4/5.0.



Other statistics

- Min. instructor evaluation: 3.12
- Max. instructor evaluation: 4.80
- Avg. instructor evaluation: 4.30
- Avg. course evaluation: 4.00

Details of Student Evaluations

Semester Offered	Course Name	Course Designation	Enrolled students	Evaluation	
				Course	Instructor
Spring 2011	*Low-Power Computing*	CSE 591	10	4.58	4.87
Fall 2010	*The ASU Experience*	ASU 101	19	4.67	4.80
Fall 2010	*Computer Architecture I*	CSE 420/598	47	4.12[1]	4.40[1]
Spring 2010	*Low-Power Computing*	CSE 591	8	4.79	4.70
Fall 2009	*Computer Architecture I*	CSE 420/598	52	3.66[1]	3.86[1]
Fall 2009	*Computer Organization*	CSE 230/EEE 230	29	3.55[1]	3.62[1]
Spring 2009	*Low-Power Computing*	CSE 591	20	4.31[1]	4.48[1]
Spring 2009	*Computer Organization*	CSE 230/EEE 230	17	4.16[1]	4.17[1]
Fall 2008	*Computer Organization*	CSE 230/EEE 230	22	3.85[1]	4.41[1]
Spring 2008	*Low-Power Computing*	CSE 591	8	4.25	4.68
Fall 2007	*Computer Organization*	CSE 230/EEE 230	22	3.82[1]	4.34[1]
Spring 2007	*Low-Power Computing*	CSE 591	16	3.82	4.38
Fall 2006	*Computer Organization*	CSE 230/EEE 230	41	3.04[1]	3.12[1]
	Average			**4.00**	**4.30**

Note 1: Superscript 1 in this table identifies that the score is for combined classes. For example, in Fall 2010, Computer architecture 1 class (third row) was composed of students from two sections, CSE 420, and CSE 598. For such combined classes, I have computed the average scores weighted by the number of student responses. For example, in this class, instructor evaluation was 4.29 by 18 CSE 420 students, and 4.80 by 5 CSE 591 students. As a result, the average student evaluation for this class is computed as (4.29*18+4.80*5)/(18+5) = 4.40.

Note: One of the most important parameter that I use to personally judge the quality of my teaching is the attendance of students in class. I do not take roll calls, or require students to attend the classes, or even have marks for class participation (and there is certainly no shortage of that). Inspite of all this, my classes consistently have very high (close to 100%) attendance, for almost all of my courses. I consider this as very a strong reaffirmation of the fact that in this digital age, when there are multiple sources of gaining knowledge (especially true in computer science), students find my teaching an effective way of learning.

New Courses Developed

I have spent significant effort towards revamping the existing courses, and creating new courses. I have revamped two undergraduate courses and designed a new graduate research course. Below is a summary of the major teaching innovations in these courses.

Teaching Innovation in CSE 230: Computer Organization and Assembly Language

I completely revitalized the computer organization class. I changed the focus of the class from learning assembly language to learning the design of a processor. Today there is little value in learning assembly language programming, because firstly it is just another programming language, and secondly, thanks to advanced compiler technology, programming in assembly language is now minimal. Now I teach only 3 weeks of assembly programming and 5 weeks of processor design, rather than the other way round. Students have learnt how to program in high level languages, like Java in CSE 100 (a pre-requisite), and they also know how to design small logic components like an adder, multiplexer etc. in CSE 120 (another pre-requisite). This course needs to fill in the gap by teaching them how to implement high-level languages using these small logic components – which is exactly what a processor is.

Teaching Innovation in CSE 420: Computer Architecture I

Computer architectures have rapidly evolved, and now it is going through a very big transformation, whose affects will soon be visible to the whole applications community. The transformation I am referring to is the shift to multi-core processors. Power and temperature problems in computers are forcing us to slow down the computation, and therefore the only way to improve performance will be through the use of parallelism, in the form of multi-cores. All computing is going multi-core, including cell phones. However the computer architecture textbooks are old, and do not deal multi-cores architecture or programming. In order to prepare the students to compete in the necessarily multi-core computing world, I increased the emphasis on multi-core architectures. I taught them about the new and popular multi-core architectures, and how to program them. In addition, I gave assignments aimed at understanding application development on the multi-core processors. All students were able to finish the assignment. Students were very excited about programming on a cutting-edge platform, and claimed it to be the best assignment.

Teaching Innovation in CSE 591: Low-Power Computing

This research class is aimed at preparing beginning Ph.D. students in computer science and engineering to start focusing on research. Most research in computer engineering is somehow related to power, since power is the most important design metric both for battery-powered embedded systems, e.g., cell phones, and in high performance systems. This course covers a wide variety of topics in low-power computing, from transistor level to system level techniques of modeling and optimizing for power consumption. The objective of this research class is to come up with some novel scheme for power reduction, and submit the work to a conference.

In the Spring 2011 class, students did projects on i) optimizing the power consumption of graphics applications, ii) profile guided branch hinting on the Cell processor, iii) Implementing Standard Template Library on Cell processor, iv) Data Prefetching in CUDA, v) Enabling multi-threading on CGRAs, and vi) modeling the impact of soft error on processor pipelines. Projects ii), iii), iv), and v) have resulted in papers. The paper on project iii) is already accepted for publication in CASES 2011, and enabling multithreading the others are under submission. This was a highly successful class, and in the student evaluations, students claimed that there must be more research classes like this at ASU.

STUDENT THESES AND DISSERTATIONS SUPERVISED

Graduated Ph.D. Students

GP1. **Reiley Jeyapaul**, defended his thesis in Fall 2011
Thesis: Smart Compilers for Reliable and Power-efficient Embedded Computing
Will continue as a post-doc with Dr. Shrivastava at ASU

Graduated Master's Students

GM7. **Fei Hong**, graduated in Spring 2011
Thesis: UnSync: A Soft-Error Resilient Redundant CMP Architecture
Employed by Allied Telesis, San Jose, CA.

GM6. **Saleel Kudchadker**, graduated in Fall 2010
Thesis: Managing Stack Data on Limited Local Memory Multi-core Architectures
Employed by AMD, Sunnyvale, CA.

GM5. **Seung-chul Jung**, graduated in Spring 2010
Thesis: Dynamic Code Mapping for Limited Local Memory Architectures
Entrepreneur.

GM4. **Sai Mylavarapu**, graduated in Spring 2009
Thesis: Improving Application Response Times of Nand Flash based Systems
Employed by Qualcomm, Sunnyvale, CA.

GM3. **Rooju Chokshi**, graduated in Spring 2009
Thesis: Residue number system enhancements for programmable processors
Employed by Microsoft, Redmond WA.

GM2. **Amit Pabalkar**, graduated in Fall 2009
Thesis: A Dynamic Code Mapping Technique for Scratch Pad Memories in Embedded Systems
Employed by Nvidia, Santa Clara, CA.

GM1. **Arun Kannan**, graduated in Fall 2009
Thesis: A Software-Only Solution for Stack Management on Systems with Scratch Pad Memory
Employed by Intel, Santa Clara, CA.

Current PhD Students

CP4. **Ke Bai,** Computer Science, Fall 2008 – present.
Thesis: *Memory Management on Limited Local Memory Multi-core Processors*.
Status: Thesis Proposal in Fall 2011, Expected graduation: Fall 2012.

CP3. **Yooseong Kim,** Computer Science, Fall 2009 – present.
Research topic: *Memory Management in Non Coherent Cache Architectures*.
Expected graduation: Fall 2013.

CP2. **Jing Lu,** Computer Science, Spring 2011 – present.
Research topic: *Software Branch Hinting for Power-Efficient Processors*.
Expected graduation: Fall 2014.

CP1. **Mahdi Hamzeh,** Computer Science, Fall 2010 – present.
Thesis: *Compilation for Coarse Grain Reconfigurable Architectures (CGRAs)*.
Status: Expected graduation: Fall 2014.

Current Masters Students

CM8. **Shashank Reddy Kaareddy,** Computer Science, Spring 2011 – present
Research topic: Architecture Exploration of CGRA
Expected graduation: Fall 2012.

CM7. **Jian Cai,** Computer Science, Spring 2011 – present
Research topic: Efficient multi-threaded communication on limited memory multi-core processors.
Expected graduation: Fall 2012.

CM6. **Tushar Rawat,** Computer Science, Spring 2011 – present
Research topic: Efficient Execution multi-threaded programs on Hybrid distributed and shared memory multi-core processors.
Expected graduation: Fall 2012.

CM5. **Abhishek Rhisheekeesan,** Computer Science, Spring 2011 – present.
Research topic: Power-Efficient Reliability in Multi-core Architectures.
Expected graduation: Fall 2012.

CM4. **Bryce Holton,** Computer Science, Fall 2010 - present.
Research topic: Code prefetching in Limited Local Memory Multi-core Processors.
Expected graduation: Fall 2012.

CM3. **Russel Dill,** Computer Science, Fall 2010 – present
Research topic: Integerated Design of flash translation layer and flash file system.
Expected graduation: Fall 2012.

CM2. **Jared Pager,** Computer Engineering, Spring 2010 – present
Research topic: Enabling multi-threading on CGRAs.
Expected graduation: Spring 2011.

CM1. **Di Lu,** Computer Science, Spring 2010 – present
Research topic: Vector Class on Limited Local Memory Multi-core Processors.
Expected graduation: Spring 2011.

Current Undergraduate Students

CU1. **Anurag Kamasamudram** (Spring 2011-present)
Research Topic: Automatic Parallelization of multi-threaded applications on the Cell Processor

SAMPLE PUBLICATIONS

The four sample publications that I have selected are:

1. *Enabling Multithreading in CGRAs*
   Aviral Shrivastava, Jared Pager, Reiley Jeyapaul, Mahdi Hamzeh, and Sarma Vrudhula
   ICPP 2011: *Proceedings of the International Conference on Parallel Processing*
   Acceptance rate: 22%

2. *CuMAPz: A tool to Analyze Memory Access Patterns in CUDA*
   Yooseong Kim and Aviral Shrivastava
   DAC 2011 :*Proceedings of the 48th Design Automation Conference*
   Acceptance rate: 24%

3. *Heap Data Management for Limited Local Memory (LLM) Multi-core Processors*
   Ke Bai and Aviral Shrivastava
   CODES+ISSS 2010 :*Proceedings of the 8th IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis*
   Acceptance rate: 34%

4. *Cache Vulnerability Equations for Protecting Data in Processor Caches from Soft Errors*
   Aviral Shrivastava, Jongeun Lee, and Reiley Jeyapaul
   LCTES 2010 :*Proceedings of the 2010 International Conference on Languages Compilers and Tools for Embedded Systems*
   Acceptance rate: 31%
   Second Best Paper

Note: ASU student names are underlined