REVIEW EXAM 3

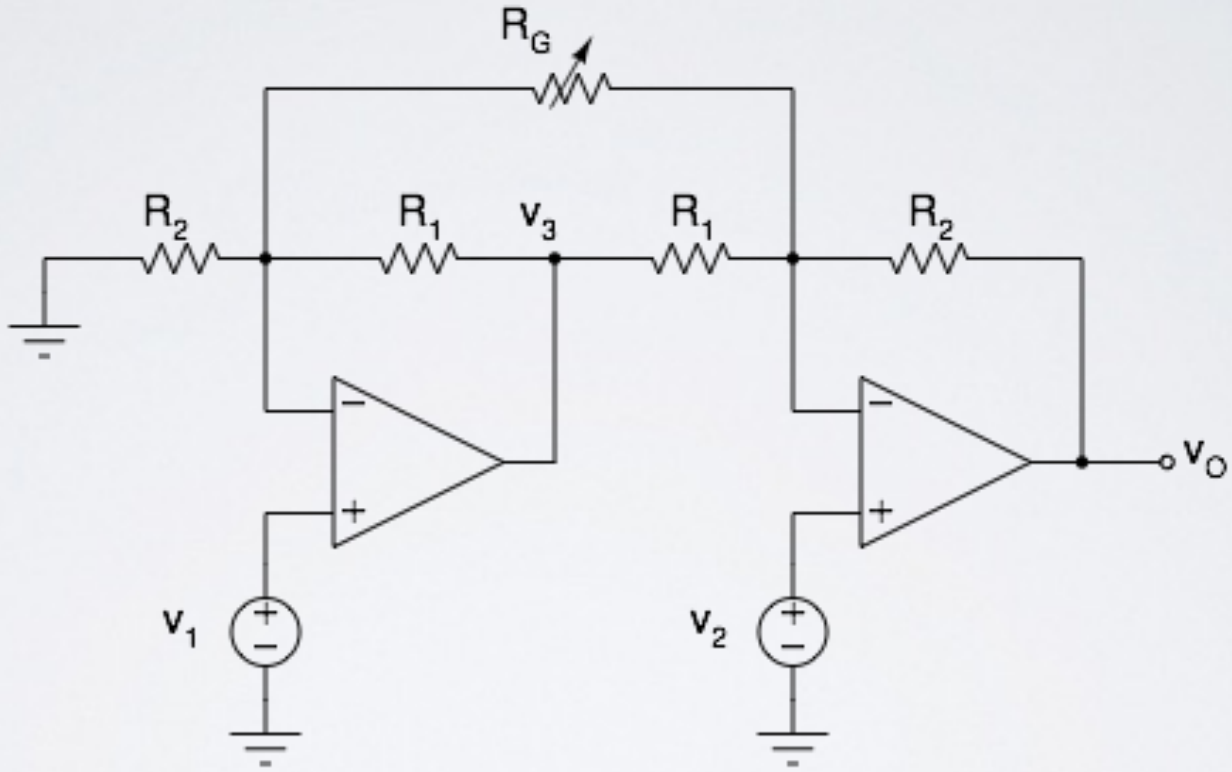
INEL 4202 - Fall 2015

TOPICS

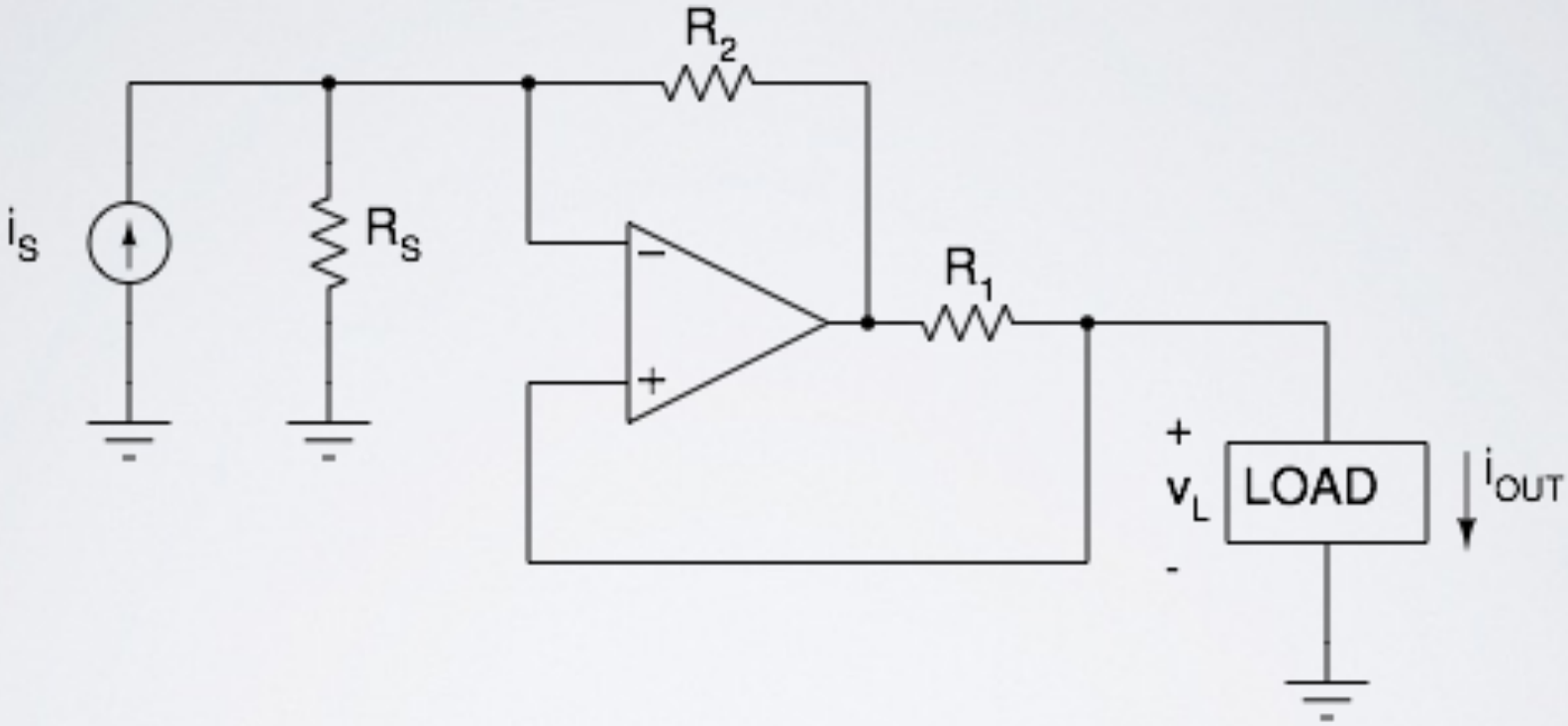
18 (10/16)	Integrators and differentiators, Applications	2.5	2.79, 2.80
19 (10/21)	Current sources	7.(4,5)	7.(46, 47, 48, 55, 56, 58, 67, 70, 76, 77, 78)
20 (10/23)	The differential amplifier	8.(1-3, 5)	8.(1, 2, 9, 25, 27, 29, 32, 33, 53, 60, 61, 62, 63, 64, 85, 91, 94, 102)
21 (10/28)	DC analysis of the 741 opamp	12.(3,4)	12.(23, 24, 25, 28, 29, 37, 39)
22 (10/30)	AC analysis of the 741 op-amp	12.5	12.(42, 43, 47, 50)
23 (11/4)	Frequency response and slew rate	12.6	12.(59, 62, 63)
24 (11/6)	CMOS opamp DC and AC analysis	12.1	12.(2, 3, 5, 6)
25 (11/10)	Freq. resp. and slew rate of CMOS opamp		12.(9, 10, 11)
26 (11/13)	Folded cascode opamp	12.2	12.(15, 16, 18, 19)

OP-AMP & APPLICATIONS

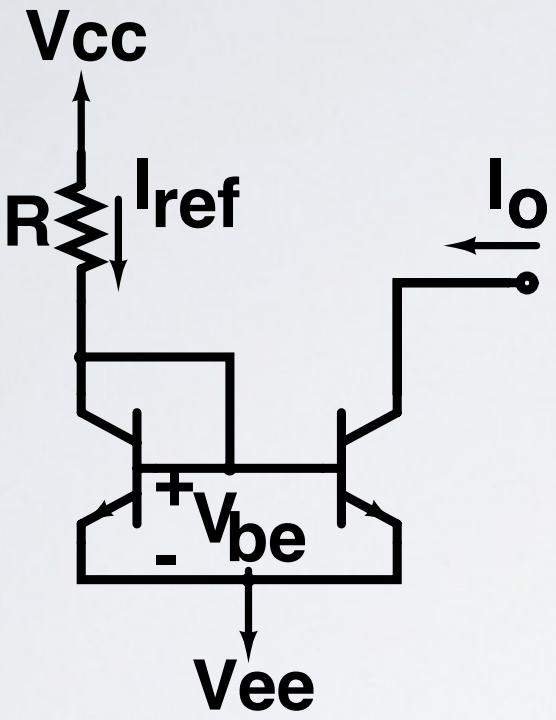
DUAL-OPAMP IA WITH VARIABLE GAIN



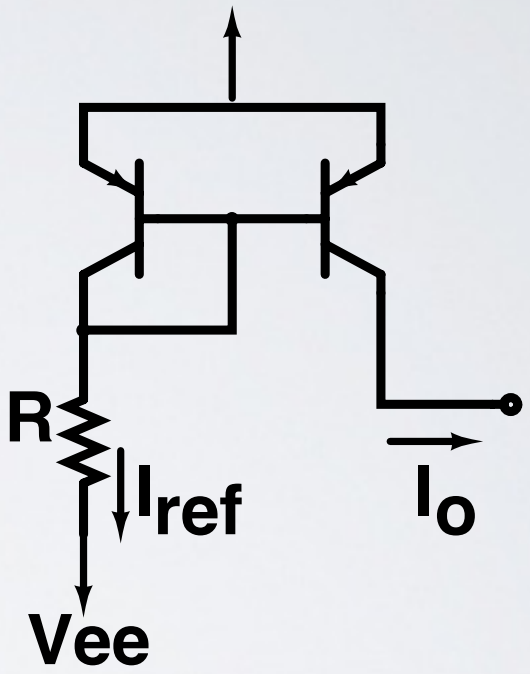
GROUNDED-LOAD CURRENT AMP



CURRENT SOURCES
&
ACTIVE LOADS

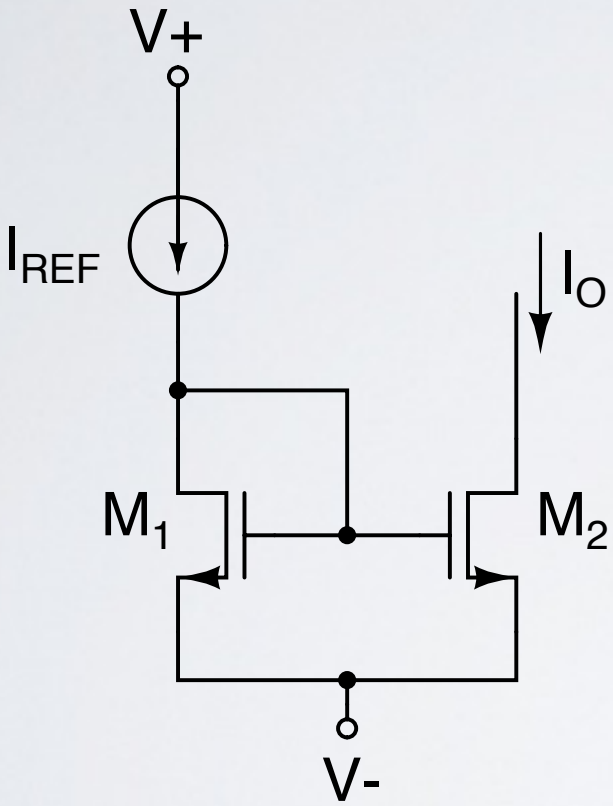


Basic C.S.



Basic C.S. with PNP BJTs

MOSFET CSs

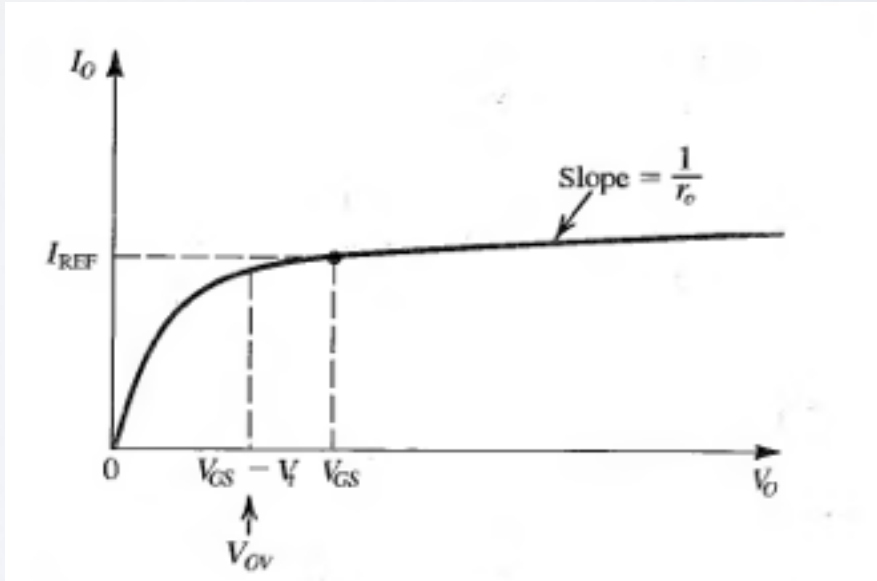


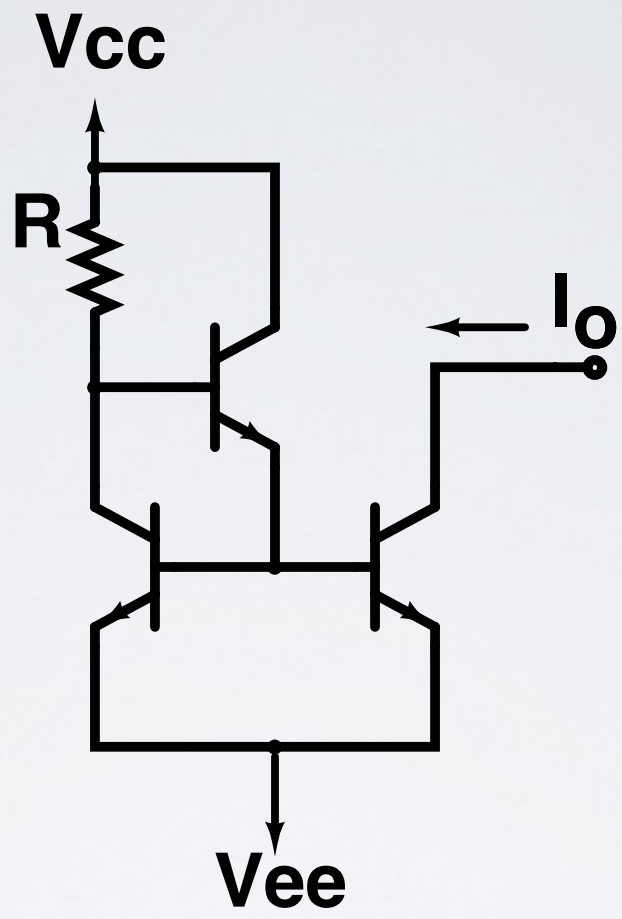
$$v_{GS,1} = v_{GS,2} = v_{DS,1}$$

$$i_{D,1} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (v_{GS,1} - V_t)^2$$

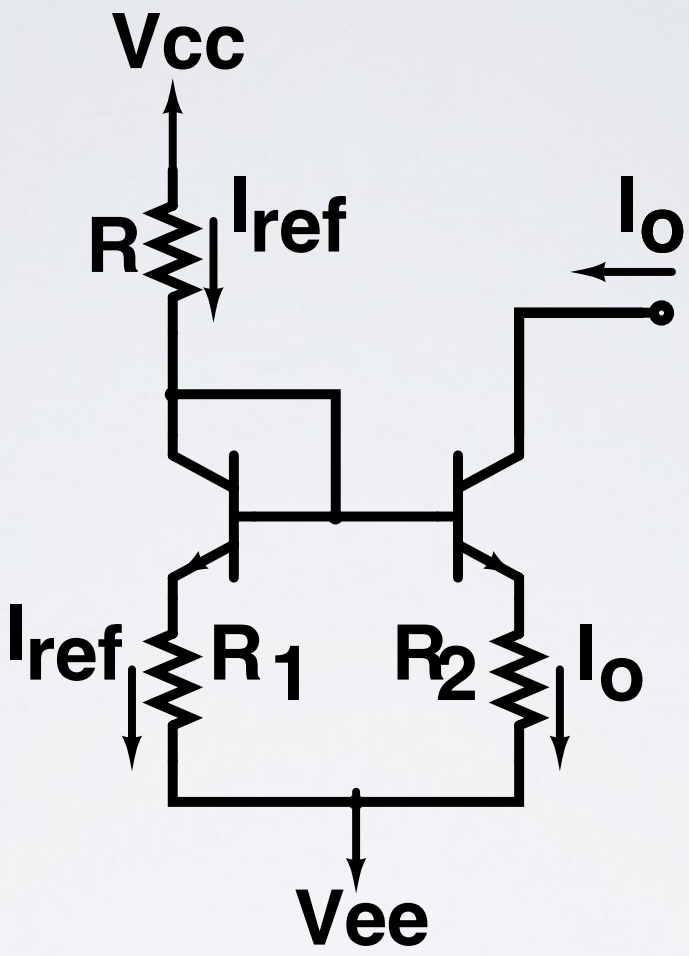
$$i_{D,2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (v_{GS,1} - V_t)^2$$

$$\frac{i_{D,2}}{i_{D,1}} = \boxed{\frac{I_O}{I_{REF}} = \frac{(W/L)_1}{(W/L)_2}}$$

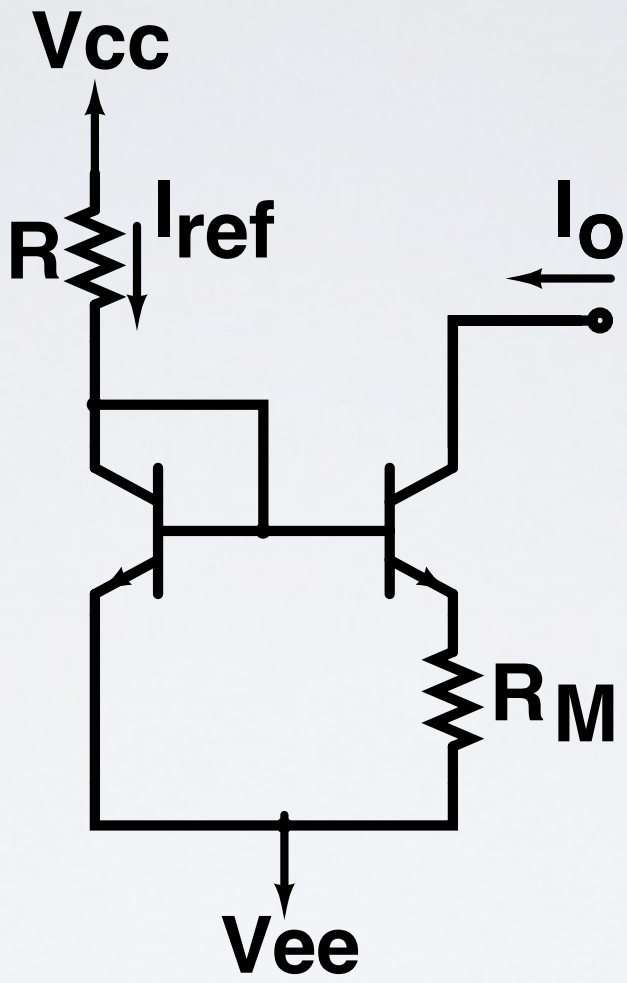




Mirror with base-current compensation

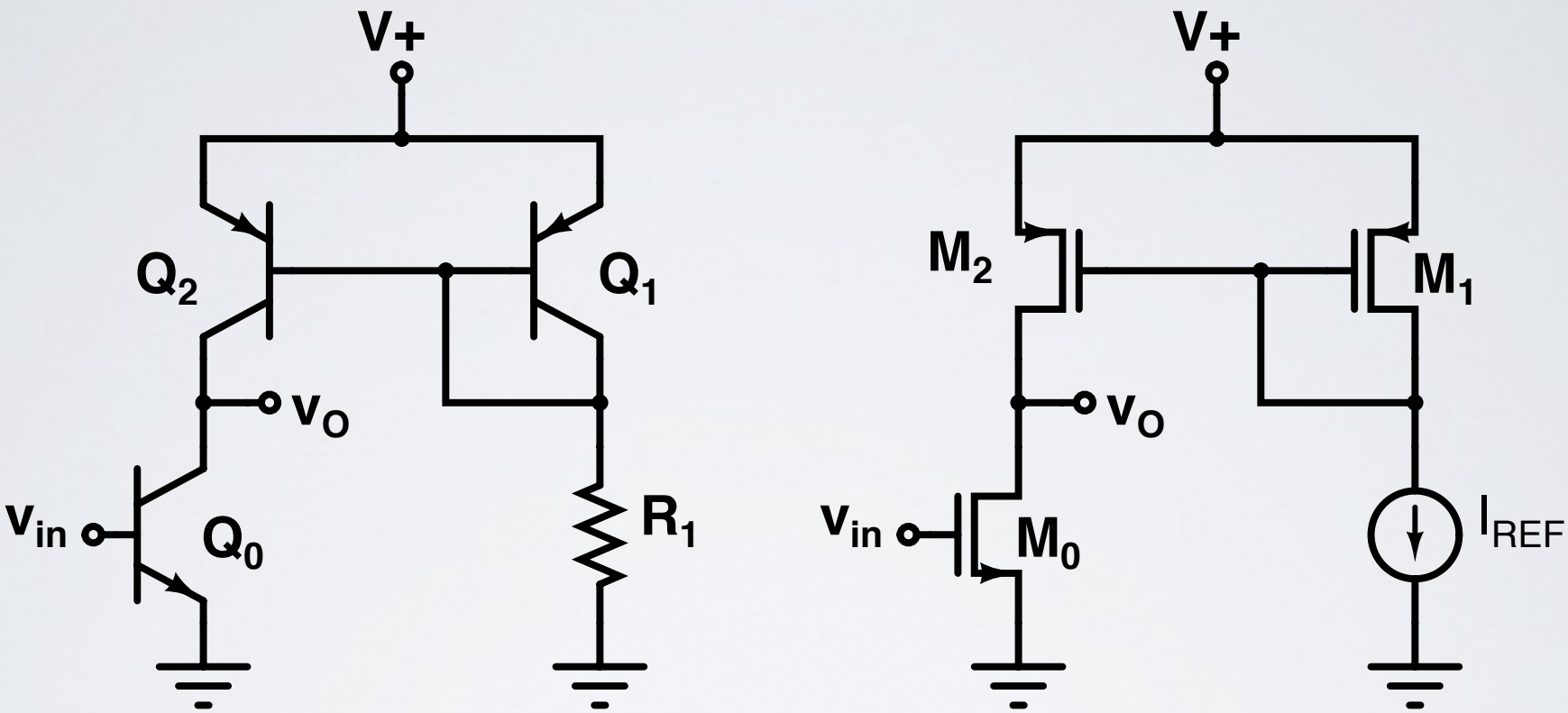


Basic Source with Emitter Resistors



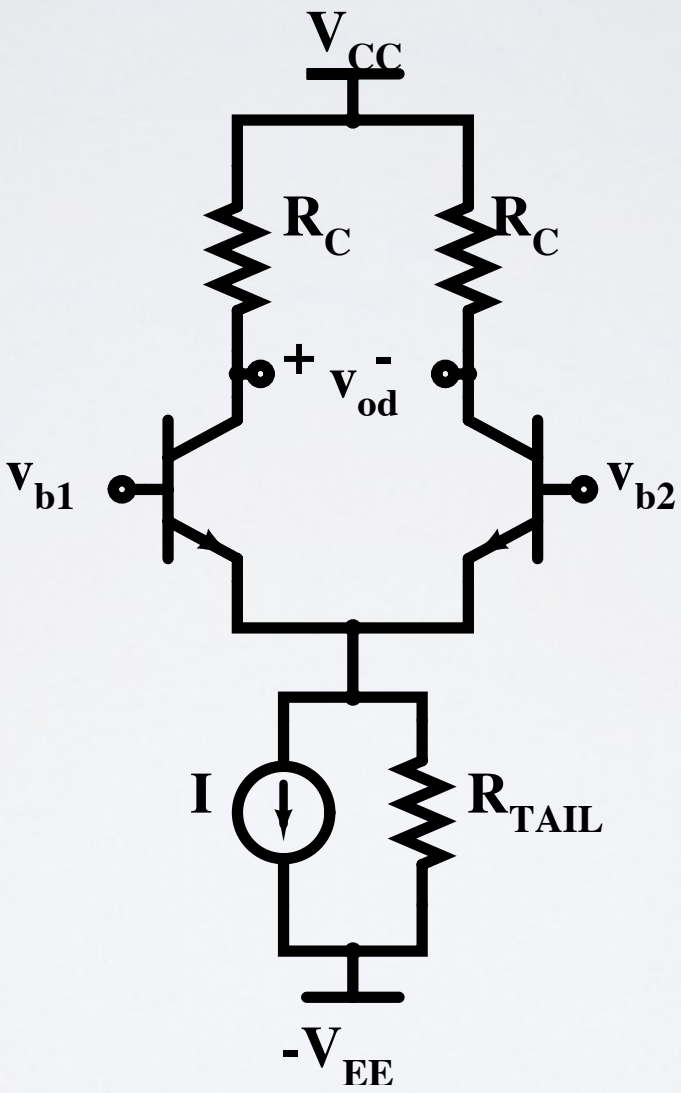
Widlar C.S.

Active Loads

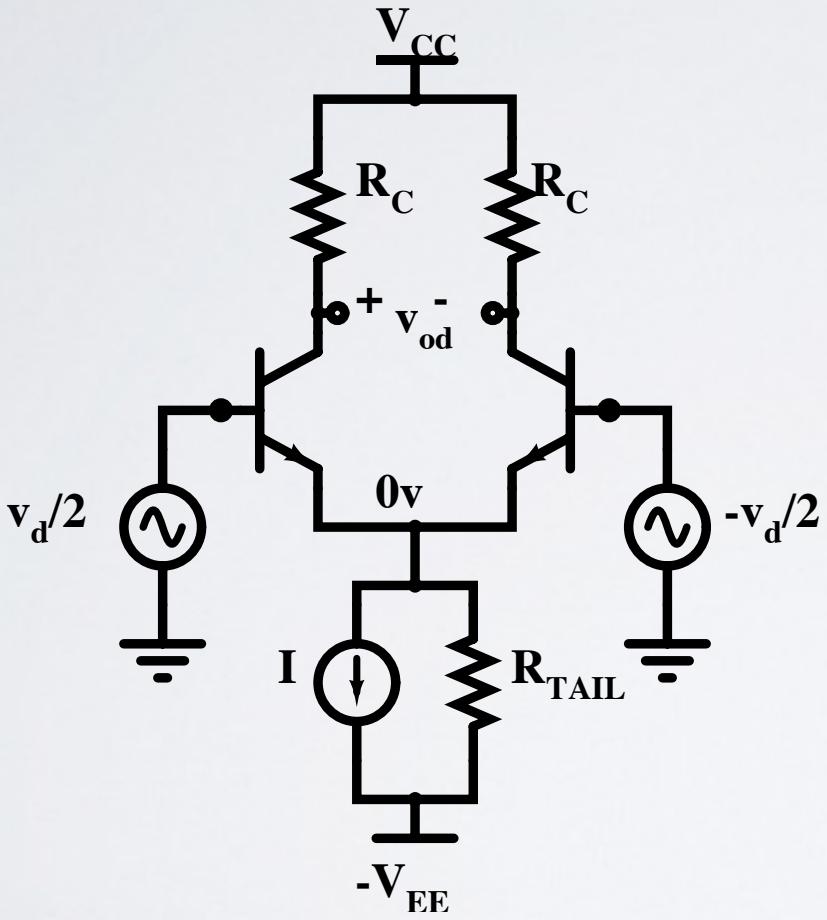


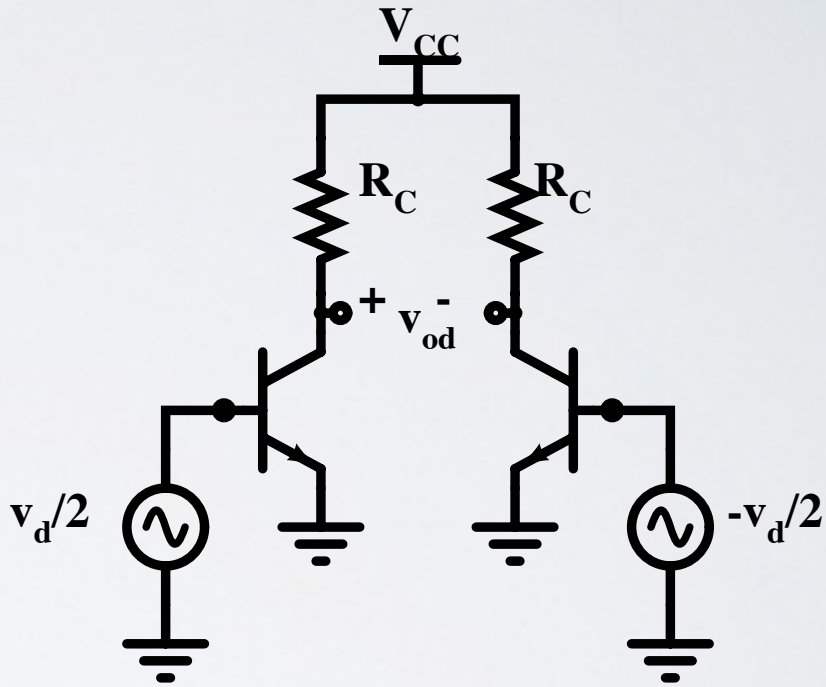
DIFFERENTIAL AMPLIFIERS

Basic Configuration

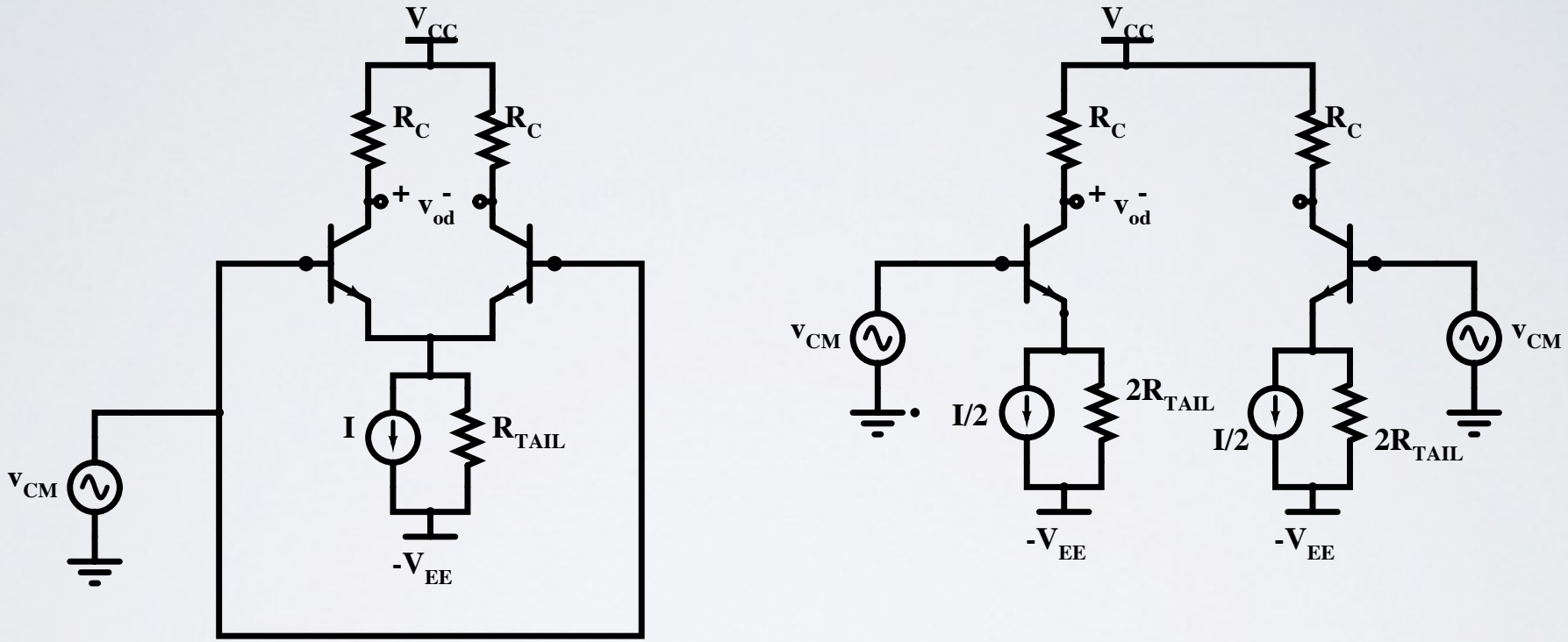


Differential-mode gain and input resistance.

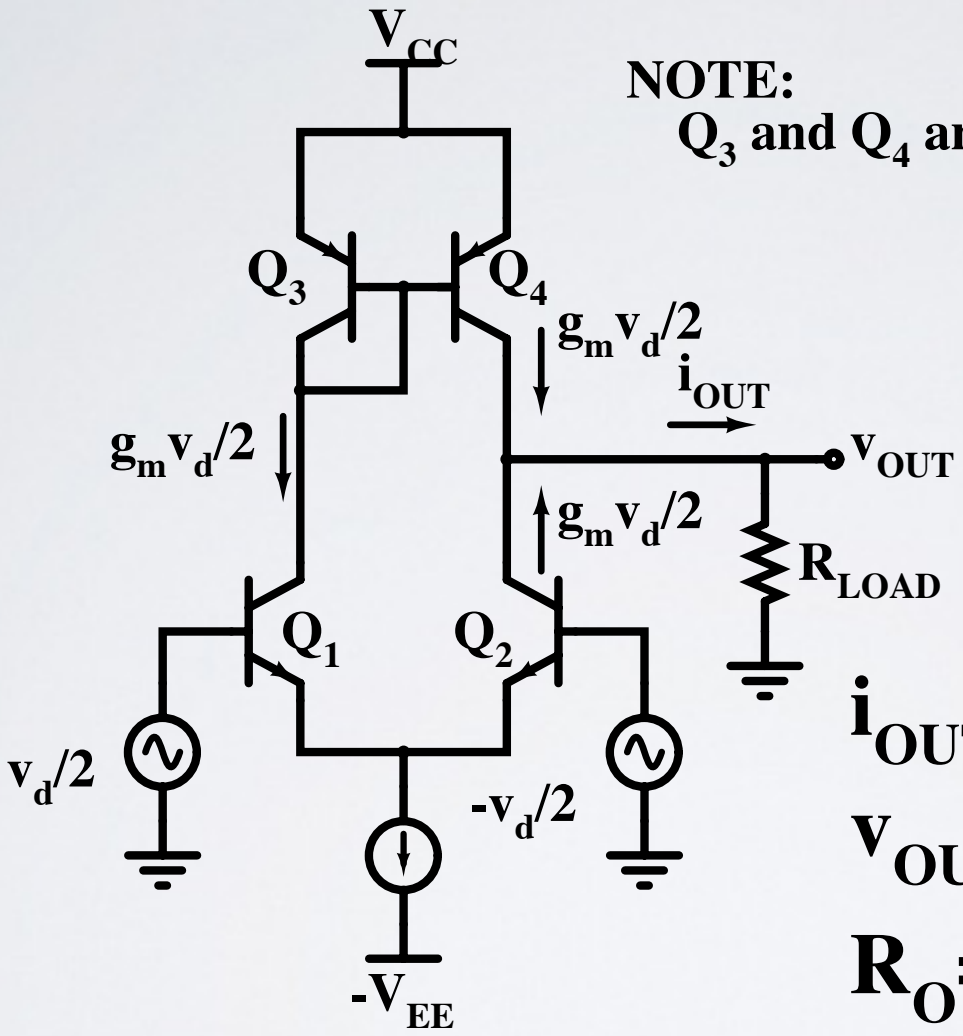




Common-mode gain and input resistance.



Active Loads

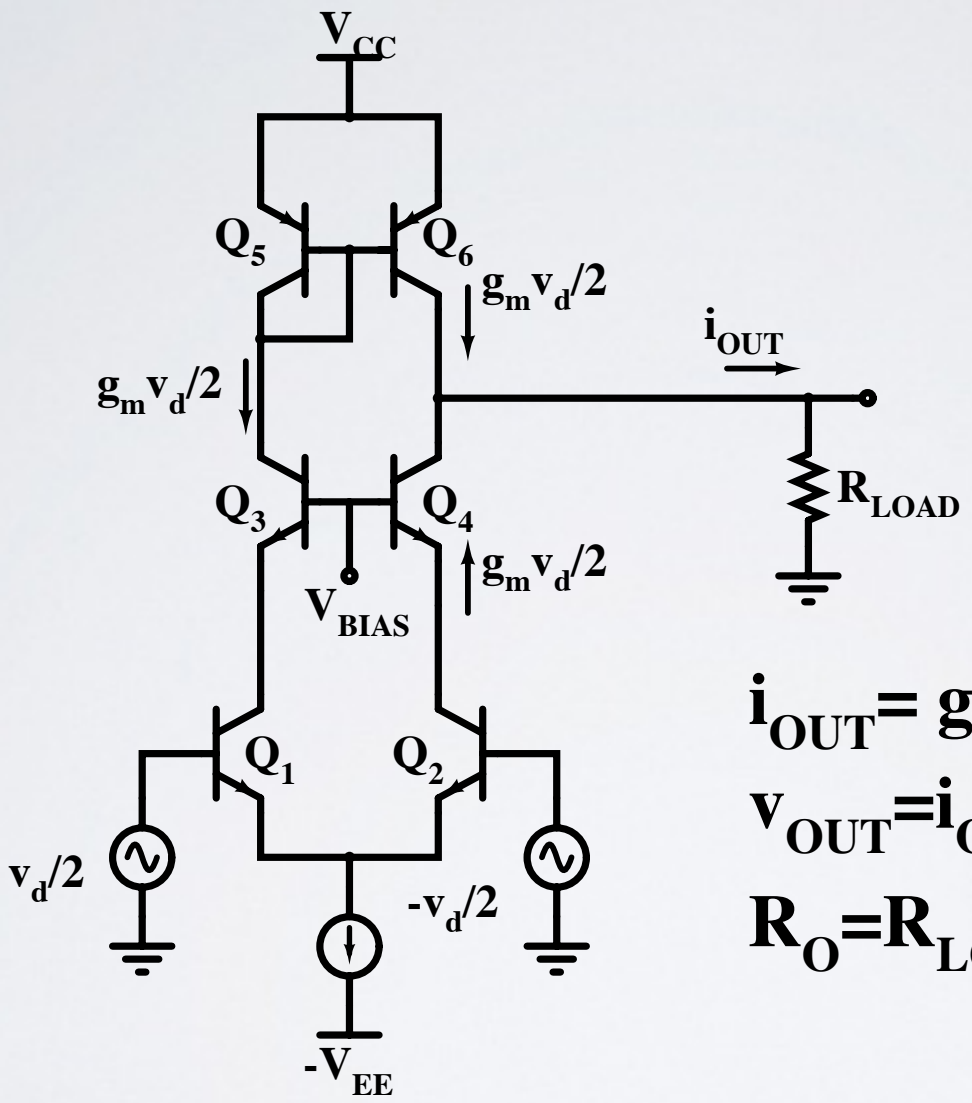


NOTE:
Q_3 and Q_4 are PNP BJTs

$$i_{OUT} = g_m v_d$$

$$v_{OUT} = i_{OUT} R_O$$

$$R_O = R_{LOAD} \| r_{O2} \| r_{O4}$$

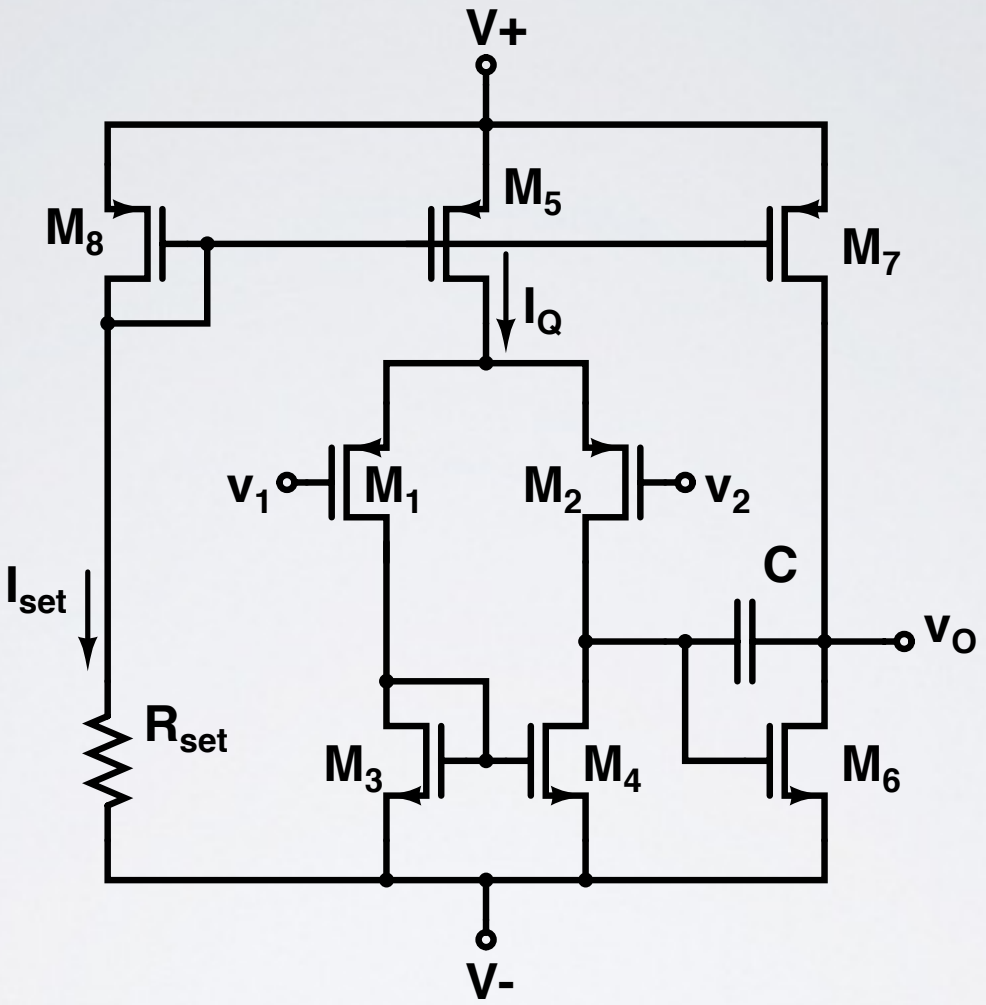


$$i_{OUT} = g_m v_d$$

$$v_{OUT} = i_{OUT} R_O$$

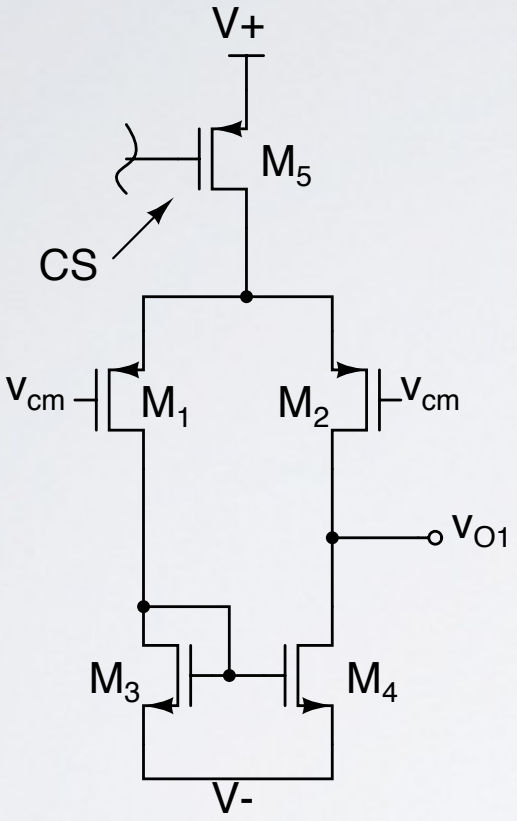
$$R_O = R_{LOAD} \| r_{O6} \| (1+\beta) r_{O}$$

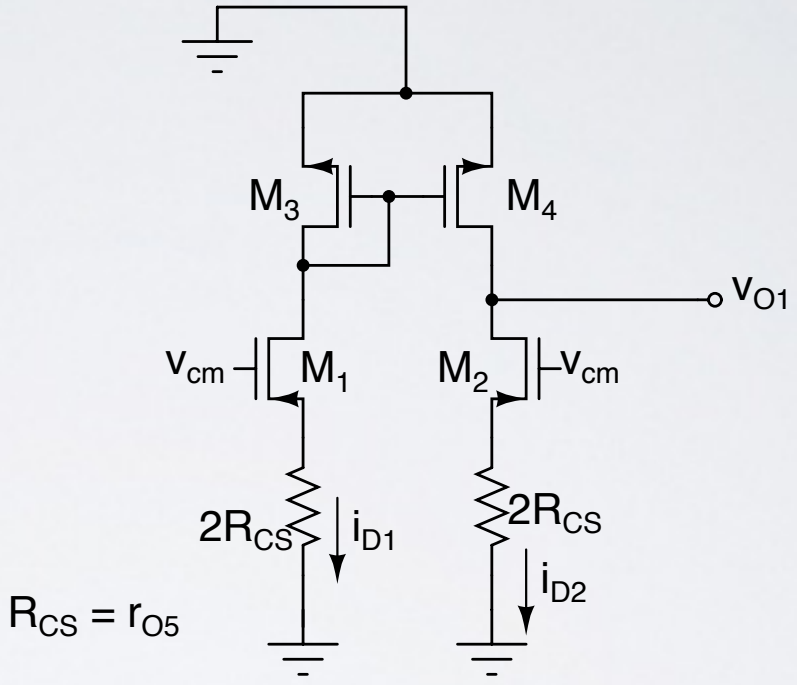
CMOS OPAMPS



Example 13.8: Find DC bias current when $V_{TN}=0.5V$, $\frac{1}{2}\mu_n C_{ox}=20uA/V^2$, $\lambda_n=0.02V^{-1}$, $V_{TP}=-0.5V$, $\frac{1}{2}\mu_p C_{ox}=10uA/V^2$, $\lambda_p=0.02V^{-1}$, $R_{SET}=225k\Omega$,$(W/L)_3=(W/L)_4=6.25$, $(W/L)_{OTHER}=12.5$, V+=5V, V-=-5V. (ANSWER: $I_{REF}=39.7uA$)
Example 13.9: Find gain. (ANSWER: $A_v=(125)(125)=15{,}625$)

A_{CM} for differential stage with active load due to and error ε in K (for example, $(W/L)_1 = (1+\varepsilon)(W/L)_2$)





small-signal equivalent ckt.

i_{D1} is the incremental drain current

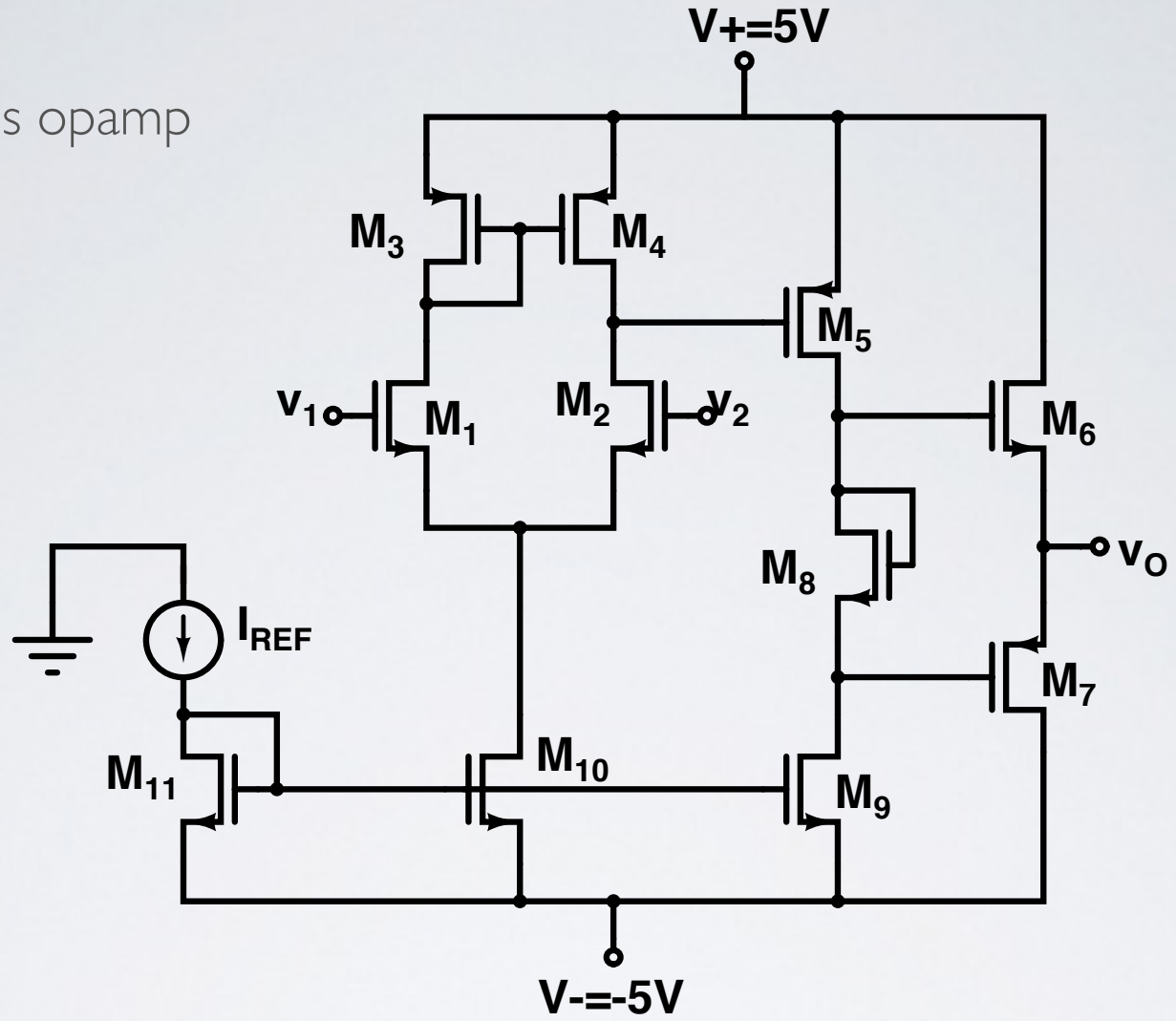
A_{CM} for differential stage with active load due to and error $\boldsymbol{\varepsilon}$ in K (for example, $(W/L)_1 = (1+\boldsymbol{\varepsilon})(W/L)_2$)

$$
\begin{aligned}
i_{d,1} &= g_{m1} v_{gs,1} \\
v_{gs,1} &= v_{g,1} - v_{s,1} \\
v_{g,1} &= v_{cm} \\
v_{s,1} &= 2R_{CS} \times i_{d,1} \\
i_{d,1} &= g_{m1}\left(v_{cm} - 2R_{CS} \times i_{d,1}\right) \\
i_{d,1}\left(1 + g_{m1} 2R_{CS}\right) &= g_{m1} v_{cm} \\
i_{d,1} &= \frac{g_{m1} v_{cm}}{1 + g_{m1} 2R_{CS}} \\
i_{d,2} &= \frac{g_{m2} v_{cm}}{1 + g_{m2} 2R_{CS}} \\
g_{m1} &= g_{m2}\left(1 + \epsilon\right) \\
i_{o,1} &= i_{d,1} - i_{d,2} = \frac{g_{m2}\left(1+\epsilon\right) v_{cm}}{1 + g_{m2}\left(1+\epsilon\right) 2R_{CS}} - \frac{g_{m2} v_{cm}}{1 + g_{m2} 2R_{CS}} \\
v_{o,1} &= i_{o,1}\left(r_{o4} \| r_{o2}\right)
\end{aligned}
$$

If $2g_{m2}\epsilon R_{CS} \ll 1$, (or equivalently, $\epsilon \ll \frac{1}{2g_{m2}R_{CS}}$)

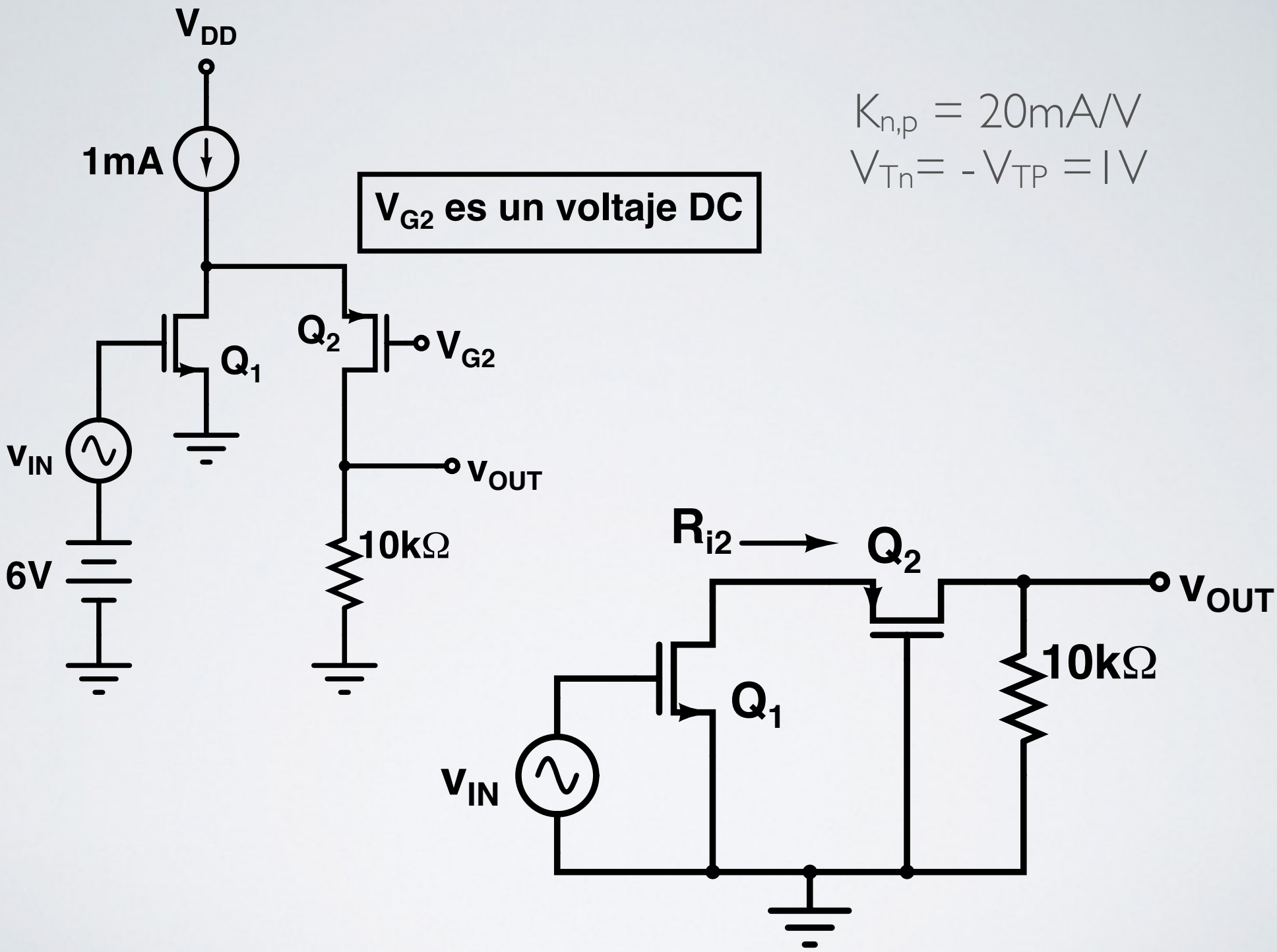
$$
\begin{aligned}
i_{o,1} &\simeq \frac{g_{m2}\epsilon v_{cm}}{1 + g_{m2} 2R_{CS}} \\
A_{cm,1} &= \frac{v_{o,1}}{v_{cm}} = \frac{g_{m2}\epsilon\left(r_{o4} \| r_{o2}\right)}{1 + g_{m2} 2R_{CS}} \Rightarrow CMRR = \frac{1 + g_{m2} 2R_{CS}}{\epsilon}
\end{aligned}
$$

Three-stage cmos opamp



Example: Find DC and AC characteristics. V_{TN}=0.7V, k_n'=80uA/V^2, λ_n=0.01V^{-1}, V_{TP}=-0.7V, k_P'=40uA/V^2, λ_p=0.015V^{-1}, I_{REF}=160μA, $(W/L)_1=(W/L)_2$=15/1, $(W/L)_3=(W/L)_4$=40/1, $(W/L)_5$=80/1, $(W/L)_6$=25/1, $(W/L)_7$=50/1, $(W/L)_9=(W/L)_{10}=(W/L)_{11}$=20/1. Select $(W/L)_8$ so that $V_{GS6}=V_{GS7}$=0.85V.

ANSWER: $(W/L)_8$ = 4; $I_{D6}=I_{D7}$=22.5uA; A_v=(219)(-253)=-55407 V/V.



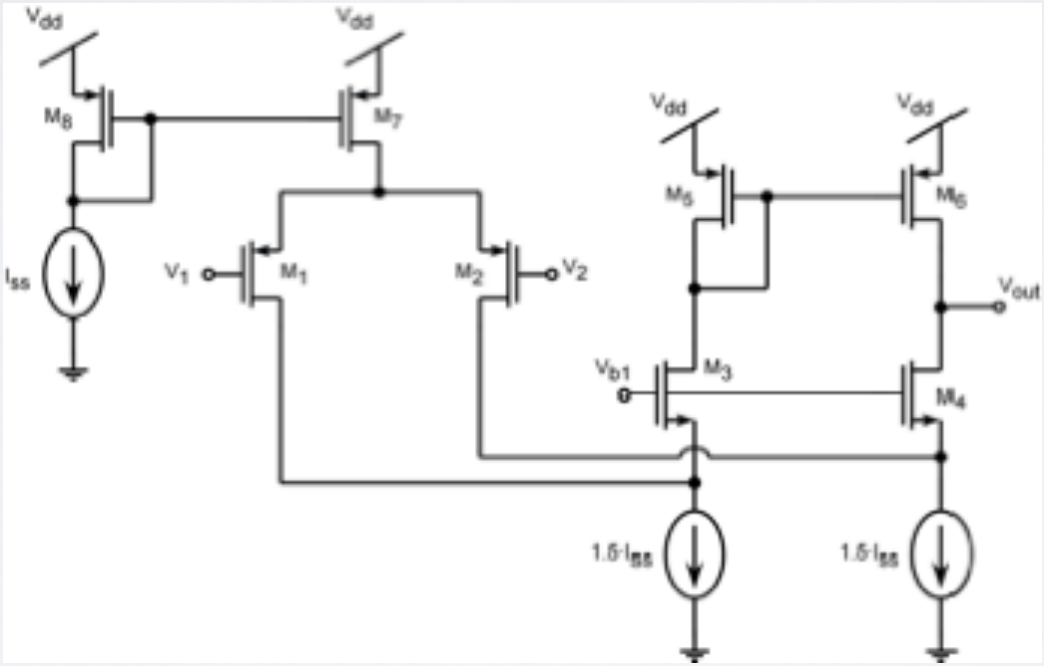
$K_{n,p} = 20mA/V$

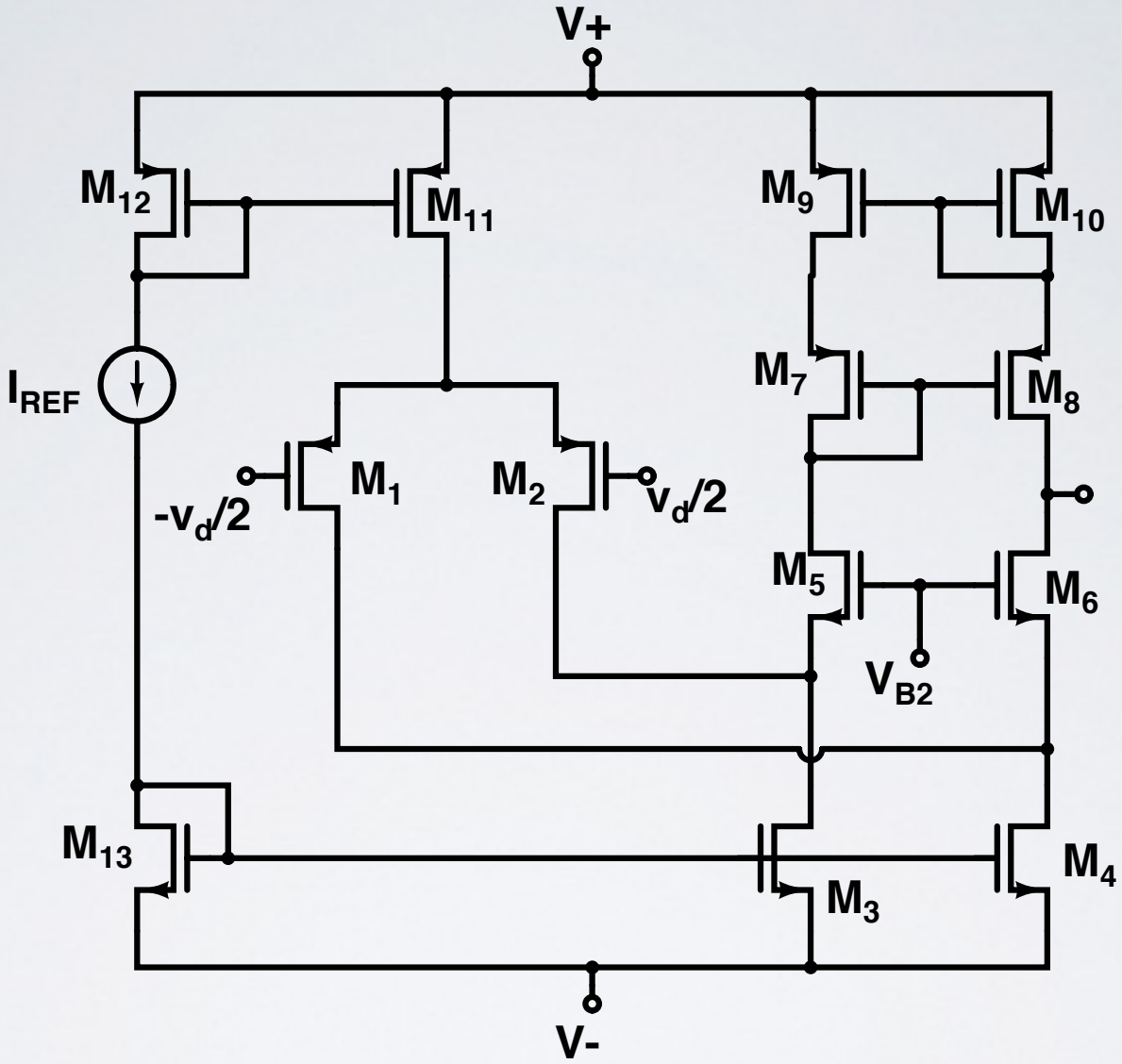
$V_{Tn} = -V_{TP} = 1V$

For the following CMOS amplifier, where V_{b1} and V_{b2} are DC voltages for proper operation of the circuit:

a) identify the negative and the positive terminals
b) find the expression for the differential gain $A_{id}=V_{out}/V_{id}$
c) find the expression for the differential input resistance R_{ind}
d) find the expression for the output resistance R_{out}

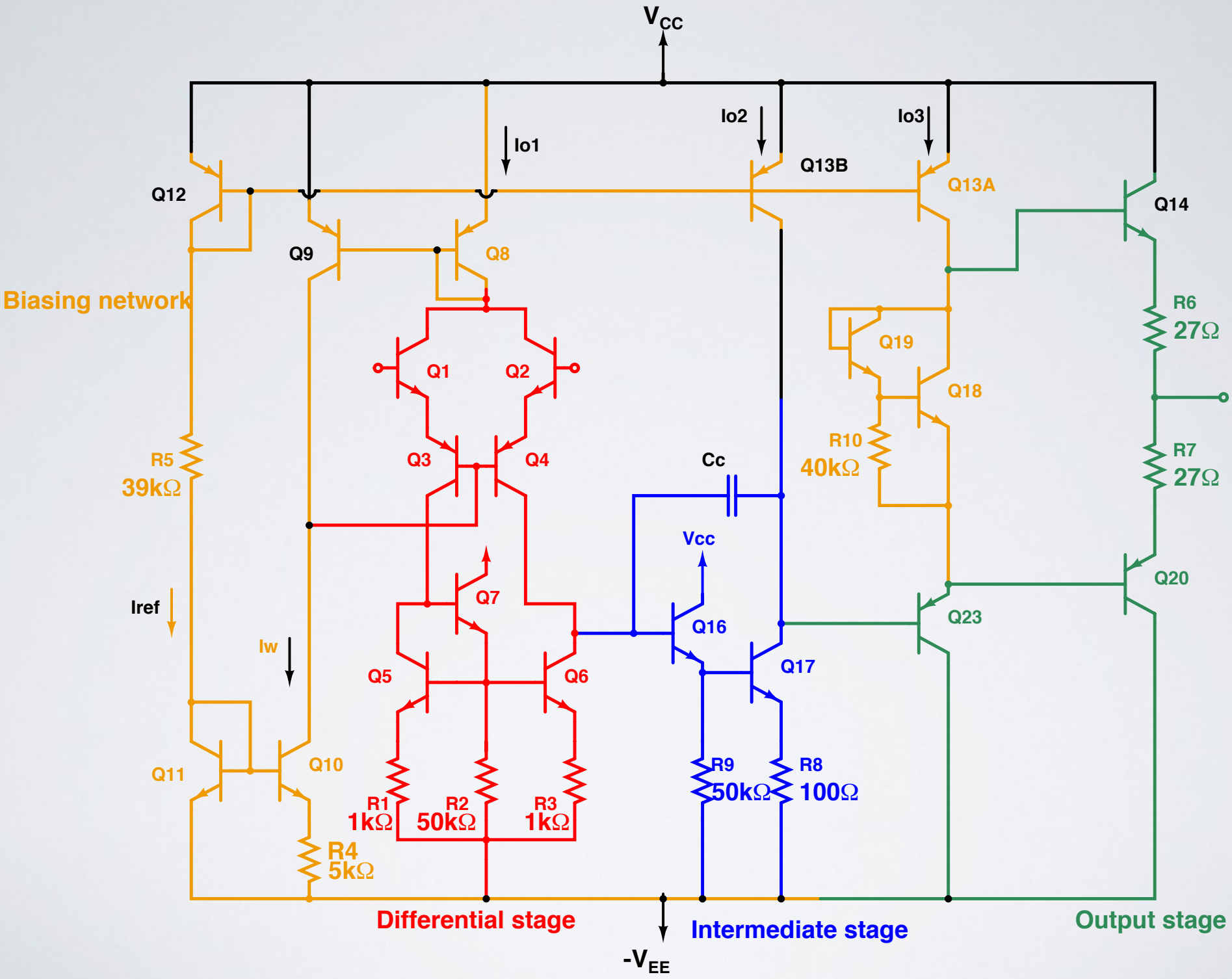
Assume: I_{ss} = ideal current source

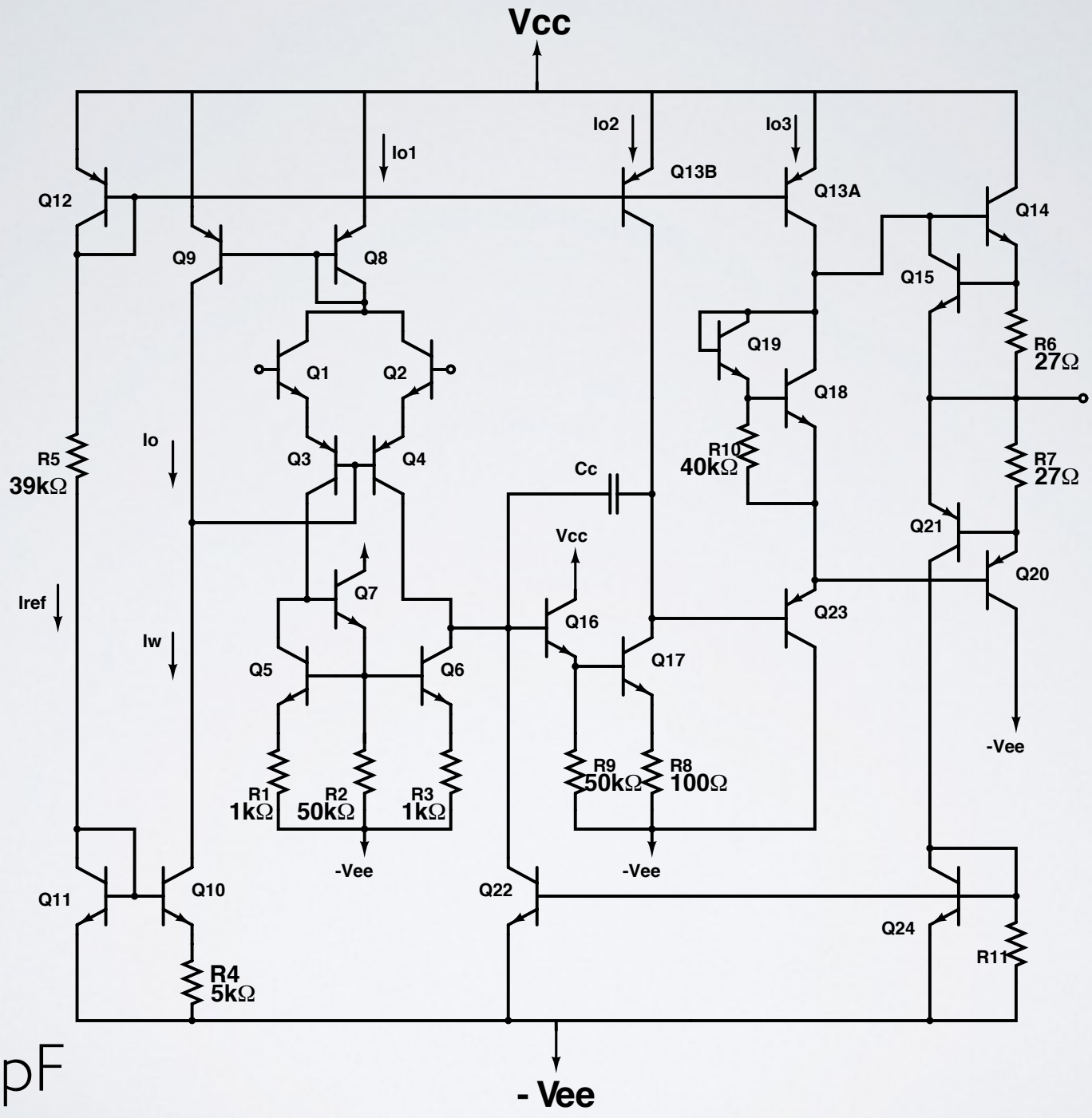




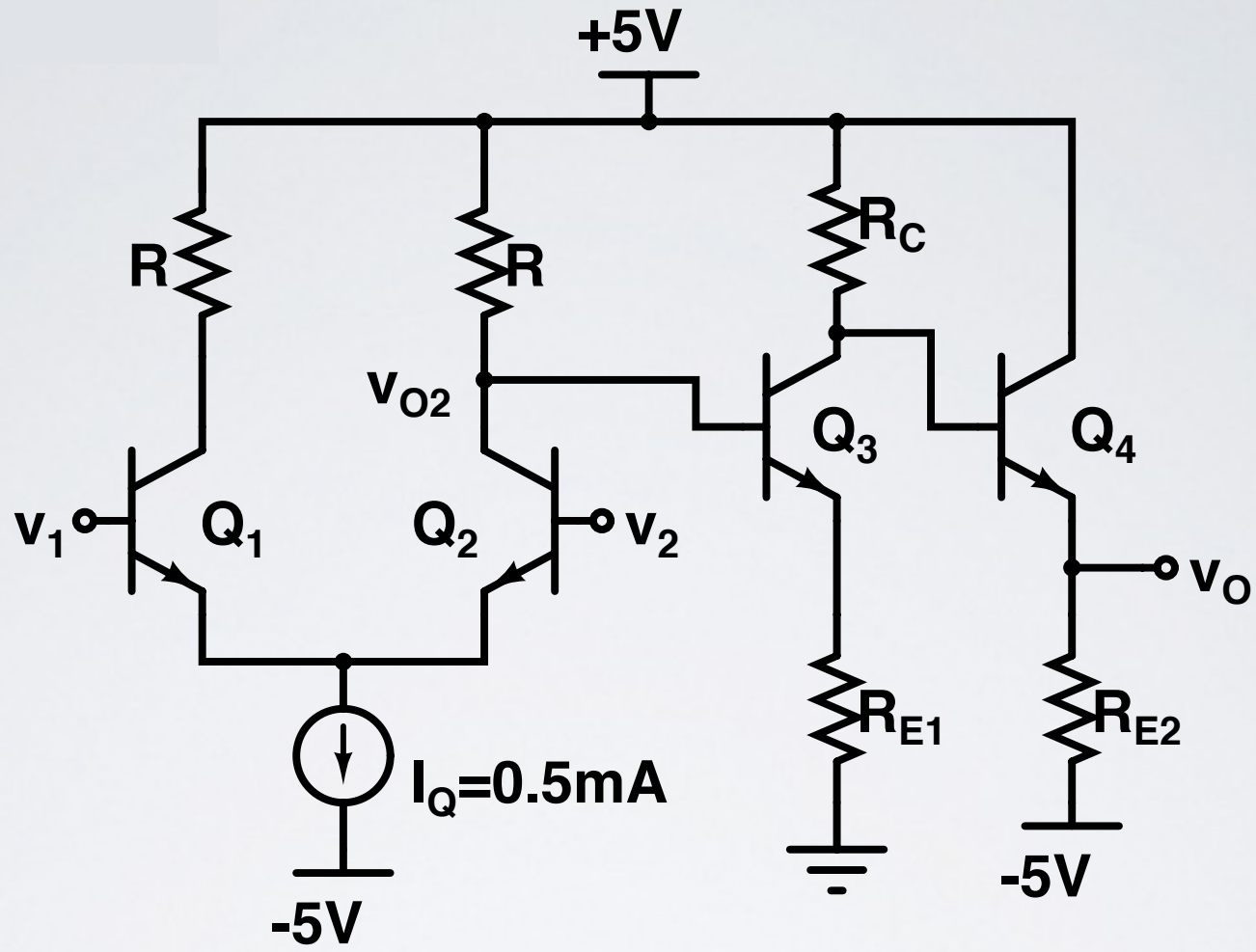
Example: I_{REF}=100uA, k_n'=80uA/V^2, K_p'=40uA/V^2,(W/L)=25, y $\lambda_n=\lambda_p=0.02V^{-1}$. Find voltage gain. (ANSWER: A_d=32000)

BJT OPAMPS & UA741


V_{CC}
Io1
Io2
Io3
Q12
Q9
Q8
Q13B
Q13A
Q14
Biasing network
Q1
Q2
Q3
Q4
Q19
Q18
R6
27Ω
R10
40kΩ
R7
27Ω
R5
39kΩ
Cc
Vcc
Iref
Iw
Q7
Q16
Q20
Q23
Q5
Q6
Q17
Q11
Q10
R9
50kΩ
R8
100Ω
R1
1kΩ
R2
50kΩ
R3
1kΩ
R4
5kΩ
Differential stage
Intermediate stage
Output stage
$-V_{EE}$


Vcc
Io1
Io2
Io3
Q12
Q13B
Q13A
Q14
Q9
Q8
Q15
Q1
Q2
Q19
R6
27Ω
Q18
Io
R5
39kΩ
Q3
Q4
R10
40kΩ
Cc
R7
27Ω
Vcc
Q21
Iref
Q7
Q16
Q20
Q23
Iw
Q5
Q6
Q17
-Vee
R9
50kΩ
R8
100Ω
R1
1kΩ
R2
50kΩ
R3
1kΩ
-Vee
-Vee
Q11
Q10
Q22
Q24
R11
R4
5kΩ
- Vee

C_C=30pF



Assume h_{FE}=100, V_{BE}=0.7V, V_A=∞, $R_{O(CS)}$ =100kΩ (a) For v_1=v_2=0V, design so that v_{O2}=2V, v_{C3}=3V, I_{CQ3}=0.5mA, I_{CQ4}=3mA; (b) Find A_{d1}=v_{O2}/v_d & A_d=v_O/v_d; c) Find A_{cm1}=v_{o2}/v_{cm} and A_{cm}=v_O/v_{cm}, and the overall CMRR

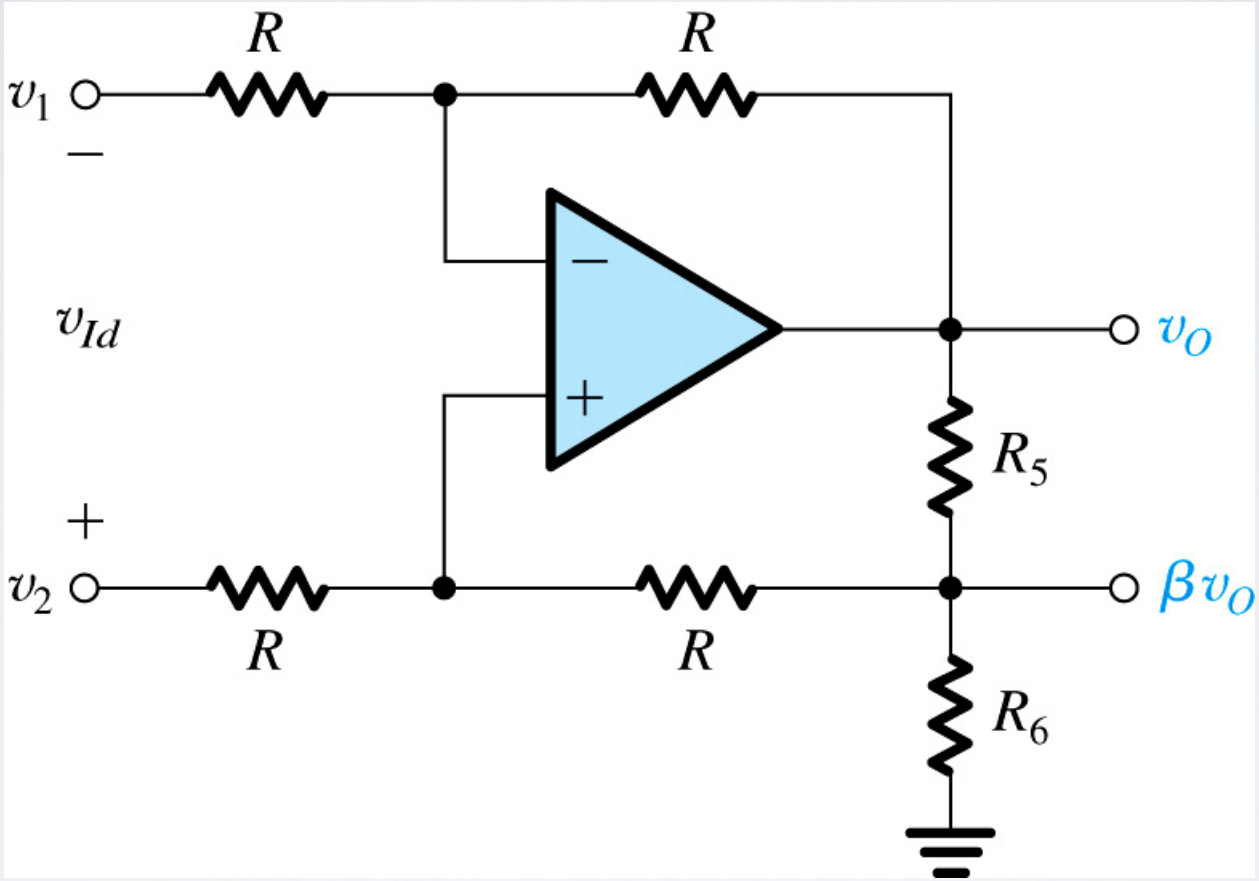
**2.69 To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. P2.69 employs positive feedback, in addition to the negative feedback provided by the resistor R connected from the output to the negative input of the op amp. Specifically, a voltage divider (R_5, R_6) connected across the output feeds a fraction β of the output, that is, a voltage βv_O back to the positive-input terminal of the op amp through a resistor R. Assume that R_5 and R_6 are much smaller than R so that the current through R is much lower than the current in the voltage divider, with the result that $\beta \simeq R_6/(R_5 + R_6)$. Show that the differential gain is given by

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{1}{1-\beta}$$

(*Hint:* Use superposition.)

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of 2 MΩ. Select values for R, R_5, and R_6, such that $(R_5 + R_6) \leq R/100$.

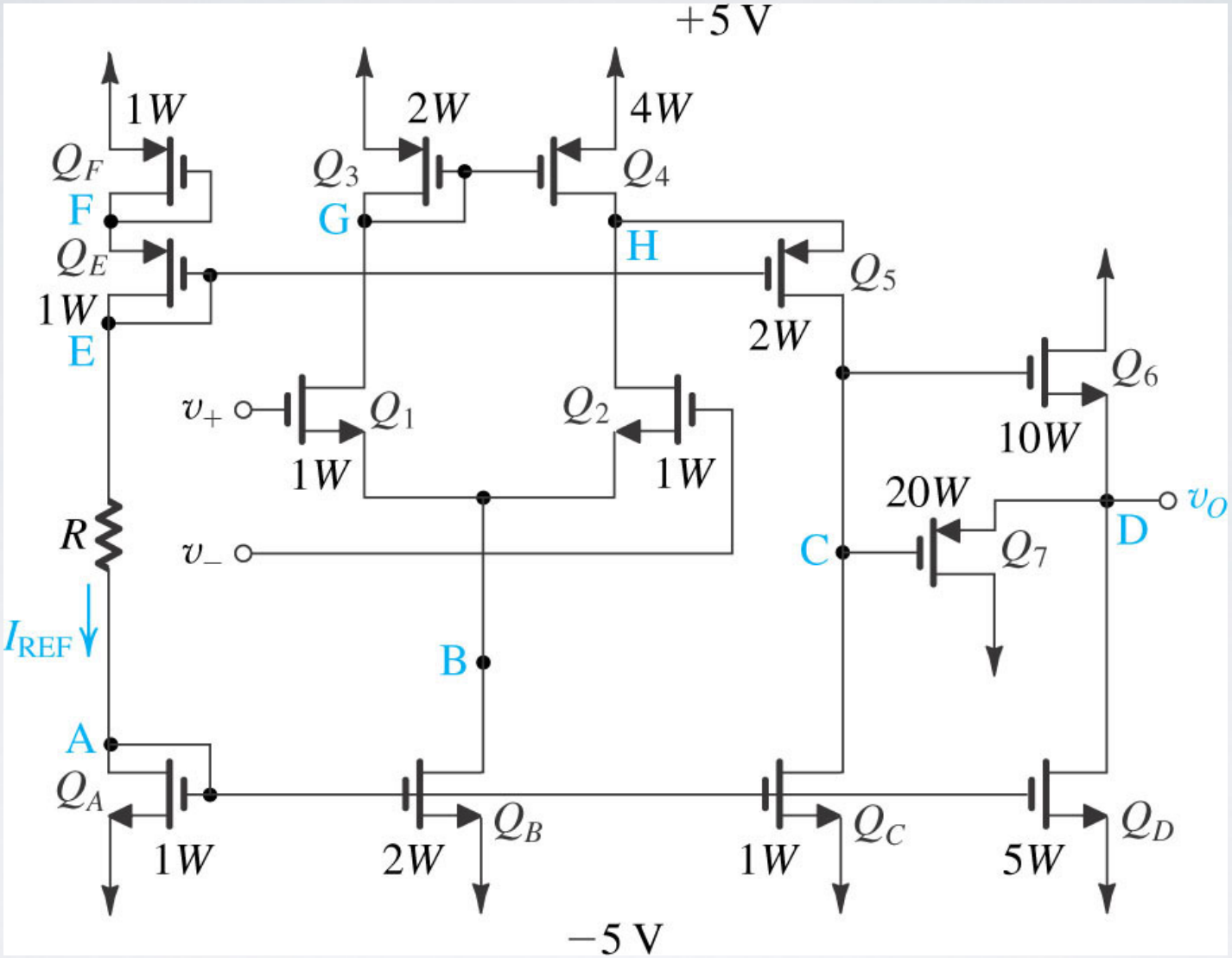
P2.69



D ***8.121 In the CMOS op amp shown in Fig. P8.121, all MOS devices have $|V_t| = 1$ V, $\mu_n C_{ox} = 2\mu_p C_{ox} = 40\ \mu A/V^2$, $|V_A| = 50$ V, and $L = 5\ \mu m$. Device widths are indicated on the diagram as multiples of W, where $W = 5\ \mu m$.

(a) Design R to provide a 10-μA reference current.
(b) Assuming $v_O = 0$ V, as established by external feedback, perform a bias analysis, finding all the labeled node voltages, V_{GS} and I_D for all transistors.
(c) Provide in table form I_D, V_{GS}, g_m, and r_o for all devices.
(d) Calculate the voltage gain $v_o/(v_+ - v_-)$, the input resistance, and the output resistance.
(e) What is the input common-mode range?
(f) What is the output signal range for no load?
(g) For what load resistance connected to ground is the output negative voltage limited to −1 V before Q_7 begins to conduct?
(h) For a load resistance one-tenth of that found in (g), what is the output signal swing?

P8.121


+5 V
1W
2W
4W
Q_F
Q_3
Q_4
F
G
H
Q_E
Q_5
1W
2W
E
Q_6
v_+
Q_1
Q_2
10W
1W
1W
20W
v_O
R
v_-
C
Q_7
D
I_{REF}
B
A
Q_A
Q_B
Q_C
Q_D
1W
2W
1W
5W
−5 V

D *12.63 Figure P12.63 shows a circuit suitable for op-amp applications. For all transistors $\beta = 100$, $V_{BE} = 0.7$ V, and $r_o = \infty$.

(a) For inputs grounded and output held at 0 V (by negative feedback) find the collector currents of all transistors. Neglect base currents.

(b) Calculate the input resistance.

(c) Calculate the gain of the amplifier with a load of 5 kΩ

(d) With load as in (c) calculate the value of the capacitor C required for a 3-dB frequency of 100 Hz.

P12.63