REVISED COURSE STRUCTURE

B.Tech. (Computer Science & Engineering)

(6 Semesters)

FIRST SEMESTER					
THEORETICAL		**L**	**T**	**P**	**C**
CSEB101	COMPUTATIONAL MATHEMATICS -I	2	1	0	3
CSEB102	BASIC ELECTRONICS	2	0	0	2
CSEB103	DATA STRUCTURE	3	1	0	4
CSEB104	COMMUNICATION SKILL	2	0	0	2
CSEB105	SYSTEMS PROGRAMMING	2	1	0	3
CSEB106	DIGITAL LOGIC	2	1	0	3
PRACTICAL					
CSEB107(P)	GROUP A: ENGINEERING DRAWING & WORKSHOP	0	0	3	2
CSEB108(P)	GROUP B: SYSTEM PROGRAMMING LABORATORY	0	0	2	2
CSEB108(P)	BASIC ELECTRONICS LABORATORY	0	0	3	2
CSEB109(P)	DATA STRUCTURE LABORATORY	0	0	3	2
CSEB110(P)	DIGITAL LOGIC LABORATORY	0	0	3	2
					27
SECOND SEMESTER					
THEORETICAL					
CSEB201	COMPUTATIONAL MATHEMATICS - II	2	1	0	3
CSEB202	COMPUTER ORGANIZATION	2	1	0	3
CSEB203	DATA COMMUNICATIONS	2	1	0	3
CSEB204	OPERATING SYSTEMS	3	1	0	4
CSEB205	MICROPROCESSOR & MICROCONTROLLER	2	1	0	3
CSEB206	FORMAL LANGUAGE & AUTOMATA THEORY	2	1	0	3
PRACTICAL					
CSEB207(P)	OPERATING SYSTEM LABORATORY	0	0	3	2
CSEB208(P)	MICROPROCESSOR LABORATORY	0	0	3	2
CSEB209(P)	DATA COMMUNICATIONS LABORATORY	0	0	3	2
CSEB210(P)	SOFTWARE LABORATORY	0	0	3	2
					27
THIRD SEMESTER					
THEORETICAL					
CSEB301	SOFTWARE ENGINEERING –I	3	1	0	4
CSEB302	COMPUTER ARCHITECTURE	3	1	0	4
CSEB303	COMPILER DESIGN	2	1	0	3
CSEB304	DESIGN & ANALYSIS OF ALGORITHMS	3	1	0	4
CSEB305	DATABASE MANAGEMENT SYSTEMS	3	1	0	4
CSEB306	OBJECT ORIENTED SYSTEM	2	1	0	3
PRACTICAL					
CSEB307(P)	SOFTWARE ENGINEERING LABORATORY	0	0	3	2
CSEB308(P)	SYSTEM DESIGN LABORATORY	0	0	3	2
CSEB309(P)	OBJECT ORIENTED SYSTEM LABORATORY	0	0	3	2
CSEB310(P)	DATABASE MANAGEMENT SYSTEMS	0	0	3	2
					30

FOURTH SEMESTER					
THEORETICAL					
CSEB401	SOFTWARE ENGINEERING II	3	1	0	4
CSEB402	COMPUTER NETWORKS	3	1	0	4
CSEB403	ARTIFICIAL INTELLIGENCE	2	1	0	3
CSEB404	OPTIMIZATION TECHNIQUES	2	1	0	3
CSEB405	COMPUTER GRAPHICS	3	0	0	3
CSEB406	ECONOMICS	2	0	0	2
PRACTICAL					
CSEB407(P)	SOFTWARE ENGINEERING LABORATORY - II	0	0	3	2
CSEB408(P)	COMPUTER NETWORKS LABORATORY	0	0	3	2
CSEB409(P)	ARTIFICIAL INTELLIGENCE LABORATORY	0	0	3	2
CSEB410(P)	COMPUTER GRAPHICS LABORATORY	0	0	3	2
					27
FIFTH SEMESTER					
THEORETICAL					
CSEB501	BUSINESS PROCESS LOGIC	2	0	0	2
CSEB502	MULTIMEDIA TECHNOLOGY	2	0	0	2
CSEB503	INTERNET TECHNOLOGY	3	0	0	3
CSEB504	VLSI TECHNOLOGY	3	1	0	4
CSEB505	SOFT COMPUTING	3	1	0	4
CSEB506	ELECTIVE –I	3	0	0	3
PRACTICAL					
CSEB507(P)	MULTIMEDIA TECHNOLOGY LABORATORY	0	0	3	2
CSEB508(P)	INTERNET TECHNOLOGY LABORATORY	0	0	6	4
CSEB509(P)	SOFT COMPUTING LABORATORY	0	0	3	2
CSEB510(P)	TERM PAPER –I	0	2	0	2
					26
SIXTH SEMESTER					
THEORETICAL					
CSEB601	INDUSTRIAL MANAGEMENT	2	0	0	2
CSEB602	DIGITAL SIGNAL PROCESSING	3	1	0	4
CSEB603	ELECTIVE-II	3	0	0	3
CSEB604	ELECTIVE-III	3	0	0	3
PRACTICAL					
CSEB605(P)	TERM PAPER-II	0	2	0	2
CSEB606(P)	GENERAL VIVA	0	2	0	2
CSEB607(P)	PROJECT WORK	0	0	16	8
					24

Set of Elective Papers: (B.Tech.)

Elective-I:

1. Distributed Systems
2. Cryptography
3. Fuzzy Systems
4. Principles of Programming Language

Elective –III:

1. Parallel Computing
2. Cognitive Computing
3. Information Security
4. Computational Geometry

Elective-II:

1. Embedded System
2. Coding & Information Theory
3. Neural Networks
4. Modeling and Simulation

REGULATIONS 3-YEAR (6-SEMESTER) B.TECH.
COURSE
IN
COMPUTER SCIENCE & ENGINEERING
UNIVERSITY OF CALCUTTA

1.	The minimum qualification for 3-year B. Tech. Course in Computer Science & Engineering of Calcutta University is a 3-year B.Sc. degree (with Honours in Physics / Mathematics / Statistics / Computer Science) of Calcutta University or an equivalent degree.
2.	The duration of the Course will be divided into 6 Semesters each of 6 months duration and the total credit of the examination for the B.Tech. degree in Computer Science and Engineering would be as follows:-

Examination	**Duration**	**Total Credits**
B.Tech. Semester-I	6 months	27
B.Tech. Semester-II	6 months	27
B.Tech. Semester-III	6 months	30
B.Tech. Semester-IV	6 months	27
B.Tech. Semester-V	6 months	27
B.Tech. Semester-VI	6 months	24

The schedule of papers and distribution of credits for the B.Tech. Semesters I, II, III, IV, V, & VI examinations in Computer Science and Engineering is given in Appendix-I .

3.	One credit theory paper means three lecture hours or two lecture-hours and one tutorial-hour or zero tutorial-hour per week while one practical paper means at least three compact hours in the laboratory per week. For project-work, there will be 16 contact-hours per week and for general , Term-paper-I and Term-paper-II, no contract hours will be provided.
4.	Each Theoretical/Practical paper and Tutorial will carry **"CREDIT"** according to the number of periods devoted per week as indicated in the following table.

Item	**No. of periods/week**	**Credit assigned**
Theoretical	**1**	**1**
Tutorial	**1**	**1**
Practical	**3**	**2**

5.	The number of lecture periods/week devoted to each Compulsory/Elective paper and Tutorial, and the Credit thereof will be determined from the Course Structure in conjunction with the Table in Item 4.
6.	The total credit to be earned to complete the B. Tech. course will be 161.

7. The examinations for the B. Tech. Course shall be held in 6 parts. At the end of each Semester, an examination of the Papers covered in that Semester will be held. This examination will be referred to as the **B.Tech. …Semester Examination** In any semester, the study break between the completion of regular classes and the commencement of the Semester Examination will generally be a maximum of 10 calendar days. The schedule of a Semester examination and the credit to be earned will be according to the course structure given below. A student earns the credit assigned to a Theoretical/Practical paper or to a Tutorial or to Term paper or to Project Work or to General Viva Voce, when he/she satisfies the performance criteria stated below in Item 9.

8.
a) Examination of a Theoretical paper carrying of 3 hour duration.
b) Paper Setters and Examiners for Theoretical papers will be appointed from a Board of Examiners consisting of all the faculty members .
c) Evaluation of performance in a Practical paper will be based on Sessional work in that paper and an end-semester viva voce. On completion of all the experiments in a Practical paper, a student will be given marks, out of notional full marks, according to the following divisions:

   i. 50% for experiments performed in the lab - the Sessional work to be evaluated by the Teacher under whom the laboratory will be assigned.
   ii. 40% for viva voce on the experiments to be conducted by a Board consisting of the Faculty members of the Department and/or External Examiner(s).
   iii. 10% for Lab Report to be evaluated by the Viva Voce Board.

d) Evaluation of performance in a Tutorial will be through assignments handed out by the Teacher concerned.
e) Evaluation of the performance in a Term paper will be evaluated by a board of examiners

9. (a) The performance of a student in a paper (Theoretical/ Practical), Tutorial, Project work and General Viva Voce will be evaluated in terms of **'Grades'**, and **'Grade Points'** earned by the student. The equivalence between 'Grade', 'Grade Point' and the Percent Marks (out of notional full marks) is tabulated below.

Percentage of Marks	Grade	Explanation	Grade-Point(P)
95-100	O	Outstanding	10
90-94	A	Excellent	9
80-89	B	Very Good	8
70-79	C	Good	7
60-69	D	Satisfactory	6
50-59	E	Fair	5
40-49	P	Poor	4
<40	F	Fail or Absent in any end-paper	0

Grade 'F' also implies failure to earn the corresponding credit. Grades higher than 'F' and Grade Points ≥4 indicate successful clearing of a unit that will earn the student the corresponding Grade Point (P) and the Credit (C) assigned to that unit.

(b) The overall performance of a candidate in a particular (j th, j=1,2,3,4,5,6) Semester examination, who earns all the credit of that Semester in one chance, will be assessed by the **Semester Grade Point Average (SGPA) 'S' to** be computed from

$$SGPA\left[S^{(j)}\right] = \frac{\sum_i P_i^{(j)} C_i^{(j)}}{\sum_i C_i^{(j)}} \qquad \textbf{(I)}$$

where the summations are over the Grade Points and Credit earned in the examination of the jth Semester. Cj may be the credit associated with a Theoretical or a Tutorial or a Practical paper or Project Work or General Viva

Voce and Pi would be the corresponding Grade Point earned. $\sum_i C_i^{(j)}$ is the total credit of the jth Semester and $\sum_i P_i^{(j)} C_i^{(j)}$ is the weighted sum of the Grade Points earned in the jth Semester.

(c) On completion of the B. Tech. course (when 161 credits have been earned as per regulations), the combined result of a candidate will be shown through the **Consolidated Grade Point Average(CGPA).**

CGPA will be computed from

$$CGPA = \frac{\sum_{J=1}^{6} s^{(J)}.c^{(J)}}{\sum_{J=1}^{6} c^{(J)}} = \frac{\sum_{J=1}^{6} s^{(J)}.c^{(J)}}{161} \qquad \textbf{(II)}$$

for a student who earns the total credit of the course in single chance (6 consecutive semesters without any back credit); and from

$$CGPA = \sum_K P_K C_K / 161 \qquad \textbf{(III)}$$

for a student who completes the B.Tech. course in 6 Semesters but with back credit or in more than 6 Semesters as per regulations, where P_K is the Grade Point earned in a unit carrying C_K credit and the summation is over all the Theoretical/Practical papers, Tutorials, Project Works and General Viva Voce of the B. Tech. course.

10.	(a) Each student will be allotted the topic of the Project Work at the beginning of the 5th Semester. He/She will have to carry out the Project Work under i) the supervision of a Faculty member of the Department Or ii) the joint supervision of more than one Faculty members of the Department Or iii) the joint supervision of one or more Faculty members of the Department and an External Supervisor belonging to another institution/organization. (b) At the end of the 6th Semester, a student will have to submit, through the respective Supervisor(s), a dissertation on the Project Work (Final) carrying 6 credit to a Board of Examiners consisting of the Faculty members of the Department, External Supervisor(s) and External Examiner(s). (c) For Project Work, 40% of the notional full marks will be set aside for the Sessional Works and 60% for the Viva Voce and the Report. (d) At the end of the 6th Semester, a student will have to appear at a General Viva Voce carrying 2 credit to be conducted by Boards of Examiners consisting of the Faculty members of the Department and External Examiner(s).
11.	(a) The 2nd to 6th Semester classes will begin immediately after the completion of the previous Semester Examinations. (b) A student who fails to earn the total credit of a Semester (1st to 4th) in the Semester examination, will be allowed to continue in the next semester, provided he/she earns at least 15 credit in the Semester examination. (c) A student who earns at least 15 credit in the 5-th-Semester examination will be allowed to continue in the 6-th Semester. (d) If a student earns less than 15 credit in a Semester examination (Semester 1-5), he/she will be deemed to have failed in that Semester examination. (e) In order to pass in the 6-th Semester examination, a student will have to earn the total 10 credit of the Semester in a single chance. (f) The due-to-earn or 'back' credit of a Semester will have to be earned during the examination of the next Semester . The candidate will have two such additional chances to earn the due credit.. (g) For a student who fails to earn the total credit of a Semester but gets promoted to the next Semester by virtue of earning at least 15 credit (clauses 1 l(b),(c)), it would be necessary that the total 'back' credit carried by the student at any stage does not exceed 15. If at the end of a Semester, the accumulated back credit of a student exceeds 15, the student will not be permitted to pursue the course further. (h) A student who fails in a Semester examination (clause 11(d)) will not be allowed to continue in the next Semester and will have to revert to the same Semester in the next academic session. i. In order to complete the B.Tech. course, a student will have to utilize all the allowed chances within 4 years or 4 consecutive academic sessions from the date of the first admission. ii. A student who fails to earn the total credit of the B.Tech. course within the allowed chances, will not be permitted to continue the course.
12.	At the end of each Semester examination , the University will publish lists of successful candidates as per this regulation.

13.	In order to be able to appear in a Semester examination, a candidate shall have to pursue a regular course of studies in the Semester and attend at least 65% of the total Theoretical (including Tutorial) and total Practical classes (including the supporting theoretical classes, if any) separately in the Semester. A candidate who fails to earn the total credit of a Semester but gets promoted to the next Semester by virtue of earning at least 20 credit (clauses 1 l(b),(c)), will not have to attend classes in the paper(s) corresponding to the back credit.

APPENDIX-I

REVISED (DETAILED) SYLLABUS FOR 3-YR. B.TECH. 6 SEMESTERS EACH OF 6 MONTHS DURATION IN COMPUTER SCIENCE & ENGINEERING --- UNIVERSITY OF CALCUTTA

B.Tech 1st Semester

Theoretical:

CSEB 101: COMPUTATIONAL MATHEMATICS – I (2L + 1T + 0P) (3 Cr) Full Marks-100

Set Theory : Set and subsets, Empty set and power set, Equality of sets, operations on sets Cartesian Product of sets, Relations ,Domain and Range of a Relation, Equivalence relation, Equivalence classes, Functions, Special type of Functions (Injective, Surjective and Bijective), Identity function, composite Functions, Invertible Functions, Groups, Semi Group and Monoid, Subgroup, More characterizations of a Group, Rings, Some Special classes of Ring, Subring, Algebra of Subrings, Ideals and quotient rings, Properties of integral domains, Fields, Field of Fractions.
Combinatories : Mathematical induction, Recurrence Relations, The Characteristic Polynomial, Generating Functions, The Principle of Inclusion-Exclusion, The Addition and Multiplication Rules, The Pigeon-Hole Principle, Permutations and Combinations.
Mathematical Logic : Propositions, Connectives, Truth Table, Propositional Equivalence, Logical Equivalence, Tautologies, Predicates and Quantifiers, Negations.
Linear Algebra : Characteristic Equations, Eigen Values and Eigen Vectors, Properties of Eigen Values, Cayley-Hamilton Theorem, Reduction to Diagonal form, Canonical forms.

CSEB102: BASIC ELECTRONICS (2L + 0T + 0P) (2Cr) Full Marks-100

Physics of Semiconductor Devices: Conductivity, mobility, carrier lifetime, E-B diagram, Fermi level, effective mass, classification of semiconductors,
P-N junction:Structure, operations and V-I characteristics built-in potential, forward and reverse biasing, different junction capacitances,different types of breakdown-Avalanche breakdown and Zener breakdown .
Bipolar Junction Transistors (BJTs): Structures, mode of operation, different methods of biasing, h-parameter analysis of transistors, amplifiers and oscillators circuit using BJTs,
Field Effect Transistors (FETs): Structures of JFET and MOSFET, V-I characteristics, equivalent circuits, CMOS, MOS capacitors,
Operational Amplifiers (Op-Amp): Basic building block, equivalent circuit, modes of operation,use of op-amp in inverting and non-invertible modes. gain-frequency response, use of op-amp in analog computation, 555 timer circuit and Schmitt trigger using op-amp,Design of astable and monostable multivibrator.
Multivibrator circuits : Monostable, bistable and astable and their applications.
Power Supply : Basic building block of a power supply, Regulated fixed and variable voltage supply, UPS, SMPS.Design of dc regulated power supply usin op-amp
Electronic Measuring Equipment: Analog & digital multimeters, Cathode Ray Oscilloscope (CRO), signal generators.

CSEB 103: DATA STRUCTURE **(3L + 1T + 0P) (3 Cr)** **Full Marks-100**

Data Structure and algorithm preliminaries: Definitions; Time and Space analysis of Algorithms; Time and space trade-off, Recursion,ADT
Array: Definitions of Arrays and Lists; Stacks; Queues; Strings; Row/Column major representation of Arrays; Sparse matrix.
Linked List: Singly linked list; circular linked list; doubly linked list, operations on linked list.
Stack: Push; Pop; Applications of Stack; stack representation using array and linked list.
Queue: Representation using array and linked list; Insertion and deletion operations; circular queue; priority queue.
Graph Algorithms: Representation and Traversal, Basic Algorithms Minimal Spanning Tree, Shortest Path, All pairs Shortest Path, Transitive Closer
Searching and Sorting Methods: Various Searching and Sorting algorithms with complexity analysis.
Tree: Definition; Generalised tree representation; Binary tree - definitions and properties; binary tree traversal algorithms with and without recursion.
Binary Search Tree - creation, insertion and deletion operations, Threaded tree (One way and Two way); AVL tree balancing; B-tree; Application of trees

CSEB 104: COMMUNICATION SKILL **(2L + 0T + 0P) (2 Cr)** **Full Marks-100**

Basic Skills Development using English as medium; Listening skill :narrations and descriptions,taking notes,appropriate response.Speaking: Intelligent and Fluent way of making statements,reporting events. Reading texts. Writing sentences. Creative articles. Translation skills. Preparation of Presentation materials. Reference to modern day technological terminologies. Grammar :Familiarity with different types of sentences Preposition and their uses.Familiarity with Tenses Familiarity with degrees of objectives – Positive, Comparative, Superlative.Familiarity withCommon English idioms and everyday expressions.Common English group verbs and everyday expressions.Agreement of the subject with the verb. Salutations: Good Morning, Good day, Good Evening etc. and Modes of Address: e.g., Sir, Madam, Your Excellency, Tour Honour, Your Grace etc.Expression of a composite subject in one word e.g., An 'Entrepreneur' is a person who starts or organizes some 'Business'.Correction of sentences.Conversation with –Bus driver, taxi drivers etc.,At a telephone booth, railway station, airport etc.With a shop-keeper or a Chemist.With a doctor or with officials in a Bank.Mock interview for a Job.Mock Interview. Overall Revision.

CSEB 105: SYSTEMS PROGRAMMING **(2L + 1T + 0P) (3 Cr)** **Full Marks-100**

System Hardware and Software :interaction
Language Issues : Types and levels of languages; Interpretation and Translation; Translation of Low Level Languages and High Level Languages.: Characteristicsand differences
Assemblers : Algorithm; Pseudo operations; Expressions.
Debuggers, Word Processors, Editors .
Tools : LEX and YACC/JavaCC
Macro Processors; Recursive and nested macros.
Linking and Loading
Compilers : introduction..

CSEB 106: DIGITAL LOGIC **(2L + 1T + 0P) (3 Cr)** **Full Marks-100**

Switching algebra and its applications, Boolean algebra vs. Switching algebra, Switching functions, Gate concepts, Minimization of switching functions, Universal logic module.
Synthesis and Analysis of Logic Circuits, Two level and multilevel realizations, Propagation delay, Noise margin and Power dissipation, Switch and Inverter as functionally complete elements, Gates. Registers and Processor level design of Digital Systems, Structure and behavior components, Finite state model for Sequential circuits. Flip Flops, Synthesis of Sequential machines, Counters and Registers, Decompositions, Unitness and Symmetric Boolean functions. Threshold functions, Logic families, Static and Dynamic memories, Flash memories, PLA and PROM.

PRACTICAL

CSEB107(P) GR-A : ENGINEERING DRAWING AND WORKSHOP ACTICE

(0L + 0T + 3P) (2 Cr)

Full Marks-50

Working on different machines. To be based on assignments. Use of AutoCAD.

CSEB107(P) GR-B : SYSTEM PROGRAMMING LAB (0L + 0T +2P) (2 Cr) Full Marks-50

Installation & Configuration of Operating Systems.
Design and implementation of Assemblers.
Text Editors,linkers
Use of Lex,YACC,JavaCC
Lexical Analyzers
Parsers

CSEB 108(P): BASIC ELECTRONICS LAB (0L + 0T + 3P) (3 cr) Full Marks-100

Clipping and Clamping circuits with diodes and transistors
Use of op amp as:
Inverting amplifier
Non-inverting amplifier
AC amplifier
Integrator And frequency response (Bode* Amplitude plot)
Elimination determination of frequency response
Regulated DC Voltage and current sources using op amps- regulation characteristics
with load.
Study of 555 timer chips and testing of
Astable multi-vibrator (Clock generator) (ii) monostable multi-vibrator.

CSEB 109: DATA STRUCTURE LAB (0L + 0T + 3P) (2 Cr) Full Marks-100

Programming with C: Fundamentals of C programming, control statements, array and pointers, functions, scope of variables, parameter passing, structures, union, files.
General assignments on C programming language before the students start their work on Data Structure.
Assignments on developing programs and functions related to the theoretical paper coverage on Data Structures.
Separate class/tutorial hours should be included for teaching.

CSEB110: DIGITAL LAB (0L + 0T + 3P) (2 Cr) Full Marks-100

Prerequisites
Documentations Standards, Transfers characteristics, Universal Gate set operations, concept of propagation delay, Fan in, Fan out, Noise margin.
Digital System
Combinational Logic Design Practices
Decoder, Cascading, VHDL, Seven Segment Decoder.
Encoders – priority encoder and keyboard displays, encoders in VHDL.
Three State devices – standard SSI and MSI. Buffers 74125, 74126 and 74541.
Multiplexers – standard MSI Multiplexer, expanding Multiplexer, MUX as Universal logic module, VHDL description.
Exclusive OR gates and Priority circuits, the 74280 9 bit priority generator.
Comparator Iterative circuits standard MSI comparator.
Adder, Subtractor, and ALU.
Multiplication by repeated addition shift and all multiplication.
Sequential Logic Design Examples
Latches an Flip flops.
Counters universal 74193.
Shift Registers universal 74194
Simulation: Multisym, PSpice and other simulator available are to be used for chip level simulation.

B-Tech 2nd Semester

CSEB 201: COMPUTATIONAL MATHEMATICS II (2L + 1T + 0P) (3 Cr) Full Marks – 100

Probability and Statistics- Mean, Median, Mode, Standard deviation, Sample Space & Events, Conditional Probabilities and Expectations, Independent Events, Baye's Formula, Discrete and Continuous Random Variables, Expectation of a Random Variable (Both Discrete & Continuous case), Independent Random Variables, Correlation and Regression, Distribution (Binomial, Poisson, Normal, Exponential, Uniform, Gamma, Geometric), Limit Theorem, Strong Law of large Numbers, Central Limit Theorem, Stochastic Processes, Markov (Chains & Processes), Poisson Process, Counting Processes, Birth & Death Process, Queuing Theory and application to Performance evaluation and modeling.
Transforms- Fourier Transforms, Laplace Transforms, Z Transform.
Numerical Methods- Errors , Solution of Algebraic and Transcendental equations:, Solution of Linear simultaneous Equations, Numerical Integration, Interpolation, Solution of Differential Equations, Solution of Partial Differential Equations

CSEB202: COMPUTER ORGANIZATION (2L + 1T +0P) (3 Cr) Full Marks-100

CPU Organization:Fundamentals, Fixed and Floating point numbers, Instruction Set formats, modes, types and programming. Datapath Design Fixed and Floating point arithmetic. ALU pipeline programming. Control Design .Hardware control, Microprogramed control and Pipeline control.Memory Organization:Technology, RAM and SAM. Multilevel Memory, Virtual memory and Cache memory.System Organization:Bus control, Arbitration.,Program I/O, DMA and Interrupt I/O programming

CSEB 203: DATA COMMUNICATION (2L + 1T + 0P) (3 Cr) Full Marks-100

Introduction to communication systems, Data, signal and Transmission: Analog and Digital, Transmission modes, Transmission Impairments, Performance criteria of a communication system
Goals of computer Network, Networks: Classification, Components and Topology, Layered architecture of a Network software, OSI and TCP/IP model
Encoding: Line coding and Block coding, Error detection codes, Modulation: Digital to Analog and Analog to Analog conversion techniques
Bandwidth utilization techniques: Multiplexing: Frequency division, Time division and Wave division multiplexing, Spread spectrum concepts
Transmission Media: Guided and Unguided: Architecture, Transmission characteristics and application
Switched Networks: Circuit switching and Packet Switching, Circuit Switching principle and the Modems used in a Telephone network, Connection oriented and Connection-less approach in packet switching network
Information Theory: Measure of Information, Entropy, Discreate and Continious channel, Shannon's encoding algorithms

CSEB 204 :OPERATING SYSTEMS (3L+ 1T + 0P) (4Cr) Full Marks-100

Introduction- Role of OS, Evolution of OS, Structural Overview, Concept of Process, Threads, Process Control Block, Process Management & Scheduling, Hardware Requirements, Protection, Content switching, Privileged mode
Process Synchronization, Critical Section Problem, Hardware Mechanism for synchronization, Semaphores and Mutex objects, Classical Problems (producer consumer, dining philosophers etc),
Deadlocks and Detection, Prevention and Avoidance Mechanisms.
Memory Management, Virtual Memory - Dynamic Linking, Segmentation, Paging Protection, Demand paging, Page Replacement polices-Thrashing, Pre-paging and other issues, Swapping
File and Directories - File Organization in directories, File attributes, Operation on file, Directory attributes and operations on directories, File protections.
File System Implementation, Concepts of mounting, Allocation mechanisms, Contiguous, Linked and indexed allocations. Free Space management.
Device Drivers - Storage management, Disk Scheduling, Disk Management
Security and Protection Mechanism - Password based protection, Encryption and Decryption, System

Threats – Viruses, Wormholes, Trojan horses etc

CSEB 205 :MICROPROCESSOR & MICROCONTROLLER (2L + 1T + 0P) (3 Cr) Full Marks-100

Introduction to microprocessors and microcomputers: Function of microprocessors- architecture of 8086- pin configuration and functions – tristate bus concept - generation of control signals - bus timings – de-multiplexing – flags - memory decoding - interfacing of RAM and EPROM - I/O addressing - I/O mapped I/O - and memory mapped I/O schemes - instruction execution - fetch/execute cycle - instruction timings and operation status.
Memory organization - program memory - data memory - direct & indirect addressing area - Program status word - register banks - addressing modes - instruction set – arithmetic - logical and data transfer instructions - Boolean instructions - program branching instructions - Programming examples.
Machine cycles – interrupts - interrupt sources - interrupt enable register - interrupt priority - interrupt control system - interrupt handling - single step operation - port bit latches and buffers - port structures and operation - accessing external memory – programming examples.
Timer0 & Timer1 - TMOD SFR - mode0, mode1, mode2, mode3 - TCON SFR - serial interface - SCON SFR - mode0, mode1, mode2, mode3- block schematics- baud rates- power on reset circuit- ONCE mode- on chip oscillator- external program & data memory timing diagrams- I/O port timings – programming examples.
Microcontroller 8051 – Architecture - pin configurations - internal block schematic - PORT0, PORT1, PORT2, PORT3, idle & power down mode - power control register - program protection modes - flash programming & verification. I/O interfaces with microcontroller, Real Time Control Issues, Embedded Systems, Programming Examples

References

1. The 8051 Microcontroller: Muhammad Ali Mazidi, Pearson Education.
2. The 8051 Microcontroller: Kenneth J Ayala, Penram International
3. Microprocessors and Architecture: Ramesh S Goankar
4. Microcomputers and Microprocessors: John Uffenbeck, PHI

CSEB 206: FORMAL LANGUAGES AND AUTOMATA THEORY (2L +1T+0P) (3Cr)
Full Marks-100

Introduction and Review of Finite State Machines: Deterministic, Nondeterministic M/cs, Minimization of FSM, Inverse FSM.
Finite Automata (FA) & Regular Expression: Definition, Deterministic & Nondeterministic FA, FA null string, Regular Expression, Two way FA, Linear Bound Automata, Applications
Regular Set: Definition, Properties, Pumping Lemma, Decision Algorithm, Minimization
Grammar: Introduction, Definition, Different types, Derivation Tree, Different Normal Forms, Ambiguous Grammar and its implications, Chomsky hierarchy, Context Sensitive Languages, Different Classes of Languages, Deterministic Context Free Language and its Properties
Pushdown Automata: Definition, PDA and CFL, Acceptance of Strings, Alternative Forms of PDA
Turing Machine: Introduction, Turing Machine Model, Computable Languages & Function, Church's Hypothesis
Undecidability: Introduction, Recursive and Recursively Enumerable Languages, Recursive Function Theory and its Application

PRACTICAL

CSEB 207(P): OPERATING SYSTEM LAB (0L + 0T + 3P) (3 Cr) Full Marks-100

UNIX:-
File System, Utilities, Editor, Process, Communication, Filters, Shell Programming, System Administration.
C-Programming using UNIX System Calls relating File Structure, Process, Inter Process Communication.
DOS and Windows: Commands, Utilities and Tools.
Familiarities with SUN-Solaris: Commands and Utilities.

CSEB 208(P): MICROPROCESSOR LAB (0L + 0T + 3P) (3 Cr) Full Marks-100

Assembly language programming to explore instruction set of 8085 / 8086
Design and implementation of basic interface circuits
Programming of microcontroller 8051
Interfacing with 8051

CSEB 209(P): DATA COMMUNICATION LAB (0L + 0T + 3P) (3 Cr) Full Marks-100

Familiarity with Networking equipments, Setting up and configuration of a Network;
Experiments on communication- Encoding, modulation, multiplexing.

CSEB 210(P): SOFTWARE LABORATORY (0L + 0T + 3P) (3 Cr) Full Marks-100

Scripting and Front-end Languages
Familiarity with Editing, Presentation, Multimedia, Desktop Publishing Software with suitable application
System security concepts, configuration and implementation