The NEW CEVA-X Processors

Revolutionizing Baseband Design

www.ceva-dsp.com

The NEW CEVA-X Architecture Framework

The World's Most Efficient Processor Architecture for Baseband Applications

- Combines **Control** plane processing with advanced **DSP** capabilities
- Targets high-end baseband, MTC and connectivity modems
  - Leveraging on CEVA's long heritage in baseband, powered more than 6 billion handsets to-date, 1 in 3 handsets worldwide

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- CEVA-X4 first member of The NEW CEVA-X family – multi-RAT PHY control processor targeting 2G/3G/4G/5G modems
  - Scalable VLIW/SIMD architecture supports both fixed- and floating-point operations to deliver unmatched performance and power efficiency
  - Orchestrating the entire PHY system comprising of DSPs, coprocessors, accelerators and other hardware resources

2X
More DSP Horsepower*

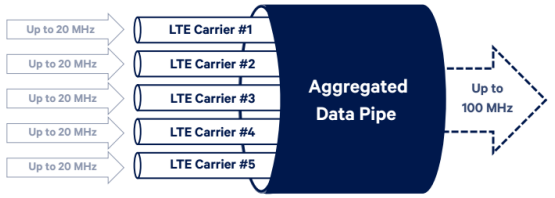
3X
More Control Performance*

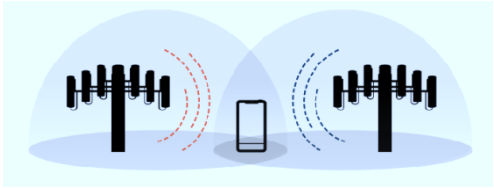
50%
Lower Power Consumption*

Addressing Wide Range of Baseband Applications

New Challenges in Baseband Design (1)

- Carrier Aggregation grows to increase capacity
  - 5 Carriers aggregation introduces huge modem control challenge
  - Need to execute measurements, calibration and other processing functions **per carrier**
- Dual-connectivity complexity
  - Handling dual-cells simultaneously
  - Increase complexity of the Rx control
- Merging Multi-RAT into one-single modem
  - Software solution to efficiently merge LTE-A, 3G, TD-SCDMA and 2G
  - Ultra-low Latency to move from one RAT to the other





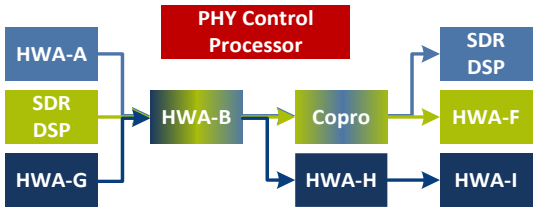
2G 3G

CHINA MOBILE TD-SCDMA

LTE Advanced Pro

New Challenges in Baseband Design (2)

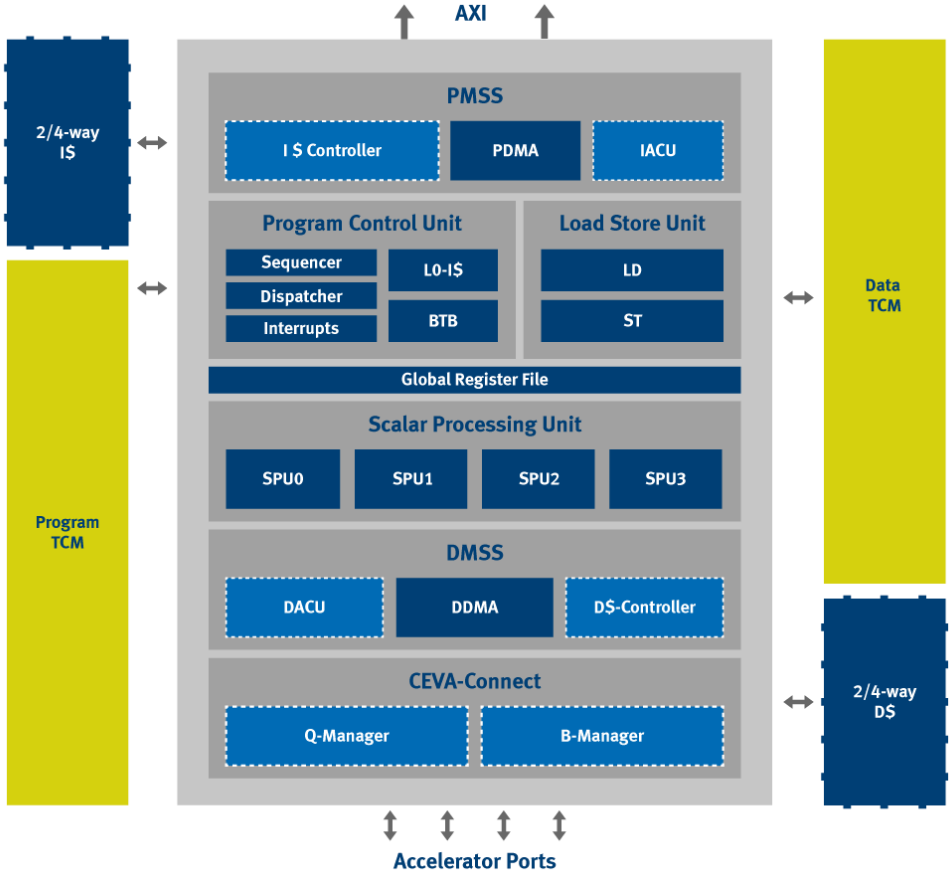
- Huge headache to orchestrate modem PHY
  - Real-time scheduling of many accelerators, processors and coprocessors
  - Requires sophisticated mechanisms to automatically sequence PHY components under ultra-low latency without overhead
- Voice processing complexity is growing significantly
  - VoLTE (EVS) complexity: 4-5X comparing to legacy codecs
  - Very strict power-consumption budget
  - Memory requirements are 10X compared to AMR
- Ultra-low energy modem design
  - Increase in complexity must meet competitive battery life
  - Special power-down mode required for modem idle phase



CEVA-X4 Introduction

- CEVA-X4 is the first derivative in The NEW CEVA-X Architecture Framework
- Designed for most advanced baseband architecture introduced in LTE Advanced Pro Rel13 supporting Multi-RAT
- Unique processor, solving the dual-requirements for powerful DSP and Control in a single solution
- Achieves 4.0 CoreMark/MHz
- Reaches 1.5GHz in 16nm

CEVA-X4 Architecture Diagram



CEVA-X4: Efficient Controller Capabilities

CEVA-X4 is equipped with high-end features to compete with best off-the-shelf controllers

- Up to 8 scalar operations in parallel
- Zero-latency ISA for optimal cycle count in serial code
- Comprehensive RTOS feature set
  - Ultra-fast context switch
  - Supervisor and User modes
  - Semaphores, etc..
- Dynamic branch prediction
  - Branch Target Buffer (BTB)
  - Branch history table
  - Return address stack
- Static branch prediction
- 32-bit HW support for division and multiplication

CEVA-X4: Powerful DSP Processing

- Eight 16x16 MAC
- Quad 32x32 MAC
- Native support for post-shift and saturation
- Large memory bandwidth 256-bit
- All C fixed-point data types supported: 8-bit / 16-bit / 32-bit / 64-bit
- Optional support for up to 4 Single-Precision FPU operations
- Dedicated ISA for important algorithms like FFT

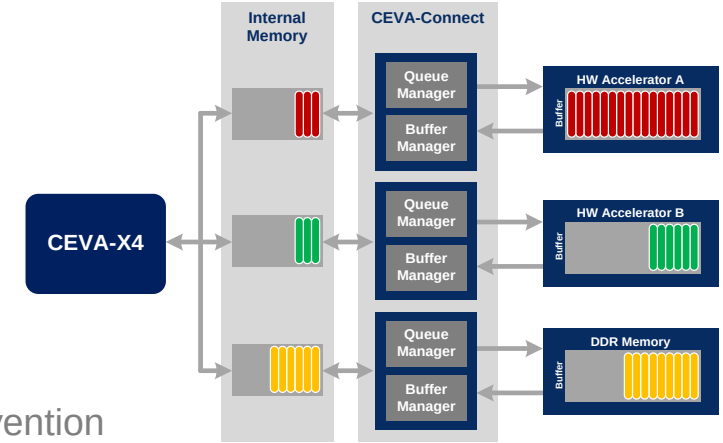
Features	Capacity
MAC32x32	4
MAC16x16	8
Shift operation 32/64	4
Arithmetic 32-bit (Add/Sub/etc..)	Eight 16-bit operations Four 32-bit operations Four 64-bit operations
Logical operation	
Accumulation types	

CEVA-X4: Orchestrating PHY Components

CEVA-Connect

CEVA X4

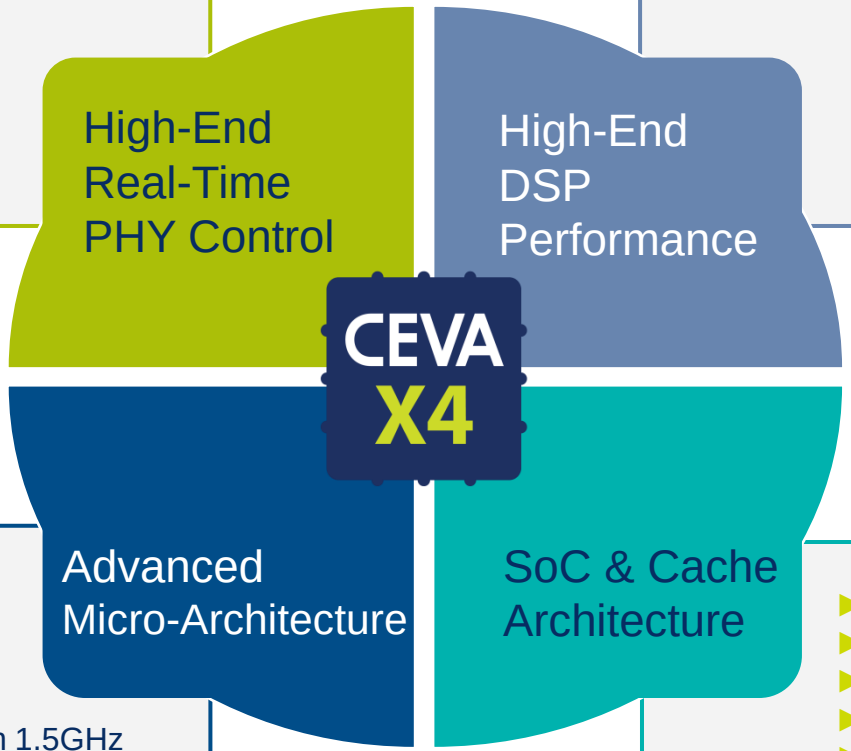
- Data transfers are performed automatically without DSP intervention
  - Saves DSP cycles
- Based on Queue Manager and Buffer Manager
  - Maintains multiple independent tasks queues
  - Dedicated activation interface with external HWA
  - Flexible priority and tasks queues to guarantee QoS
  - Dedicated accelerator ports
- Benefits
  - Data is automatically partitioned and fetched w/o DSP intervention
  - Saves DSP resources and efficiently manages the memory BW consumption
  - Manages flow control automatically



Putting It All Together

- Coremark/MHz: 4.0
- Advanced BTB
- RTOS Fully-Featured
- Ultra Fast Context Switch

- Eight MAC 16x16
- Quad MAC 32x32
- 128-bit SIMD
- 256-bit Memory Bandwidth
- Dedicated FFT Acceleration
- IEEE SP Floating Point



- Variable length pipeline
- Ultra Low Power with PSU
- High Memory Density
- High-speed Implementation 1.5GHz

- High QoS with Q-Managers
- Automatic Buffer Management
- Multiple HW Accelerator Ports
- Program & Data Cache
- TCM Memories

Thank You

For more information, visit http://launch.ceva-dsp.com/ceva-x

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