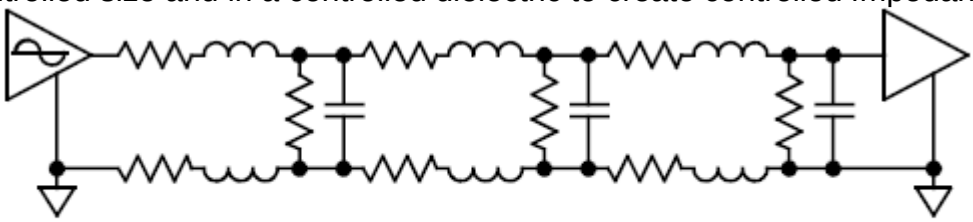
RF / Microwave PC Board
Design and Layout
Base Materials for High Speed, High Frequency PC Boards – Rick Hartley

http://www.qsl.net/va3iul/

RF / Microwave Design – Basics

- Unlike digital, analog signals can be at any voltage and current level (between their min & max), at any point in time.
- Standard analog signals are assumed to be between DC and a few hundreds of MHz.
- RF/Microwave signals are one frequency or a band of frequencies imposed on a very high frequency carrier.
- RF/Microwave Circuits are designed to pass signals within band of interest and filter energy outside that range.
- Signal band can be narrow or wide.
  - Narrow band circuits usually have pass band less than 1 MHz.
  - Broad band circuits pass a range of frequencies up to tens of MHz.
- When digital and microwave exist in the same unit, pass bands of microwave circuits usually fall (by design) outside the harmonic range of the digital signals.
- RF / Microwave PC Board layout simply follows the “Laws of Physics”-
- When laws of physics can’t be followed, know what compromises are available.
- Microwave signals are very sensitive to noise, ringing and reflections and must be treated with great care.
- Need complete impedance (Zo) matching (50 ohm out/ 50 ohm line/ 50 ohm in).
  - Minimizes Return Loss / VSWR.
- A Transmission Line is any pair or wires or conductors used to move energy from point A to point B, usually of controlled size and in a controlled dielectric to create controlled impedance (Zo).



Evenly Distributed R, L, G & C – $Zo=\sqrt{\frac{R}{G}+\frac{j\omega L}{j\omega C}}$

- Inductance (L) is determined by the loop function of signal and return path.
  - Small spacing (tight loop) creates high flux cancellation, hence low inductance.
- Capacitance (C) is function of signal spacing to the return path.
  - Small spacing creates high capacitance.
- Since small spacing (tight loop) creates low L & high C, and since:
  - Zo = √ L/C, small spacing creates low Zo.
- Additionally, Zo is function of signal conductor width & thickness and a function of the DK dielectric constant (Er) of the material surrounding the lines.
- Sometimes dielectric surrounding transmission line isn’t constant (outer layer trace on PCB).
  - DK above trace is Air (= 1.0008).
  - DK below trace is FR4 (approx = 4.1).
  - Effective Relative Er (Er_eff) is 3 to 3.25.
- Signal return currents follow the path of least impedance (in high frequency circuits that = path of least inductance).

- Whenever we neglect to provide a low impedance return path for RF / Microwave signals, they WILL find a path.
- It may NOT be what we had in mind.
- Signal Wavelength -
  - Wavelength (λ) of a signal is the distance it travels in the time of one cycle.
- For a signal traveling in free space -
  - λ = c (speed of light) / f (frequency), (λ = 11.78”/nsec at 1GHz = 11.78”)
- Signal in a higher dielectric - λ = *c* / [*f* •(1 / √Er)]
- Signal critical length
  - How long a PCB trace can be before we MUST pay attention to impedance control?
  - Function of frequency (1/16th wavelength)

$$L_{critical} = \frac{c}{f} \bullet \frac{1}{\sqrt{\varepsilon_{eff}}} \bullet \frac{1}{16}$$

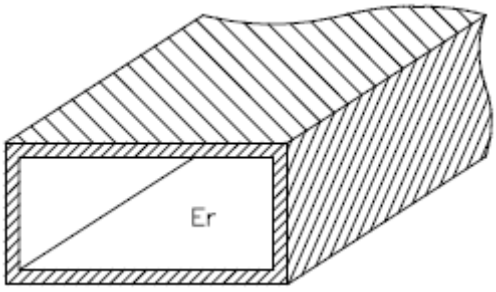
At 1 GHz = approx .425” (microstrip- FR4)
At 1 GHz = approx .375” (stripline - FR4)

Signal Loss / Noise

- Reflections -
  - Return Loss / VSWR
- Skin Effect -
  - Increased resistance of PCB trace due to decreased cross sectional area.
  - In analog circuits above 100 MHz.
  - Skin depth - 0.000822” @ 10 MHz and 0.000026” @ 10 GHz.
- Loss Tangent -
  - Dielectric Loss caused by molecular structure of board material.
  - In analog circuits above 200 MHz.
  - PTFE’s far better than FR4.
- Energy Coupling-
  - Cross Talk.
  - Noise Induction.

Line Types and Impedance (Zo)

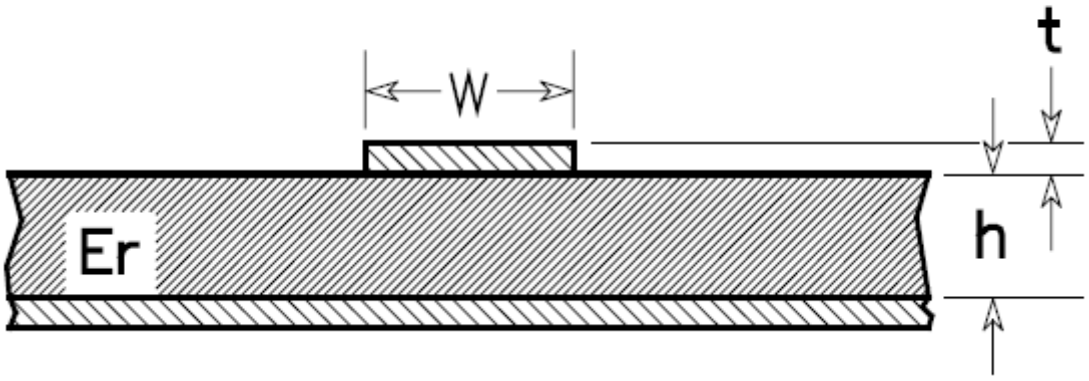
- Waveguide



  - Uses air as transmission medium and side walls of tube as return path.
  - Won’t support energy propagation below cutoff frequency.
  - Works best at ultra high frequencies with millimeter wavelengths.
  - With an air dielectric, signals propagate at the speed of light.
  - Very low loss due to smooth side walls and the air dielectric.
  - Ultra low loss with high density, ultra smooth coating on walls.
  - In very high power applications, uses solid dielectric to prevent voltage arcing.
- Signal traces longer than critical length (1/16 λ in DK) need impedance control to prevent return loss due to reflections.

- Shorter circuit elements don't require impedance control, but it usually does NO harm.
- Don't bother to Zo control, short lines if it will create a problem (ie- DFM – Design for Manufacturing).
- Impedance (L/C)-
  - Lower Er materials - net higher impedance traces and faster propagation times per given trace width & trace-to-ground separation.
  - As trace width increases, trace impedance decreases (thickness has min effect).
  - As trace spacing from ground increases, impedance increases.

Microstrip



$$Z_0 = \frac{120\pi}{2.0\sqrt{2.0}\pi\sqrt{\varepsilon_r + 1.0}} \ln\left\{1.0 + \frac{4.0h}{w'}\left[\frac{14.0 + 8.0/\varepsilon_r}{11.0}\frac{4.0h}{w'} + \sqrt{\left(\frac{14.0 + 8.0/\varepsilon_r}{11.0}\right)^2\left(\frac{4.0h}{w'}\right)^2 + \frac{1.0 + 1.0/\varepsilon_r}{2.0}\pi^2}\right]\right\}(\Omega)$$

where: $w' = w + \Delta w'$

$$\Delta w' = \Delta w\left(\frac{1.0 + 1.0/\varepsilon_r}{2.0}\right)$$

(Replace Er with Eeff)

$$\frac{\Delta w}{t} = \frac{1.0}{\pi}\ln\left[\frac{4e}{(t/h)^2 + \left(\frac{1/\pi}{w/t + 1.1}\right)^2}\right]$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \bullet \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \quad \text{if} \quad \frac{w}{h} < 1$$

otherwise

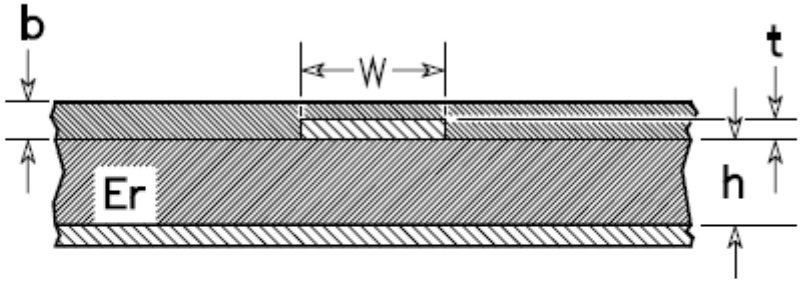
$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}} \bullet \frac{1}{\left(\frac{w}{h} + 1.393 + 0.677 \bullet \ln\left(\frac{w}{h} + 1.444\right)\right)}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.04\left(1 - \frac{w}{h}\right)^2\right] \quad \text{if} \quad \frac{w}{h} < 1$$

otherwise

$$\varepsilon_{eff} = \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}}\right]\right]$$

Embedded Microstrip

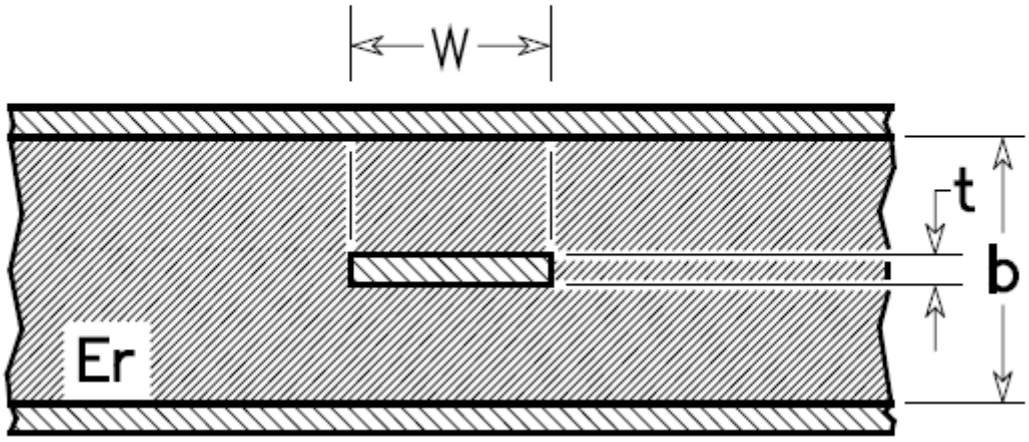


Multiply Zo (from Microstrip) by -

$$\frac{\varepsilon_{eff}}{\varepsilon_{eff} \cdot e^{(-2.0b/h)} + \varepsilon_r\left[1.0 - e^{(-2.0b/h)}\right]}$$

Can use w/Soldermask over Microstrip (Often NOT Needed)

Centered Stripline



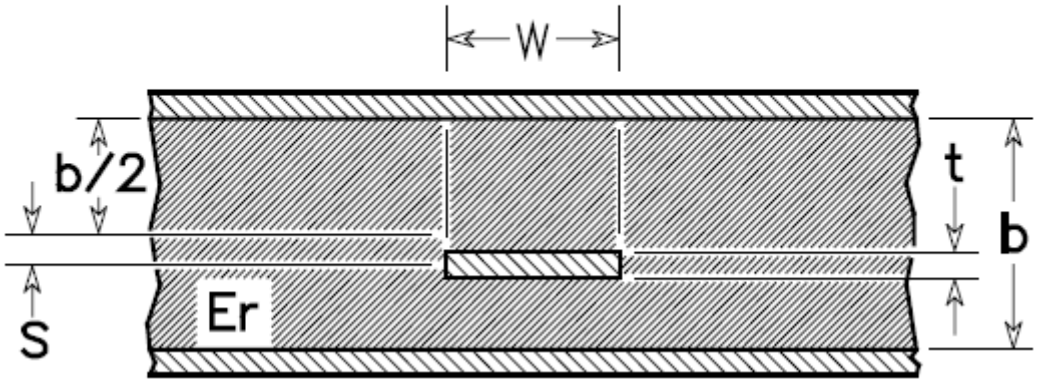
$$Z_0 = \frac{120\pi}{2.0\pi\sqrt{\varepsilon_r}} \ln\left\{1.0 + \frac{4.0(b-t)}{\pi w'}\left[\frac{8.0(b-t)}{\pi w'} + \sqrt{\left(\frac{8.0(b-t)}{\pi w'}\right)^2 + 6.27}\right]\right\}$$

where: $b = 2.0h + t$

$$w' = w + \frac{\Delta w}{t}t$$

$$\frac{\Delta w}{t} = \frac{1.0}{\pi}\ln\left[\frac{e}{\sqrt{\left(\frac{1}{2.0(b-t)/t+1}\right)^2 + \left(\frac{.25\pi}{w/t+1.1}\right)^m}}\right]$$

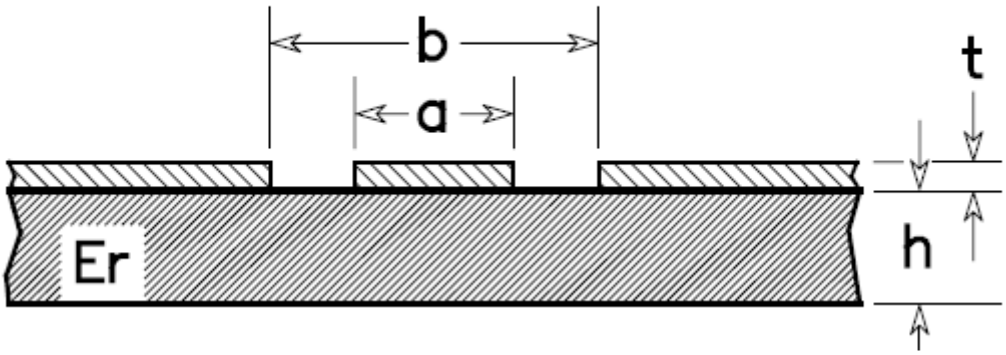
Off-Center Stripline



Microstrip verses Stripline

- Microstrip has lower loss-tangent problem.
- Microstrip has faster propagation time.
- Stripline has better immunity to crosstalk.
- Stripline has better EMI characteristics.

Coplanar Waveguide



- ‘b’ should be less than λ/2 for best performance.
- Ground must extend greater than 5x‘b’ on either side of trace ‘a’.
- Lower loss-tangent than Microstrip (signals couple mostly through air).
- Higher skin-effect losses (fields concentrate on edges of trace and grounds).

- May need to strap grounds together on either side of trace, every 1/20th wavelength.
- Only need one side of board to be accessible.
- No plated holes needed,
- Can narrow trace to match component leads.
- CPW allows variation of trace width, or spacing-to-ground or dielectric thickness to control Zo.
- Zo of CPW decreases as dielectric thickness increases.
- CPW produces smaller trace per given Zo than Microstrip.

$$Z_0 = \frac{30.0\pi}{\sqrt{\varepsilon_{eff,t}}} \bullet \frac{K(kt')}{K(kt)}$$

$$k1 = \frac{\sinh\left(\frac{\pi a_t}{4.0h}\right)}{\sinh\left(\frac{\pi b_t}{4.0h}\right)}$$

$$\varepsilon_{eff,t} = \varepsilon_{eff} - \frac{\varepsilon_{eff} - 1.0}{\frac{(b-a)/2.0}{0.7t} \bullet \frac{K(k)}{K'(k)} + 1.0}$$

$$k1' = \sqrt{1.0 - k1^2}$$

$$\varepsilon_{eff} = 1.0 + \frac{\varepsilon_r - 1.0}{2.0} \bullet \frac{K(k')K(k1)}{K(k)K(k1')}$$

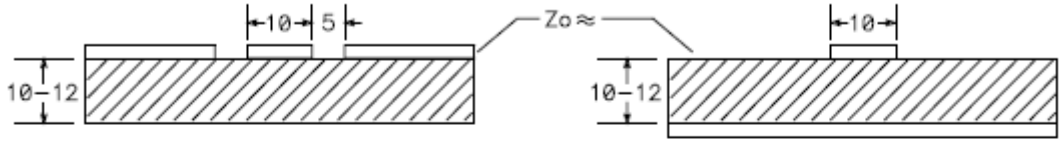
$$a_t = a + \frac{1.25t}{\pi}\left[1.0 + \ln\left(\frac{4.0\pi a}{t}\right)\right]$$

$$k_t = \frac{a_t}{b_t} \qquad k = \frac{a}{b}$$

$$b_t = b - \frac{1.25t}{\pi}\left[1.0 + \ln\left(\frac{4.0\pi a}{t}\right)\right]$$

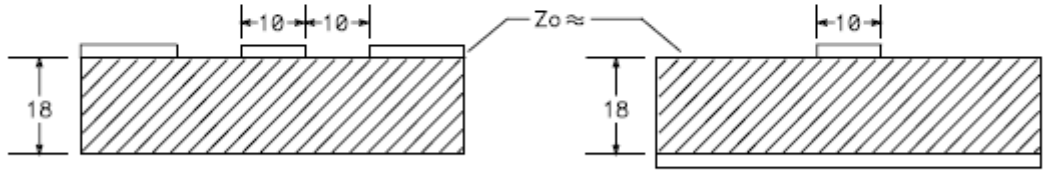
$$k_t' = \sqrt{1.0 - k_t^2} \qquad k' = \sqrt{1.0 - k^2}$$

CPW verses Microstrip



$\varepsilon_r = 4.2$ - Zo = 76 (ε_{eff} = 2.44 (CPW) & 3.02 (MS))

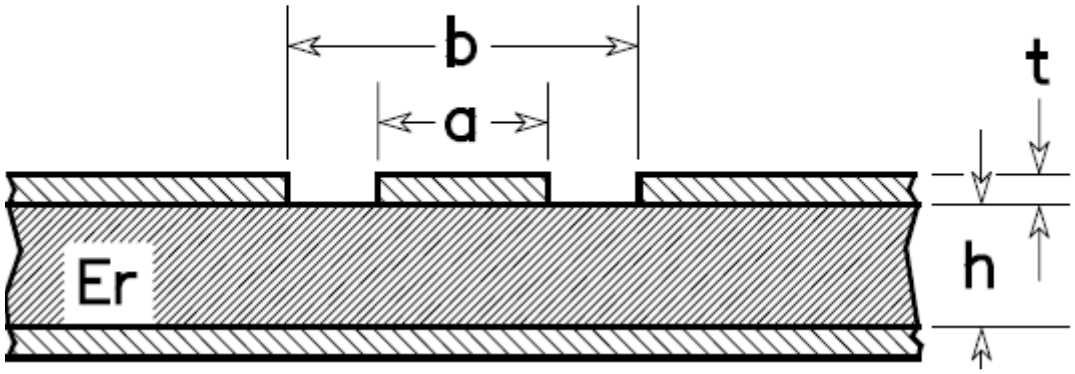
$\varepsilon_r = 2.5$ - Zo = 94 (ε_{eff} = 1.66 (CPW) & 1.96 (MS))



$\varepsilon_r = 4.2$ - Zo = 94 (ε_{eff} = 2.45 (CPW) & 2.95 (MS))

$\varepsilon_r = 2.5$ - Zo = 115 (ε_{eff} = 1.68 (CPW) & 1.92 (MS))

Coplanar Waveguide w/Ground



- In Reality, Microstrip transmission line in the RF / Microwave arena is CPWG.

$$Z_0 = \frac{120\pi}{2.0\sqrt{\varepsilon_{eff}}} \bullet \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k1)}{K(k1')}}$$

$$k = a/b$$

$$k' = \sqrt{1.0 - k^2}$$

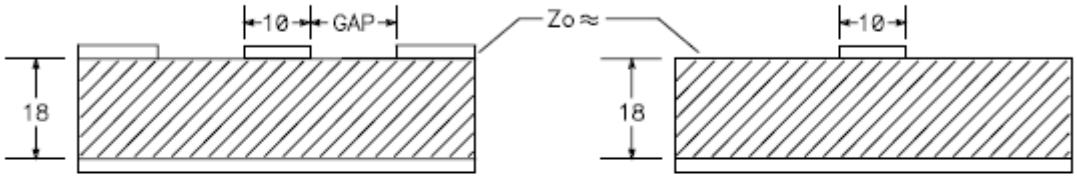
$$k1' = \sqrt{1.0 - k1^2}$$

$$\varepsilon_{eff} = \frac{1.0 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k1)}{K(k1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k1)}{K(k1')}}$$

$$k1 = \frac{\tanh\left(\frac{\pi a}{4.0h}\right)}{\tanh\left(\frac{\pi b}{4.0h}\right)}$$

- To avoid Microstrip mode, h >b and left & right ground extend away from ‘a’ by more than ‘b’.
- Zo of CPWG is increased as dielectric thickness increases. Opposite of CPW.
- If ‘ h’ is large, CPW and CPWG behave in similar fashion.

CPWG verses Microstrip



$\varepsilon_r = 4.2$ - Zo = 94 Ohms (At Gap = 30)

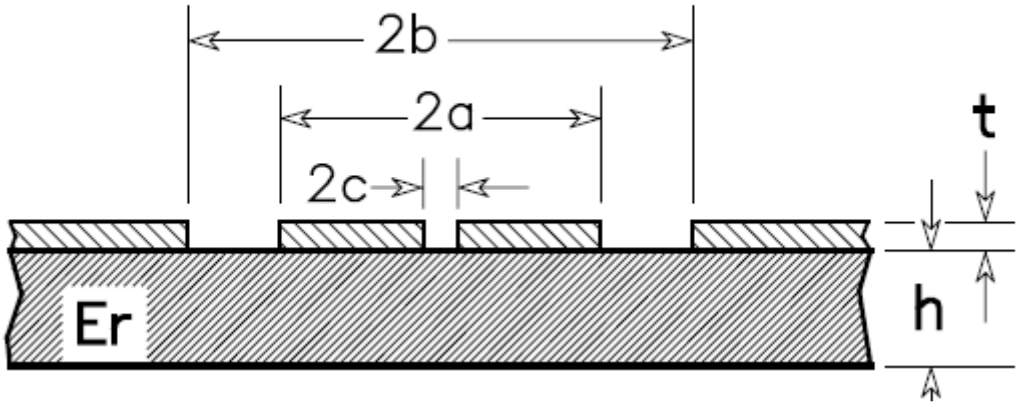
(ε_{eff} = 2.92 (CPWG) and 2.95 (MS))

$\varepsilon_r = 2.5$ - Zo = 115 Ohms (At Gap = 27)

(ε_{eff} = 1.89 (CPWG) & 1.92 (MS))

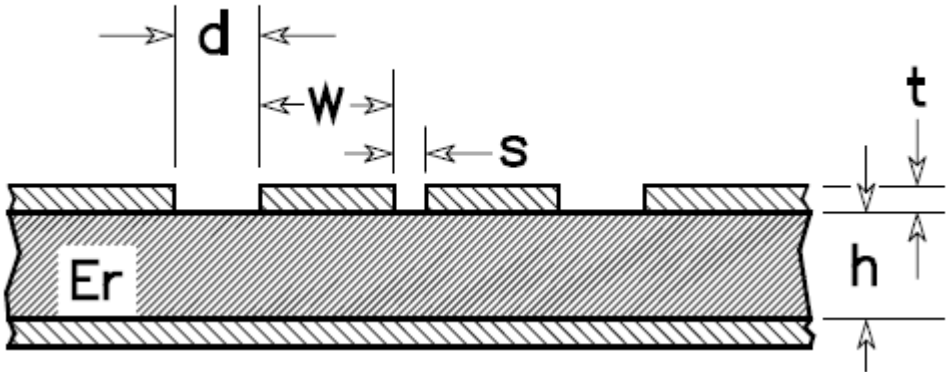
- Beyond gaps shown above, CPWG is like Microstrip.

Edge Coupled CPW (CP Differential Pair)



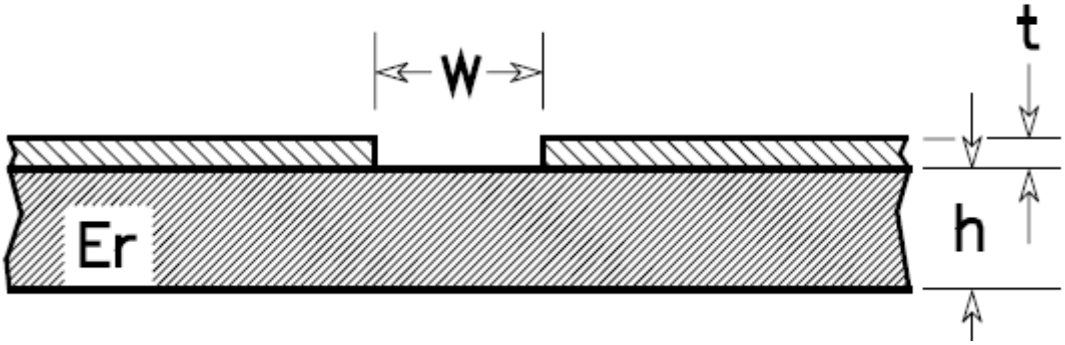
- Gives an extra degree of Signal-to-Noise isolation over standard CPW. (w/o plane, fields are large).

Edge Coupled CPWG (CP Diff Pair w/Grnd)



- Much better field containment than coupled CPW. Better yet in edge couple Stripline.

Slotline



- Acts like Waveguide with air dielectric.

Other Configurations

- 3 Line Coplanar Strip w & w/o Ground.
- Microstrip w/ limited width plane (and/or) limited width dielectric.
- Metal plate or shield covered CPW/CPWG.
- Metal plate or shield covered slotline.
- Offset CPW or CPWG.

Zo Calculations

- Use equations given or Wadell or Gupta.
- Use H.P. AppCAD (DOS and/or Windows).
- Use Rogers Corp. MWI (Dr R. Trout).
- Buy Field Solver (2D or 3D) Based Zo Calculator (i.e.- POLAR Ltd.)
- Don’t use Equations or Calcs for Dig Layout that Don’t Comp for Coplanar Effects.

Tpd, Capacitance and Inductance calculations (for all previous configurations)

$$Tpd = \sqrt{\varepsilon_{eff}} \ / \ c(\text{spd of light})$$

$$C = \ Tpd \ / \ Zo$$

$$L = \ Zo^2 \times C \ (\text{or } Tpd \times Zo)$$

Integral Components

- Components can be designed into the PC board utilizing the right configuration of lines and shapes to form-
  - Inductors
  - Capacitors
  - Couplers (similar to transformer)
  - Resistors (very small value)
  - Filters
- Capacitor formed by 2 copper plates separated by PCB dielectric (free component)

$$C = \ \varepsilon_r \times \varepsilon_0 \times (A/h)$$

Where: ε_r - DK of PCB Material

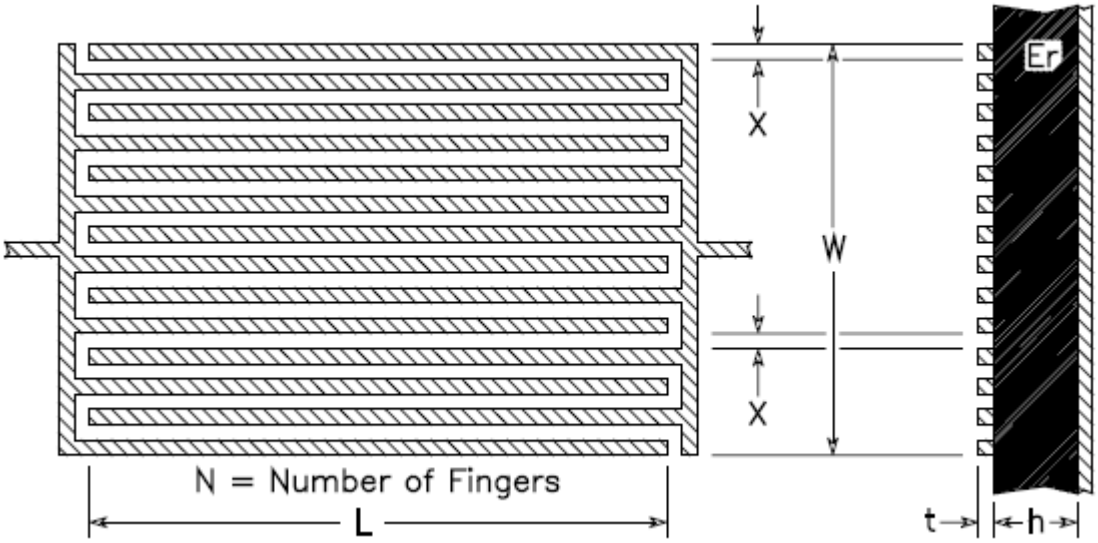
ε_0 - Permittivity of Space

$(2.25 \times 10^{-13}$ ferrads/in.)

A - Area of Plate (L x W)

h - Dielectric Thickness

- Interdigital Capacitor



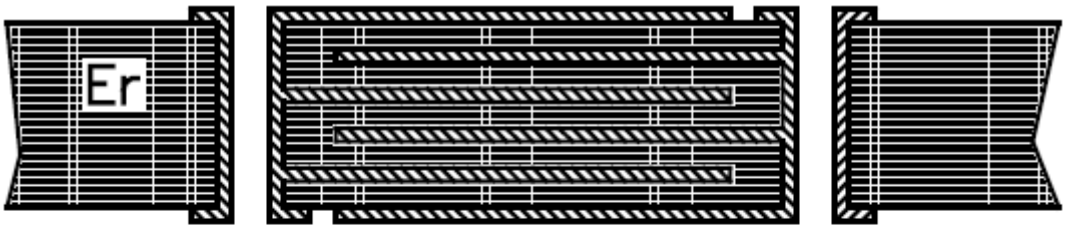
$$C_2 = \frac{\varepsilon_r + 1.0}{w} L\left[(N - 3.0)A1 + A2\right] \quad (\text{pF / in})$$

$$A1 = \left[0.3349057 - 0.15287116\left(\frac{t}{X}\right)\right]^2$$

$$A2 = \left[0.50133101 - 0.22820444\left(\frac{t}{X}\right)\right]^2$$

(Equation valid for h>w/N)

- Multilayer Capacitor



$$C = \frac{0.229\varepsilon_r A(n - 1.0)}{d} \quad (\text{pF})$$

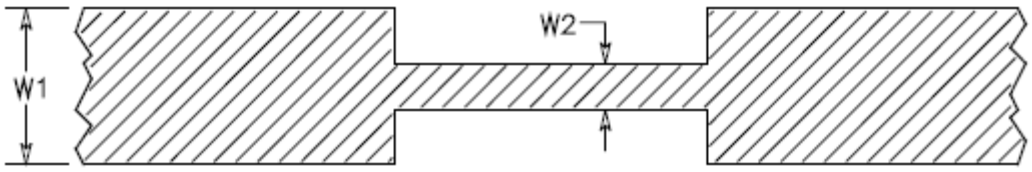
where:

A = area of planes in square inches

n = number of conductor layers

d = plate spacing

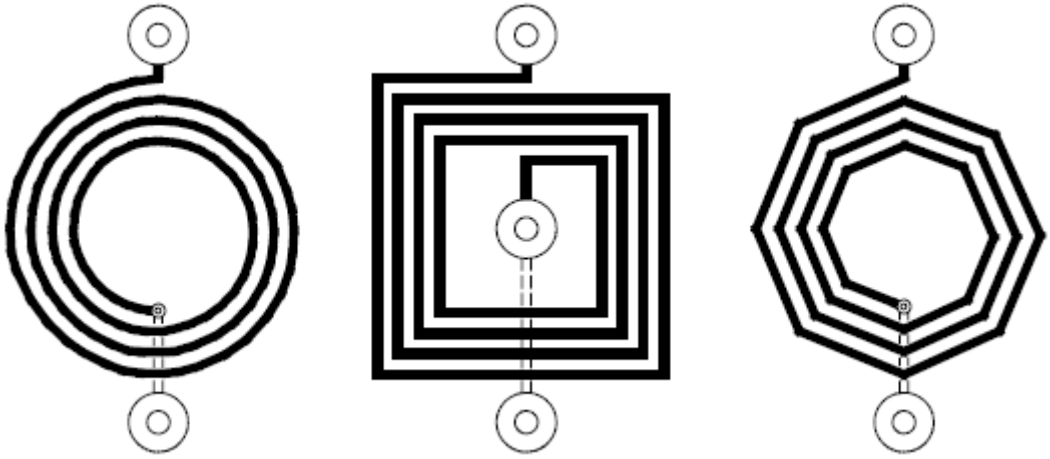
- Inductor- inline inductor is formed by a very thin, high-impedance trace.



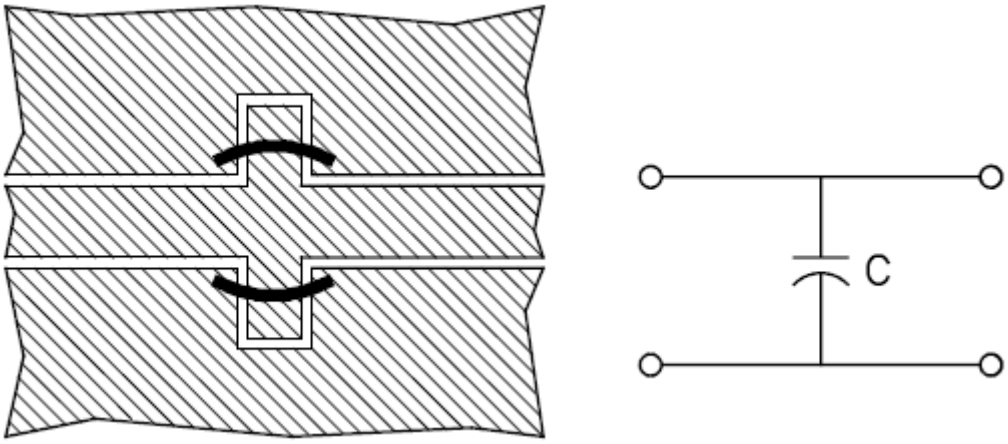
✧Length Must be Shorter than Critical Length to Prevent Reflections. Can Remove Plane(s) to Boost Inductance.

✧L = Zo^2 x C or Tpd x Zo (Many Equations available. This is Extremely Accurate.)

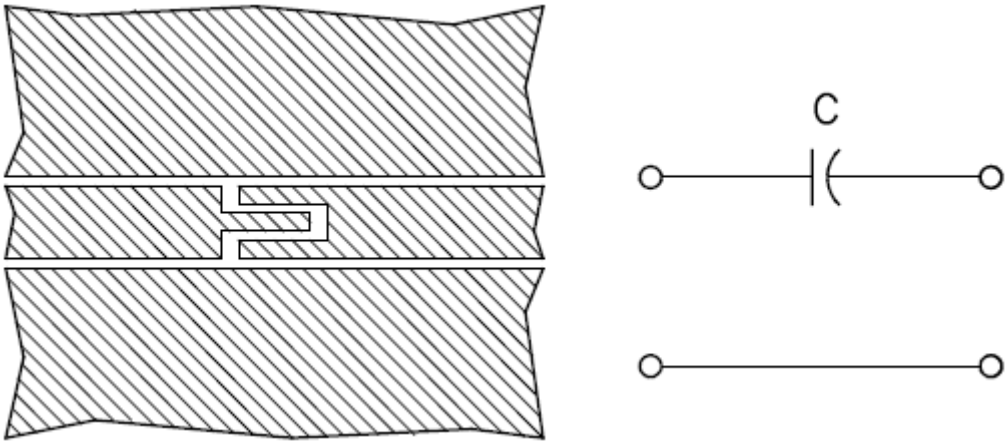
- Spiral Inductors



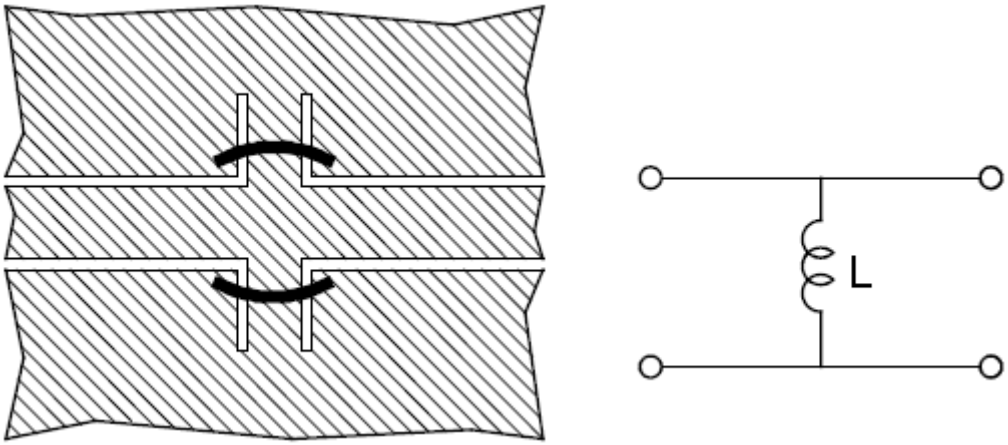
- CPW & CPWG Shunt Capacitor



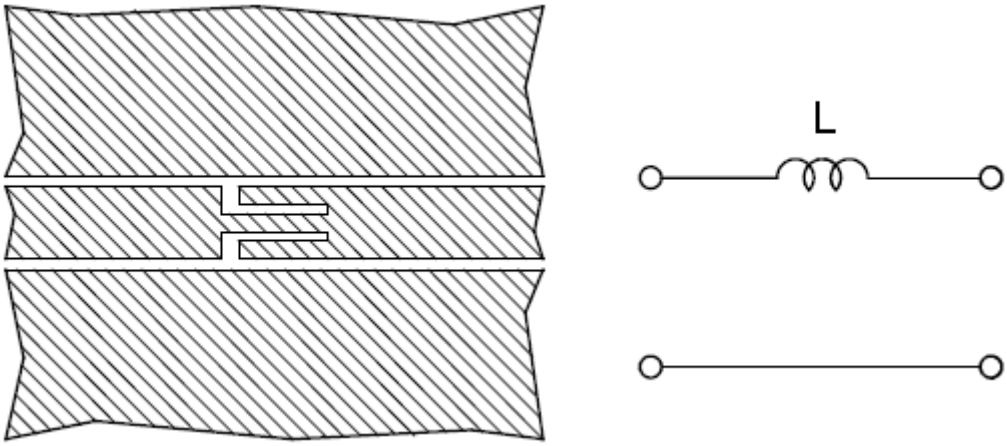
- CPW & CPWG Series Capacitor



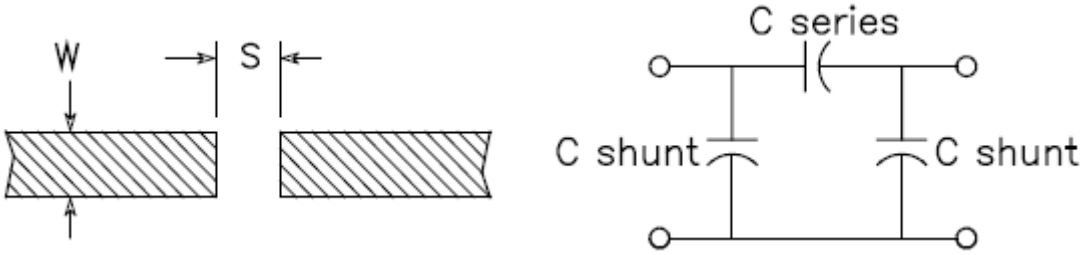
- CPW & CPWG Shunt Inductor



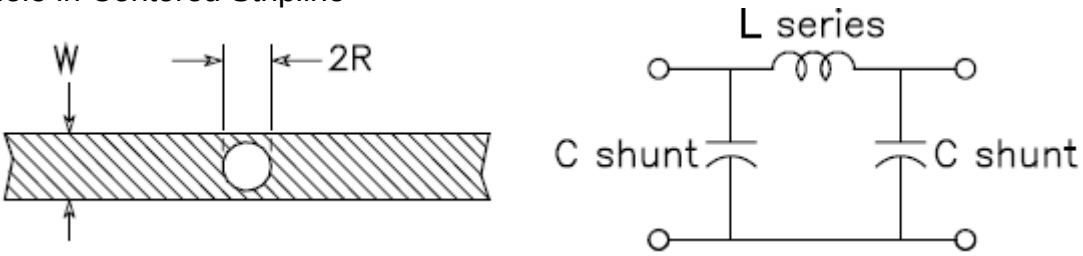
- CPW & CPWG Series Inductor



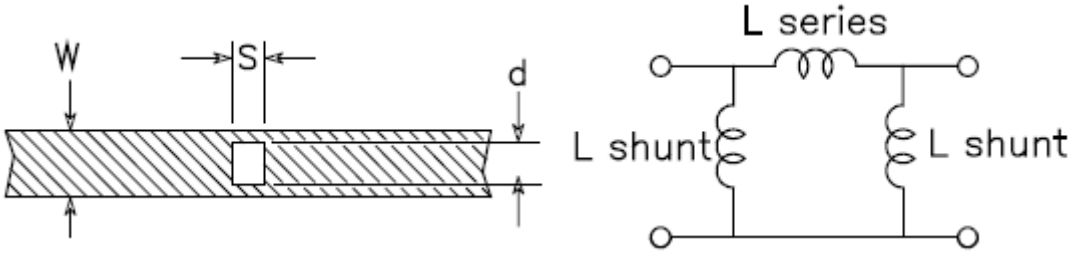
- Gap in Centered Stripline Conductor



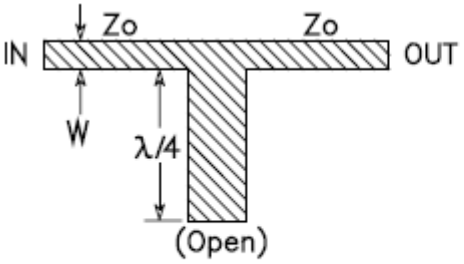
- Round Hole in Centered Stripline



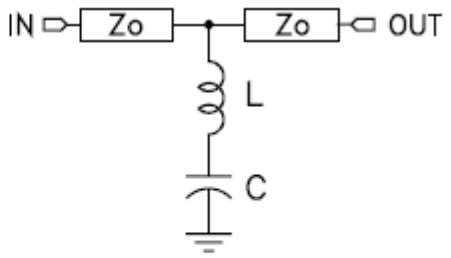
- Rectanular Hole in Centered Stripline



- Filters can be made from the L & C circuit elements discussed.
  - λ/4 Stub is series resonant circuit at frequency.
  - Circuit shorts to ground at λ/4, 3/4λ, etc.
  - Open circuit at DC, λ/2, λ, etc.



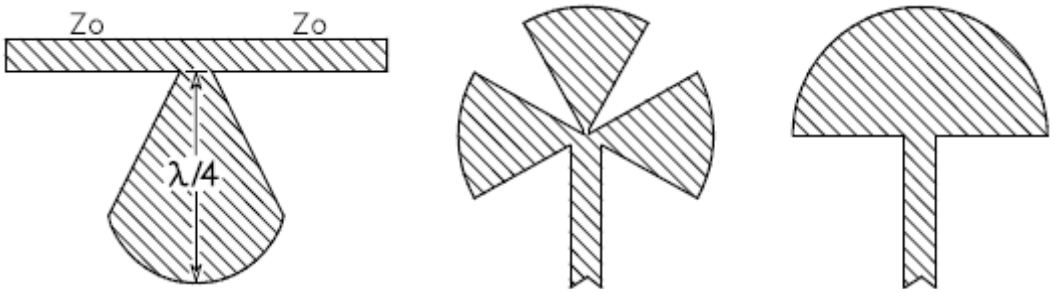
Microstrip Open–Stub



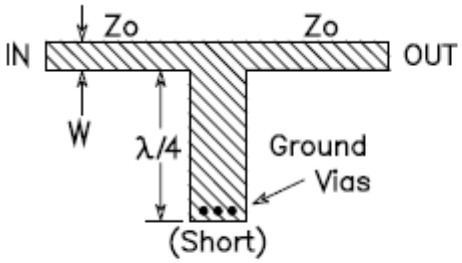
Microstrip Open–Stub Equivalent Circuit at Resonant Frequency

  - 2W wide for high-Q and to prevent reflections
- Open Stubs (one just shown) have narrow frequency over which they short to ground.

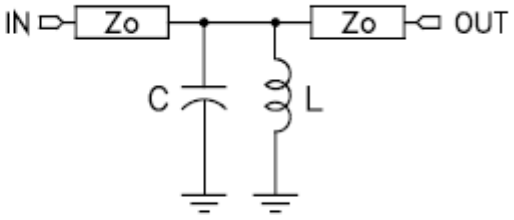
- Flaring the Stub increases frequency response.



- λ/4 Stub, shorted to ground, is parallel resonant filter at frequency of interest.
- Circuit shorts to ground at DC, λ/2, λ, etc.
- Open circuit at λ/4, 3/4 λ, etc.

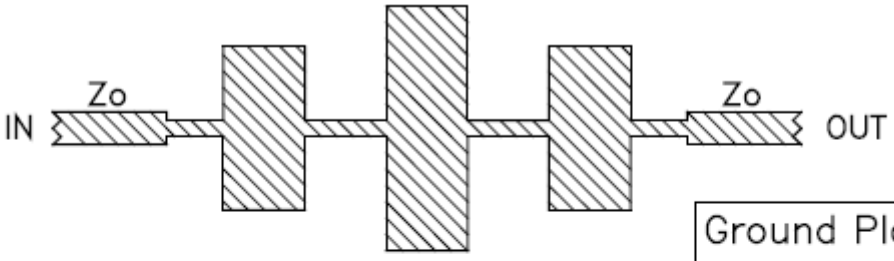


Microstrip Shorted–Stub

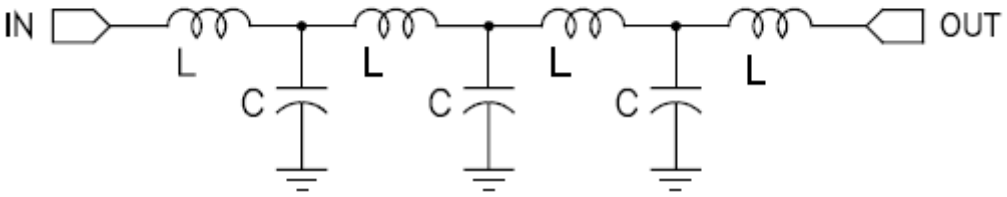


Microstrip Shorted–Stub Equivalent Circuit at Resonant Frequency

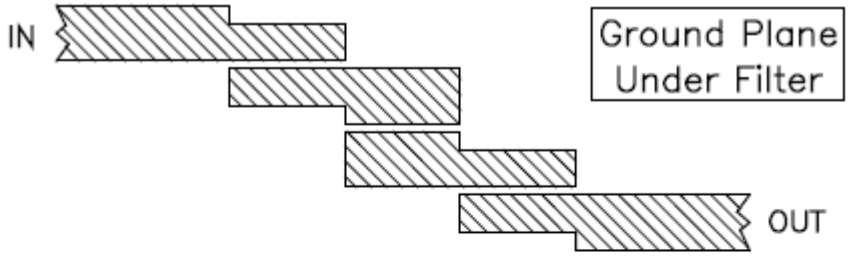
- Low Pass Filter



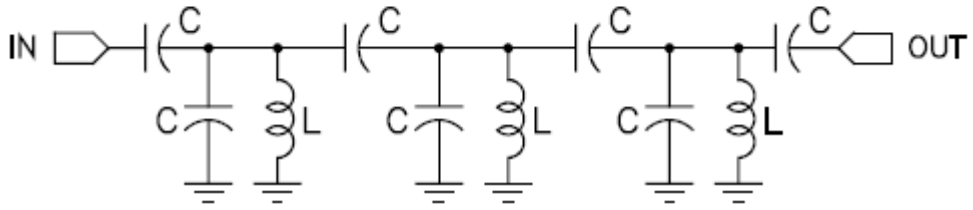
Microstrip Low Pass Filter



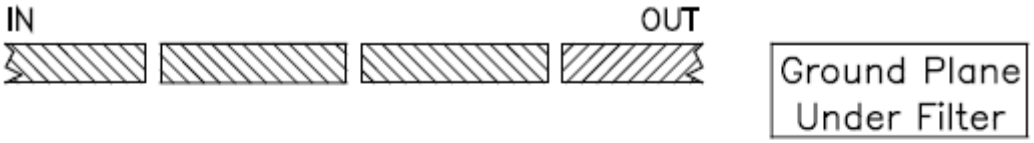
- Edge Coupled Band Pass Filter



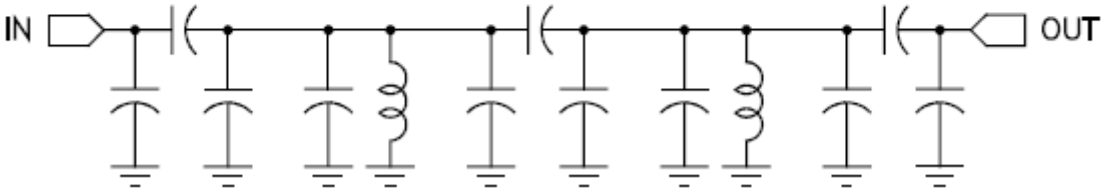
Microstrip Band Pass Filter (Edge Coupled)



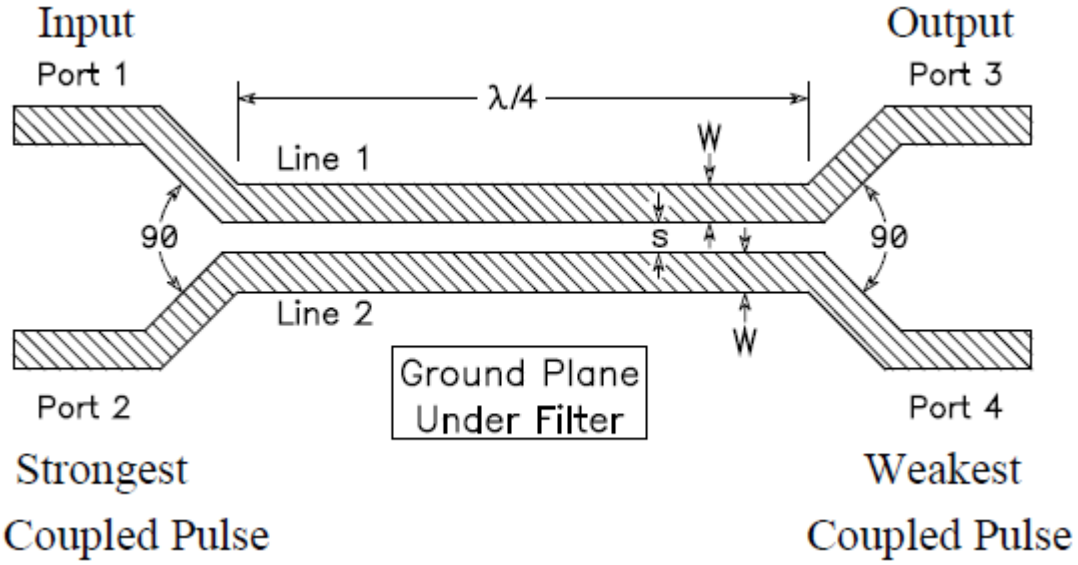
- End Coupled Band Pass Filter



Microstrip Band Pass Filter (End Coupled)



- Directional Coupler

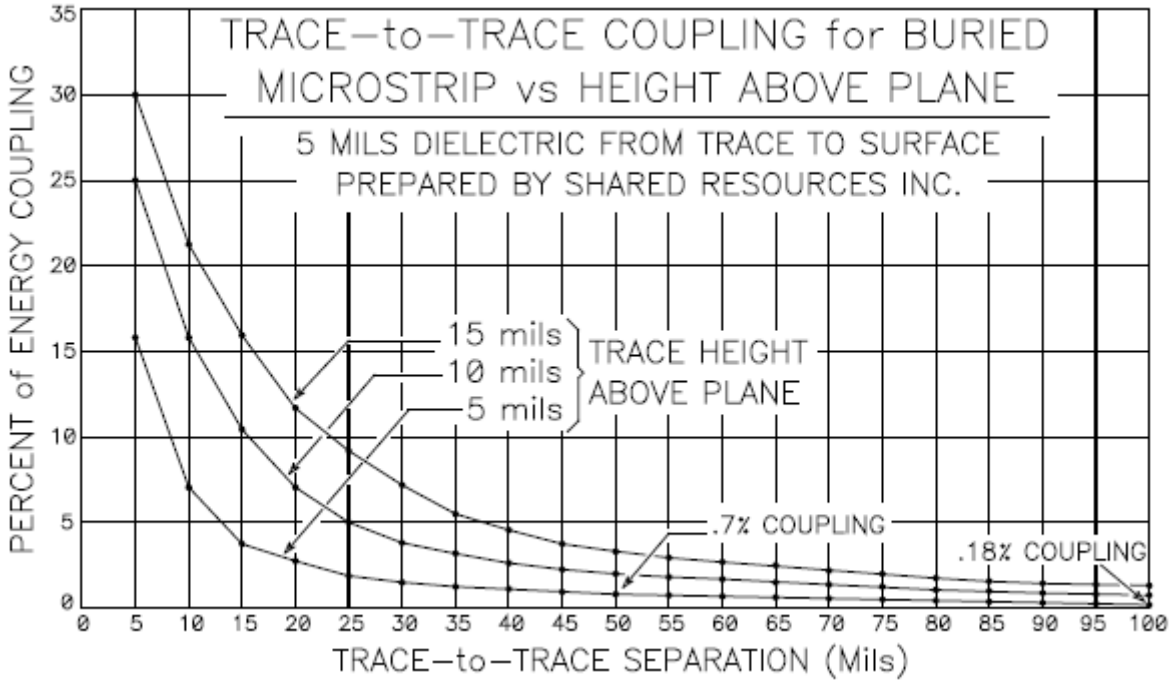


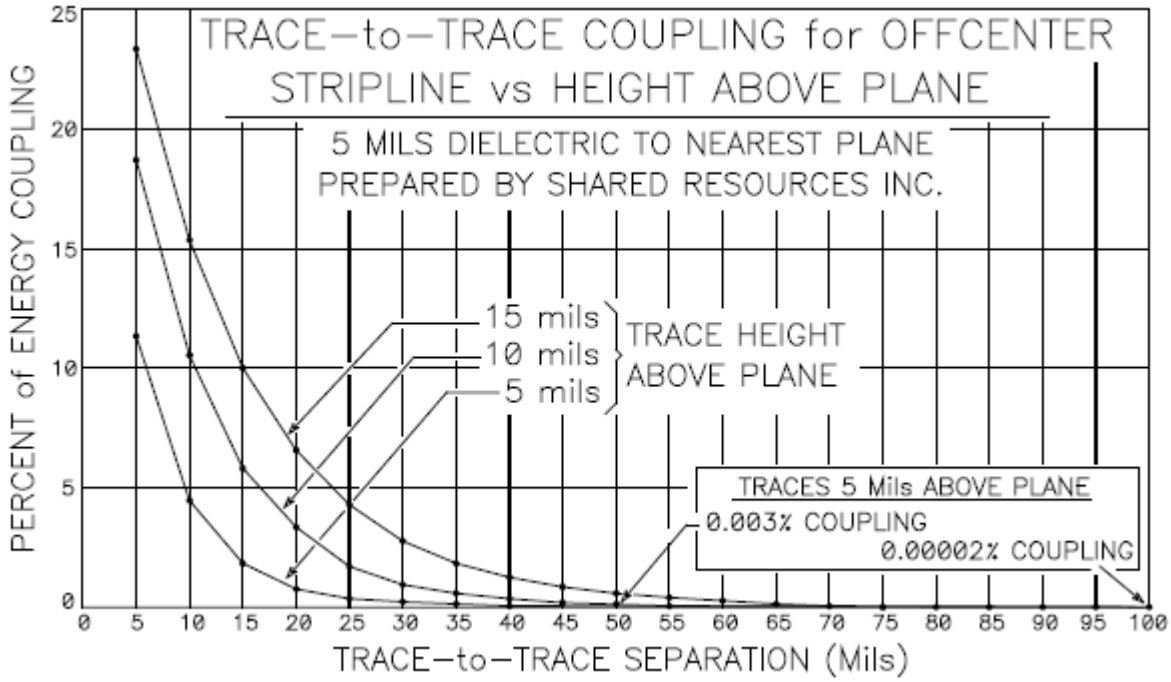
- Directional Coupler can be used as:
  - A Filter at λ/4 Frequencies.
  - Non loading method to transfer energy to another circuit.
  - A method to monitor power send to Port 3.
  - Closed loop feedback control.
  - A non-loading way to measure a signal with an oscilloscope.

- Resistors
  - Impractical when made from PCB copper.
  - Requires extremely long lines to achieve
  - Resistance of a few ohms.
- One Exception -
  - When very small ‘R’ is needed to measure a very large current.

Layout Techniques and Strategies

- Low level analog, RF/Microwave and digital sections must be separated.
- Divide RF/Microwave section into circuit groups (VCO, LO, Amps, etc.).
- Place high frequency components first, to minimize length of each RF route (orientation for function more critical than DFM).
- Place Highest Frequency Components nearest Connectors.
- Don’t Locate Unrelated Outputs and Inputs Near Each Other. Especially Multi-Stages Winding Back on One Another.
- When Either the Output or Input to Amplifiers Must be Long, Choose the Output.
- Remember, Trace Impedance (Zo) is a Critical Factor in the Effort to Control Reflections.
- Impedance must Match Driver and Load.
- In Traces Shorter than 1/20th λ Long, Zo Matching is usually Not Important.
- When Pull-up Resistors or Inductors are used on the Outputs of Open Collector Devices, Place the Pull-up Component Right At the Output Pin it’s Pulling.
- Also, make certain to decouple the Pull-up, in Addition to the Main Power Pins of the IC.
- Inductors have Large Magnetic Fields Around Them-
  - They Should Not be Placed Close Together, when In Parallel (Unless Intent is to have Their Magnetic Fields Couple).
  - Separate Inductors by One (1) Times Body Height (Min) -(OR)-
  - Place Perpendicular to One Another.
- Keep “ALL” Routes Confined to the Stage or Section to which they are Assigned-
  - Digital Traces in the Digital Section. Period.
  - Low Level Analog in Low Level Analog.
  - RF / Microwave in RF / Microwave Section.
  - Don’t Route Traces into Adjoining Sections.
- Short RF Traces should be on Component Side of Board, Routed to Eliminate Vias.
- Next Layer Below RF Traces to be Ground.
- Minimizing Vias in RF Path Minimizes Breaks in Ground Plane(s)-
  - Minimizes Inductance.
  - Helps Contain Stray Electric & Magnetic Fields.
- Controls Lines can be Long, but Must Route Away from RF Inputs.
- RF / Microwave Lines Must be Kept Away From One Another By Min Distances to Prevent Unintended Coupling & Crosstalk.
- Minimum Spacing is a Function of How Much Coupling is Acceptable.

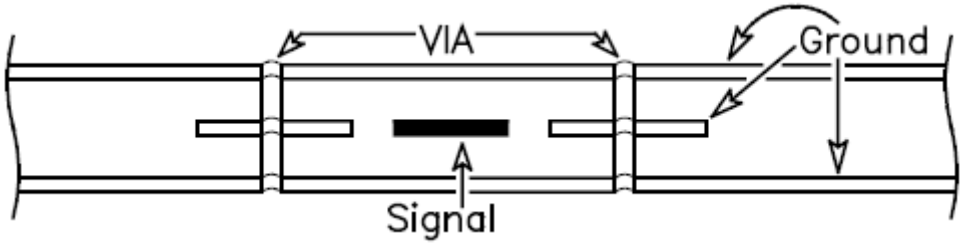




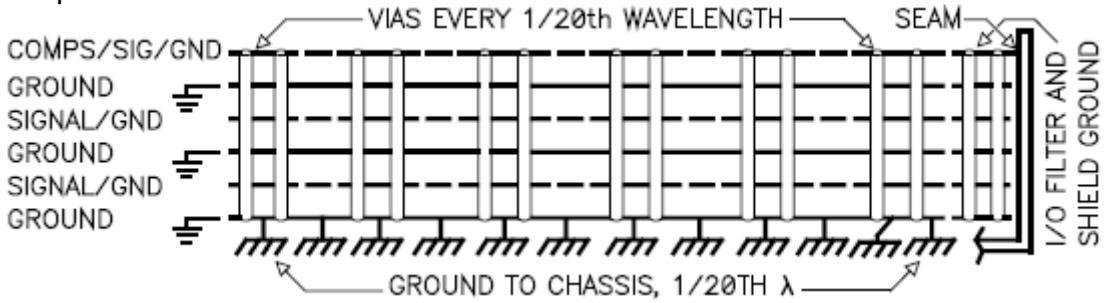
- When Circuit MUST Loop Back on Itself and Outputs end up Near Inputs –
  - Place Ground Copper (20 H Wide) Between Sections, Most specifically Between Inputs and Outputs.
  - Use 20 H Wall if Copper is Less than 20 H Wide.
  - Attach Ground Copper to Board Planes Every 1/20th Wavelength of Principal Frequency.
- Use Same Methods when Unrelated Inputs and Outputs Must Be Near One Another.
- In Multilayer Boards, When Signals Must Change layer, Route in Layer Pairs -
  Layer 1 Signals Reference Ground on Layer 2.
  When Direction Change Needed, Via Signal to Layer 3.
- i.e.: First Four(4) Layers of a Board

- - - - - - - - - - - Layer 1 (Signal - X Direction)
---------- Layer 2 (Ground Plane)
- - - - - - - - - - - Layer 3 (Signal - Y Direction)
---------- Layer 4 (Ground Plane)

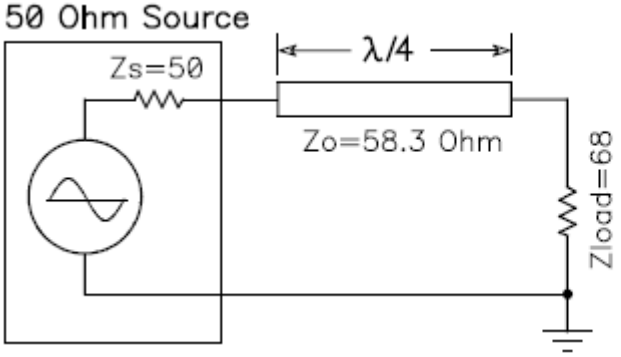
- Components Connecting to Ground
  - Flood Component Lead with Surface Ground. (Let Soldermask or Mask Dam Define Pad).
  - Ground Vias as Close to Component Lead as Possible. Preferably ON Component Lead.
  - Multiple Vias (3, 4, etc.) Reduce Inductance and Help Eliminate Ground Bounce.
  - Direct Connection. No Thermal Vias.
  - Must attempt to permit Proper Solder Reflow.
- Ground: All Designs, 2 Layer or Multilayer –
  - Unused Areas of Every Layer to be Poured with Ground Copper.
  - Ground Copper and All Ground Planes through Board to be Connected with Vias Every 1/20th - Wavelength Apart (Where Possible).
  - Vias Closer than 1/20th λ are Better.
  - Very Critical Circuits - Vias Closer than 1/ 20thλ Help Reduce Noise.
  - Direct Connect Vias. No Thermal Vias.
  - 'Copper Pours' Too Small to have Vias Must be Removed (Can Act as Antenna).
  - Arrange Poured Ground Around Signals to Completely Surround Signals



  - Ground Vias to Include Picket Fencing at Edge of Board. In Very Critical Circuits, Plate Board Edge.
  - By Maintaining Isolation Between Circuits, Do Not Split Ground Plane.
  - Attach Ground to Case Continuously.
  - One Exception is Ground for Cable Shields.

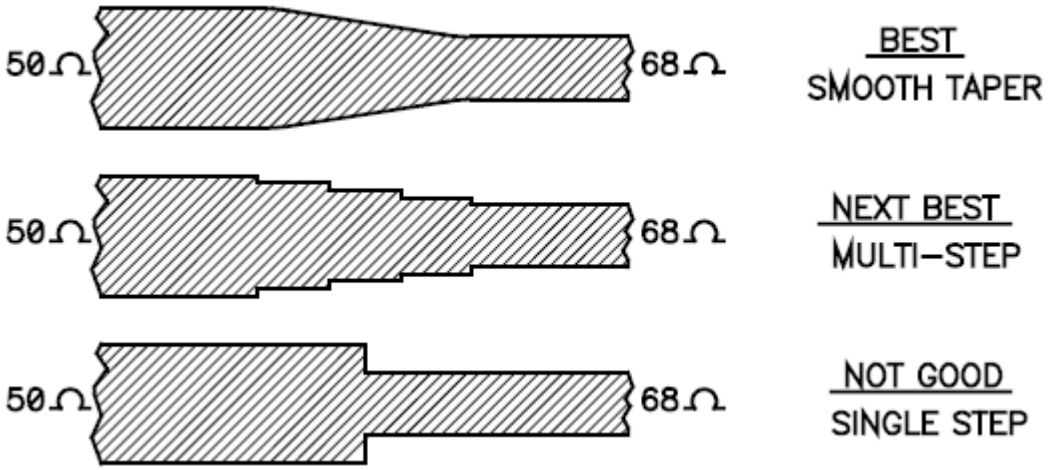


- Mismatched Source and Load Impedance:
  - If Line can be λ/4 Long

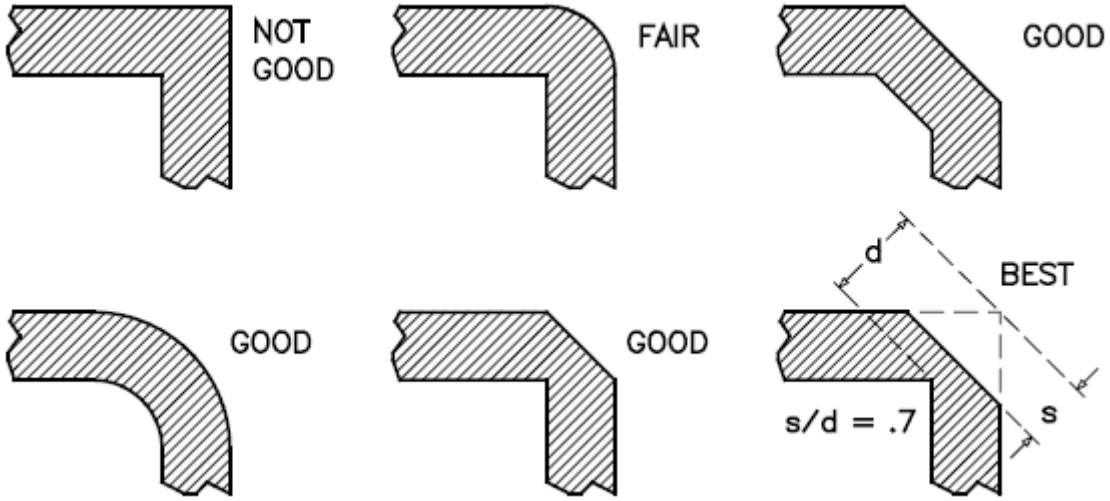


$$Z_0 = \sqrt{Z_s \bullet Z_{load}}$$
$$= \sqrt{50x68}$$
$$= \sqrt{3400}$$
$$= 58.3\Omega$$

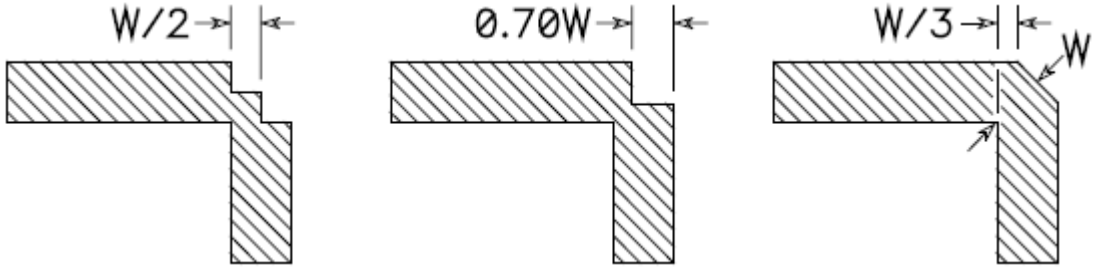
  - (λ/4 is Calculated From Frequency of Source and Eeff of the Transmission Line.)
- Mismatched Source and Load Impedance:
  - If Line Can NOT be λ/4 Long -



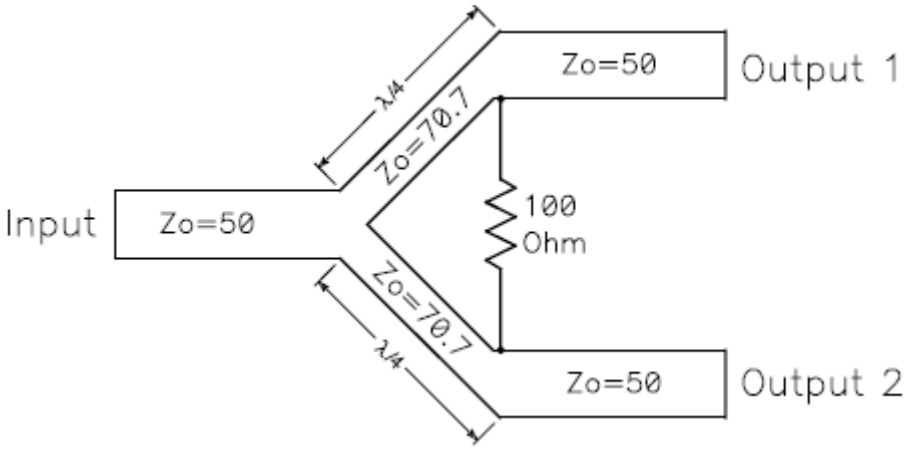
- Trace Corners



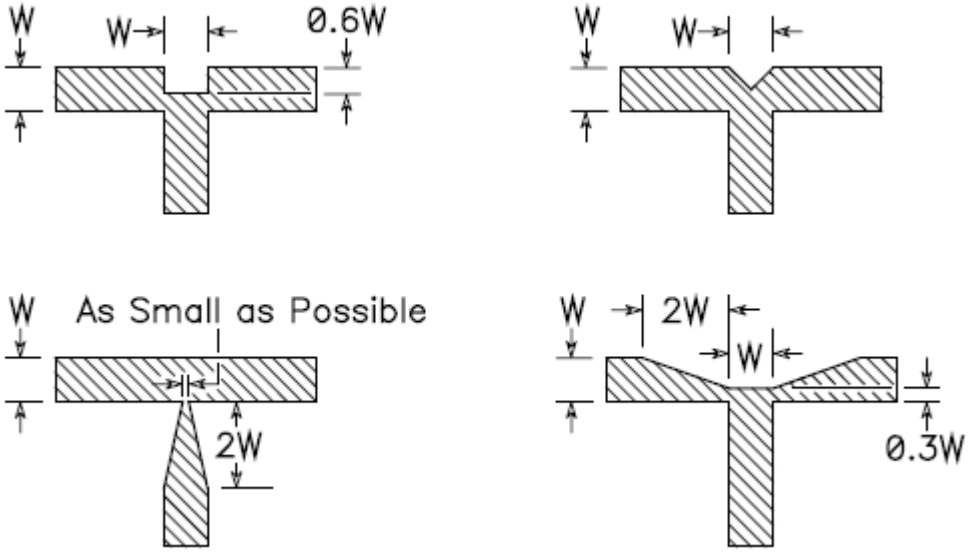
- Others Considered Fair to Good



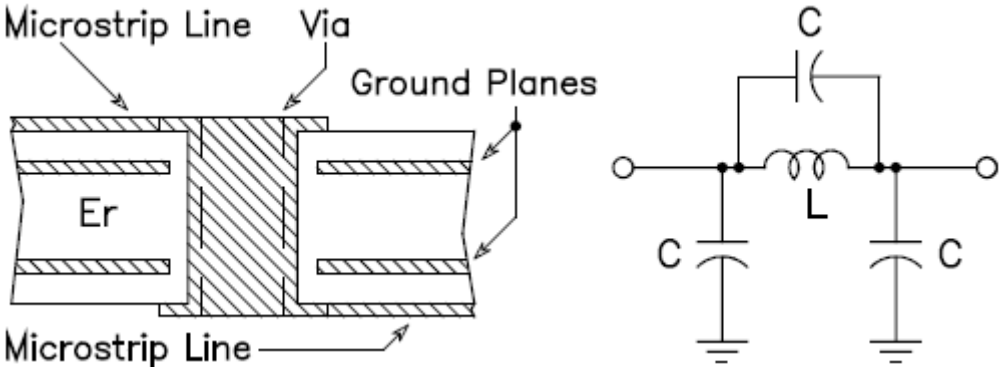
- 'T'-Junctions:
  - Ideal is the Wilkinson Splitter



- ‘T’-Junctions (Acceptable):



- Impedance of Vias



- Copper Patches can be placed Next to Signal Traces to Create Attachment Points for Wire or Solder to Create Tuning ‘C’ or ‘L’

- Long Microstrip Traces can be Antenna for Radiation of EMI or Reception of Noise.
- Ideal Trace Antenna is 1/4 Wavelength Long.
- In Designs where Stripline is available, Keep Outer Layer Traces under Critical Length.

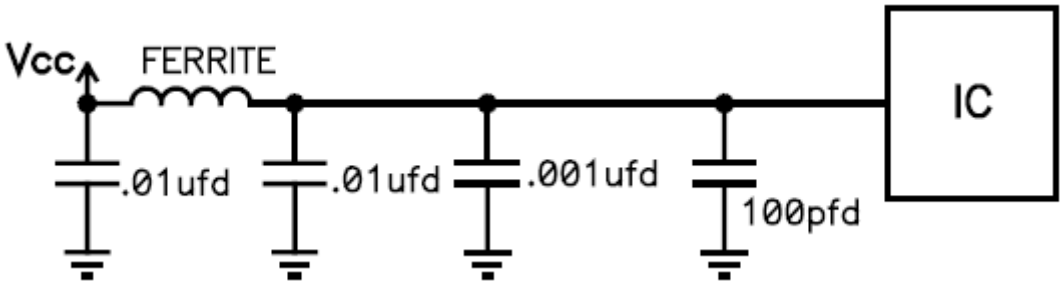
Power Bus

- Route Power in 2 Layer Board (Microstrip, CPW or CPWG) (Only Plane is Ground).
- In Multilayer Boards Power Can be Plane if One(1) Voltage or Split Plane if Several Voltages.
- In Multilayer Board with Many Voltages, Power is Usually Routed on One (1) or more Layers.
- When Routed, Make Power Grid if two(2) or more Layers are used. Grid Most Closely Emulates Behavior of a Plane.
- Due to Self Resonance of Decoupling Caps, selected to match Frequency of Operation, Wide Routes work as well in Analog Circuits to distribute Power as do Planes.

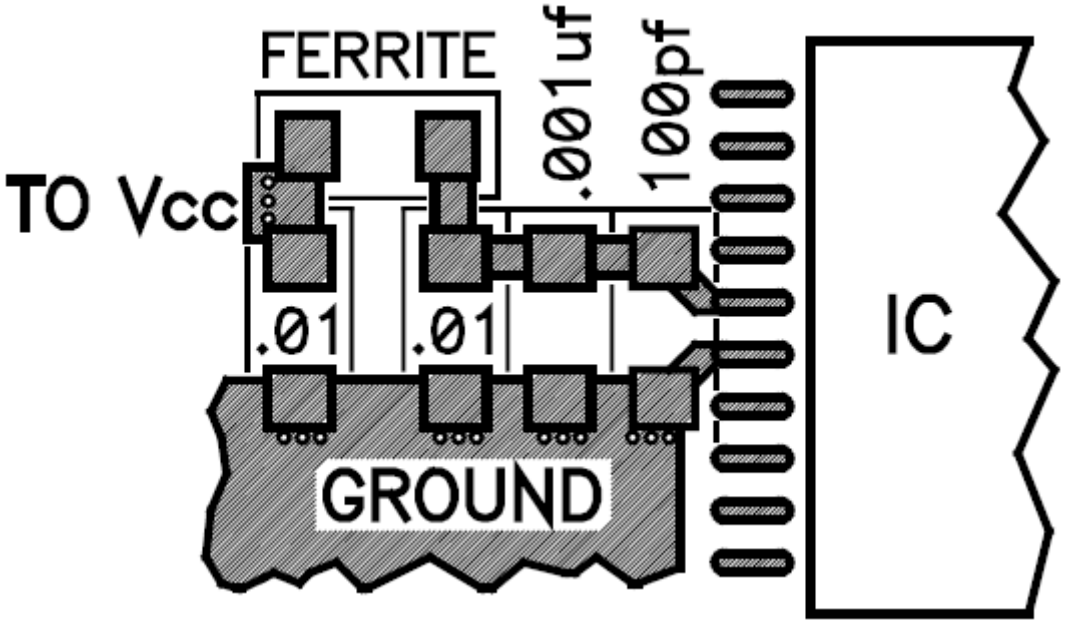
- Power is generally routed between Power Ground Planes to help Lower Noise Coupling in Power Bus.

---------- Ground
-- -- -- -- -- -- Power
---------- Ground

- Ground Planes are **Always** Continuous. (Only Split at Front Panel for Cable Shields and Filters).
- Power Decoupling Consists of Low Pass Filter with Several Capacitors to Cover a Broad Range of Frequencies and Currents-



- Select Capacitors in Low Pass Filter so Smallest Value has Self Resonance of Operating Frequency of Circuit.
- Largest Value selected to carry Maximum Current Drawn by IC.
- Capacitors Progress Upward in Value in Steps of 10 Times.
- Place Caps w/ Smallest Value Near IC, then Next Largest Value, etc.
- Place Smallest Value Capacitor **AT** Power and Ground Pins of IC.
- Ideally, Capacitors are in Parallel with Power & Ground Pins of IC.
- When Not Possible, Place Smallest Value Capacitor at Power Pin of IC and as Near Ground Pin as Possible.
- Attach Caps w/ Wide Traces & Gnd Floods.
- Many Vias, Large Enough to Carry Current.



Board Stack-Up

- In 2 Layer Boards, Dielectric Will be Tightly Controlled (And Usually Not .062").
- Dielectrics of .015-.025" Thick, Common.
- In ALL Designs, One Ground Plane MIN.

- In CPW, to create Continuous Ground, Strap Across Sig Lines From Ground to Ground.
- In Microstrip / CPWG, Pour Ground on Sig Side, w/ Continuous Ground Opposite Side.
- In Multilayer Board, have Ground on Every Other Layer.
- Signals Located on Either Side of Ground Plane Must Cross at Right Angles.
  (Planes give 60 dB of Isolation of Currents on Either Side. 60 dB May Not be Enough in RF / Microwave Circuit, Hence Right Angle Routing.)
- Remember, Route in Layer Pairs.
- Typical High Layer Count Board

Layer 1	-- - -- - -- - -- - --	Devices, Short Signals, Ground
Layer 2	----------	Ground Plane
Layer 3	-- - -- - -- - -- - --	Signals, Ground Pour
Layer 4	----------	Ground Plane
Layer 5	-- - -- - -- - -- - --	Signals, Ground Pour
Layer 6	----------	Ground Plane
Layer 7	----------	Power Plane or Power Routes
Layer 8	----------	Ground Plane
Layer 9	-- - -- - -- - -- - --	Signals, Ground Pour
Layer 10	----------	Ground Plane
Layer 11	-- - -- - -- - -- - --	Signals, Ground Pour
Layer 12	----------	Ground Plane

- When RF Stages Located on Opposite Sides of a Board, Blind Vias May Be Needed in Each Stage to Effectively Create Back-to-Back Boards

Layer 1	-- - -- - -- - -- - --	Devices, Short Signals, Ground
Layer 2	----------	Ground Plane
Layer 3	-- - -- - -- - -- - --	Signals, Power, Ground Pour
Layer 4	----------	Ground Plane
Layer 5	----------	Ground Plane
Layer 6	-- - -- - -- - -- - --	Signals, Power, Ground Pour
Layer 7	----------	Ground Plane
Layer 8	-- - -- - -- - -- - --	Devices, Short Signals, Ground

Signal Attenuation

- Increases or Decreases Pulse Amplitude
  1)Reflections (Return Loss / VSWR - Critical).
  2) Signal Cross Talk (Critical in RF).
  3)Reference Voltage Accuracy (Critical in RF).
  4) Power Bus Noise (Minimal- Filtered).
  5) Ground/Vcc Bounce (Minimal in RF).
  6) Skin Effect (Resistive Loss in Conductor).
  7) Loss Tangent (Property of PCB Dielectric).

Skin Effect

- Increases Resistive Signal Loss (Adds Heat).
- Losses Increase with Increased Frequency.
- Amplitude Loss in Analog Circuits.
- Most effected by Line Width and Length.
- Can be a problem above 10's of MHz in Analog circuits.

$$R = \frac{\rho \bullet Length}{AREA_{eff}} \qquad \rho = 6.787 \text{ x } 10^{-7} \text{ ohm-in}$$

$$\rho = 1.724 \text{ x } 10^{-5} \text{ ohm-mm}$$

$$AREA_{eff} = 2(w + t) \bullet SD$$

w - Trace Width

t - Trace Thickness

$$SD = \frac{2.6}{\sqrt{f}}$$

SD - Skin Depth in Inches

f - Frequency in Hertz

$$SD = \frac{66}{\sqrt{f}}$$

SD - Skin Depth in mm

f - Frequency in Hertz

- "R" from equation is ONLY Accurate for Centered Stripline configuration.
- "R" of all other Transmission Line configurations must be adjusted due to 'Proximity Effect'.
  - Microstrip (50 to 75 ohm) - Multiply "R" by 1.70
  - Embedded Microstrip (50-75) - Multiply "R" by 1.85
  - Offset Stripline -
    - Adjust "R" based on Factor Determined by Percent of Offset from Center (OR)
    - Adjust Percent of Attenuation of Signal based on Percent of Coupling to Nearest Plane.
- Attenuation of the Signal is a Function of 'Skin Effect' Resistance and Current in the Transmission Line.

$$Atten(volts) = R \bullet I$$

$$\underline{\text{Where}} - \quad I = \frac{V_{DRIVER}}{Zo_{LOADED}}$$

$$Atten(dB) = \frac{2R \bullet 3dB}{Zo_{LOADED}}$$

Loss Tangent (tan(δ))

- Loss of Signal into PCB Material (Increases Heat).
- Function of Molecular Structure of PCB Material.
- Losses Increase with Increased Frequency.
- Amplitude Loss in Analog Circuits.
- Worse in FR4 (Alternative Materials available).
- Material Selection- Weigh Performance and Price.
- Can be problem above tens of MHz in Analog circuit.

- The amount a signal is attenuated from Loss Tangent can be determined with the equation

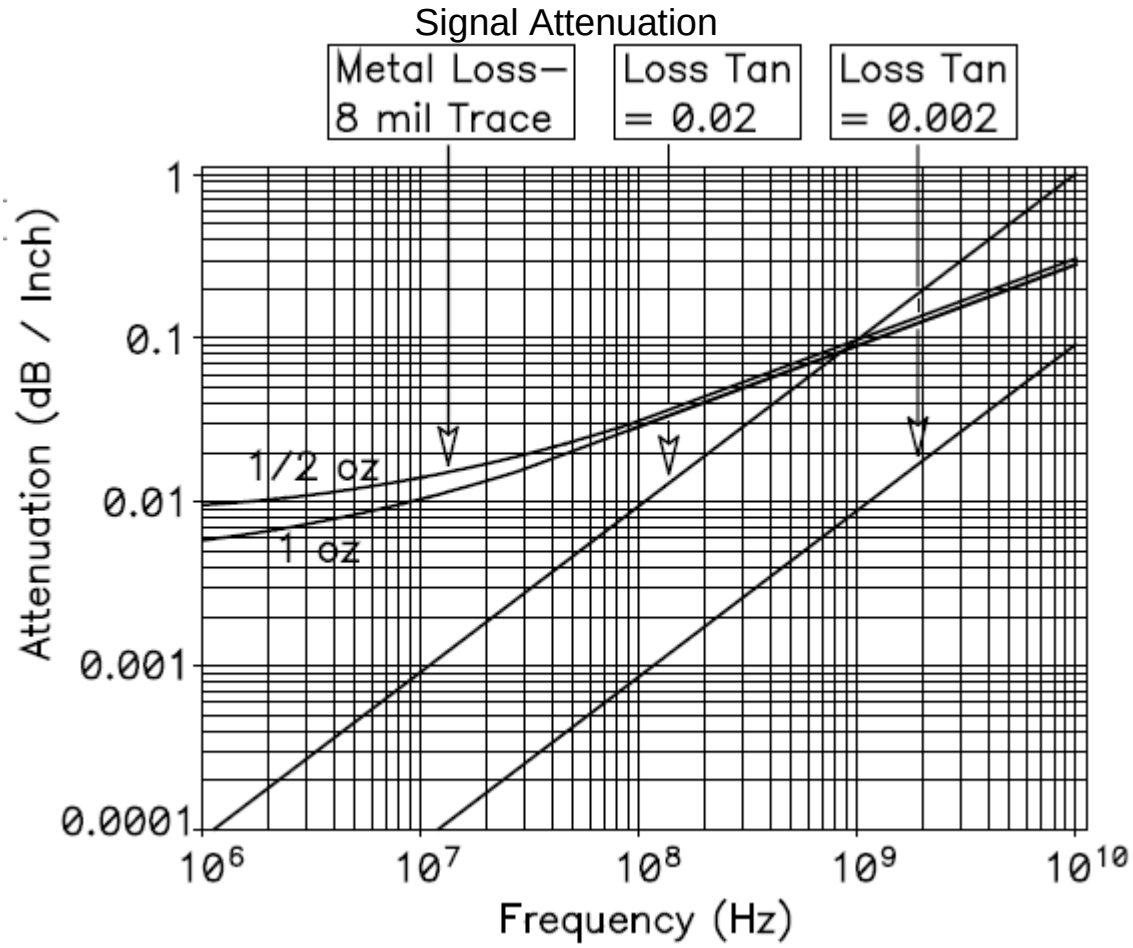
$$\alpha = 2.3 f \cdot \tan(\delta) \cdot \sqrt{\varepsilon eff}$$

Where : α = Attenuation in dB / Inch.

f = Frequency in GHz.

$\tan(\delta)$ = Loss Tangent of Material.

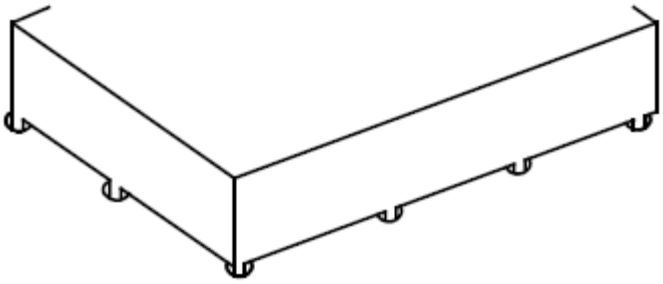
εeff = Effective Relative Er of Material. (Er for Stripline)



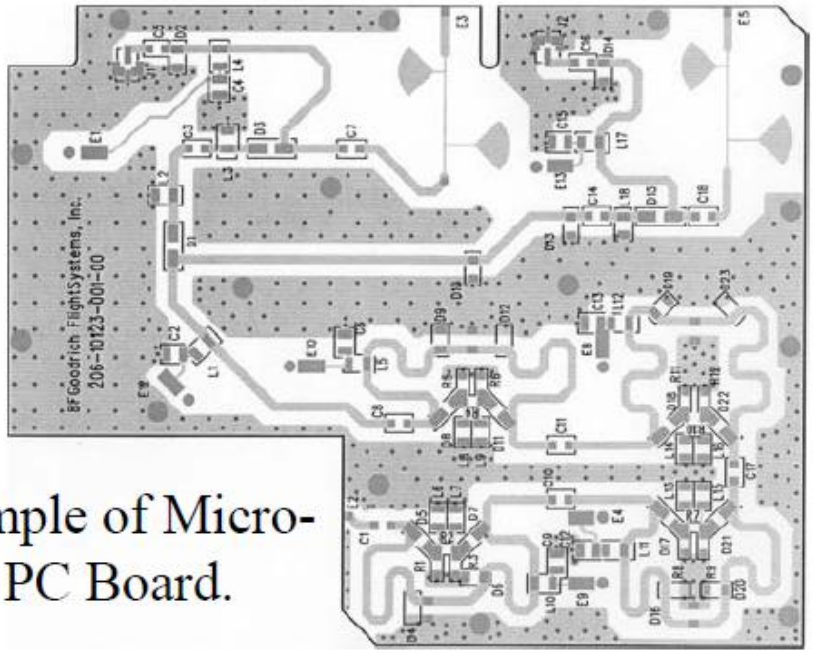
Shields and Shielding

- Use a Metal Can, Grounded Shield when -
  - Circuits are so Close Together that Noise Coupling Naturally Occurs.
  - EMI is Extreme and Cannot be Contained.
  - Circuit is So Sensitive that Normal, Ambient EMI Levels affect Performance.
- Problems! Shields -
  - Use up Valuable Board Space.
  - Are Expensive.
  - Make Trouble Shooting and Repair Very Difficult.
- Shield Cost -
  - Least Expensive is Off-the-Shelf.
  - Next Lowest Cost is Photo Etched.

- Resolve Trouble Shooting / Repair Issues-
    - Tabs Every 1/20th λ instead of Continuous Connection to Ground on Circuit Board.



- Traces Running out of Shielded Area to be Routed on Inner Layers, if possible.
- When Routing from Shield Area on Same Layer as Shield, have a Minimum Opening in Shield Side Wall.
- Cable Exiting Shield Must have 360 degree Attachment of Cable Shield to Metal Can.
- Avoid Other Openings in Shields.
- Open Soldermask Under Shield Edges enough to allow Good Solder Attachment of Shield Walls to Ground Plane.
- Alternative to Soldered Shield- Make Case Lid with Fins/Vanes Long enough to Reach PCB Surface and Contact Ground to Create Compartments inside Enclosure.



Example of Micro-strip PC Board.

PC Board Materials

- Don't Use FR4 in High Power Circuits or Broad Band Applications (Loss & Er).
- Dielectric Loss (Loss Tangent) causes as much as 1/2 Signal Loss in 3" Trace Run over Thick Dielectrics in FR4 at 12 GHz.
- Resistive Loss, Especially Skin Effect, Can be High at Frequencies Above 500 MHz. In Very Sensitive Circuits, even Small Losses Can Create Big Problems.

Board Fab and Assembly

- Teflon Based Materials used in Many RF/ Microwave Circuits Require Fab Houses which Specialize in Such Materials.
- Items Like Tetra-Etch are Essential in the Fabrication of Plated Holes.
- Items such as Large Ground Planes, Flooded Ground Pins of Parts and Multiple Vias On or Near Component Pads force Very Special Attention to Solder Profiles During Assembly.

Base Materials for High Speed, High Frequency PC Boards

Introduction

Two questions often asked, “Will a circuit board made of FR4 laminate work for my High Speed or High Frequency design?” and, “If FR4 isn’t OK, where do I turn?” The answers to these questions are specific to each individual circuit and can only be answered through analysis of the characteristics of FR4 verses other material choices, relative to the demands of the circuit’s noise budget.
This article will outline the material parameters that affect circuit performance and give some direction about how to decide when to choose the correct material for any specific application. For those people who don’t have simulation tools to help calculate the effect of material parameters, a few equations and a graph are included. Near the end of the article is a list of some of the materials available, followed by links to their specifications.
One of the major goals of this article is to provide information that allows designers and engineers to select a material for every PCB application that optimizes both performance and cost.

Circuit Types

There are two basic types of circuits that fall under the heading of high frequency, RF / Analog (aka-RF/Microwave) and High Speed digital. Each of these has their own unique requirements, which have spawned two distinct classes of materials.

RF/Analog circuits usually process precision and/or low level signals. Hence these circuits require much tighter control of parameters pertaining to signal losses. The two losses of greatest concern are losses caused by signal reflections, due to impedance mismatch or impedance changes and the loss of signal energy into the dielectric of the material. Some critical applications also need to focus on losses due to ‘Skin Effect’.

Impedance variations result from two things, material parameters that vary with changes in frequency or temperature and variations in the processes at the fabricator. The amount of signal lost into the dielectric is a function of the material’s characteristics. Skin effect can be partially controlled through choice of copper type in or on the PC board.

Material choice can have a major impact on all these sources of energy loss. As a result materials geared to the RF/Analog domain tightly control parameters such as Dielectric Thickness, Dielectric Constant (Er/DK), Loss Tangent (tan (δ)) and even copper type. In contrast digital circuits can tolerate much greater signal loss and still function. Losses are important in the digital domain as well but because of very broad noise margins of digital ICs, usually don’t affect circuit performance until they become a very significant portion of the noise budget. This most often occurs at very high operating frequencies. Also digital circuits are generally very complex and dense and often require very large, high layer count boards. This tends to put the emphasis for digital materials on process capabilities and cost. These needs have spawned the second group of materials, geared to digital applications.

PCB Materials Development

Through the several decades prior to the 1990’s many high-end laminates were developed for use in RF/Analog circuits, mostly for military applications. Most of these materials are expensive and only a few work well for multilayer boards. Fortunately most of the RF/Analog circuits for which they were developed have low complexity and generally don’t require high layer count boards. During that same period virtually all digital circuits and most low frequency analog circuits utilized the spectrum of FR4 base materials.

Through the 1990's and into this century we have seen a shift in the focus of high frequency and high speed circuitry. As the commercial end of the RF/analog industry has dramatically increased in size, attention has been sharply drawn to the need to produce high end RF/Analog laminates without the 'high end' price tag.
At the same time many digital circuits for telecomm equipment and computers are being pushed into the realm of frequencies where losses can be significant. In today's sub-one nanosecond rise time digital circuits, where clock frequencies are in the hundreds of MHz, the selection of base materials and prepregs used in the laminate structure can play a role in the success or failure of the overall system performance.

Material Parameters

There are a number of material parameters and characteristics important to the overall success of any circuit board. There are 4 parameters that generally affect signal losses:

- Er
- Dielectric Thickness
- Line Width
- Loss Tangent
- There is also a fifth issue that can cause significant losses at some frequencies, Skin Effect.

To gain true control of high speed and high frequency signals, all of these must be considered.

Er (ε_r)

- Relative permittivity is a measure of the effect an insulating material has on the capacitance of a conductor embedded in the material or surrounded by it. It is also a measure of the degree to which an electromagnetic wave is slowed down as it travels through the insulating material.
- The higher the relative permittivity, the slower a signal travels on a trace, the lower the impedance of a given trace geometry and the larger the stray capacitance along a transmission line.
- Given a choice, lower dielectric constant is nearly always better.
- Relative permittivity varies with frequency in all materials. In some materials the variation is small enough that it can be ignored even in very sensitive applications.
- Some materials, like FR4, have broad variations in Er with changes in frequency.
- Changes in Er can be a serious problem in broadband analog circuits. Two common problems are changes in transmission line impedance and changes in signal velocity as the circuit operates across its entire frequency range.
- Impedance changes cause reflections of signal energy that affect circuit performance and often create circuit malfunction.
- Changes in signal velocity will result in phase distortion.
- Broadband RF and microwave circuits usually need to be fabricated from materials with low and fairly constant Er.
- Changes in Er with frequency can also affect digital circuits.
- The greatest effect is to cause errors between calculated and measured impedance. Most suppliers of FR4 laminate measure Er at 1 MHz. If impedance is calculated using an Er measured at 1 MHz and the resulting circuit board's impedance is measured using a TDR with rise time set somewhere between 50 and 150 psec, the resulting impedance measurement will be different than the calculated impedance by as much as 5 to 6%. Engineers and designers need to determine correct values of Er for the board material, at operating frequency. With that knowledge impedance calculations can be made using Er at the frequency of operation and at the test frequency so the effects can be compensated for problems won't develop.
- Another area involving Er that can have major impact is an ultra-fast switching application where low Er is necessary to ensure rapid propagation of signals. In these situations, be they analog or

digital, materials must be selected that offer the operating characteristics required. There are a number of materials designed for analog circuits with low and stable Er. There are also several materials designed for the digital arena that offer a fairly low and stable Er.

- Another potential concern for sensitive analog circuits is the 'Coefficient of Thermal Expansion relative to Permittivity' (CTEr). If the circuit will operate in a broad temperature changing environment attention may need to be paid to CTEr.

Dielectric Thickness and Trace Width

Both of these parameters play a key role in transmission line impedance. Control of each is necessary during fabrication of the board, with the greatest degree of control needed for high frequency analog circuits. How much these parameters vary is a function of both process control by the fabricator and selection of the base material.

- A 20% change in dielectric thickness (trace height above the power or ground plane) can cause as much as a 12% change in impedance (Zo). As dielectric thickness increases, Zo increases. This becomes especially critical with very thin dielectric layers. Due to resin type, glass or filler type and glass/filler-to resin ratios, some materials are much easier to maintain control of dielectric thickness than others. A tolerance on dielectric thickness is generally listed on the data sheets or in the specifications for the various materials.
- A 20% change in trace width can cause as much as a 10% change in impedance. As width increases, Zo decreases. Control of trace width is both a function of process control by the board fabricator and to some degree the type of copper used on the base material.

Printed circuit copper comes in two forms, rolled sheets and electrodeposited (ED) sheets. Each has advantages and disadvantages. The contribution each makes to skin effect is discussed later. Rolled copper is made by cold forming, with heavy steel rollers, thick copper sheets into sheets thin enough to use on a PC board. Rolled copper has mechanical stresses built into it by the rolling process and excellent flatness on both surfaces. This flatness coupled with the high mechanical stresses cause rolled copper to be more prone to delaminate than ED copper, from the base resin. The advantage of the high density and flat surfaces of rolled copper is better control of etching, hence very tight control of trace width.
Electrodeposited (ED) copper is formed by turning a metal drum in a solution of copper sulfate. The copper/liquid is contained in a tank called a plating cell. As the negatively charged drum rotates through the solution in the positively charged cell, copper migrates to the drum surface and forms as an even copper deposition. At the top of the rotation, the copper is pulled off the drum as a foil sheet. The thickness of the copper is a function of charge potential between the cell & drum and the speed of the drum. ED copper has no internal stresses. Additionally it has one smooth surface (the drum surface) and one surface filled with little, spiked bumps known as dendrites. The rough, low density and no stress nature of ED copper (compared to rolled copper) makes it less prone to delaminate but also makes it more difficult to etch precisely.

- The effect on impedance, caused by the difference in etch capability between rolled and ED copper, would barely be noticed in a typical digital circuit.
- The difference can be significant in an analog circuit needing precise impedance control.

The current spectrum of materials designed for digital applications are all supplied with ED copper. Among the spectrum of analog based materials, most offer rolled or ED copper.

- Copper thickness plays a minor role in the impedance of a transmission line.
- A 20% change in copper thickness will cause only a 3% change in Zo. This secondary effect, coupled with the ability of laminate suppliers and fabricators to control copper thickness, make it a variable we can generally ignore.
- In a sensitive, ultra high frequency analog circuit copper thickness variations can have a noticeable effect, but circuits demanding such ultra tight control of copper thickness are rare.
- Copper choice vs resin material is listed on the data sheets or in the specifications for various materials. Material selection will play a role in trace width control and a key role in dielectric thickness control but the fabricator is also a major contributor to proper control of both, especially in high layer count boards. Fabricator selection is an issue that's frequently not given just attention.

All too often the purchasing department of many OEMs and contract assembly houses will make a blind selection of the fabricator based solely on price and delivery. Given the complex nature of quality board fabrication, that's a really bad idea, even in the digital domain. In the high frequency analog domain it's nearly a criminal act. But perhaps that's the subject of another article.

Loss Tangent - tan (δ)

- Loss tangent is a measure of how much of the signal pulse (electromagnetic wave) propagating down the PCB transmission line will be lost in the dielectric region (insulating material between copper layers).
- Loss tangent is a function of the material's resin type and molecular structure (molecular orientation). Lower loss tangent equates to more of the output signal getting to its destination(s).
- The loss factor becomes especially important when working with low level signals like those in many receivers and block down converters (LNB's) or with very high power applications, where a 5% difference in signal loss could mean many watts of lost energy.
- Also of significance in the digital domain are multi-gigabit signals, such as those in ultra high speed Ethernet circuits.

Ideally we want to specify and use materials with very low loss tangent. Unfortunately that can carry a heavy cost penalty, which is why we need to analyze which materials will work and which won't. This gives the freedom to choose a cost effective solution.

- The amount of signal loss in a circuit is not only a function of material type but is also a function of frequency and line length in or on the PCB.

Length will be discussed. Frequency must be viewed differently in digital circuits than in analog circuits. Analog signals consist of sine waves and variations of sine waves and what you see in the time domain is basically what you get in the frequency domain.

- When a sine wave is launched into a transmission line, the frequency of the sine wave propagates unchanged but the amplitude will drop off due to the effects of loss tangent. Since analog signals are sine wave in nature, loss tangent causes a reduction in signal amplitude as the signals propagate. The further a signal travels the greater the reduction in amplitude.
- In contrast digital signals are square waves, which consist of a series of embedded sine waves called harmonics. These harmonics are multiples of the clock frequency and generally have strong amplitude out to a frequency that can be determined by equation:

$$f = 0.35 / Tr \qquad [1]$$

where: f – Frequency in GHz
Tr – Signal Rise or Fall time (Tf) in nsec

- This means that digital signals have a bandwidth of frequencies that are affected by Loss Tangent. The bandwidth starts at the clock frequency of the circuit and extends to the frequency determined by equation [1].

As an example, a circuit with 200 psec rise time signals and a clock frequency of 500 MHz will have a bandwidth of concern from 500 MHz to 1.75 GHz. When a digital signal propagates through a transmission line, each of the sine wave harmonics in the rising and falling edge lose amplitude, as the signal propagates, due to loss tangent, with the highest frequency harmonics suffering the highest losses.

- The loss of amplitude of the harmonics is manifested as a degradation of Rise and Fall time of the signal. This can seriously affect timing of level sensitive signals and can affect both timing and circuit performance of edge driven signals (clocks, enables, resets, etc.).
- There is certainly no rule of thumb to decide at what point an analog circuit will be affected by losses. Every analog circuit must be analyzed to determine anticipated loss verses acceptable loss.
- Digital circuits must also be analyzed individually, but in general when losses to the first harmonic exceed approximately 3dB across the total length of the transmission line it can be assumed that circuit performance will be severely affected. That is to say in a 10 inch line, the amount of loss per inch shouldn't be allowed to exceed 0.3 dB. Again, this is a rule of thumb and is not always a safe bet but it's a good estimation of roughly when to be concerned.

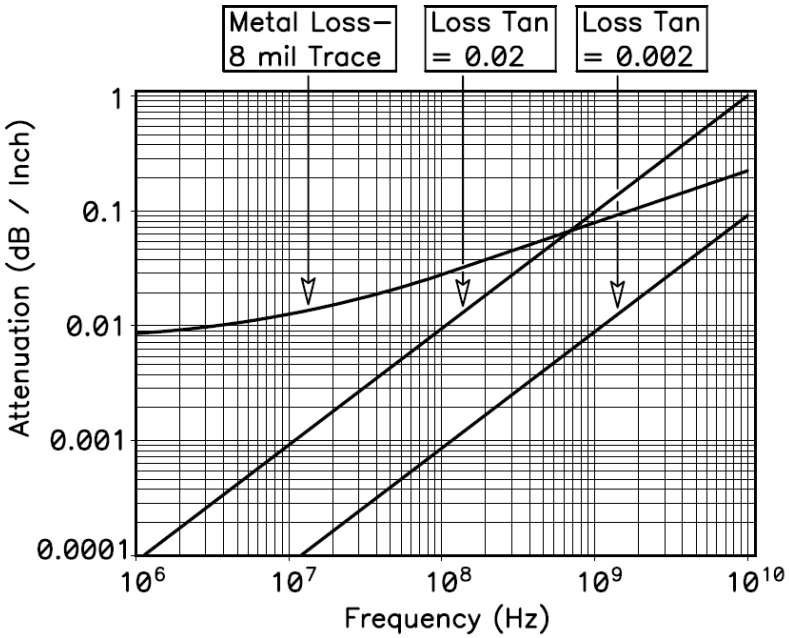


Figure 1 – Graph of Attenuation (tan(δ) & Skin Effect) verses Frequency

The graph in Figure 1 can be used to determine the actual amount of loss per inch in materials with a tan(δ) of .02 (typical for FR4) and materials with a tan(δ) of .002 (typical for several Teflon (PTFE) based materials). Equation [2] was used to build the graphs in Figure 1 and can be used to calculate tan losses for other materials. Notice the graph also shows attenuation for resistive loss in the metal (next section).

$$\alpha = 2.3\, f \cdot \tan(\delta) \cdot \varepsilon_{eff} \quad [2]$$

where: α – Attenuation in dB / Inch.
f – Frequency in GHz.
tan(δ) – Loss Tangent of Material.
ε*eff* – Effective Relative Er of Material.

Resistive Losses and Skin Effect

Voltage drop along a PCB trace, due to resistance in the trace, is a fact of life. From DC through frequencies up to a few MHz, the current in a trace moves through the entire cross sectional area of the trace. At these frequencies resistance is extremely small, hence resistive losses are extremely small. An 8 mil wide trace, at low frequencies, made of 1 ounce copper (1.4 mil) has an approximate resistance of .06 ohms per inch. This was derived from equation [3].

$$R = (\rho\, L) / A \quad [3]$$

where: R – Trace Resistance in Ohms.
ρ – Bulk Resistivity of Copper (6.787 x 10**-7** ohm-in)
L – Trace Length in inches.
A – Cross Sectional Area of the Trace in sq. inches.

When driving a signal into a 50 ohm line with a 50 ohm load, it's easy to see that the resistive drop at these frequencies would be extremely small, in the order of a few milivolts. As frequency increases the energy moving in the trace is forced to the outer perimeter by the large magnetic fields present in higher frequency signals. This is known as skin effect because the majority of the energy is forced to the outer skin of the trace.

Penetration of the signal into the trace is measured in 'Skin Depths', with approximately 66% of the energy penetrating to one skin depth and approximately 97% of the energy penetrating to three skins depths. One skin depth at 10 MHz is .0008 inches. At 10 GHz one skin depth is .000028 inches.

Looking at the example of 10 GHz, most of the energy in the trace would be limited to a depth of approximately 84 millionths of an inch. The net result is a decrease in effective cross sectional area of the trace because much of the copper is not used. It's as if the trace were hollow. Because of skin effect, resistance of an 8 mil trace at 10 GHz will be a little more than 1 ohm per inch. That means the resistive drop from a 3.3 volt signal in a 5 inch, 50 ohm line with a 50 ohm load, at 10 GHz will be greater than 300 mv. In most cases this cannot be ignored. What effect does this have on material choice? In the digital domain, none. Among the materials available for analog boards, as mentioned earlier, some are available with rolled copper. Because of the smooth, dense nature of rolled copper is will suffer less from skin effect losses than its much rougher counterpart, ED copper. According to data gathered by laminate suppliers of high frequency materials, the losses in ED copper are about 12% higher than rolled copper losses, from 3 to 12 GHz. Those needing to calculate skin effect are encouraged to visit Howard Johnson's web article, "Skin Effect Calculations" (see references). Howard does a great job of walking through the calculation of skin depth and resistance at high frequencies. Howard's calculations assume ED copper.

When using materials with rolled copper, losses can be adjusted according. At high frequencies, on microstrip traces (referenced to one plane only), almost all the energy will be on the side of the trace nearest the plane. On stripline (referenced to two planes) the energy will balance for centered stripline and will be offset proportionally in off centered stripline. This is called 'Proximity Effect'. As a result, other than in centered stipline, changes in copper weight (trace thickness) will have little effect on trace resistance at high frequencies. In all cases, changes in width and length will have the greatest effect on resistance at high frequencies.

Combined Effect of Loss Tangent and Skin Effect

In digital circuits resistive drops will have an effect similar to that of loss tangent, meaning rise and fall time of the wave will degrade due to decreased amplitude of the harmonics, with the highest frequency harmonics being affected the most.

In analog circuits the effect is usually a direct loss of signal amplitude.

Looking at the curve for metal loss in Figure 1, we can see that above 1 GHz loss tangent becomes much more severe than skin effect in FR4. To get a true picture of signal loss we need to calculate the combined effects of loss tangent and skin effect. Studies performed by groups such as AMP (Tyco) and NESA (see references) indicate the combined effects of loss tangent and skin effect are often not severe enough, with digital circuits in FR4, to cause circuit malfunction, well into the low GHz operating range. The studies also show that changing material will improve signal quality. But if a circuit will function at a given frequency in a given material, switching to a better grade material at a higher price may offer no benefit. Each circuit should be analyzed based on its particular requirements and available noise and timing budget, especially in the analog domain.

Material Choices –

As mentioned, materials are basically divided into two groups, those designed for digital circuits and those designed for analog circuits. Based on operating parameters, the major differences between the materials are:

- Analog materials generally have a much lower Er that's more stable over frequency and changing temperature.
- Analog materials generally have tighter tolerance on dielectric thickness.
- Analog materials are often offered with Rolled or ED copper. Digital materials come with ED copper only.
- Only a few analog materials are designed for multilayer applications. All digital materials are designed for multilayer applications.

- Loss tangent varies a great deal across the material choices, but is generally much lower in analog materials, often by a factor of 10 or more.

Some of the materials aimed at the digital arena could be used in an analog circuit and in many cases that might be a good use of resources. In fact many of the materials now considered to be high end digital materials were developed for the commercial end of the high frequency analog arena.
Looking through the specs of these materials it will be apparent which are well suited to analog applications, even at very high frequencies.
Table 1 lists materials for digital boards. Some materials list a broad range for Er.
Within a given material low glass content yields a low Er and high glass content yields a higher Er.

Material	Er (* at 1.0 MHz)	Thickness Tolerance	Copper Style	Multilayer Compatible	Loss Tangent
FR4	3.9 – 4.6*	+/- 1-2 mils	ED Only	Yes	.02 - .03
FR408	3.4 – 4.1*	+/- 1-2 mils	ED Only	Yes	.01 - .015
BT Epoxy	3.9 – 4.6*	+/- 1-2 mils	ED Only	Yes	.015 - .02
Cyanate Ester	3.5 – 3.9*	+/- 1-2 mils	ED Only	Yes	.009
Polyimide	4.0 – 4.5*	+/- 1-2 mils	ED Only	Yes	.01
GETEK	3.5 – 4.2*	+/- 1-2 mils	ED Only	Yes	.012
Nelco 4000-13	3.7 (1GHz)	+/- 1 mil	ED Only	Yes	.01
Nelco 4000-13SI	3.5 (1GHz)	+/- 1 mil	ED Only	Yes	.009
Nelco 6000	3.5 (1GHz)	+/- 1 mil	ED Only	Yes	.008
Nelco 6000SI	3.2 (1GHz)	+/- 1 mil	ED Only	Yes	.005
Speedboard N	3.0 *	+/- 1 mil	Prepreg	Yes	.02
Speedboard C	2.6 – 2.7*	+/- 1 mil	Prepreg	Yes	.004
Arlon 25 / Rogers 4003	3.4 (10GHz)	+/- 1 mil	ED Only	Yes	.0027

Table 1 – Materials intended for Digital Applications.

Of the materials listed above BT Epoxy, Cyanate Ester and Polyimide were developed as replacements for FR4 in applications needing extreme mechanical stability, with Cyanate Ester also offering some improvement in performance. GETEK and FR408 are intended to offer improved electrical performance. The four Nelco materials offer a great deal of improvement in electrical performance and the two Speedboard materials were designed as prepregs, to use in applications where a low Er material can be mixed with fairly low cost materials to create a board with a lower Er and imprved performance. Arlon 25 and Rogers 4003 were originally designed to fit into the analog market as a commercial replacement for some of the high cost, high end military grade laminates. They are listed with the digital materials because many engineers consider them an excellent choice when very high end parameters are required in digital circuits. Table 2 lists materials for analog circuits. The materials listed give an order number for Rogers Corp only. This is not an attempt to push one supplier. The numbers listed are most familiar to the writer. Most of these materials have equivalent choices from other makers of laminates (Arlon. Taconic and 3M – See supplier list at end of article).

Material	Er (10.0 GHz)	Thickness Tolerance	Copper Style	Multilayer Compatible	Loss Tangent
Rogers Ultralam 2000	2.4 – 2.6	+/- .5 mil	ED / Rolled	No	.0019
Rogers 5870	2.3	+/- .5 mil	ED / Rolled	No	.0012
Rogers 5880	2.2	+/- .5 mil	ED / Rolled	No	.0009
Rogers 6002	2.94	+/- .5 mil	ED / Rolled	Yes	.0012
Rogers 3003	3.0	+/- 1 mil	ED / Rolled	Yes	.0013
Rogers 6006	6.15	+/- .5 mil	ED / Rolled	No	.0019
Rogers 6010	10.2	+/- .5 mil	ED / Rolled	No	.0023
Rogers 3006	6.15	+/- 1 mil	ED / Rolled	Yes	.0025
Rogers 3010	10.2	+/- 1 mil	ED / Rolled	Yes	.0035

Table 2 – Materials for Analog Applications.

The Ultralam and the 5000 and 6000 series materials are all approved for military applications. The 3000 series materials are commercial equivalents of the 6000 series materials. Each of these is designed for specific environments and applications, all of which are too lengthy to state in this article. Research of the materials and their equivalents from other suppliers is encouraged. As mentioned, most of these materials have an equivalent from suppliers such as Arlon, Taconic or 3M. Material costs are not listed, as they change frequently. The user is strongly encouraged to talk with their fabricator about cost of the finished board, utilizing one material verses another. Some of the fairly expensive materials are easy to fabricate and might result in a finished board that's less expensive than a cheaper material that creates manufacturing difficulties. Overall costs of the material alone range from $1.50/sq. ft., for the low end of the FR4 spectrum, to as much as $100.00/sq. ft, for some of the very high end, analog laminates.

Tg

One material parameter not discussed is Tg.

- All materials exhibit changing temperature coefficients of expansion as temperature increases.
- Tg is the temperature at which materials begin to expand at an uncontrolled rate.
- Boards operating beyond Tg are subject to failure.

This is another parameter the reader is encouraged to understand. A number of articles exist regarding Tg. One excellent article is by Lee Ritchey (Speeding Edge) entitled, A Survey and Tutorial or Dielectric Materials used in the Manufacture of Printed Circuit Boards (see references).
For circuits operating in a broad temperature environment, additional parameters that should be investigated are CTEr, CTE and CTE of the base material verses copper.

Conclusion

The reader is encouraged to run through the equations provided for Loss Tangent and check those available on Howard Johnson's website for Skin Effect, then compare the numbers against the available noise and timing budget for the circuit in question. This analysis will show that most digital circuits today (0.2 to 2.0 nsec rise and fall times) can use FR4 as a base material without concern of circuit malfunction. Analog circuits must always be analyzed to compare the operating parameters of the material against the acceptable losses in the circuit, then choose the material most suited to the application, looking at cost as only one of the driving factors. Once a material is chosen, equal care should go into selection of the fabricator for the bare board, keeping in mind that an acceptable level of quality and lowest price may not walk hand in hand. This is especially true for sensitive, high frequency analog boards, requiring fabricators who have the equipment and process controls needed to make boards from the specialized materials discussed. Remember too, fabricators can be a wealth of knowledge about materials.

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