ECE 3274 MOSFET amplifier design. Richard Cooper

Setion1 CS amp open loop

Section 2: CS with Rsf gain controlled

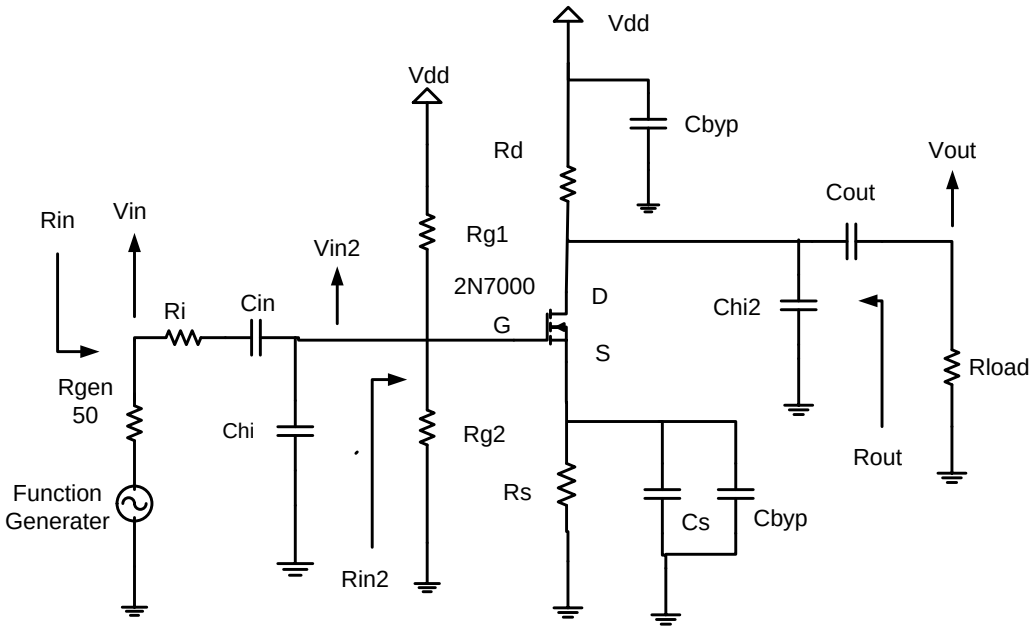
Section 3: CD amp

Common source (CS)

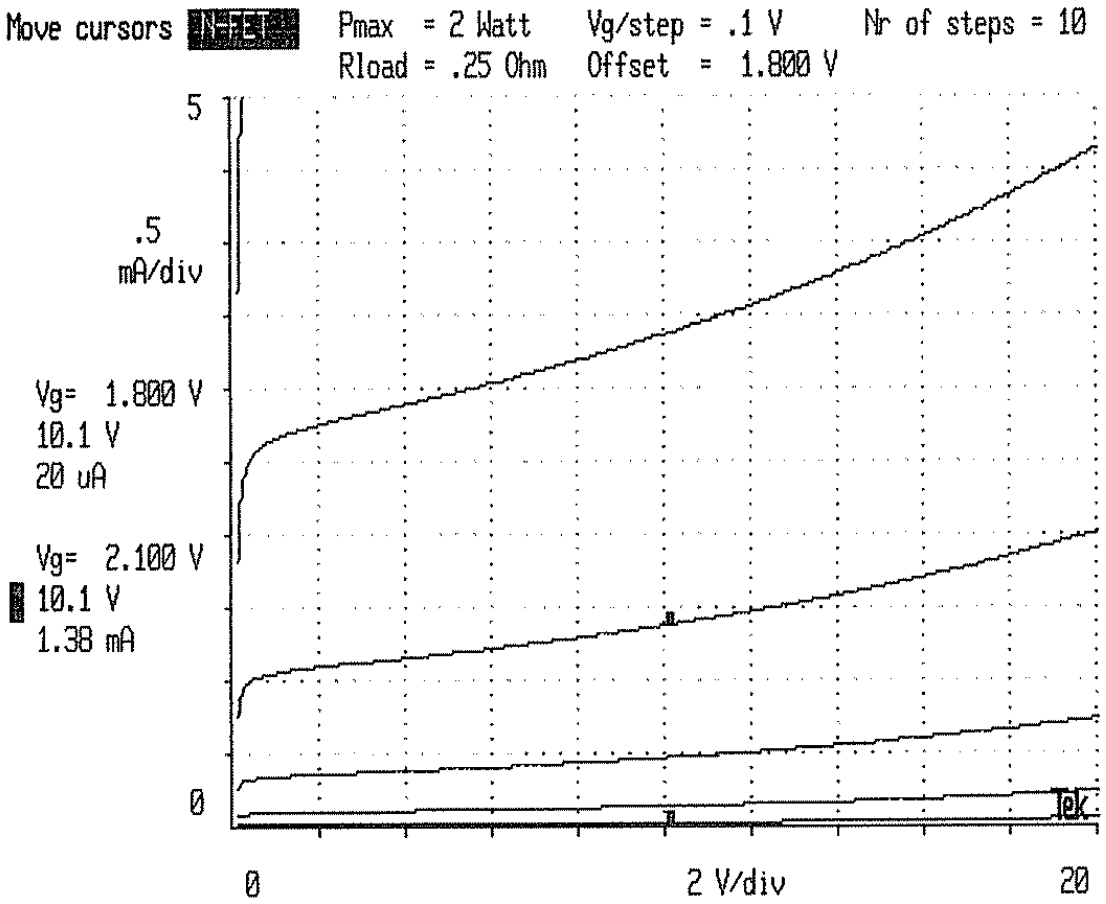
Designing procedure of common source MOSFET amplifier can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements, it leaves the designer enough freedom to choose the operating point as necessary for the application. However, it is to remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are fairly tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.

Section 1: Common Source with Source Resistance Bypassed Configuration (open Loop)

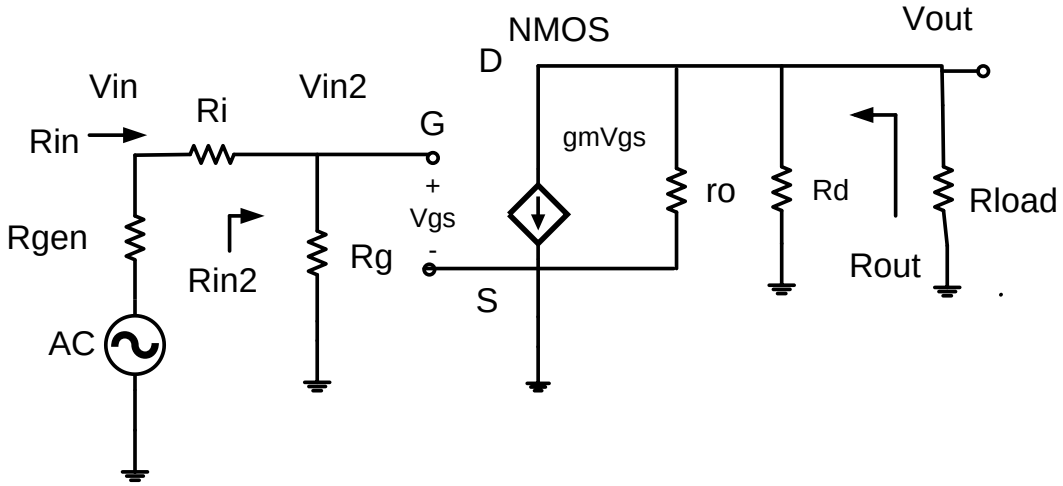
In this configuration, R_S is bypassed with Cs. The circuit diagram with necessary variables is provided in CS Fig.1.



CS Figure 1: MOSFET Common Source



CS Figure 2: MOSFET characteristics, Example not your Q-point



CS Figure 3: Common Source Small Signal Equivalent Circuit

CS Part 1: Measure the device parameters

For the design of the amplifier, the 3 parameter values required are r_o and gm. Derived from the transistor characteristics curve shown in CS Fig.2, one can set an approximate Q-point (V_{DS} and I_D) in the active region and measure ro and gm. We will solve for V_{DS} and estimate ID.

Solve for V_{DS} see below.

For an approximate I_D Q-point use $I_D \approx 2.2 * I_{load}$ this is not the solution to your design Q-point. We can use an approximate I_D because ro and gm will not very much with small changes in Q-point.

ro = $\Delta V_{DS} / \Delta I_D$ the slope of a line thru Q-point

gm = $\Delta I_D / \Delta V_{SG}$ measured around Q-point

Plot the estimated Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves estimate VDSsat the point where the curve begins to flattens out ≈ 1 Vdc

CS Part 2: Determine the Q-point.

Start with your MOSFET determine the Q-pint and select the bias 4 resistors.

CS Step 2.1: Choose V_S

Set V_S = between 2V to 3V. provides negative feedback DC bias

CS Step 2.2: Calculate the midpoint V_D.

Midpoint selection will allow for maximum output voltage swing.
We will add 20% to Vout so the design is not on the edge of the solution.

$V_{D(max)} = V_{DD}$ - (Vout + 20%Vout)
$V_{D(min)} = V_S + V_{DS}$ sat + (Vout + 20%Vout)
$V_D = (V_{D(max)} + V_{D(min)}) / 2$ Midpoint V_D Q-point
$V_{DS} = V_D - V_S$

CS Step 2.3: Calculate R_D.
The DC equation: $V_{DD} - V_D = V_{RD} = R_D I_D$
The AC equation: $V_{out} = i_d (R_D \parallel r_o \parallel R_L)$
Combined equation: $V_{out} = V_{RD} (r_o \parallel R_L) / (Rc + (r_o \parallel R_L))$
Rewriting to solve for R_D.
Added 20%Vout to move I_D off the edger\

$$R_D = \frac{V_{DD} - V_D}{V_{out} + 20\%V_{out}} (r_o \parallel R_L) - (r_o \parallel R_L)$$

CS Step 2.4: Calculate I_D.
$I_D = (V_{DD} - V_D) / R_D$
Thus, Q-point is (V_{DS},I_D).

CS Step 2.5: Find VSG, and V_G

Plot the Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves, find VSG.
$V_G = V_S + V_{SG}$

CS Part 3: Determine bias resistors.

CS Step 3.1: Calculate R_S.

$I_S = I_D$

$$\therefore R_S = \frac{V_S}{I_S}$$

CS Step 3.2: Calculate R_{g1}, R_{g2}. Based on required value for Rin.

Set Rin to desired value

$V_G = V_S + VSG$
Rin desired = RinW
Rin2W = RinW – Ri desired Rin2
Rg1 = (Vdd / V_G) Rin2W
Rg2 = Rg1 V_G / (Vdd – V_G)

Check Rin meets requierments
Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

CS Part 4: Calculating impedance and Gain

Refer to the small signal equivalent of the circuit you have just built in CS Fig. 3. We can calculate the following:

CS Step 4.1: Input Impedance:

Rin2 = Rg = R_{g1} || R_{g2} R_S completely bypassed
Rin = Rin2 + Ri

CS Step 4.2: Output Impedance

Rout = R_D || r_0. R_S completely bypassed i.e. Rsf = 0

CS Step 4.3: Voltage Gain AC equations
Recall Rin2 = Rg = R_{g1} || R_{g2}
Vout = - gm Vsg(Rd || ro || Rload)
Vin = ((Rin2 + Ri) / Rin2) Vin2 = (Rin/Rin2) Vin2

Vin2 = Vsg If Rsf = 0

Av2 = Vout / Vin2= - gm Vsg(Rd || ro || Rload) / Vsg

Cancel Vsg Av2 = - gm (Rd || ro || Rload)

Av = Vout / Vin = Av2 (Rin2 / Rin2 +Ri) = -(Rin2 /Rin) * gm(Rd || ro || Rload)

CS Step 4.4: Current Gain

$$\mathrm{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \mathrm{Av}\frac{\mathrm{Rin}}{\mathrm{Rload}}$$

CS Step 4.5: Power gain
G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai
In decibels G_{dB} = 10log (Av * Ai)

CS Step 4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator

CS Part 5: Frequency response

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output waveform.

First we will select C_{in}, C_{out} and C_S which jointly would set the low cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Three capacitors will introduce 3 zeros in the transfer function of the system. Because we will set 3 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1}$$

Where n is the number of poles for low frequency breakpoints at same frequency.

$$f_L = \frac{f_{C_{in}} + f_{C_{out}} + f_{C_E}}{3\sqrt{2^{\frac{1}{3}} - 1}}$$

Setting the 3 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_{CS} = f_L \sqrt{2^{1/3} - 1}$ = FL * BWshrinkage

Find the C for each breakpoint f_{Cin} , f_{Cout} , and f_{CE} where n = 3.

$$C = \frac{1}{2\pi f_C \,(\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_C

R is the Thevenin equivalent resistance seen by the capacitor.

$R_{Cs} = Rs \,||\, (ro + R_D \,||\, R_{Load}) \,||\, (1 / gm)$

The following table enlists the particular expressions.

Rsig	Rgen+Ri
C_{in}	Rsig + Rin2
Cout	Rload + Rout
C_S	$Rs \,||\, (ro + R_D \,||\, R_{Load}) \,||\, (1 / gm)$
C_{hi}	Rsig || Rin2
C_{hi2}	Rout || Rload

CS Table 1: Resistance Seen By Capacitors

C_{hi}, on the contrary, sets the higher cut-off frequency f_H which is to be set from the specified range.

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$ = FH/ BWshrinkage

Rin2 = Rg1 || Rg2

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi}\,(\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$

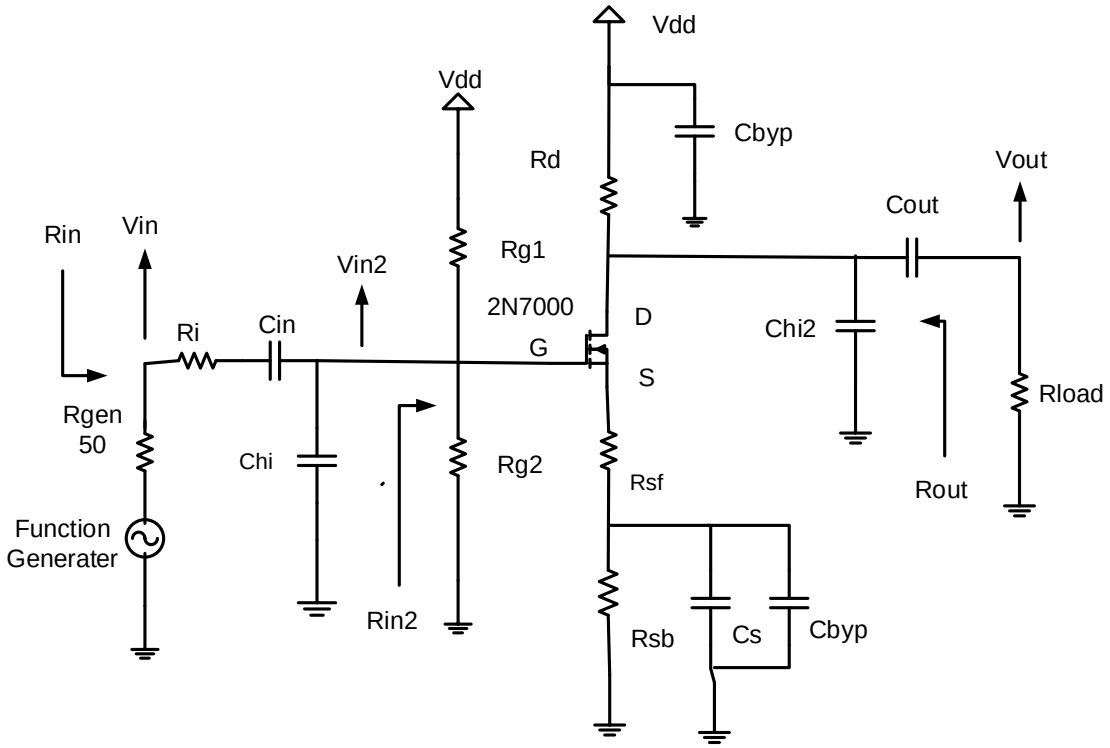
Section 2: Common Source with source degeneration (partial Rs bypassed)

Common source with source degeneration (CSwRsf)

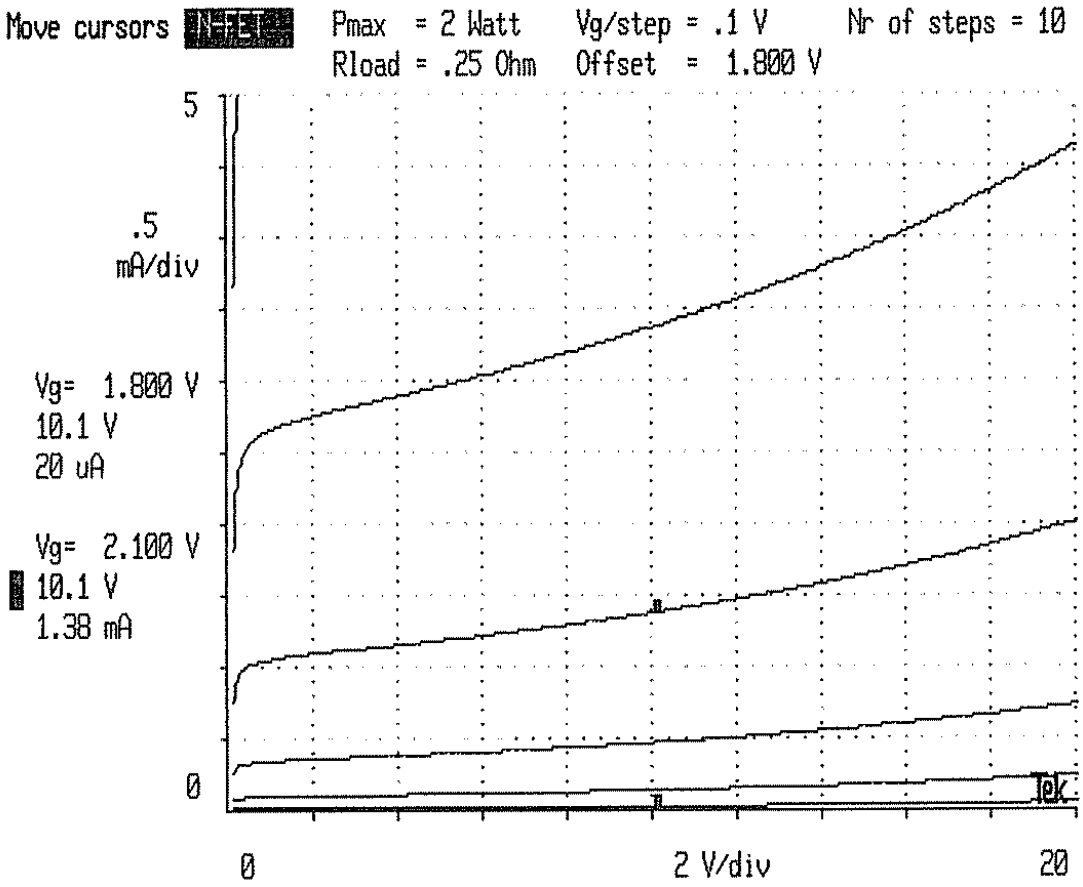
Designing procedure of common source MOSFET amplifier with source degeneration can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements, it leaves the designer enough freedom to choose the operating point as necessary for the application. However, it is to remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are fairly tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.

Common Source with Source Resistance partially Bypassed (CSwRsf)

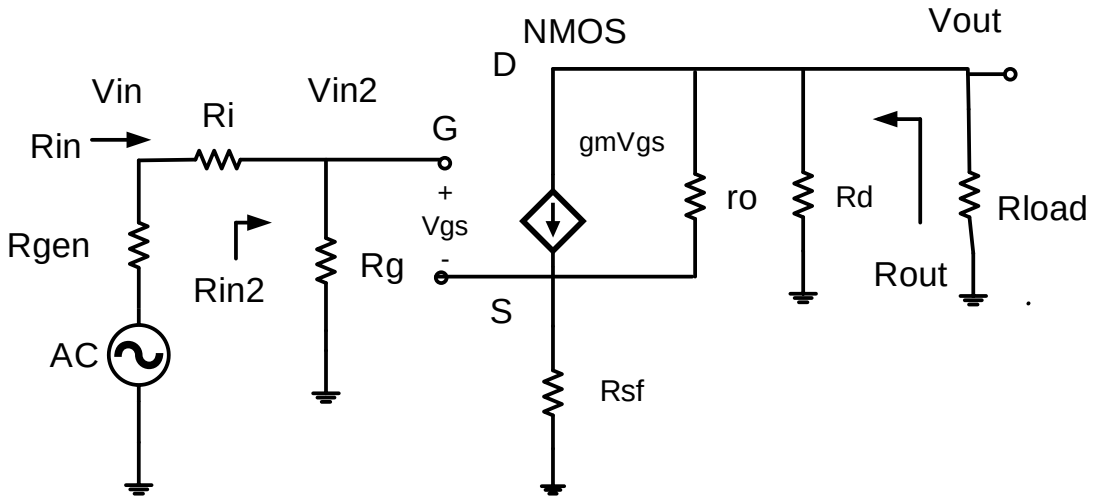
In this configuration, R_S is bypassed with Cs. The circuit diagram with necessary variables is provided in CSwRsf Fig.1.



CSwRsf Figure 1: MOSFET Common Source



CSwRsf Figure 2: MOSFET characteristics, Example not your Q-point



CSwRsf Figure 3: Common Source Small Signal Equivalent Circuit

CSwRsf Part 1: Measure the device parameters

For the design of the amplifier, the 3 parameter values required are r_o and gm. Derived from the transistor characteristics curve shown in CS Fig.2, one can set an approximate Q-point (V_{DS} and I_D) in the active region and measure ro and gm. We will solve for V_{DS} and estimate ID.

Solve for V_{DS} see below.

For an approximate I_D Q-point use $I_D \approx 2.2 * I_{load}$ this is not the solution to your design Q-point. We can use an approximate I_D because ro and gm will not very much with small changes in Q-point.

ro = $\Delta V_{DS} / \Delta I_D$ the slope of a line thru Q-point

gm = $\Delta I_D / \Delta VSG$ measured around Q-point

Plot the estimated Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves estimate VDSsat the point where the curve begins to flattens out ≈ 1 Vdc

CSwRsf Part 2: Determine the Q-point.

Start with your MOSFET determine the Q-pint and select the bias 4 resistors.

CSwRsf Step 2.1: Choose V_S

Set V_S = between 2V to 3V. To provide negative feedback in DC bias

CSwRsf Step 2.2: Calculate the midpoint V_D.

Midpoint selection will allow for maximum output voltage swing.
We will add 20% to Vout so the design is not on the edge of the solution.

$V_{D(max)} = V_{DD}$ - (Vout + 20%Vout)
$V_{D(min)} = V_S + V_{DS}$ sat + (Vout + 20%Vout)
$V_D = (V_{D(max)} + V_{D(min)}) / 2$ Midpoint V_D Q-point
$V_{DS} = V_D - V_S$

CSwRsf Step 2.3: Calculate R_D.
The DC equation: $V_{DD} - V_D = V_{RD} = R_D I_D$ Voltage across R_D
The AC equation: $Vout = i_d (R_D \| r_o \| R_L)$
Combined equation: $Vout = V_{RD} (r_o \| R_L) / (R_D + (r_o \| R_L))$
Rewriting to solve for R_D.

$$R_D = \frac{V_{DD} - V_D}{V_{out} + 20\%V_{out}} (r_o \parallel R_L) - (r_o \parallel R_L)$$

CSwRsf Step 2.4: Calculate I_D.
$I_D = (V_{DD} - V_D) / R_D$
$I_S = I_D$
Thus, Q-point is (V_{DS},I_D).

CSwRsf Step 2.5: Find DC bias V_{SG}, and V_G

Plot the Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves, find V_{SG}.
$V_G = V_S + V_{SG}$

CSwRsf Part 3: Determine bias resistors.

CSwRsf Step 3.1: Calculate R_{g1}, R_{g2}. Based on required value for Rin.

Set Rin to desired value

$V_G = V_S + V_{SG}$ DC bias point values.
Rin desired = RinW
Rin2W = RinW – Ri desired Rin2W
Rg1 = (Vdd / V_G) Rin2W
Rg2 = Rg1 V_G / (Vdd – V_G)

Check Rin meets requierments
Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

CSwRsf Step 3.2: Calculate Rsf from required gain.

$I_S = I_D$
$\therefore R_S = \frac{V_S}{I_S}$ = Rsf + Rsb total DC source resister.
Recall Rin2 = Rg = R_{g1} || R_{g2}
Vout = - gm Vsg(R_D || Rload || (r_o + Rsf || 1/gm)

Vin = ((Rin2 + Ri) / Rin2) Vin2

Vin2 = Vsg + v_s AC voltage signal.
Vin2 = Vsg + (gm Vsg) * Rsf = Vsg (1 +gm Rsf)

Av2 = Vout / Vin2 = (- gm Vsg(R_D || (r_o + (Rsf || 1/gm)) || Rload)) / Vsg (1 +gm Rsf)
Cancel Vsg Av2 = (- gm (R_D || (r_o + (Rsf || 1/gm)) || Rload)) / (1 +gm Rsf)

Av = Av2 (Rin2 / (Rin2 +Ri))

Av = Vout / Vin =(Rin2 / (Rin2 + Ri)) * (- gm(R_D || (r_o +(Rsf || 1/gm)) || Rload) / (1 +gm Rsf))

Rearrange Av = - gm (Rin2/(Rin2 + Ri)) * (R_D || Rload || (r_o + (Rsf || 1/gm)) / (1 + gm Rsf)

1 +gm Rsf = - gm (Rin2/(Rin2 + Ri)) * (Rd || Rload || (r_o + (Rsf || 1/gm))) / Av

Note: Av is negative.

Rsf = -((Rin2/(Rin2 +Ri)) * (Rd || Rload || (r_o + (Rsf || 1/gm))) / Av)) - 1 / gm

We do not have Rsf yet so we will approximate the term

ro + Rsf || 1/gm ≈ ro

Yielding **Rsf** = ((Rin2/(Rin2 + Ri)) * (Rd || Rload || r_o)) / Av) - 1/gm

CSwRsf Step 3.2: Calculate R_{g1}, R_{g2}. Based on required value for Rin.
Set Rin to desired value

$V_G = V_S + V_{SG}$ DC bias point values.
Rin desired = RinW
Rin2W = RinW – Ri desired Rin2W
Rg1 = (Vdd / V_G) Rin2W
Rg2 = Rg1 V_G / (Vdd – V_G)

Check Rin meets requierments
Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

CSwRsf Part 4: Calculating impedance and Gain

Refer to the small signal equivalent of the circuit you have just built in CS Fig. 3. We can calculate the following:

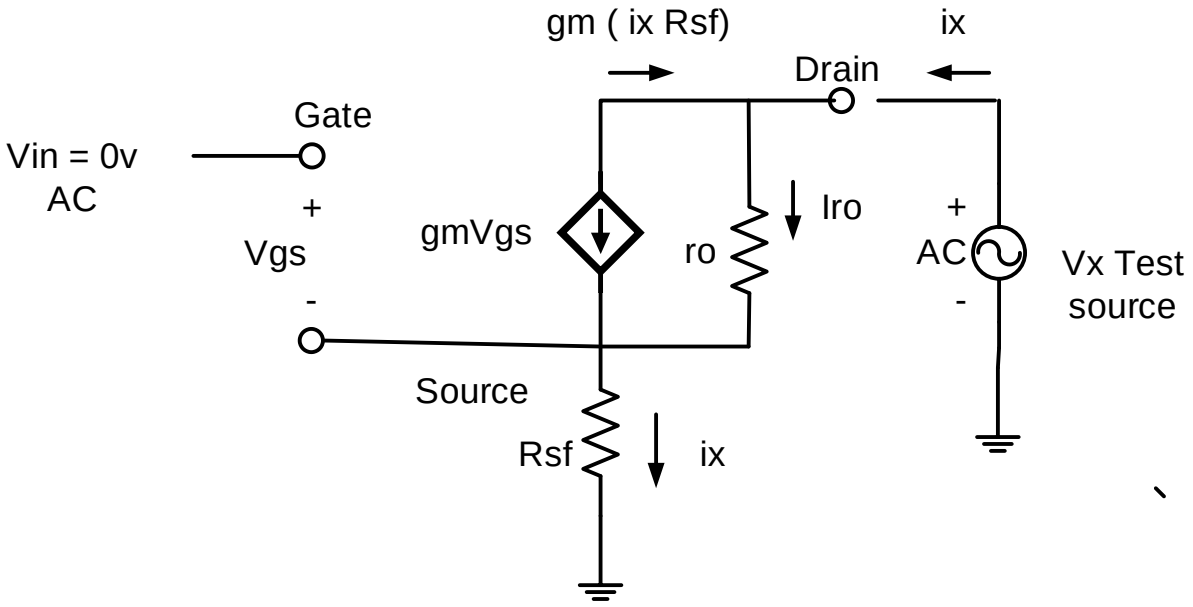
CSwRsf Step 4.1: Input Impedance:

Rin2 = Rg = R_{g1} || R_{g2}
Rin = Rin2 + Ri

CS wRsf Step 4.2: Output Impedance

Derivation of the equation for the resistance looking into the drain.

I_x current from the test voltage v_x applied to the Drain of MOSFET we will ignore Rd for now.



CSwRfs Figure 4: Small signal equivalent circuit Drain resistance.

$V_{sg} = - i_x R_{sf}$ V_{sg} caused by applied test voltage, v_g gate voltage = 0v (AC signal voltage).

$- gm(- i_x R_{sf})$ Current in the dependent source of MOSFET (AC signal current)

Current flowing thru r_o $i_{ro} = i_x - gm(- i_x R_{sf}) = i_x + gm\ i_x R_{sf}$

$V_x = r_o (i_x + gm\ i_x R_{sf}) + i_x R_{sf}$ divide thru by i_x

The equation for the resistance looking into MOSFET Drain.

$V_x / i_x = r_o (1 + gm R_{sf}) + R_{sf} = ro + ro\ gm R_{sf} + R_{sf}$

Now apply Rd in parallel with impedance looking into MOSFET Drain.

$R_{out} = Rd \parallel (r_o (1 + gm R_{sf}) + R_{sf}) = Rd \parallel (ro + ro\ gm R_{sf} + R_{sf})$

CSwRsf Step 4.3: Voltage Gain calculated

Recall Rin2 = Rg = R_{g1} || R_{g2}
Vout = - gm Vsg (AC load) = - gm Vsg(R_D || Rload || (ro + ro gm Rsf + Rsf))
Vin = (Rin2 + Ri / Rin2) Vin2
Vin2 = Vout / Av2
Vin2 = Vsg + v_s AC voltage signals.

i_s = gm * Vsg AC signal current not bias current Is

Vin2 = Vsg + Rsf * i_s = Vsg + Rsf(gm * Vsg) = Vsg (1 +gm Rsf)

Av2 = Vout / Vin2 = = - gm Vsg(R_D || Rload || (ro + ro gm Rsf + Rsf)) / Vsg (1 +gm Rsf)

Av = Vout / Vin = - ((Rin2/(Rin2 + Ri)) * gm Vsg(R_D || Rload || (ro + ro gm Rsf + Rsf)) / Vsg (1 +gm Rsf)

Rearrange Av = - gm((Rin2/(Rin2 + Ri)) (R_D || Rload || (ro + ro gm Rsf + Rsf)) / (1+ gm Rsf)

This is the calculated value for Av using the components that we selected.

Av = Vout / Vin = - gm ((Rin2/(Rin2 + Ri)) (R_D || Rload || (ro + ro gm Rsf + Rsf)) / (1+ gm Rsf)

This gain will be higher than out design value because we made an approximation in step CSwRsf Step 3.2 above for finding Rsf. r**o + Rsf || 1/gm ≈ ro**

CSwRsf Step 4.4: Current Gain

$$\mathrm{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \mathrm{Av}\frac{\mathrm{Rin}}{\mathrm{Rload}}$$

CSwRsf Step 4.5: Power gain
G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai
In decibels G_{dB} = 10log (Av * Ai)

CSwRsf Step 4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator

CSwRsf Part 5: Frequency response

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output waveform.

First we will select C_{in}, C_{out} and C_S which jointly would set the low cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Three capacitors will introduce 3 zeros in the transfer function of the system. Because we will set 3 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1}$$

Where n is the number of poles for low frequency breakpoints at same frequency.

$$f_L = \frac{f_{C_{in}} + f_{C_{out}} + f_{C_E}}{3\sqrt{2^{\frac{1}{3}} - 1}}$$

Setting 3 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_{CS} = f_L \sqrt{2^{1/3} - 1}$ = FL * BWshrinkage

Find the C for each breakpoint f_{Cin} , f_{Cout} , and f_{CE} where n = 3.

$$\text{C} = \frac{1}{2\pi f_C \,(\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_C

R is the Thevenin equivalent resistance seen by the capacitor.

R_{Cs} = Rsb || (Rsf + (ro + R_D || R_{Load}) || (1 / gm))

The following table enlists the particular expressions.

Rsig	Rgen+Ri
C_{in}	Rsig + Rin2
Cout	RL + Rout
C_S	Rsb || (Rsf + (ro + (R_D || R_{Load})) || (1 / gm))
C_{hi}	Rsig || Rin2
C_{hi2}	Rout || Rload

CSav Table 1: Resistance Seen By Capacitors

C_{hi}, on the contrary, sets the higher cut-off frequency f_H which is to be set from the specified range.

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$ = FH / BWshrinkage

Rin2 = Rg1 || Rg2

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi}\,(\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$

Section 3: Common Drain (CD)

Designing procedure of common drain MOSFET amplifier can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements, it leaves the designer enough freedom to choose the operating point as necessary for the application. However, it is to remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are fairly tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.

For common drain configuration, the circuit diagram in CD Fig.1. The small signal equivalent model in CD Fig.3.

For this configuration, same steps are involved for the calculation of Rg1, Rg2 and R_S with few minor changes. Note that R_D is absent in this case and we have added an isolation resister Riso because of the capacitive loading of Chi2.

CD Part 1: Measure the device parameters

CD Step 1.1: We need to estimate a Q-point to find an estimate for Vdssat, ro and gm.

For the design of the amplifier, the 3 parameter values required are r_o and gm. Derived from the transistor characteristics curve shown in CD Fig.2, one can set an approximate Q-point (V_{DS} and I_D) in the active region and measure ro and gm. We will solve for V_{DS} and estimate I_D.

Solve for V_{DS} see below.

For an estimated I_D Q-point use $\mathbf{I_D \approx 3^* I_{load}}$ this is not the solution to your design Q-point. We can use an estimated I_D because ro and gm will not very much with small changes in Q-point.

ro = $\Delta V_{DS} / \Delta I_D$ the slope of a line thru the estimated Q-point

gm = $\Delta I_D / \Delta$VSG measured around the estimated Q-point

Plot the estimated Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves CD Fig. 2 estimate V_{DS}sat the point where the curve begins to flattens out ≈ 1 Vdc

CD Part 2: Find the Q-point

CD Step 2.1: Derive Vs Q- point

We will start with V_S(max) and V_S(min).

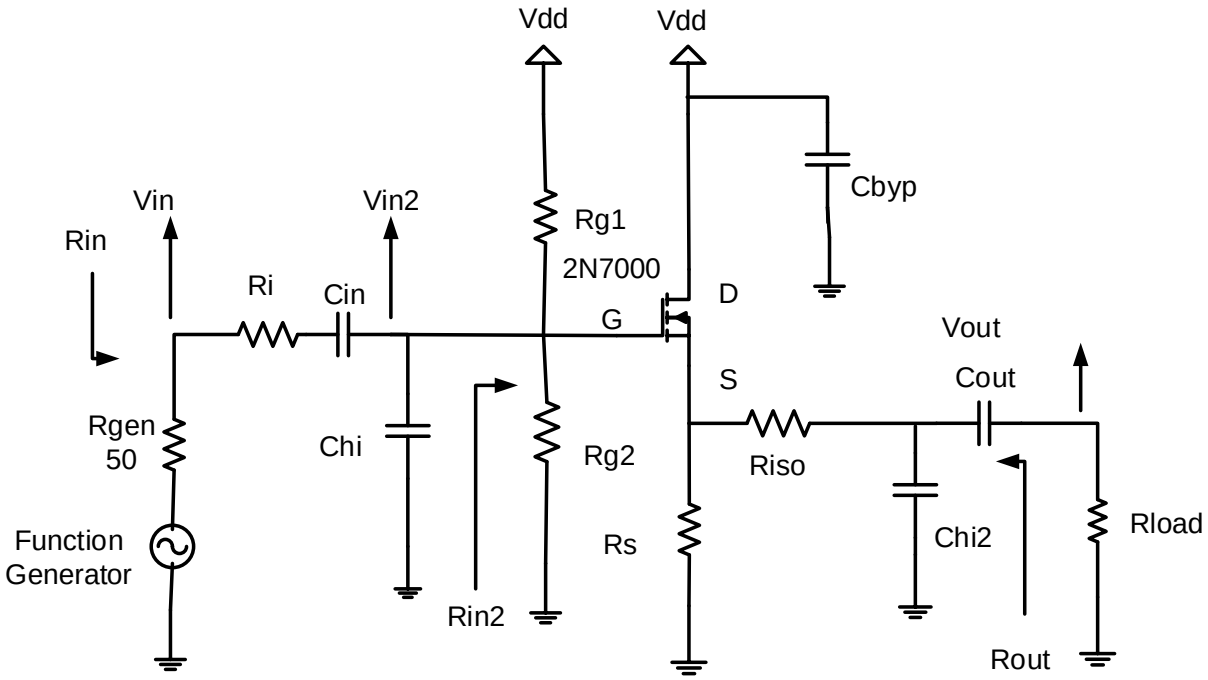
VoutSource = Vout + I_{Load} * Riso Vout at the source

V_S(max) = Vdd – V_{DS}sat – (VoutSource + 20%VoutSource)

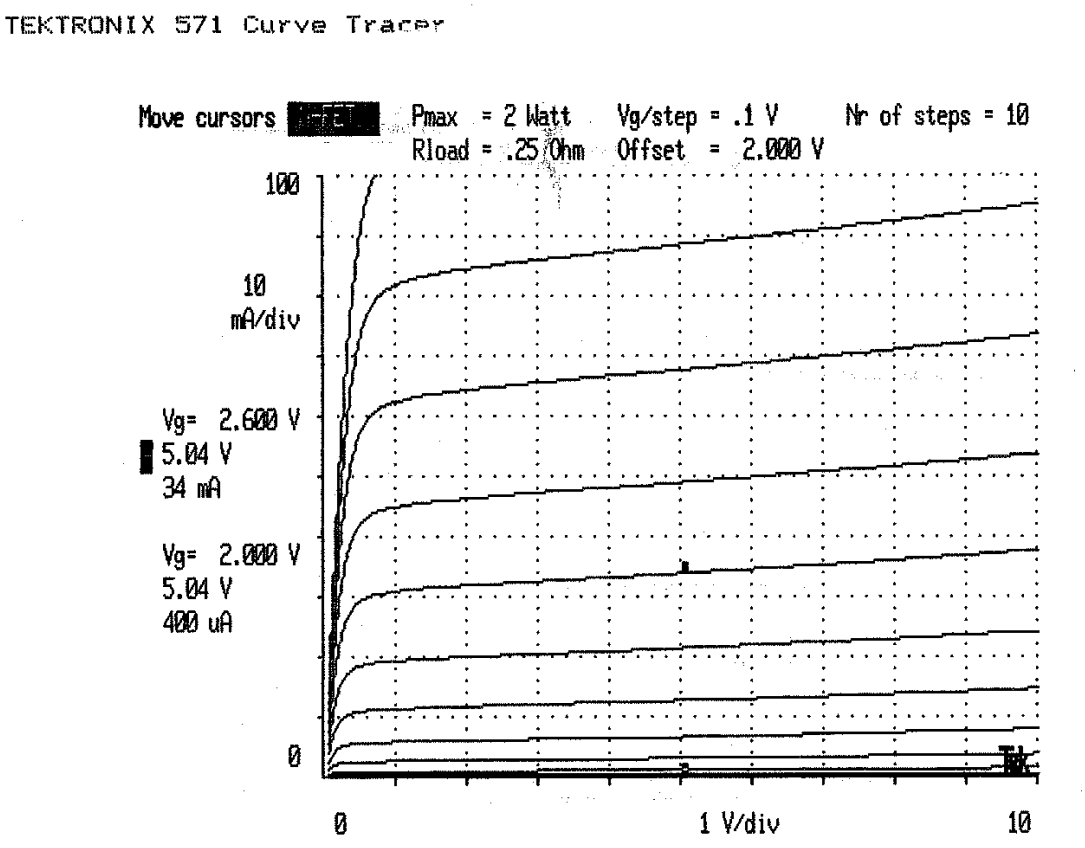
V_S(min) = VoutSource + 20% VoutSource

$V_S = (V_S(max) + V_S(min)) / 2$ Midpoint V_S Q-point

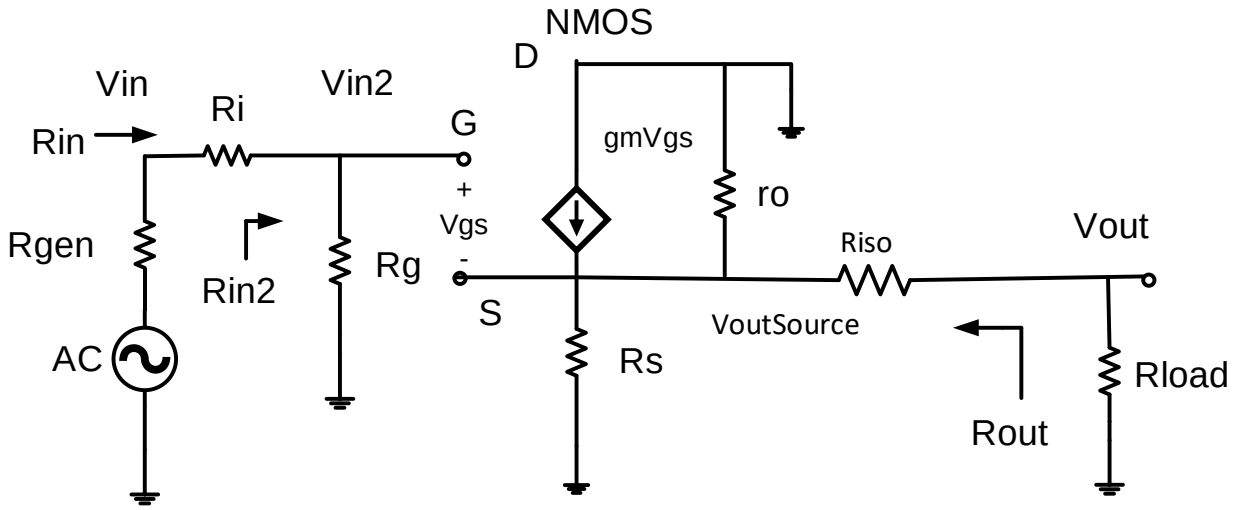
$V_{DS} = V_D – V_S$



CD Figure 1: MOSFET Common Drain CD configuration



CD Figure 2: CD MOSFET curve.



CD Figure 3: Small signal equivalent model for common drain model

CD Part 3: Determine bias resistors

CD Step 3.1: Now find the value of R_S and I_S

We need a higher VoutSource then Vout because of voltage divider Riso, Rload.

VoutSource = Vout * (Rload + Riso) / Rload = Vout + ILoad * Riso

The DC equation: $V_S = V_{RS} = R_S I_S$

The AC equation: $VoutSource = i_s (R_S \parallel r_o \parallel (R_{Load} + Riso))$

Combined equation: $VoutSource = V_s (r_o \parallel (R_{Load} + Riso)) / (Rs + (r_o \parallel (R_{Load} + Riso)))$

$R_S = \frac{V_S}{V_{out}Source + 20\% V_{out}\,Source} (r_o \parallel (R_L + Riso)) - (r_o \parallel (R_L + Riso))$ Rearrange combined equation

Calculate Is

$I_S = I_D = V_S / R_S$

CD Step 3.2: Calculate R_{g1}, Rg_2. Set Rin to desired value

$V_G = V_S + V_{SG}$

Rin desired = RinW

Rin2W = RinW – Ri

Rg1 = (Vdd / V_G) Rin2W

Rg2 = Rg1 Vg / (Vdd – Vg)

Check Rin meets requirements

Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

Rout = (Rs || ro || (1 / gm)) + Riso

CD Part 4: Calculate Rin, Rout, Av, and Ai

CD Step 4.1: Input Impedance:

Rin2 = Rg = R_{g1} || R_{g2}
Rin = Rin2 + Ri

CD Step 4.2: Output Impedance

Rout = (Rs || ro || (1 / gm))+ Riso

CD Step 4.3: Calculation of Av Voltage Gain

Referring to CD Fig.3, let us find $\frac{v_{out}}{v_{in}}$ which would be a key step in calculating Av.

Rin = Ri + Rin2

Rin2 = Rg = Rg1 || Rg2

Rout = (Rs || ro || (1 / gm)) + Riso Looking into the CD amp output.

VoutSource = gm Vsg (Rs || ro || (Rload + Riso)) Voltage across Rload + Riso.

Vout = VoutSource * (Rload / (Rload + Riso)) Voltage divider to Vout from VoutSource.

Voltage at the function generator Vin = Vin2 (Rin / Rin2)

Voltage at the Gate Vin2 = Vsg + VoutSource AC equation.

Vin2 = Vsg + gm Vsg (Rs || ro || (Rload + Riso)) = Vsg (1 +gm(Rs || ro || (Rload + Riso)))

Av3 = VoutSource / Vin2= gm (Rs || ro || (Rload+ Riso)) / (1 +gm(Rs || ro || (Rload+ Riso))

Av = Vout / Vin = (Rin2 / Rin) * (Rload / (Rload +Riso)) * Av3

Thus, the voltage gain should be close to 1. Hence, the output follows the input. So, the Common Drain configuration is known as Source follower.

CD Step 4.4: Current Gain

$$\mathrm{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \mathrm{Av}\frac{\mathrm{Rin}}{\mathrm{Rload}}$$

CD Step 4.5: Power gain

G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai

In decibels G_{dB} = 10log (Av * Ai)

CD Step 4.6: Vin and Voc of Vgen

Input signal level need to produce the required output voltage.

Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.

Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator

CD Part 5: Frequency response.

The capacitor values can be calculated as before, the only difference being *n* = 2 for low pass calculations since we are using two capacitors instead of 3.
With the Q-point set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output waveform.

First we will select C_{in}, and C_{out} which jointly would set the roll-off beyond the lower cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Two capacitors will introduce 2 zeros in the transfer function of the system. Because we will set 2 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\mathrm{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1} \qquad \mathrm{n} = 2$$

Where n is the number of zeros for low frequency breakpoints at same frequency.

Setting 2 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_L \sqrt{2^{1/2} - 1}$ = FL * BWshrinage

Find the C for each breakpoint f_{Cin} , and f_{Cout} , where n = 2.

$$C = \frac{1}{2\pi f_C \, (\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_C

R is the Thevenin equivalent resistance seen by the capacitor.

The following table enlists the particular expressions.

Rsig	Rgen+Ri
C_{in}	Rsig + Rin2
Cout	R_{Load} + Rout
C_{hi}	Rsig || Rin2
Chi2	Rout || Rload

CD Table 1: Resistance Seen By Capacitors

Chi, and Chi2 on the contrary, sets the high cut-off frequency f_H which is to be set from the specified range.

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$ = FH / BWshrinkage

Rin2 = Rg1 || Rg2

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi} \, (\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload

$$C_{hi2} = \frac{1}{2\pi f_{Chi2} \, (\text{R seen by } C_{hi2})}$$