TECHNICAL BRIEF

RISC-V and Open Source Hardware Address New Compute Requirements

Prepared by:
Western Digital

RISC-V®

About Western Digital

Western Digital is a leader in data infrastructure. The company is driving the innovation needed to help customers capture, preserve, access and transform an ever-increasing diversity of data. Everywhere data lives, from advanced data centers to mobile sensors to personal devices, our industry-leading solutions deliver the possibilities of data. Our data-centric solutions are marketed under the G-Technology™, SanDisk®, WD®, and Western Digital® brands.

Why RISC-V?

The existing general purpose processing solutions are hamstrung from their legacy architectures. As compute requirements continue to expand, a clean slate approach to processing is now required. RISC-V is an open instruction set architecture (ISA) that has broad industry support to address the compute needs for today's processing challenges. To make RISC-V based devices a reality, an open and collaborative environment is highly desirable. Along with other leading semiconductor companies, Western Digital joined CHIPS Alliance to develop open source hardware designs and software development tools. Learn more at https://chipsalliance.org.

Western Digital RISC-V Hardware Innovation and Development

RISC-V CPU Cores

In 2019, Western Digital developed and open-sourced through CHIPS Alliance a super-scalar (2-way), 9-stage pipeline, mostly in-order, open-source core based on the RISC-V RV32IMC instructions set, named SweRV Core EH1. See further details at https://www.westerndigital.com/risc-v. This core was designed to target datapath controller applications for NAND flash. Customers who are interested in commercial support of the SweRV Core EH1 can visit http://www.codasip.com/swerv.

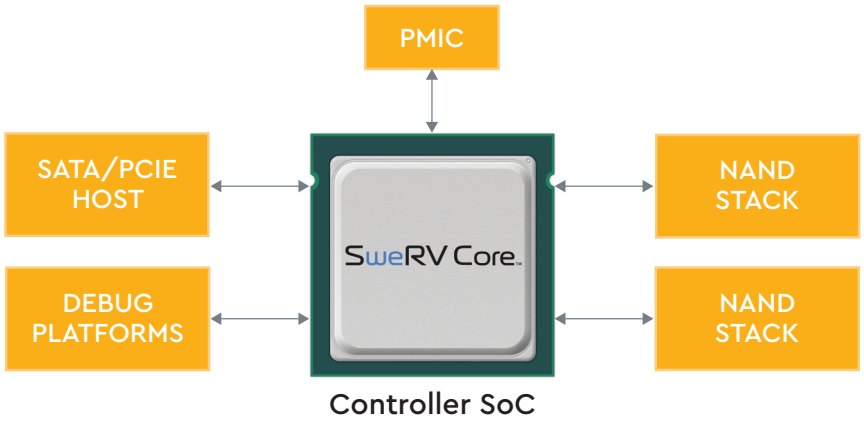

Figure 1: Storage Controller Block Diagram

Western Digital now has developed the SweRV Core EH2 and SweRV Core EL2. SweRV Core EH2 is a multi-threaded version of EH1 that supports Simultaneous Multi-Threading (2 threads) on top of the superscalar architecture of SweRV EH1. The host software can simultaneously run two RISC-V threads at one time. The EH2 introduces two sets of RISC-V Architecture Register Files and doubles microarchitectural resources such as fetch buffers, instruction buffers, commit logic and so on. Most of the pipeline follows the EH1 superscalar 9-stage pipeline, leading to an implementation size that is only incremental to EH1. In essence, the host software sees "2 cores" for the price of one. The multi-threaded design will typically offer superior compute density when the code has numerous "IO" operations with high latency. The simulated combined Coremark performance for dual threaded operation is 6.3 CM/MHz.

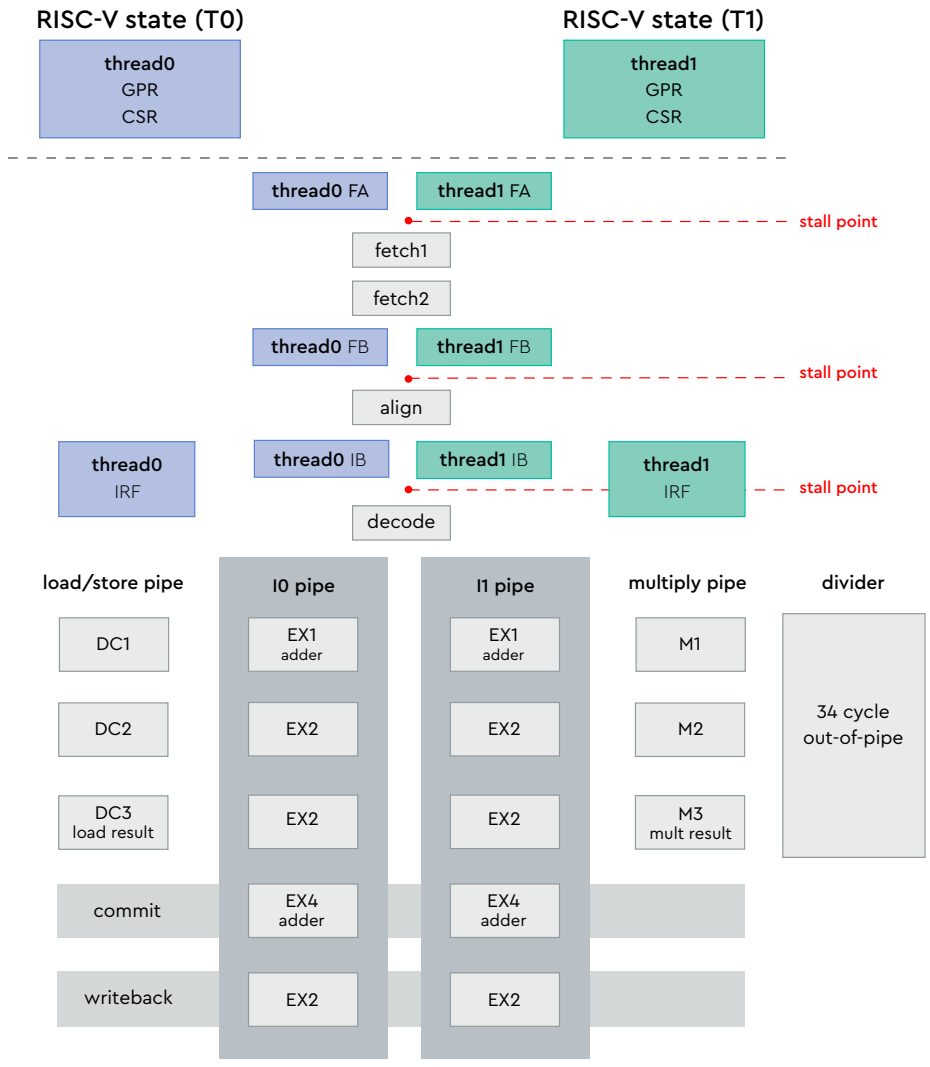

Figure 2: SweRV Core EH1 and EH2 pipeline. The green and blue boxes only apply to the SweRV Core EH2

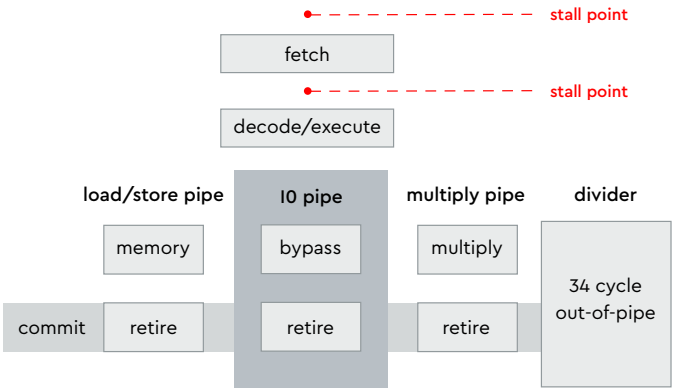

Figure 3: SweRV Core EL2 pipeline

The SweRV Core EL2 is a ultra-low power 4-stage, single issue pipeline, optimized for maximum performance to power ratio. SweRV EL2 is a general purpose embedded core targeting a variety of applications inside a typical SoC: state-machines sequencers and waveform generators for example. The coremark score for this core in simulations is 3.6 CM/MHz. To download any of the SweRV Cores, visit https://github.com/chipsalliance/Cores-SweRV.

RISC-V ISA Enhancements LR/SC

Western Digital leadership, in cooperation with other RISC-V members, has resolved long-standing issues with RISC-V load-reserve/store-conditional (LR/SC)behavior. The RISC-V LR/SC had strong, per thread forward-progress properties, which were hard to implement, and scaled poorly for many applications. The updated specification now resembles LR/SC forward-progress properties in other architectures. This change will greatly simplify implementation of RISC-V in many-core systems.

RISC-V and Security: Open Titan

opentitan

With its foundations in open source, RISC-V provides the perfect building block to enable the future of trustworthy secure processors. One such processor, named Open Titan, is a RISC-V based silicon root of trust. It is currently being developed under the LowRISC banner with Western Digital playing a leading role in its design and implementation. Our contributions will include hardware IP, software and firmware implementation of various security protocols. One of the primary use cases for Open Titan will be a root of trust integrated within the system on chip for a storage device controller. Further details are available at https://github.com/lowRISC/opentitan.

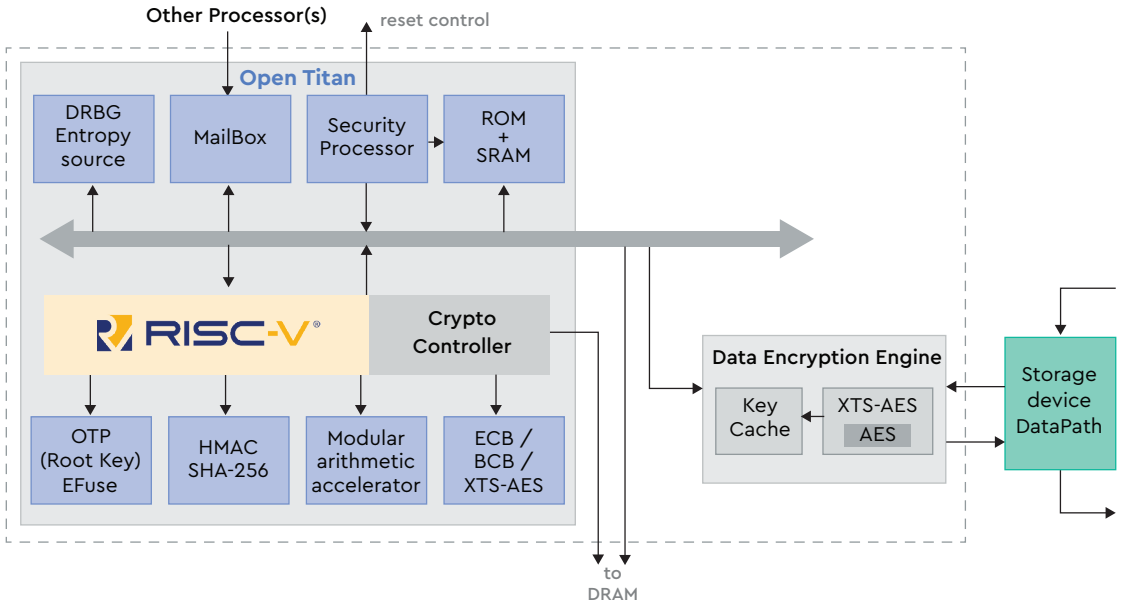

Figure 4: Open Titan Block Diagram

Western Digital RISC-V Software Innovation and Development

Open Source Software and RISC-V Ecosystem

RISC-V needs a complete software ecosystem surrounding it in order to thrive. The components of the ecosystem are very diverse, spreading across all layers from low level firmware and boot loaders up to a fully functional operating system kernel and applications. Each of these components is important to ensure the success of RISC-V and the power of open source contributions accelerates the build out.

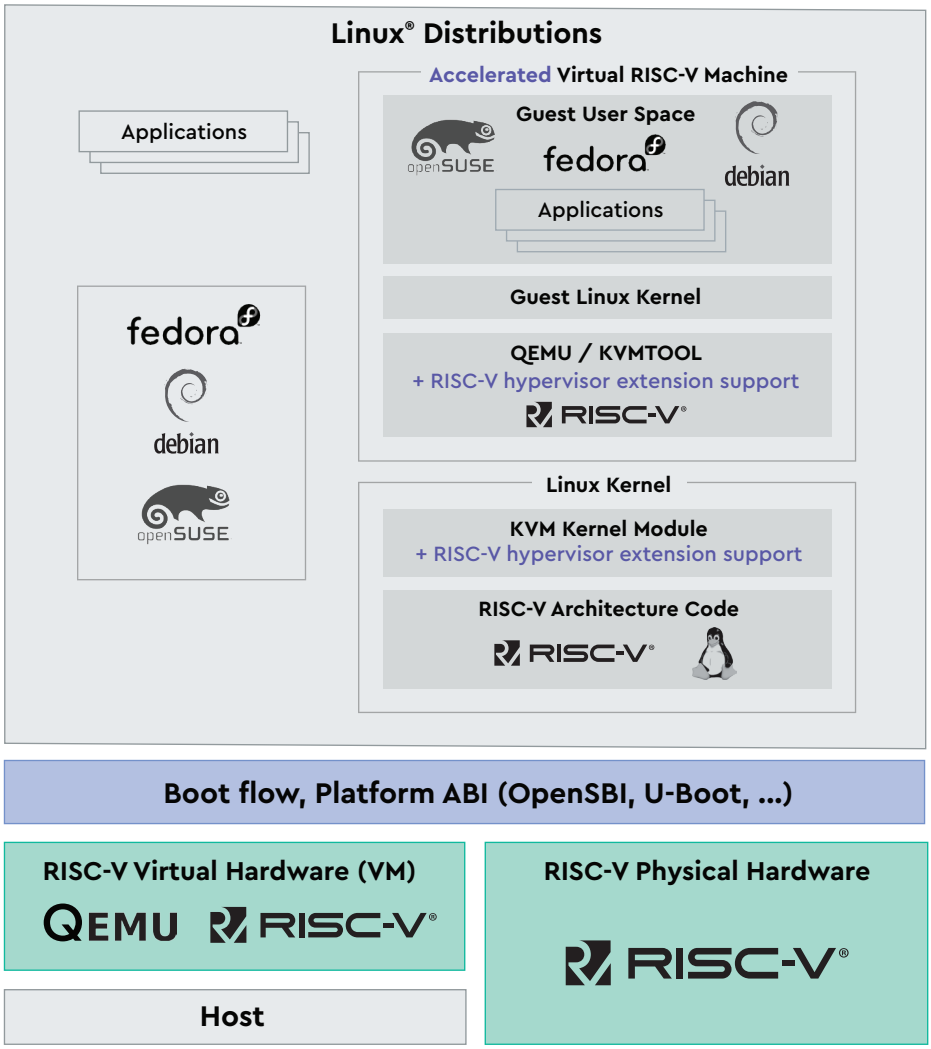

Figure 5: Linux Kernel-based RISC-V Virtual Machine (KVM) with hardware acceleration provided by RISC-V Hypervisor ISA extensions

To help encourage innovation in the ecosystem, Western Digital has made numerous contributions to the Linux® community. This includes contributions to the upstream Linux kernel, to the U-Boot boot loader project and the release of the OpenSBI project. These contributions enable Linux distributions such as Fedora, OpenSUSE and Debian to support RISC-V hardware and help to achieve a boot process similar to other architectures (e.g. x86, ARM).

Western Digital activity contributed to a working implementation of the RISC-V hypervisor extension support in Linux to help with validating the specifications and provide a test environment for hardware vendors. This implementation in QEMU and the Linux kernel now enables running a Linux Kernel-based Virtual Machine (KVM) guest with hardware acceleration, putting RISC-V on par with the most advanced enterprise class processors. Further details are available at https://github.com/kvm-riscv.

RISC-V Code Density

The RISC-V ISA has been designed as a simple and small instruction set, which also supports compressed instructions ("C" extension). However, the maturity of compilers for RISC-V has not been fully developed. Currently GCC emitted code density is 10–20% behind other instruction set architectures. Western Digital did analysis on GCC-RISC-V compiler results and came up with specific examples where GCC can be improved. The patches were submitted to GNU upstream to be part of GCC for RISC-V target. Alongside the GCC patches Western Digital supports upstreaming a new technique to find the "best optimization flags" to give the smallest code footprint. Lastly, with the usage of link-time-optimization (LTO), we can decrease the size of the original code by ~20%. See figure 6.

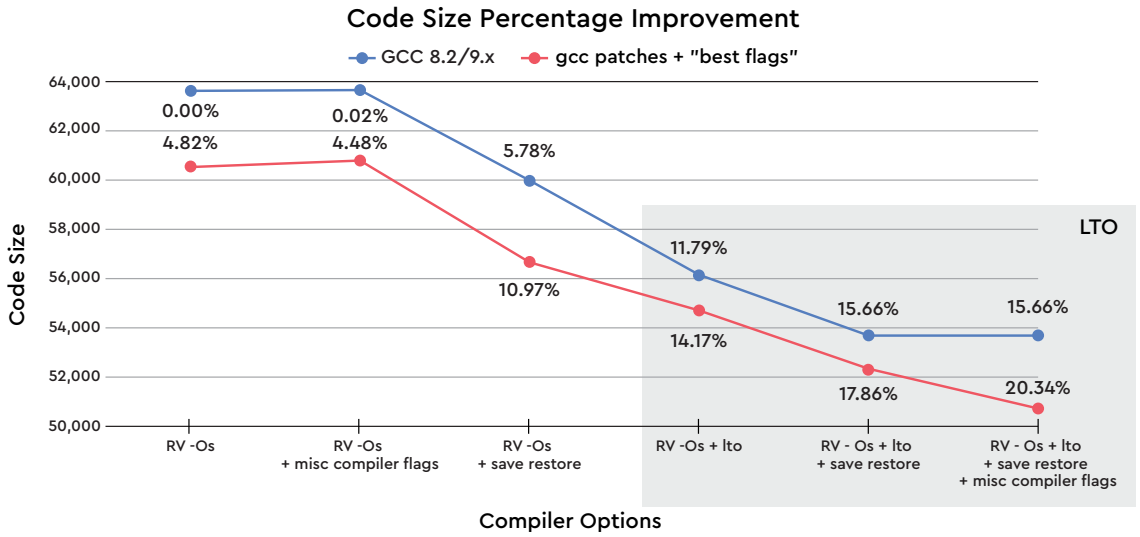

Figure 6: Plot of compiler options and code size showing the RISC-V Code Density Improvement

Western Digital System Innovation and Development

OmniXtend™: Direct to Caches over Commodity Fabric

With the increasing adoption of RISC-V in numerous different processor microarchitectures, there is an urgent need for the RISC-V ecosystem to have a common scale-out protocol for the cache coherency bus. OmniXtend is the first cache coherent memory technology providing open-standard interfaces for memory access and data sharing across a wide variety of processors, FPGAs, GPUs, machine learning accelerators, and other components. With an open cache coherency bus, heterogeneous devices can now access main memory.

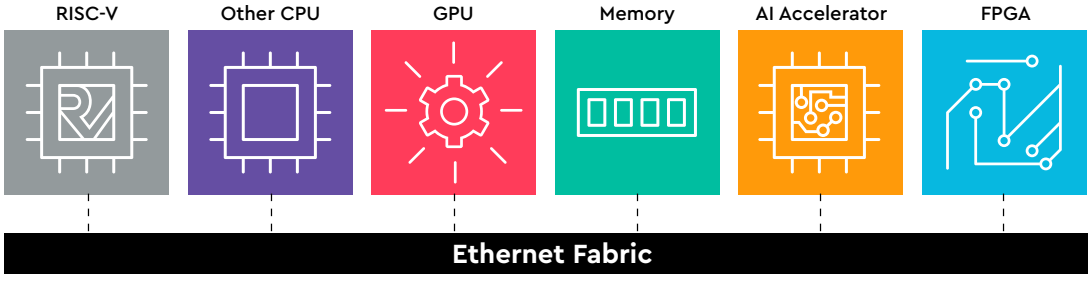

Figure 7: OmniXtend allows main memory to be equally shared over Ethernet

Western Digital's OmniXtend is an open cache coherence protocol utilizing the programmability of modern Ethernet switches to enable processors' caches, memory controllers and accelerators to exchange coherence messages directly over an Ethernet-compatible fabric. OmniXtend builds upon the TileLink coherence protocol, to scale beyond the processor chip. The programmability of OmniXtend dataplane allows future improvements to the protocol to be deployed immediately in the field, without requiring new system software or new ASICs.

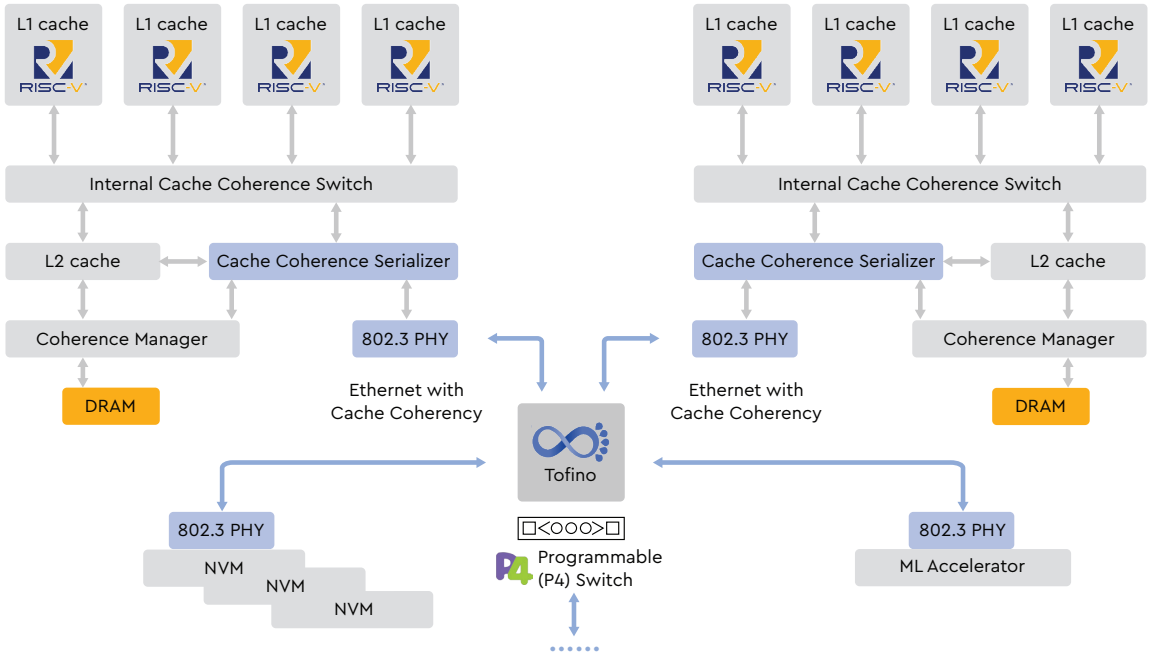

Figure 8: System block diagram for OminiXtend

For further details on OminiXtend, please go to https://www.westerndigital.com/risc-v.

Future development on OmniXtend will be done in CHIPS Alliance. See more at https://github.com/chipsalliance/omnixtend.

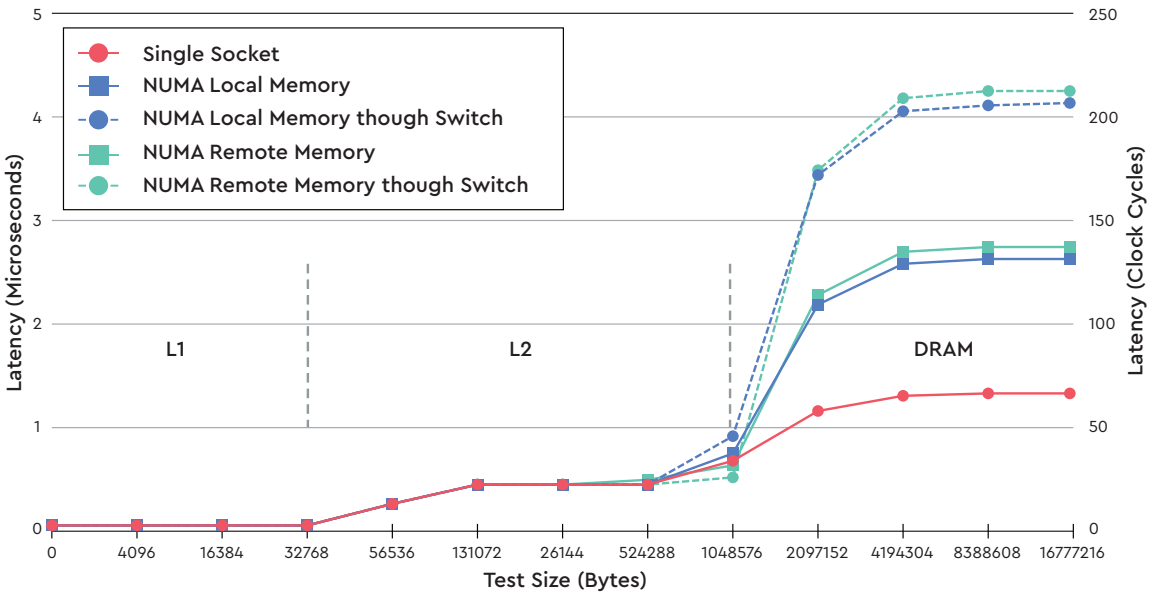

Figure 9: Latency measurements demonstrate the performance of OmniXtend architecture on an FPGA prototype system running at 50 MHz

Academic Engagements in Support of RISC-V Ecosystem

Western Digital partners with numerous prestigious universities around the globe to understand new and emerging computational use cases and develop appropriate purpose-built solutions for each major application. We see the RISC-V ISA as a key enabler of this strategy. Western Digital has partnered with the India Institute of Technology (IIT) in Madras and the Indian Institute of Science (IISC) in Bangalore. The goal of these two engagements is to develop course material for multiple undergraduate and graduate level courses related to RISC-V as well as to create appropriate toolchains in support of all stages of design and verification of the RISC-V ISA. These materials are to be made fully available to the community.

Looking Ahead

To realize the possibilities of data, we need to capture, preserve, access, and transform it to its full potential. The extreme data-centric environments of tomorrow's applications require purpose-built environments that support independent scaling of data transformation resources in an open manner.

Western Digital is committed to the mission of the RISC-V Foundation and its ecosystem, and together, we can create environments for data to thrive. When data thrives, our people, communities and planet can thrive, all through the power, potential and possibilities of data.

Keep up with Western Digital RISC-V activities
by visiting www.westerndigital.com/risc-v

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Forward-looking Statements

This document contains forward-looking statements that involve risks and uncertainties, including, but not limited to, statements regarding our product and technology positioning, the anticipated benefits of our new technologies and transitioning into RISC-V open instruction set architectures. Forward-looking statements should not be read as a guarantee of future performance or results, and will not necessarily be accurate indications of the times at, or by, which such performance or results will be achieved, if at all. Forward-looking statements are subject to risks and uncertainties that could cause actual performance or results to differ materially from those expressed in or suggested by the forward-looking statements.

Additional key risks and uncertainties include the impact of continued uncertainty and volatility in global economic conditions; actions by competitors; difficulties associated with go-to-market capabilities and transitioning into RISC-V open instruction set architectures; business conditions; growth in our markets; and pricing trends and fluctuations in average selling prices. More information about the other risks and uncertainties that could affect our business are listed in our filings with the Securities and Exchange Commission (the "SEC"). and available on the SEC's website at www.sec.gov, to which your attention is directed. We do not undertake any obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future developments or otherwise, except as otherwise required by law.

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