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Robustness and reliability aspects of SiC power devices

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Agenda

1. SiC reliability: gate oxide, cosmic ray aspects and body diode performance
2. SiC Product release process and robustness validation approach
3. Key takeaways

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SiC reliability: gate oxide aspects

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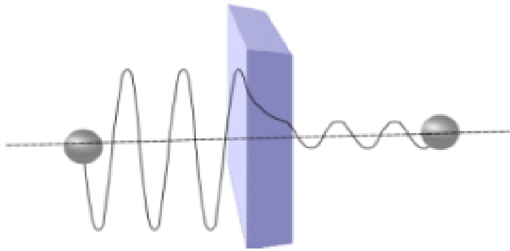
Gate oxide (GOX) requires special attention in SiC MOSFETs

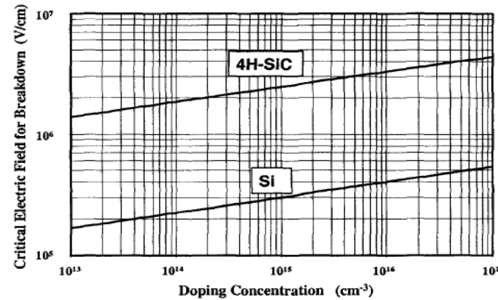
SiC has a larger bandgap
(1.1 eV Si vs. 3.2 eV SiC)



Enhanced tunneling

Less relevant for FIT rates under nominal operating conditions

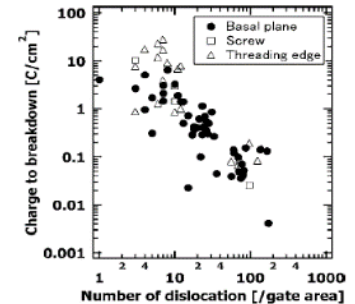
SiC has higher blocking capability
(0.3 MV/cm Si vs. 3.0 MV/cm SiC)



Higher fields in blocking state

GOX stress induced by V_{DS} in blocking mode as well

SiC has higher defect density in substrate and in GOX



Higher risk of early GOX breakdown

Measures to sort out affected devices required to meet FIT rates

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Oxide in SiC MOSFET devices

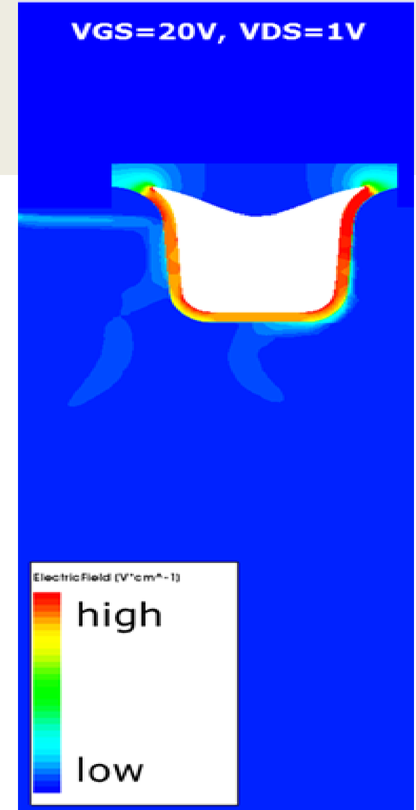
Stressed by electric fields in on- and off-state

Oxide reliability in SiC:

Especially critical in **on-state**,
mainly for planar concepts **due to high fields**
under use conditions

Once device is turned on
→ **electric field is at its maximum designed value**

Affects the complete oxide



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Oxide in SiC MOSFET devices

Stressed by electric fields in on- and off-state

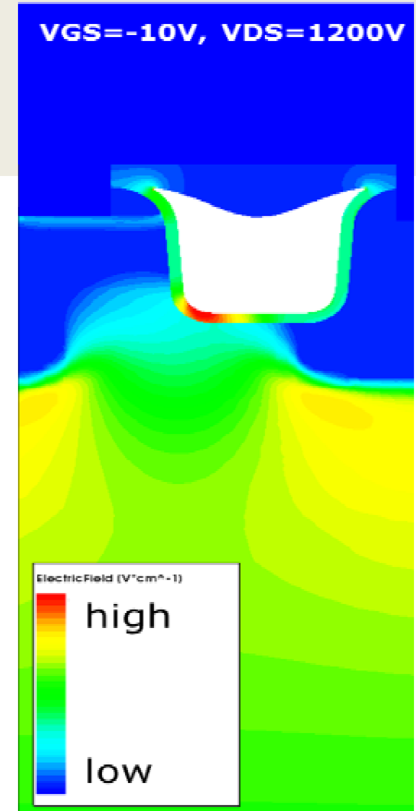
Reverse mode:

Important and more challenging for Trench concepts, but it has **less impact** under nominal use conditions **compared to the on-state**

Max. field achieved at the full rated V_{DS} only (1200 V for lead types)

→ **Real application:**
mission profile based cumulated **stress lower compared to on-state** (e.g. In case of a DC link voltage of 800 V)

Just a small area of the oxide is stressed



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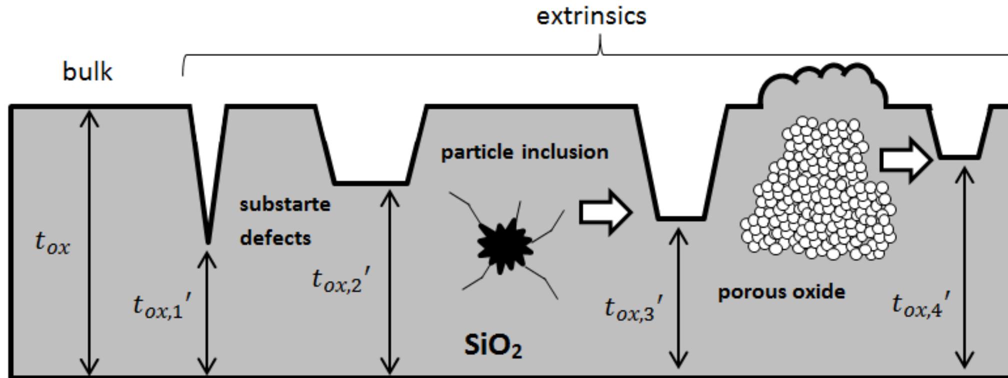
Effect of high gate oxide defect density on SiC MOSFETs' stability : Extrinsic challenge

Substrate defects, particles, process variations, … → **GOX distortions ("extrinsics")** → Decreased lifetime of affected devices → **Early breakdown**

Any distortion can be described as a **local oxide thinning**



The thinner the GOX,
the higher is the electric field
at a certain gate bias
and the lower is the
time to breakdown

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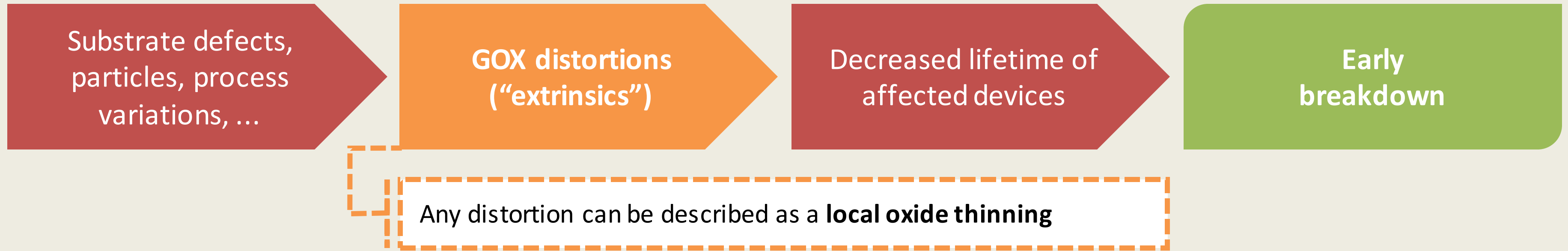
Effect of high gate oxide defect density on SiC MOSFETs' stability: Weibull Plot characterization



Failure probability of
Time-Dependent-Dielectric-Breakdown (TDDB)
Distribution is described in a **Weibull Plot**

After an end of life test of a larger number of devices, the **failure rate over time is plotted**

GOX failure probability typically determined by the extrinsic branch

Intrinsic branch bulk related

1 chip life

Extrinsic branch DD related

$ln(-ln(1-F))$

$ln(t)$

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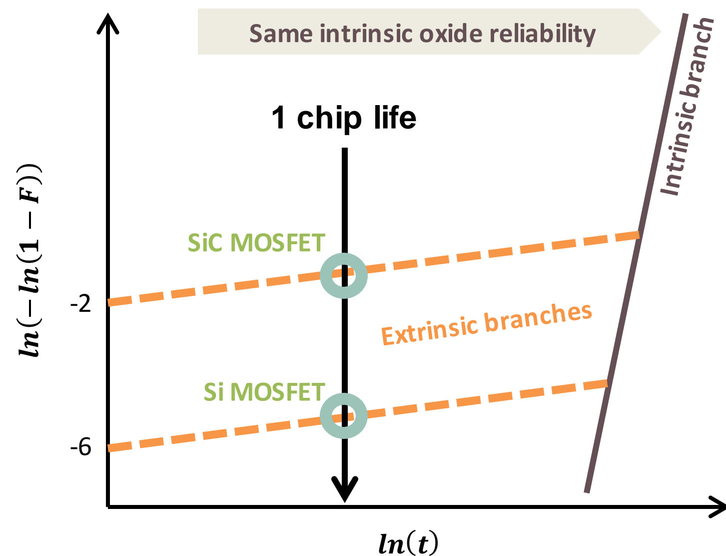
Effect of high gate oxide defect density on SiC MOSFETs' stability: Analyzing failure statistics

How does Weibull Plot look like for SiC and Si MOSFETs?

(same area and gate oxide thickness)



At the end of processing (EOP):

SiC MOSFETs → much larger extrinsic defect density

Failure probability: up to 4 orders of magnitude higher

Many decades of development away to **drop extrinsic GOX defect density below 1% at EOP** in modern SiC MOSFETs

< 0.001% (10 ppm) or < 0.0001% (1 ppm) is needed!

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How can we get rid of devices with critical extrinsics?

Devices are "aged" by an electric screen pattern at the gate

Devices with **critical extrinsics fail/degrade**

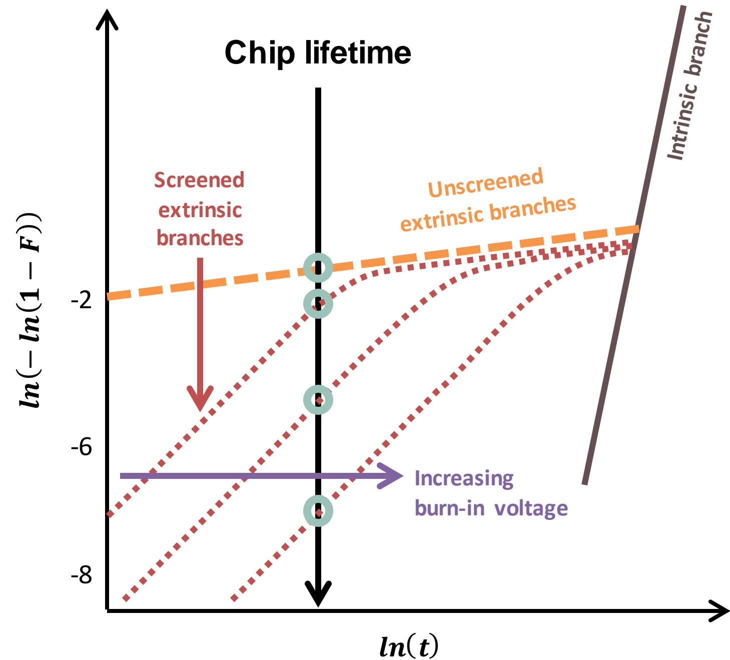
Devices **without critical extrinsics pass**
(small amount of lifetime taken)

Screening more efficient
→ if ratio between screen bias* and use bias is high**

Screen bias level
must not degrade device performance

Conclusion : Thicker oxides enable lower FIT rates:

1 FIT = 1 Failure In Time = $\frac{1\,fail}{10^9\,hours}$



* Screen bias: bias for the test
** Use bias: recommended value for the gate bias based on datasheet

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How can we get rid of devices with critical extrinsics?

Devices are "aged" by an electric screen pattern at the gate

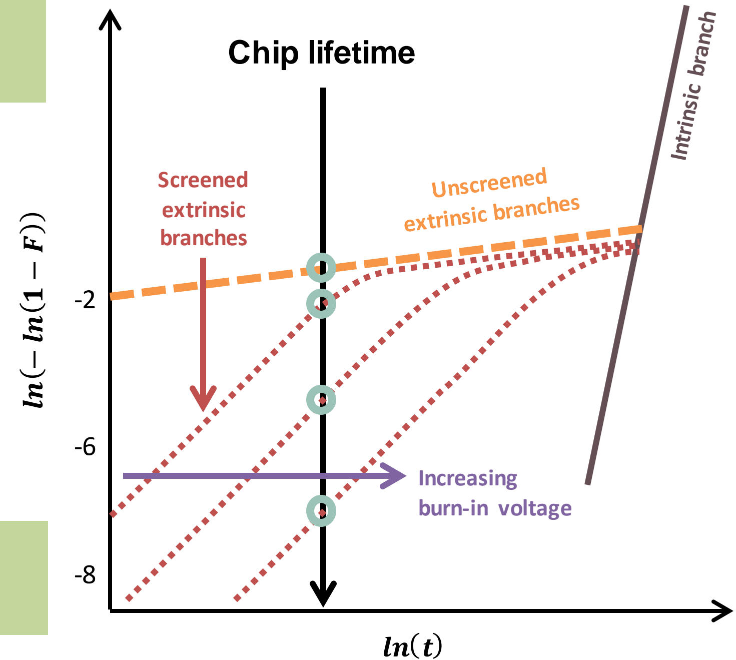
Challenge : Thicker gate oxides increase the R_{on}

Reliability increases **exponentially** with GOX thickness

and

R_{ON} increases only **linearly** with GOX thickness

Over-proportional benefit for reliability



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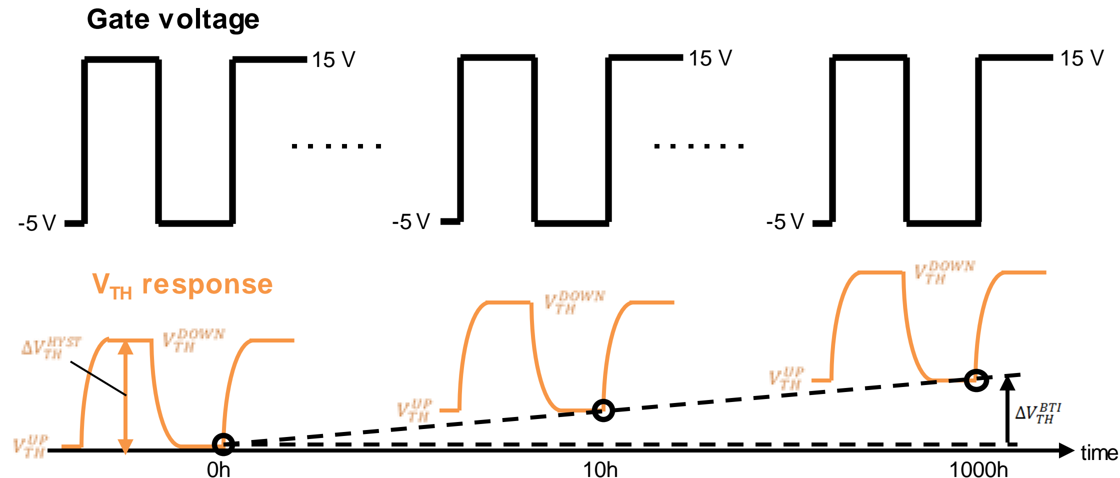
Drift of the threshold voltage in SiC MOSFETs: Static contribution

2 quasi-static Bias Temperature Instability (BTI) components exist



Fully reversible threshold voltage hysteresis ($\Delta V_{TH}{}^{HYST}$)

More permanent threshold drift ($\Delta V_{TH}{}^{BTI}$)

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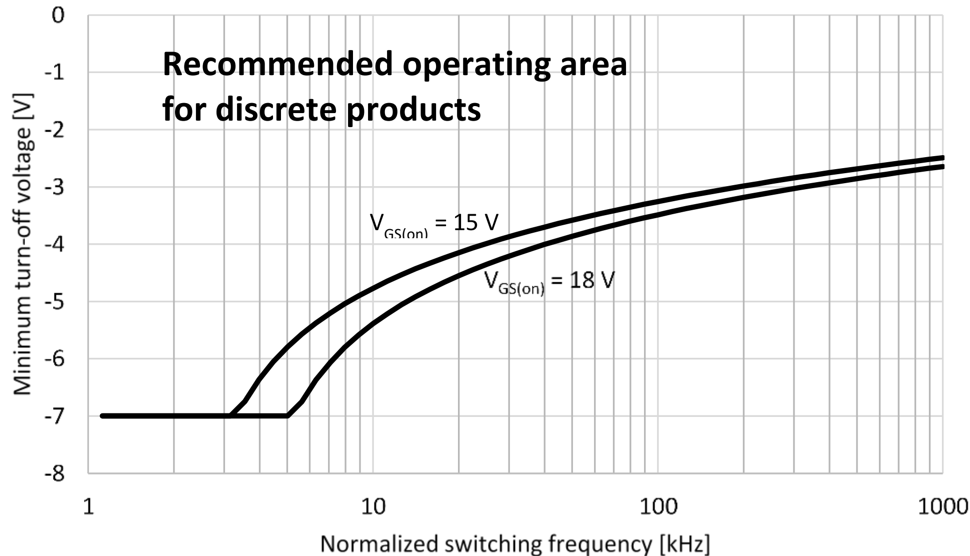
Drift of the threshold voltage in SiC MOSFETs: Dynamic contribution*

By switching triggered, a 3rd Bias Temperature Instability (BTI) components exist



Triggered by switching device, a **third effect needs to be taken into account** when V_{TH} effects are quantified

Amount of V_{TH} drift mostly **influenced by switching frequency** and **chosen bias for turning off the MOSFET**, partially also by turn-on bias at the gate

Infineon provides an Application Note (AN2018-19) that describes how to make sure to **stay within the safe operating area.**

Magnitude of the effect needs to assessed for a certain technology and is in the focus of optimization targets.

*H. Jiang, X. Zhong, G. Qiu, L. Tang, X. Qi and L. Ran, "Dynamic Gate Stress Induced Threshold Voltage Drift of Silicon Carbide MOSFET" IEEE Electron Device Letters, vol. 41, no. 9, pp. 1284-1287, Sept. 2020

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SiC reliability: cosmic ray aspects

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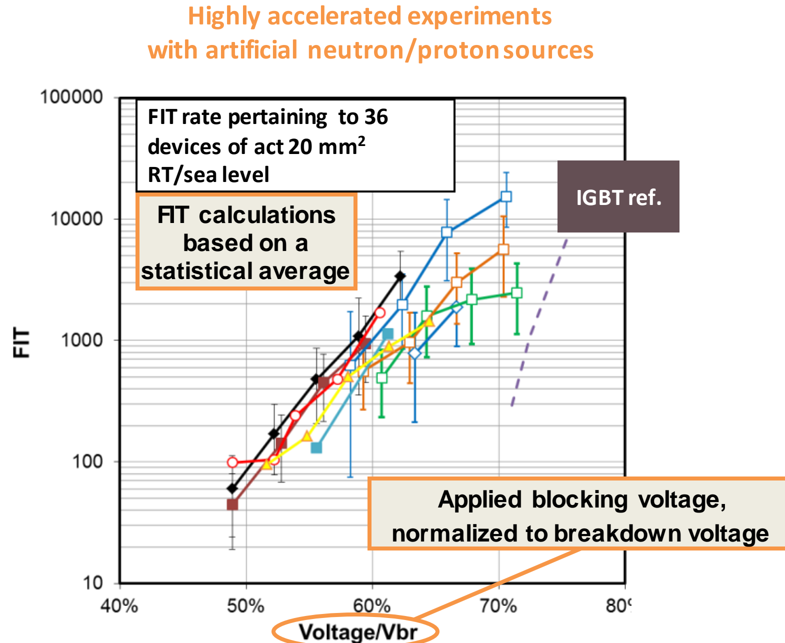
Cosmic ray failure rates: Situation for SiC

Cosmic ray: radiation caused by extraterrestrial sources that causes fatal device fails

Highly accelerated experiments
with artificial neutron/proton sources



Customized calculation and tuning of cosmic ray robustness

Failure rates are measured in FIT

Typical applications require ~1 – 100 FIT for a single device during whole lifetime

FIT rate in field depend on:

Mission profile
- Voltage over time profile
- Altitude profile

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Cosmic ray and SiC: Impact on real designs and difference from Si

SiC MOSFET: **smaller active area** than Si IGBT/diode (same current)

SiC MOSFET: **no need of free wheeling diode** (which contributes to CR FIT)

Si FIT rate: **larger descrease with rising T_j** (compared to a SiC MOSFET)

Graph represents typical CR FIT values for a 200 A Si- and SiC-based half-bridge at 25ºC and sea level

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SiC reliability: body diode performance

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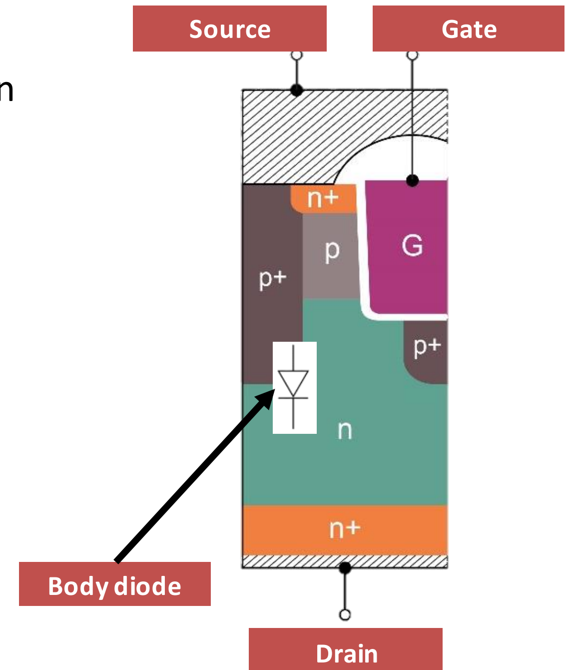
MOSFET body diodes: Structure and requirements

Vertical power MOSFETs (planar and trench types)

These contain a diode that allows conduction in the 3rd quadrant and can be used as freewheeling diode – **body diode**

Since V_F of pn-based diodes in SiC is high
→ **It is recommended to use synchronous rectification**

Turn on the channel after a short dead time
In this mode, channel carries most of the current and low losses (comparable to the 1st quadrant) are secured



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The potential degradation in bipolar SiC elements: Recombination induced increase of $R_{DS(on)}$ and V_{SD}

Bipolar degradation might **affect all SiC MOSFET** technologies

Effect is defect-driven and related to defects of **substrate material**

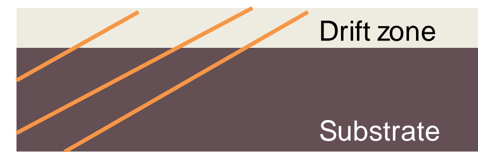
Statistical effect: **devices without these defects will not have bipolar degradation effect**

Effect **only triggered by bipolar operation** (body diode conducting) **and saturates** after limited time

Driven by electron hole recombination, **stacking faults grow in the drift zone and act as a barrier for current**

Top view

Cross section



What is the impact of bipolar degradation in application?

Drift of $R_{DS(on)}$ and diode V_{SD} over operation time due to reduction of effective active area of the device

No other major properties will change (e.g. V_{br}, $V_{GS(th)}$, …)

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Bipolar degradation: Countermeasures

Infineon's strategy to tackle the effect

Applying screening approach (as for gate oxide extrinsics) as long as defect density is above a critical threshold

Dropping down defect density to avoid stacking fault growth

Avoiding recombination at stacking faults

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Product release process and robustness validation approach

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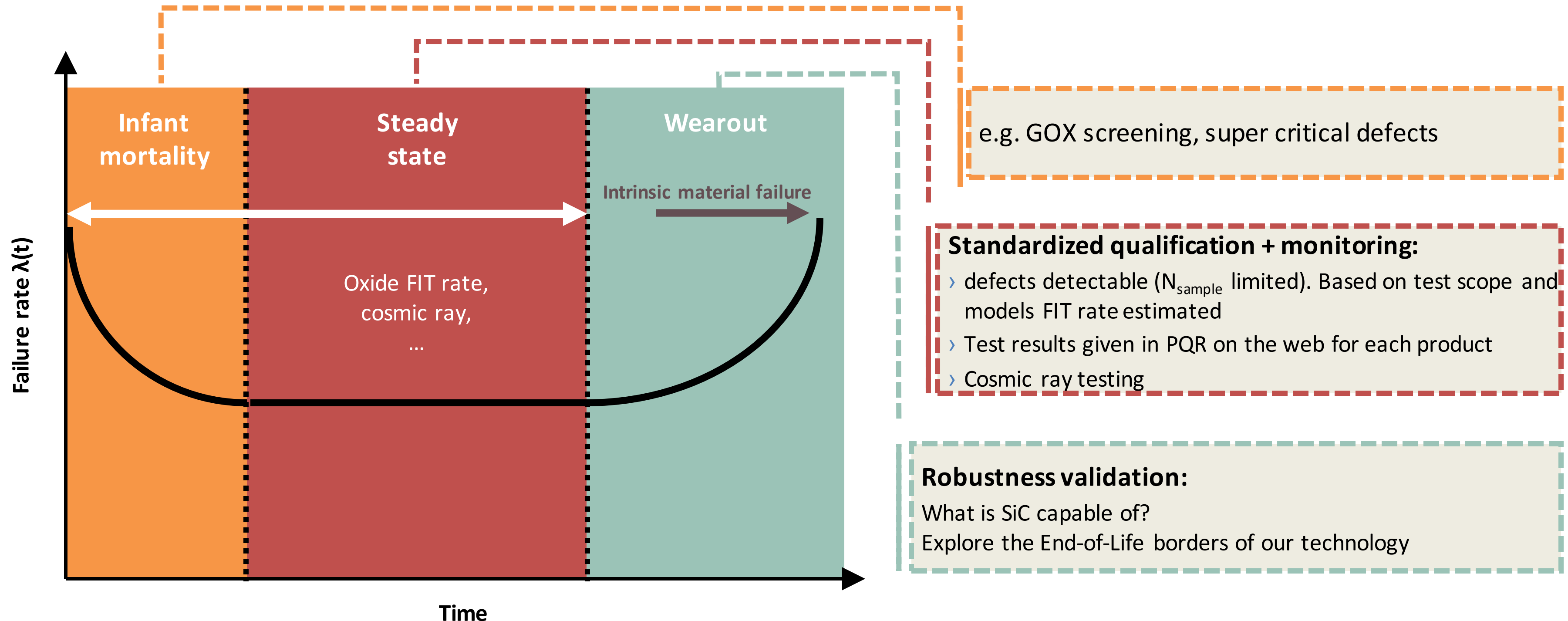
Robustness and bathtub curve: Short introduction



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Robustness validation for Infineon's power modules

Test	Test conditions	Serial release: stress time
HTRB	V_{DS} = 1080 V T = 150°C	1000h
HTGS	V_{DS} = 0 V V_{GS} = +20 V/-20 V T = 150°C	1000h
H3TRB	V_{DS} = 80 V T = 85°C rH = 85%	1000h
HV-H3TRB	V_{DS} = 960 V T = 85°C rH = 85%	1000h
AC HTC	T_{cycle} = -20°C/85 °C rH = 93% V_{DS} = typ. (AC) f = typ. kHz	21d (only SiC)

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Robustness validation for Infineon's discrete devices

Stress test	Test conditions	Duration	
HTRB	V_{DS} = 1200 V; T_{vj} = 175°C; V_{GS} = 0 V	2000 h	Extended HTRB section
HTRB w/ negative voltage (blocking state)	V_{DS} = 1200 V; T_{vj} = 175°C; V_{GS} = -10 V	2000 h	
HTRB w/ negative voltage (blocking state)	V_{DS} = 1100 V; T_{vj} = 175°C; V_{GS} = -15 V	1000 h	
HTRB w/ pre-stressed parts	V_{DS} = 960 V; T_{vj} = 175°C; V_{GS} = 0 V w/ initial 0x and 10x short-circuit stressed parts	1500 h	
HTGS	V_{GS} = +20/-20 V constant; T_{vj} = 175°C	2000 h	Extended HTGS section
HTGS w/ pre-stressed parts	V_{GS} = +20/-20 V constant; T_{vj} = 175°C w/ initial 0x and 10x short-circuit stressed parts	1000 h	
HV-H3TRB	V_{DS} = 1200 V; T_a = 85°C; rH = 85%	2000 h	Humidity section
Dynamic H3TRB	T_a = 85ºC; rH = 85%; $V_{DC\ link}$ = 960 V; V_{GS} = +15 V/0 V; IL peak = 16 A; f_{SW} = 25 kHz; dv/dt = 70 V/ns	1000 h	
Dynamic Reverse Bias (DRB)	T_a = 25ºC; $V_{DC\ link}$ = 960 V; V_{GS} = +15 V/-5 V; dv/dt ~ 200 V/ns; f_{SW} = 100 kHz	1000 h	

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Key takeaways

- There are three main aspects that make SiC MOSFET systems different from silicon:
  - Larger bandgap
  - Higher blocking capability
  - Higher defect density, which is why stricter measures are required to assure long-term reliability
- There are dedicated measures in place to overcome the challenges posed by SiC such as gate oxide and cosmic ray aspect as well as body diode performance

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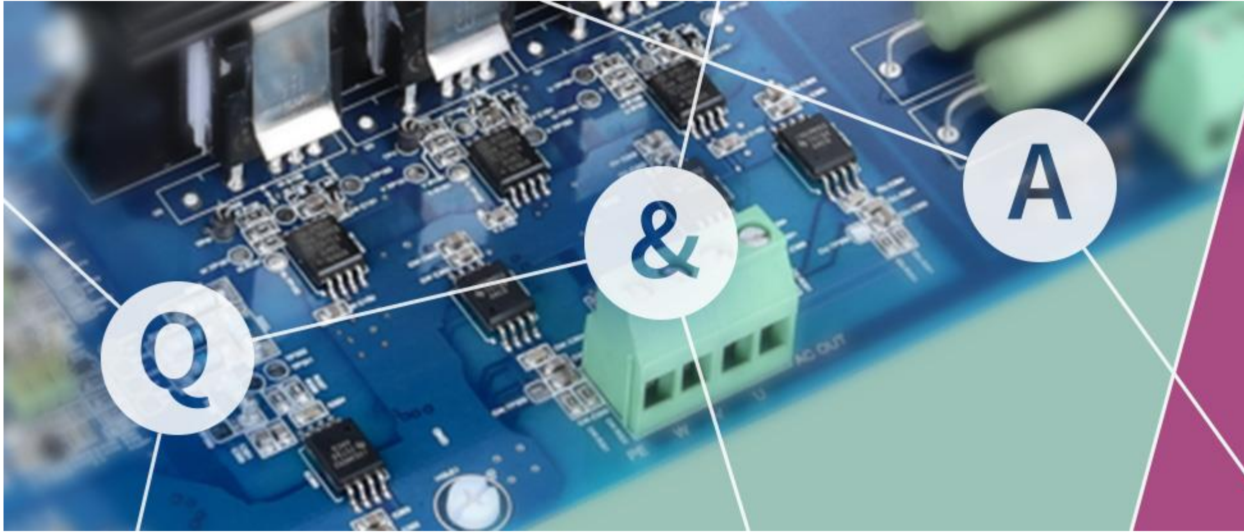

I’m happy to answer your questions now!

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