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In this study, we report solution-processed amorphous zinc tin oxide transistors exhibiting high operational stability under positive gate bias stress, translated by a recoverable threshold voltage shift of about 20% of total applied stress voltage. Under vacuum condition, the threshold voltage shift saturates showing that the gate-bias stress is limited by trap exhaustion or balance between trap filling and emptying mechanism. In ambient atmosphere, the threshold voltage shift no longer saturates, stability is degraded and the recovering process is impeded. We suggest that the trapping time during the stress and detrapping time in recovering are affected by oxygen adsorption/desorption processes. The time constants extracted from stretched exponential fitting curves are $\approx 10^6$ s and 10^5 s in vacuum and air, respectively. © *2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.* [http://dx.doi.org/10.1063/1.4919057]

Solution based amorphous oxide semiconductors (AOSs) provide an innovative and low-cost processing technology for thin-film transistors (TFTs).[1–4] In order to exploit them into practical circuits, it is important to assure that their electrical performance is stable under the required working conditions. One of the sources of instability is related with the threshold voltage shift (ΔV_{th}) when the TFT is operated under constant gate voltage. The phenomena known as gate-bias-stress are common to all TFT technologies, including amorphous oxide TFTs.[5–7] This instability is related with surface states of the dielectric which trap charge carriers and shield the externally applied gate-voltage. In the particular case of oxide semiconductors, oxygen adsorption/desorption processes are also enhanced by an externally applied electric field, contributing to increase instability.[8] In spite of all efforts to mitigate this effect, the problem has not been yet properly solved. In fact, even for high quality thermal SiO₂ typically used in test structures for performance evaluation of thin film semiconductors, it is not possible to assure an entirely perfect interface between dielectric and semiconductor. Previously, amorphous oxides using SiO₂ as dielectric suffer from a pronounced ΔV_{th}, with time constants (τ) of 10^4-10^5 s.[6,7,9] Here, we show evidences of intrinsically more stable solution-based zinc tin oxide (ZTO) TFTs from studying the time and temperature dependence of bias stress and recovering process. We propose that this enhanced stability is promoted by a defect passivation or neutralization of the SiO₂ surface and consequently reducing the number of traps. We suggest that this passivation is brought out during the thin film fabrication process of the ZTO solution.

The TFTs are produced in a staggered bottom-gate, top-contact structure. Zinc nitrate and tin chloride-based precursors are used to prepare a ZTO solution which is then spin coated on top of a 100 nm thick thermal SiO₂ on Si substrate. The film is annealed at 350 °C in air during 30 min. Next, Al source and drain electrodes (70 nm thick) are e-beam evaporated on top of the annealed ZTO film with typical channel width (W) and length (L) of 1400 μm and 100 μm, respectively
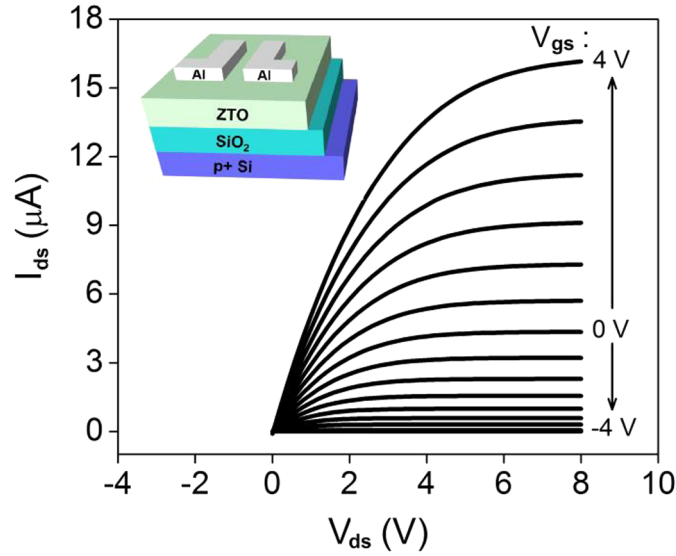
FIG. 1. Output characteristic of the solution based ZTO TFTs on thermal SiO$_2$. The inset shows the ZTO-SiO$_2$ TFT structure.

(W/L = 14). Patterning is obtained via shadow masks. Figure 1 shows the typical output characteristic of the device. The schematic of device structure is shown in the inset of this figure. For the mobility μ_n, the value of the field-effect mobility at V_{ds} = 1 V is chosen. The subthreshold swing (SS) is taken as the minimum value of $d(\log(I_{ds})/(V_{gs}))^{-1}$. Typical values for the as-fabricated devices are V_{th} = −3.1 V, SS = 0.35 V/dec, and μ_n = 2.5 cm^2/V s at room temperature.

During the positive gate-bias stress (PBS) experiment, all TFTs are biased with a constant gate voltage while source and drain are grounded. After a prefixed time, the bias stress is interrupted and the gate voltage (V_{gs}) is swept at V_{ds} = 1 V to measure the I_{ds}-V_{gs} characteristics of TFT. Stress measurements are performed in air and under vacuum (10^{-5} millibars, leaving the device at this pressure for 1 h prior starting the stress experiment) under dark condition. To overcome the problem of non-linearity of transfer characteristics, V_{th} is taken as the voltage corresponding to I_{ds} = 1 nA. PBS displaces the transfer curves to the positive direction. The ΔV_{th} occurs toward the applied stress voltage and is continuously shutting down the drain-source current. Figure 2(a) shows the shift of the transfer curves under constant V_{gs} = 5 V in vacuum. Interestingly, PBS in vacuum results into threshold voltage displacement during 8 h with ΔV_{th} saturating after ≈1 V shift over this period. The time dependence of ΔV_{th} can be well fitted by a stretched-exponential equation as below,

$$\Delta V_{th} = V_0 \left\{ 1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta} \right] \right\},$$

where t is the stress time, $V_0 = |\Delta V_{th}|$ at the infinite time, β is the dispersion parameter which is related to the degree of barrier energy dispersion, and τ is the time constant. Table I shows all the fitting parameters values in different PBS conditions.

In order to get further insight into the physical mechanism of the gate-bias stress, the kinetics of the threshold voltage recovering process is also monitored while the device is kept unbiased under dark conditions. The stress and recovering times are compared in Fig. 2(b). The recovering time is fast <1 h, and V_{th} shift is linearly proportional to the logarithmic time, as observed in the inset of Fig. 2(b) supporting charge detrapping as the dominant mechanism. The fast device recovery is technologically relevant and to the best of our knowledge, has not been reported so far. The observed behavior can be interpreted in terms of a trap model. The fact that ΔV_{th} reaches saturation shows that the number of states or defects available is limited. During stress time, the trap filling rate is dominated by the number of defects or available sites (N_t). ΔV_{th} is then given as $\Delta V_{th} = eN_t/C_{ox}$, where C_{ox} is the capacitance of the gate dielectric and e is the elementary charge. Throughout the stress measurement, more defect states are filled and consequently there are fewer
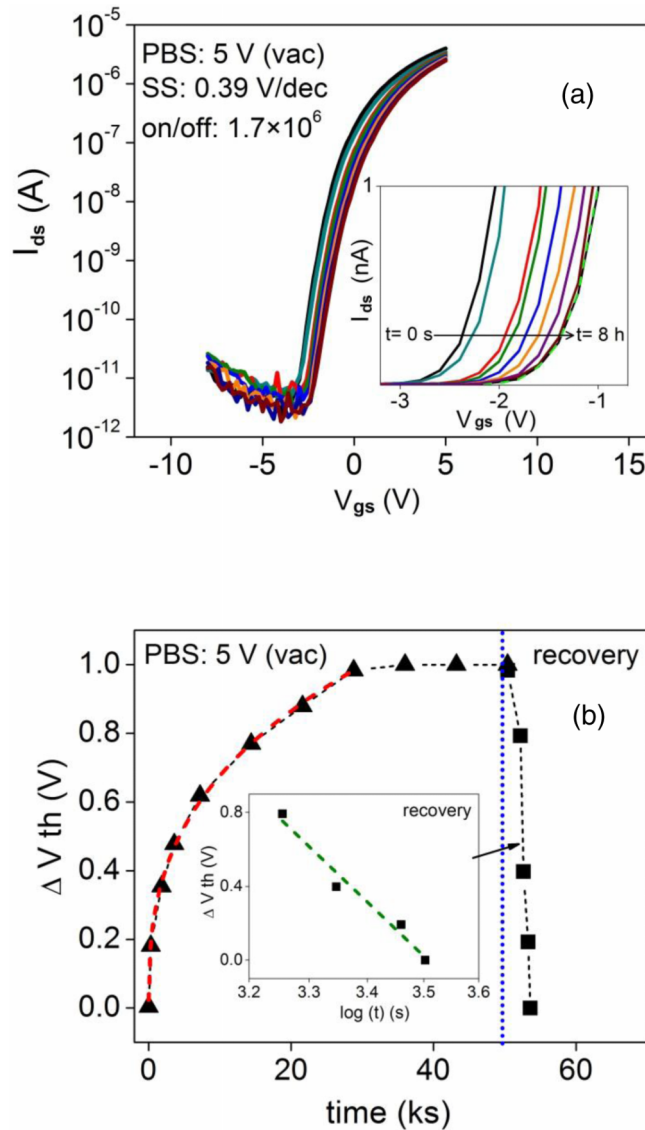
FIG. 2. (a) Transfer characteristics of ZTO-SiO$_2$ TFT at V$_{ds}$ = 1 V during gate bias stress with V$_{gs}$ = 5 V, operating in vacuum. The inset shows the current level at 1 nA. (b) Threshold voltage shift as function of time in vacuum. Red short dashed lines are fitting curves with standard stretched exponential time dependence equation. The green dashed line shows V$_{th}$ shift is linearly proportional to the logarithmic time.

states available; therefore at a long enough stress time, all defect states will be eventually filled leading to threshold voltage saturation. It is difficult to assess if the saturation of the threshold voltage is caused by trap exhaustion or alternatively by a competing trap filling/emptying mechanism. At long stress times, the backward (trap emptying) reaction eventually becomes faster than the forward reaction (trap filling). This stops further change in threshold voltage after a certain period of time. As a result, instantaneous threshold voltage shift becomes virtually zero.

Figure 3 shows the temperature dependence of the threshold voltage shift within the stress time. The time dependence of $\mathit{\Delta V_{th}}$ under stress is fitted by a stretched-exponential equation. The inset of Fig. 3 shows that τ is thermally activated by fitting the data to the following equation:

$$\tau = \tau_0 \exp(E_\tau / kT),$$

where T is the absolute temperature, k is the Boltzmann constant, and E_τ is the activation energy. The obtained activation energy is 0.64 eV. This value has been already reported for TFTs based

TABLE I. Stress condition at different temperature, threshold voltage shift ΔV_{th}, time constant τ, dispersion parameter β, and recovery time.

Stress condition	T (K)	ΔV_{th} (V)	τ (s)	β	Recovery
PBS (air, 14 h)	295	3.44	1.5×10^5	0.52	~7days
PBS (vacuum, 8 h)	295	0.98	5.6×10^6	0.36	53 min
NBS (air, 6 h)	295	−2.23	8.2×10^6	0.25	~30 min
NBS (vacuum, 6 h)	295	−2.15	9.0×10^6	0.28	~30 min
PBS (vacuum, 6 h)	345	1.20	1.9×10^6	0.43	<20 min
PBS (vacuum, 6 h)	395	1.49	6.3×10^5	0.51	<20 min
PBS (vacuum, 6 h)	420	1.63	4.4×10^5	0.51	<20 min

on other semiconductor technologies using SiO_2 as a gate dielectric, supporting the view that this defect is not intrinsic to ZTO but instead related with the SiO_2 surface.[7,9]

Under the presence of ambient atmosphere (295 K, 1 bar) during PBS process, the ZTO-TFT stability is severely degraded. However, the presence of oxygen does not affect the negative bias stress (NBS) instability. The fitting parameters β and τ are approximately equal for NBS measurements under vacuum and in the presence of atmosphere as shown in Table I.

Fig. 4(a) shows the typical electrical characteristics of the device under a gate-bias stress of 5 V in ambient atmosphere. The time dependence of ΔV_{th} associated with fitting plots is shown in Fig. 4(b). The time constant ($\tau = 10^5$ s) is now one order of magnitude lower than the one measured in vacuum ($\tau = 10^6$ s). Higher value of τ indicates that at a particular temperature, the course of threshold voltage shift persists longer and the operational stability is enhanced. In this respect, τ can be used as a figure of merit to quantify operational stability. The value of β ($\beta = 0.52$) is higher in vacuum than in air ($\beta = 0.36$). This means that the distribution of energy barriers or trap sites becomes broader when oxygen adsorption occurs. Furthermore, the V_{th} does not saturate, suggesting that more defect states become available in the presence of atmosphere. Most relevant, the ability of the device to recover the original V_{th} is severely impeded, being the recovering time now more than 10^6 s. This time contrasts with the behavior in vacuum where a few minutes under unbiased conditions are enough to fully recover the original V_{th}. The recovering fitting shows the time constant of 5.5×10^4 s. This value is one order of magnitude smaller than trapping time during PBS in air. It
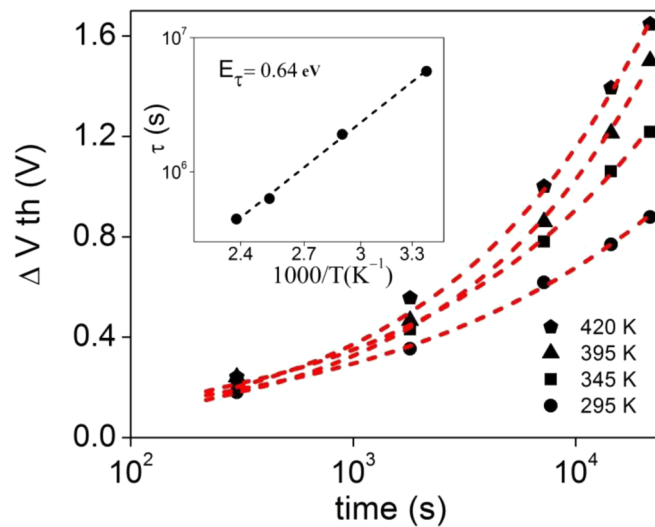

FIG. 3. Threshold voltage shift as function of time on a logarithmic scale for gate bias stress of 5 V at various temperatures: 295 K, 345 K, 395 K, and 420 K. The red dashed lines are fitting curves with stretched exponential equation. The inset shows the time constant τ as function of reciprocal temperature. The black dashed line indicates that τ is thermally activated with $E\tau = 0.64$ eV.
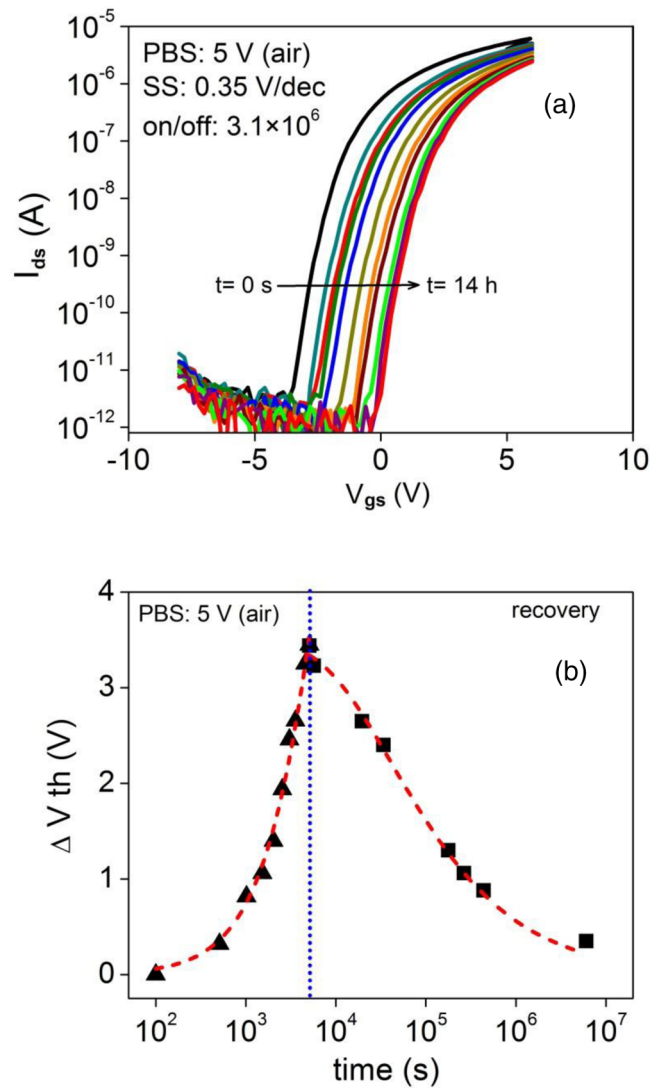
FIG. 4. (a) Transfer characteristics of ZTO-SiO$_2$ TFT at $V_{ds} = 1$ V during gate bias stress with $V_{gs} = 5$ V, operating in air. (b) Threshold voltage shift as function of time on a logarithmic scale and the recovery processes in air. The red dashed lines are fitting curves with stretched exponential equation.

supports that the recovering process is not only charge detrapping process but also the oxygen ion desorption from the channel surface contributes in the recovering mechanism. Nevertheless, the β is the same for stress/recovery process indicating the similar barrier energy dispersion of trap sites.

The fact that the threshold voltage can shift faster in air than in vacuum has been reported by a number of authors and tentatively explained by several mechanisms.[10,11] The new finding reported here is that for solution based ZTO, the presence of atmospheric species impedes the fast recovering of the V_{th} observed under vacuum conditions. In order to explain this behavior, we propose that oxygen species adsorb to the ZTO back channel exposed surface. The effect of external electric field which can induce the chemisorption of oxygen on zinc oxide thin film has been already reported in 1968. A field which brings electrons to the surface would favor increased oxygen adsorption.[8] Oxygen is a weak electron acceptor and removes free electrons from the bulk ZTO leading to overall reduction in the free carrier concentration. Therefore, it results in a depletion layer on the surface and increase of threshold voltage. During the recovering time when the device is kept unbiased, it is difficult to remove the oxygen molecules without any driving force. Therefore, the V_{th} hardly recovers back to its initial value. Two instability mechanisms simultaneously occur in TFT under

gate bias stress experiment in air: (i) surface dielectric states trap electrons and shield the external gate bias, and (ii) adsorbed oxygen layer on the top exposed ZTO surface captures free carriers from ZTO. The two effects add to each other contributing to a further increase in threshold voltage shift in air.

In summary, we have shown that solution based ZTO-TFTs are highly stable in vacuum. The threshold voltage shift saturates in a time scale of 10^4 s. Furthermore, when the TFTs are kept unbiased, they exhibit a remarkable fast recovering behavior of the threshold voltage shift. We attributed this high operational stability to a passivation/neutralization of SiO_2 surface defects occurring during the drying/annealing of the ZTO solution. Saturation of the threshold voltage shift may arise because the number of traps is finite, or alternatively because the internal field caused by the immobile trapped carriers will lead to a balance between trap filling and emptying. The presence of atmospheric species eliminates the ability of the stressed device to restore the original threshold voltage. We propose that a negatively charged oxygen layer is depleting the ZTO bulk from free carriers and impedes the V_{th} to be restored to original values. Encapsulation of the devices should prevent the interference of oxygen species and diminish this effect. The deposition of semiconductor layers under vacuum should in principle lead to a better control of impurity densities, interestingly the results reported here suggest that solution based amorphous oxides can intrinsically passivate the dielectric surface and lead to highly stable devices.

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