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Role of Remote Interfacial Phonon (RIP) Scattering in Heat Transport Across Graphene/SiO_2 Interfaces

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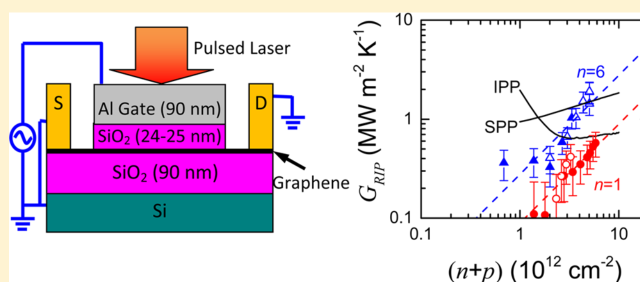
Supporting Information

ABSTRACT: Heat transfer across interfaces of graphene and polar dielectrics (e.g., SiO_2) could be mediated by direct phonon coupling, as well as electronic coupling with remote interfacial phonons (RIPs). To understand the relative contribution of each component, we develop a new pump–probe technique called voltage-modulated thermoreflectance (VMTR) to accurately measure the change of interfacial thermal conductance under an electrostatic field. We employed VMTR on top gates of graphene field-effect transistors and find that the thermal conductance of SiO_2/graphene/SiO_2 interfaces increases by up to $\Delta G \approx 0.8$ MW m^{-2} K^{-1} under electrostatic fields of <0.2 V nm^{-1}. We propose two possible explanations for the small observed ΔG. First, because the applied electrostatic field induces charge carriers in graphene, our VMTR measurements could originate from heat transfer between the charge carriers in graphene and RIPs in SiO_2. Second, the increase in heat conduction could be caused by better conformity of graphene interfaces under electrostatic pressure exerted by the induced charge carriers. Regardless of the origins of the observed ΔG, our VMTR measurements establish an upper limit for heat transfer from unbiased graphene to SiO_2 substrates via RIP scattering; for example, only <2% of the interfacial heat transport is facilitated by RIP scattering even at a carrier concentration of $\sim 4 \times 10^{12}$ cm^{-2}.



KEYWORDS: *Remote interfacial phonon (RIP) scattering, graphene interfaces, interfaces of 2D materials, interfacial thermal conductance, electrostatic pressure, electrostatic control of heat conduction*

Charge carriers in carbon nanotubes (CNTs), graphene, and other 2D materials can remotely couple to surface polar phonons (SPPs) in the underlying polar substrates via a mechanism usually called remote interfacial phonon (RIP) scattering.[1−3] (We use surface polar phonons to refer to thermally excited vibrational modes near the surface that have an electric dipole moment, including e.g., surface phonon polaritons.) In RIP scattering, remote coupling between charge carriers in graphene or CNTs and SPPs in the polar substrates, spatially separated over a distance of <1 nm, is facilitated by oscillating surface electric fields created by the SPPs and is accompanied by momentum and energy exchange.[4] RIP scattering of charge carriers has been frequently invoked to explain electrical and optical properties of graphene and CNTs, the reduction of the mobility of charge carriers in supported graphene and CNTs,[1,2] current saturation in graphene,[3,5] and nonvanishing absorption of light by graphene.[6]

In principle, with the remote coupling through RIP scattering, remote energy transfer occurs between charge carriers in graphene (or CNTs) and the dielectric substrates. While a few theoretical studies of the role of RIP scattering in heat transfer across interfaces of graphene or CNTs exist in the literature,[4,7−10] experimental measurements[11] of heat transport due to RIP scattering are limited beause of difficulties in isolating heat transfer by RIP scattering from heat transfer due to vibration modes (i.e., phonons). In this paper, we present a novel approach to directly measure the change of interfacial

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thermal conductance under electric fields, which could become a generally applicable tool to study the contribution of RIP scattering to interfacial heat transfer of many other 2D materials under varying bias conditions.

Knowledge of heat transport across graphene interfaces[12,13] is crucial for thermal management of graphene devices. For undoped and unbiased graphene, we previously demonstrated that heat is predominantly carried across inherently decoupled graphene interfaces through transmission of acoustic phonons.[13] (Throughout this paper, we use "unbiased graphene" to refer to graphene with no electric current flowing because no lateral source-drain bias is applied.) However, under high vertical electric fields (induced by a gate, as in an operating graphene field-effect transistor), a high concentration of charge carriers is induced in the graphene channel. As a result, electrons and holes could play a significant role in heat conduction across graphene interfaces via RIP scattering.[9,14]

In fact, this remote heat transfer via RIP scattering is thought to dominate heat dissipation from CNTs to dielectric substrates.[7,11] Specifically, Rotkin et al. calculated that RIP scattering contributes thermal conductance per unit length of $g_{RIP} \approx 0.1$ W m^{-1} K^{-1} to interfacial heat transfer of a single-walled CNT (~1.3 nm in diameter) with a carrier concentration of 0.1 e/nm.[7] Later, Baloch et al. estimated from their measurements on multiwalled CNTs (~25 nm in diameter) that the contribution by RIP scattering is $g_{RIP} \approx 0.02$ W m^{-1} K^{-1} when driven by high source-drain biases.[11] (We discuss below our estimates related to Baloch's work and note that in reaching their conclusion, they used a low thermal contact conductance[15] by vibration modes of 0.004 W m^{-1} K^{-1}.)

Here, we experimentally demonstrate that unlike CNTs, contribution of RIP scattering to interfacial heat conduction across unbiased graphene (without current flow) and SiO_2 is small compared to the phonon contribution, even at high carrier concentrations. We accurately measured the change of thermal conductance of SiO_2/graphene/SiO_2 interfaces under modulated electrostatic fields and find that the thermal conductance of the graphene interfaces increases by up to ~0.8 MW m^{-2} K^{-1} under a vertical electrostatic field of <0.2 V nm^{-1}. We postulate that this (small) enhancement in heat conduction is due to either better conformity of graphene to the substrates under electrostatic pressure or an additional heat transfer channel by RIP scattering of charge carriers in graphene. In either case, we successfully establish an upper limit to heat conduction via RIP scattering; we estimate that the contribution does not exceed 1.6 MW m^{-2} K^{-1}, which is <2% of total thermal conductance of the unbiased graphene interfaces, even at a carrier concentration of 4×10^{12} cm^{-2}. We note that graphene in our experiments is unbiased (with no current flow), while CNTs in prior calculations[7] and experiments[11] were source-drain biased and carrying an electrical current, which could play an additional role in RIP scattering.[7,10]

The changes of thermal conductance that we observed in this work, while still small in magnitude and thus currently not yet suitable for practical applications, could inspire a new and unconventional approach to control heat conduction in future devices, that is, via application of electrostatic fields.

Our test structure is a dual-gated graphene field-effect transistor (GFET), see Figure 1a,b. Details of sample preparation are presented in the Supporting Information. We deposited graphene flakes on 90 nm SiO_2 on Si by micromechanical exfoliation[16] from natural graphite. We determined the numbers of graphitic layers from the ratios of the integrated intensity of the G and 2D peaks,[17] and of the G and Si peaks[18] of the Raman spectra (Figure 1c). We then annealed the samples in a chemical vapor deposition (CVD) furnace at 400 °C for 35 min in Ar/H_2 mixture gas to remove the adhesive residue from the tape. After annealing, we patterned and subsequently deposited Ti/Au (1/40 nm) on the graphene as source/drain electrodes, SiO_2 as the gate dielectric layers and Al (90 nm) as the top gates, by e-beam lithography, e-beam evaporation, and lift-off. The thin layer of SiO_2 was thermally evaporated on the samples by an e-beam evaporator at ~8×10^{-7} Torr. The thickness of the SiO_2 films was measured by ellipsometry; h_{SiO2} = 24−25 nm.

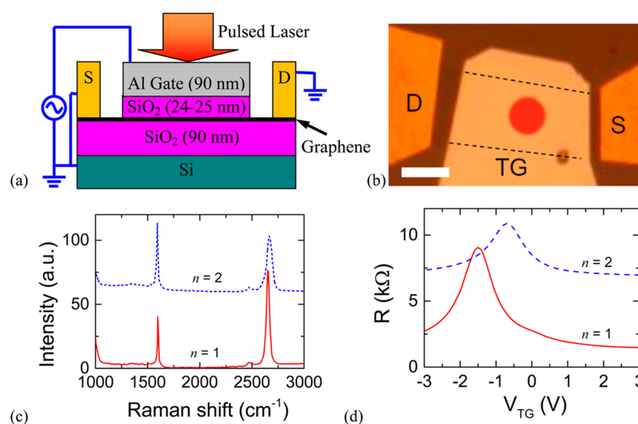

Figure 1. (a) Vertical cross section of the samples (not-to-scale). An Al (90 nm) thin metal pad was patterned on a graphene flake on SiO_2 (90 nm) on Si substrate as the top gate of the GFET. In all our measurements, the sources and drains are grounded. In VMTR measurements, the thermoreflectance signals of the top gate are monitored while the electrostatic potential of the gate is modulated. (b) An optical image of a monolayer GFET sample. D, S, and TG indicate drain, source and top-gate electrodes. The red spot on top-gate electrode represents the laser spot for the VMTR measurement. The scale bar is 10 μm. (c) Raman spectra of a monolayer (n = 1) and a bilayer (n = 2) graphene used in our experiments. The curves are vertically shifted for the clarity. Number of graphitic layers of the graphene flakes is determined from the ratio of integrated intensity of G and 2D, and Si and G peaks as described in refs 17 and 18. (d) Electrical resistance of our GFETs as a function of top-gate voltage (V_{TG}). The charge-neutral-point is located at around −1.5 V for the monolayer graphene sample and −0.75 V for the bilayer graphene sample.

We verified that the e-beam lithography, lift-off, and evaporation processes did not damage our graphene flakes through our Raman, electrical, and thermal measurements. We performed Raman spectroscopy measurements on graphene covered by evaporated SiO_2 and found that the Raman spectra are similar to the Raman spectra of pristine[13] graphene with reasonably small D peaks (which indicate low-defect concentrations in graphene), see Figure 1c. Figure 1d displays transistor modulation of the graphene devices using the top gates, when the bottom-gates are grounded. We estimated mobility of 1900 and 280 cm^2 V^{-1} s^{-1} for our monolayer and bilayer graphene, respectively. We measured the thermal conductance G of SiO_2/graphene/SiO_2 interfaces by the differential time-domain thermoreflectance (TDTR); details of our approach are described in ref 13. We find that $G \approx 41$ MW m^{-2} K^{-1} with an uncertainty of ~28%. The uncertainty is

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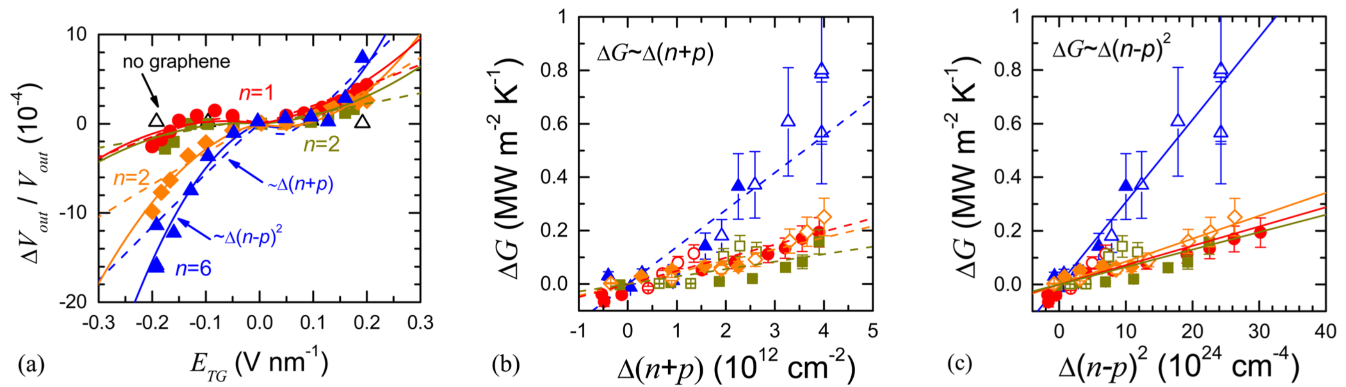

Figure 2. (a) Voltage-modulated thermoreflectance (VMTR) measurements (ΔV_{out}) normalized by the out-of-phase signal (V_{out}) without top gate modulation for a monolayer graphene (circles), two bilayer graphene (squares and diamonds) and a few-layer graphene (triangles) GFETs, as a function of the "on"-state electrostatic field (ΔE_{TG}) applied to the Al top gate of the GFETs. Open triangles are VMTR measurements on the few-layer graphene sample on a region without the graphene flake. We estimate the uncertainty from standard deviations of the mean of the measurements; they are smaller than the size of the symbols. The VMTR measurements are fitted assuming that $\Delta G \sim \Delta(n + p)$ (dashed lines) and $\Delta G \sim \Delta(n-p)^2$ (solid lines), where n and p are electron and hole concentrations, $\Delta G = G_{TG} - G_0$, $\Delta(n + p) = (n + p)_{TG} - (n + p)_0$ and $\Delta(n - p)^2 = (n - p)^2_{TG} - (n - p)^2_{TG}$, the subscripts TG and 0 represent properties at gate voltages of V_{TG} and 0 V. (b,c) ΔG of SiO_2/graphene/SiO_2 interfaces, as a function of (b) $\Delta(n + p)$ and (c) $\Delta(n - p)^2$. Solid symbols are for the case that electrons are the dominant carrier ($n > p$) and open symbols for holes as the dominant carriers ($n < p$).

rather high due to low sensitivity of TDTR signals to G, see the sensitivity plots in Figure S4 in the Supporting Information. The measured thermal conductance is roughly half of $G = 83$ MW m^{-2} K^{-1} for single SiO_2/graphene interface;[12] this is consistent with our previous conclusion that for heat conduction graphene interfaces can be regarded as two discrete interfaces acting in series, even for monolayer graphene.[13]

We measured the change of thermal conductance of graphene interfaces under electrostatic fields by a new technique called voltage-modulated thermoreflectance (VMTR). VMTR is an extension of time-domain thermoreflectance (TDTR), a pump−probe technique to study thermal energy transport in nanostructures[19−21] and across interfaces.[13,22,23] In VMTR measurements, ultrashort laser pulses (∼100 fs) from a Ti:sapphire oscillator are split into a pump and a probe beams. The pump beam, modulated at a radio frequency (rf) of f_{pump} = 10 MHz, is absorbed by the metal electrodes, generating periodic heating at their surface. The probe beam is then used to monitor the periodic temperature response induced by the heating through thermoreflectance (i.e., changes of reflectance with temperature), using a photodiode and a rf lock-in amplifier. We fixed the relative time between pump and probe pulses (which is called the delay time) at $t = -40$ ps. At this delay time, the out-of-phase signals (V_{out}) of the rf lock-in amplifier are inversely proportional to the thermal conductance of the samples[24] and thus could be used to measure changes in thermal conductance induced by electrostatic fields. The rationale of choosing $t = -40$ ps and f = 10 MHz is illustrated in the sensitivity plots (Figure S4) in the Supporting Information.

To assess the effects of electrostatic fields on heat conduction, we employed 50% duty-cycle, on−off square-wave voltage modulation to the GFET top gates while keeping the Si substrates grounded, see the schematic in Figure 1a. We set the modulation frequency at an audio frequency (af) of f_{TG} = 300 Hz and changed the "on"-state gate voltage V_{TG} from −5 to 5 V. We monitored the resulting change in V_{out} at frequency f_{TG} (ΔV_{out}) using an af lock-in amplifier. We normalized ΔV_{out} with a TDTR measurement of V_{out} without gate modulation to eliminate the need to accurately measure the laser power absorbed by the metal gates. To improve the signal-to-noise of the VMTR measurements, we repeated the measurements for 40−100 times with a time constant of 10 s for each measurement and obtained the average values for ΔV_{out}.

We note that VMTR is a substantial improvement over previous measurements (e.g., in ref 25) of monitoring TDTR signals as the applied voltage changes. In conventional TDTR, the accuracy in determining ΔV_{out} (or other TDTR signals) due to the applied voltage depends on the precision of TDTR measurements over time, that is, the repeatability of TDTR measurements when the same experimental parameters are employed. The precision of TDTR measurements is usually limited by, for example, phase drift in the rf lock-in amplifier and is typically on the order of 1%. In VMTR, however, we apply double modulations by replacing the modulation on the probe beam in TDTR with voltage modulation on the top Al transducer at an audio frequency (e.g., 300 Hz). We then use an audio frequency (af) lock-in amplifier to extract the TDTR responses to changes of electric fields, and thus directly and accurately measure ΔV_{out}. Because of the use of the af lock-in amplifier, the uncertainty of ΔV_{out} is significantly reduced from the uncertainty in the original TDTR measurements of G, see Figure S5 in the Supporting Information for the raw data and the uncertainty of our TDTR and VMTR measurements. The uncertainty of $\Delta V_{out}/V_{out}$ is estimated from standard deviation of the means to be $<2 \times 10^{-5}$, improved from the precision of conventional TDTR by more than a factor of 100. Because all other parameters (e.g., Al thickness, laser spot sizes) do not change in VMTR measurements, VMTR is not sensitive to these other parameters. Thus, VMTR is suitable to sensitively detect any small changes of heat transport under electrostatic fields.

We derived the change of the thermal conductance ΔG from our VMTR measurements; $\Delta G = G_{TG} - G_0$, where G_{TG} and G_0 are the thermal conductance of the SiO_2/graphene/SiO_2 interfaces at the top-gate voltages of V_{TG} and 0 V, respectively. Because $\Delta G \ll G$, ΔG is linearly proportional to $\Delta V_{out}/V_{out}$ and can be expressed as

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$$\Delta G = \alpha G_0 \frac{\Delta V_{out}}{V_{out}} \mathrm{sgn}(V_{TG}) \tag{1}$$

where $\alpha = (V_{out}/G_0)(\partial G_0/\partial V_{out})$ is a dimensionless proportionality constant derived from the thermal model[24] for TDTR measurements; $\alpha \approx 10$ for our GFET samples. $\mathrm{sgn}(V_{TG})$ in eq 1 is the sign of the applied "on"-state gate voltage and it accounts for the sign flip of ΔV_{out} across $V_{TG} = 0$ V. At negative V_{TG}, the af lock-in amplifier in our setup reads a negative value of ΔV_{out} for an increase of V_{out} due to 180° out-of-phase of the gate voltage and the corresponding V_{out}. Thus, a negative value of ΔV_{out} at a negative V_{TG} denotes an increase of V_{out}.

In Figure 2a, we plot our VMTR measurements on the GFETs as a function of the electrostatic field across the SiO_2/graphene/SiO_2 interface during the "on"-state of gate modulation, E_{TG}. We estimated E_{TG} from the "on"-state gate voltage V_{TG} using $E_{TG} = V_{TG}/h_{SiO2}$. Our $\Delta V_{out}/V_{out}$ measurements at large E_{TG} are 2 orders of magnitude larger than the experimental uncertainty and thus are not an experimental artifact. We find that the measured $\Delta V_{out}/V_{out}$ are mostly positive at positive E_{TG} and negative at negative E_{TG}, suggesting that the thermal conductance increases with gate voltages of both signs. Also, we observe that the VMTR measurements differ between samples with no clear systematic dependence on the number of graphitic layers, see Figure 2a. For example, in Figure 2a, the VMTR signals are very different for two bilayer graphene samples, thus indicating that there must be some other important factors (such as the degree of conformity, roughness, and so forth) that play a major role. For example, the graphene-substrate interaction could differ between samples due to variations in adhesion caused by the sample exfoliation technique.

We postulate that the increase of interfacial thermal conductance could be due to either additional heat transfer channel by induced charge carriers in graphene or electrostatic pressure exerted by the induced charge carriers. To test the postulates, we fit the VMTR measurements in Figure 2a using the corresponding dependence on the carrier concentrations in graphene. If the VMTR measurements are due to additional heat transfer channeled by the induced charge carriers in graphene, for example, via RIP scattering[1,7,11,14] of charge carriers in graphene by SPPs in SiO_2, ΔG is approximately proportional to the change of sum of the concentrations of electrons (n) and holes (p) in graphene, as long as the charge concentrations are sufficiently low and the SPPs are essentially unscreened. Mathematically, $\Delta G \sim \Delta(n + p)$, where $\Delta(n + p) = (n + p)_{TG} - (n + p)_0$ and subscripts "TG" and "0" denote values under top gate voltages of V_{TG} ("on"-state) and 0 V ("off"-state), respectively. We estimate[26] that $n + p = \sqrt{n_{cv}^2 + 4n_0^2}$. Here, $n_{cv} = |n-p| = (C_{ox}/q)(|V_{TG} - V_0|)$ is the carrier concentrations induced by the applied gate voltage V_G, V_0 is the Dirac voltage, C_{ox} is the top-gate oxide capacitance, $q = 1.6 \times 10^{-19}$ C is the elementary charge, and n_0 is the carrier density due to thermal generation and electrostatic spatial inhomogeneity in SiO_2. We derived V_0 from the transistor modulation measurements for two of our GFETs, see Figure 1d, and obtained V_0 for the remaining two GFETs by fitting our VMTR measurements. We assume a dielectric constant of 3.9 for the top-gate oxides, see the justification in the Supporting Information, and obtain $C_{ox} \approx 1.4 \times 10^{-3}$ F m^{-2} for our GFETs. We estimate $n_0 = 3.3-6.8 \times 10^{11}$ cm^{-2} using the measured or fitted values of the Dirac voltage, following the procedures outlined in ref 26.

Using the estimated $\Delta(n + p)$, we fitted our VMTR measurements assuming $\Delta G \sim \Delta(n + p)$, see the dashed lines in Figure 2a. The fits are reasonably good except for the largest $\Delta V_{out}/V_{out}$ at $E_{TG} = -0.18$ V nm^{-1}. We then derived ΔG from our VMTR measurements using eq 1 and plot ΔG as a function of $\Delta(n + p)$ in Figure 2b. We note that the derived ΔG has much higher uncertainty than our VMTR measurements in Figure 2a due to the high uncertainty of G_0 in eq 1. The measured ΔG is independent of types of charge carriers (i.e., electrons or holes) induced in graphene, which is consistent with the ambipolar nature of graphene. The largest $\Delta G = 0.8$ MW m^{-2} K^{-1} occurs at $E_{TG} = -0.18$ V nm^{-1}, or equivalent $\Delta(n + p) = 3.7 \times 10^{12}$ cm^{-2}. We thus can place an upper bound on the remote energy transfer between charge carriers in unbiased graphene and SPP modes in SiO_2 via RIP scattering; $G_{RIP} < 1.6$ MW m^{-2} K^{-1} for a single graphene/SiO_2 interface at $n + p \approx 4 \times 10^{12}$ cm^{-2}. (We multiply the measured ΔG by a factor of 2 because there are two graphene/SiO_2 interfaces in our sample.)

The upper bound value of G_{RIP} derived from our VMTR measurements is an order of magnitude lower than heat conduction by phonons across graphene/SiO_2 interfaces.[12,13,27] (However, we note that RIP heat conduction has been predicted to be up to an order of magnitude higher with Al_2O_3 substrates.[4]) In addition, our findings are also in contrast to the apparently dominant contribution of RIP scattering to the interfacial heat conduction of CNTs on SiO_2 substrates, predicted by calculations of Rotkin et al.[7] for single-wall CNTs and the experiments of Baloch et al. for multiwall CNTs.[11] Rotkin et al. calculated that for single-walled CNTs on SiO_2 the thermal conductance per unit length due to RIP scattering is $g_{RIP} \approx 0.1$ W m^{-1} K^{-1} when the doping level is 0.1 e nm^{-1} (i.e., $\sim 2.5 \times 10^{12}$ cm^{-2}) and the lateral field is >2 V μm^{-1}. Baloch et al. estimated from their measurements on metallic multiwalled CNTs that remote heat transfer via RIP scattering is ~5 times larger (i.e., 84% vs 16%) than heat dissipation via vibration modes that they previously deduced ($g \approx 0.004$ W m^{-1} K^{-1}).[15] We thus approximate $g_{RIP} \approx 0.02$ W m^{-1} K^{-1} for heat transfer by RIP scattering in the experiments of Baloch et al.[11]

To compare these CNT results with our VMTR measurements on graphene interfaces, we assume a width of overlap between the CNTs and the substrates of ~1 nm for the CNTs in the calculations by Rotkin et al. and of ~5 nm for the CNTs in the experiments by Baloch et al. Using these estimated footprints, the average thermal conductance per unit area by RIP scattering across the CNT/dielectric interfaces is derived as 100 MW m^{-2} K^{-1} (Rotkin et al.) and 4 MW m^{-2} K^{-1} (Baloch et al.), respectively. It is interesting to note that the upper limit of the RIP contribution derived from our measurements (1.6 MW m^{-2} K^{-1}) is on the same order of magnitude as that derived from measurements by Baloch et al. The difference is actually in heat conduction by phonons across interfaces of graphene and CNTs, that is, ~50 MW m^{-2} K^{-1} for graphene interfaces[12,13,27] and ~0.8 MW m^{-2} K^{-1} for the multiwall CNT interfaces[15] (estimated using a footprint of ~5 nm).

There are two possible explanations for the different behavior in graphene and CNTs. First, unlike graphene that mostly conforms to the substrates,[28] CNTs do not conform to the substrates and thus the actual contact area for CNTs and the substrates is minute, especially if the substrate roughness is comparable to the nanotube diameter. The minute contact area

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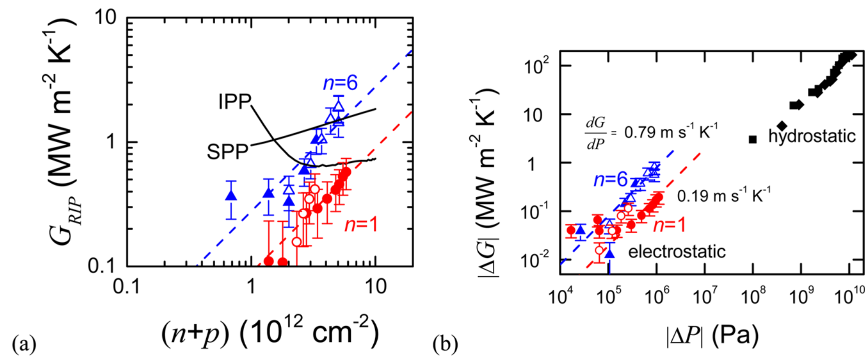

Figure 3. (a) The thermal conductance (G_{RIP}) across graphene/SiO_2 interfaces due to remote interfacial phonons (RIP) scattering, estimated from our VMTR measurements of a monolayer graphene (circles, this work) and a few-layer graphene (triangles, this work) with the assumption that the VMTR measurements are due to RIP scattering. The estimated G_{RIP} is compared with calculations (solid lines) by ref 4 taking into account either static screening of surface polar phonons in SiO_2 (labeled SPP) or hybridization of plasmon in graphene and SPPs in SiO_2 (labeled IPP). The dashed lines are fitted lines in Figure 2. (b) Increase in the thermal conductance (ΔG) of SiO_2/graphene/SiO_2 interfaces of a monolayer graphene (circles, this work) and a few-layer graphene (triangles, this work), as a function of increase in the electrostatic pressure, assuming that the VMTR measurements are due to better conformity of the graphene under electrostatic pressure. The measured ΔG is compared to increase in the thermal conductance of Al/graphene/SiC (squares) and Al/graphene/SiO_2 interfaces (diamonds) due to hydrostatic pressure.[29] The dashed lines are dG/dP of 0.86 and 0.16 m s^{-1} K^{-1} respectively.

diminishes heat conduction by phonons (i.e., vibration modes). Because RIP scattering across nanometer-sized gaps and voids is still substantial,[1] the effective contact area (i.e., footprint) for the remote energy transfer could be significantly larger for nonconformal CNTs. The larger effective contact area enhances the relative contribution of remote energy transfer due to RIP scattering in CNTs. Another key difference is that our measurements are for unbiased graphene without current flowing, whereas the CNT predictions and measurements assumed significant current flow.[7,11] RIP scattering could be an order of magnitude stronger when the charge carriers are driven under high electric field[7] due to, for example, excitation of high-energy SPP modes in the polar substrates by hot electrons in graphene or CNTs. Thus, the low-energy of charge carriers in our unbiased graphene could contribute to low G_{RIP} compared to those measured in biased CNTs.[11] Reference 10 has predicted that for even for graphene, a lateral field >0.5 V/μm could lead to substantial scattering between graphene and RIPs (on SiO_2); however this is a regime that must be examined in future experiments.

We further compare our VMTR measurements to theoretical calculations of interfacial thermal conductance via RIP scattering (G_{RIP}) in Figure 3a. To have a fair comparison, we approximate G_{RIP} during the "off"-state of our VMTR measurements, $G_{RIP,0}$, from the charge concentrations $(n + p)_0$ using the fits in Figure 2b. We then derive $G_{RIP} = \Delta G + G_{RIP,0}$ from our VMTR measurements in Figure 2b and plot G_{RIP} of the monolayer and the few-layer graphene samples as a function of $(n + p)_{TG}$ in Figure 3a. In the same figure, we plot calculations of two models by ref 4 as solid lines. In the first model (labeled "SPP"), the authors assume that the SPPs in the oxide are electrostatically screened but are essentially decoupled from the charge carriers in graphene. With this assumption, the thermal conductance increases monotonically with carrier concentrations, but the dependence is rather weak due to enhanced electrostatic screening at high carrier concentrations, see Figure 3a. In the second model (labeled "IPP"), the authors assume that the SPPs in the oxide are strongly coupled to the plasmons in graphene forming interfacial plasmon-phonons (IPPs). The authors predicted a stronger thermal conductance at low carrier concentrations because the plasmon motion is out of phase with the SPP modes and thus do not screen the SPP modes.[4] We find that predictions of both models contradict the stronger than linear dependence on carrier concentration that we observe in our VMTR measurements, see Figures 2a,b and 3a.

The second possible explanation of the observed increase in ΔG at high gate voltages is that heat flow is enhanced by the electrostatic force exerted by induced charge carriers in graphene, resembling tuning of phononic heat conduction by hydrostatic pressure.[29,30] If this is the case, we expect $\Delta G \sim \Delta(n - p)^2$, where $\Delta(n - p)^2 = (n - p)^2_{TG} - (n - p)^2_0$. $(n - p)$ is derived from the gate voltages as previously described. Using this dependence, we fit our VMTR measurements, see the solid lines in Figure 2a. We also plot the derived ΔG from our VMTR measurements as a function of $\Delta(n - p)^2$ in Figure 2c. We find that our VMTR measurements are slightly better fitted using the assumption that $\Delta G \sim \Delta(n - p)^2$ than the assumption that $\Delta G \sim \Delta(n + p)$, especially at high gate voltages as shown in Figure 2a,c.

In Figure 3b, we compare the measured ΔG of SiO_2/graphene/SiO_2 interfaces due to change of electrostatic pressure to the change of thermal conductance of Al/graphene/SiC and Al/graphene/SiO_2 interfaces due to change of hydrostatic pressure.[29] We estimate the change of electrostatic pressure (ΔP) induced by the gate voltages from $\Delta P = [q^2\Delta(n - p)^2]/(2\varepsilon)$, where $\varepsilon = 3.5 \times 10^{-11}$ F m^{-1} is the permittivity of SiO_2, and q is the elementary charge constant. We plot ΔG as a function of ΔP and find a linear dependence of ΔG on ΔP with a slope of $dG/dP = 0.2{-}0.8$ m s^{-1} K^{-1}. The dependence on ΔP is stronger than dependence of graphene interfaces under high hydrostatic pressure[29] by a factor of ~10, see Figure 3b.

We consider a few possible mechanisms that could engender increase in heat conduction across graphene interfaces under electrostatic pressure. First, the observed ΔG could be caused by strengthening of interface stiffness of graphene/SiO_2 interfaces under electrostatic pressure, similar to enhanced interface stiffness under high hydrostatic pressure.[29] With higher interface stiffness, more high-frequency phonons could transmit through the weak graphene interfaces and thus result in higher thermal conductance. However, we find this

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Nano Lett. 2016, 16, 6014−6020

explanation unsatisfactory due to significantly stronger dependence on ΔP observed in our measurements, compared to that under high hydrostatic pressure. The huge difference is unlikely if the underlying mechanism were the same. Second, the observed ΔG could be due to enhanced near-field radiative heat transfer across smaller gaps between graphene and SiO_2 under electrostatic pressure.[31] This explanation is nonetheless rather unlikely as well, because calculations[31] indicate that near-field radiative thermal conductance across a 1 nm gap is only ~0.05 MW m^{-2} K^{-1} at room temperature, 2 orders of magnitude smaller than our measurements.

Lastly, because graphene is only partially conformal to the SiO_2 surfaces,[27,28] graphene and SiO_2 might elastically deform under electrostatic pressure, resulting in larger contact areas between graphene and SiO_2 and thus higher thermal conductance.[27,32,33] Under elastic deformation of graphene, prior analysis[33] suggests that when ΔP is small, $dG/dP = G_0/(3P_0)$, where G_0 and P_0 are the thermal conductance and pressure without the applied electrostatic fields, respectively. For our VMTR measurements, $G_0 \approx 41$ MW m^{-2} K^{-1} and $P_0 = 10^7$ Pa; thus $dG/dP \approx 1.4$ m s^{-1} K^{-1}, which is on the same order of magnitude as our measurements. Moreover, the difference in dG/dP that we observe in the VMTR measurements of our samples could be readily explained by different degrees of conformity of the graphene flakes from the exfoliation process. We thus propose the enhanced conformity of graphene to SiO_2 substrates under electrostatic pressure as the possible explanation to our measured ΔG.

In summary, we observed an enhancement of heat conduction across graphene/SiO_2 interfaces under electrostatic fields through our accurate VMTR measurements and thus experimentally establish an upper limit for heat conduction by RIP scattering across interfaces of graphene and SiO_2. Unlike predicted for biased CNTs, we find that the contribution of RIP scattering is rather insignificant (<2%) for graphene/SiO_2 interfaces with unbiased graphene. We propose two possible explanations to the measured (but small) increase in the thermal conductance of graphene interfaces, that is, additional heat transfer channel via RIP scattering and better conformity of graphene to the SiO_2 substrates under electrostatic pressured exerted by charge carriers in graphene. We argue that this enhancement of heat conduction under electrostatic fields should be generic to 2D materials that do not fully conform to the polar substrates and could be significantly larger for graphene on rough substrates with poor conformity,[27] for substrates like Al_2O_3,[4] or when the 2D materials carry a large current driven by high source-drain biases, where the RIP heat transfer has been predicted to be enhanced.[4,7,10] Thus, our results could lead to a possible electrostatic approach to control phonon transport in future phononic thermal devices.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b01709.

Fabrication process; sample images and Raman spectra; electrical characterization; sensitivity plots; comparison of raw data of TDTR and VMTR (PDF)

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Notes

The authors declare no competing financial interest.

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Supplementary Information

Role of remote interfacial phonon (RIP) scattering in heat transport across graphene/SiO_2 interfaces

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S1. Fabrication process

Dual-gated graphene field-effect transistors were prepared by nano-fabrication processes as shown in Supplementary Fig. 1.

(a) Graphene flakes were mechanically exfoliated on a SiO_2/Si substrate and a graphene flake is located by an optical microscope.

(b) A PMMA (Polymethyl methacrylate) layer was coated on the substrate at 6000 rpm and baked at 200 ^{o}C for 2 minutes. Two regions of the selected graphene were exposed to the air after e-beam lithography and development processes.

(c) Ti (10 nm) and Au (40 nm) were successively deposited by a thermal e-beam evaporation.

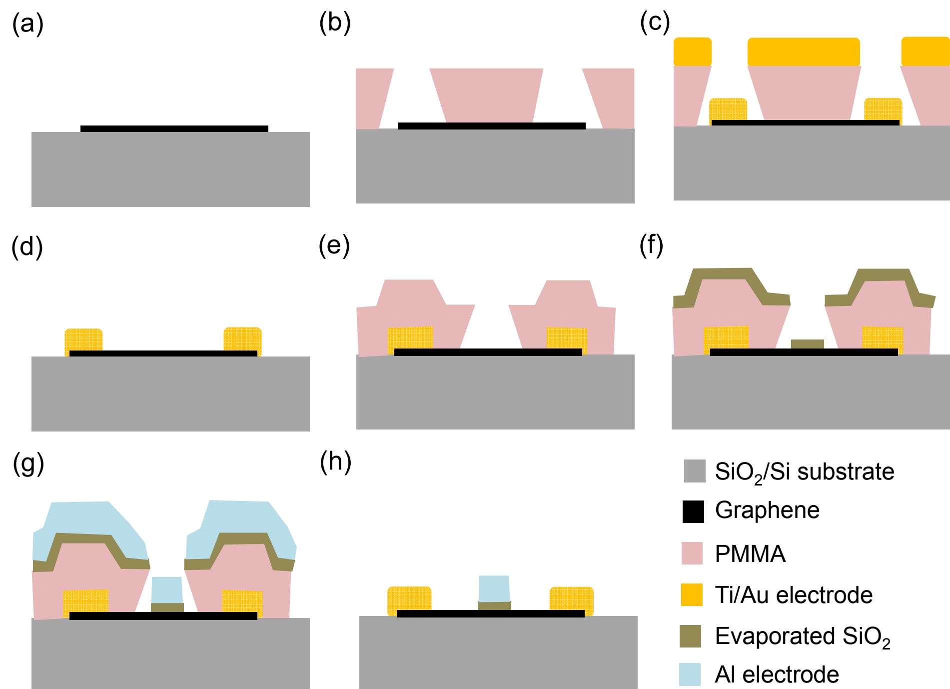
(d) A lift-off process with acetone left a graphene with source and drain electrodes.

(e) With the same recipe of (b) for the PMMA coating and e-beam lithography process, a region between the source and drain was developed.

(f) SiO_2 (~24 nm) was thermally evaporated by an e-beam evaporator at ~8×10^{-7} Torr.

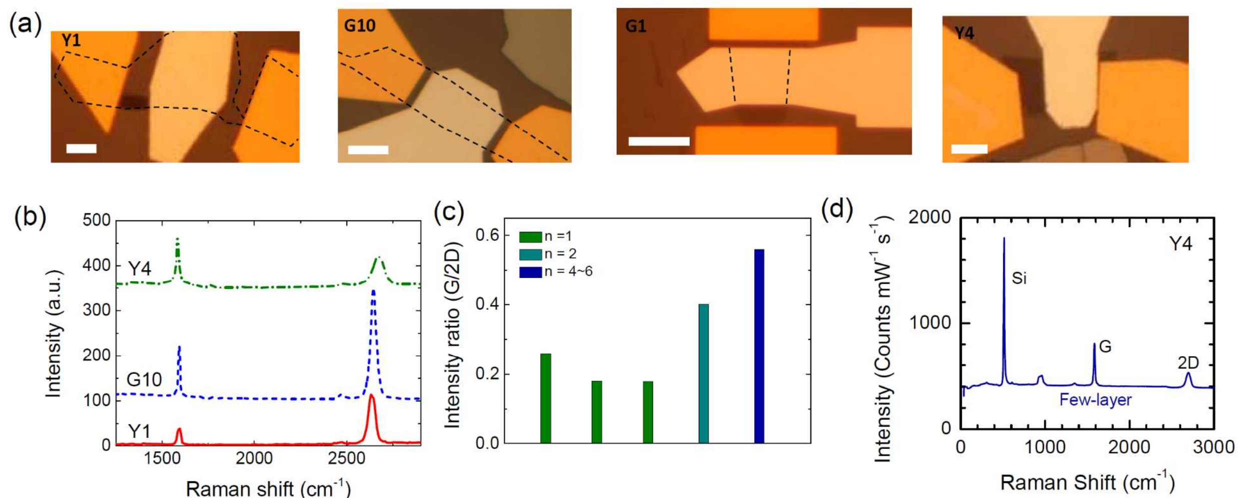
(g) After transferring the substrate to another e-beam evaporator, a Al (90 nm) were deposited.

(h) After a lift-off process in acetone, a top-gated graphene field-effect transistor was completed.



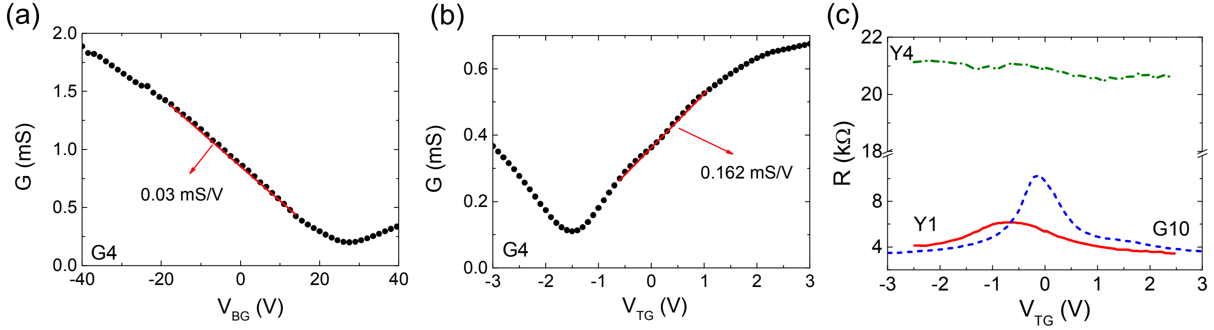
Supplementary Fig. S1 Schematic of fabrication process of a graphene dual-gated field-effect transistor.

S2. Sample images and Raman spectra



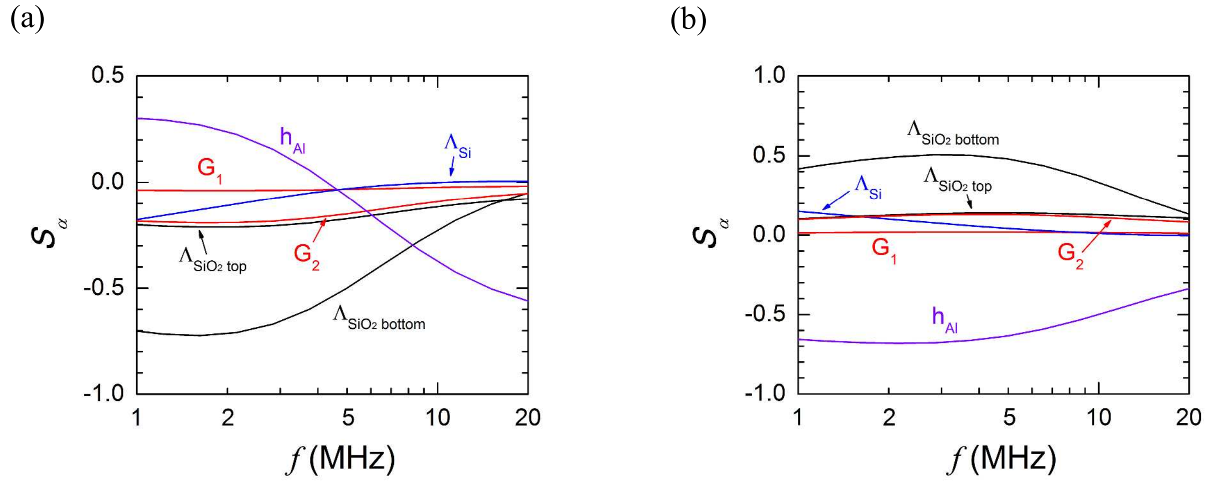
Supplementary Fig. S2 (a) Optical microscope images of samples, Y1, G10, G1 and Y4. Scale bar are 10 µm. (b) Raman spectra of Y1, G10 and Y4. (c) Intensity ratio of G and 2D peak (G/2D) of G4, Y1, G10, G1 and Y4. In Ref. [S1], it has been shown that the G/2D intensity ratio gives the number of graphene layer (*n*): 0.2~0.3, 0.35~0.41, 0.45~0.55, 0.53~0.71 and 0.6~0.8 for *n* = 1, 2, 3, 4 and 6, respectively. Following this report, we assigned *n* as shown in the figure. (d) Raman spectrum of Y4. For the sample Y4, the intensity ratio of G and Si peaks, 0.49 was additionally considered and we confirmed *n* = 6 for Y4 [2].

S3. Electrical characterization



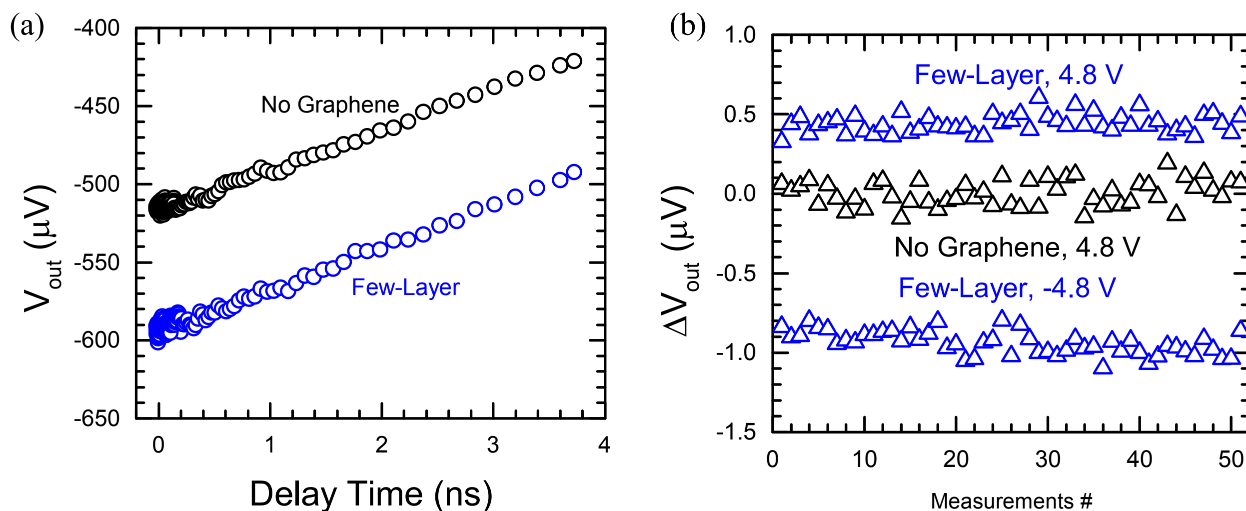
Supplementary Fig. S3 Electrical conductance as a function of (a) back-gate voltage (G-V_{BG}) and (b) top-gate voltage (G-V_{TG}) of G4. Here G-V_{BG} was obtained before defining the top gate. We estimated a low-field mobility from the transfer curve based on a relation of $\boldsymbol{\mu = \frac{L}{W}\frac{1}{C_{ox}}\frac{dG}{dV_G}}$, where C_{ox} is the gate capacitance per unit area and V_G is the gate voltage. The back-gate channel length is L_{BG} = 33.7 μm, top-gate channel length, L_{TG} = 25 μm and channel width, W = 14 μm. With slopes of linear regions in the transfer curves of (a) and (b), indicated by red solid lines, we get mobility of μ_{BG} = 1820 $cm^2V^{-1}S^{-1}$ and μ_{TG} = 1950 $cm^2V^{-1}S^{-1}$, respectively. Here, we used the dielectric constant for both of back- and top-gate SiO_2 layers as 3.9. Since the both mobility for the back- and top-gate effect is the similar value with the same dielectric constant, we confirmed that the thermally evaporated 24 nm thick top-SiO_2 shows the dielectric constant as ~3.9 as a usual value. (c) Resistance vs. top-gate voltage (R-V_{TG}) curves for Y1, G10 and Y4.

S4. Sensitivity plots



Supplementary Fig. S4 (a) Sensitivity of V_{out} signals and (b) V_{in}/V_{out} signals to various parameters used in the thermal model, as a function of modulation frequency *f*. We used the structure of sample G1 for the calculation, which is a multilayered structure consisting of 84 nm Al / 25 nm SiO_2 / exfoliated graphene / 90 nm SiO_2 / Si substrate. The parameters are thermal conductance of Al/SiO_2 interface G_1, thermal conductance of SiO_2/G/SiO_2 interface G_2, thermal conductivity of Si substrate Λ_{Si}, thermal conductivity of top SiO_2 layer $\Lambda_{SiO2\ top}$, thermal conductivity of bottom SiO_2 layer $\Lambda_{SiO2\ bottom}$ and thickness of Al Λ_{Al}. We fix the delay time at -40 ps and 100 ps for (a) and (b) respectively and assume a laser spot $1/e^2$ radii of 4 µm. As illustrated in the figures, we choose to use V_{out} and $f \approx 10$ MHz in our VMTR measurements, to achieve the highest sensitivity to G_2 and lowest sensitivity to other parameters.

S5. Comparison of raw data of TDTR and VMTR



Supplementary Fig. S5 (a) Out-of-phase components of TDTR measurements (V_{out}) on the few-layer graphene sample and a region without graphene on a sample, as labeled. In these measurements, we used a modulation frequency of 10 MHz, a total laser power of ~62 mW and laser spot sizes of ~4 μm. The noise, usually on the order of 2% of the signals (~10 μV), originates from the noise in laser intensity, the variation of phase in the rf lock-in amplifier, etc. From measurements to measurements, the precision of TDTR measurements is on the order of 1% (~5 μV), usually limited by phrase drift in the rf lock-in amplifier. (b) VMTR measurements on the same sample as in (a), using the same laser power and laser spot size as in (a). The "on"-state gate voltages that we applied are as labeled. By averaging 40-100 VMTR measurements as in the figure, we are able to reduce the uncertainty of VMTR measurements to ~0.012 μV, more than 100 times better than the uncertainty of TDTR measurements.

References for Supplementary information

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