Ruben Reyes Curriculum Vitae

Office@RubenReyes.com
408-857-4771
http://www.linkedin.com/in/rubenreyesresume

OVERVIEW

- Structured ASIC from placed-routed
- Co-authored IBM technical papers
- Over 24 years of electrical engineering experience
- Recognized for technical and people leadership
- Business Plan development
- Business acumen
- Business development
- Driven by: career growth and ROI
- Team building
- Technical marketing
- ASIC Methodology Development
- Software development
- Product development
- Technical consulting
- Business savvy and start-up experience
- Team and individual IC Chip design and tape-outs
- Trained in market leader EDA tools: Cadence, Synopsys, and IBM
- Customer-facing roles, sales and business development or product marketing
- Physical design and post tape-out operations
- Largest tape-out 5 million gate design
- Process technology: 0.25um, 0.13um, 0.15um, 0.10um, 90nm, 65nm, 45nm
- Strong common business sense
- Strategic planning and development and implementation of strategic programs
- Working relationships with ASIC and COT customers in the Bay Area
- Good hands-on experience: RTL Synthesis, Floor Planning, Place & Route, Clock Tree Synthesis, Static Timing Analysis, Cross talk & Power Analysis, Physical Verification
- Contingency and risk planning
- Independent contractor
- Project Management

TECHNICAL ACCOMPLISHMENTS

Noted are the highlights.

AMD

Complete RTL to tape-out GDS. Part of a PCIE, GDDR going into a highly complex SOC. Using state of the art methodology and EDA tools and process. Included timing analysis, IR/EM drop methodology development and analysis, DRC/LVS, driving timing closure. Taped out sub-GDDR5 block designs, in production and working.

- TOOLS: SOC Encounter, Calibre, Star-RCXT, Hercules, Apache RedHawk, Perforce (p4), FlowTracer, IC Compiler, Star-RCXT, Primetime, Cadence Finale
- WORK: Synthesis, DFT, Floorplanning, timing optimization, DRC/LVS, place&route, CTS.
- DESIGN: low power using UPF methodology, chip level floorplanning, several blocks, small blocks but technically challenging, IP development (confidential)
- PROCESS: TSMC 32nm/28nm and Global Foundries 28/20nm
- ASIC LIBRARY: AMD internal group IP development, TSMC, Global Foundries

Apple, Inc.

- TOOLS: IC Compiler, Astro, StarRC-XT, Primetime-SI
- WORK: ECO place and route.
- DESIGN: 4 blocks,
- PROCESS: 65nm and 45nm
- ASIC LIBRARY: confidential

Qualcomm, Inc.

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- TOOLS: Qualcomm methodology, First Encounter, Astro, StarRC-XT, Primetime-SI
- WORK: place and route 2 blocks, for their second version of a communications chip. Involved optimizing a few pins for routability and floorplanning, refine the aspect ratio due to increase netlist and follow the Qualcomm methodology.
- DESIGN: 2 blocks,
- PROCESS: TSMC 65nm
- ASIC LIBRARY: Qualcomm and TSMC

Lightspeed, Inc.

- TOOLS: Blast Fusion, StarRC-XT, Primetime-SI
- WORK: Took a Structured ASIC placed design into MAGMA Blast Fusion through routing, extraction and timing analysis (5modes, 2 cases). Used two designs to flush out the design methodology development. Using the TI Pyramid flow as a reference. Worked with teams in the United States and France (TI).
- DESIGN: ARM968 core,
- PROCESS: 90nm and 65nm Texas Instruments
- ASIC LIBRARY: Lightspeed Structured ASIC, SR50LX Texas Instruments

PLX Technologies

- TOOLS: Jupiter-XT, Physical Compiler, Astro, StarRC-XT, Primetime-SI, Astro Rail
- WORK: Chip level floorplanning, modifying the existing floorplan, editing the IO Pads, SerDes PAD placement and routing the Rambus SerDes power routes, IR/EM analysis, std cell and macro placement, CTS, routing, RC extraction, timing analysis w/xtalk and w/o xtalk.
- DESIGN: 500K placed instances, 17 macros, 216 IOs
- PROCESS: 0.13um TSMC
- ASIC LIBRARY: TSMC 0.13um Low Voltage

Morpho Technologies
http://www.morphotech.com/index.html

- TOOLS: Astro v2004.06, StarRC-XT, Primetime
- WORK: Block level floorplanning, placement, CTS, routing, RC extraction, timing analysis, assisting the customer with improving synthesis strategies, improving timing constraints, identifying timing converging issues (i.e. logic level number), timing convergence, power convergence (i.e. reduce die area, gate count, library).
- DESIGN: Reconfigurable DSP IP core, 300K gates, 125 Macros, 1729 IO Pins macro
- The work was very intensive and worked closely with the customer.

Arrow Electronics, Inc.
http://www.arrow.com

- Trained in the LSI LOGIC Flexstream physical design methodology.
- Used Mentor Graphics Calibre DRC/LVS to do DRC and LVS fixing.
- Created and customer adopted my script to do chip finishing: filler cells, spare cells, metal fill, nwell strippiing, and decoupling cap cells.
- Identified poorly designed standard cell causing DRC violations between li-m1 via spacings.
- Identified DRC violation between a non-PLL and PLL IO pad. The only solution to slightly space them apart.
- This was about a two month contract in Los Angeles. I quickly joined the team and hit the road running. At the end, the customer was extremely happy with my team spirit, get-up-to-speed attitude and ethics. Received excellent review from the customer.

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Synopsys, Inc.
http://www.synopsys.com

- Low power and signal integrity ASIC design methodology development from synthesis to GDSII. The tools This included Power Compiler, Floorplan Compiler, Physical Compiler, PC-CTS, Astro, Astro Rail, STAR-RCXT and Hercules.

- Contributed to the TSMC Reference flow version 4.0. We used a TSMC design as our testcase. The design was a 100k instance design. Using the TSMC 90nm process and ASIC standard cell library.

- Extensive IR Drop/EM/cross-talk prevention/analysis/repair using 90nm TSMC technology design flow development, 100k testcase design
- Floorplan Compiler Power Network Analysis design flow development
- Synopsys and Cadence tools design flow development
- Extensive Clock Tree Synthesis design methodology development
- Extensive Synopsys physical design methodology development
- Custom block P&R/extraction/verification using Infineon proprietary design methodology, 60k design
- Cadence physical design methodology development
- DesignWare PCI-X tapeout, gate-level to GDSII, 0.18um process, 60k design
- ARM 500K design P&R/extraction/verification using Cadence GCF methodology
- 0.18um, PCIX interface with FIFOs and off chip RAM test chip, 60k design
- 0.18um, dual-port RAM blocks test chip, Verilog to final GDSII, 10k design
- 0.18um, Single-port RAM blocks test chip, Verilog to final GDSI, 10k design
- Design of an automated physical design environment
- 0.25um, ECO 200 gate & wire change, 3.2M design, hierarchical, team effort
- 0.25um, 3.2M design, 12.6mm^2, custom scripts, Cadence P&R&CTS three large blocks.
- 0.35um, ECO on a graphics chip doing a metal mask change, custom scripts

Cadence Design Systems, Inc.
http://www.cadence.com

- Cadence (consulting for Fujitsu): Physical design, large ECO, affecting m6 block, doing Silicon Ensemble, Qplace, Wroute & Ctgen and Physical design planner extraction. Follow-on to the T3DX project. 2000 gate ECO.
- Cadence (consulting for Fujitsu) : Physical design and ECO, Silicon Ensemble, Qplace, wroute, ctgen & physical design planner, two blocks (m3 & m6), using timing driven routing and placement. Design part of a 13 million transistor chip, measuring 12.6mm x 12.6mm.
- Cadence (consulting for Tseng Labs): In the 3D graphics chips company, worked on correlating the Cadence TLF and Synopsys .lib files. This increased the performance of the timing driven placement tools (Qplace) and detail router.
- Co-authored a technical paper on, “Methodology Assessment for Deep SubMicron Design (Back End Flow) during the Tseng Lab project.
- Cadence (consulting for Tseng Labs): Ruben, lead the back-end Cadence team in the graphics company into doing timing driven routing, the next step in meeting timing for

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deep submicron designs.

- Cadence (consulting for Tseng Labs): Lead technical writer. Writing and editing the back-end methodology assessment project and participated in its delivery.

IBM Corporation (Thomas J. Watson Research Center)
http://www.IBM.com

- Custom physical design (0.25um) of a 64-bit register macro, schematic to final GDSII.
- SKILL programming to improve automation of DRACULA physical verification.
- Extensive mechanical engineering touch screen design.
- Design of the touch sensitive tethered stylus.
- Contribution to the design of the IBM Infowindow product.
- Printed circuit board layout design using the IBM IGS II system
- Design and testing of the analog IO IBM PC interface card.

Documentation

Synopsys

- co-authored the design flow training documentation for field engineers
- Power point presentation to management on signal integrity challenges and physical design solutions.
- Power point presentation to management describing a custom automated scripted environment for ASIC physical design from netlist to DRC/LVS/ANT clean GDSII.
- Documentation on methodology enhancements to the Infineon (Siemens) Highway Flow. Well received by customer. Exceeded customer's expectations.

Cadence Design Systems, Inc.

- Deep submicron technology methodology assessment project. Front to back using Cadence tools.
- Ruben took the lead in organizing and contributing to the documentation for a deep submicron back end design methodology for a graphics company.

IBM Corporation (Thomas J. Watson Research Center)

- Touch screen documentation for assembly and design.
- Touch sensitive stylus documentation for assembly and design.
- Laser Screen Input Device documentation for assembly and design.
- Nose tracker input device documentation for assembly and design.

Technical Expertise

- Low power gates to GDSII design methodology
- Signal integrity gates to GDSII design methodology
- Synopsys synthesis, place and route tools
- Cadence Place and Route and CTS tools
- Shell scripting to automate all my back-end physical design work.
- System-On-a-Chip physical design methodologies.

Pre-Sales

- Cadence (consulting for Tseng Labs): Increased sales revenue by showing through an on-site benchmark of Silicon Ensemble the added value of the soon to be released EDA tool set. Also recognized by Cadence for initiative.

Deep-Submicron

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- Gained a depth of knowledge and experience, during three years at IBM Research performing custom physical design using their 0.25um technology. This included becoming familiar with their dynamic circuits that were timing critical and dictated sizes of metal wires.
- Familiar with issues such as long wire as the dominating factor instead of devices, library migration between technology, and IBM's deep-submicron technology.

PROJECT MANAGEMENT HIGHLIGHTS

NOTE: Details omitted due to company proprietary information.

Project: Place and Route
Resources: Two engineers
Company: Morpho Technologies
Contingency plan: Access to all the tools and engineering resources if needed.
Risk Assessment: New office in San Jose, working remotely to San Diego
Description: Hit the road running and get the project done ASAP. I had another engineer assigned to assist if necessary. Tasks were delegated and milestones again were set. Customer satisfaction was exceeded.

Project: To influence the GUI development and arrive to one.
Resources: Ten engineers
Company: Synopsys, Inc.
Contingency plan: If one GUI did not work, several were in place and working.
Risk Assessment: Alpha code too slow and difficult to use. The look and feel was under development. The competition had working code and adopted by customers. Too many GUIs and one GUI was not enough.
Description: Milestones were set, actions items assigned and followed up to stay on schedule. An online survey was developed to poll the field engineers for more information and justify customer feedback. Product engineers were invited to the weekly meetings to gather their input as well as the customers. Project was a success, survey data and actions items results were fed back to R&D to help in coding the GUI. Management was excited to receive the data.

Project: Benchmark Silicon Ensemble4.5 and Wroute against Cell3 and groute/froute
Resources: One place and route engineer
Company: Tseng Labs (consulting for Cadence Design Systems, Inc)
Contingency plan: If production code failed, beta code would be used.
Risk Assessment: Production code threatened by competition, beta code not fully tested and chance of failure in real design.
Description: This project involved working at the customer site. Setting milestones, collecting data points using customer's actual design, presenting to customer engineers and management the enhanced performance of Silicon Ensemble4.5 over Cell3. Results were well received and adopted quickly in the current flow.

Project: Custom layout for CPU design and develop a methodology to estimate custom layout work
Resources: Three custom layout engineers
Company: IBM Thomas J. Watson Research Center
Contingency plan: Worked actually required one layout engineer. With Three, layout effort was divided among the three and weekly meetings allowed anyone to takeover in case of absence. We set requirements to accept schematics before accepting layout to reduce throw away work.
Risk Assessment: Vacation, sickness, and unexpected layout changes.
Description: Working with three other custom

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layout engineers, milestones were created to keep the project on track and check progress, weekly meetings to check status and assess risk and address critical issues. The project successfully delivered the custom blocks and documentation on how to set a schedule based on the number of devices to be drawn.

PUBLISHED TECHNICAL PAPERS

1.	February 1993	IBM Corp.	"Optical Contact Sensor for Input Stylus," R.L. Garwin, J.L. Levine and R. Reyes. IBM Technical Disclosure Bulletin, Vol. 36, No. 02, pp. 477. Y0890-0940. JLB.
2.	January 1996	IBM Corp.	"Self-Resetting Logic Register and Incrementer". Acknowledgement for physical design.
3.	September 1987	IBM Corp.	"Ultrasonic Contact Sensor for a Handwriting Stylus" Levine, J. L. and Schappert, M. A. and Reyes, R. IBM Research Internal Document, RC-13100
4.	June 1987	IBM Corp.	"An Electronic Podium for the Classroom" Levine, J. L. and Schappert, M. A. and Reyes, R. Published in 1987 SID International Symposium Digest of Technical Papers.
5.	November 1986	IBM Corp.	"Electronic Podium for Classroom Use" Levine, J. L. and Garwin, R. L. and Schappert, M. S. and Reyes, R. Published in the ITL Displays Journal no. 1186 p5-7
6.	November 1991	IBM Corp.	"An Add-on Touch Screen Using Strain Gauge Sensors" Levine, J. L., Garwin, R. L., Reyes, R., Schappert, M. A. ITL- Terminals and Displays. Raleigh, NC. p88-93
7.	November 1990	IBM Corp.	"An Add-on Touch Screen Using Strain Gauge Sensors" Levine, J. L., Garwin, R. L., Reyes, R., Schappert, M. A. IBM Research Internal Document, order no. 91A 00588
8.	September 1990	IBM Corp.	"An Add-on Touch Screen Using Strain Gauge Sensors" Levine, J. L., Garwin, R. L., Reyes, R., Schappert, M. A. ITL- Terminals and Displays. Hursley, England. P69-73

EMPLOYMENT/CONTRACT EXPERIENCE

RUBEN REYES. Sunnyvale, California DATE- 2014
Physical Design and Project Management
Physical Design Consultant

AMD. Sunnyvale, California 2014 - 2011
Physical Design
Member of Technical Staff

Complete RTL to tape-out GDS. Part of a PCIE, GDDR going into a highly complex SOC. Using state of the art methodology and EDA tools and process. Included timing analysis, IR/EM drop methodology development and analysis, DRC/LVS, driving timing closure.

- TOOLS: SOC Encounter, Calibre, Star-RCXT, Hercules, Apache RedHawk, Perforce (p4), FlowTracer, IC Compiler, Star-RCXT, Primetime, Cadence Finale
- WORK: Synthesis, DFT, Floorplanning, timing optimization, DRC/LVS, place&route, CTS.
- DESIGN: low power using UPF methodology, chip level floorplanning, several blocks, small blocks but technically challenging, IP development (confidential)
- PROCESS: TSMC 32nm/28nm and Global Foundries 28/20nm
- ASIC LIBRARY: AMD internal group IP development, TSMC, Global Foundries

RUBEN REYES. Sunnyvale, California 2013 - 2008

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Physical Design and Project Management

Senior Physical Design Consultant

Responsible for block place and route down to 20nm, part of a highly complex SOC. Using Cadence SOC Encounter, MAGMA Talus or Synopsys ICC. Developed customs flow as needed. Taking a design from netlist through tape-out GDS2. Mentoring engineers. Contract negotiation. Working with multi-site project and engineers. Physical verification, DRC/LVS with Hercules/Calibre. Timing ECO with Primetime. Built a team for physical design and drove project, process and IP vendor. Project manager for team of engineers: resource, scheduling and deliverables. Working and driving the CAD team to bring up design flow.

Recent projects are:

AMD

Complete RTL to tape-out GDS. Part of a PCIE, GDDR going into a highly complex SOC. Using state of the art methodology and EDA tools and process. Included timing analysis, IR/EM drop methodology development and analysis, DRC/LVS, driving timing closure. Developed methodology and implemented reversing the design and doing eco place and route.

- TOOLS: SOC Encounter, Calibre, Star-RCXT, Hercules, Apache RedHawk, Perforce (p4), FlowTracer, IC Compiler, Star-RCXT, Primetime, Cadence Finale
- WORK: Synthesis, DFT, Floorplanning, timing optimization, DRC/LVS, place&route, CTS.
- DESIGN: several blocks, small blocks but technically challenging, IP development (confidential)
- PROCESS: TSMC 32nm/28nm and Global Foundries 28/20nm
- ASIC LIBRARY: AMD internal group IP development, TSMC, Global Foundries

SYNAPSE, INC.

SOC Encounter & Hercules to check/fix DRC/LVS violations. Primetime to implement timing ECOs. Ground up physical design flow.

- TOOLS: SOC Encounter, Primetime, Hercules
- WORK: Fix DRC and LVS violation using SOC Encounter and Hercules. Implement timing ECOs using Primetime. Worked with teams in the China and Texas.
- DESIGN: one block, 1 million placeable instances (4 million gates)
- PROCESS: TI 40nm
- ASIC LIBRARY: Synopsys 40nm

CHIPSTART, LLC.

- TOOLS: Salesforce (CRM)
- WORK: Negotiated win-win solutions for the vendors. Data mining, lead generation, and qualifying leads. Responsible for the IC design services and IP sales & business development for the corporation in the Bay Area (Northern California). Managed immediate business accounts. Continued researching and fact-finding to develop or modify internal client´s information. Focused on driving the company's internal and external operations, engineering, developing customer solutions, business development and sales channel setup. Developed and close to over 300 qualified contacts and established relationships for business development. Used LinkedIn, Twitter, Facebook for lead generation. Contract negotiations, project management & scheduling, engineering consultant interview/hiring, cold calling, creating Statement of Work, human resources, developing business plans, developing profit and loss, marketing services and overseeing all other necessary business operations in my designated area. Created presentations, conducted high level technical/business meetings, negotiate pricing and business terms, manage contract negotiation, closed deals as well as monitor project deliverables and managed projects. Worked with executive management, engineering, legal, marketing and finance to define and close new core IP business opportunities. Managed revenue opportunities and customer relationships.

GLOBAL TRIVIUM CORP 2008 - 2009

Founder and Chief Operating Officer
849 Hollenbeck Avenue
Sunnyvale, CA 94087
408-857-4771

- Responsible for company's internal and external operations.
- Interviewing and placing engineering consultants
- Working with and developing customer solutions
- Establishing and building company’s sales channel
- Selling our design consultants for on-site or off-site technical services

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QTHINK, INC. 2004 - 2008

Engineering&Design Services Group
90 Bonaventura Drive
San Jose, CA 95134
408-240-1137

- Methodology assessment and development
- Technical lead for several netlist to tapeout GDSII projects using Astro/Cadence/Magma EDA tools
- Local LINUX/UNIX system admin person
- Involved in interviewing engineers
- Mentored junior engineers
- Managed the network and computing hardware
- Created and managed intellectual database through company internal web

ARROW ELECTRONICS, INC. 2004

Engineering&Design Services Group
20935 Warner Center Lane
Woodland Hills, CA 91367
818-932-1000

- 2 month contract, July to September, contract through QThink, Inc.
- Joined the Arrow team and quickly learned the LSI LOGIC methodology.
- Created and reduced the effort in doing chip finishing.
- Used Calibre DRC/LVS and Astro to debug/fix DRC/LVS and placement violations.
- This was an on-site project working closely with the customer.

SYNOPSYS, INC. 2003 – 1998

700 East Middlefield Road
Mountain View, California
650-584-4860 (main telephone #)
Compensation: CONFIDENTIAL

- Developed/initiated/influenced product requirements for Power Network Analysis/Synthesis. Low power methodology innovations. Proposed/influenced CTS, Routing, and floorplanning methodologies/enhancements. Created/executed test plans. Performed CTS and routing benchmarks. Published technical papers for the Synopsys engineering community. Created/supported CAE forums to enforce communication.Taped out several IP designs to silicon, from Verilog to GDSII. Developed physical design methodologies & environments using Cadence, Synopsys and Milkyway based tools. Created an automated ASIC design methodology for performing test chip tape-outs.
- Responsibilities: Milkyway support and development, gain expertise in customer's ASIC flows, supervising, good knowledge of ASIC low ////////power design methodologies, communication skills and leadership. Knowledge of EDA tools in the following areas: logic synthesis, simulation, timing analysis, physical design & routing, and library development. Writing technical papers, place&route benchmarks, front to back consulting, working with

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CTS/power/routing/floorplanning R&D, writing scheme/Korn/csh/sed/awk scripts, tape-outs of test chips, Milkyway, and Cadence tools consulting.

- Lots of physical design presentations and instruction to the Physical Synthesis Business Unit.
- Taped out several designs to silicon, from Verilog to test house.
- Developed physical design methodologies & environments using Cadence, Synopsys and Avanti tools.
- Experienced in: Primetime, Design Compiler, Physical Compiler, Arcadia, FlexRoute, Chip Architect.
- HIGHLIGHTS
  - Several testchips (0.25um)
  - Cadence tools consultant
  - Routing technology contribution
  - Floorplanning technology contribution
  - CTS technology contribution
  - Tools flow consultant
  - All Synopsys GUI contribution
  - Power Network Synthesis contribution
  - Low Power Design Methodology contribution
  - Place and Route Suite (PRSuite) evaluation
  - Physical Compiler – Astro testing (SDC/Library)

CADENCE DESIGN SYSTEMS, INC. 1998 – 1996
San Jose, California

- Hands-on management: design schedules, project documentation, Microsoft Project & Powerpoint. Completed several Place&Route projects that were taped out. Wrote many UNIX Korn shell scripts to automate and do batch mode Place&Route
- Responsibilities: supervising, ASIC design methodology consulting, writing technical papers, Verilog to GDSII tape-outs, routing benchmarks, and IBM technology consulting.
- HIGHLIGHTS
  - Deep submicron design methodology consultation
  - Traveling 80% of time
  - Tape-outs using 0.25um technology
  - Expertise in Silicon Ensemble, CTGEn, Wroute, LEF/DEF

IBM Corp. **1996 – 1982**
Thomas J. Watson Research Center
Thomas J. Watson Research Center
Yorktown Heights, New York
914-945-3000 (main telephone)

- Worked on IBM's leading edge submicron technology in custom physical design & methodology. Worked on a custom physical 64-bit register, using IBM technology. Custom physical designers: proactive and initiated direction, prepared schedules and evaluated progress. Conducted weekly

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meetings and prepared reports to stay on schedule. Established/supported remote verification for the custom physical design team.

- Worked on several IBM chips and products: PowerPC 630 chip, TouchSelect, 4055 Infowindows, 8516 Touchscreen, and the Advanced Technology Classrooms, & systems on a chip(ASIC). Familiar with SKILL language. Used Analog Artist, Layout Editor and simulation(SPICE & ASX), verification(Dracula, Niagara, DIVA). Research&Development of touchscreens and pressure sensitive stylus. Prototype design of a handwriting recognition stylus, Touchscreen bezel, industrial touch screen and test equipment. Board level design: Butterworth filters with op-amps, wire-wrapped boards, board layout with IBM IGSII system. Negotiated with vendors for best service and pricing. Spreadsheet analysis for parts needed for touchscreen prototypes. Managed technician building prototypes.
- Responsibilities: supervising, custom layout design, mechanical engineering, board level design, applied physical sciences research.
- Worked with IBM's leading edge submicron technology (cmos5x and cmos7) in custom physical design. As well as setting up a design methodology for measuring performance when doing custom physical design.
- Designed a custom 64-bit register, using IBM technology, hard block for a CPU chip for the datapath. Using cmos5x, 0.25micron IBM technology. Physical design and verification (IBM Niagara and Cadence Dracula)
- Created and lead in establishing one way of doing remote verification for his custom physical design team.
- HIGHLIGHTS
  - Applied research in the physical sciences
  - High performance CPU design
  - Using the latest IBM technology & EDA tools (Cadence)
  - Trained in IBM's Advanced RTL to GDSII design metho
  - Schematic to layout
  - Physical verification

Designs of analog filters using op-amps.
CMOS Physical Design of Standard Cells (using IBM proprietary technology).
comparators
latches
logic gates
CMOS Circuit Design of Standard Cells.
MUX's
16bit ripple-through carry look-ahead adder
I took an intensive CMOS design course by IBM and instructors from Columbia, Cornell, and MIT. In my graduate course work, I concentrated in digital signal processing (my interest). Involved in high performance CPU design custom layout.

EDUCATION and BEYOND

"The illiterate of the 21st century will not be those who cannot read and write, but those who cannot learn, unlearn, and relearn" Alvin Toffler, from *"Rethinking the Future"*

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Certificate	Business Management	DeAnza College Cupertino, California	Spring 2004 Spring 2003 Pass
Certificate	Supervisory Management	DeAnza College Cupertino, California	Winter 2003 Fall 2003 Pass
Certificate	Planning & Managing Projects	IPS Project Management Program	Spring 2001 Pass
Master Of Science	Electrical Engineering	Polytechnic University Brooklyn, New York	January 1995 Fall 1991 GPA 3.00
Certificate	Custom Integrated Design	IBM Thomas J. Watson Research Center / Cornell University / MIT / Columbia University	January 1993 August 1993 Pass
Bachelor Of science	Electrical Engineering with honors	Pratt Institute Brooklyn, New York	Winter 1991 Fall 1986 GPA 3.447
Diploma	Electrical Engineering Technology	DeVry University Woodbridge, New Jersey	October 1982

EDA TOOLS (hands-on, tape-outs, working knowledge)

Company: Qualcomm
First Encounter, Astro, Primetime-SI, Customer's Own Tooling and flow methodology

Company: Arrow Electronics, Inc.
Company methodology LSI LOGIC Flexstream 3.3
Calibre DRC/LVS

Company: Synopsys, Inc.
Design Compiler
Physical Compiler
Given a Synopsys setup file and design constraints file.
Floorplan Compiler
Physical Compiler(CTS)

Company: Avanti
Milkyway
Astro
Astro DRC/LVS/ANT
Hercules
Astro Rail

Company: Cadence Design Systems, Inc.
Silicon Ensemble (groute, froute, power planning, LVS, DRC)
CtGen
Wroute
PEARL static timing analyzer
Dracula
Analog artist
INQUERY
Compactor
FASTNET (Cadence RC extractor)
CDC (Cadence Delay Calculator)

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HyperExtract (Cadence detail RC extractor)
Preview w/Cell3
CELL3
Device Level Editing
DIVA
Cadence Licensing
Cadence Tool installation
DFII
Netlister (Cadence)
PCells (Cadence)
LAS
Layout Editor Plus
Virtuoso

Company: IBM Thomas J. Watson Research Center
BULLDOZER(device tuning)
NIAGARA(DRC/LVS)

PARTIAL LIST, FORMAL EDA TOOL TRAINING

TOOL	COMPANY	DATE
Custom Integrated Design Training Program	Thomas J. Watson (IBM) Research Center	August 1993
Advanced CELL3 Ensemble	Cadence	June 25, 1996
Silicon Ensemble	Cadence	October 11, 1996
IC Craftman	Cooper&Chyan Technology	January 28, 1997
Physical Design Planner	Cadence	June 19, 1997
Chip Synthesis	Synopsys	1998
TDL Saturn	AVANTI	February 11, 1999
Apollo Fundamentals	AVANTI	March 10, 1999
Blast Fusion, Blast Rail, Blast Plan Pro, Blast Create	MAGMA	March 2006
Planet PL	AVANTI	March 12, 1999

SEMICONDUCTOR PROCESSES

I have taped out and/or understand the DRC rules for the following process

TSMC 65nm
TSMC 90nm
TSMC 0.18um
TSMC 0.25um
TSMC 0.35um
IBM CMOS7X
IBM CMOS5X
SAMSUNG 65nm
Global Foundry 20nm
TSMC 28nm

INTERNATIONAL WORK ASSIGNMENTS

1. Two weeks in Germany working and training at Infineon to do place and route, engage the customer and answer technical questions.

LEADERSHIP ACTIVITIES

1. Pratt Institute Student Trustee
2. Eta Kappa Nu President
3. Owner/President of Universal Images
4. Pratt Institute Student Committee Chairman

WELL RECEIVED PRESENTATIONS/PAPERS

1. Signal integrity in placement and routing and LEF using Cadence tools.
2. What are the challenges for signal integrity and low power methodology.
3. Standards for synthesizing a power network to meet IR and EM constraints.

Ruben Reyes Curriculum Vitae

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PROGRAMMING LANGUAGES

Working knowledge, from simple scripts to parse a text file to elaborate scripts to automate a backend job.

TcL	C-shell and Korn-shell	BASIC
PERL	C	Assembler
SED	Pascal	
AWK	FORTRAN	

OPERATING SYSTEM

UNIX	WINDOWS	MAC OS
AIX	DOS	

COMPUTER SKILLS

WORD	Excel	Eudora
Powerpoint	Outlook	

MANAGEMENT SKILLS

Hiring	Mentoring	Project management
Interviewing	Coaching	

INCREASING SALES REVENUE

- Very methodical in my work and focused. This increases productivity and can be duplicated by others involved. Reduces repetitious work and reduces cost and increases quality of results.
- I drive projects with the ends in sight.
- Improving QOR (Quality Of Results) through team building, aggressive and attainable milestones, and team recognition.

BUSINESS SKILLS

Contracts	Presentations	Business planning
Negotiations	Budgeting	

AWARDS AND RECOGNITIONS

Synopsys, Inc.
DesignWare PCI-X tapeout, gate-level to GDSII, 0.18um process, November 20, 2000.
Cadence Design Systems, Inc.
Q1 1997, *Customer Satisfaction Award*: Tseng Labs “Bruins II” project completed succesfully
August 1997, *Special Achievement Award*: customer adoption/purchase of SiliconEnsemble5.0
IBM Corporation:
December 1995, *IBM Research Division Technical Group Award*: *PowerPC* First RIT & Stand Alone Bring Up.
May 1994, *IBM Research Division Technical Group Award*: *PowerPC* 630 April 30th Checkpoint Achievement.
January 1992, *IBM Research Division Award*: technical contribution to manufacturing, *IBM TouchSelect* product.
January 1987, *IBM Research Division Award*: touch-screen terminal design assistance, *IBM*

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4055 Infowindows product.

Pratt Institute:
President's (1989, 1990, 1991) and Dean's (1989) List
Certificate of Excellence (May 1991): award for Outstanding Service to the School of Engineering.
Search Committee for the Dean of Engineering (Spring 1991)
Community Standards Review Committee (Fall 1990 - Spring 1991)
Board of Trustees' Standing Committee on Education (Fall 1991 - Date)
Board of Trustees' Standing Committee on Student Affairs (Fall 1991 - Spring 1992)
Chairman for the Board of Trustees' Standing Committee on Student Affairs (Fall 1992 - Spring 1993)
Graduate Student Trustee on the Pratt Institute Board of Trustees (Fall 1991 - Fall 1993)

PROFESSIONAL MEMBERSHIPS

Tau Beta Pi (Engineering Honor Society)
Eta Kappa Nu (Electrical Engineering Honors Society, Chapter President: 1990 to 1991)
I.E.E.E.

Detail Tool Experience

IC Compiler (Synopsys)

1. Hierarchical ECO, since the flat ECO had problems.
2. Performed floorplan exploration, using the ICC scripted design flow.

BlastFusion (MAGMA)

3. Routed a block placed by LightSpeed placer (a tool from their Structured ASIC design methodology).
4. The technology process was TI 65nm and libraries created by LightSpeed.

First Encounter

5. Used the tool to examine the floorplan and edit the IO Pin placement.
6. Wrote out the DEF/LEF
7. Save the design database
8. Did a fast route to examine the routing congestion.

Physical Compiler

1. Examine constaints
2. Initial placement and refine placement
3. CTS
4. detail routing
5. write/read DEF
6. graphical viewer to examine floorplan, edit placement properties

mantle

1. Used the tool in the MAGMA boot camp using a test case.

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PEARL static timing analyzer

1. Took a Cadence PEARL class to learn about the tool.
2. Used to create the GCF file from a Synopsys timing constraint file.
3. Used PEARL command to figure out the maximum frequency before getting negative slack.

CELL3 and Preview

1. On the job training in CELL3 and Preview.
2. Used a customer design to benchmark against Silicon Ensemble 4.5

Silicon Ensemble 4.5 through 5.3

1. Trained in Silicon Ensemble and Advanced Silicon Ensemble.
2. Used for floorplanning block and flat chip designs.
3. Creating power grids and saving it as DEF files
4. Saved designs as DEF to read into stand alone wroute(detail router).
5. Saved the command files to create batch scripts and run several batch jobs.
6. Used groute and froute to repair scenic routes.
7. Search and repair, using a small sbox, to fix shorts or congested areas.

Astro Experience

1. (Infineon) using Scheme scripts to automate place and route withing the Infineon Highway Flow
2. Create power and ground rails (graphically and Scheme script)
3. Use the Astro to capture and edit the Scheme command to automate the batch runs
4. Create the design library
5. Create the reference library
6. Place and Route of block designs
7. Automated clock tree synthesis feature
8. Routed the clock tree with non-default rules, different layers, wire spacing to prevent crosstalk problems
9. Familiar with Astro SI repair and Primetime-SI analysis
10. Involved in the development of Astro rail using Power Compiler(Synopsys) and Floorplan Compiler(Synopsys)
11. Ran Astro Rail power analysis to generate the input for Astro Rail analysis
12. Created the electromigration rules input setup file to perform Astro rail analysis on the power and grounds
13. Search and repair of block designs (local or the entire area)
14. Flow development using Physical Compiler(Synopsys) --> Astro

Astro Rail

1. Developed the setup file for Astro to read the electromigration rules for each metal and maximum IR drop.
2. Created and developed the scheme scripts to automate the process of doing power analysis and rail analysis using Astro.
3. The flow did not use a SAIF (switching activity input file) input, but used the default and that is the probability of a node switching. A switching probability of 30% was used.
4. Power map was used to compare it

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against Floorplan Compiler's PNA. The results were off by about 5 percent.

MILKYWAY

1. (Infineon) using Scheme scripts to automate place and route withing the Infineon Highway Flow
2. Create power and ground rails (graphically and Scheme script)
3. Use the Astro to capture and edit the Scheme command to automate the batch runs
4. Create the design library
5. Create the reference library
6. Place and Route of block designs
7. Automated clock tree synthesis feature
8. Routed the clock tree with non-default rules, different layers, wire spacing to prevent crosstalk problems
9. Familiar with Astro SI repair and Primetime-SI analysis
10. Involved in the development of Astro rail using Power Compiler(Synopsys) and Floorplan Compiler(Synopsys)
11. Ran Astro Rail power analysis to generate the input for Astro Rail analysis
12. Created the electromigration rules input setup file
13. Search and repair of block designs (local or the entire area)
14. Flow development using Physical Compiler(Synopsys) --> Astro

REFERENCES

NAME	TITLE	COMPANY	RELATIONSHIP	CONTACT INFORMATION
Dr. James L. Levine	IBM Research Staff Member	IBM Thomas J. Watson Research Center	1st line manager	IBM Corp. P.O. 214 Yorktown Heights, NY 94045 levine2@us.ibm.com 914-945-1174
Yimin-Jiang	R&D engineer	Synopsys, Inc.	Team member	Synopsys, Inc. Yimin.jiang@synopsys.com
Hiroshi Ishikawa	Engineer	Synopsys, Inc.	Team member physical design engineer	Cadence Design System, Inc. hiro@cadence.com 408-944-7142
Oliver Omeisel	Engineer	Synopsys, Inc.	Team member ASIC design engineer	Cadence Design System, Inc. oliver@cadence.com 408-576-3607