RVFPGA:

The Complete Course in Understanding Computer Architecture

The Movement to Open-Source Hardware

Prof. David Patterson speaking to the RVfpga team on 6th May 2020:
"RISC-V is simple, real, and will pervade every computing level in the next 5 years. The distinguishing feature is the basic Instruction Set. All the extras are in optional extensions. Openness sparks collaboration and global participation!"

Introduction

RISC-V is an open standard instruction set architecture (ISA) based on established reduced instruction set computer (RISC) principles. Unlike other ISA designs, this ISA is provided under open source licenses that do not incur fees. Many companies are offering RISC-V hardware, with more to follow. Open-source operating systems with RISC-V support are available and the instruction set is supported by popular software toolchains.

The RVfpga course provides the foundation knowledge and hands-on experience that the next generation of Programmers and Engineers need to harness the potential of RISC-V. It consists of 20 Labs with detailed instructions, examples, short questions and practical exercises with solutions, giving you the teachers flexibility to choose between a practical and an exam-based structure for the course at your faculty.

The RVfpga package provides instructions, tools, and labs that show how to:
- Target a commercial RISC-V system to an FPGA
- Add more functionality to the RISC-V system
- Analyze and modify the RISC-V core and memory hierarchy

The RVfpga system uses the Chips Alliance's SweRVolf SoC, which is based on Western Digital's RISC-V SweRV EH1 core. The SweRV is a fully-verified production level processor core, that is fully open-source, and now being used by several SoC designers including Imagination Technologies, the leaders of this project, in their A series GPU.

The Authors

The course materials were developed by Dr. Sarah Harris, Associate Professor of Electrical and Computer Engineering at University of Nevada, Las Vegas (U.S.A.). Dr. Harris co-wrote the popular book, *Digital Design and Computer Architecture*, now in its fourth edition, RISC-V version, which will be published in 2021.

Dr. Daniel Chaver-Martínez, Associate Professor of Department of Computer Architecture and System Engineering at Universidad Complutense de Madrid (Spain).

Target Courses

Digital Design & Microarchitectures (BSc), Computer Organisation & Architecture, Advanced Computer Architecture (BSc, MSc), SoC design (MSc), Design Verification (MSc), Embedded Systems projects (BSc, MSc) and Processor Architecture: modifications, enhancements, optimisation…(MSc, PhD)

Duration

The complete course runs for three one-semester course to illustrate the key points and give students hands-on experience -- Computer Fundamentals (1st part), Computer Organization (2nd part) and Computer Architecture (3rd and 4th parts).

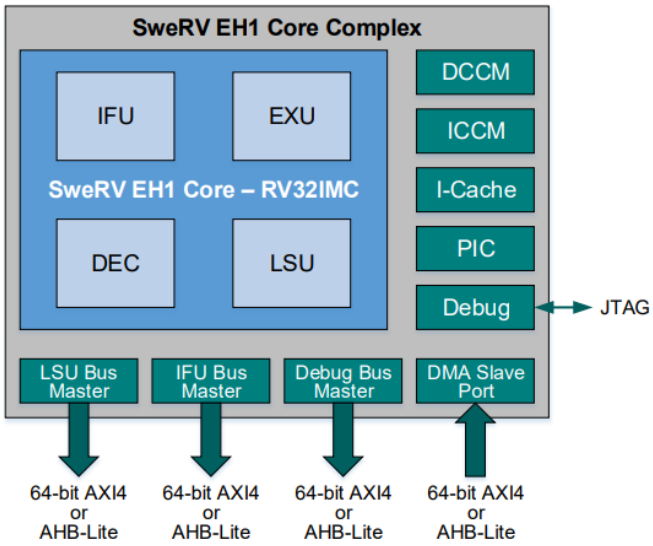
Tools Required

Software

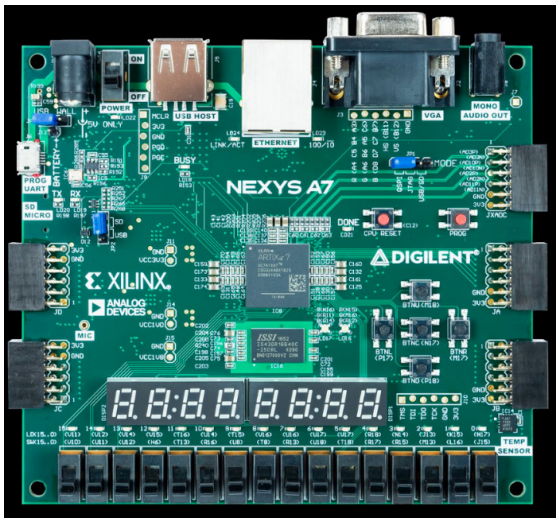
- Xilinx Vivado 2019.2 WebPACK
- Microsoft's Visual Studio Code
- PlatformIO with Chips Alliance platform, which includes: RISC-V Toolchain, OpenOCD, Verilator HDL Simulator, WD Whisper ISS.

Hardware

- Digilent's Nexys A7 or Nexys 4 DDR FPGA Board
- RISC-V Core & SoC:
  - Core: Western Digital's SweRV EH1
  - SoC: Chips Alliance's SweRVolf



Western Digital EH1 SweRV Core



Digilent Nexys A7 FPGA board with Xilinx Artix 7 XC7A100T

Contents

Lecture Topic	Details
Lab 0	Introduction - Direct to Quick Start Guide or Getting Started Guide - Overview of Tools - Overview of Labs
Lab 1	Vivado Project - Simulation (Verilator). - Creating a Vivado project using SweRVolf RTL (Verilog), generating a bitfile and downloading it onto the Nexys A7 FPGA board.
Lab 2	C Programming - Example C program - Boot code - Exercises
Lab 3	Assembly Programming - Simulation - using Whisper, the SweRV-ISS, Instruction Set Simulator - Boot code - Exercises
Lab 4	Function Calls - RISC-V ABI - Procedure Calling Convention - Exercises
Lab 5	C with Assembly Code - Embedding assembly code with C code - Exercises
Lab 6	Introduction to I/O - Program-driven GPIO - Overview of Nexys A7 I/O - C and Assembly Programs - Exercises
Lab 7	7-Segment Displays - Build 7-segment display decoder for driving Nexys A7's built-in 7-segment displays - Examples in C and assembly - Exercises
Lab 8	Interrupt-driven GPIO - Introduction to SweRVolf's interrupt support - Overview of the main changes to the controller - Examples in C and assembly - Exercises
Lab 9	Timers - Understand the timer controller obtained from Opencores (https://opencores.org/), an online community for the development of gateware IP (Intellectual Properties) Cores in the spirit of Free and Open Source collaboration. - Examples in C and assembly - Exercises

Lecture Topic	Details
Lab 10	Serial Buses - SPI, I2C, and UART - Understand the serial bus controllers obtained from OpenCores. The controllers that you will use in this lab are available at: https://opencores.org/projects/uart16550 (UART, which is provided inside SweRVolf), https://opencores.org/projects/i2c (I2C) and https://opencores.org/projects/simple_spi (SPI). - Examples in C and assembly - Exercises
Lab 11-15	Understanding and Modifying the RISC-V Datapath - Diagram of the core structure - Instruction flow through the pipeline (Arithmetic/Logic, Memory, Jumps, and Branches) - Hazards and how to deal with them - Implement new instructions and execute them on the board (use - Understand the Branch Predictor and make some changes to it - Understand superscalar processing
Lab 16-20	Understanding and Modifying the RISC-V Memory Hierarchy - Understand the operation of the memory hierarchy including cache hits and misses. - Test different cache sizes, configurations and management policies - Understand the cache controller - Understand the ICCM and DCCM

Release Dates & Languages:

- November 2020: RVfpga Getting Started Guide, RVfpga Quick Start Guide, RVfpga Labs 1 to 10 (Parts 1 & 2)
- March 2021: MSc-level SoC Design Course Autumn 2021: RVfpga Extended Labs 11 to 20 (Parts 3 & 4)
- All materials will be delivered in English & Chinese (Spanish & Japanese in plan)

Complementary Materials:

- A series of video tutorials given by Prof. Sarah Harris and Prof. Daniel Chaver-Martinez are in preparation
- A global programme of online and in-university workshops are planned for 2021
- The popular textbook *Digital Design & Computer Architecture: RISC-V Edition 2021* which provides a uniquely relevant accompaniment to RVfpga
- *Computer Organisation and Design* by David Patterson and John L. Hennessy remains the "bible" for these activities
- Relevant textbooks: http://university.imgtec.com/resources/books/

Support:

- The RVfpga forum is specifically for technical questions about RVfpga https://university.imgtec.com/forums/rvfpga/
- For curriculum and other discussions, there is the IUP (Imagination University Programme) forum here

Plans :

- A webinar for RVfpga is planned for 8th October 2020, register here: https://hubs.ly/H0v3l-r0
- Our global Workshop Schedule Programme is regularly updated at University Events
- Videos from these workshops will be available online in 2021
- Encouragement will be given to translators who wish to make these materials available in other languages. Please contact IUP@imgtec.com
- Joint activities with RISC-V International (formerly the RISC-V Foundation) and other partners are under discussion

Press Release:

https://www.imgtec.com/news/press-release/imagination-announces-the-first-risc-v-computer-architecture-course/

RISC-V Global Forum Paper by Harris & Chaver-Martinez:

https://events.linuxfoundation.org/riscv-global-forum/register/

Our Partners

We have worked closely with 17 partners and supporters who have given outstanding support to this large and complex project.

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