S/C Packaging Assembly Challenges Using Organic Substrate Technology

Presented by

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ASE Group

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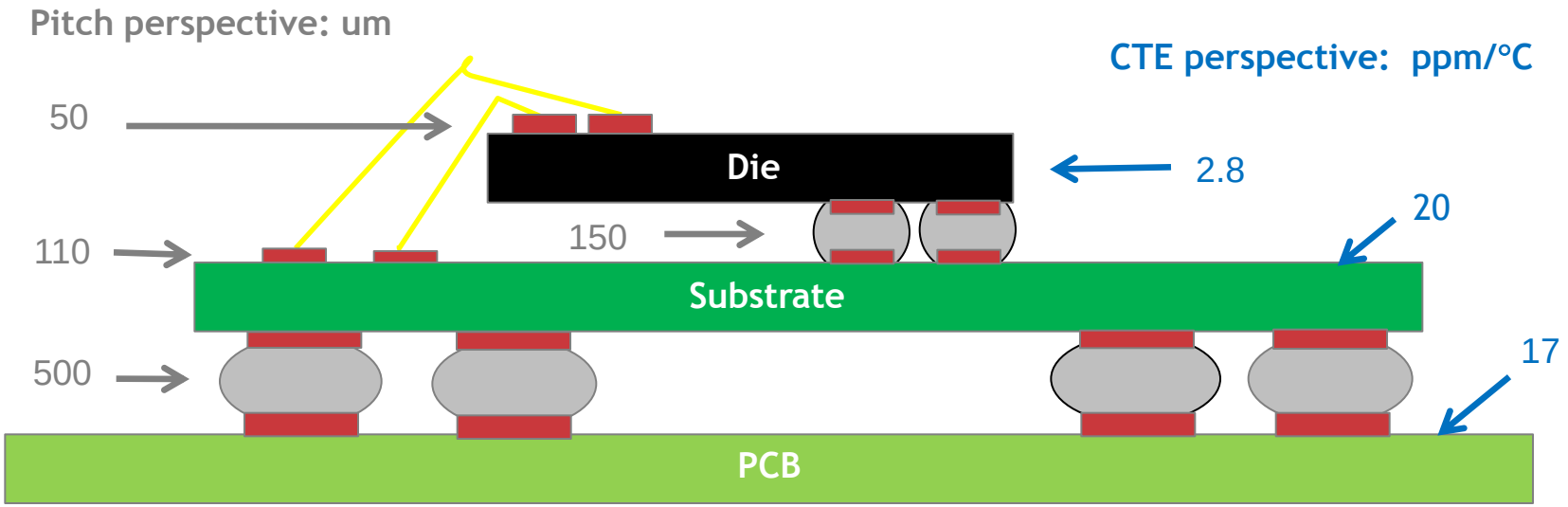
Overview

- The Packaging Challenge
- Chip Substrate Interactions
- **Stiffeners for FC-BGA Packages**
- **PoP Packaging**
- **PBGA & CSP Substrates**

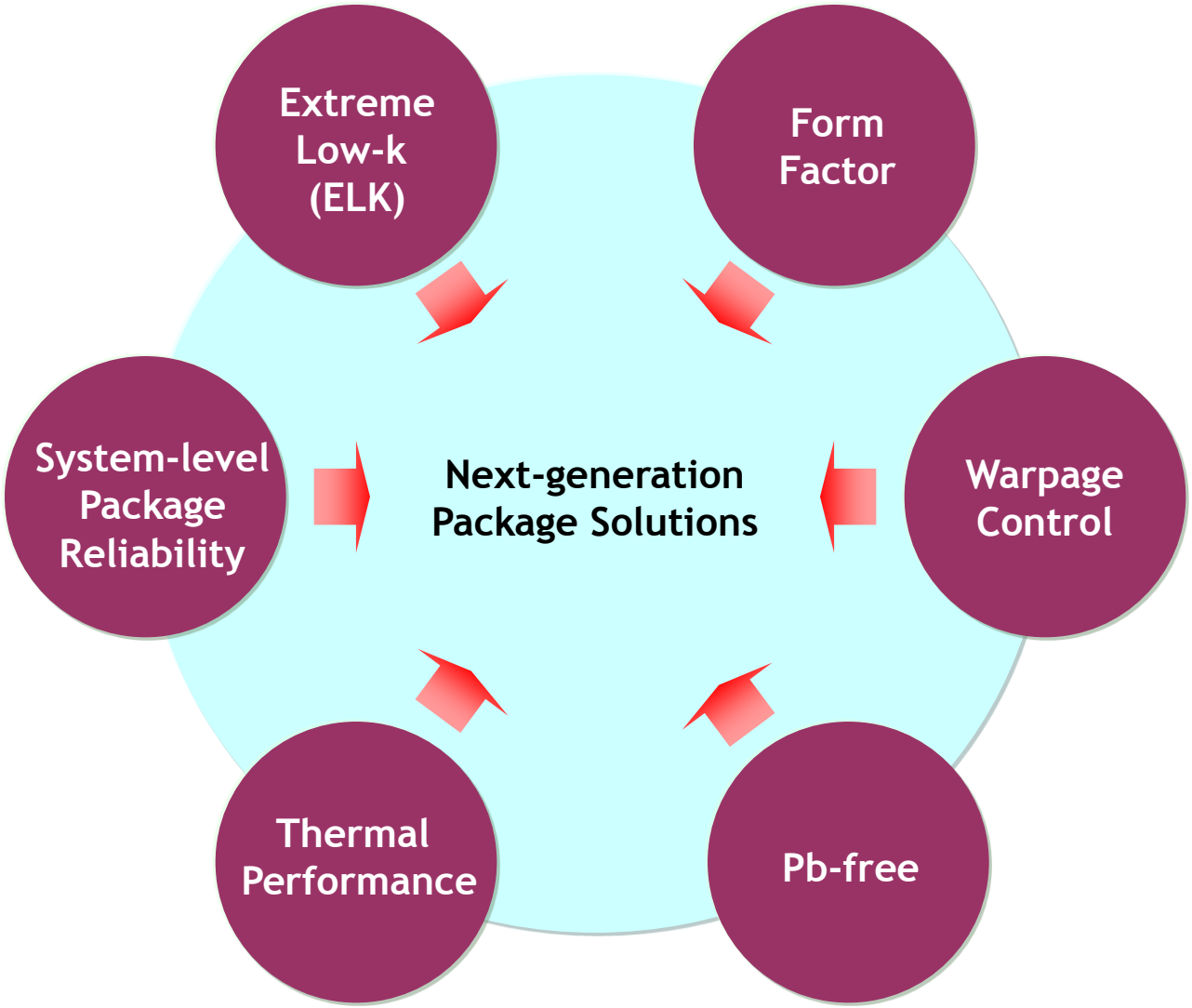
Packaging Challenges



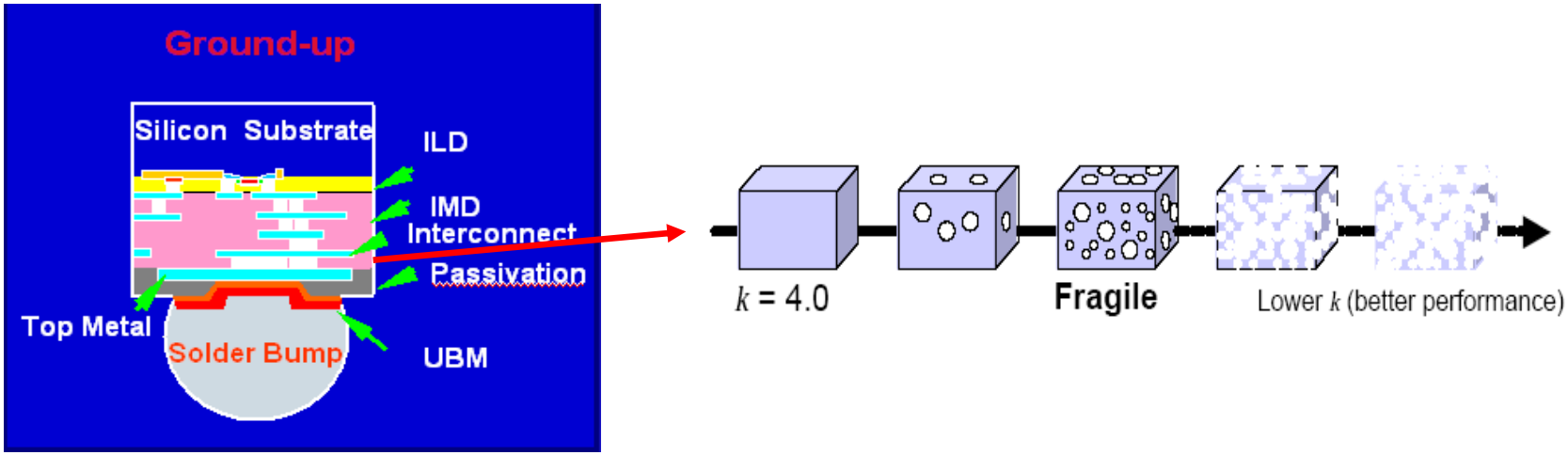
Underfill, Overmold / Lid omitted for simplicity

- CTE mismatch: reliability & warpage concern
- Increasing interconnect density
- Decreasing substrate thickness

Packaging Challenges



Packaging Challenges from ELK



- Assembly challenges from ELK:
  - Die separation process
  - Underfill selection for ELK and bump protection
  - Pb-free bump: Higher stress on ELK layers
  - Fine-pitch bump application

CSI (Chip Substrate Interaction)

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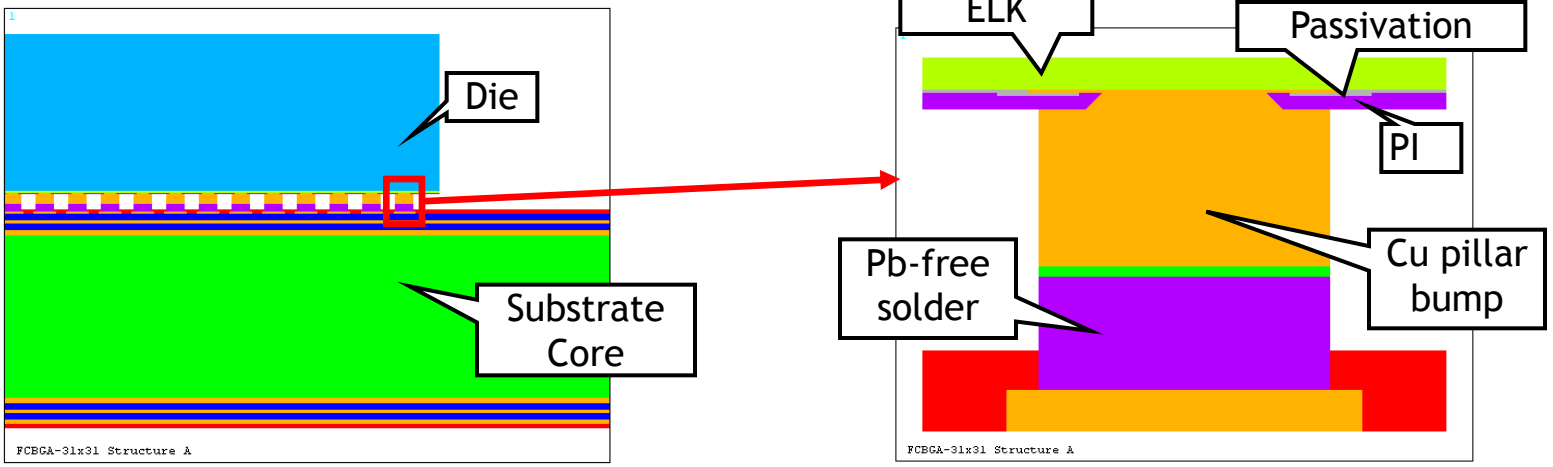
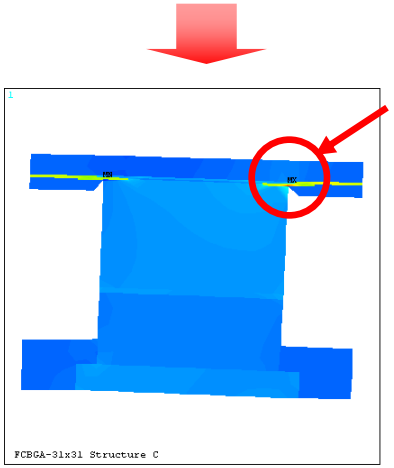
- Structure:
  - SnPb -> Pb-free -> Cu pillar
  - FSG -> LowK -> ELK
  - pitch -> fine pitch -> finer pitch
  - thick -> thin -> thinnest -> coreless

- Cost
  - unit -> strip (FC)
  - std -> MAP -> LMAP -> XLMAP -> XXLMAP
  - mold blocks: 4 -> 3 -> 2 -> 1
  - UF & MC -> MUF

Design Optimization for ELK Devices



Global model **Sub-model**



High stress at ELK

- Design and material optimized for:
  - Polyimide (PI)
  - Under Bump Metallurgy (UBM)
  - Bump & pre-solder
  - Underfill

Copper Pillar Bump Construction

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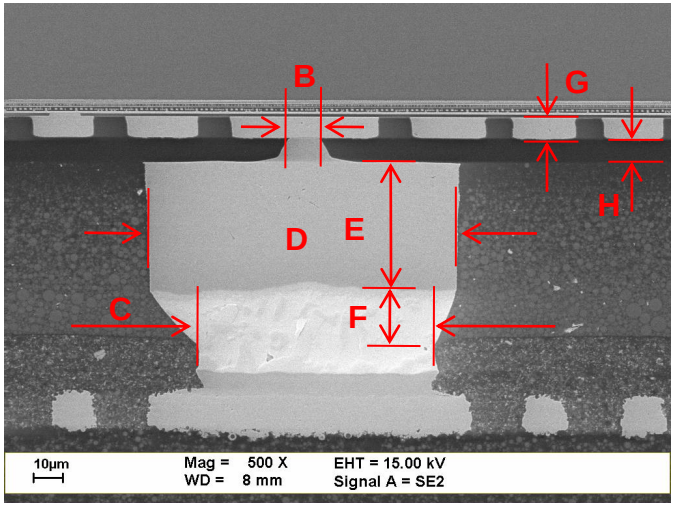
Copper Pillar Bump Design Preference

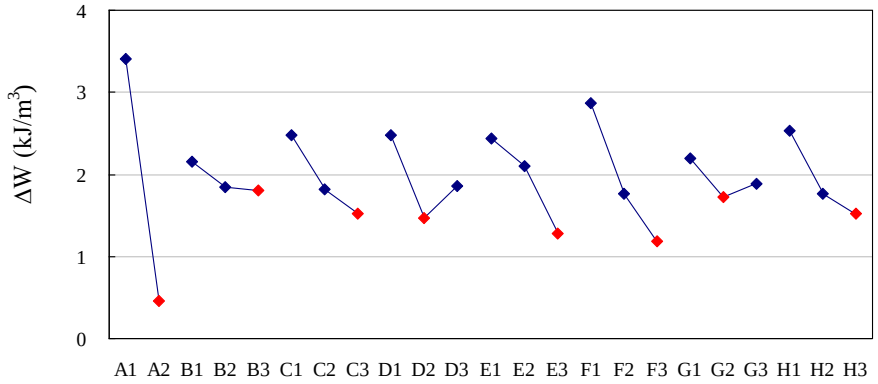
- **Effect on TC reliability: Underfilled > Solder cap thickness > Soldermask opening > Copper pillar thickness**
  - **Thicker solder cap**
  - **Thicker Copper pillar**
  - **Larger soldermask opening**



Intel Atom 45 nm
Cu pillar+SnAg solder cap on ENIG substrates

- DOE Matrix by Taguchi Method $L_{18}(2^1 \times 3^7)$

Factor	Item	Level 1	Level 2	Level 3
A	Underfill filled	without	with	
B	Passivation opening	10	20	30
C	Soldermask opening	60	80	100
D	UBM diameter	60	80	100
E	Cu pillar thickness	30	40	50
F	Solder cap thickness	5	15	25
G	Die pad thickness	1	5	8
H	Polyimide thickness	1	5	8



Quality factor responses

Copper Pillar Bump vs. Solder Bump

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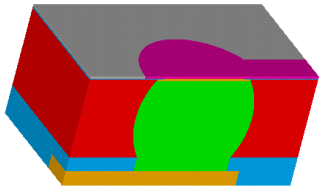
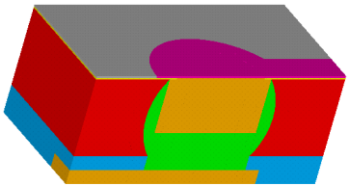
Advantages of Copper Pillar Bump

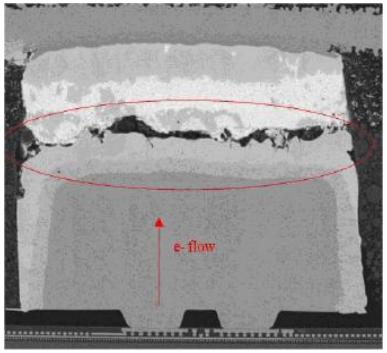
- Good heat dissipation
- Good electromigration reliability
- Fine pitch

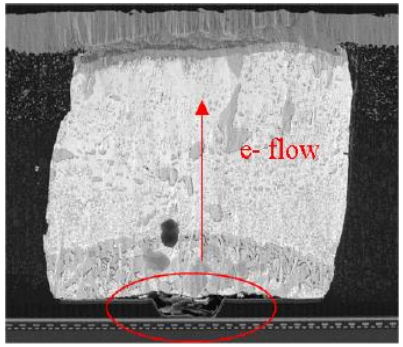


Solder bump

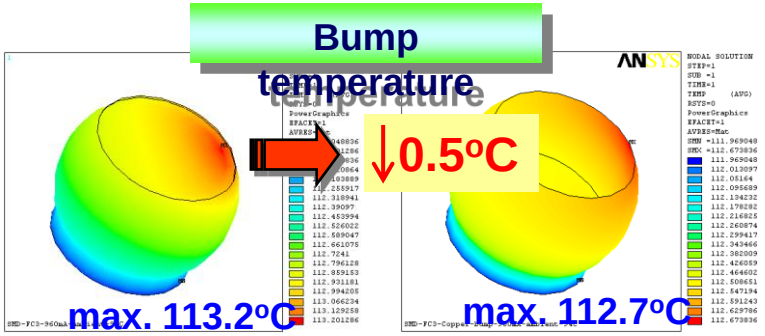


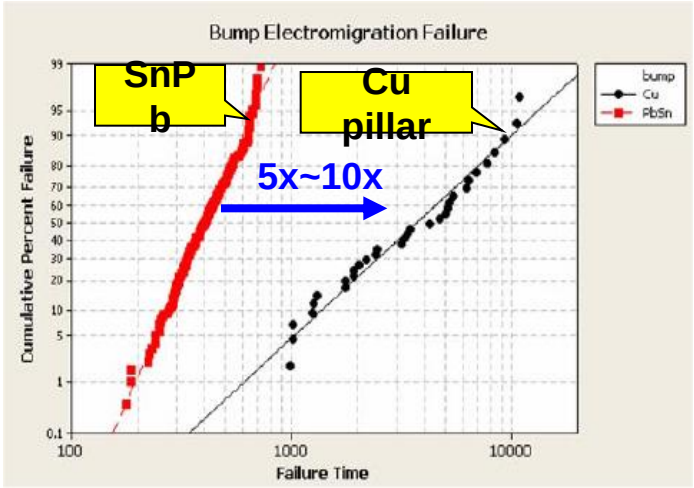
Cu pillar bump





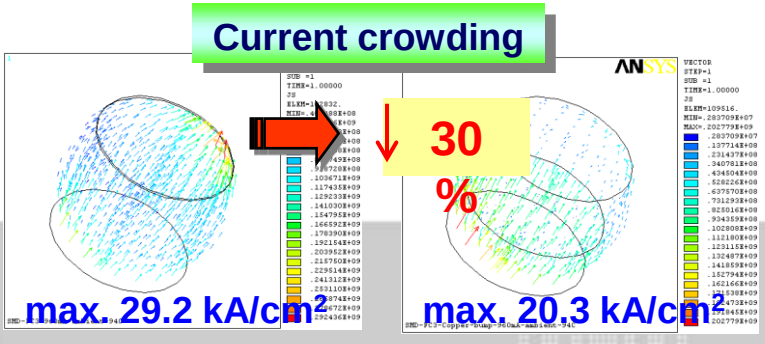
Cu pillar bump (left) and SnPb (right)





Cumulative EM failure probability chart

2006 ECTC, pp. 1611-1615 (Intel, 65 nm)



Modeling for Robust N40/N32 ELK Flip Chip

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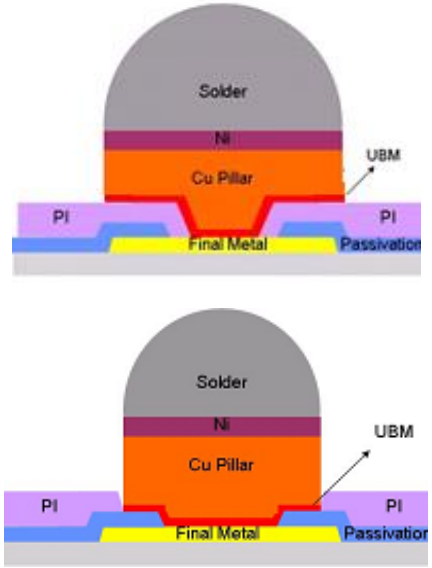
- White bumps (ELK delam beneath UBM) observed upon flip chip bond
- Strategy against white bumps:
  - ➢ Thin die – but leads to great warpage
  - ➢ PI implementation – stress buffer
  - ➢ Thin UBM – less stiff
  - ➢ SnPb is better than Pb-free
  - ➢ No significant improvement with low-CTE substrate

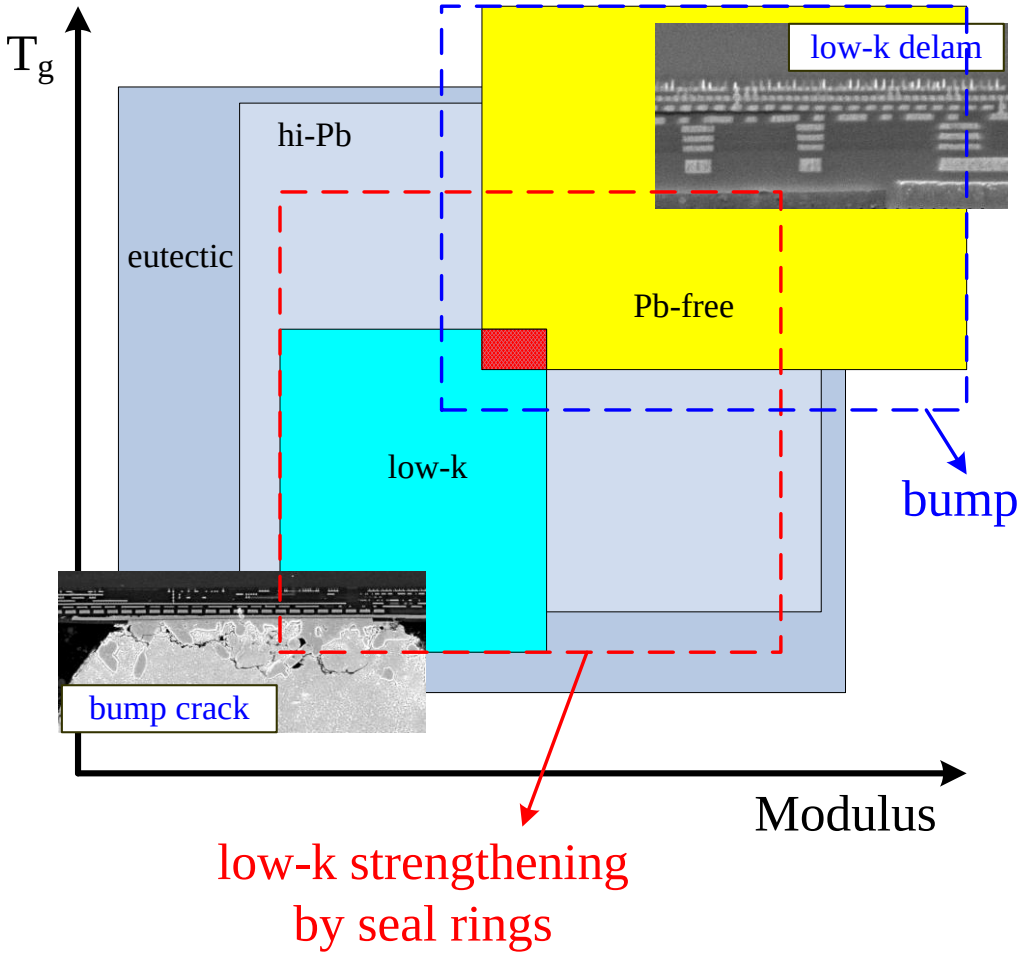


Smaller contact is better

Larger contact is better

Different trends for different bump structures

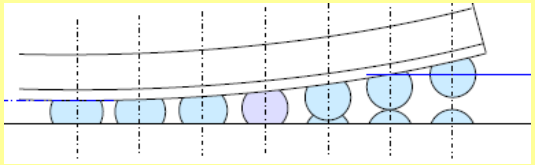
Underfill Selection for Low-k Flip Chip



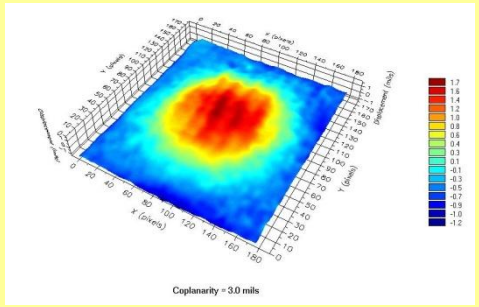
Underfill Selection Rules

- High Tg/High E: Good for bumps
- Low Tg/low E: Good for low-K
- Window is small for Pb-free
- Window can be expanded:
  - Seal rings in chip
  - Bump composition change

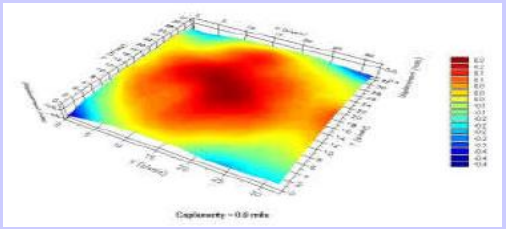
Warpage Control Challenges



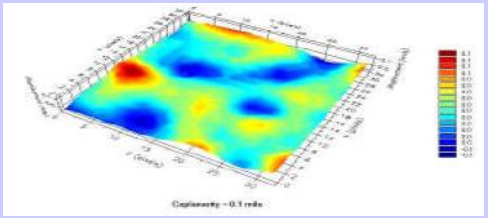
Critical warpage for SMT



Substrate warpage verification (@260 °C)



(@25 °C)

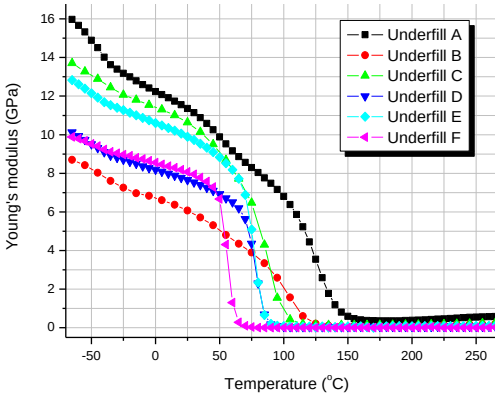


(@125 °C)

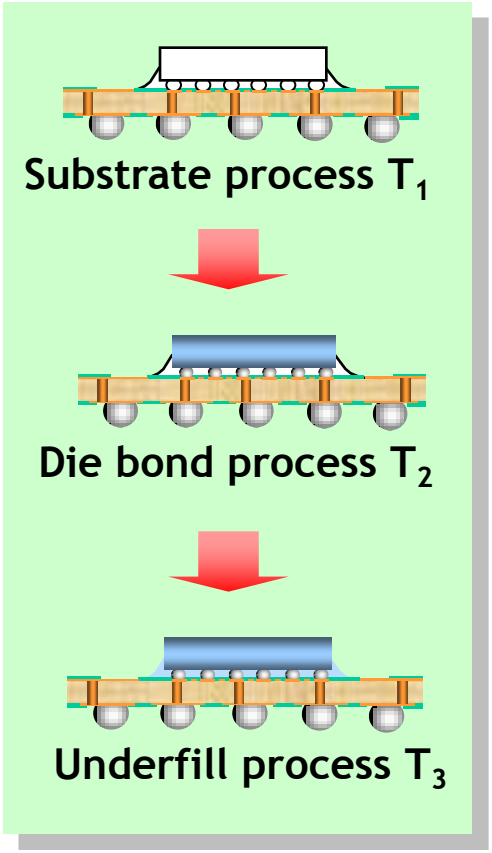
Die warpage variation

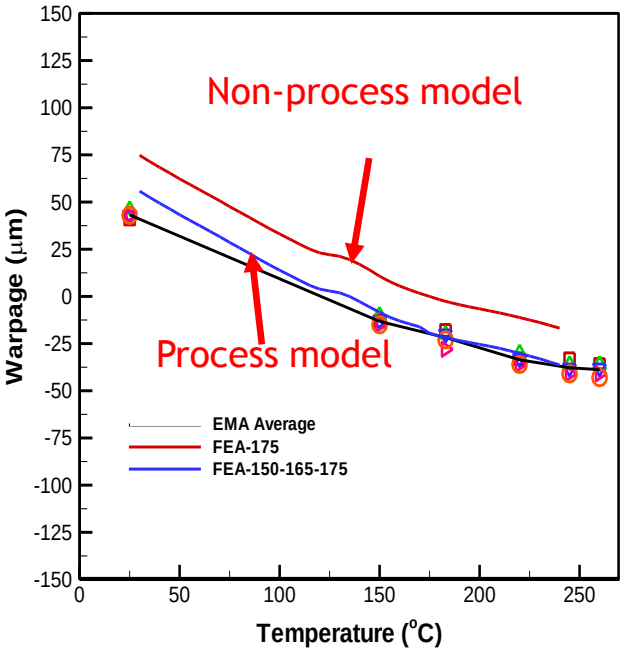
- Fine ball pitch makes the warpage control more challenging
- Die warpage variation impacts the performance of TIM above die

Warpage Modeling



Temp-dependent material properties





- Advanced FEA modeling incorporating various process temperatures has been utilized for warpage optimization

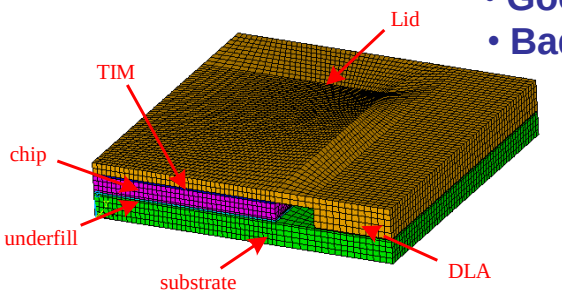
Stiffeners for FC-BGA Packages

- External
  - After die attach
    - Single piece
    - Two piece
  - Before die attach
    - Custom
    - Open tool
- Internal
  - Cu / Invar / Cu
  - Stainless

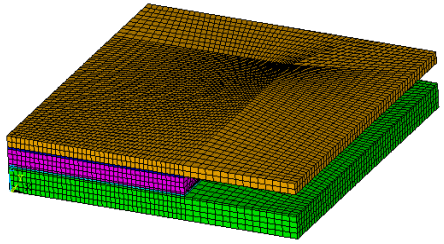
Lid and Stiffener Ring Effect for Flip Chip

- Lid with wider ring leads to smaller warpage
- No direct-lid-attach (DLA) is preferred for solder bump TC reliability
- For different package sizes, trends of the maximum warpage and stress are similar

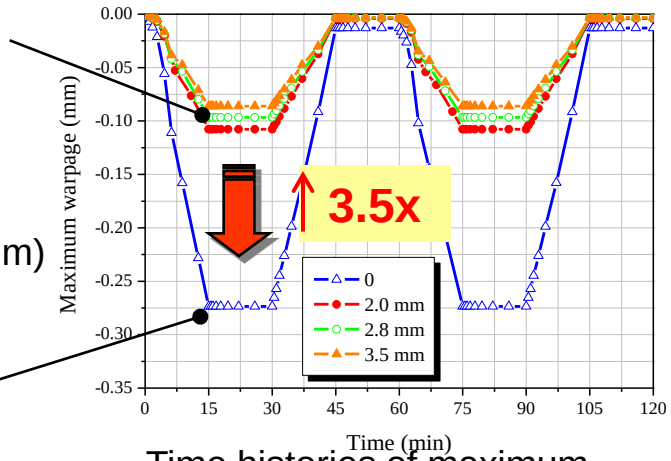
• **Good Warpage**
• **Bad Reliability**



HFCBGA 27x27 mm^2 (DLA-3.5mm)



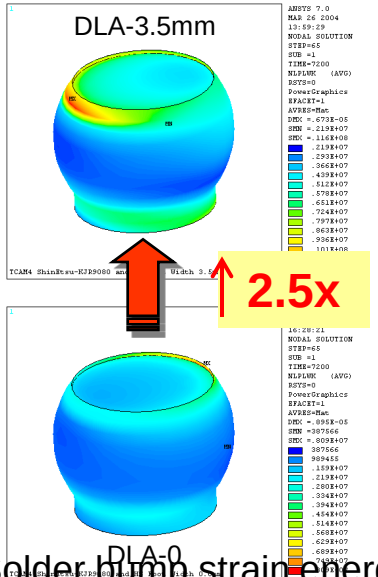
HFCBGA 27x27 mm^2 (DLA-0)



Time histories of maximum warpage

• **Bad Warpage**
• **Good Reliability**

Strain energy density of solder bump



Solder bump strain energy density

PoP Packaging

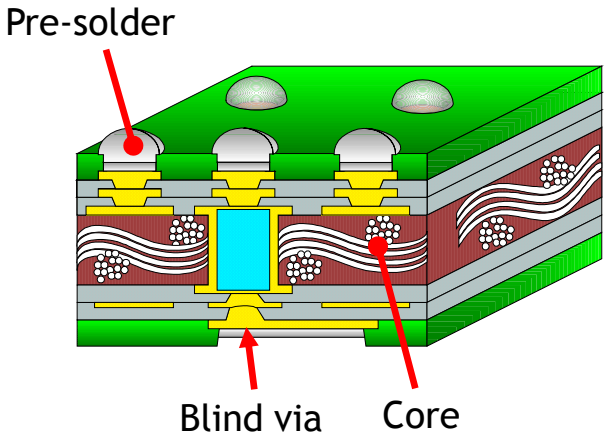
- co-planarity
  - substrate thickness: thick -> thin
  - die thickness: thick -> thin
  - CTE core: std -> low
  - area ratio substrate / die
  - MC modulus

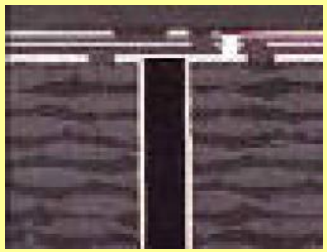
- stacked package height

- cost

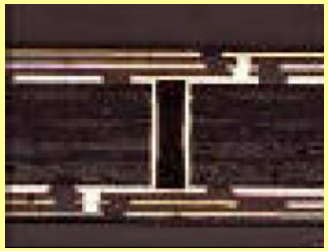
Substrate Development Trends

- Low-CTE substrate core
  - CTE: 12 ppm/°C → < 10 ppm/°C
- High interconnect density
  - Bump pitch: 150 μm → 130 μm
    (alternative solutions for pre-solder?)
  - Stacked via: 3 stacked → 4 stacked
- Thin substrate
  - Core thickness: 400 um → 200 um → 100 um → Coreless



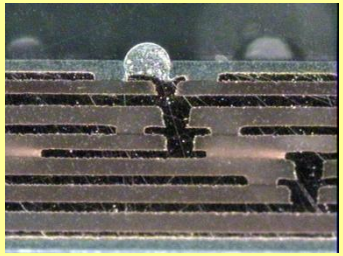


800-μm core



400-μm core

...



Coreless

BGA Warpage Reduction Guideline

- Warpage due to CTE mismatch

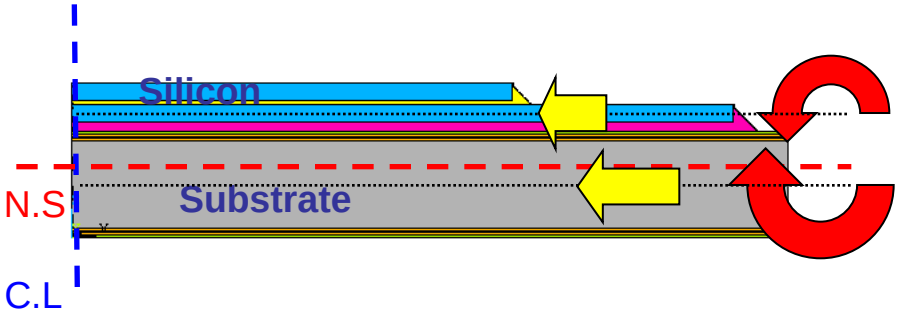
Cooling to room temp. ⇒ Convex shape

Moment

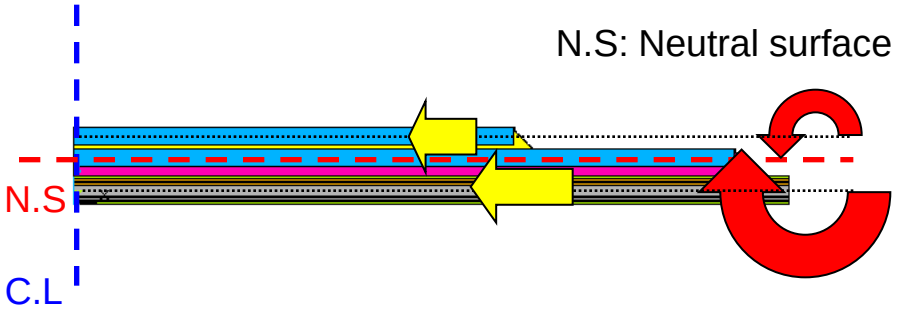
Shrinkage

C.L: Centerline

N.S: Neutral surface



Thick substrate → small warpage



Thin substrate → big warpage

Determine the position of neutral surface → **Shrinkage from each component** → **Force/Moment balance to determine warpage**

Dependent on package modulus and thickness

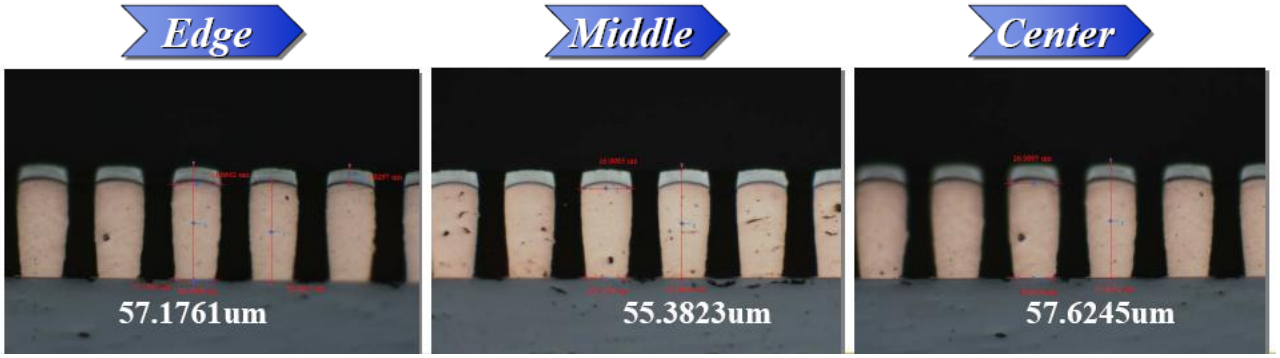
Dependent on package CTE

→ **Substrate with Low CTE, High Modulus and Great Thickness are preferred to reduce package warpage**

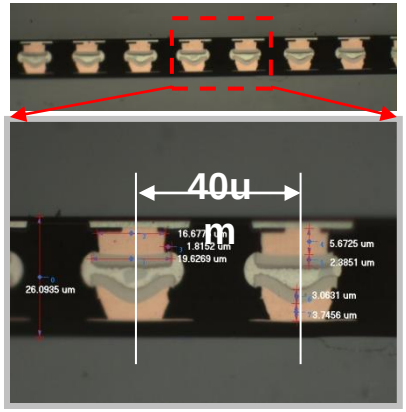
3D- packaging

- **micro-bump assembly for TSV**

- TSV Middle-End
  - ❑ High AR Microbump 1st article prototype of 20um size/ 56um height



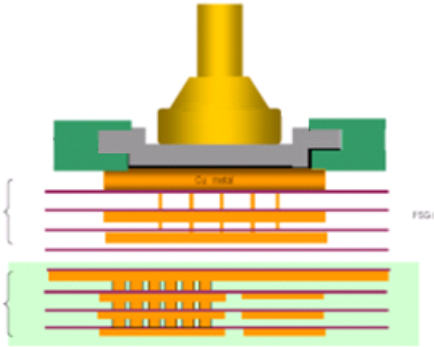
- ❑Joined fine pitch micro bumps

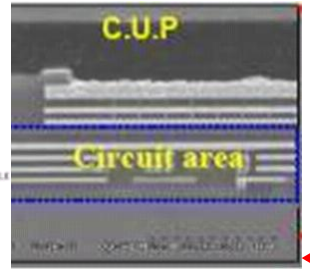


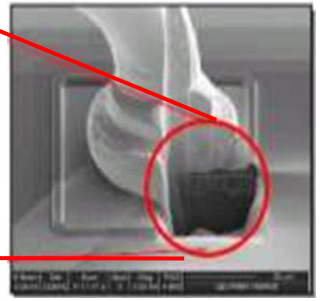
Wire Bond Challenges for lowK

- Cu wire
  - higher force
  - CUP
  - fine pitch: 1 mil -> 0.8 mil -> 0.7 mil

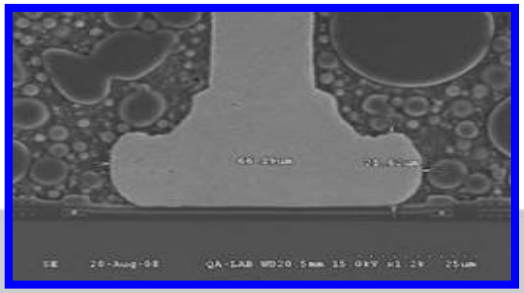
CUP Design & LowK Wafer



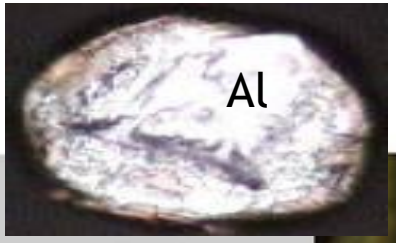


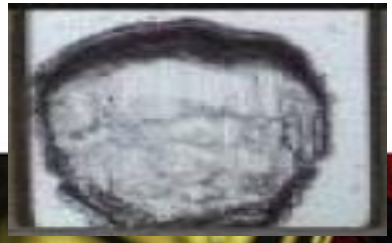


- High energy transformation capillary.
- Parameter optimization.
- Ball shape control.
- Ball shear inspection.



After ball shear test





PBGA & CSP Packaging

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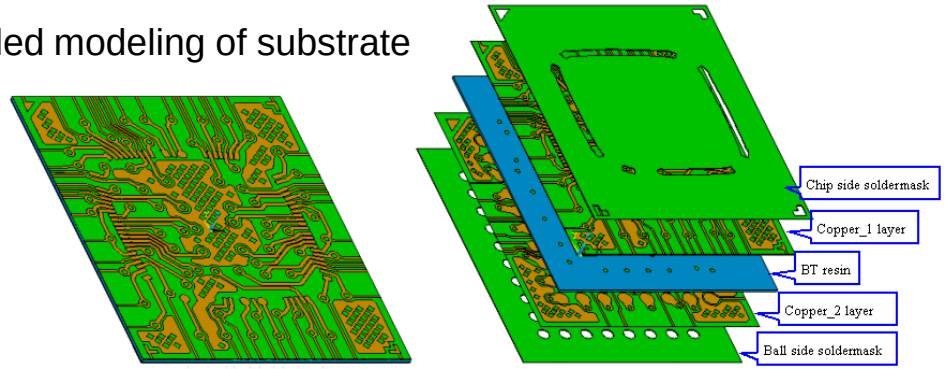
- Structure:
  - 2L thin: 130μ -> 110μ -> 100μ -> 90μ
  - L/S pitch: 50/50 -> 40/40 -> 30/30 -> 20/20

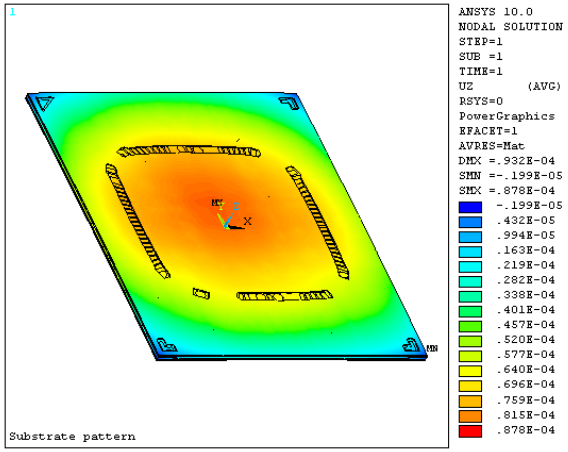
- Cost, cost, cost, …
  - strip size: std -> MAP -> LMAP - XLMAP
  - 2L -> 1L
  - 4L -> 2L
  - NiAu -> ENEPIG

Warpage of Bare Laminate Substrate

- Thicker BT - Reduces substrate warpage
- Thinner BT - Soldermask thickness has significant impact on substrate warpage

Detailed modeling of substrate

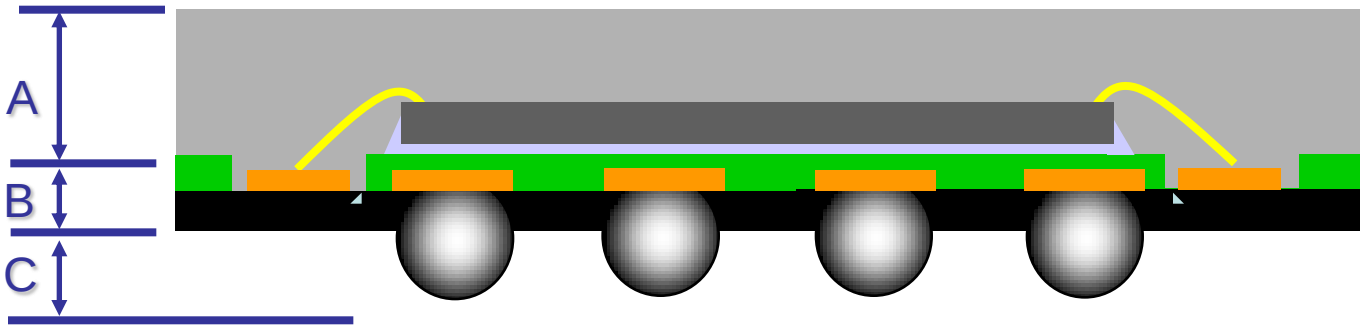




Warpage contours

Maximum warpage for different BT/Soldermask thickness

a-S³ Package outline & X-section



Package Outline				
Total Thickness	Mold Cap Thickness(A)	Substrate Thickness(B)	Ball Size BPO	Stand Off(C)
0.5 mm Max.	0.25 mm	0.085mm	0.25mm / 0.3 mm	0.14mm Max.
0.6 mm Max.	0.3 mm	0.095mm	0.25mm / 0.25 mm	0.17mm Max.
0.8 mm Max.	0.45 mm	0.095mm	0.3mm / 0.275 mm	0.23mm Max.
1 mm Max.	0.54 mm	0.095mm	0.35mm / 0.3mm	0.29mm Max.

Feasibility study cases—3 (for Middle lead count QFN)

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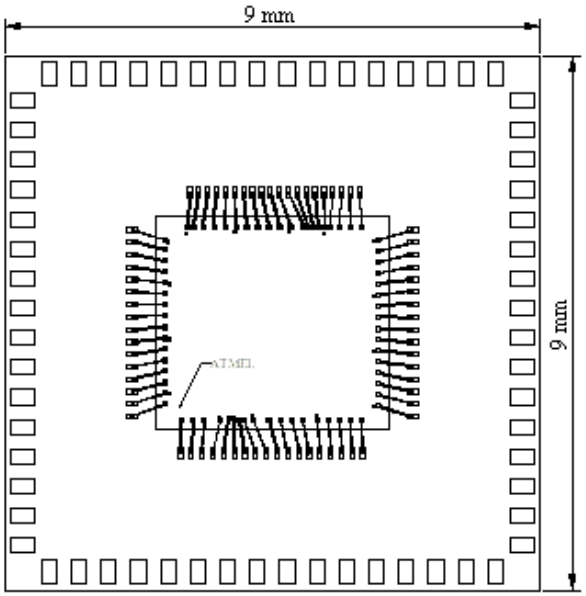
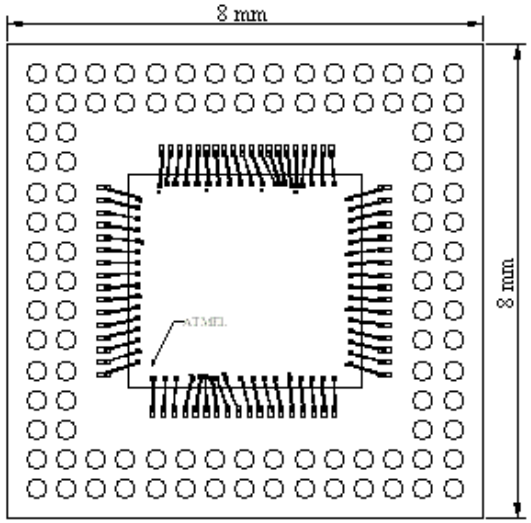
- Save the package size
- Save the wire
- Enhance the BLR performance
- Allow more lead count

Package type	Package size	Ball/ Lead count	Ball pitch	Max. wire length	3D total wire length
QFN	9x9mm	64	0.5mm	3500um	213 mm
LGA (S3)	9x9mm	64	0.5mm	323um	47 mm
BGA (S3)	8x8mm	105	0.5mm	323um	47 mm
BGA (S3)	6x6mm	64	0.65mm	1183um	88 mm

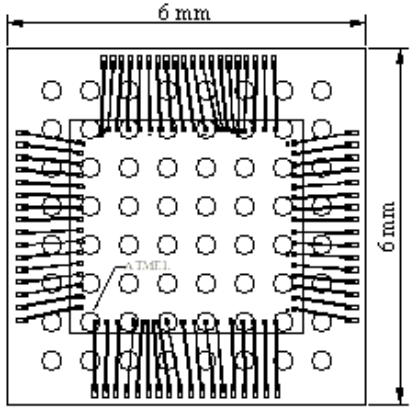
a-S^3 option-1



a-S^3 option-2



a-S^3 option-3



Summary

- Meeting the challenges from ELK and Pb-free bumps, chip-package-system co-design is essential
- As the interconnect pitch decreasing, warpage control is getting critical
- Advanced modeling is the one of the keys for warpage control
- Materials properties need to be planned & developed methodically

Thank You

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