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SET2DIL: Method to Derive Differential Insertion Loss from Single-Ended TDR/TDT Measurements

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ABSTRACT

This paper presents a novel method to derive Differential Insertion Loss (SDD21) using only single-ended TDR/TDT (or 2-port VNA) measurements at a single probe location. Extensive simulation and measurement data are provided to demonstrate its accuracy.

The method, in conjunction with a proposed hand-held probe would, for some applications, replace current 4-port measurements of 2 probe locations which are appropriate for a laboratory environment only. The SET2DIL method would allow much easier measurement of SDD21, making it acceptable for a broader variety of users including High Volume Manufacturing (HVM).

AUTHORS BIOGRAPHIES

Jeff Loyer is currently a Signal Integrity Lead for Intel's Enterprise Server Division, responsible for ensuring proper signal integrity of all busses on future 2 & 4-socket server designs. He has presented at DesignCon on the "Fiberweave Effect", and authored articles on signal integrity for both EDN and Printed Circuit Design & Manufacture magazines. He holds a Bachelor of Science degree in electrical-engineering technology from Arizona State University (Tempe), and has taught signal-integrity classes both inside and outside Intel.

Richard Kunze is currently a senior staff engineer in the Enterprise Platform Technology Division (EPTD) organization within the Digital Enterprise Group (DEG), Intel Corporation, DuPont, Washington. His past experience in Intel includes leading the working group responsible for signal integrity of the PCIE bus interface in Intel Server systems, research and development of passive EM structures for high speed interconnects, and advancing the development of package power delivery modeling methodology and its application to package designs for Enterprise CPU's and chipsets. Richard Kunze received his B.S. degree in physics from the University of Rochester, Rochester, NY, in 1973 and Ph.D. in physics from SUNYAB, Buffalo, NY in 1980.

OVERVIEW

This paper is intended to lead the reader through an introduction to the need for the method, some background into current insertion loss techniques using 4-port VNA, a derivation of the SET2DIL algorithm, and demonstrations of its accuracy.

The derivation starts with illustrations of how TDR/TDT can be used instead of VNA, and how only 2 of the 4 ports' waveforms are necessary to derive SDD21 from a symmetric system. Once that is established, we show how, for symmetric differential pairs, the needed information can be gleaned at a single probing location, using 2 ports. This is the concept behind SET2DIL. We then demonstrate the algorithm on actual measured waveforms and show the results – a credible SDD21 graph.

After that, we demonstrate some of the nuances of SET2DIL and the waveforms using Agilent's ADS simulator. We also show correlation between SET2DIL and VNA measurements through a large variety of trace topologies (impedance, loss) using Hspice simulations.

Finally, we give a comprehensive overview of the results of test boards that were designed, built, and measured to check the correlation between SET2DIL and VNA up to 20 GHz.

INTRODUCTION

Signal attenuation and distortion from dielectric and conductor losses is a major factor in proper high-speed differential bus simulation and design. Measuring differential insertion loss (SDD21) historically requires a 4 port VNA or TDT measurement, typically with 2 ports measured at one location, while the other 2 ports are measured at another location. Simultaneously probing these 4 ports is prohibitively challenging for High-Volume Manufacturing (HVM), whose procedures for impedance testing are limited to probing a single location only. Several techniques for solving this problem are proposed in IPC TM-650 2.5.5.12; this paper proposes another possibility.

The paper outlines a novel method for measuring SDD21 using only a 2-port measurement. It takes advantage of the fact that:

1) For symmetric differential traces, SDD21 = S21-S41 [i]
2) These parameters can be extracted from the corresponding single-ended TDR/TDT waveforms, T21 and T41
3) A differential pair can be looped back at its far end to allow far-end measurements to be probed at a single probe location
4) From measurements of this structure, waveform manipulation in the time domain allows converting the results to T21 and T41
5) The corresponding frequency-domain result, SDD21, is then readily calculated

Note: 2-port VNA measurements can be used instead of TDR/TDT, but those results will have to be converted into time-domain waveforms for waveform manipulation.

The method also has the advantages that its test structure:

- is ½ the length of a standard insertion loss test structure, and
- can also be used as an impedance test coupon.

DIFFERENTIAL INSERTION LOSS MEASUREMENT BACKGROUND

Insertion loss (S21) is a dominant factor in signal integrity of multi-GHz busses, and needs to be modeled correctly for simulations to represent actual performance. It must also be validated on actual designs to ensure simulation assumptions were met.

For single-ended traces, typically the measurement requires exciting a trace (Device Under Test, or DUT), to be characterized at one end (p1), and measuring the resultant waveform at the other end (p2), as shown in Figure 1a. For proper fidelity, the trace is typically ≥8" long (compared to 6" for typical impedance coupons), and the measurement entails probing both ends of the trace simultaneously. The two ends of the trace are usually physically separated, making the measurement more difficult. For single-ended traces, however, this problem can easily be overcome by using a somewhat circular structure with adjacent probing locations for both ports, as shown in Figure 1b.

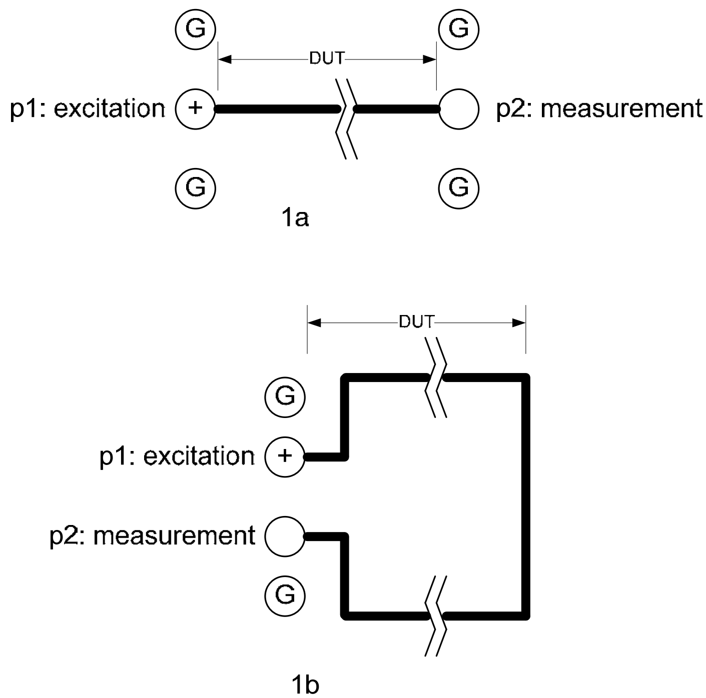


Figure 1: Singled-Ended Insertion Loss Traces

The vast majority of our multi-GHz busses are differential, however, and the measurement of SDD21 requires probing the differential pair at both ends. SDD21 is derived from four single-ended measurements as SDD21=0.5*(S21-S23-S41+S43)[i], see Figure 2. This requires simultaneously contacting four signals and their associated grounds, a standard task in the laboratory environment, but a more difficult task in the HVM setting, see Figure 3 and Figure 4. HVM tools for impedance testing currently are only probing at a single location for TDR of differential traces; requiring probing of two locations would require extensive modification to their equipment and procedure.

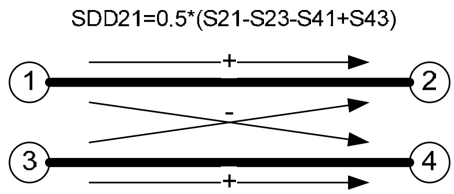


Figure 2: SDD21 Parameters

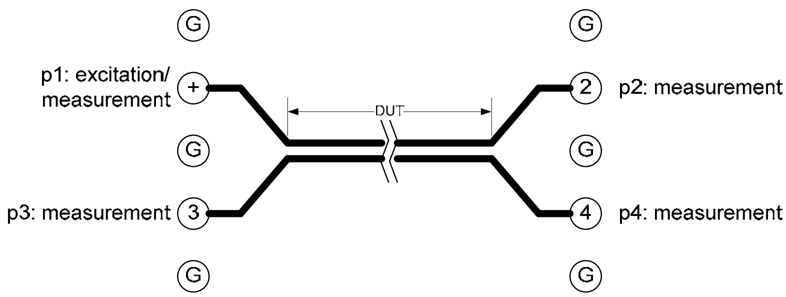


Figure 3: Differential Insertion Loss Traces

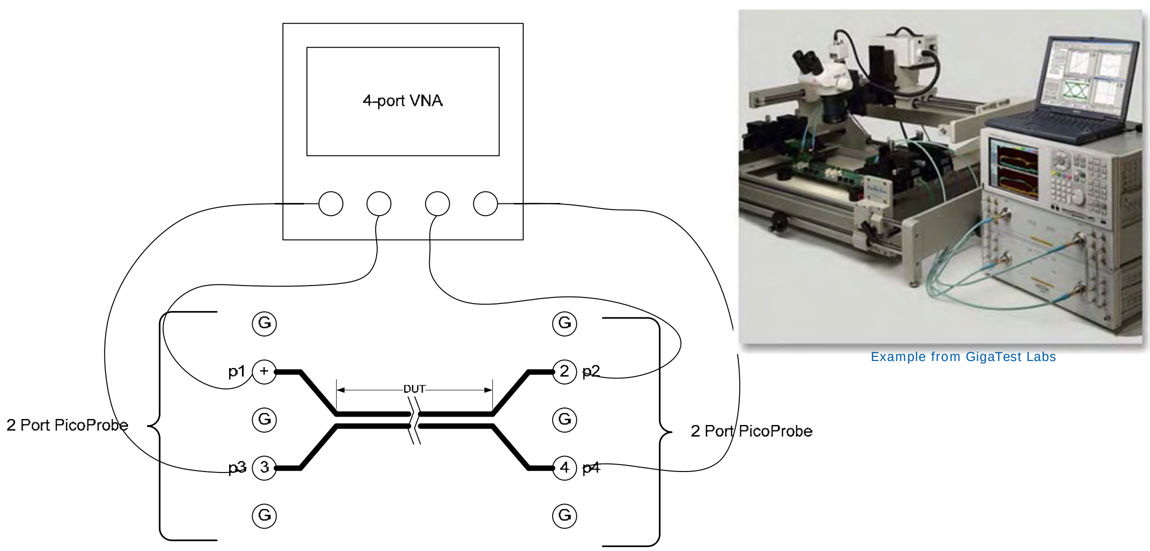


Figure 4: Current SDD21 Measurement Setup

Differential Insertion Loss Measurement Simplified - from TDR/TDT

There are aspects of our particular DUT, a line-to-line symmetric differential pair, that make our task easier – we don't have to measure every port to determine all the components of the equation SDD21=0.5*(S21-S23-S41+S43). For ideal symmetric traces, S21 ~ S43 and S41 ~ S23. The equation then simplifies to SDD21 = S21 – S41; we only have to excite port 1 while measuring ports 2 and 4 to extract SDD21. In actual manufacturing, the traces won't be perfectly symmetrical: graphing S21 - S41 shows slight differences from S43 - S23, and both are not equal to the actual SDD21.

In the time-domain, S21 is equivalent to TDT (or T21), and S41 is equivalent to far end crosstalk (FEXT, or T41), of a single-ended trace with a coupled victim trace.

These measurements can be done with either a VNA or TDR/TDT, since the losses are within the capabilities of TDR equipment (>-40dB). Software to convert from the time-domain TDR/TDT waveforms to the frequency domain is readily available from multiple sources, or can be accomplished in Matlab or similar software.

A simplified measurement structure/method might be as follows (Figure 5):

1) Terminate port 3 of the DUT to 50 ohms, and excite port 1 single-endedly while capturing the waveforms of ports 2 (T21, green waveform in Figure 8) & 4 (T41, blue waveform in Figure 8).
2) Characterize the reference T21 pulse (without the DUT) using a “thru” structure (Figure 6, red waveform in Figure 8).
3) Subtract T41 from T21 (brown waveform in Figure 9), convert the result into the frequency domain and compare that to the frequency domain representation of the “thru” measurement to derive SDD21 (Figure 10).

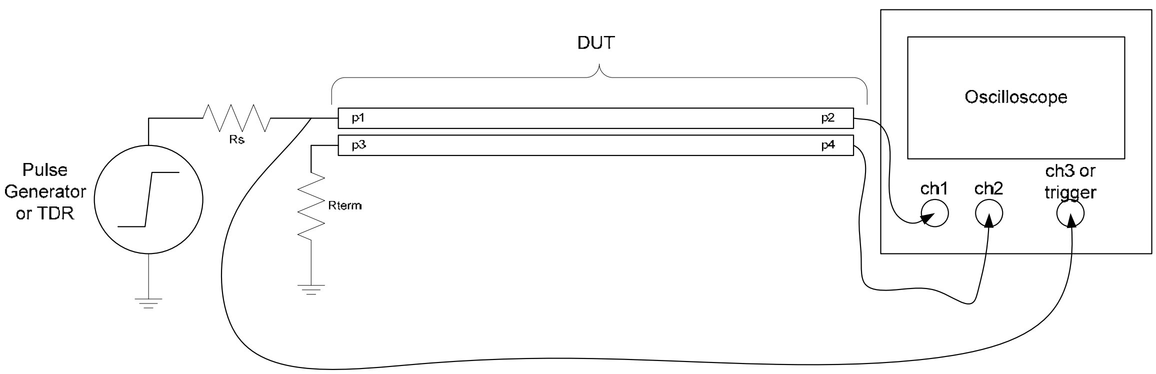


Figure 5: Simplified Method to Measure SDD21 using Time Domain

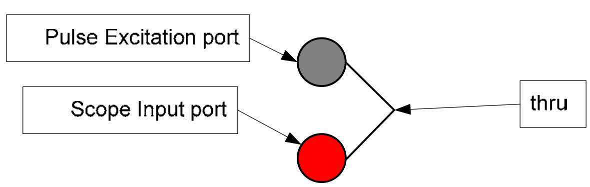


Figure 6: “thru” structure

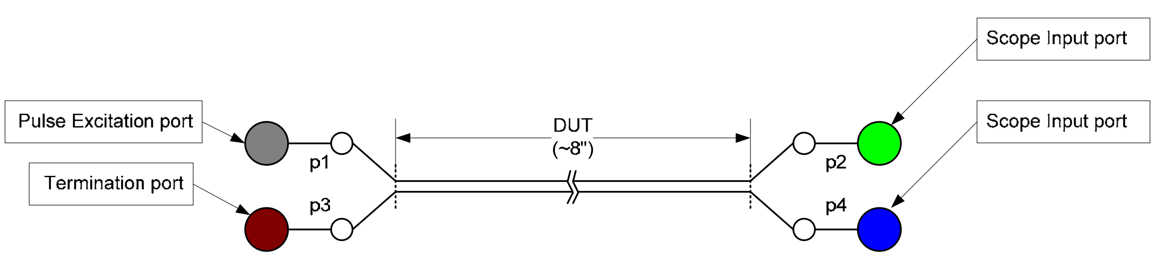


Figure 7: Measurement structure

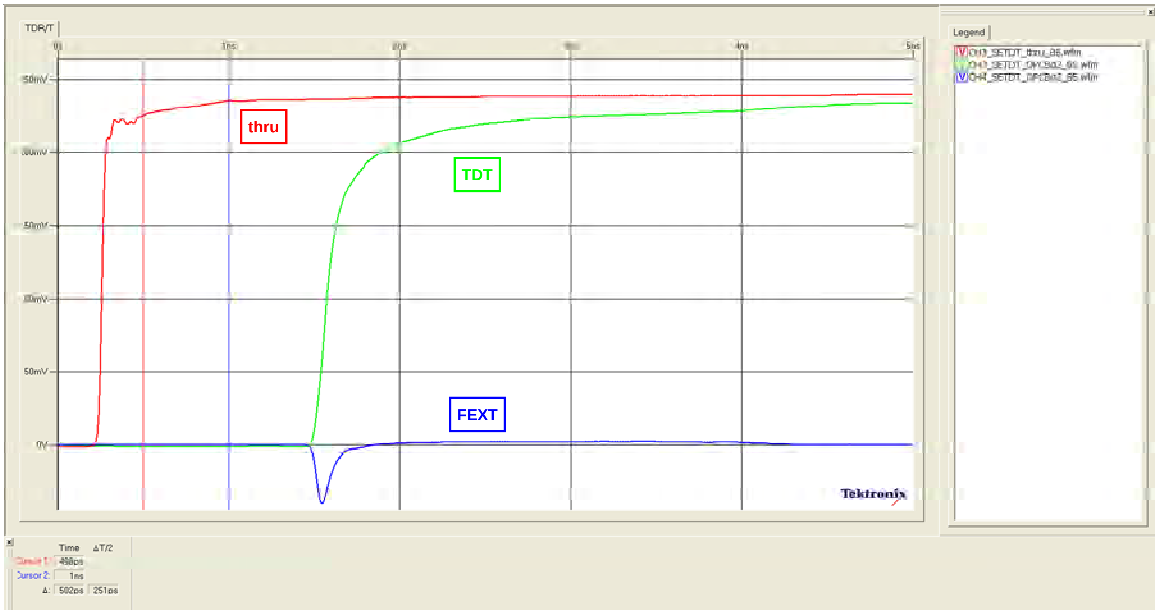


Figure 8: Measured Waveforms

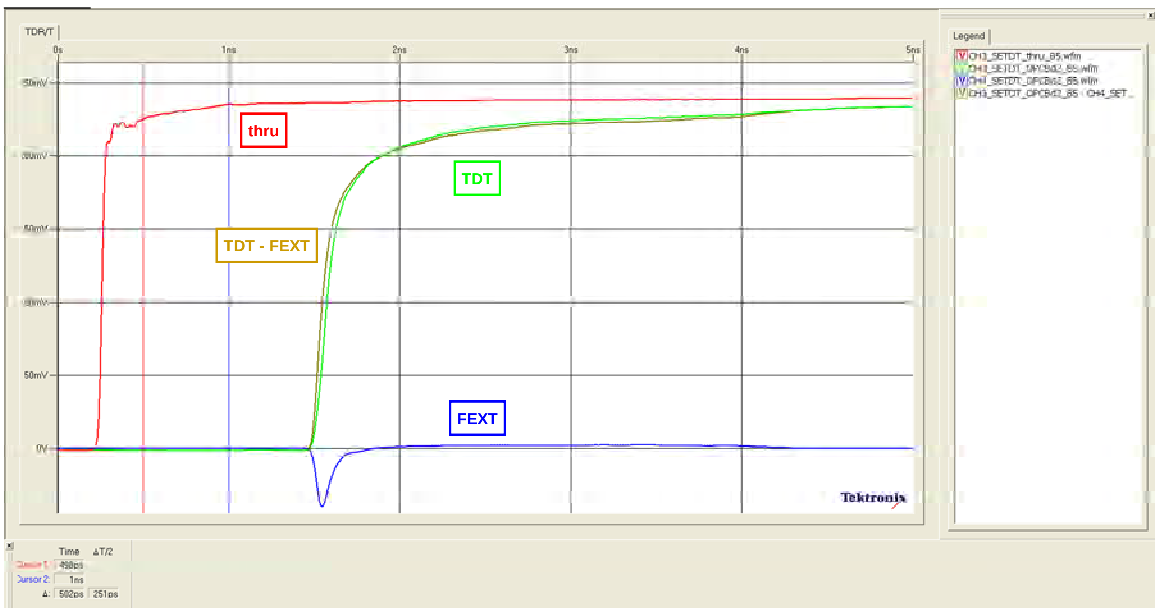


Figure 9: Manipulated Waveform

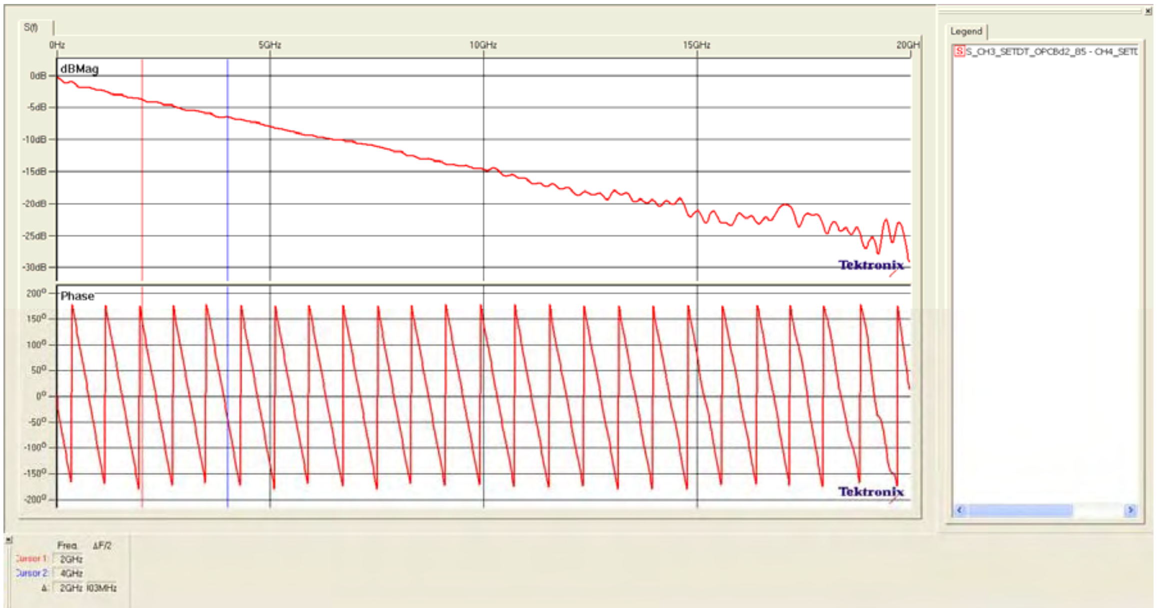


Figure 10: Resultant SDD21

The technique is, however, reliant on symmetry between the two halves of the differential pair, which will not be exact in a non-simulation environment. Figure 11 shows the difference between SDD21 derived from the entire formula (black) vs. S21-S41 (blue) and S43-S23 (Red) on a representative microstrip pair (from our test boards). There are discrepancies, but they are slight and not a significant source of error, up to 20GHz.

With this method, 4-port VNA measurements have been replaced by simpler single-ended TDR/TDT measurements. Another refinement can simplify the SDD21 measurement further, as explained in the next section.

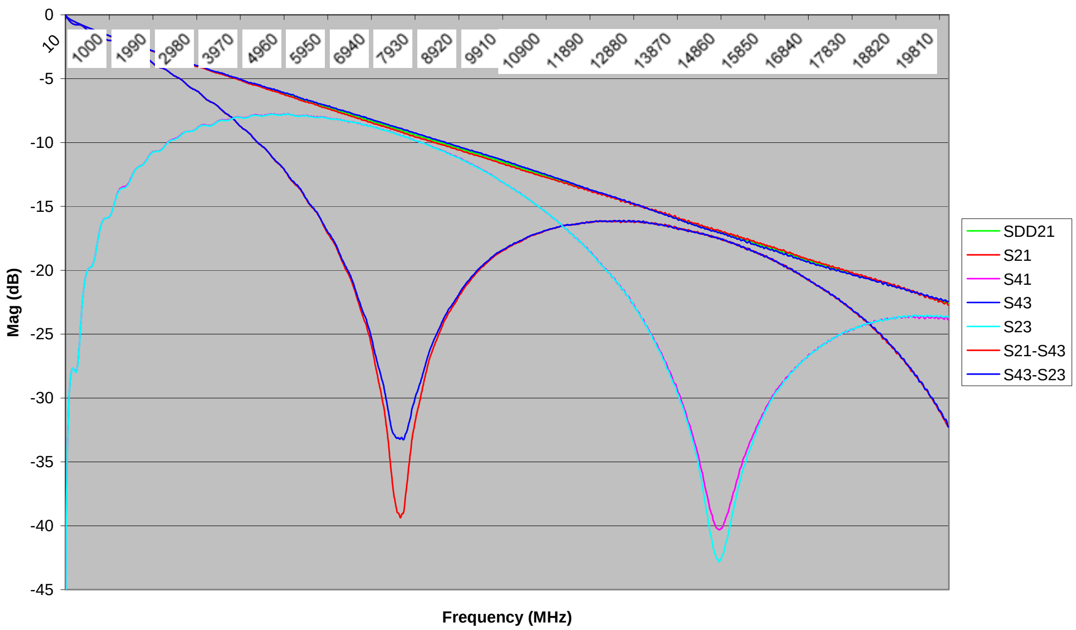


Figure 11: Difference between SDD21 and result from S21–S41, S43-S23

SINGLE-ENDED TDR/TDT TO DIFFERENTIAL INSERTION LOSS (SET2DIL) I.E. SDD21 FROM SINGLE-ENDED TDR/TDT MEASUREMENTS AT A SINGLE LOCATION

If we now cut the DUT in half and loop back the far end (Figure 12), we can make all the measurements we need from a single location, but we will need to manipulate the resultant waveforms to extract the equivalent 4-port T21 and T41.

Referring to Figure 13, the 2 waveforms we are interested in (T21, or "TDT" and T41, or "FEXT") will be superimposed on other waveforms that we aren't interested in (T11, or "TDR" and T31, or "NEXT"). Note that the TDR pulse at q1 induces NEXT and FEXT on the adjacent trace. The NEXT is seen immediately at q2, reaches a maximum amplitude, and then remains at a constant level. The FEXT continues to grow as it follows the TDR trace down towards the end.

Because the signals are looped back, the length of the 4" differential structure is effectively doubled to 8".

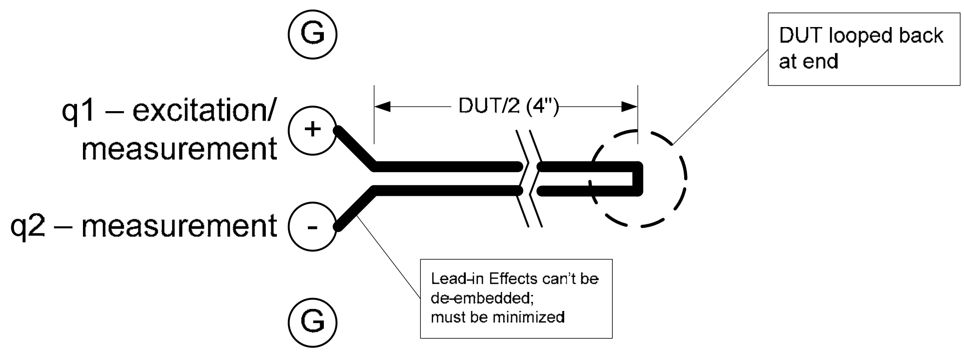


Figure 12: SET2DIL Test Structure

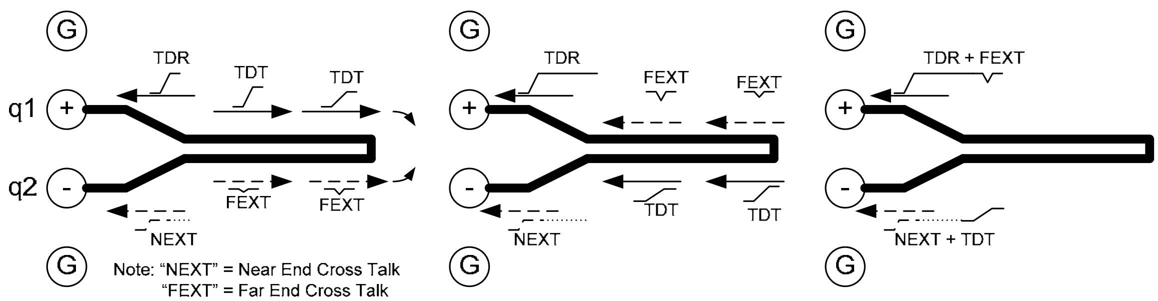


Figure 13: SET2DIL Waveforms (simplified)

To perform SET2DIL measurements we TDR/TDT the test structure and a "thru" reference structure (see Figure 14), and capture:

1) q1: red waveform, TDR of our test structure, but which also includes FEXT after Td (t1, time delay of DUT plus thru) and effects of multiple reflections after 2*Td, t2.
2) q2: green waveform, TDT, or T21, of our test structure, which also includes NEXT until t1 and effects of multiple reflections after t2.
3) "thru": blue waveform, identical to what we did for our "simplified" structure, Figure 6.

NOTE: A “q” is used for the SET2DIL ports instead of “p” throughout this paper to distinguish them from VNA ports.

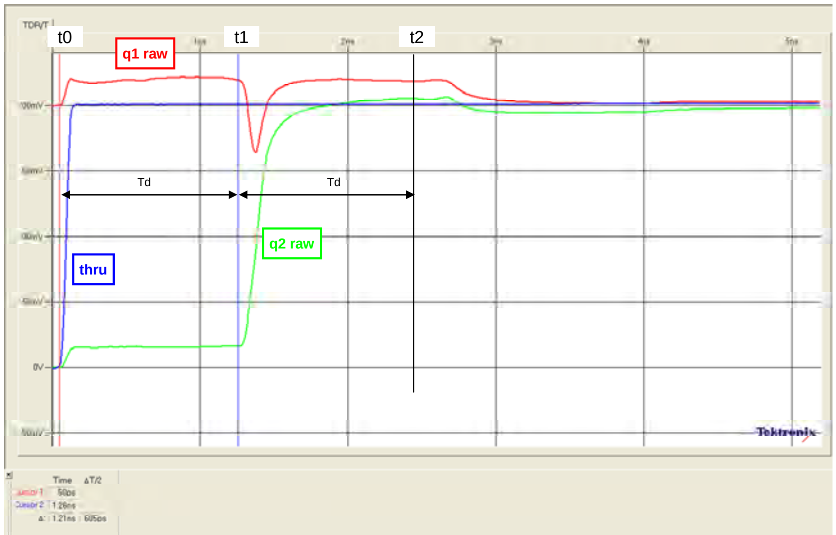


Figure 14: Initial SET2DIL Waveforms

Port 1 Waveform Manipulation

The waveform at q1 (red waveform in Figure 14) contains the single-ended TDR response plus the response of port 3 of our “Simplified” structure. To remove the TDR response we:

1) Locate the rising edge of the “thru” (blue waveform) – this is **t0** (50ps).
2) Locate the rising edge of q2 (green waveform) – this is **t1** (1.26ns).
3) Locate t2, which is t1 + (t1-t0); this represents the time after which multiple reflection effects dominate. In this case, it is 1.26ns + (1.26ns – 50ps) = 2.47ns.
4) Find q1’s initial offset voltage at t1 (239mV), and subtract that from the initial q1 waveform; result is the blue waveform of Figure 15 (which is masked by the green waveform after t1).
5) Zero all q1 values before t1 (green waveform of Figure 15).
   NOTE: the transition at t1 is smoothed so that no erroneous high-frequency components are added.

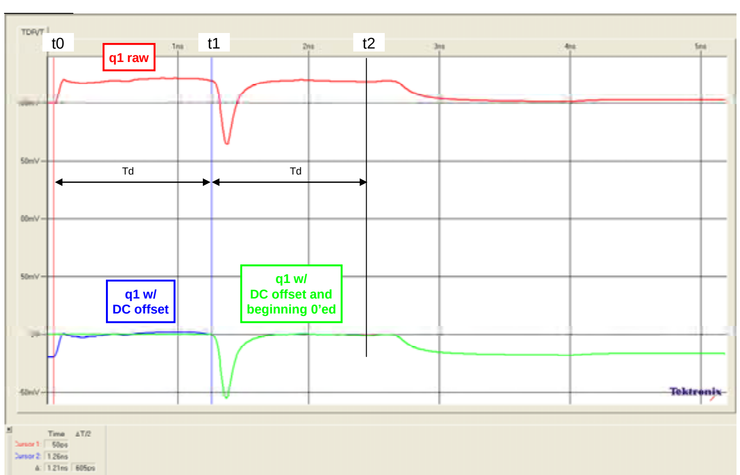


Figure 15: q1 w/ DC Offset, and Beginning Zeroed

6) Draw a smooth line between the resultant q1 value at t2 and 0V at t=∞ (green waveform of Figure 16). This eliminates multiple reflection effects, and is the final manipulation of this waveform; it now represents an equivalent of "p3" of our "simplified" method. NOTE: the transition at t2 is smoothed so that no erroneous high-frequency components are added.

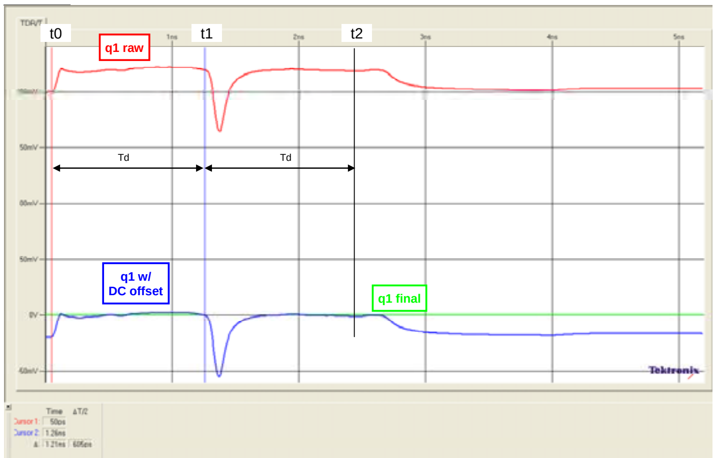


Figure 16: q1 Waveform Before and After All Manipulation

Port 2 Waveform Manipulation

The waveform at q2 (red waveform in Figure 17) contains the T21 response of our "Simplified" structure plus NEXT. We remove the NEXT components as follows:

1) Find q2's initial offset voltage at t1 (10.7mV), and subtract that from the initial q2 waveform. Result is the blue waveform of Figure 17.
2) Zero all q2 values before t1 – green waveform of Figure 17.
   NOTE: the transition at t1 is smoothed so that no erroneous high-frequency components are added.

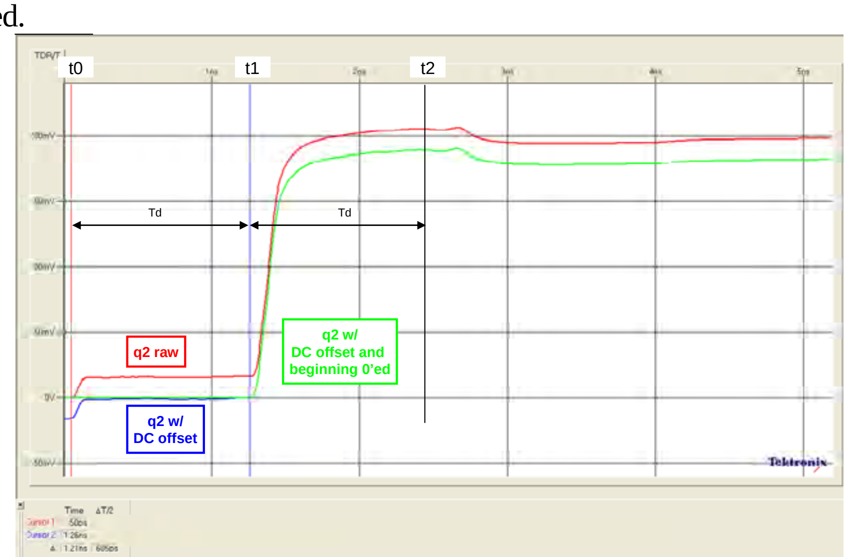


Figure 17: q2 w/ DC Offset, and Beginning Zeroed

3) Draw a smooth line (Bezier fit) between the q2 value at t2 and initial value at t=∞ (blue waveform of Figure 18). This is the final manipulation of this waveform; it now represents an equivalent of "p2" of our "simplified" method.

NOTE: the transition at t2 is smoothed so that no erroneous high-frequency components are added.

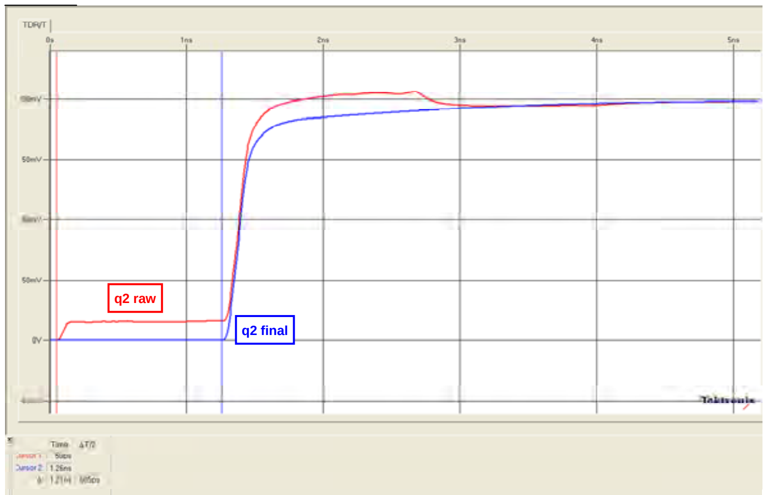


Figure 18: q2 Waveform Before and After All Manipulation

We now have 2 waveforms, equivalent to those of the "simplified" method. q1's manipulated waveform (red in Figure 19) can be subtracted from q2's manipulated waveform (green in Figure 19) to obtain TDD21 (blue in Figure 19)

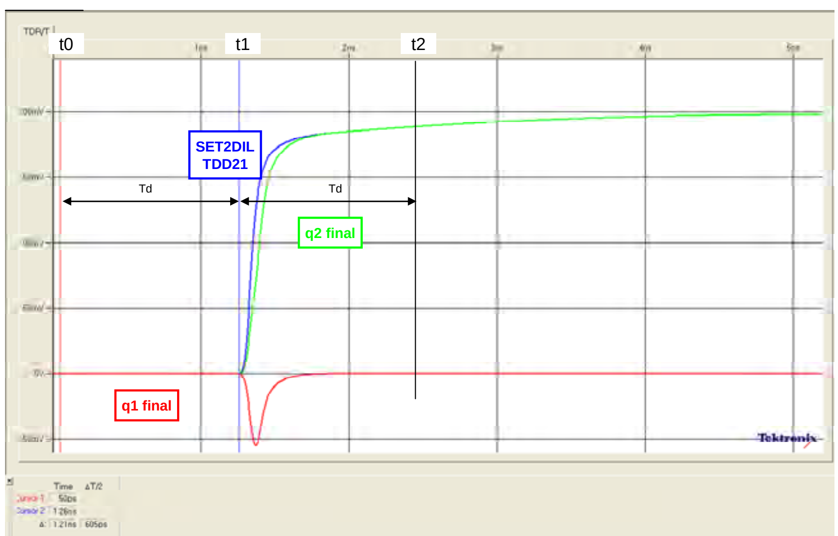


Figure 19: q1 & q2 Waveforms After All Manipulation, and SET2DIL TDD21

SDD21 Derivation

The TDD21 waveform (blue in Figure 20) can now be compared to the "thru" waveform (red in Figure 20) in the frequency domain, and the resultant SDD21 derived (red waveform in Figure 21, green waveform is VNA measurement of an equivalent structure).
NOTE: SDD21 of the VNA measurement is for a structure twice the length of the SET2DIL structure, since SET2DIL effectively doubles the length of the DUT.

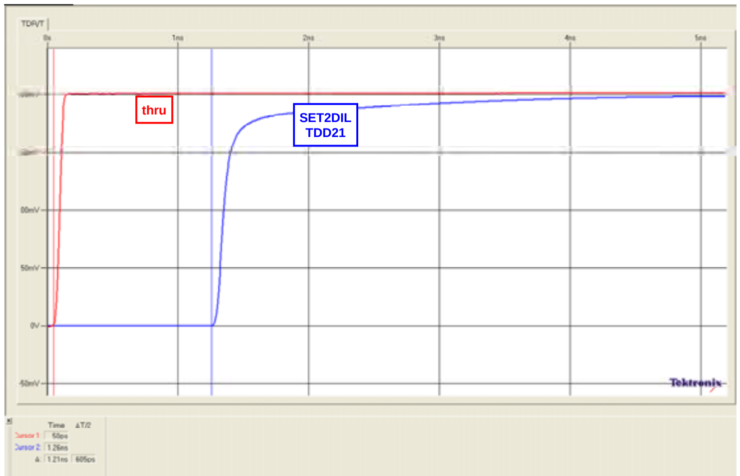


Figure 20: SET2DIL TDD21 and "thru"

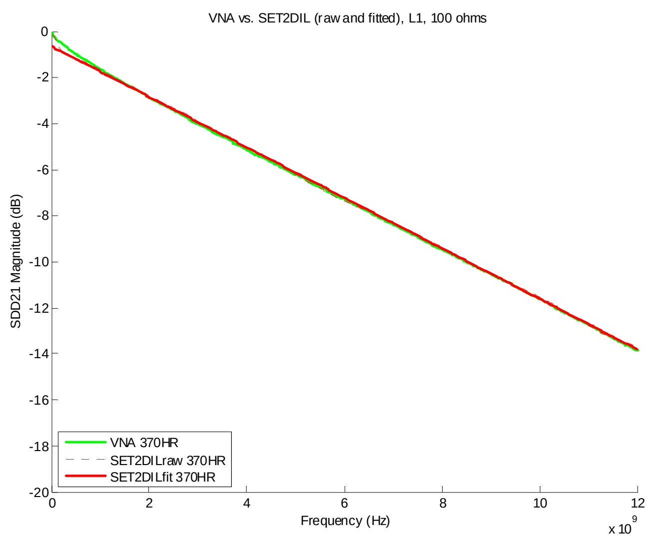


Figure 21: SET2DIL SDD21 (red) vs. VNA (green) SDD21

This SET2DIL method replaces 4-port VNA measurements for accurate measurement of SDD21. It has an added advantage that, due to the loopback, the test structure only needs to be ½ the length of its corresponding differential 4-port test structure.

It should be highlighted that measurements can be performed with a VNA and the results translated to the time-domain for waveform manipulation, and then back to the frequency domain for final SDD21 reporting. This technique then becomes an effective method to simplify the typical 4-port measurement to only a 2-port measurement.

It should also be emphasized that Matlab scripts have been developed to perform all the waveform manipulation automatically and perform FFT to derive SDD21 – no manual intervention is required.

SET2DIL Verification – Hspice Simulation

Extensive simulations were completed to compare the results of SET2DIL to VNA measurements, with very promising results. Three trace topologies were considered: microstrip, symmetric stripline, and asymmetric stripline. The impedance and loss were varied by changing the thickness of the dielectric to represent a broad range of impedance/loss characteristics (Figure 22).

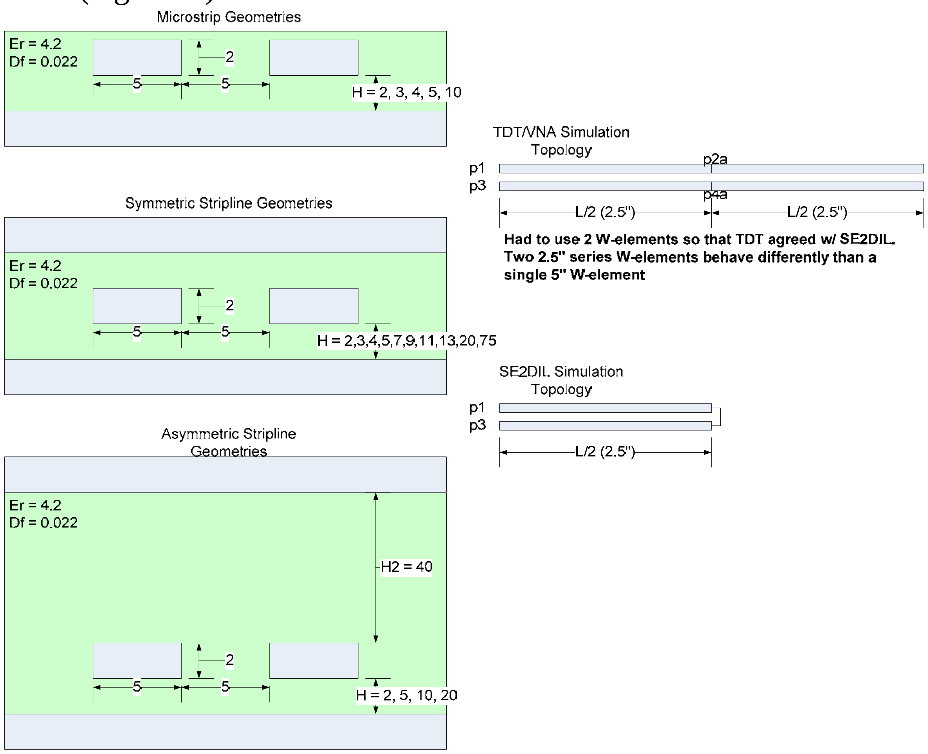


Figure 22: SET2DIL Simulation Dimensions

A critical adjustment to the simulations was to perform all simulations in the time domain, and then derive the frequency-domain response separately. Initially, we performed the VNA "baseline" simulations in the frequency domain, but found incongruities in the results. We discovered the problem to be a discrepancy between time and frequency domain results in Hspice. Performing the simulations in the time domain for both cases, and then converting to frequency domain, was used instead. Figure 24 shows an example (brown) where frequency-domain (AC) analysis is used It shows how the correlation between the 2 approaches is very good, though there is some simulator-induced discrepancy (which varied greatly, depending on the simulation topology).

Another required adjustment was to perform the TDT/VNA simulations on two 2.5" traces, instead of a single 5" trace which would be equivalent to the SET2DIL simulations on a 2.5" trace (representing a 5" DUT). There was a discrepancy between Hspice results for a single 5" DUT and two 2.5" traces.

The figures below show the simulation correlation results. SET2DIL results are in blue, VNA-equivalent results (derived from TDT) are in red. Note that, in every case, the correlation between SET2DIL and VNA is excellent. In fact, there is an added bonus that some low frequency ripples are smoothed by SET2DIL.

Though phase appears to not correlate in Figure 23, that is an artifact of the software that is plotting the results.

The asymmetric stripline case is not shown, but had similar excellent correlation.

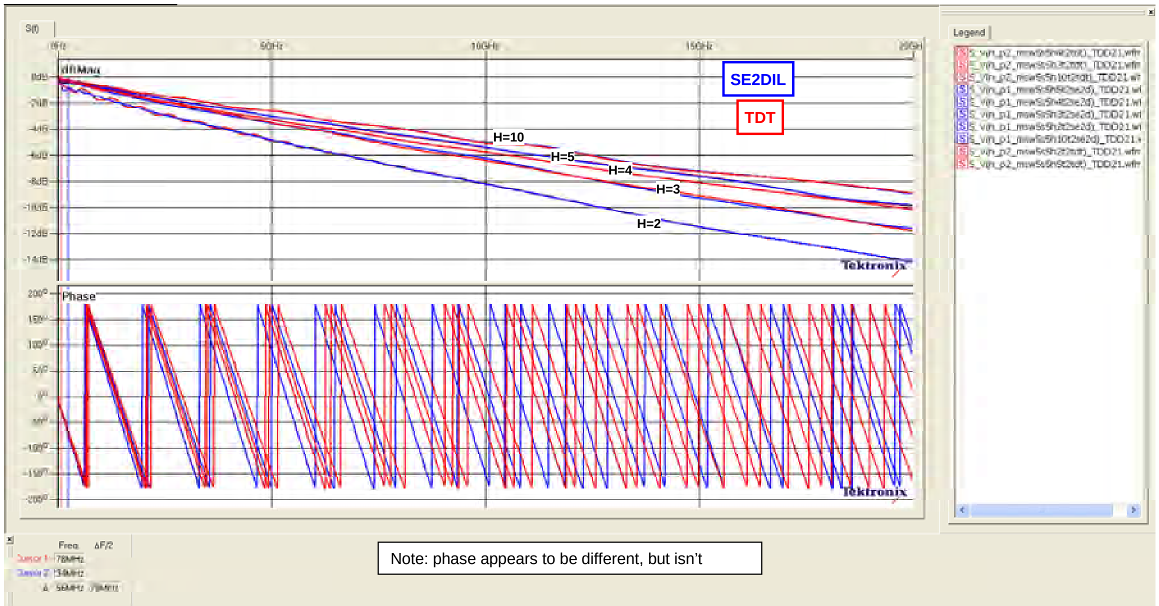


Figure 23: Microstrip Simulation Results

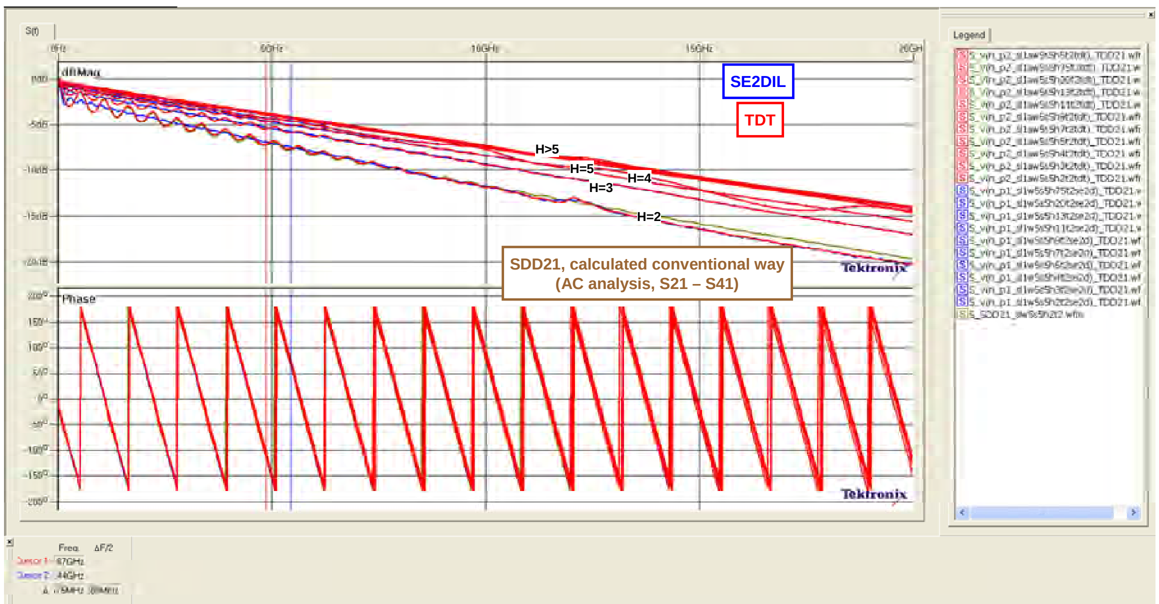


Figure 24: Symmetric Simulation Stripline Results

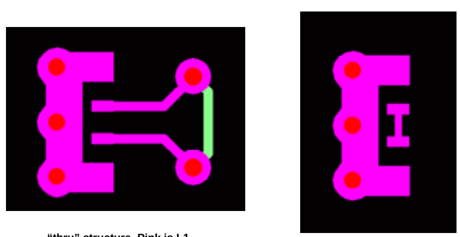
SET2DIL VERIFICATION - MEASUREMENT

Test Board Design

Test boards were built to investigate the correlation between SET2DIL and 4-port VNA.

The Test Board design had:

1) Launch structures compatible with GGB 50A-GS-450/50A-SG-450-EDP-D-450, 450 um differential probes, appropriate for >20GHz measurements, shown in Figure 25.
2) 10 representative trace types to be characterized:
   - L1 85 ohms; microstrip, no vias
   - L1 100 ohms, microstrip, no vias
   - L3 85 ohms, symmetric stripline, very short vias
   - L3 100 ohms, symmetric stripline, very short vias
   - L5 85 ohms, symmetric stripline, short vias
   - L5 100 ohms, symmetric stripline, short vias
   - L3 85 ohms, asymmetric stripline, very short vias
   - L5 85 ohms, asymmetric stripline, short vias
   - L12 85 ohms; microstrip, long vias (100 mils)
   - L12 100 ohms; microstrip, long vias (100 mils)
3) Both 4-port (standard VNA) and looped back 2-port (SET2DIL) topologies, representative of the trace type. The SET2DIL structures were ½ the length of the VNA traces, and were looped back at their end as shown in Figure 26.
4) 2 instances of each topology, spaced widely apart, to check for consistency
5) "shorting" structures for each layer – a very short connection between the 2 signal probe sites, as well as a "short thru" – a narrow trace directly between the probe sites. Both are shown in Figure 25.



"thru" structure, Pink is L1,
Green is L5
all traces 50 ohms

"short thru" structure
L1 only
4 mil trace between probe sites

Figure 25: Launch and Shorting Structures

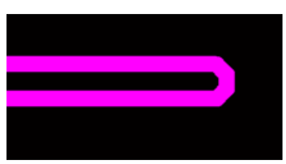


Figure 26: "Loop Back" at end of SET2DIL structures on Test Board

We built the design built using 3 different materials with various expected loss characteristics:

- Isola FR408HR ("408" in this paper)
- Panasonic 1566W Halogen Free ("1566" in this paper)
- Polyclad 370HR ("370" in this paper)

Four instances of each material built, 2 were backdrilled, and 2 were not.

Test Board Measurement Methodology

Measurements were performed with the same equipment for all structures (both 4-port and SET2DIL): an Agilent E8363B PNA with an N4420B test set for 4-port extension, with data from 10MHz to 20GHz collected. The data was collected in PLTS, which allowed for extensive post-processing.

For this paper, only measurements of the “short thru” were used as the “thru” reference. VNA calibration was performed to the probe tips, so VNA measurements would include launch parasitics and via effects. Using the “short thru” as the SET2DIL reference best mimicked the VNA measurement, though it appears it had some parasitic effect (SET2DIL consistently under predicted loss by about 0.5dB)..

For this paper (due to time constraints), only a single **backdrilled** board of each material, and only a single topology (4-port and 2-port SET2DIL) of each trace type, was measured. We emphasize here that the results of non-backdrilled test structures have not been studied, and might be markedly different.

The 4-port results were exported directly as differential touchstone format, with SDD21 directly available.

The 2-port SET2DIL results were:

1) converted to the time domain with Agilent’s PLTS
2) brought into a Matlab script (along with the “thru” time domain information), which:
    a. performed all the waveform manipulation
    b. derived SDD21
    c. performed a linear fit to the raw SET2DIL SDD21 data
    d. exported the results into an Excel-compatible file.

The 4-port VNA and SET2DIL SDD21 were then compared for each trace type/material.

Test Board Measurement Initial Results and Algorithm Enhancements

The top layer microstrip results were the first to be examined and showed SET2DIL performing poorly – SDD21 had a large amount of noise, and did not correlate well to VNA results. Careful reviewing of the raw waveforms and the result of each step of the waveform manipulation allowed enhancing the waveform manipulation algorithm to achieve better results. For instance, we found that the bumps and dips caused by impedance variation were adding unwanted noise to SDD21 throughout the frequency range. To reduce this, the algorithm truncated the data sooner – at ½ the distance between t1 and t2 (see Figure 16), instead of at t2. And, for microstrip, we truncated the data as soon as the data crossed zero after the FEXT dip, if it did (the FEXT waveform should never cross 0, hence data that was >0 was due to impedance variation). Other enhancements included filtering the initial data (measurement data was noisier than simulation data), and calculating a linear fit to the raw data, based only on the data from 2 to 12 GHz.

The results reflect these enhancements.

SET2DIL Phase

The SET2DIL Phase results always showed exceptional correlation to VNA, as would be expected, given the simplicity of its derivation. A single, worst-case graph is shown in Figure 27 – all other results were equivalent or better.

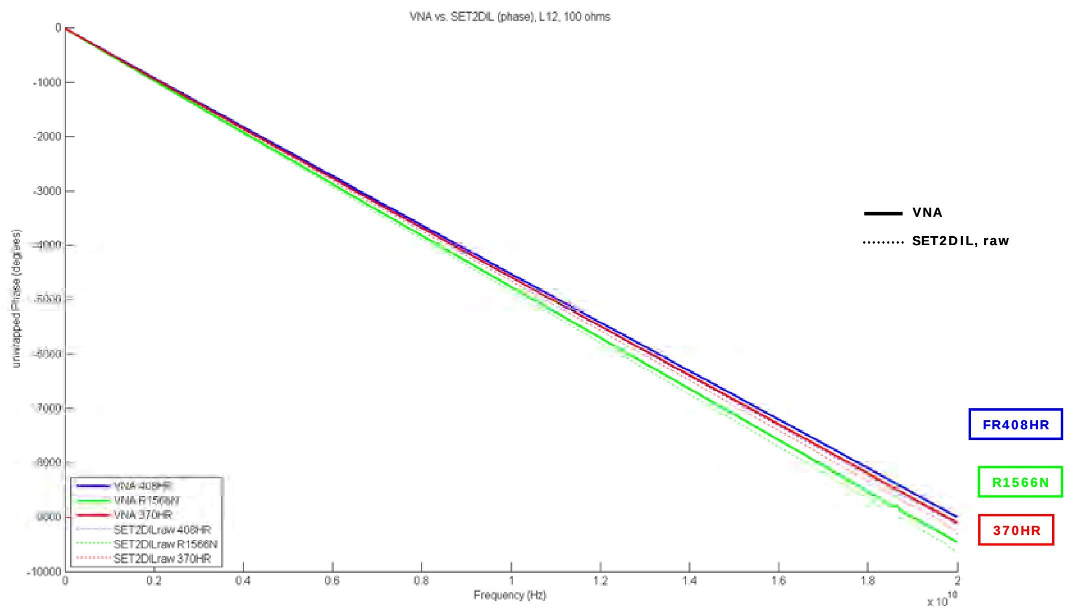


Figure 27: SET2DIL vs VNA Phase (unwrapped) – L12, 100 ohms

SET2DIL L1 Raw Results

Figure 29 demonstrates the raw results of L1, 85 and 100 ohms, w/o curve fitting applied. Some things to note:

1) Data beyond about ~12 GHz has too much noise to be credible – hence we cropped data points > 12GHz
2) The differences between the material types is clear above about 2GHz.
3) The raw data is, however, hard to use, it's not nearly as clear as the quiet results hoped for.

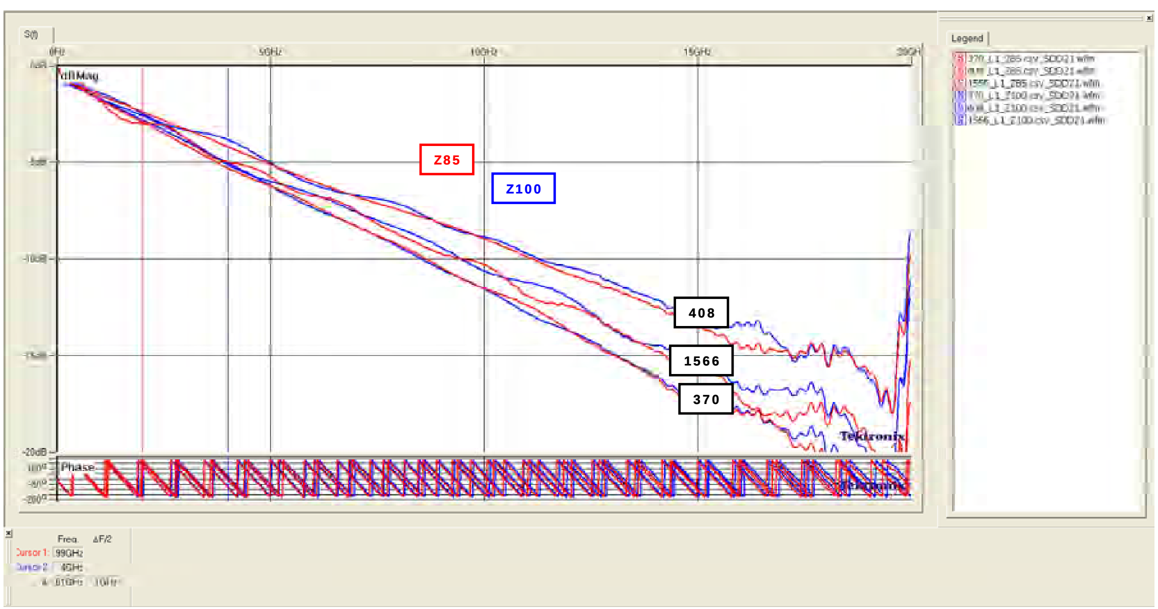


Figure 28: L1 Z100 Raw SET dB Magnitude

To smooth the data, a curve-fitting algorithm was applied, fitting the 2 to 12 GHz data to a linear function, y = mx + b.

SET2DIL L1 Fitted Results

Figure 29 demonstrates the results of the same data with the curve-fitting algorithm applied, showing raw and fitted SETDIL magnitude data vs. VNA. Some things to note:

1) The fitted SET2DIL tracks within 1/2dB of the VNA data between 2 and 12GHz – this is true for all trace types and materials, except for L12 (which will be discussed later).
2) SET2DIL predicts slightly less loss (~0.5dB) than VNA at 12 GHz for the 408 material. This is to be expected, since SET2DIL removes the effects of the launch, which are included in the VNA data (calibrated to the probe tips). Note: VNA measurements of the "thru" structure showed that it had an insertion loss of ~0.7dB at 12GHz (see Figure 30).
3) The linear fit fails below 2 GHz, where the square root function of the conductor loss dominates.

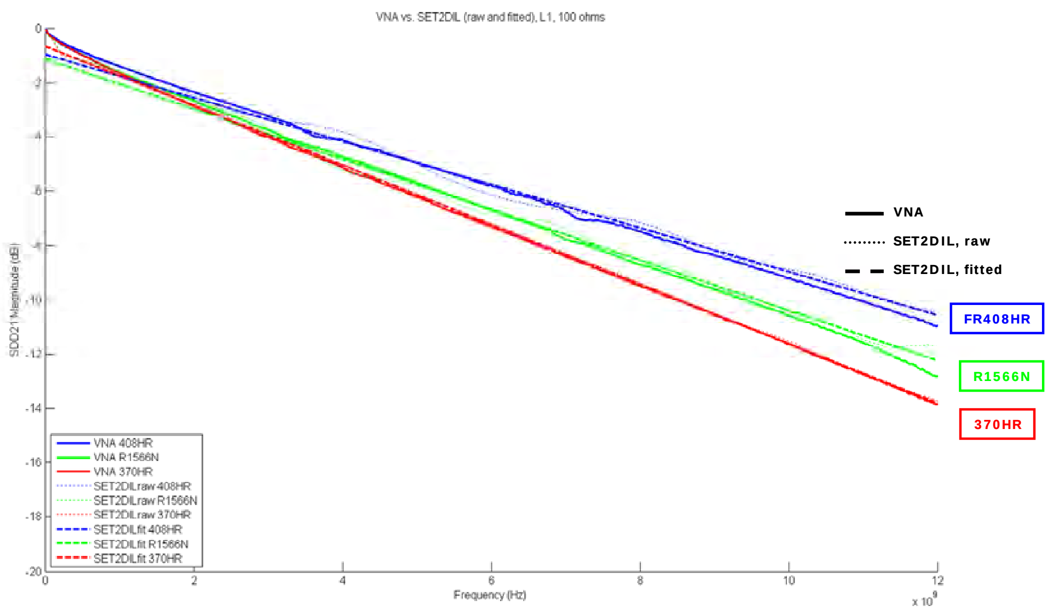


Figure 29: L1 Z100 Raw and Fitted SET2DIL vs. VNA dB Magnitude

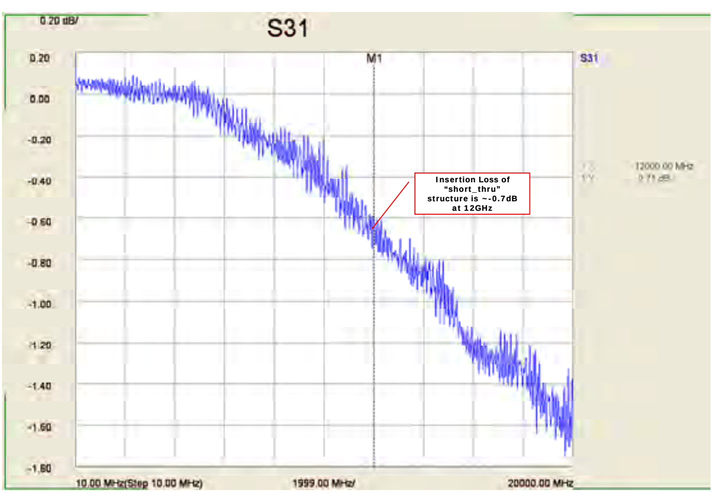


Figure 30: Insertion Loss of "short_thru"

The L1, Z85 results were similar, see Figure 31.

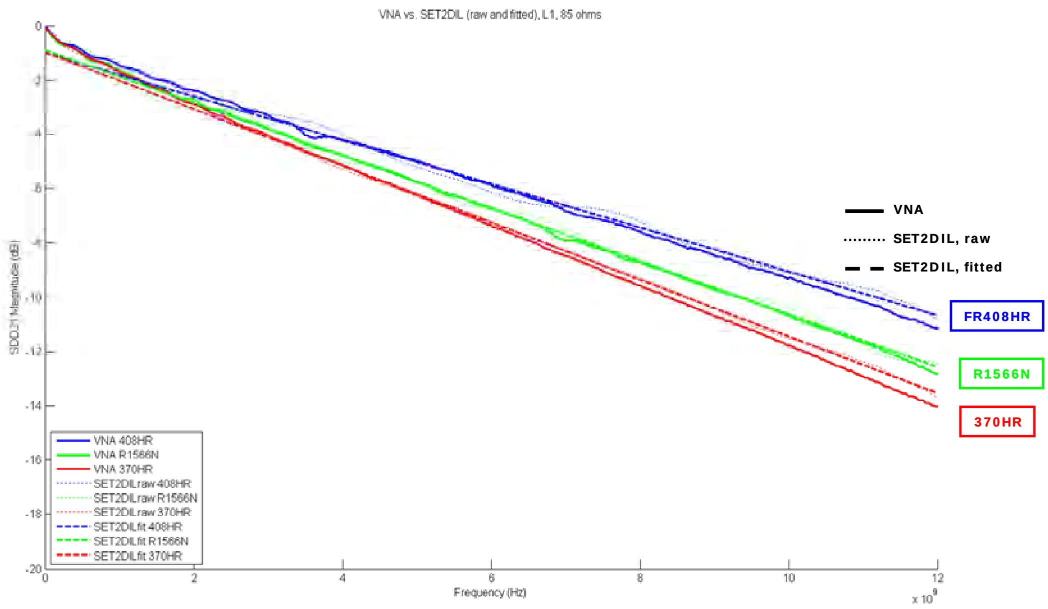


Figure 31: L1 Z85 SET2DIL vs. VNA dB Magnitude

SET2DIL Stripline Results

The stripline results were better than microstrip, with much less ripple induced from impedance variations (our assumption at this point). Figure 29 shows typical stripline results – L5, 100 ohms. As with microstrip, FR408 has the expected 0.5dB less loss at 12GHz for SET2DIL.

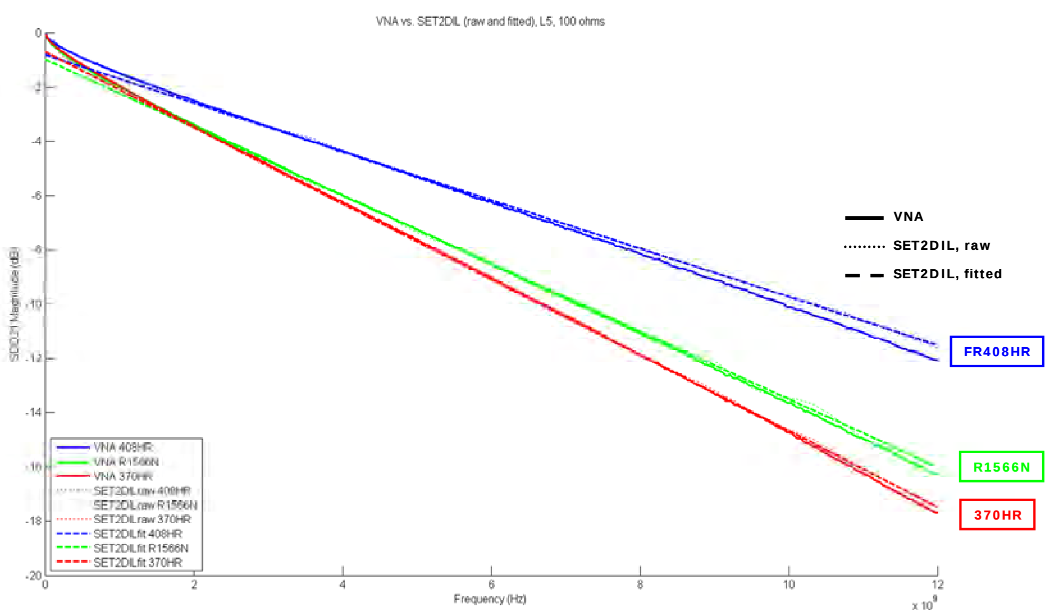


Figure 32: Typical Stripline results – L5, 100 ohms SET2DIL vs. VNA dB Magnitude

Figure 33 shows more of the stripline results,; clearly SET2DIL reproduces the VNA results very well. FR408 shows the same trend – consistently under-estimating insertion loss by about 0.5dB at 12GHz.

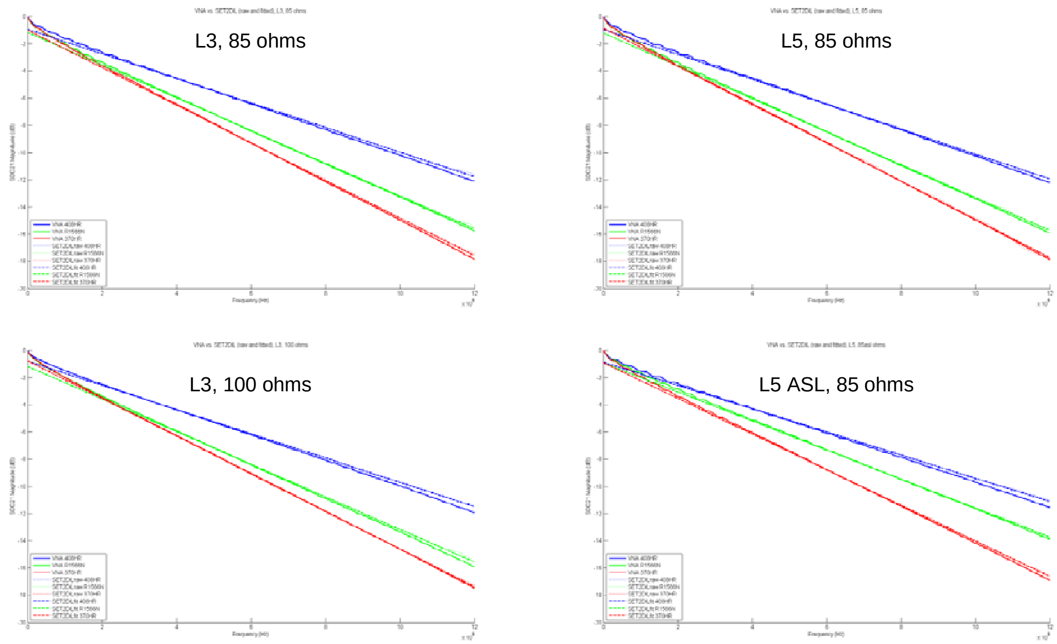


Figure 33: Representative Stripline results – SET2DIL vs. VNA dB Magnitude

SET2DIL L12 Results

As shown in Figure 34, the L12 results were markedly worse than the other trace types, apparently due to the long (0.100") vias between the launch and the trace. More study is undergoing to see if these can be improved, but they indicate that there may be a limit to how long vias can be before they impact the SET2DIL results significantly. In the absence of a fix, vendors might be forced to place loss launch structures for the bottom layer on that layer, rather than on the top. Similarly, stripline traces near the bottom of the board might have to be probed from the bottom, with the vias backdrilled from the top.

Since the vast majority of stackups are symmetric, however, it might be a valid assumption that the results from the top layer will equally apply to the bottom layer, and separate probing of the bottom layer is unnecessary. More data is needed to determine if the loss characteristics of the top and bottom layers (and corresponding equivalent stripline layers) are equal, or they are markedly different, as are impedance results.

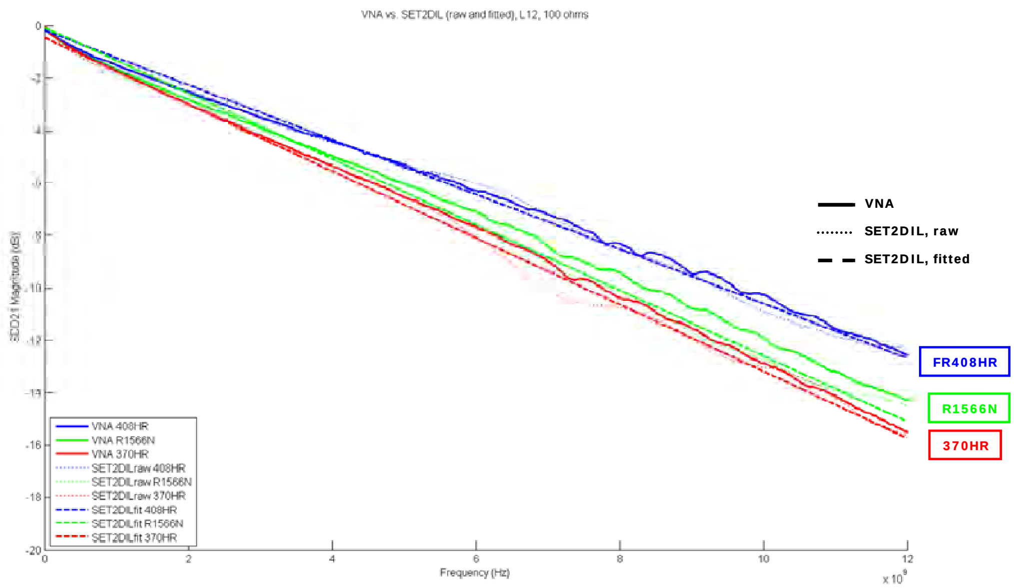


Figure 34: L12, Z100 ohms Fitted SET2DIL vs. VNA dB Magnitude

SET2DIL to Measure Impedance - SDD11

The same SET2DIL structure can be used to measure impedance and thus replace the current impedance coupons – with a slightly different algorithm to extract impedance (subtract NEXT from the TDR response). The significant differences will be:

1) A slightly shorter trace: 4" vs. 6". A quieter launch would make accurate TDR measurements of these shorter structures possible (see the "**Error! Reference source not found.**" section). This also reduces the board real estate required.
2) Traces that end in a short, instead of an open. May be confusing at first (vendors are used to seeing the waveform rise at the end), but we only care about the waveform before the end.
3) Traces that don't need a via at the far end – reducing the board real estate cost.

Effect of Vias on Stripline SET2DIL Structure

Another consideration is the effect of vias on stripline traces. To properly de-embed the effects of those vias (which can be considerable at the frequencies of interest) would require the equivalent of on-board calibration structures (probably TRL). This is not reasonable for HVM-compatible testing. Instead, the effects of vias can we minimized by:

1) Using via padstacks that have an impedance of approximately 50 ohms. This will probably take some trial-and-error, but is not exceedingly difficult. Typical 10mil drill vias are close to 50 ohms, as long as they are kept separated from each other (having 2 vias of a differential pair close together significantly lowers the impedance)
2) Backdrilling any vias with significant via stubs (>~40 mils). This is perhaps the most painful change to HVM process that will be necessary, but it is probably unavoidable for any HVM-compatible multi-GHz SDD21 measurement technique.

SUMMARY

The results from the simulations and the Test Boards were extremely encouraging, though they revealed some limits in the current implementation of the method. It is clear, however, that SET2DIL is capable of accurate enough measurements, without the need for a 4-port VNA and probing stations, as is used in the laboratory environment. Thus, the acceptable loss characteristics can be specified and measured in the HVM environment, very similar to impedance control today. The factors affecting differential insertion loss (loss tangent, trace geometries, copper texture, etc.) can then be adjusted to meet the needs of high speed differential signals.

This work should still be considered preliminary; further work might very well make SET2DIL align even better with corresponding 4-port VNA measurements and at higher frequencies. However, the current 12GHz measurements are adequate to accurately discern differences in materials and trace geometry and texture. Trace losses are also linear beyond 12GHz, so the linear fit will be valid to > 12GHz.

Coupling the SET2DIL method with a high-frequency compatible, hand-held, 2-port probe, opens up the possibility that measurements of SDD21 in an HVM environment will be very similar to today's impedance measurements, with very little added cost or time.

The next steps in realizing this goal are to:

1) Evaluate and perfect the hand-held probe
2) Bring the Matlab scripts into the measurement tool, so real-time plotting of the results is available (rather than as a separate post-processing step)
3) Make measurements, waveform manipulation, plotting results, and reporting value of reports a very simple operation – a few button clicks.

ACKNOWLEDGMENTS

Special thanks are due Xiaoning Ye and John Abbott for providing the algorithm to convert from the time to frequency domains in Matlab.

Recognition is due Dennis Miller, who conceived the hand-held probe architecture.

And finally, thanks to Brian Hood who realized the suitability of applying a Bezier fit and provided the Matlab code.

REFERENCES[i]

[i] **Mixed-mode S-parameter characterization of differential structures**
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10-12 Dec. 2003 Page(s):533 - 537