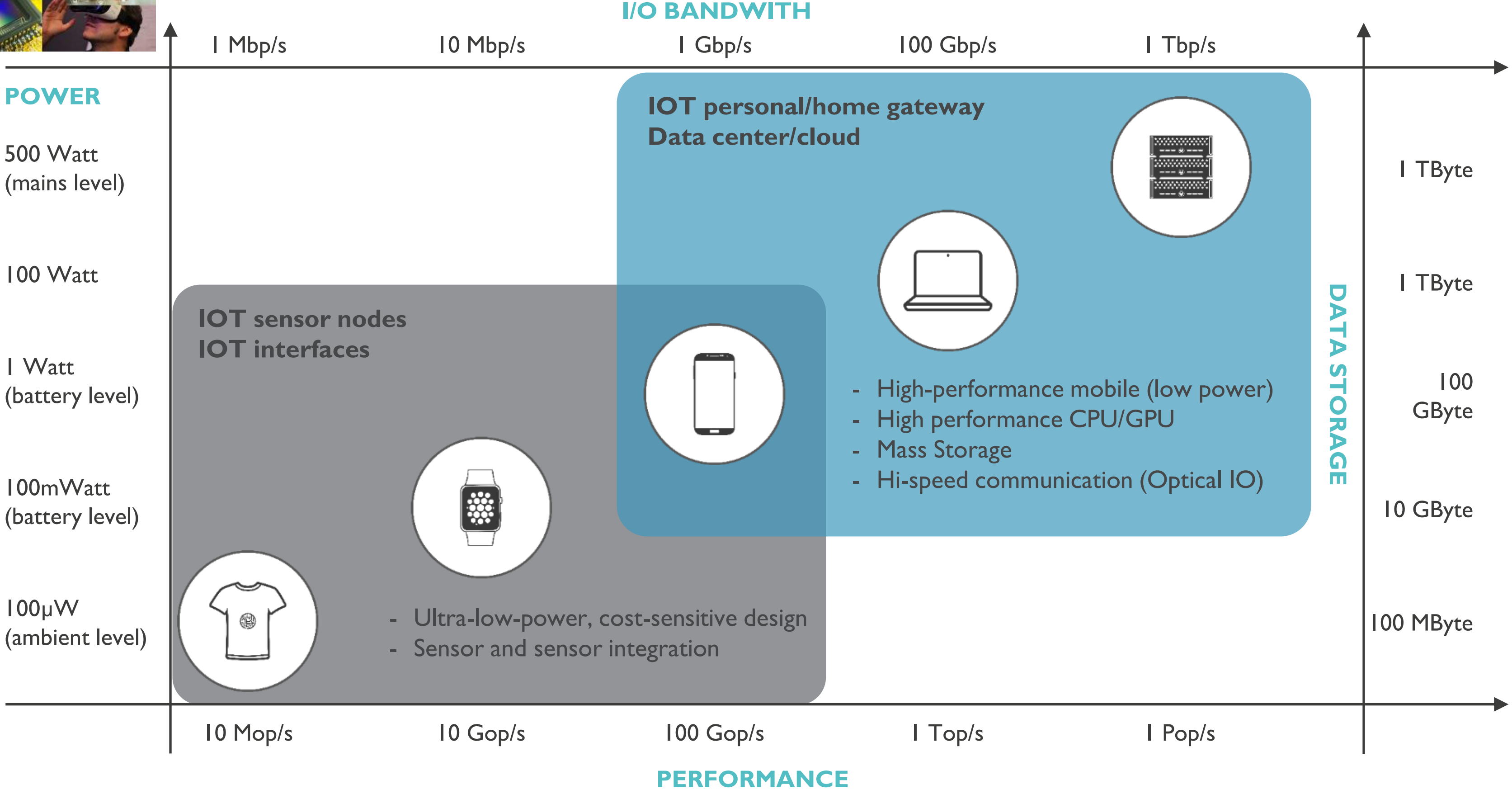
SELECTIVE ETCH REQUIREMENTS FOR THE NEXT GENERATION OF SEMICONDUCTOR DEVICES

FRANK HOLSTEYNS

ON BEHALF OF THE SURFACE AND INTERFACE PREPARATION GROUP OF THE UNIT PROCESS DEPARTMENT

10TH OF APRIL 2018



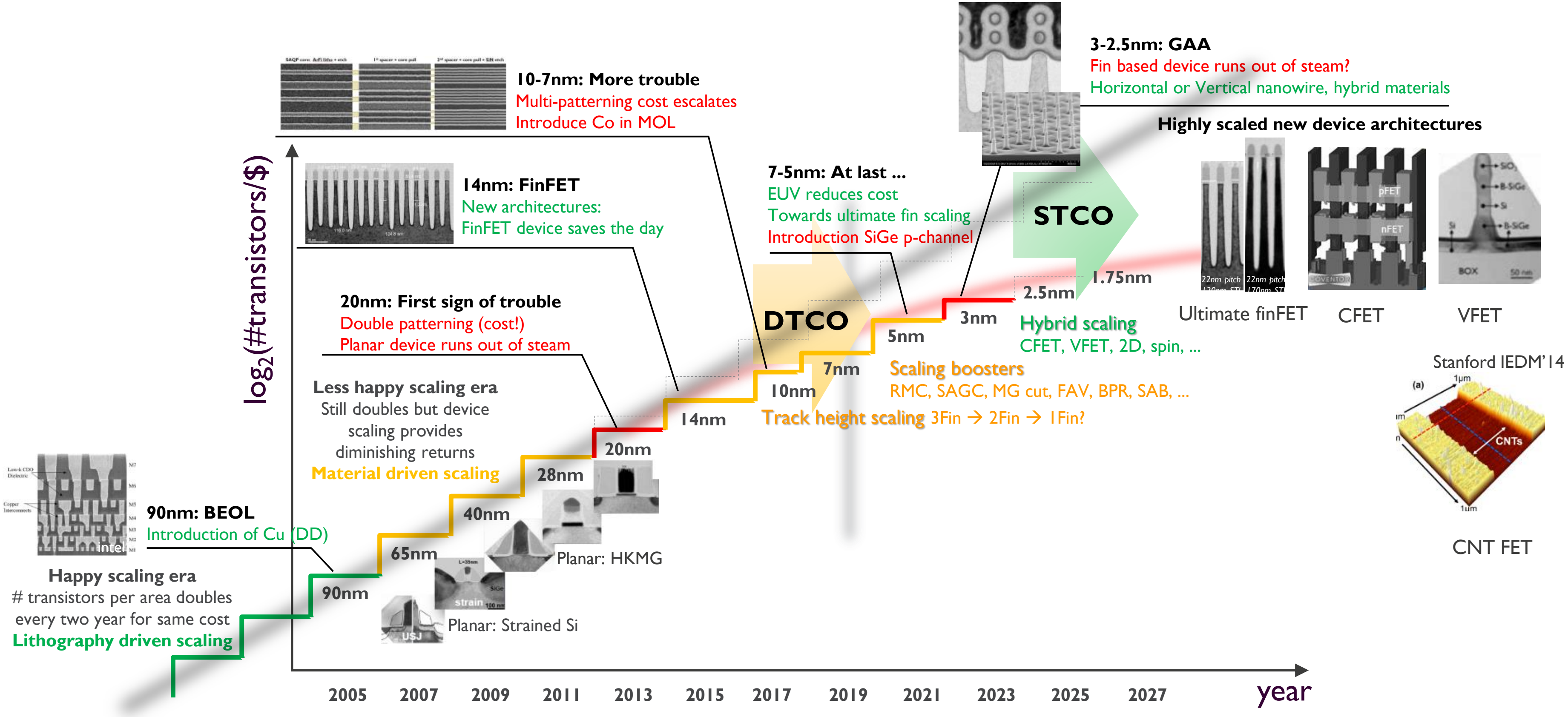
IOT personal/home gateway
Data center/cloud

- High-performance mobile (low power)
- High performance CPU/GPU
- Mass Storage
- Hi-speed communication (Optical IO)

IOT sensor nodes
IOT interfaces

- Ultra-low-power, cost-sensitive design
- Sensor and sensor integration

DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION



Happy scaling era
transistors per area doubles every two year for same cost
Lithography driven scaling

90nm: BEOL
Introduction of Cu (DD)

Planar: Strained Si

Planar: HKMG

Less happy scaling era
Still doubles but device scaling provides diminishing returns
Material driven scaling

20nm: First sign of trouble
Double patterning (cost!)
Planar device runs out of steam

14nm: FinFET
New architectures:
FinFET device saves the day

10-7nm: More trouble
Multi-patterning cost escalates
Introduce Co in MOL

7-5nm: At last …
EUV reduces cost
Towards ultimate fin scaling
Introduction SiGe p-channel

Track height scaling 3Fin → 2Fin → 1Fin?

Scaling boosters
RMC, SAGC, MG cut, FAV, BPR, SAB, …

Hybrid scaling
CFET, VFET, 2D, spin, …

3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

Highly scaled new device architectures

Ultimate finFET

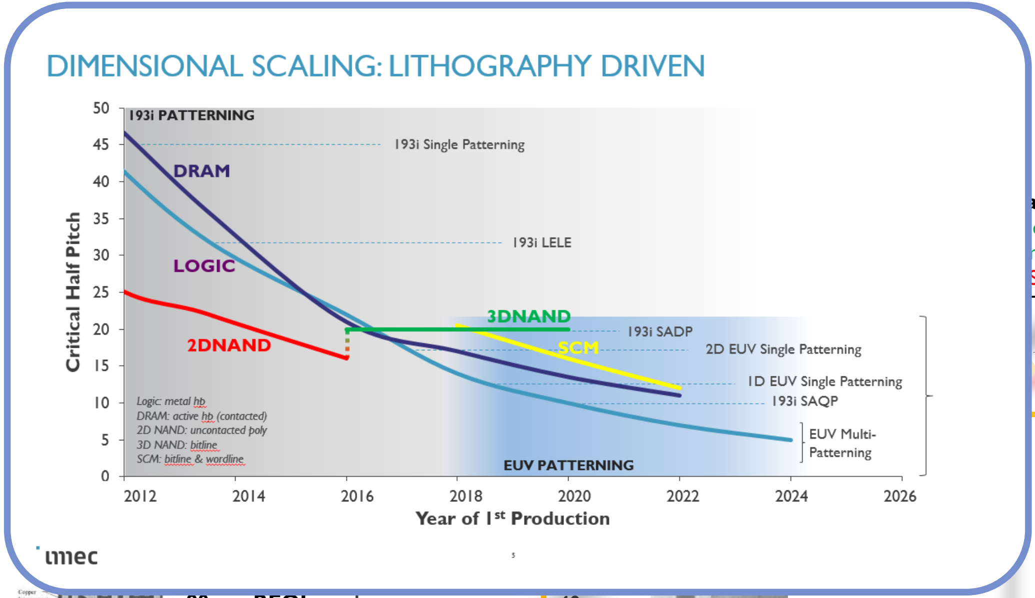
CFET

VFET

Stanford IEDM'14

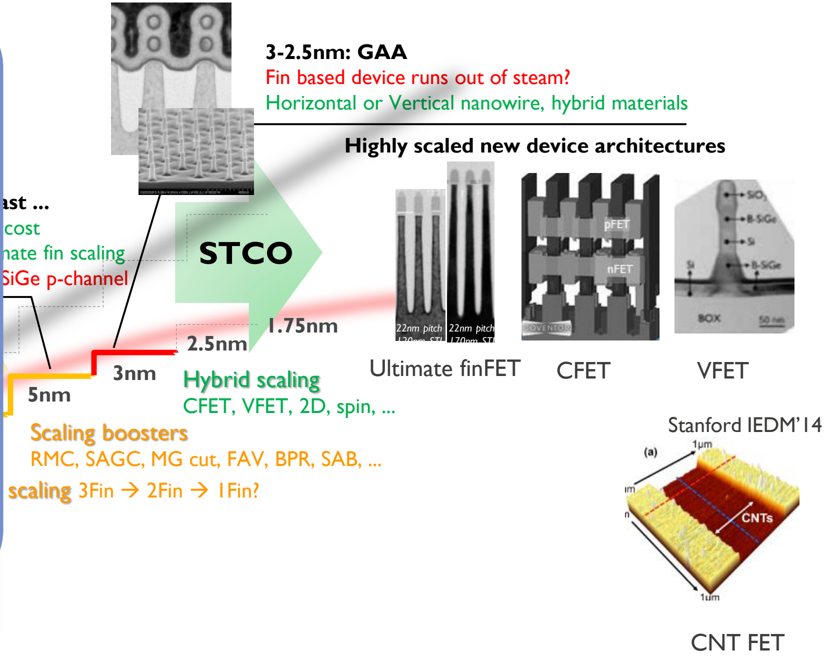
CNT FET

DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION



DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

Logic: metal hp
DRAM: active hp (contacted)
2D NAND: uncontacted poly
3D NAND: bitline
SCM: bitline & wordline



3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

Highly scaled new device architectures

ast ...
cost
nate fin scaling
SiGe p-channel

STCO

1.75nm
2.5nm
3nm
5nm

Hybrid scaling
CFET, VFET, 2D, spin, ...

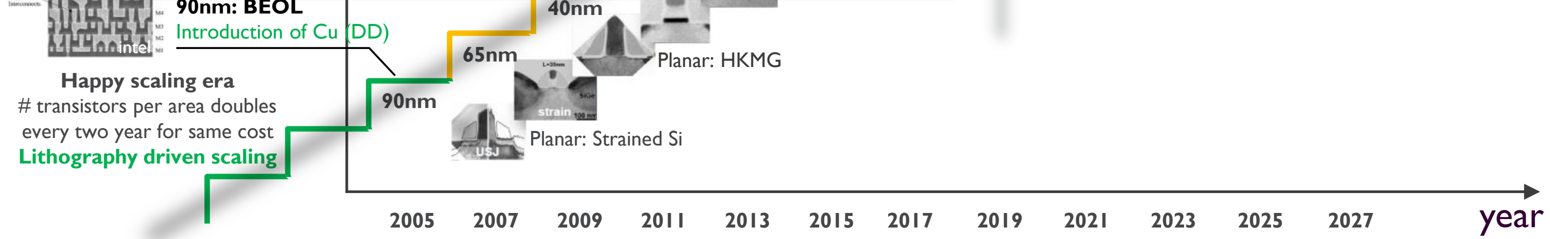
Scaling boosters
RMC, SAGC, MG cut, FAV, BPR, SAB, ...

scaling 3Fin → 2Fin → 1Fin?

Ultimate finFET
CFET
VFET

Stanford IEDM'14

CNT FET



90nm: BEOL
Introduction of Cu (DD)

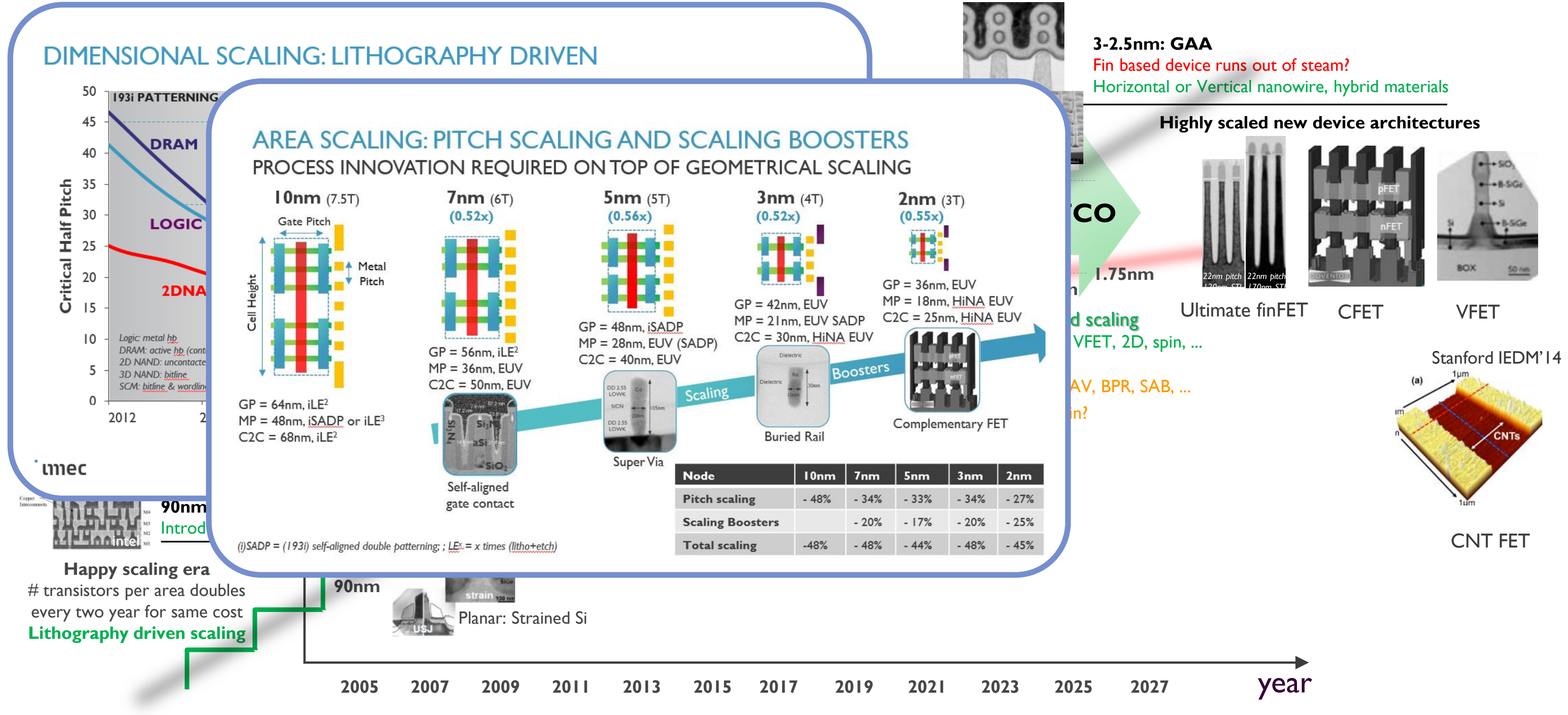
Happy scaling era
transistors per area doubles every two year for same cost
Lithography driven scaling

90nm
65nm
40nm

Planar: HKMG
Planar: Strained Si

2005 2007 2009 2011 2013 2015 2017 2019 2021 2023 2025 2027
year

DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION



DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

90nm
Introd

Happy scaling era
transistors per area doubles every two year for same cost
Lithography driven scaling

AREA SCALING: PITCH SCALING AND SCALING BOOSTERS

PROCESS INNOVATION REQUIRED ON TOP OF GEOMETRICAL SCALING

10nm (7.5T)

GP = 64nm, iLE²
MP = 48nm, iSADP or iLE³
C2C = 68nm, iLE²

7nm (6T)
(0.52x)
GP = 56nm, iLE²
MP = 36nm, EUV
C2C = 50nm, EUV

5nm (5T)
(0.56x)
GP = 48nm, iSADP
MP = 28nm, EUV (SADP)
C2C = 40nm, EUV

3nm (4T)
(0.52x)
GP = 42nm, EUV
MP = 21nm, EUV SADP
C2C = 30nm, HiNA EUV

2nm (3T)
(0.55x)
GP = 36nm, EUV
MP = 18nm, HiNA EUV
C2C = 25nm, HiNA EUV

Self-aligned gate contact

Super Via

Buried Rail

Complementary FET

Node	10nm	7nm	5nm	3nm	2nm
Pitch scaling	- 48%	- 34%	- 33%	- 34%	- 27%
Scaling Boosters		- 20%	- 17%	- 20%	- 25%
Total scaling	-48%	- 48%	- 44%	- 48%	- 45%

(i)SADP = (193i) self-aligned double patterning; ; LEˣ = x times (litho+etch)

3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

Highly scaled new device architectures

d scaling
VFET, 2D, spin, ...
AV, BPR, SAB, ...
in?

Ultimate finFET

CFET

VFET

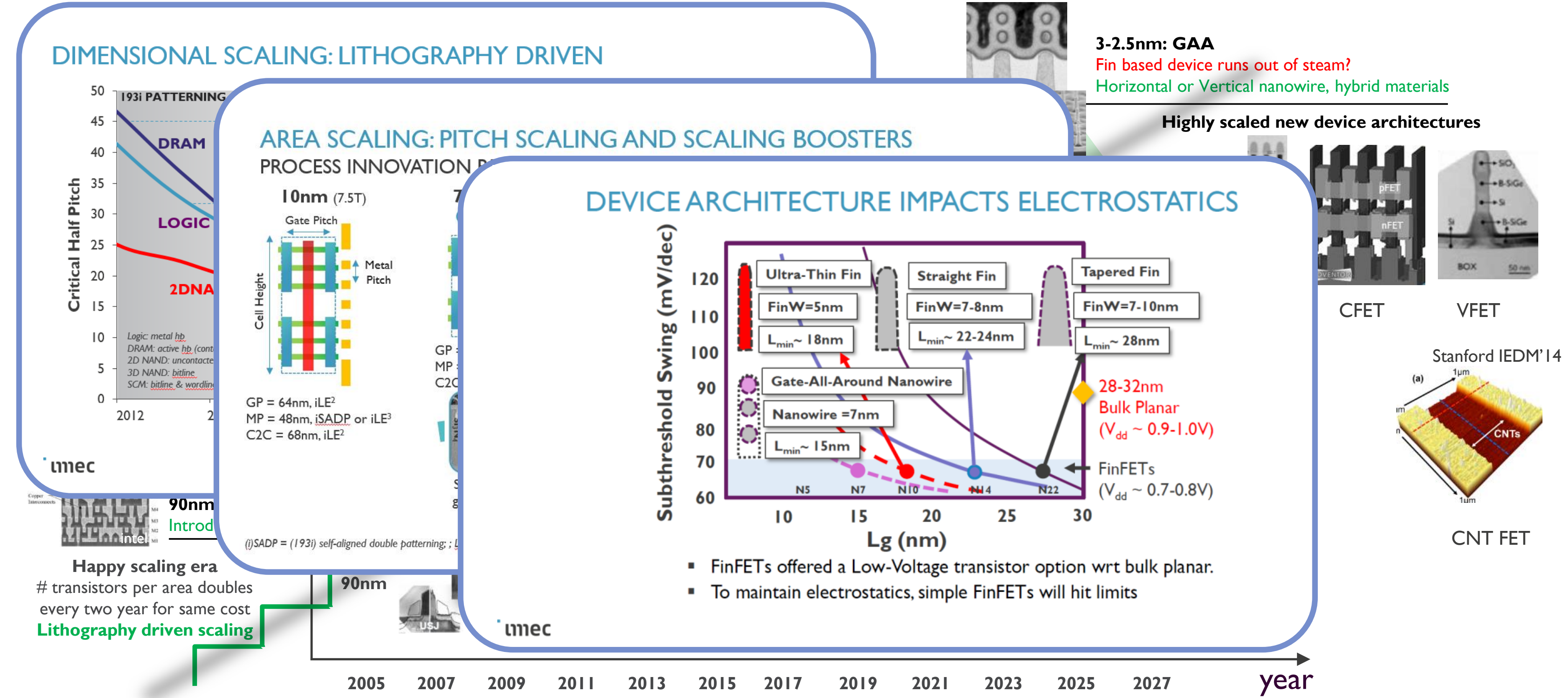
Stanford IEDM'14

CNT FET

90nm

Planar: Strained Si

DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION



DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

Logic: metal hb
DRAM: active hb (cont
2D NAND: uncontacte
3D NAND: bitline
SCM: bitline & wordlin

imec

AREA SCALING: PITCH SCALING AND SCALING BOOSTERS

PROCESS INNOVATION P

GP = 64nm, iLE^2
MP = 48nm, iSADP or iLE^3
C2C = 68nm, iLE^2

GP
MP
C2C

(i)SADP = (193i) self-aligned double patterning; ; L

DEVICE ARCHITECTURE IMPACTS ELECTROSTATICS

- FinFETs offered a Low-Voltage transistor option wrt bulk planar.
- To maintain electrostatics, simple FinFETs will hit limits

imec

90nm
Introd

90nm

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Stanford IEDM'14

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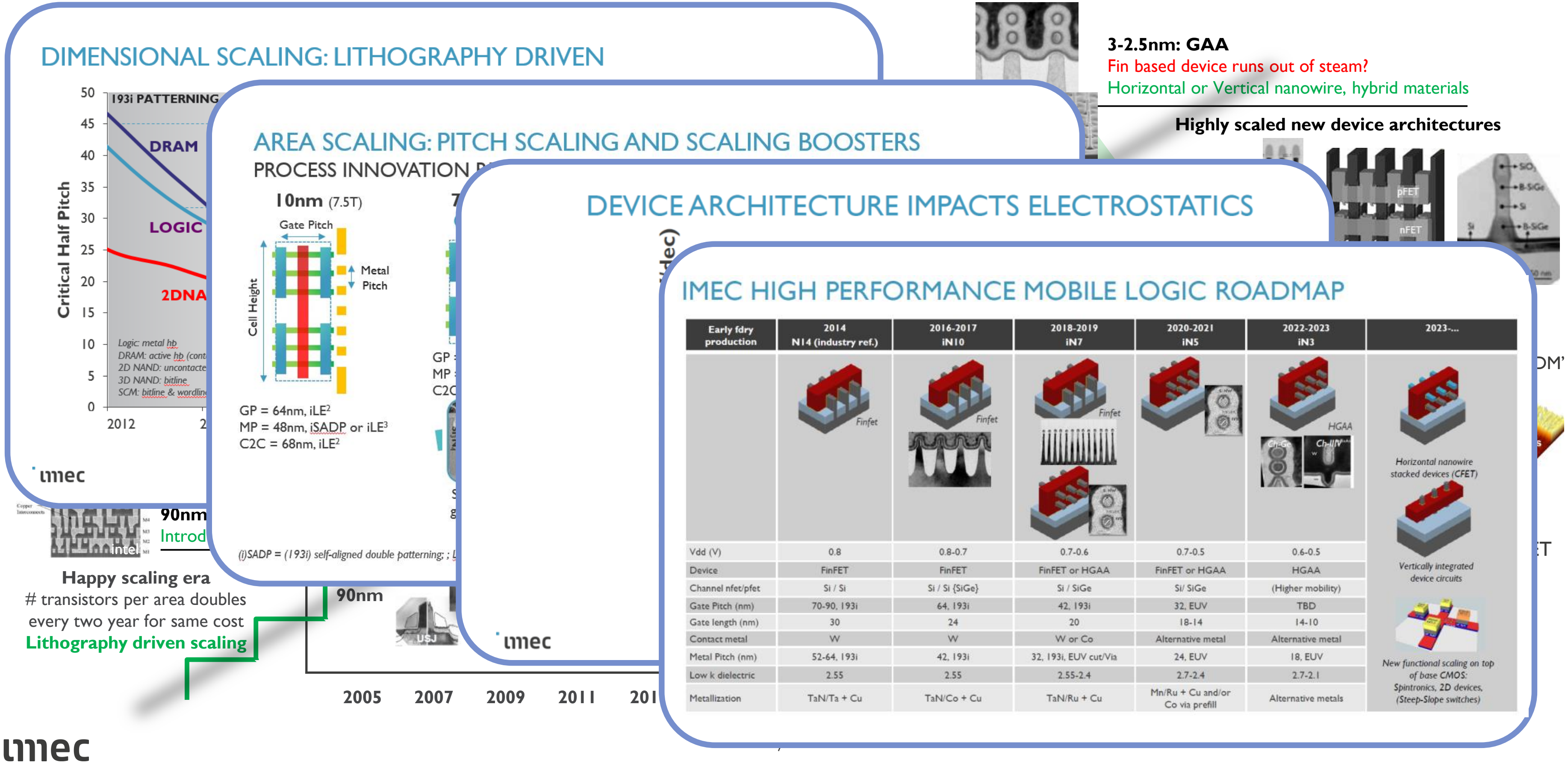

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ımec

AREA SCALING: PITCH SCALING AND SCALING BOOSTERS

PROCESS INNOVATION P

10nm (7.5T)

GP = 64nm, iLE^2
MP = 48nm, iSADP or iLE^3
C2C = 68nm, iLE^2

GP
MP
C2C

(i)SADP = (193i) self-aligned double patterning; ; L

ımec

DEVICE ARCHITECTURE IMPACTS ELECTROSTATICS

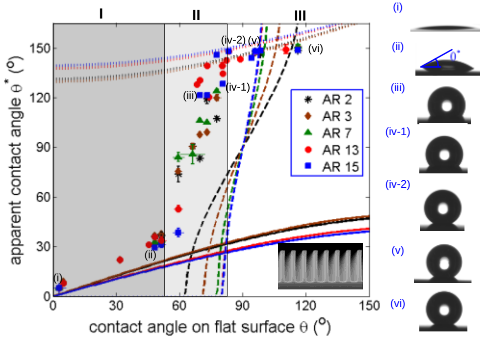
ımec

IMEC HIGH PERFORMANCE MOBILE LOGIC ROADMAP

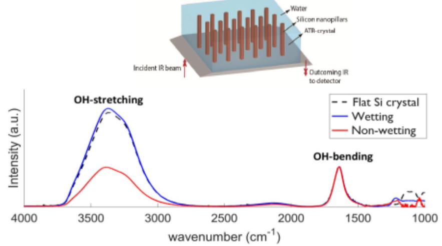
Early fdry production	2014 N14 (industry ref.)	2016-2017 iN10	2018-2019 iN7	2020-2021 iN5	2022-2023 iN3	2023-...
	Finfet	Finfet	Finfet		HGAA Ch-Ge Ch-III/V	Horizontal nanowire stacked devices (CFET) Vertically integrated device circuits New functional scaling on top of base CMOS: Spintronics, 2D devices, (Steep-Slope switches)
Vdd (V)	0.8	0.8-0.7	0.7-0.6	0.7-0.5	0.6-0.5	
Device	FinFET	FinFET	FinFET or HGAA	FinFET or HGAA	HGAA	
Channel nfet/pfet	Si / Si	Si / Si {SiGe}	Si / SiGe	Si/ SiGe	(Higher mobility)	
Gate Pitch (nm)	70-90, 193i	64, 193i	42, 193i	32, EUV	TBD	
Gate length (nm)	30	24	20	18-14	14-10	
Contact metal	W	W	W or Co	Alternative metal	Alternative metal	
Metal Pitch (nm)	52-64, 193i	42, 193i	32, 193i, EUV cut/Via	24, EUV	18, EUV	
Low k dielectric	2.55	2.55	2.55-2.4	2.7-2.4	2.7-2.1	
Metallization	TaN/Ta + Cu	TaN/Co + Cu	TaN/Ru + Cu	Mn/Ru + Cu and/or Co via prefill	Alternative metals	

AS SCALING CONTINUES, CHALLENGES ARISE IN WET PROCESSING

Wetting and kinetics for nanostructured surfaces



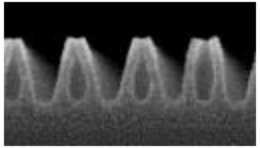
Actual wetting states confirmed by optical reflectometry; Xu et al., ACS Nano (2014).



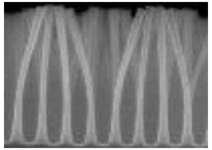
ATR-FTIR; Vrancken et al., Langmuir (2017).

3D structures with more surface area → interfacial phenomena

Capillary force induced pattern collapse



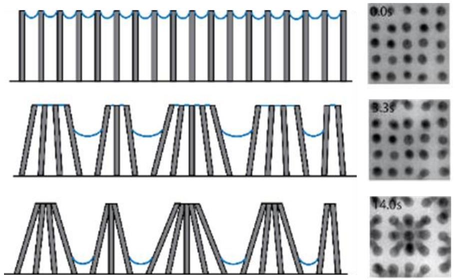
Low k: 45 nm L/S, AR~5



Si pillars AR~20

Si fins AR~10

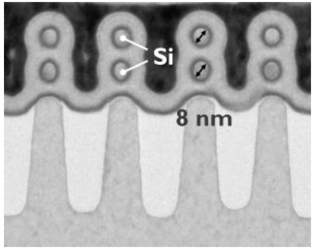
in-situ TEM observations



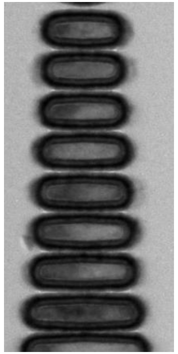
Xu et al., Mirsaidov, Semicon Korea (2017).

High surface to volume ratio → mechanical stability and structural integrity

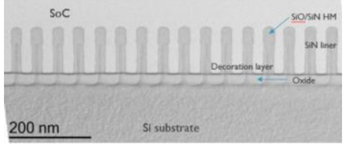
Selective etch requirements



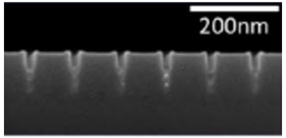
Si NW release VLSI 2016



Si NS release IFT 2017



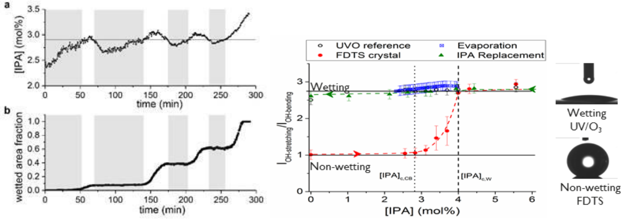
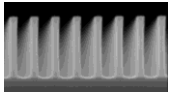
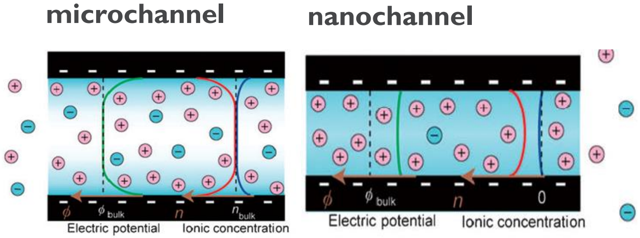
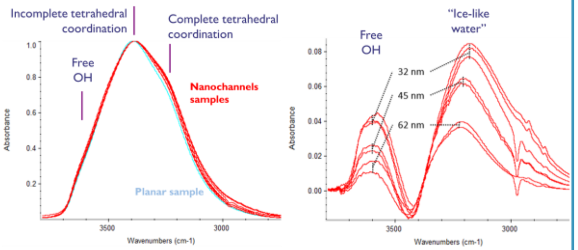
STI oxide recess, SiNx compatible



Cu recess to enable FSAV

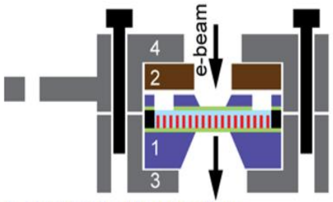
dimensional scaling → introduction of new device architectures and new selective etch requirements

KINETICS MAY VARY IN NANO-CONFINEMENT

Wetting	**electrical double layers**	**water structuring**
 (a) IPA concentration profile oscillating around the critical concentration and (b) the corresponding wetted area fraction as a function of time Wetting hysteresis 	 H. Daiguji, *Chem. Soc. Rev.* (2010).	 Vereecke, *ECIS* (2017).
Differentiation between Wenzel / Cassie-Baxter / Mixed wetting states	Overlap of electrical double layers (EDL) in nanochannel	Water confinement
In-situ study of wetting stability and hysteresis on initially non-wetting substrate	Depletion of ions with same charge as surface in channel: no electroneutrality	Formation of ice-like water in nanoconfined volumes
▪ Wetting hysteresis observed (Vrancken et al., Langmuir 2017).	▪ pH shift expected (D.Bottenus et al., Lab on Chip, 2009, 9, 219.) ▪ Depletion etchants (A. Okuyama et al., Solid State Phenom. 2015, 219, 115.)	▪ effect of water structuring on diffusivity of chemical species in nano-confined volumes expected

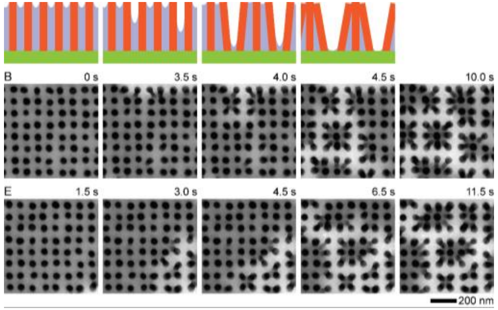
CAPILLARY FORCE INDUCED PATTERN COLLAPSE

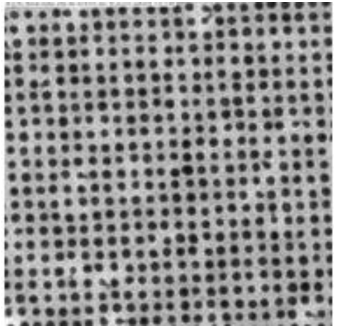
IN SITU CHARACTERIZATION OF DEWETTING AT NANOSCALE



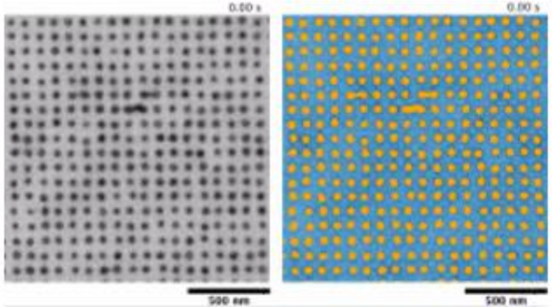
1: Liquid cell with nanopillars
2: PDMS gasket
3 & 4: Bottom and top pieces of custom brass retainer for TEM holder

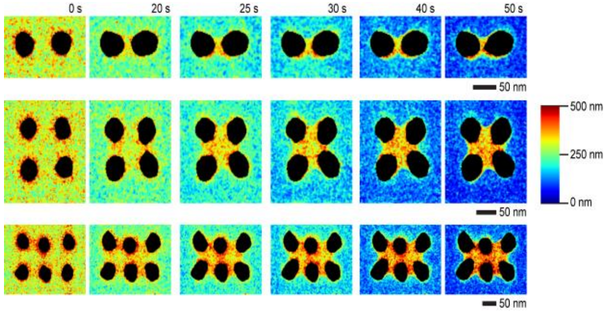
- Real-time visualization of pattern collapse with TEM in liquid cell.
- Polycrystalline Si nanopillars, height ≈ 450 nm.
- Formation of clusters due to capillary instabilities.





- During drying the water film becomes unstable, and water is drained gradually towards bended nanopillars islands.





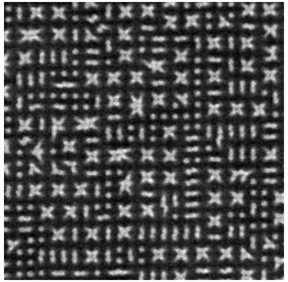
PATTERN COLLAPSE/STICTION FREE DRYING

IPA dry

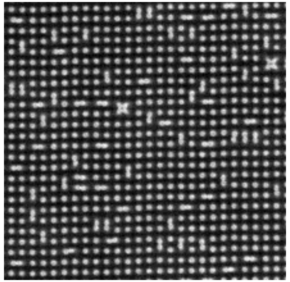
- Replace water by low surface tension (γ) solvents to reduce capillary force;
- Improve evaporation rate (gas flow and heat)
- Improve on IPA quality

Si nanopillars with native oxide

DIW (γ=0.072 N/m)



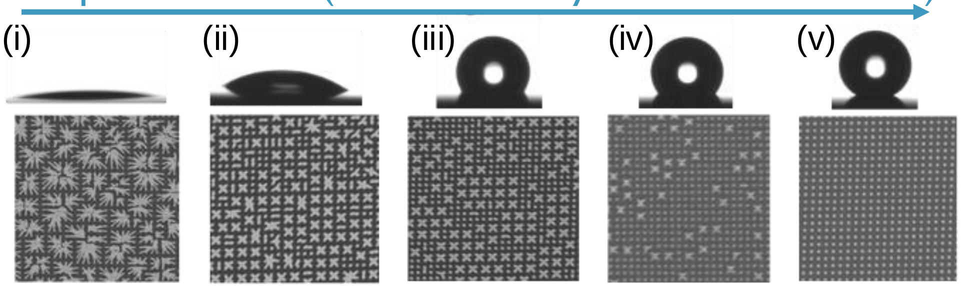
IPA (γ=0.022 N/m)



Surface functionalizing chemistry (SFC)

- Reduce capillary force by increasing contact angles (θ) of rinsing liquids;
- Reduce surface adhesion force, more relevant when IPA dry is used after SFC;
- Further reduction capillary force: towards sublimation drying

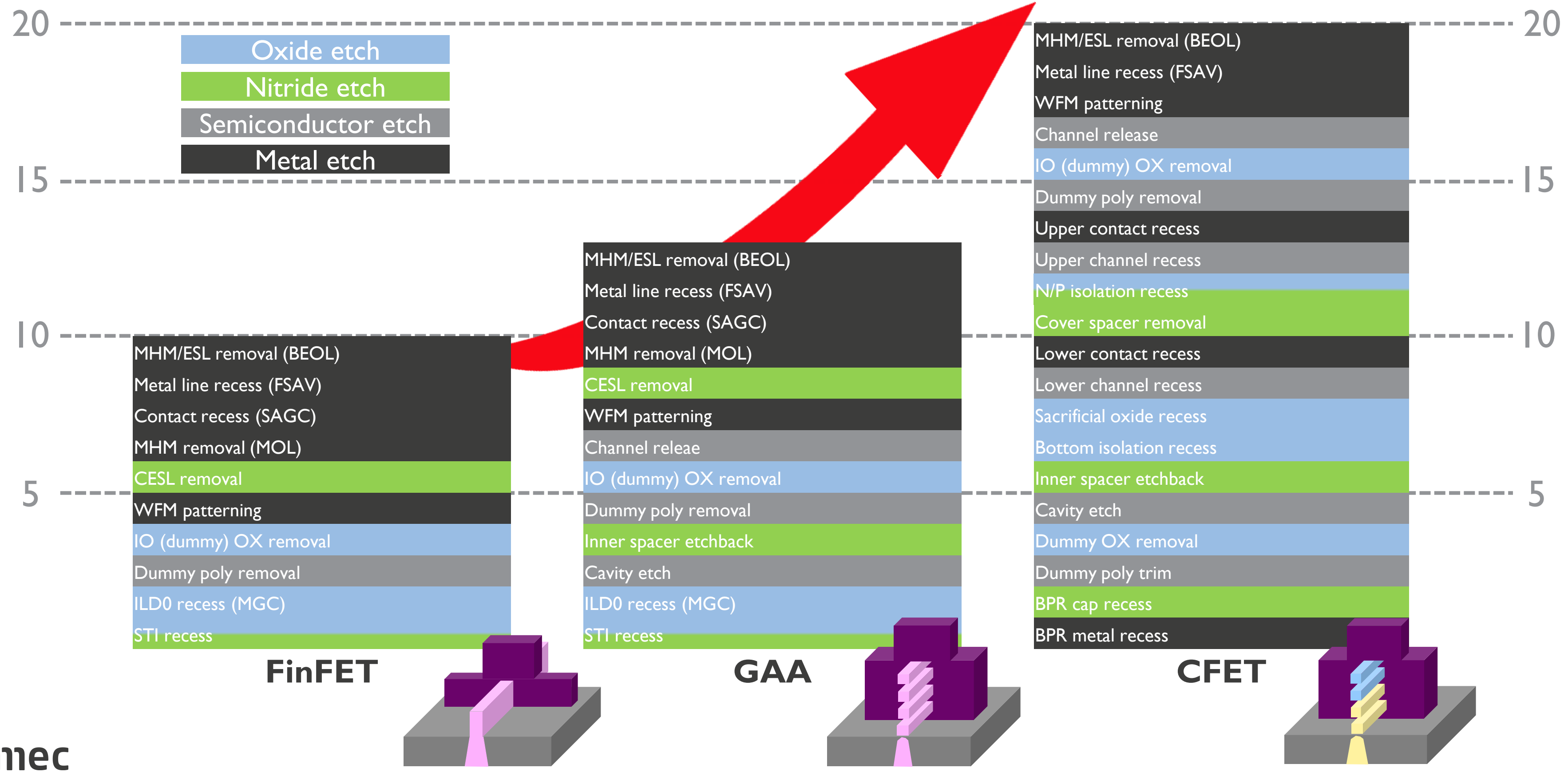
Increase surface hydrophobicity reduces pattern collapse in **water** (not necessarily for other solvents!)



SELECTIVE ETCH REQUIREMENTS

SELECTIVE/ISOTROPIC ETCH OPPORTUNITIES (WET/DRY)

FINFET → GAA → CFET



Oxide etch
Nitride etch
Semiconductor etch
Metal etch

FinFET

- MHM/ESL removal (BEOL)
- Metal line recess (FSAV)
- Contact recess (SAGC)
- MHM removal (MOL)
- CESL removal
- WFM patterning
- IO (dummy) OX removal
- Dummy poly removal
- ILD0 recess (MGC)
- STI recess

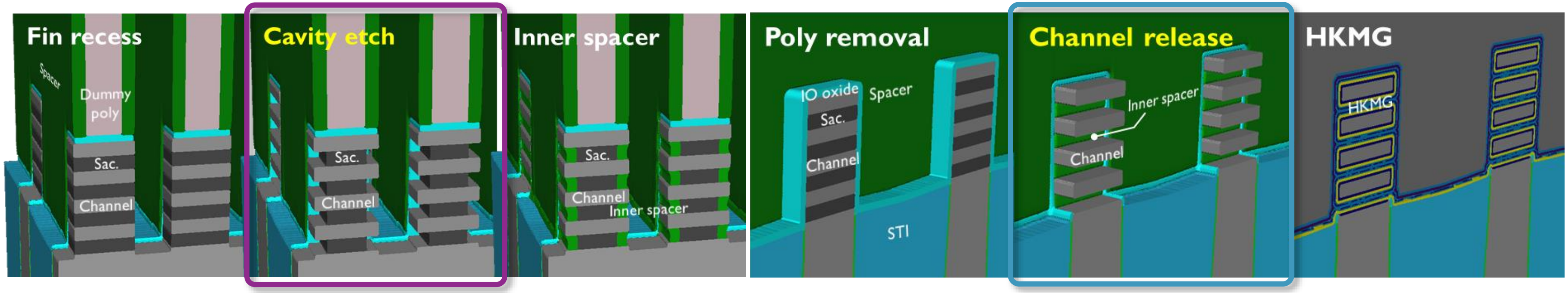
GAA

- MHM/ESL removal (BEOL)
- Metal line recess (FSAV)
- Contact recess (SAGC)
- MHM removal (MOL)
- CESL removal
- WFM patterning
- Channel releae
- IO (dummy) OX removal
- Dummy poly removal
- Inner spacer etchback
- Cavity etch
- ILD0 recess (MGC)
- STI recess

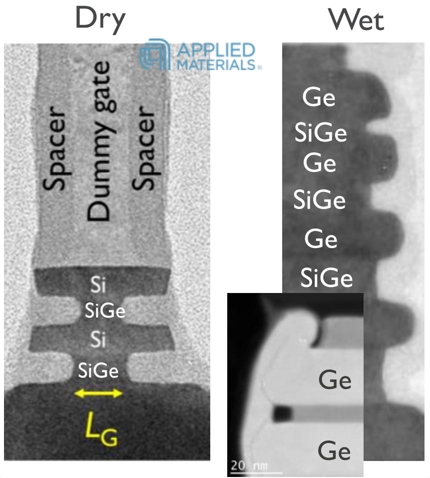
CFET

- MHM/ESL removal (BEOL)
- Metal line recess (FSAV)
- WFM patterning
- Channel release
- IO (dummy) OX removal
- Dummy poly removal
- Upper contact recess
- Upper channel recess
- N/P isolation recess
- Cover spacer removal
- Lower contact recess
- Lower channel recess
- Sacrificial oxide recess
- Bottom isolation recess
- Inner spacer etchback
- Cavity etch
- Dummy OX removal
- Dummy poly trim
- BPR cap recess
- BPR metal recess

SEMICONDUCTOR ETCH: GAA SELECTIVE ETCH REQUIREMENTS

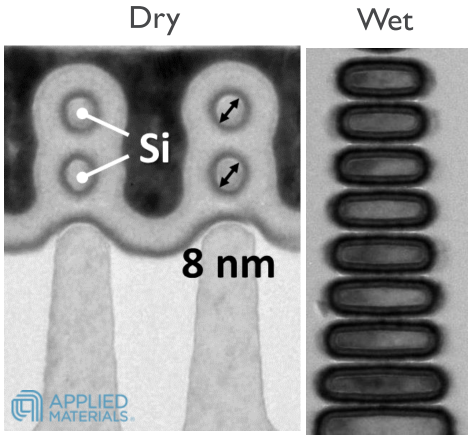


Cavity etch



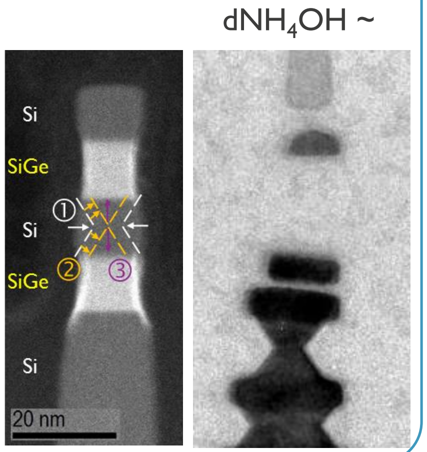
imec Mertens et al., *IEDM* (2017).

Si NW/NS release



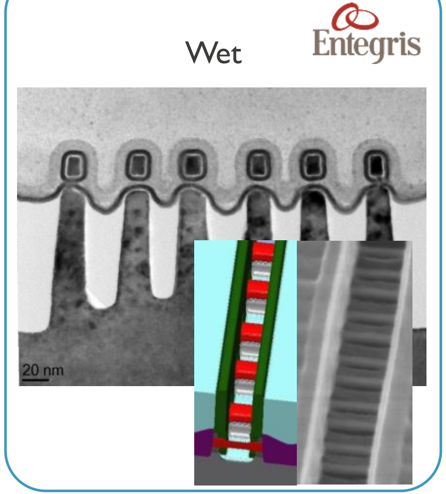
Mertens et al., *VLSI* (2016). ITF (2017)

SiGe NW release



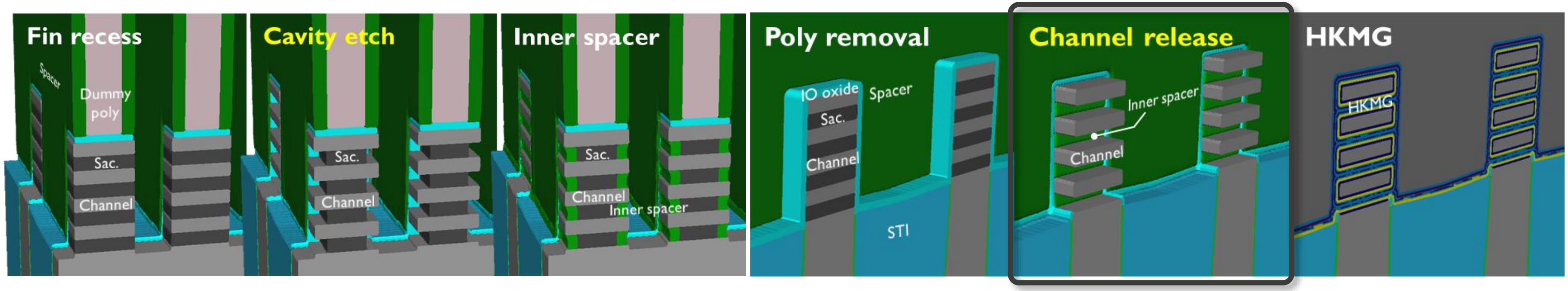
Wostyn et al., *ECS* (2015).

Ge NW release



Sebaai, *UCPSS* (2016), Witters, VLSI2017.

SEMICONDUCTOR ETCH: GAA SELECTIVE ETCH REQUIREMENTS



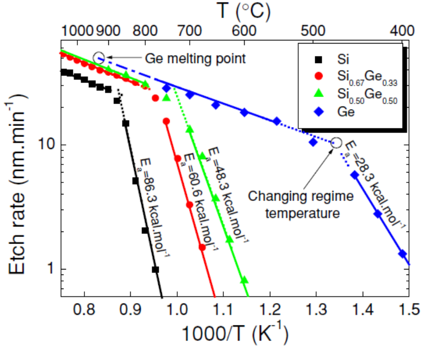
HCl (gas)

FORMULATED MIXTURE (wet)

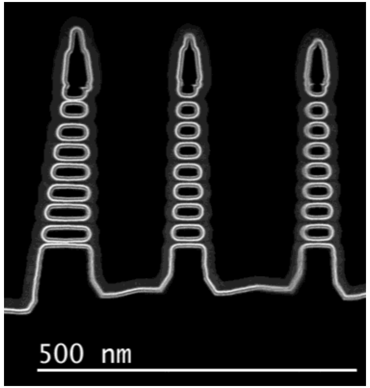
For both HCl (g) and formulated mixture, selectivity increases strongly with increasing Ge%.

Anisotropic selective etch. Process time ~ hour

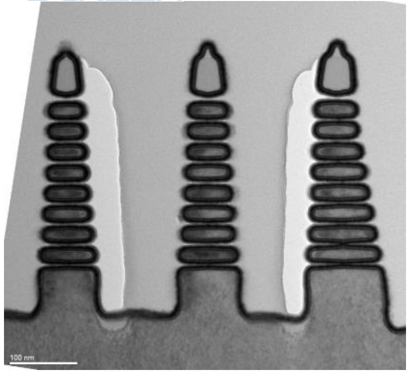
Isotropic selective etch. Process time ~ min

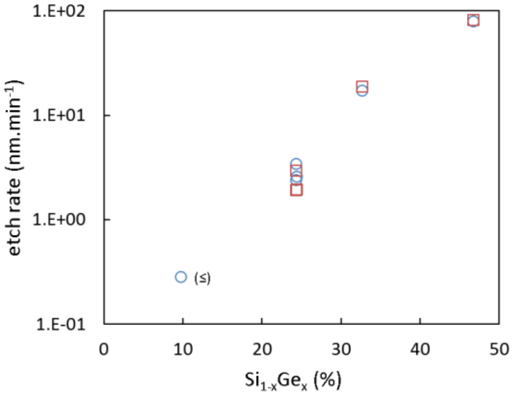


Bogumilowicz et al. Semicond. Sci. Technol. 20 (2005) 127.



SCREEN

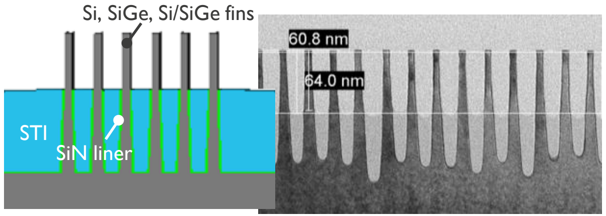




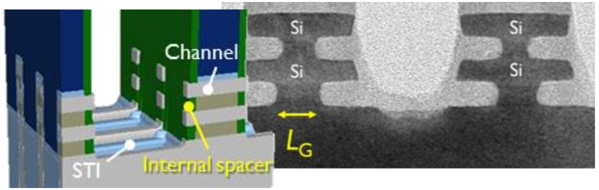
DIELECTRIC ETCH

FinFET/GAA/CFET/VFET

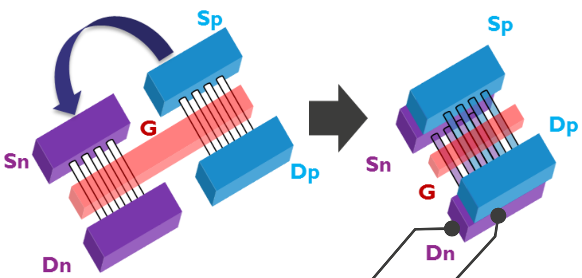
Si/SiGe, GAA Fin reveal (SiO$_2$/SiN etch)



GAA inner spacer EB [SiN(OC) etch]



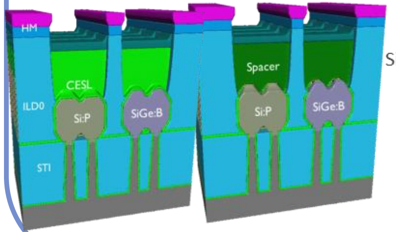
Isolation recess (SiO$_2$/SiN etch)



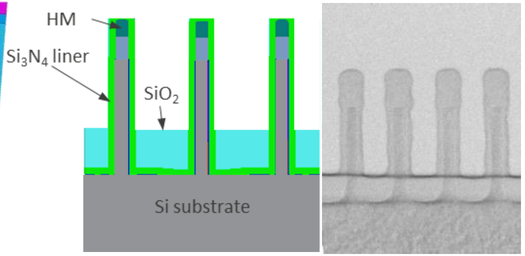
Bottom isolation recess (SiO$_2$ etch)

N/P isolation recess (SiO$_2$/SiN etch)

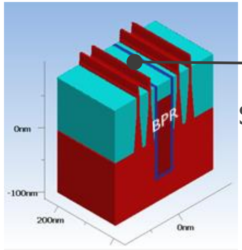
CESL removal (SiN etch)



Oxide recess selective to SiNx



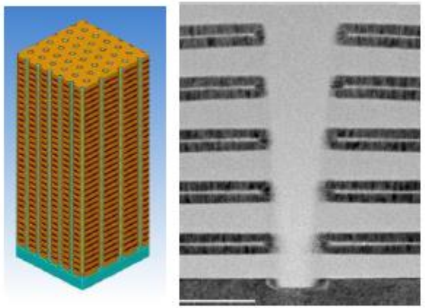
BPR isolation recess



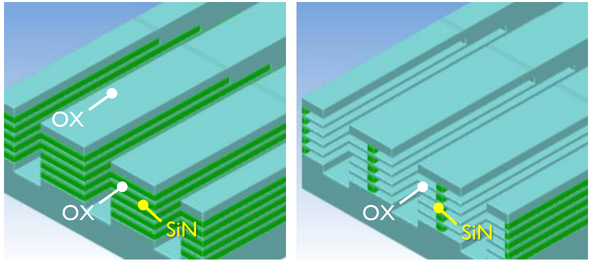
SiN etch

Memory

Selective SiNx removal for 3D-NAND fabrication



3D SCM dummy gate recess



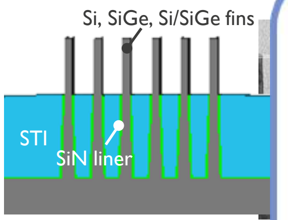
SiN recess

Mertens et al., *IEDM* (2017).
Pacco et al., *SPCC* (2018).

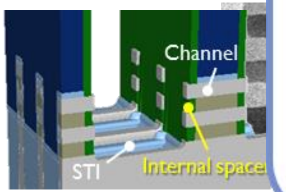
DIELECTRIC ETCH

FinFET/GAA/CFET/VFET

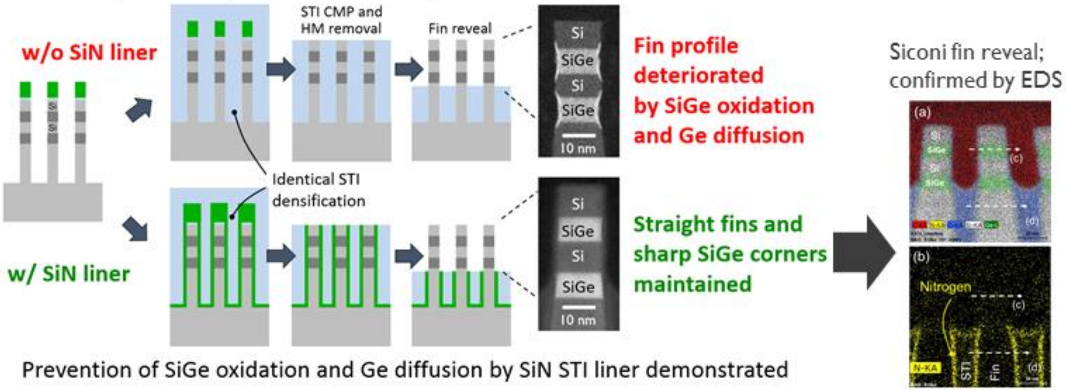
Si/SiGe, GAA Fin r



GAA inner spac

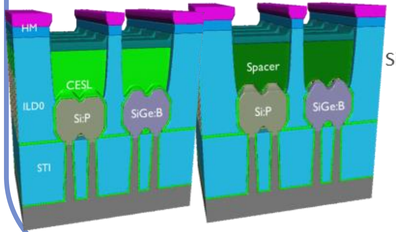


SiGe/Si fin protection by SiN STI liner

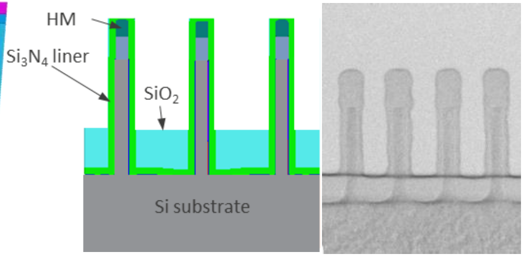


Prevention of SiGe oxidation and Ge diffusion by SiN STI liner demonstrated

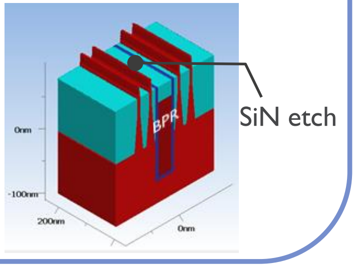
CESL removal (SiN etch)



Oxide recess selective to SiNx

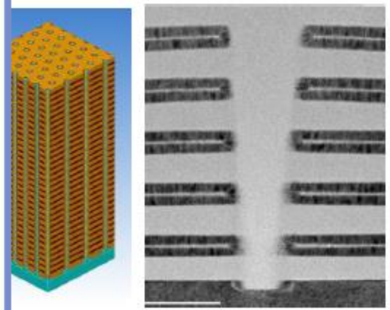


BPR isolation recess

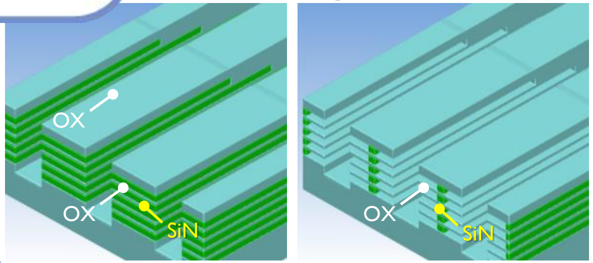


Memory

ctive SiNx removal for NAND fabrication



SCM dummy gate recess



SiN recess

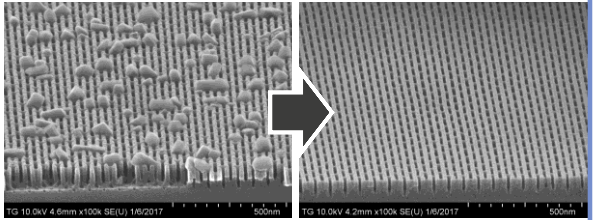
Mertens et al., *IEDM* (2017).
Pacco et al., *SPCC* (2018).

METAL ETCH

Selective removal

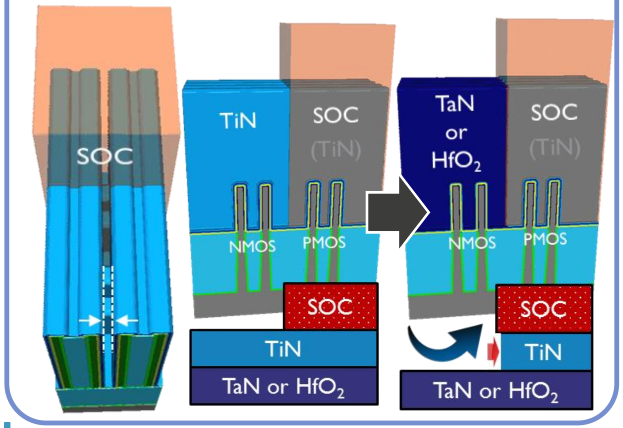
IC: MHM/ESL removal

TiN-HM (and TiFx residue) removal



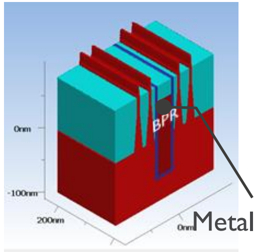
RMG WFM patterning

WFM removal in limited spaces



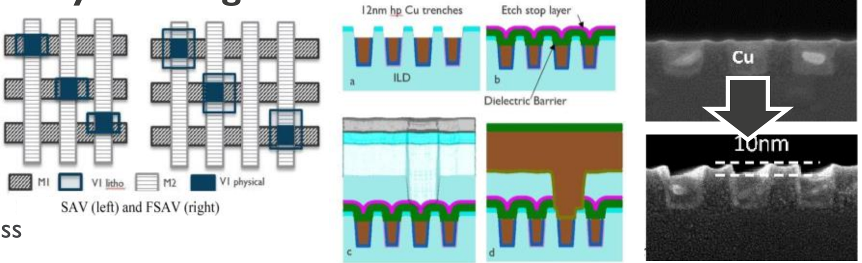
Controlled metal recess: BPR, FSAV, SAGC, CMR

BPR metal recess



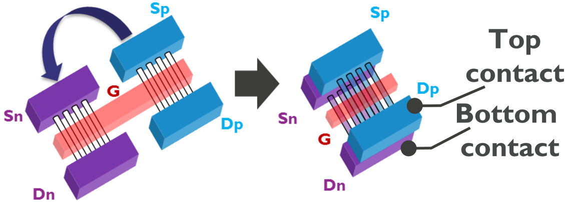
Metal recess

Fully Self Aligned Via

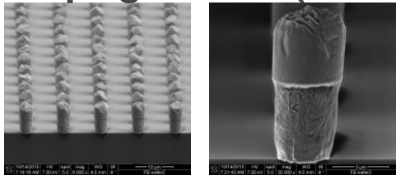


SAV (left) and FSAV (right)

CFET: contact metal rail

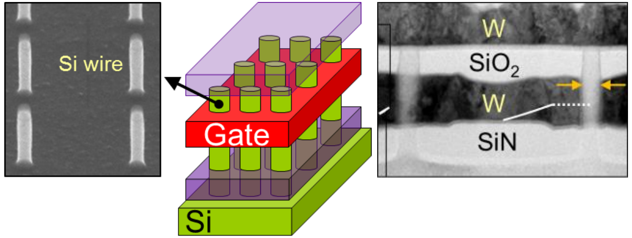


Bumping module (seed etch)

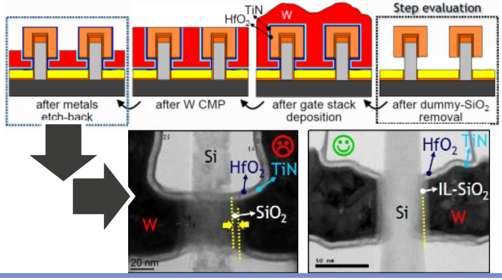


10 um pitch (CuNiSn bump)

Vertical GAA-NWFETs



RMG module VGAA-NWFETs



Oniki et al., *SPCC* (2018).

Veloso, ECS (2017); Murdoch, IEEE (2017).

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