

Semiconductor Manufacturing Technology

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Chapter 9

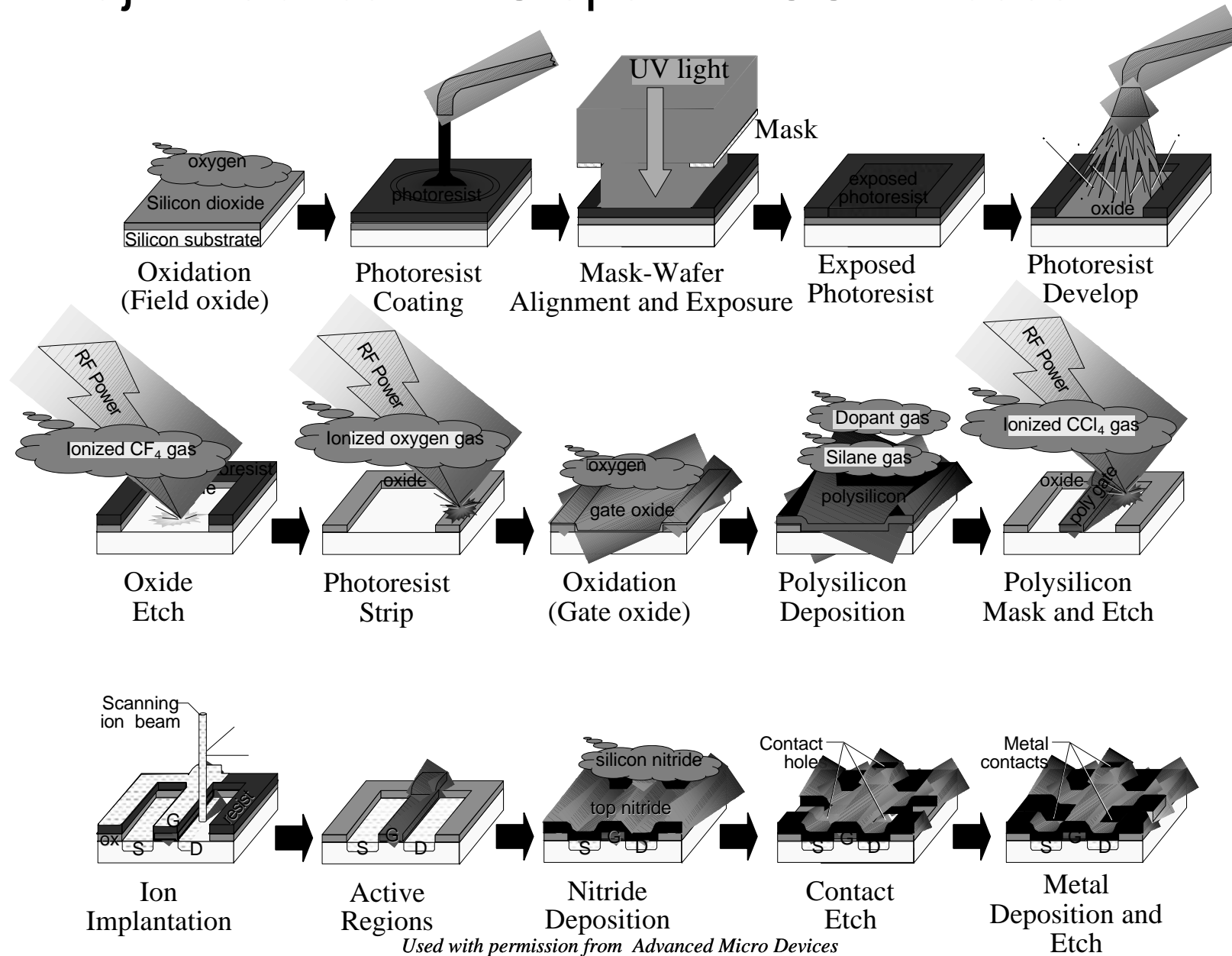
IC Fabrication Process Overview

Objectives

After studying the material in this chapter, you will be able to:

1. Draw a diagram showing how a typical wafer flows in a sub-micron CMOS IC fab.
2. Give an overview of the six major process areas and the sort/test area in the wafer fab.
3. For each of the 14 CMOS manufacturing steps, describe its primary purpose.
4. Discuss the key process and equipment used in each CMOS manufacturing step.

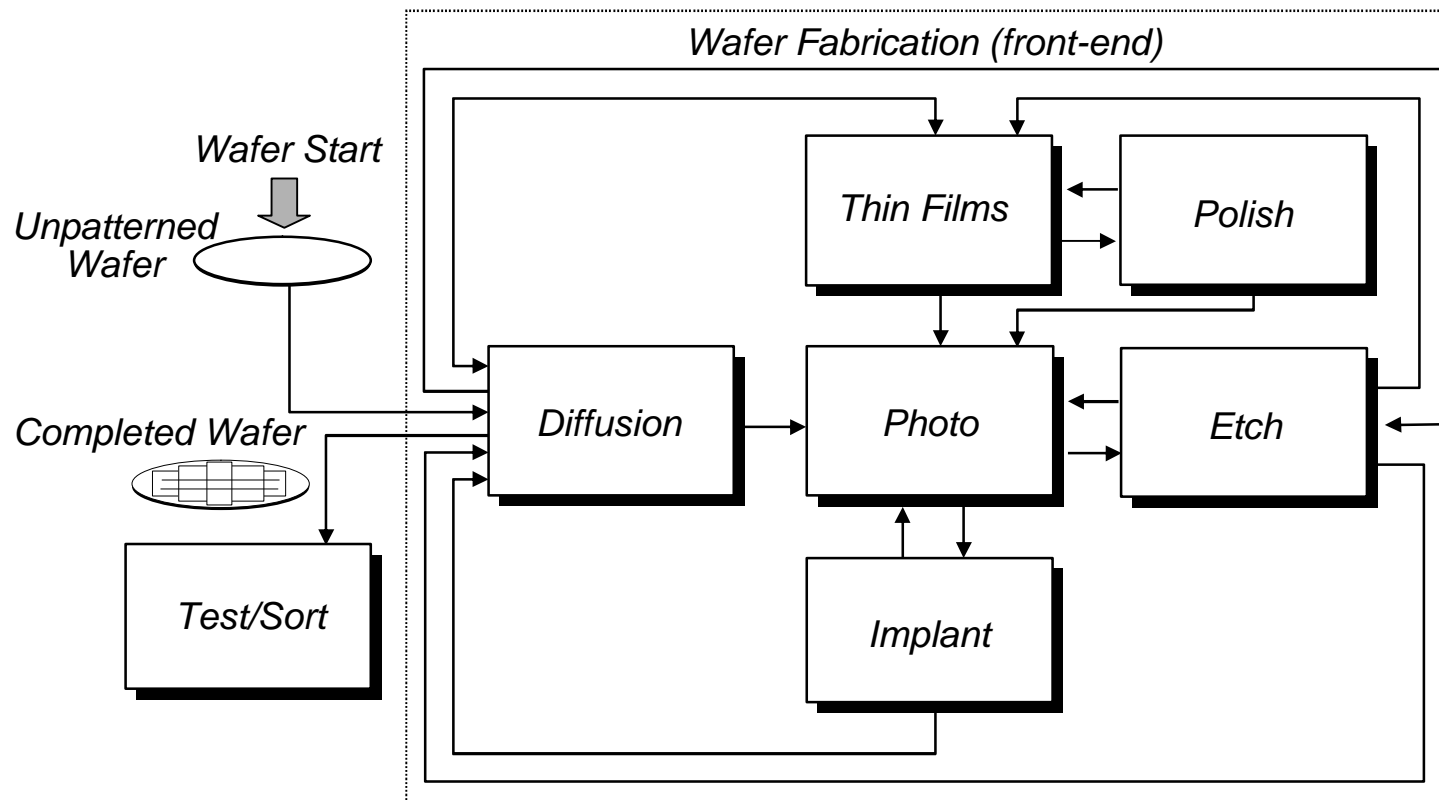
Major Fabrication Steps in MOS Process Flow



CMOS Process Flow

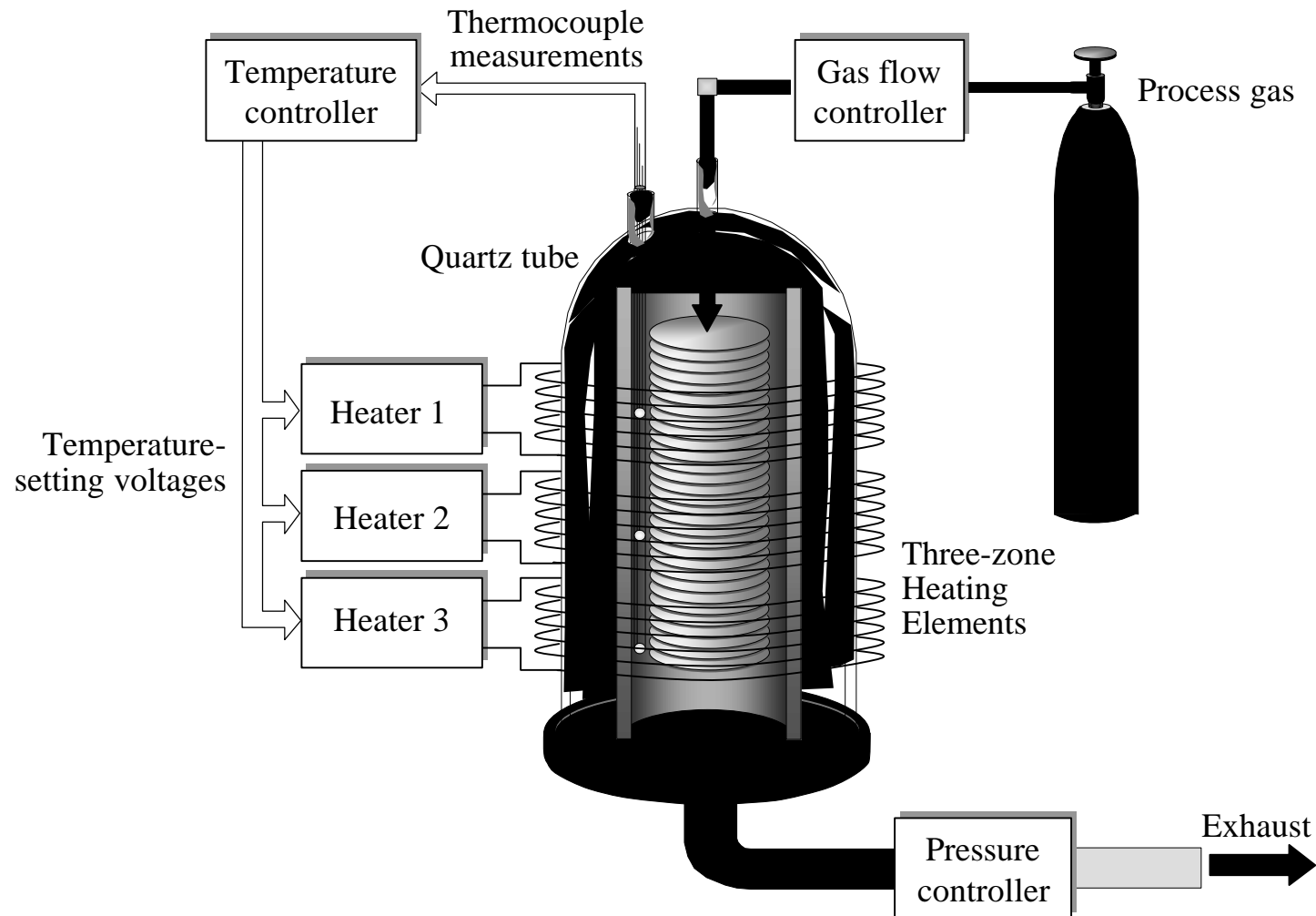
- Overview of Areas in a Wafer Fab
 - Diffusion
 - Photolithography
 - Etch
 - Ion Implant
 - Thin Films
 - Polish
- CMOS Manufacturing Steps
- Parametric Testing
- 6~8 weeks involve 350-step

Model of Typical Wafer Flow in a Sub-Micron CMOS IC Fab



6 major production areas

Diffusion: Simplified Schematic of High-Temperature Furnace



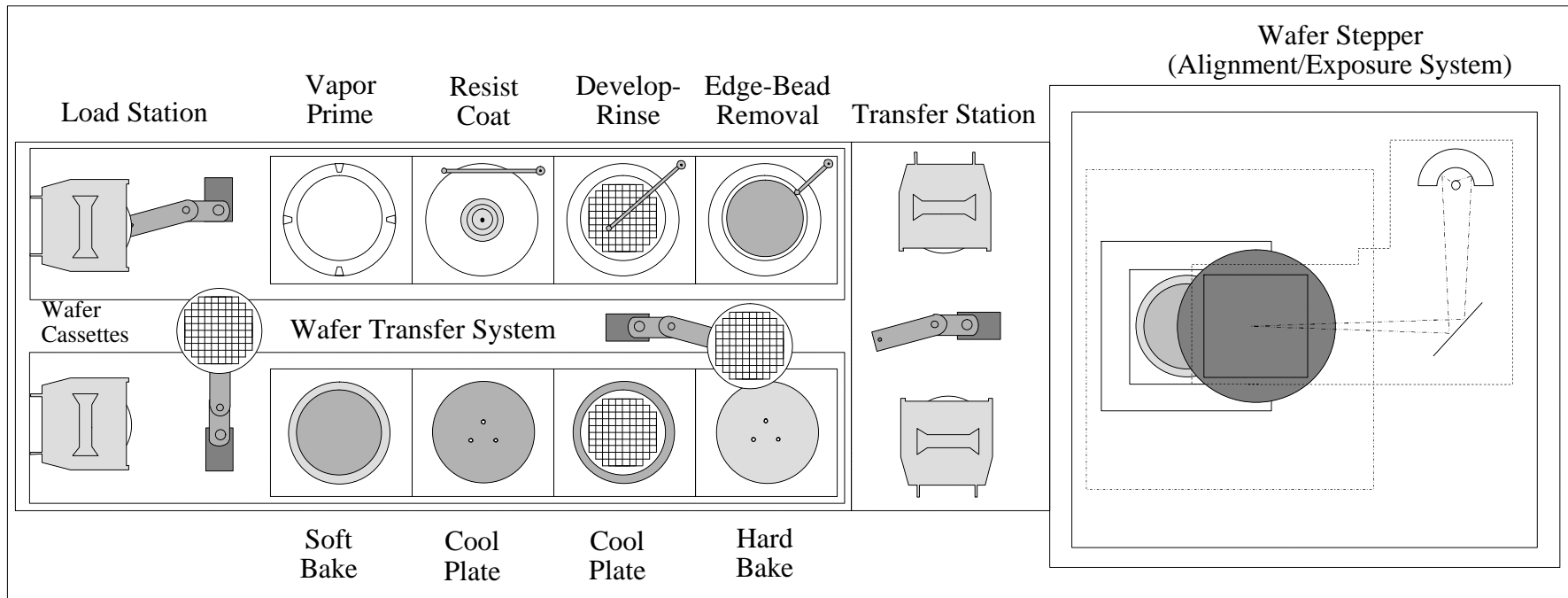
Can do : oxidation, diffusion, deposition, anneals, and alloy

Photolithography Bay in a Sub-micron Wafer Fab



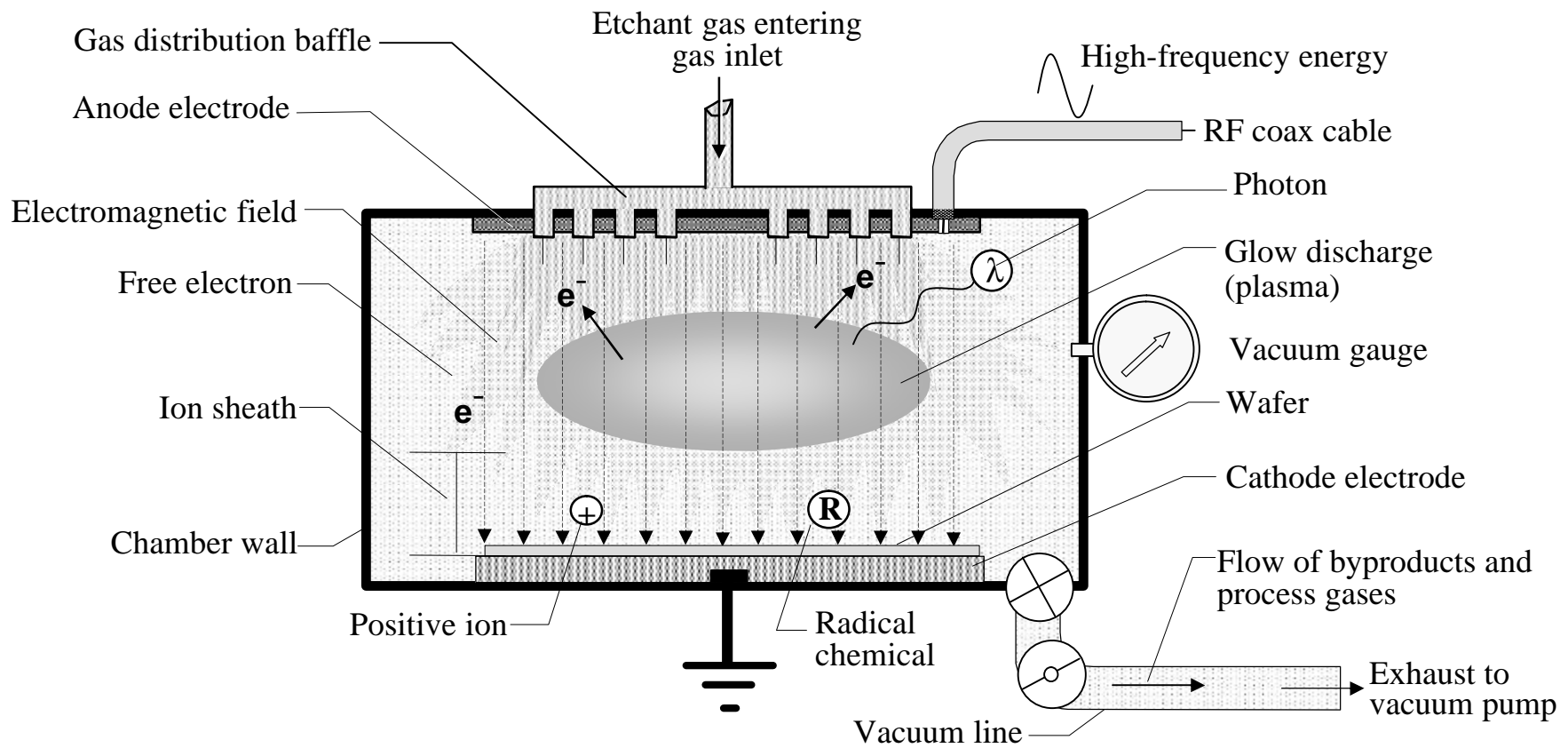
Yellow fluorescent: do not affect photoresist

Simplified Schematic of a Photolithography Processing Module

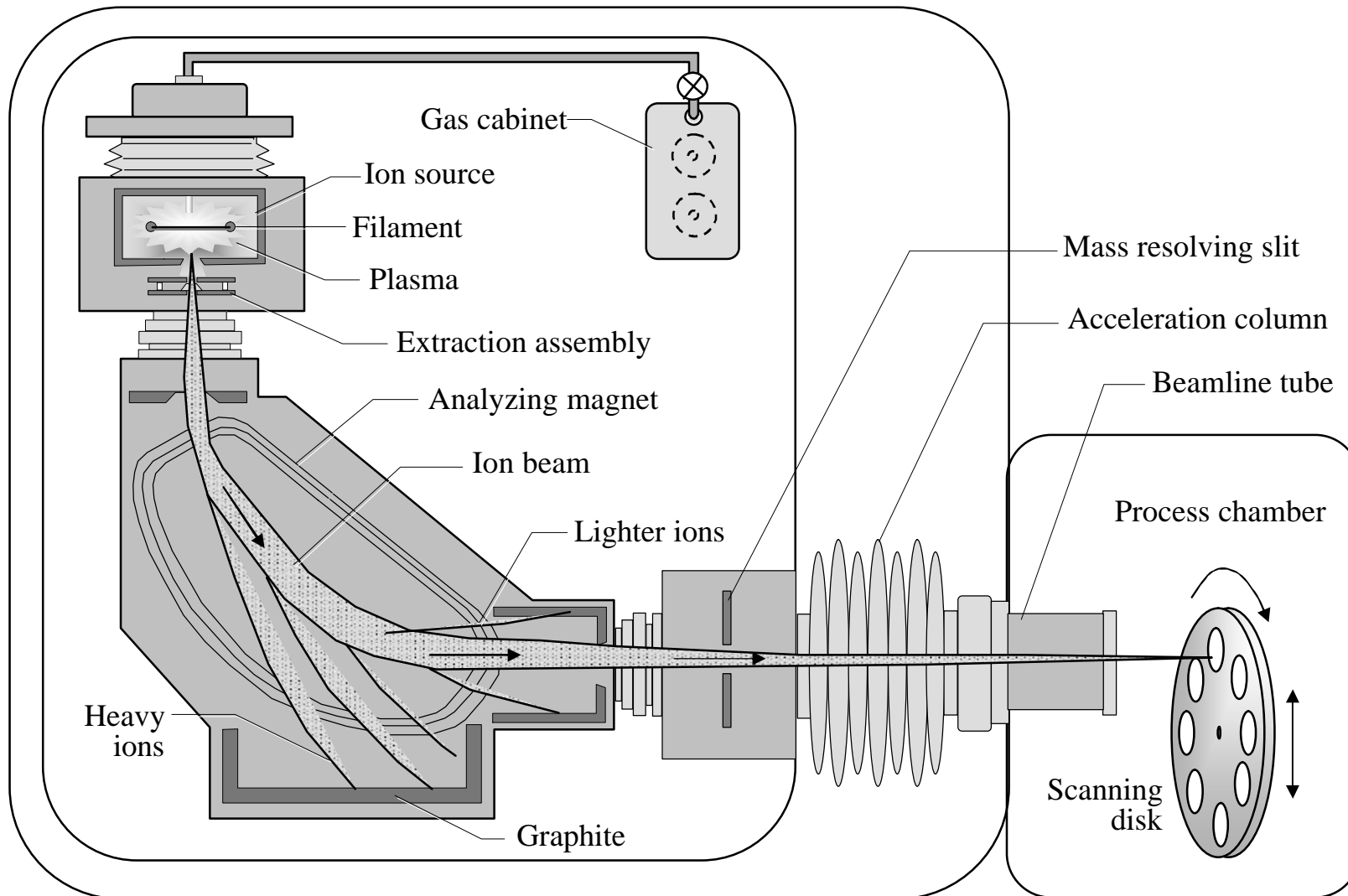


Note: wafers flow from photolithography into only two other areas: etch and ion implant

Simplified Schematic of Dry Plasma Etcher



Simplified Schematic of Ion Implanter

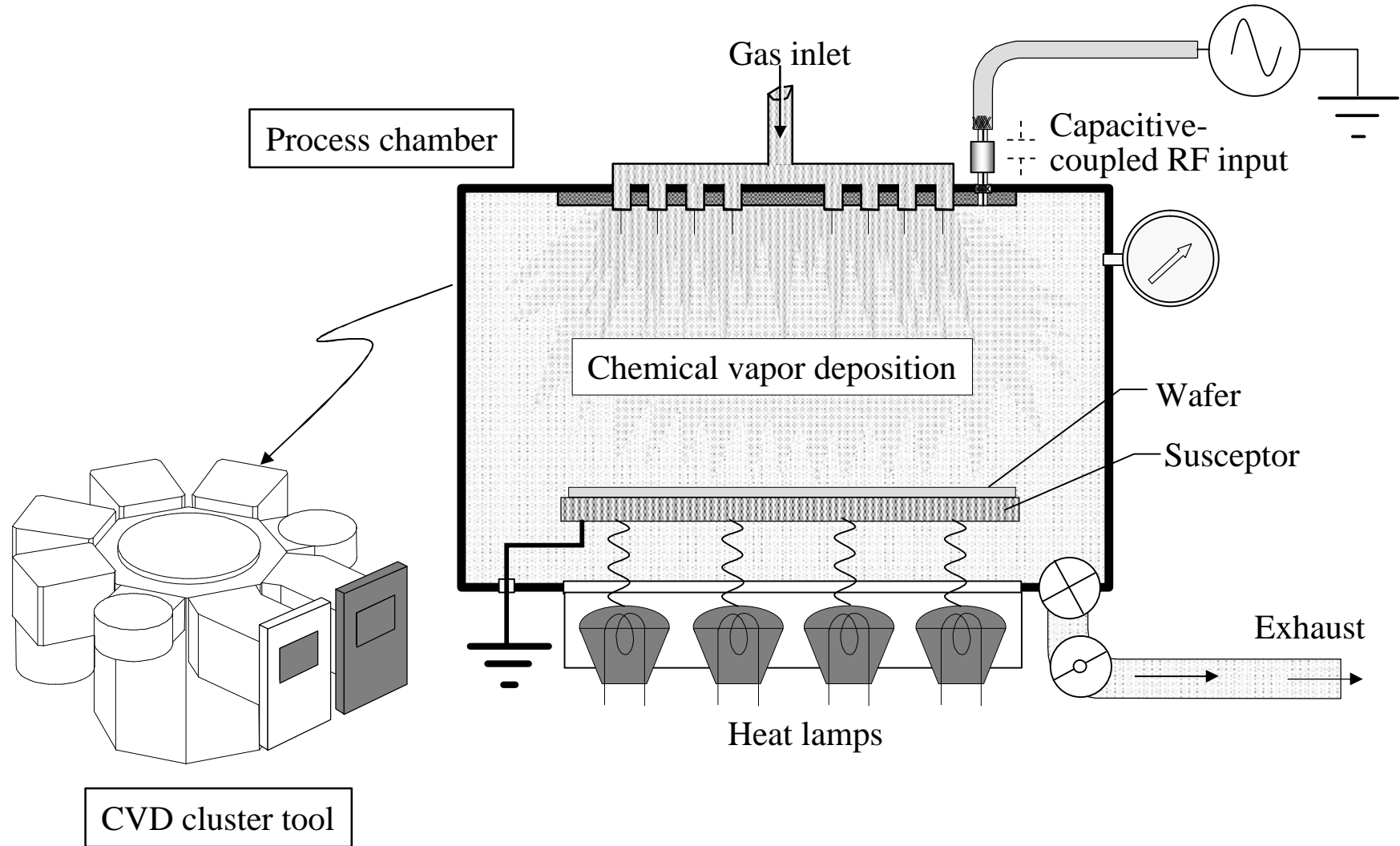


Thin Film Metallization Bay



Photo courtesy of Advanced Micro Devices

Simplified Schematics of CVD Processing System



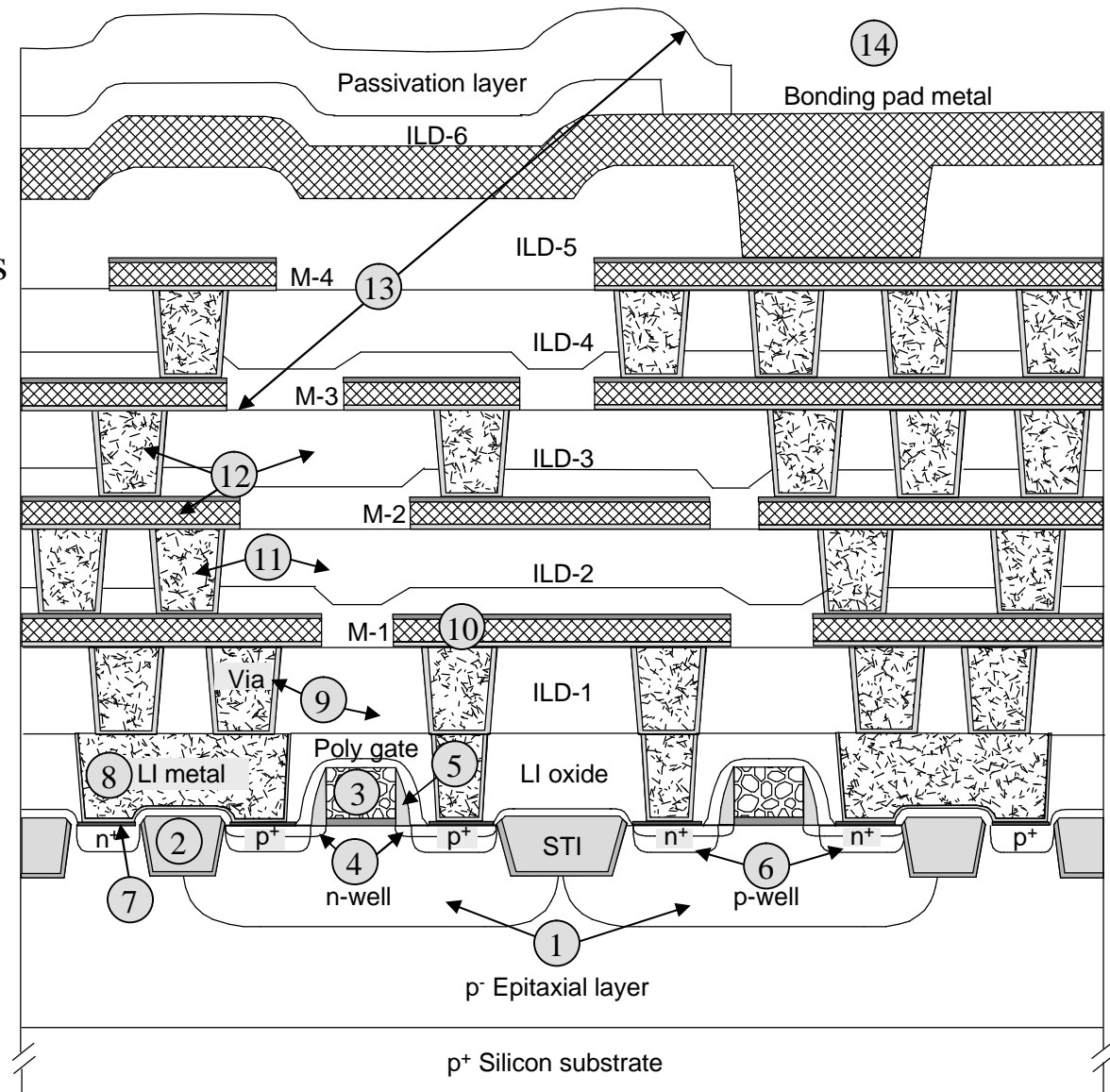
Polish Bay in a Sub-micron Wafer Fab



Photo courtesy of Advanced Micro Devices

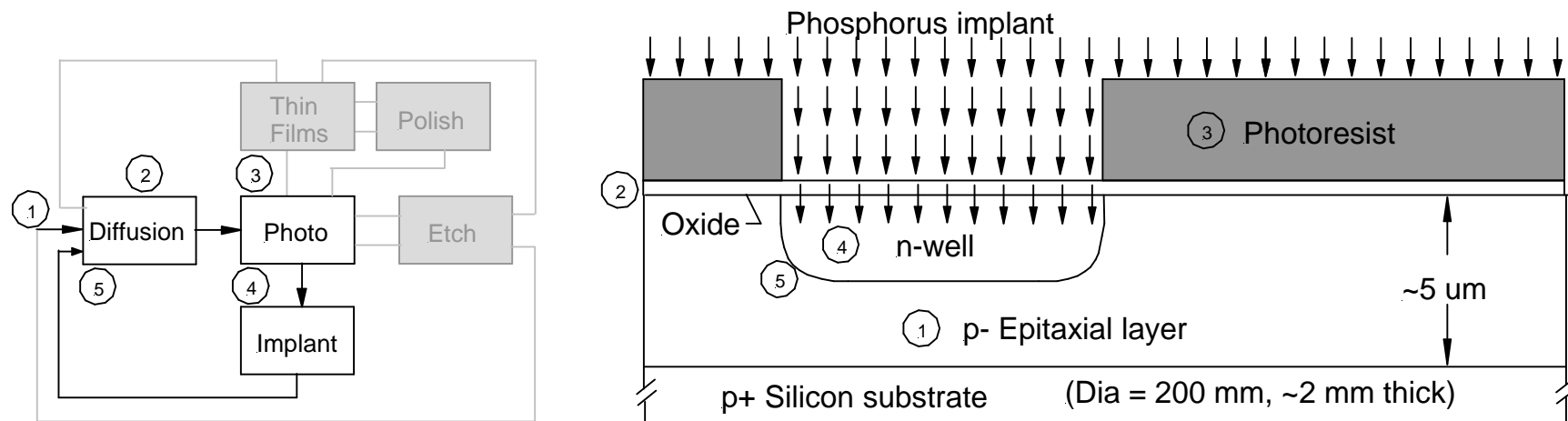
CMOS Manufacturing Steps

1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. First Metal Layer
11. Second ILD to Via-2
12. Second Metal Layer to Via-3
13. Metal-3 to Pad Etch
14. Parametric Testing

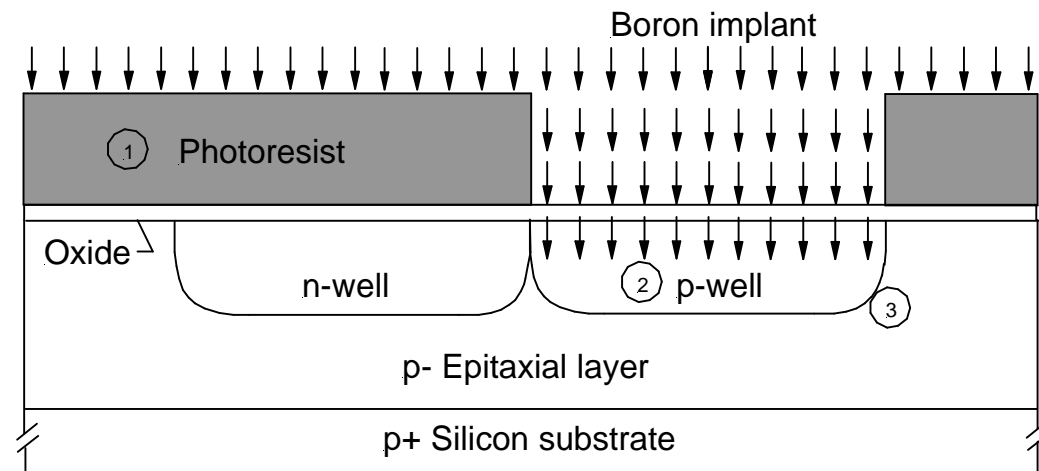
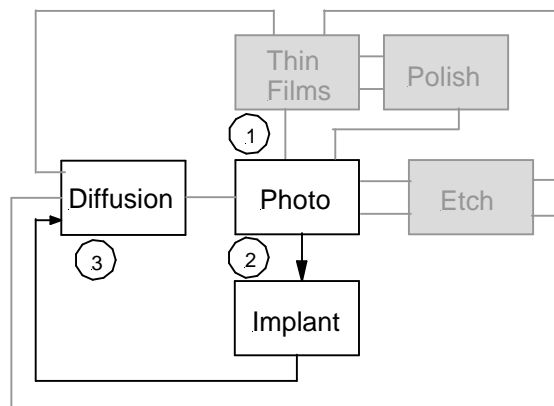


n-well Formation

- Epitaxial layer : improved quality and fewer defect
- In step 2, initial oxide: (1) protects epi layer from contamination, (2) prevents excessive damage to ion/implantation, (3) control the depth of the dopant during implantation
- In step 5, anneal: (1) drive-in, (2) repair damage, (3) activation



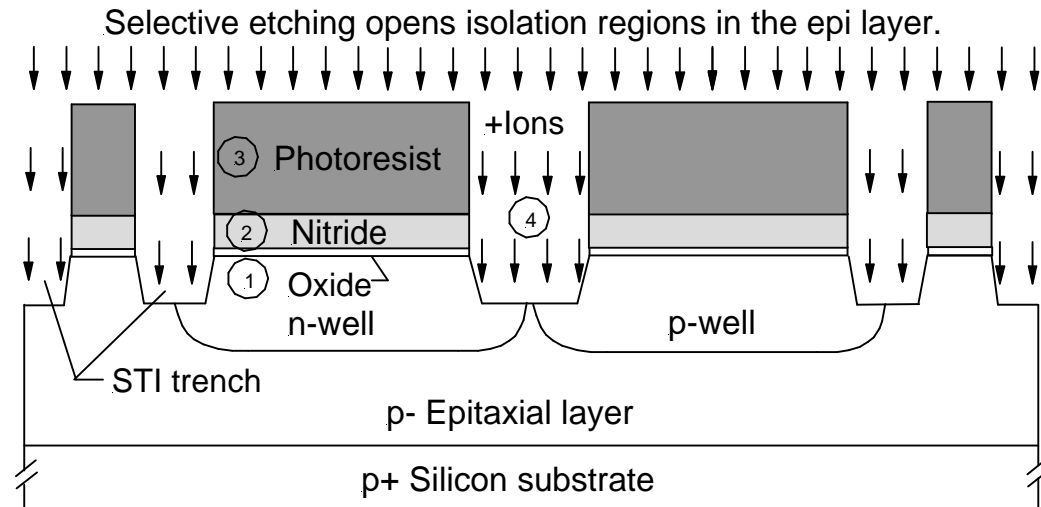
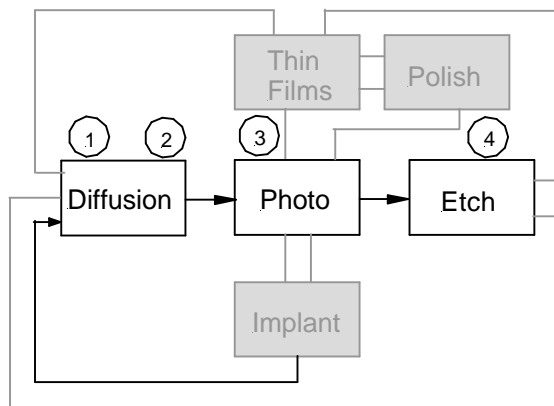
p-well Formation



STI Trench Etch

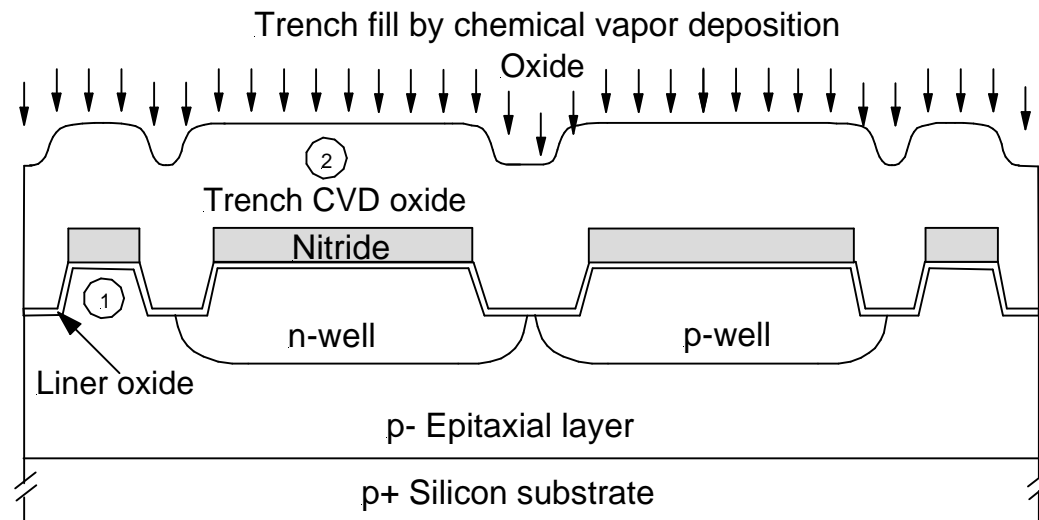
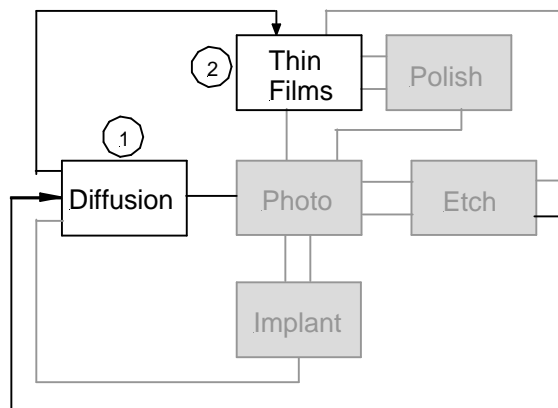
STI: shallow trench isolation

1. Barrier oxide: a new oxide
2. Nitride: (1) protect active region, (2) stop layer during CMP
3. 3rd mask
4. STI etching



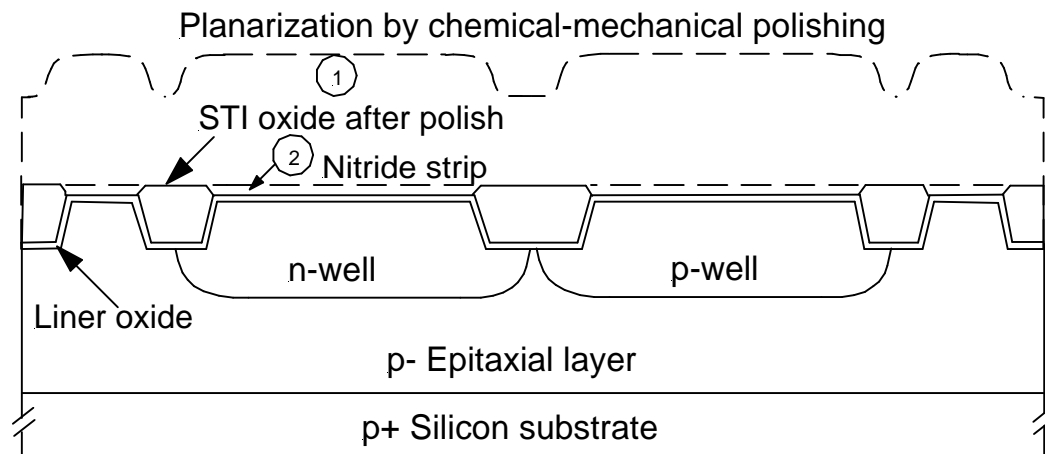
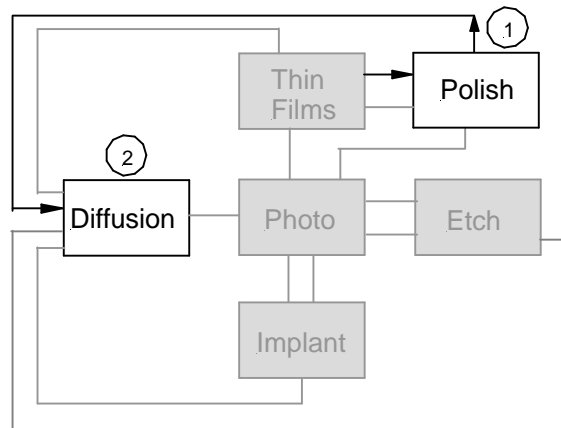
STI Oxide Fill

1. **Liner oxide to improve the interface between the silicon and trench CVD oxide**
2. **CVD oxide deposition**



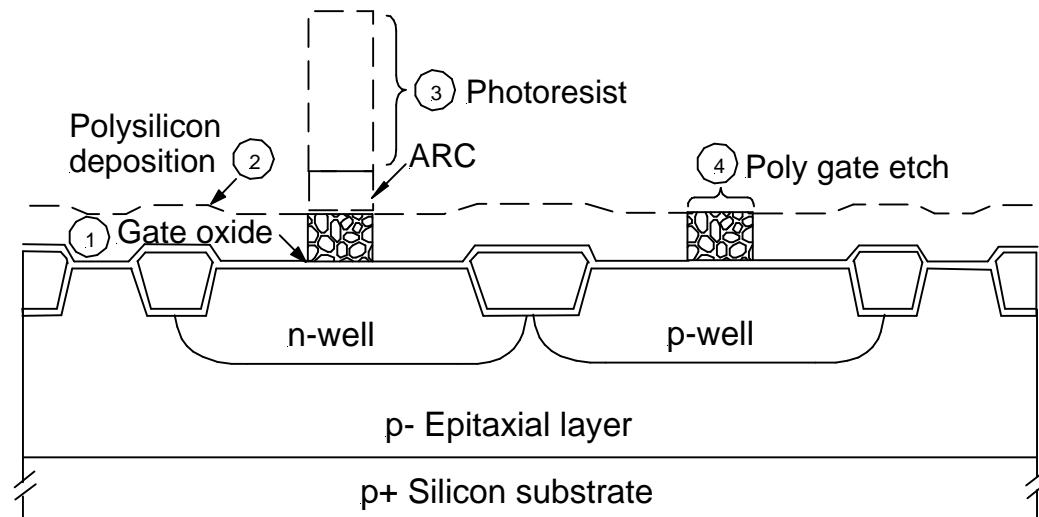
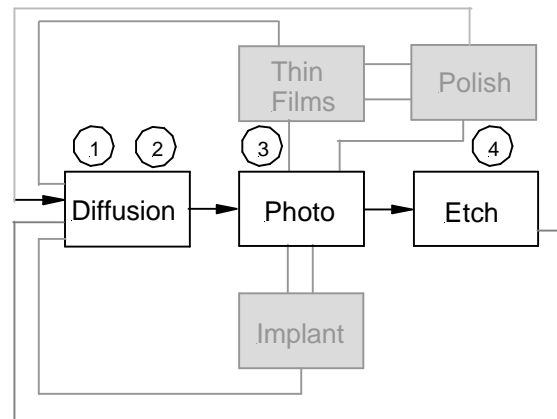
STI Formation

1. Trench oxide polish (CMP): nitride as the CMP stop layer since nitride is harder than oxide
2. Nitride strip: hot phosphoric acid



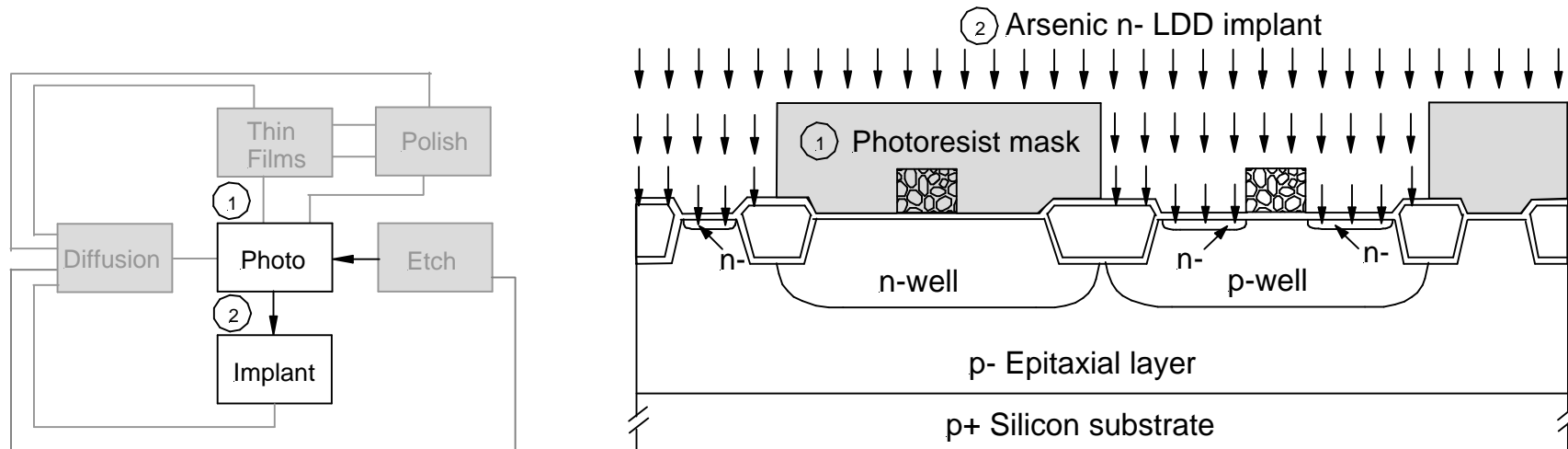
Poly Gate Structure Process

1. **Oxide thickness 1.5 ~ 5.0 nm is thermal grown**
2. **Poly-Si ~ 300 nm is doped and deposited in LPCVD using SiH₄**
3. **Need Antireflective coating (ARC), very critical**
4. **The most critical etching step in dry etching**



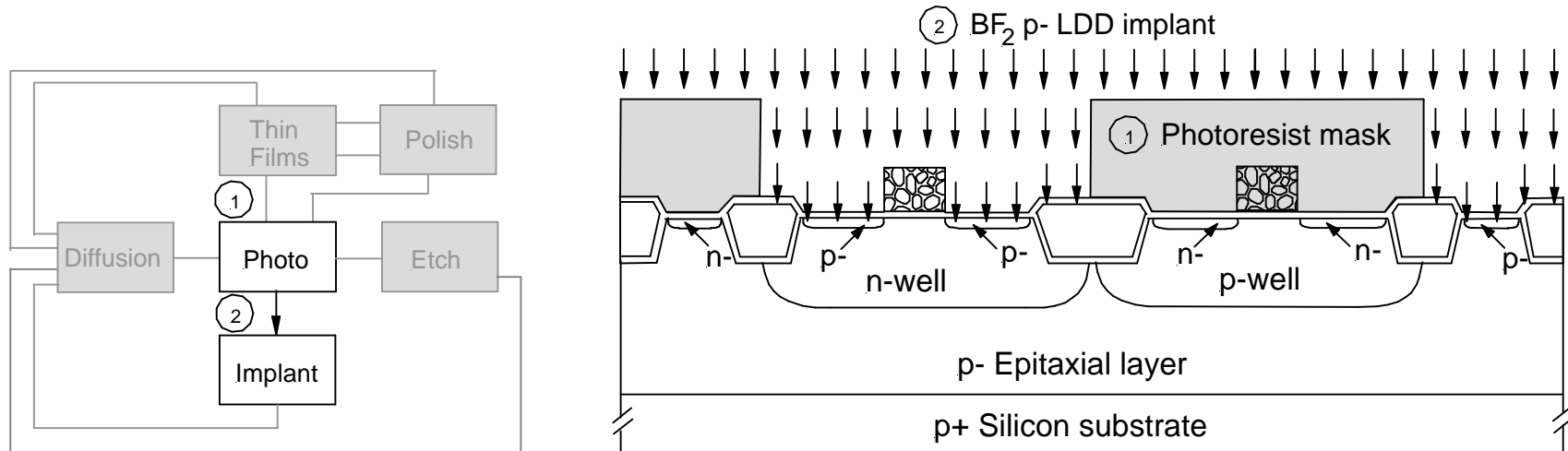
n⁻ LDD Implant

1. LDD: lightly doped drain to reduce S/D leakage
2. Large mass implant (BF₂, instead of B, As instead of P) and amorphous surface helps maintain a shallow junction
3. 5th mask



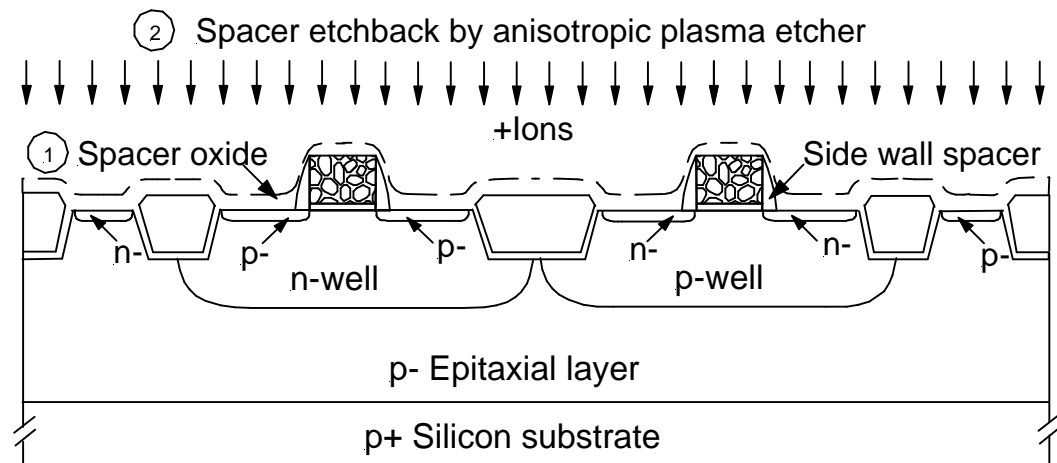
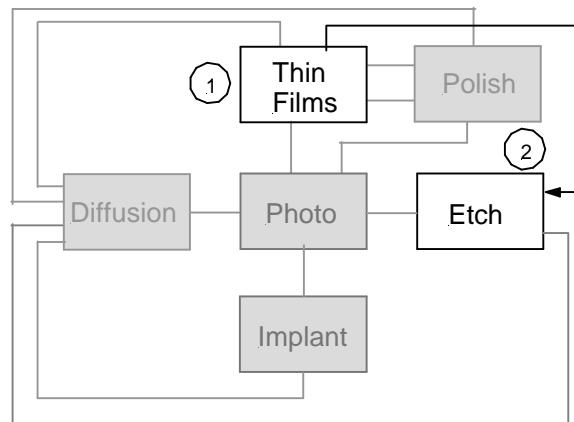
p^- LDD Implant

1. 6th mask
2. In modern device, high doped drain is used to reduce series resistance. It called S/D extension



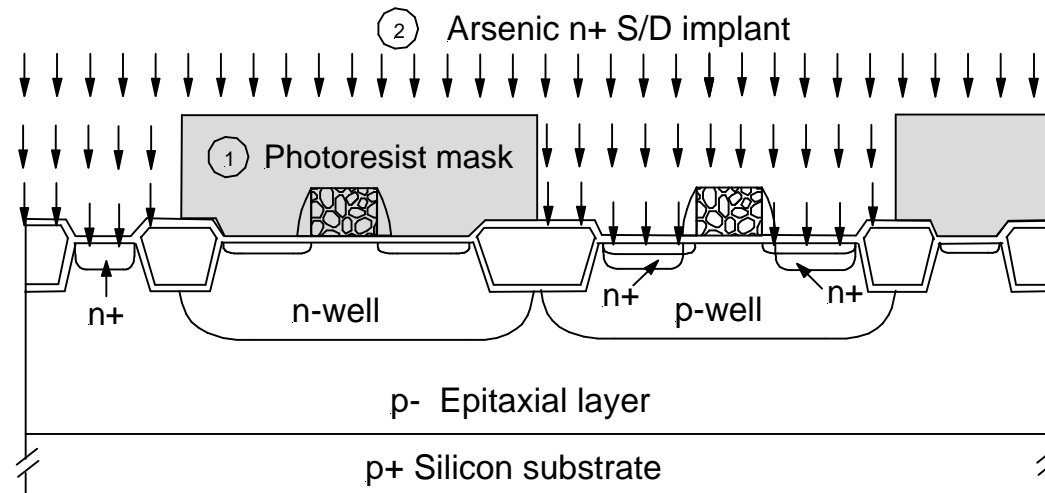
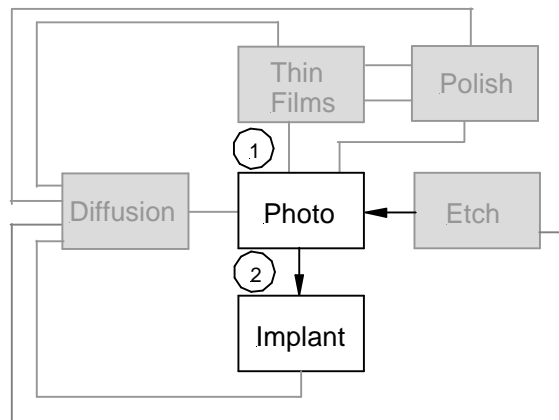
Side Wall Spacer Formation

Spacer is used to prevent higher S/D implant from penetrating too close to the channel



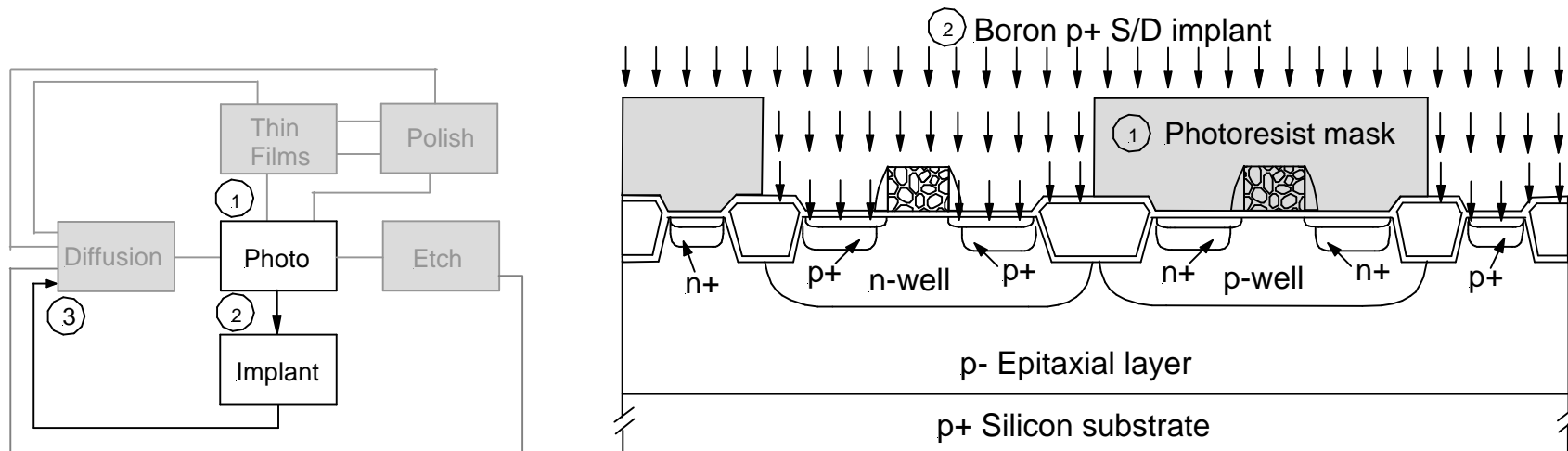
n^+ Source/Drain Implant

1. Energy is high than LDD I/I, the junction is deep
2. 7th mask



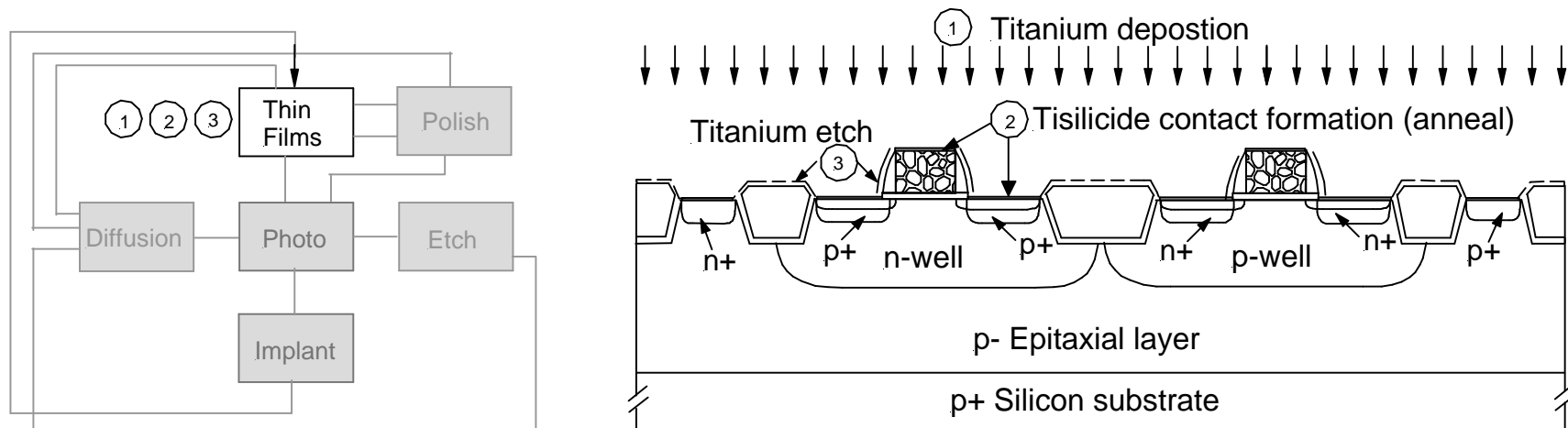
p⁺ Source/Drain Implant

1. 8th mask
2. Using rapid thermal anneal (RTA) to prevent dopant spreading and to control diffusion of dopant



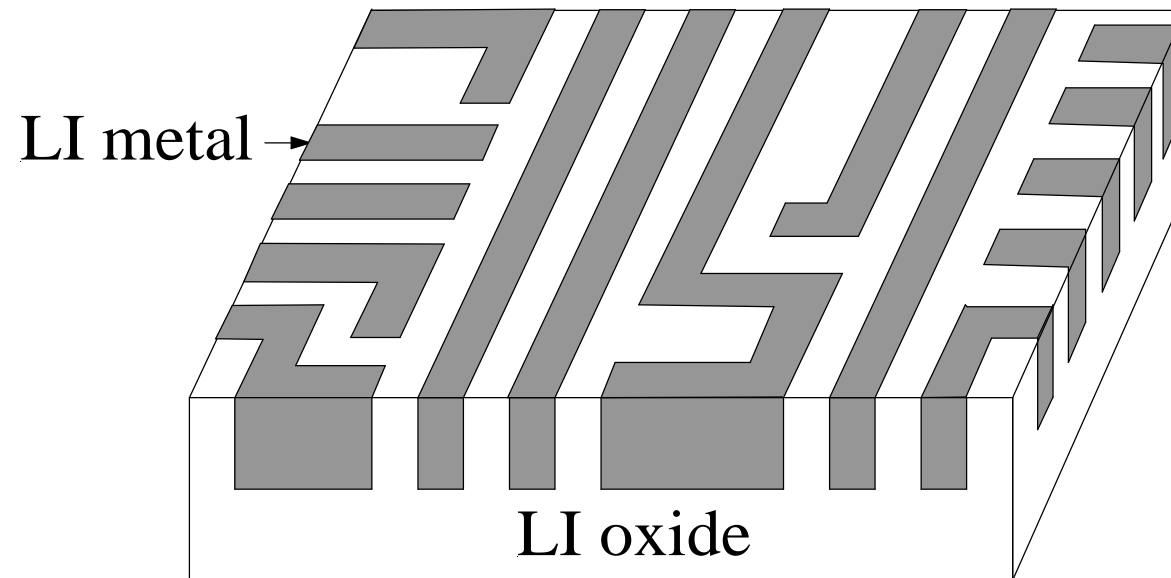
Contact Formation

1. Titanium (Ti) is a good choice for metal contact due to low resistivity and good adhesion
2. No mask needed, called **self-align**
3. Using Ar to **sputtering** metal
4. Anneal to form TiSi_2 , **silicide**
5. Chemical etching to remove unreacted Ti, leaving TiSi_2 , called **selective etching**



LI Oxide as a Dielectric for Inlaid LI Metal (Damascene)

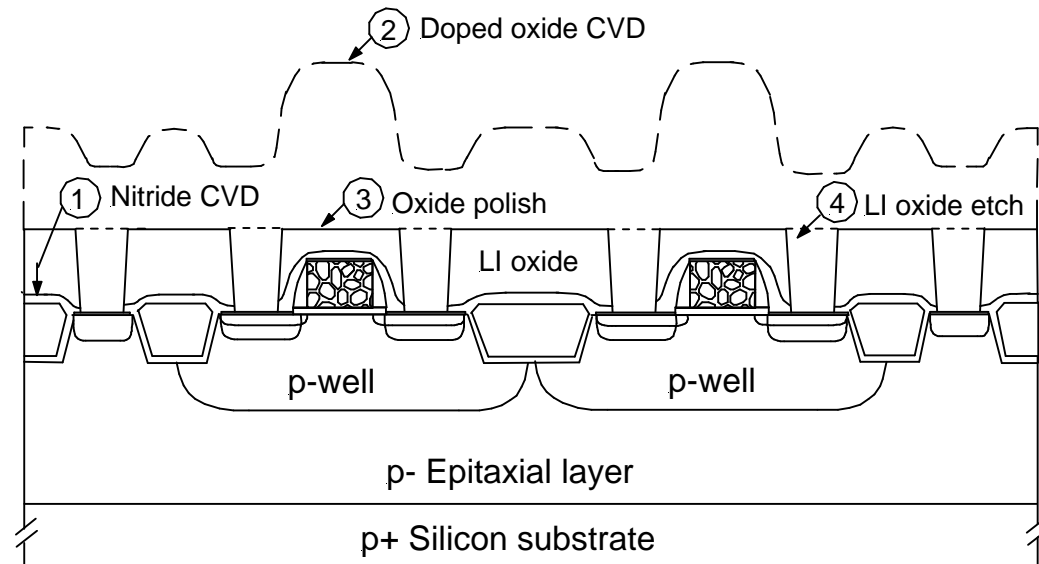
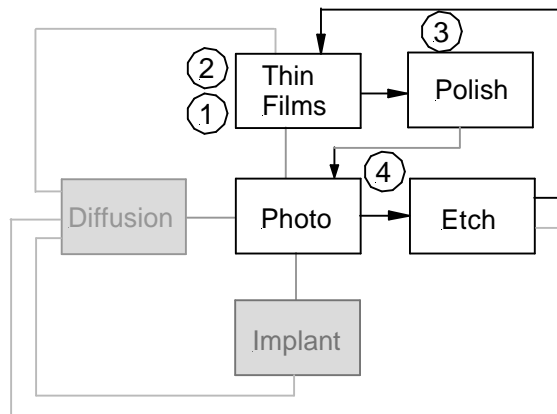
Damascene: a name coined of year ago from a practice that began thousands ago by artist in Damascus, Syria



LI: local interconnection

LI Oxide Dielectric Formation

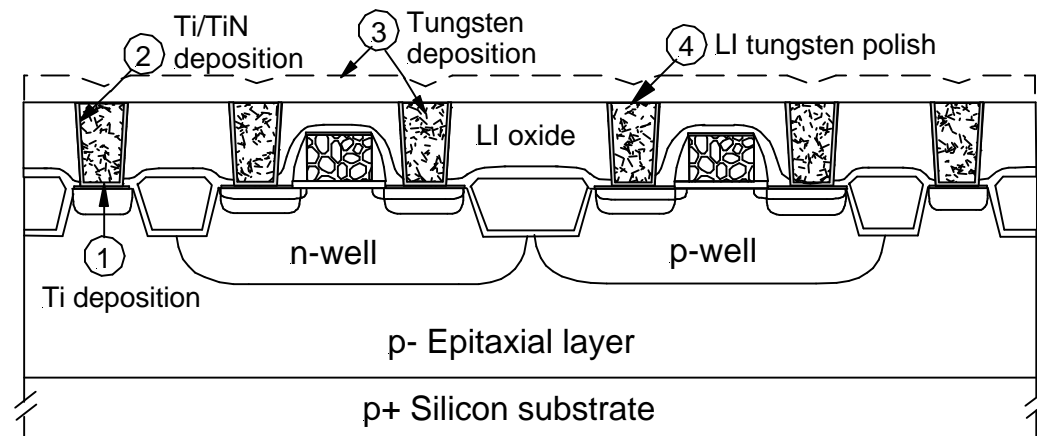
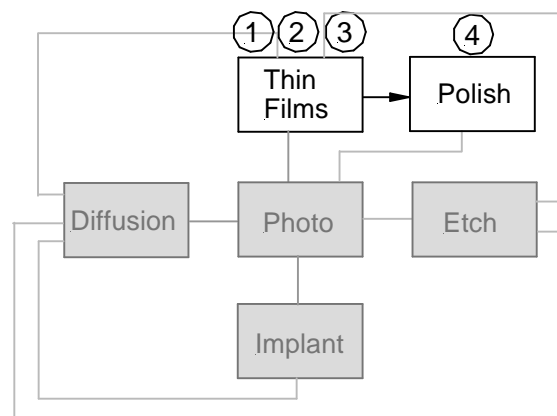
1. **Nitride: protect active region**
2. **Doped oxide**
3. **Oxide polish**
4. **9th mask**



LI Metal Formation

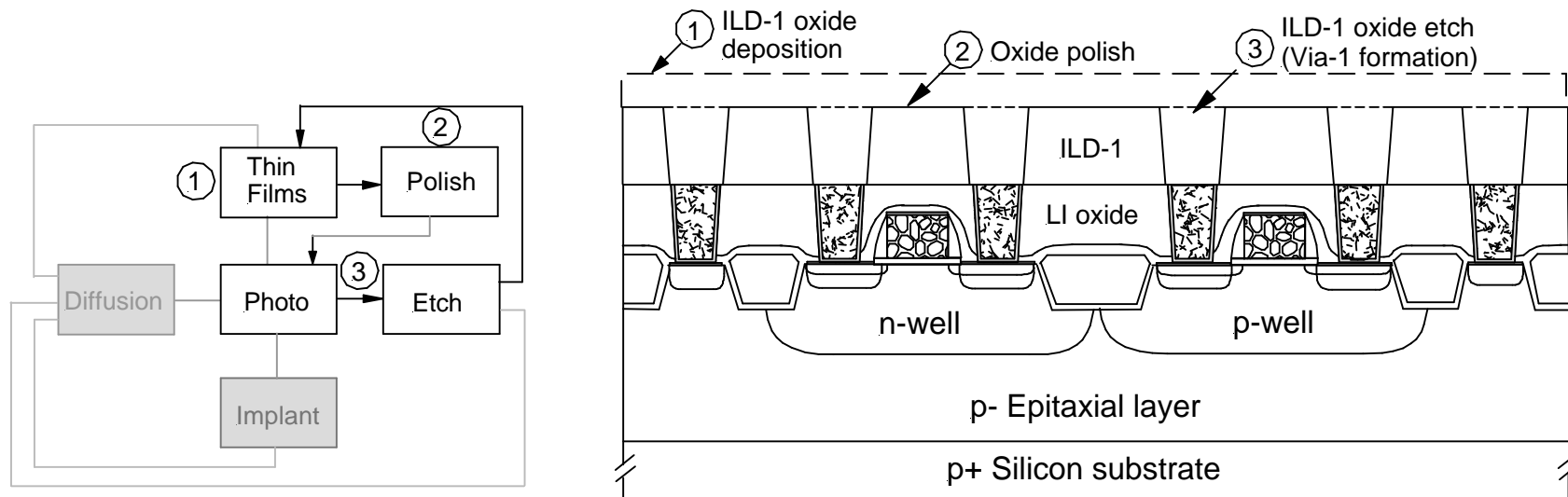
Ti/TiN is used: Ti for adhesion and TiN for diffusion barrier

Tungsten (W) is preferred over Aluminum (Al) for LI metal due to its ability to fill holes without leaving voids



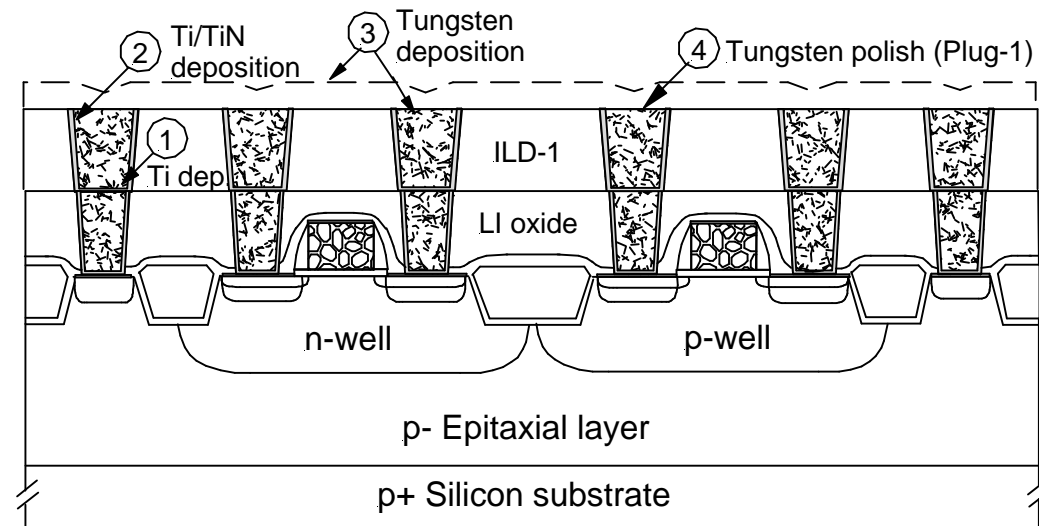
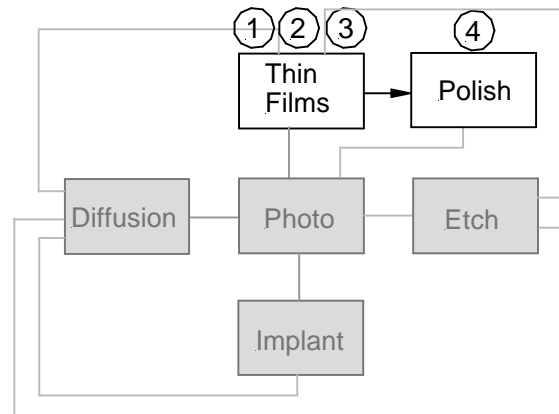
Via-1 Formation

1. **Interlayer dielectric (ILD): insulator between metal**
2. **Via: electrical pathway from one metal layer to adjacent metal layer**
3. **10 th mask**

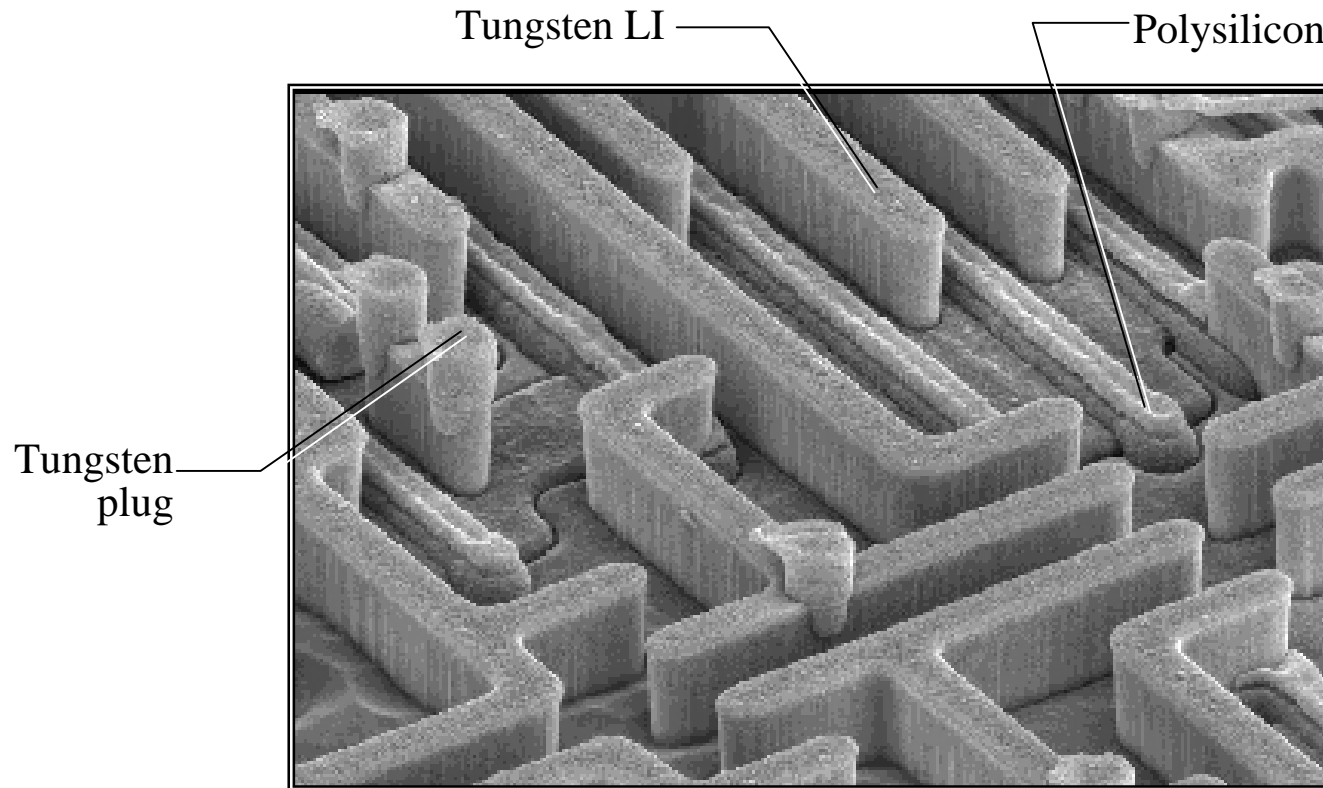


Plug-1 Formation

1. Ti layer as a glue layer to hold W
2. TiN layer as the diffusion barrier
3. Tungsten (W) as the via
4. CMP W-polish



SEM Micrographs of Polysilicon, Tungsten LI and Tungsten Plugs

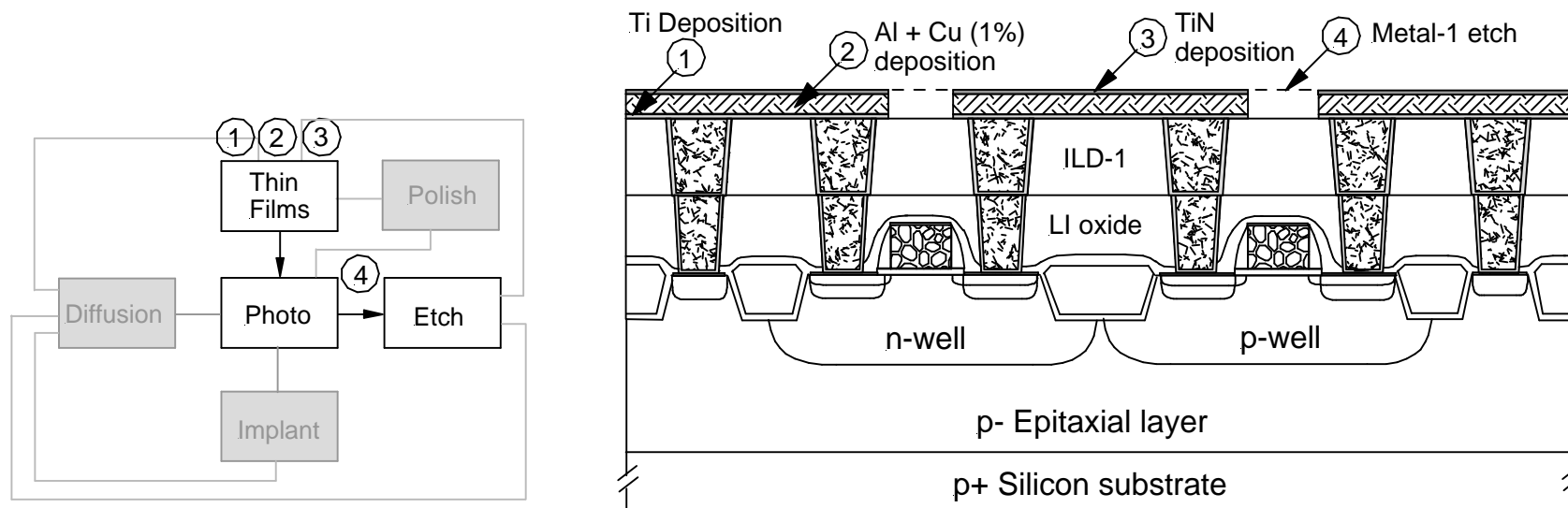


Mag. 17,000 X

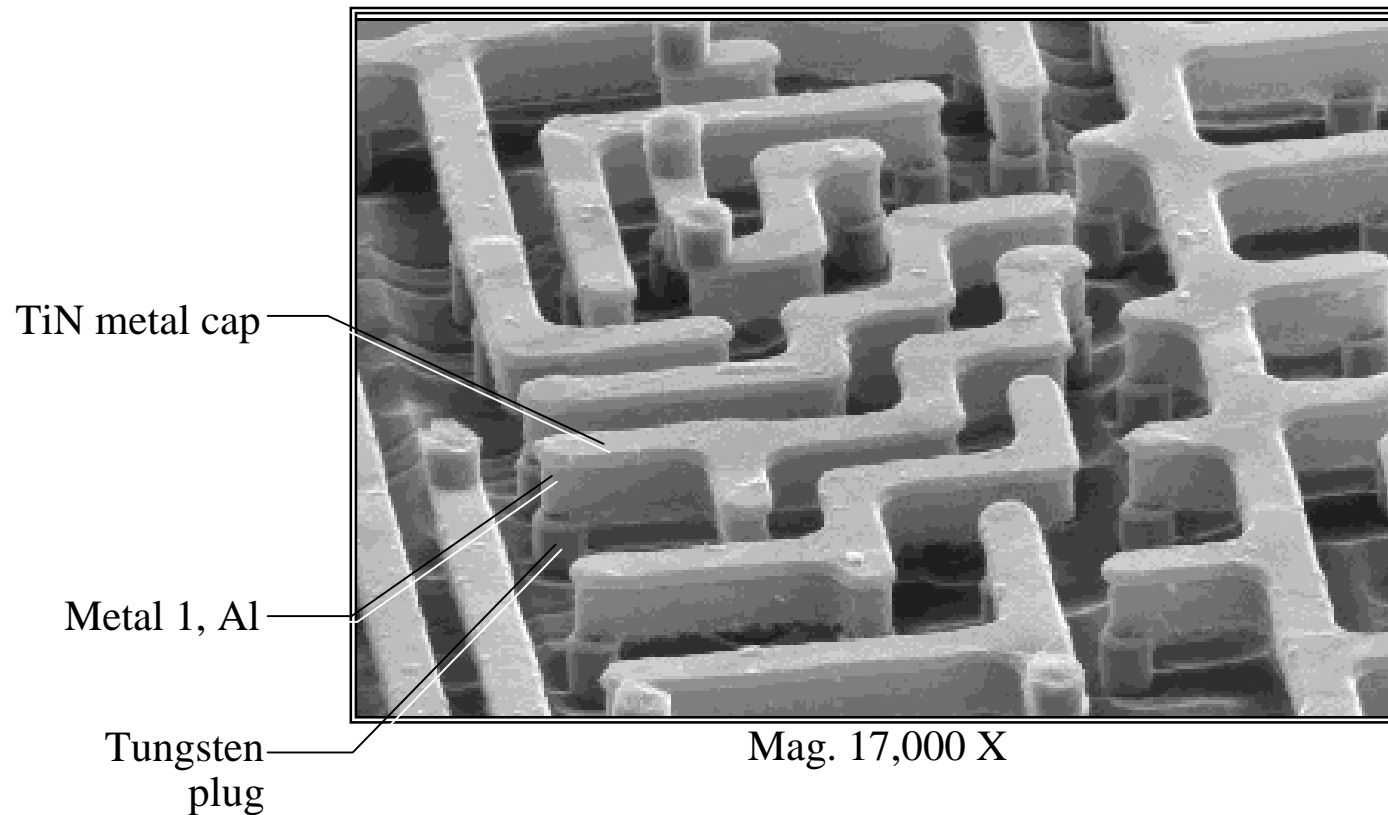
Micrograph courtesy of Integrated Circuit Engineering

Metal-1 Interconnect Formation

1. Metal stack: Ti/Al (or Cu)/TiN is used
2. Al(99%) + Cu (1%) is used to improve reliability
3. 11th mask



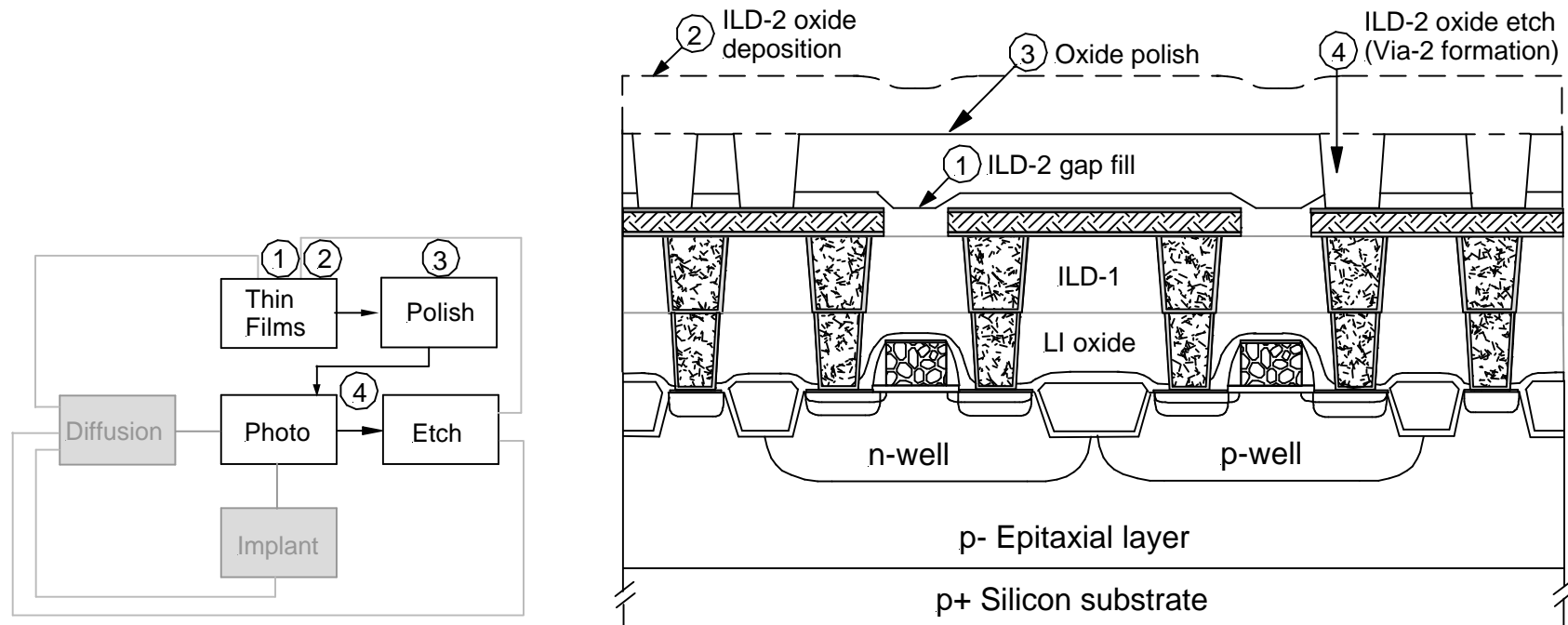
SEM Micrographs of First Metal Layer over First Set of Tungsten Vias



Micrograph courtesy of Integrated Circuit Engineering

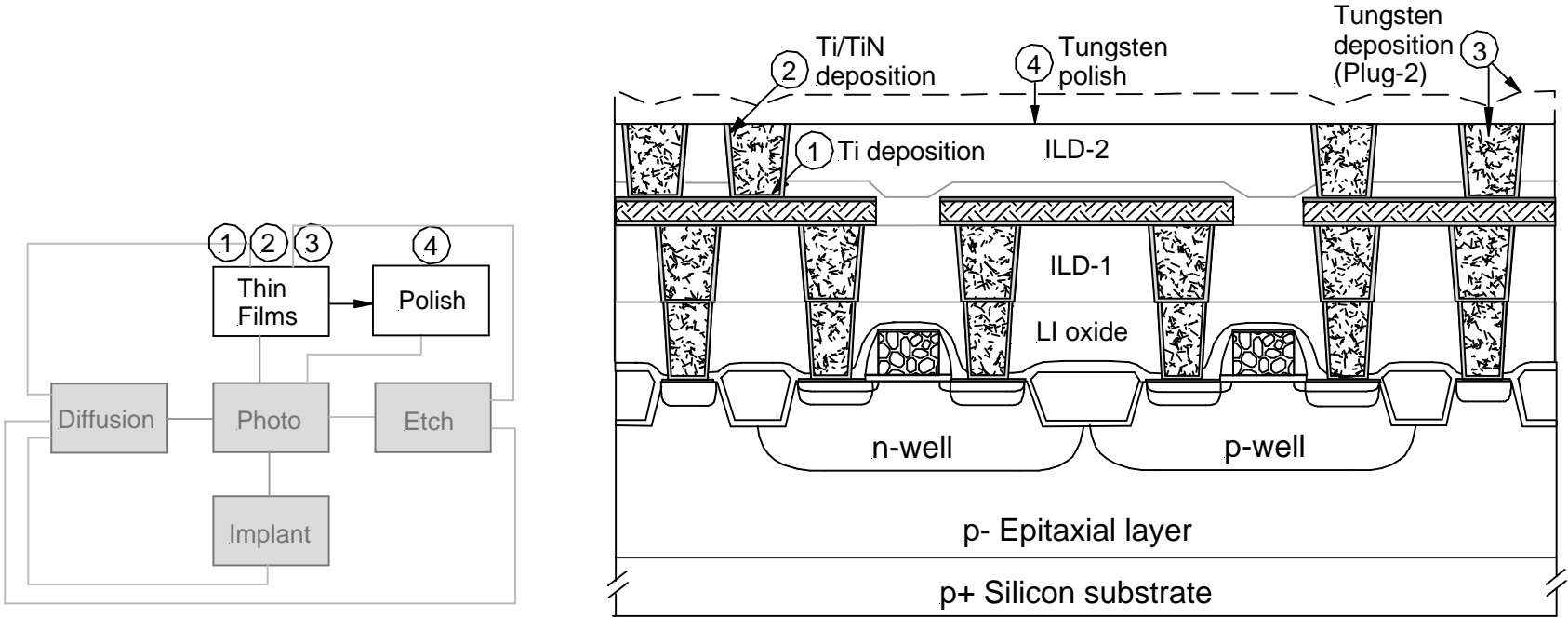
Via-2 Formation

1. **Gap fill: fill the gap between metal**
2. **Oxide deposition**
3. **Oxide polish**
4. **12 th mask**



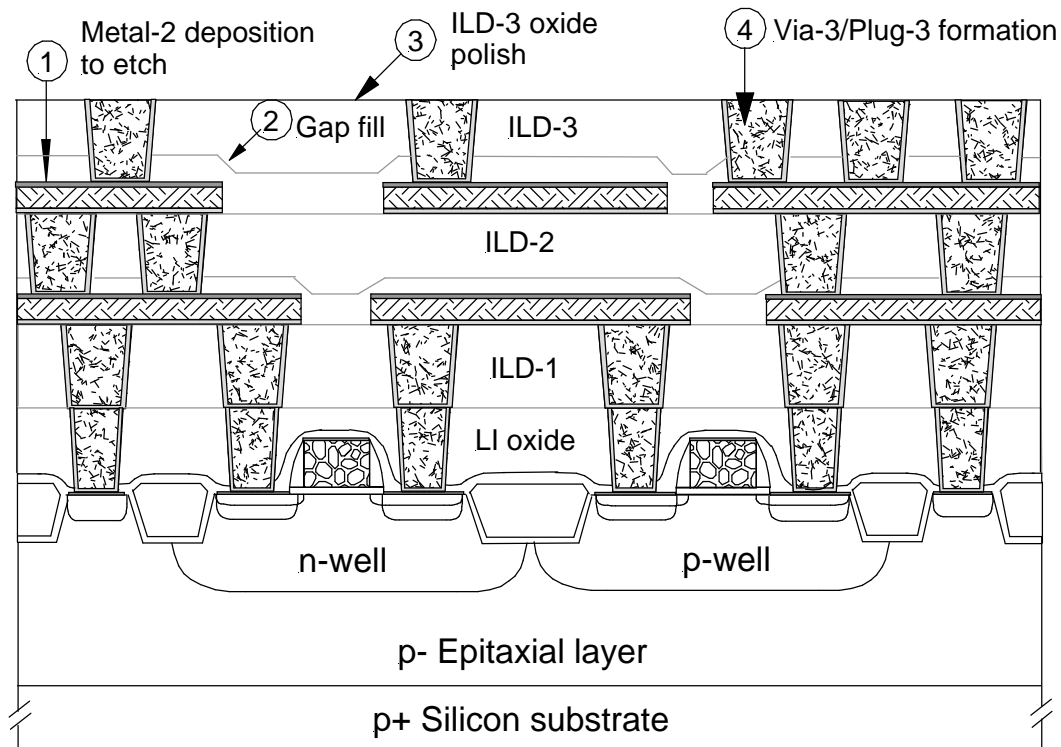
Plug-2 Formation

- 1. Ti/TiN/W
- 2. CMP W polish



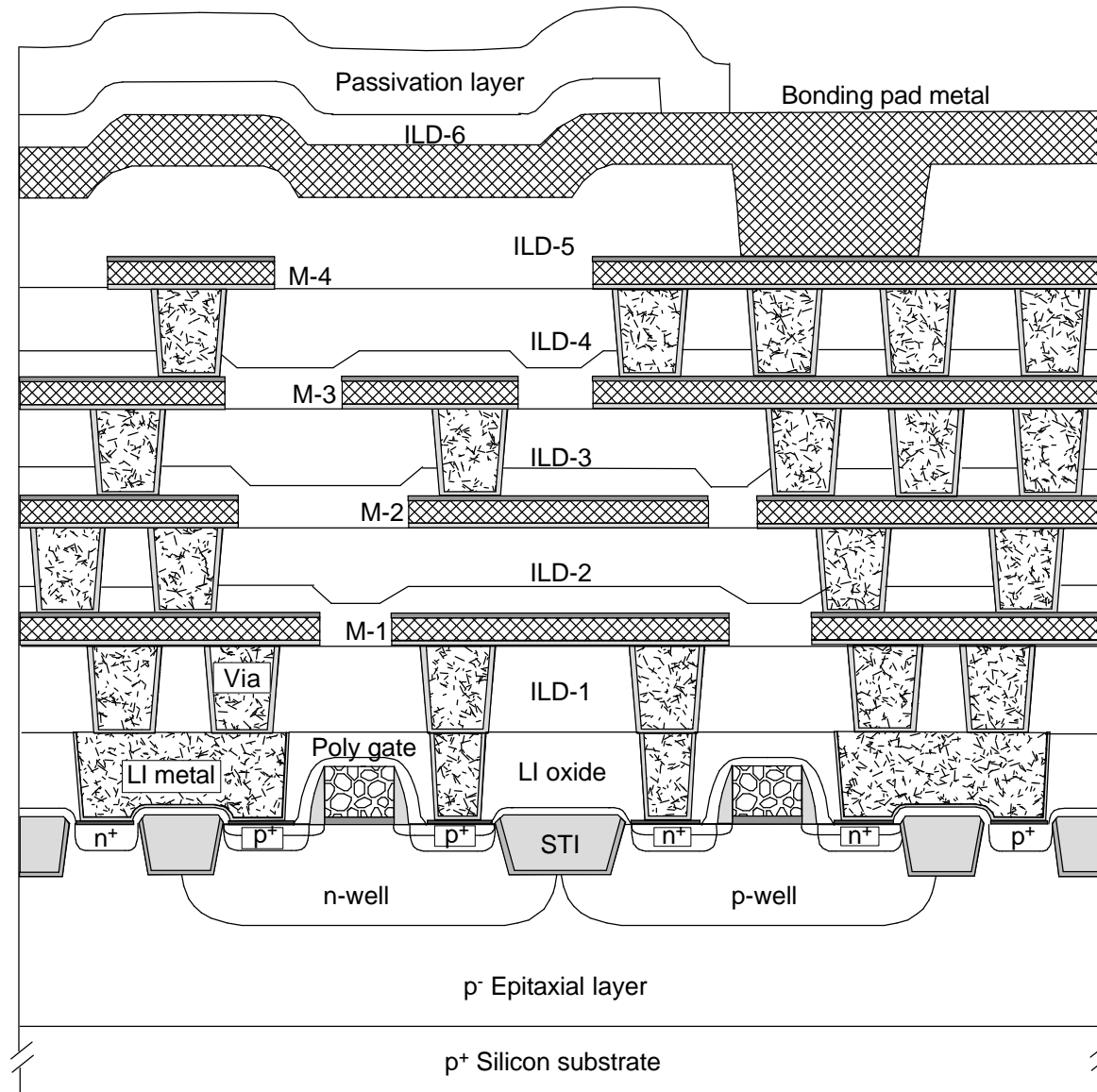
Metal-2 Interconnect Formation

1. **Metal 2: Ti/Al/TiN**
2. **ILD-3 gap filling**
3. **ILD-3**
4. **ILD-polish**
5. **Via-3 etch and via deposition, Ti/TiN/W**

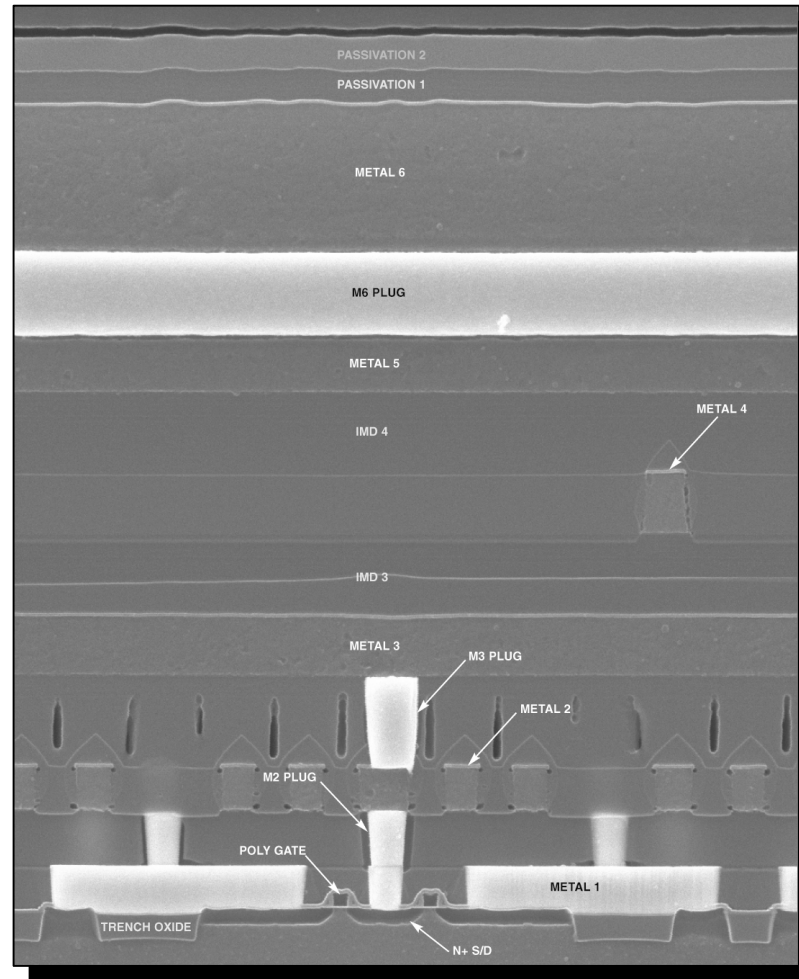


Full 0.18 μm CMOS Cross Section

1. Passivation layer of **nitride** is used to protect from moisture, scratched, and contamination
2. **ILD-6 : oxide**



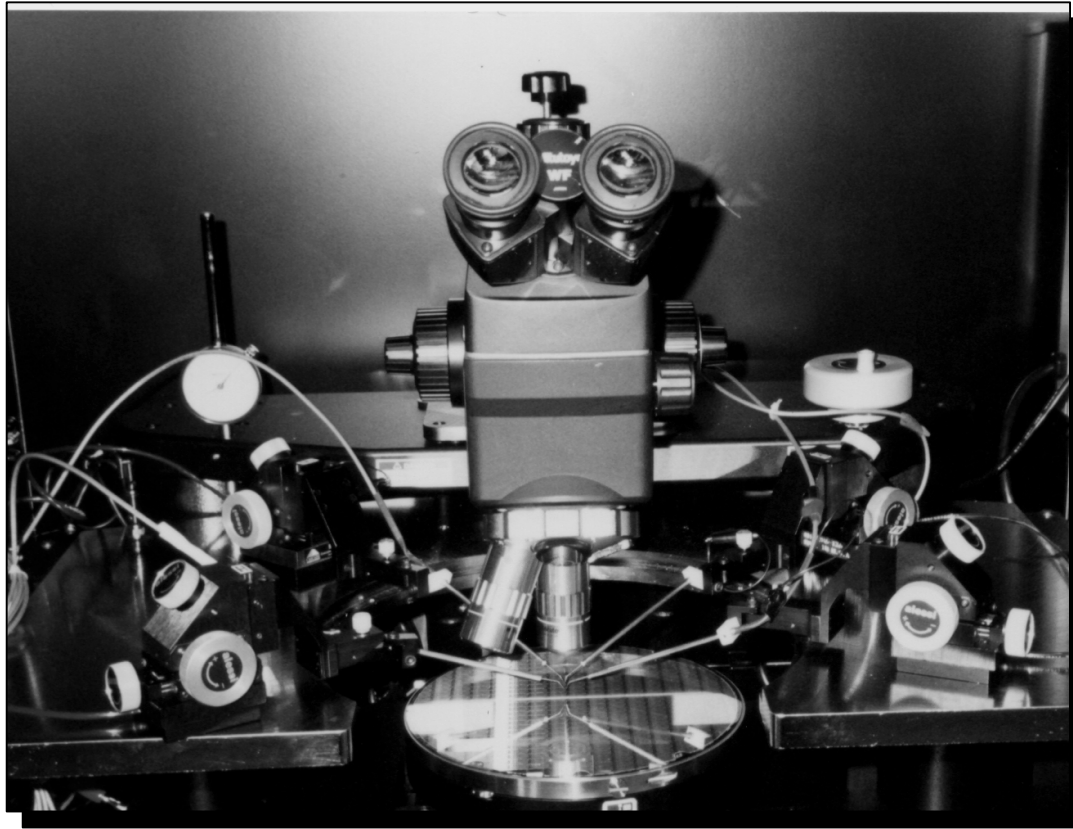
SEM Micrograph of Cross-section of AMD Microprocessor



Mag. 18,250 X

Micrograph courtesy of Integrated Circuit Engineering

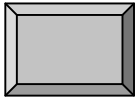
Wafer Electrical Test using a Micromanipulator Prober (Parametric Testing)



1. **After metal-1 etch, wafer is tested, and after passivation test again**
2. **Automatically test on wafer, sort good die (X-Y position, previous marked with an red ink)**
3. **Before package, wafer is backgrind to a thinner thickness for easier slice and heat dissipation**

Photo courtesy of Advanced Micro Devices

Chapter 9 Review

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