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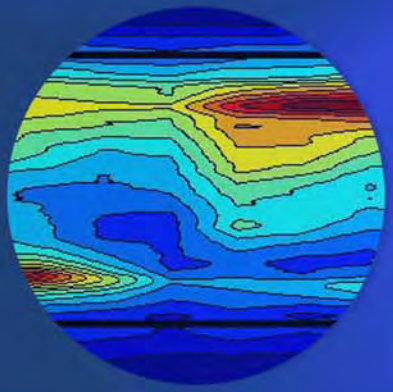

Semiconductor Microelectronics and Nanoelectronics Programs

Edited by

Stephen Knight
Joaquin V. Martinez de Pinillos
and Michele Buckley

NIST
National Institute of Standards and Technology
Technology Administration
U.S. Department of Commerce

July 2007

On the cover (top to bottom):

Joseph Hodges operating frequency-stabilized cavity ring-down spectroscopy (CRDS) for measuring very low concentration contaminants in process gases.

Time-resolved vertical distribution of optical emission at 750nm from a dual-frequency capacitively-coupled plasma.

Critical Dimension Small Angle X-Ray Scattering (CD-SAXS) detector image resulting from a dense array of 60 nm vias.

Curt Richter loads a molecular electronic sample for electrical characterization. Photo copyright Robert Rathe.

SEMICONDUCTOR MICROELECTRONICS AND NANOELECTRONICS PROGRAMS

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U.S. DEPARTMENT OF COMMERCE
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Technology Administration
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References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 2005 or the ITRS 2006 Update.

Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors, 2005 edition*. SEMATECH: Austin, TX, 2005.

These documents are available on-line at URL: http://public.itrs.net or in printed copy by contacting SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, ITRS department 860-008, phone: (512) 356-3500.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

Contents

Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards; and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the U.S. Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of 60 with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the U.S. Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which is providing a $12 million budget in fiscal year 2007.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, SEMATECH and its subsidiary, International SEMATECH Manufacturing Initiative (ISMI), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP and NIST Laboratories represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS), as well as on numerous SRC Technical Advisory Boards. NIST staff is also active in the International National Electronics Manufacturers Initiative (iNEMI), the EIA, the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI). NIST supports the United States National Committee Technical Advisory Group for the International Electrotechnical Commission Technical Committee TC113 on Nanotechnology Standardization for Electrical and Electronic Products and Systems (Technical Advisor, USNC TAG for IEC TC 113 on nanotechnology) by funding the Technical Advisor to that organization.

Learn More About Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact:

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From left to right: Joaquin Martinez de Pinillos, Stephen Knight, and Michele Buckley.

Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The workhorse tools at this point operate at 193 nm. In order to further shrink dimensions liquid immersion tools with water as the immersion fluid are being introduced. Further size reduction through the use of high index fluids, lens materials and photoresist for 193 nm tools are under intense exploration for even higher numerical aperture systems. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. At least three alpha tools were shipped to development consortia in 2006. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials, immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.

Metrology Supporting Deep Ultraviolet Lithography

Goals

Develop solutions to key optical metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of DUV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs

Increasing information technology requirements have created a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate optical measurements at DUV laser wavelengths.

A new lithography technology, immersion lithography, depends on incorporating a high-index fluid between the optical system and the wafer and possibly also incorporating a high-index material as the last lens element. Design and development of 193 nm immersion lithography requires accurate measurements of the index properties of the potential 193 nm fluids and materials.

To support these efforts, the National Institute of Standards and Technology (NIST), with SEMATECH, has developed a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential challenges for lithographic development are discussed in the 2005 International Technology Roadmap for Semiconductors. Page 1 of the Lithography section states: "Significant challenges exist in extending optical projection lithography at 193 nm wavelength using immersion lenses…." The need for advancing metrology in lithography is discussed on page 1 of the Metrology section: "Metrology continues to enable research, development, and manufacture of integrated circuits. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability."

Technical Strategy

High-accuracy measurements of the index properties of UV materials are required for the design of DUV lithography systems. NIST has been providing absolute index measurements at 193 nm and 157 nm with an accuracy of about 5 ppm to the industry using its DUV minimum-deviation-angle refractometer. To improve on this absolute accuracy, NIST has constructed a new state-of-the-art minimum-deviation system and separately developed another system based on a vacuum ultraviolet (VUV) FT spectrometer and synchrotron radiation as a continuum source (see Fig. 1). Both of these systems enable measurements to an accuracy of 1 ppm, and are used to characterize high-index lens materials and immersion fluids for 193 nm lithography systems.

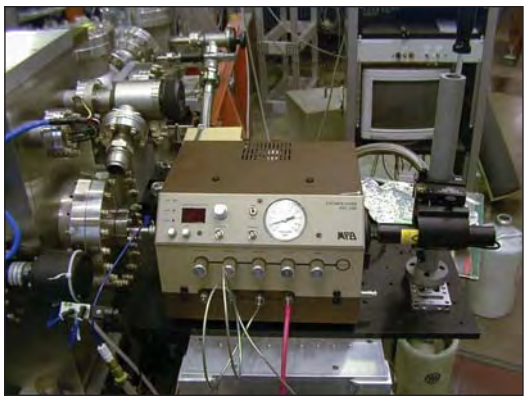

Figure 1. Facility for detector VUV radiation damage study using synchrotron radiation from SURF and a 157 nm excimer laser.

DELIVERABLES: Measurement of the refractive index of fused silica, CaF_2, and water, as well as high-index fluids and high-index lens materials, with an accuracy of 1 ppm. 4Q 2007

Taking full advantage of the potential resolution gain with immersion lithography may require using high-index materials as the last lens element, though as yet no such material has been demonstrated at 193 nm. To address this need we have, with the support of SEMATECH, undertaken and

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M. Dowell

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild, Massachusetts Institute of Technology's Lincoln Laboratory

completed a survey of candidate materials. As a result of this work we have identified two very promising materials, ceramic spinel and lutetium aluminum garnet (LuAG). Both materials have indices near 2.0 at 193 nm and have the potential for high optical quality at this wavelength. In addition, the intrinsic birefringence is low for LuAG and negligible for ceramic spinel. We are now characterizing the complete UV optical properties of these materials.

DELIVERABLES: Fully characterize the 193 nm optical properties of LuAG and ceramic spinel. 4Q 2007

An absolute light source in the DUV range based on synchrotron radiation using NIST's Synchrotron Ultraviolet Radiation Facility (SURF III) has been established using a dedicated beamline at SURF III. The flux of the DUV radiation at this beamline can be known to very high accuracy through the well established equations governing the behavior of the synchrotron radiation. The beamline is designed for customer calibration of a variety of DUV instruments to assist the development of the DUV lithography such as monochromators, discharge lamps, and irradiance meters. The spectral range covers all of the current important wavelengths for semiconductor industry such at 248 nm, 193 nm, 157 nm and even down to 13 nm. The uncertainty of such calibration is better than 1 % in the case of deuterium lamp calibration.

DELIVERABLES: Provide customer DUV calibration for discharge lamps, monochromators, and irradiance meters using SURF III source-based beamline with highest accuracy. Ongoing

Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, and specifically KrF (248 nm) and ArF (193 nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 nm, 248 nm, and 157 nm. Figure 2 shows the excimer laser calibration facility.

Figure 2. Laboratory for excimer laser energy and power meter calibrations, with measurement systems for 248 nm, 193 nm, and 157 nm. The excimer lasers are along the top right and the enclosures for nitrogen gas purging are in the foreground.

DELIVERABLES: Proven high-quality calibration services, and supporting measurements for excimer laser power and energy meters to the Semiconductor Industry at 248 nm, 193 nm, and 157 nm. Ongoing

ACCOMPLISHMENTS

- We have used our Hilger-Chance refractometer system to assist the industry in the search for appropriate high-index fluids (with *n* greater than water, 1.4366 at 193 nm) for possible use in immersion lithography resolution extension. Several promising fluids have been developed by the industry, and we have characterized their UV optical properties. Recently we have worked with the suppliers to demonstrate that several of these candidate fluids have stable optical properties over multiple exposure runs.

- As a result of our high-index materials survey, we have identified two very promising high-index 193 nm transmitting materials, that can potentially enable immersion lithography extension. These candidates are ceramic spinel and lutetium aluminum garnet (LuAG). We have demonstrated that both materials have good 193 nm optical properties, including sufficiently low spatial-dispersion-induced ("intrinsic") birefringence (see Fig. 3). Due to the results of our measurements, LuAG and ceramic spinel are now being developed by the industry for this application.

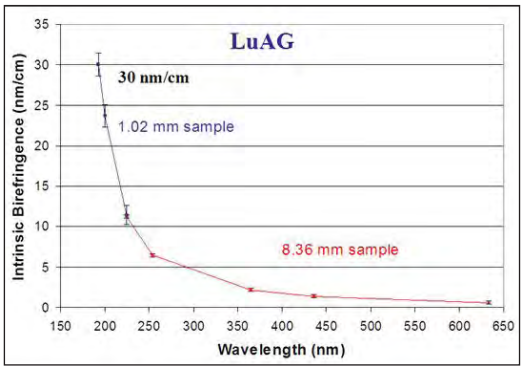

Figure 3. Measurement of the intrinsic birefringence of LuAG vs. wavelength.

■ We have constructed a radiometric facility tailored for the DUV range using a beamline at NIST's SURF III with the radiation measurement scale derived from a high-accuracy cryogenic radiometer. The beamline is designed for very general-propose high-accuracy measurements. We have used this facility to measure DUV general material properties such as transmission and reflectance. Examples of such measurements include DUV mirrors, windows, filters, and also the transmission and absorption of liquids that could be used for immersion lithography. On the detector side, we have calibrated and characterized a variety of DUV detectors such as solid state photodetectors, solar-blind detectors, photoconductive detectors, and pyroelectric detectors. We also performed irradiance calibrations for DUV irradiance meters.

■ We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation (see Fig. 4) and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F_2 excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes. For example, we have determined that for silicon photodiodes under irradiation with a 157 nm excimer laser, an important mechanism for the degradation is the formation of trap states at the interface of the silicon-silicon dioxide induced by the damaging radiation. These trap states act as recombination centers and reduce the yield of electric current generated by incident radiation. A model was developed to simulate the change in response for photodiodes irradiated by 157 nm radiation.

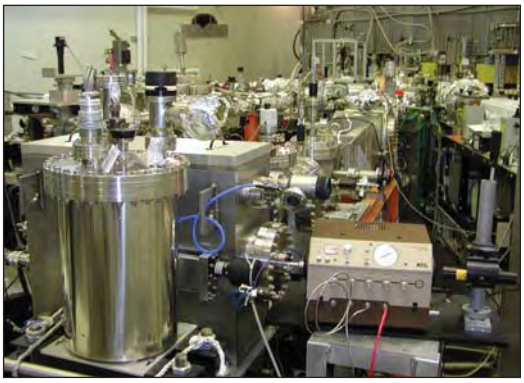

Figure 4. Measurement system for detector damage study by a 157 nm pulsed excimer laser.

■ During the last 15 years we have developed a suite of laser calorimeter standards for 248 nm, 193 nm, and 157 nm excimer laser energy and power measurements traceable to SI units. The 248 nm and 193 nm calorimeters use a specially designed absorbing cavity with a volume absorbing glass to reduce potential damage to the cavity by the high peak power in the UV laser pulses. The 157 nm calorimeter is a fundamentally new type of laser calorimeter standard that uses a thin-walled SiC absorbing cavity, which is designed to completely absorb and spread the incoming laser energy through multiple reflections. All of these calorimeters are calibrated using an imbedded electrical heater that allows for traceability to SI units through electrical standards of resistance and voltage. Calibrations for industry customers are accomplished for each wavelength with appropriate measurement systems that involve purging of oxygen to eliminate atmospheric absorption of the laser radiation.

■ As a further extension of our excimer laser services we have developed the capability to directly measure UV irradiance or "dose" at 248 nm and 193 nm, which involves homogenizing the beam profile and measuring the energy

transmitted through a calibrated aperture. This capability can improve accuracy for customers who need to measure the energy absorbed at a surface such as at the wafer plane.

We have also developed the capability to characterize the nonlinear response of 193 nm and 248 nm excimer laser detectors based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. Using this system, one can easily determine problems such as those due to the incident pulse energy, range discontinuities associated with detector gain, and detector background noise (see Fig. 5).

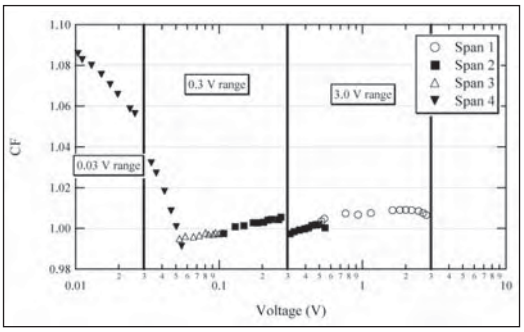

Figure 5. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

■ We completed the first internal comparison of the NIST UV excimer laser calorimeters. This work includes measurements taken over the course of a two-year period in which the performance of the NIST 157 nm, 193 nm, and 248 nm excimer laser calorimeters was monitored at the design wavelengths as well as at the other excimer laser wavelengths. The results show good agreement among the transfer standards and excellent stability over time. From these data, we determined that the responsivity of the NIST UV laser calorimeters all agree within their stated uncertainties. In all but one case, the calorimeters' responsivities agree to better than 0.3 %. The comparison between the DUV (193 nm) and UV (248 nm) calorimeters at 248 nm uncovered a 1 percent difference between the calorimeters' responsivities. This difference is due to partial transmission of the 248 nm radiation through the absorbing glass of the DUV calorimeter which, reduces the calorimeter's absorptance and alters its response.

Collaborations

DuPont, Roger French, immersion photolithography fluid development. Schott Lithotec, Lutz Partier, high index lithography materials development.

Recent Publications

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P. S. Shaw, R. Gupta, K. R. Lykke, "Stability of photodiodes under irradiation with a 157 nm pulsed excimer laser," Appl. Opt. **44**, 197 (2005).

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Metrology Supporting Extreme Ultraviolet Lithography

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S. Hill
R. Vest

Goals

Provide leading-edge metrology for the development and characterization of sources, optical components, and dosimeters used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

An intense international effort is presently under way to install EUVL into commercial production in 2011 at the 32 nm node. ASML has delivered two alpha-generation steppers for initial testing, one to SEMATECH in Albany and one to IMEC in Belgium.

Several significant challenges to commercialization of EUVL remain, including source power, optics lifetime, and optics and mask fabrication. The associated metrological challenges include the development of: (1) highly precise extreme ultraviolet (EUV) reflectometry; (2) accurate pulsed EUV radiometry for source comparisons and wafer-plane dosimetry; (3) accelerated testing techniques for optics lifetime characterization; and (4) nanometer-level optical figure measurement.

Technical Strategy

1. Precise EUV Reflectometry

The NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics up to 40 cm in diameter and 40 kg in mass. The facility has a demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.001 nm, with plans under-way to improve each accuracy by a factor of two in the near future.

Although primarily designed to serve the EUVL community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has also been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements in support of EUVL are the radiometric calibration of the "Flying Circus II" and "E-Mon" radiometers used for the comparison of source outputs, resist dosimetry, and determination of EUV optical constants through angle dependent reflectance measurements. The reflectivity of a typical mirror designed for use in a EUVL stepper is shown in Fig. 1.

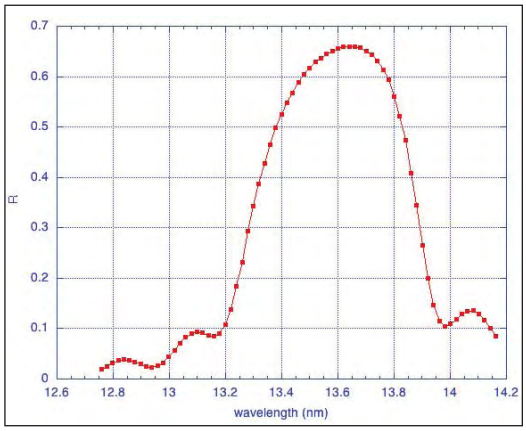

Figure 1. Reflectivity vs. wavelength of a typical MoSi multilayer mirror. The measurement was made at 5° from normal incidence.

DELIVERABLES: Full reflectivity maps of EUV mirrors up to 40 cm in diameter and 45 kg in mass on an as needed basis for the EUVL community. Many other types of EUV measurements including transmission, resist dosimetry and other testing, and cw radiometric calibrations of fully assembled filter radiometers used in source comparisons.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. The Photon Physics Group is responsible for maintaining the spectral responsivity standards in the far- and extreme-ultraviolet spectral regions, including 13.5 nm, the EUVL wavelength of interest. We operate several beamlines at the SURF III synchrotron radiation facility, a quasi-cw source, as well as a laser-produced plasma source, which is pulsed with a 10-ns pulse length. With these facilities, we can calibrate EUV detectors and dosimeter packages under either cw or pulsed conditions.

A major concern when using solid state photodiodes for detection of short pulse length radiation is that the detector may saturate under the high peak power, even though the average power is moderate. We have measured the saturation

characteristics of EUV sensitive Si photodiodes using 532 nm radiation as a proxy for 13.5 nm; the absorption characteristics in Si are nearly identical. This proxy procedure has been validated by correcting a 13.5 nm pulsed calibration for saturation in both the sample radiometer and the standard photodiode using saturation data obtained at 532 nm. The corrected results were in good agreement with individual component calibrations, while the uncorrected results were not.

We have found that the photodiode responsivity is an inherently non-linear function of pulse energy, but the responsivity can be fit by a calibration function having two constant parameters. Use of the non-linear calibration function allows the photodiode to be used with reasonable uncertainty even when the responsivity has decreased due to saturation effects by as much as a factor of two. We have developed a model of the physical processes that are responsible for saturation. The loss of total collected charge is modeled as a result of recombination processes in the device during the electronic readout time. The model correctly predicts the behavior of both calibration parameters as a function of reverse bias in the range from 0 V to 150 V and spot sizes greater than 0.01 mm^2. We have found no dependence on pulse length from 10 ns to 1 μs, indicating that the effects of saturation are the same for laser-produced plasma sources and for the pinched plasma sources with longer pulse lengths. There is substantial deviation from the expected saturation behavior as the illuminated area decreases (*i.e.*, the energy density increases) to very small spots sizes (less than 0.01 mm^2). The measured saturation loss is less than our model predicts, probably due to lateral diffusion current that reduces the local carrier density. It has been reported previously that the low-power limit of the pulsed responsivity is equal to the responsivity measured with a low-power, cw source. Combining these results, it is possible to transfer a continuous wave (cw) calibration to a pulsed application with low uncertainty.

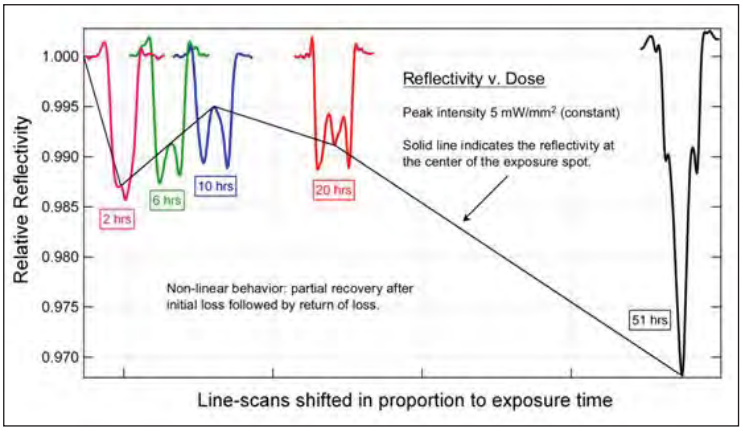

Figure 2. Detailed study of time and intensity dependence of degradation at a single pressure of 7 x 10^{-4} Pascals (5 x 10^{-6} Torr). Four regions noted: 1) very low fluence – improved reflectivity; 2) low to intermediate fluence – decreased reflectivity; 3) intermediate fluence – recovered reflectivity; and 4) high fluence – steadily decreasing reflectivity.

In 2006, we participated in an international intercomparison of EUV detector responsivity. This intercomparison will establish the world-wide equivalence of detector responsivity measurements from the major National Metrology Institutes performing these calibrations. We will also work to expand our EUV measurement capabilities to include measurements of EUV spectrograph and CCD responsivity to further aid the EUVL community.

DELIVERABLES:

- EUV detector responsivity international intercomparison; results expected. 3Q 2007
- New type of power meter for pulsed source. 2Q 2007
- Photodiodes and other EUV radiometric devices on customer as needed basis.

3. EUV Optics Damage Characterization

One of the potential showstoppers for commercialization of EUVL is the degradation of the multilayer-mirror stepper optics. The mirrors lose reflectivity because adsorbed contaminant gases such as hydrocarbons and water are cracked by the energetic (13.5 nm) photons. This leads to growth of an amorphous carbon layer on the optics surfaces or to oxidation of the optics themselves. The former effect is largely reversible; however, the latter is not. Unfortunately, these ambient contaminants cannot be eliminated by baking because the alignment of the mirror stack must be maintained to submicron tolerances and because of the presence of the outgassing from the resist coated wafer as it is being exposed.

The oxidation and carbonization are actually competing processes, and preliminary demonstrations have shown that the addition of a hydrocarbon can result in the deposition of a sacrificial layer of carbon that inhibits the oxidation of the cap layer that is used to protect the optic. The present strategy by the stepper manufacturers is to attempt to find a point in the oxidation-carbonization balance that leaves an oxidation-resistant cap layer, such as ruthenium, undamaged.

To study the effectiveness of such a strategy and to better understand the underlying processes responsible for mirror degradation, NIST has installed two beamlines at the Synchrotron Ultraviolet Radiation Facility (SURF III) that can expose capped-multilayer samples to ≈ 6 mW/mm^2 of 13.5 nm radiation in an environment of controlled water or hydrocarbon partial pressures up to 6.7×10^{-4} Pa. To date the most oxidation-resistant capping layers available have been ~ 2 nm of ruthenium or ~ 2 nm of titanium dioxide. Our exposure facility has demonstrated that multilayers with these capping layer suffer approximately one-tenth the reflectivity loss of bare Si-capped multilayers when exposed for ≈ 100 h under rather aggressive oxidation conditions of 1×10^{-4} Pa of water vapor. In addition to measuring the reflectivity loss of exposed multilayers (Figure 2), the damage will be characterized using a range of surface analysis techniques including micro XPS.

In addition to expanding our facilities, we have also established very fruitful collaborations with experts in surface science both within and outside the NIST community.

DELIVERABLES:

- Work with industrial collaborators to evaluate various hydrocarbon-oxidation balance mitigation schemes. 4Q 2007
- Develop with industrial collaborators standard testing for resist outgassing. 3Q 2007

4. Sub-nm Uncertainty Optical Figure Measurement

The commissioning of the "eXtremely accurate CALIBration InterferometeR" (XCALIBIR) at NIST is now complete and the instrument is fully functional (Fig. 3). The XCALIBIR interferometer is a multi-configuration precision phase-measuring interferometer for optical figure measurements of flat, spherical and aspheric optics that can achieve the very low measurement uncertainties that are required for the measurement of EUVL optics.

The XCALIBIR interferometer may be operated in either Twyman-Green or Fizeau configurations. A beam expander in the test arm of the interferometer provides a collimated test beam with 300 mm diameter. Transmission spheres are used to realize a spherical Fizeau interferometer for the testing of spherical and aspheric surfaces. The part under test is mounted on a remotely controlled 5+1-axis mount that can be moved on air bearings along

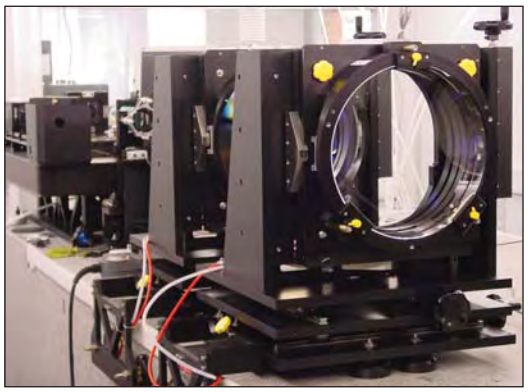

Figure 3. A view of the XCALIBIR interferometer.

a precision slideway in the direction of the optical axis of the interferometer. A system of three laser-interferometers tracks the movement of the test mount in the direction of the optical axis. A single-mode external cavity diode laser (ECDL) is used as the light source in XCALIBIR. The laser frequency can be modulated to vary the effective temporal coherence over a wide range. Optical fibers with different core diameters are used to couple the light into the interferometer. The spatial coherence of the light source can thus be varied by using fibers with different core diameter.

The 300 mm diameter reference flats for the flat Fizeau configuration of the interferometer were calibrated with a 3-flat, 6-position self-calibration test. Figure 4 shows the topography of one of the reference flats. A large number of 3-flat measurements were made to estimate the measurement uncertainty. For each of the flats A, B, and C the *rms* of the difference between the averaged flat solutions and the individual measurements was plotted in a histogram (Fig. 5, next page). A (statistical) measurement uncertainty of approximately 0.2 nm rms is evident.

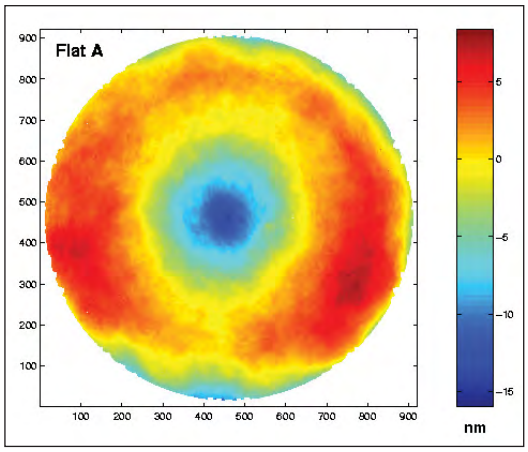

Figure 4. Topography of a 300 mm diameter XCALIBIR reference flat.

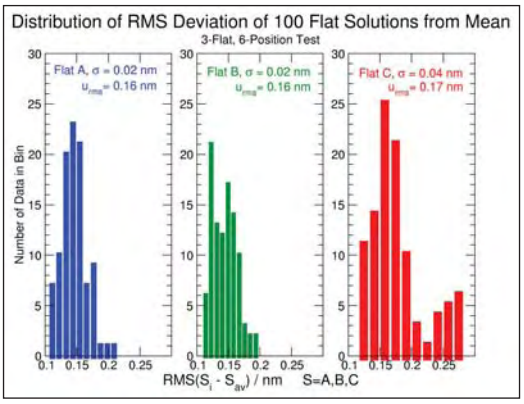

Figure 5. Distribution of rms *deviations from best estimates surface (mean) for three flats A, B, and C.*

When measurements of aspheric optics without null-optics are made, it is frequently the case that only a part, or subaperture, of a surface can be measured at once. For the figure measurement of the entire aspheric surface a number of overlapping subaperture measurements must then be combined, or "stitched" together. We have implemented flexible and robust algorithms for the stitching of subaperture measurements. To demonstrate the power of the stitching algorithm a precision silicon sphere with 96.4 mm diameter (a 1 kg mass sphere) was set up on a rotary table in XCALIBIR and the surface figure error was measured with an F/1.3 transmission sphere. 138 surface error measurements were made at 10° intervals. As shown in Fig. 6, the individual, overlapping, surface error measurements were then stitched together to form a map of the form error of the silicon sphere.

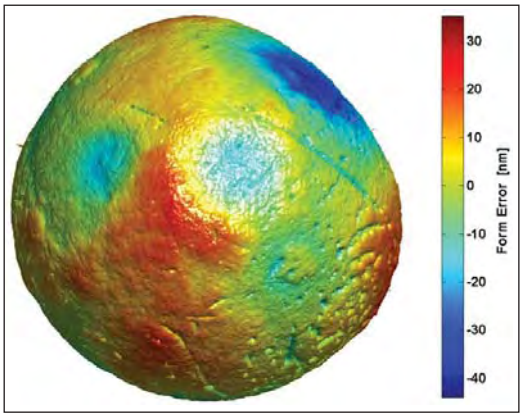

Figure 6. Deviation from perfect spherical form of a 1 kg precision silicon sphere.

In addition to the XCALIBIR interferometer, we are developing a new metrology tool for the measurement of aspheric and free-form precision surfaces, the Geometry Measuring Machine (GEMM). In its current form, GEMM is a profilometer for free-form surfaces. A profile is reconstructed from the local curvature of a test part surface, measured at several locations along a line. For profile measurements of free-form surfaces, methods based on local part curvature sensing have strong appeal. Unlike full-aperture interferometry they do not require customized null optics. The uncertainty of a reconstructed profile is critically dependent upon the uncertainty of the curvature measurement and, to a lesser extent, on curvature sensor positioning accuracy. The new instrument, shown in Fig. 7, provides an alternative means for validating the measurements made with XCALIBIR.

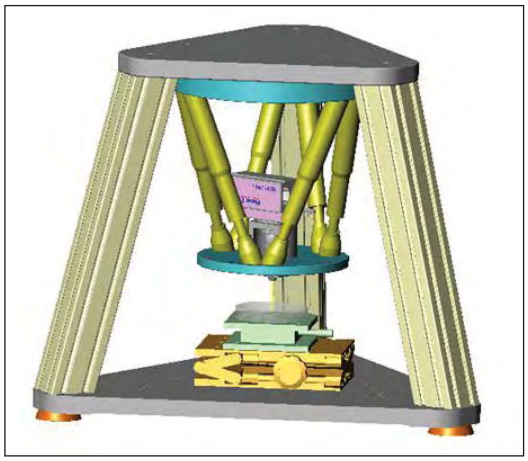

Figure 7. Geometry Measuring Machine (GEMM) for form measurements of free-form precision surfaces.

DELIVERABLES: Validation of stitching method for form error measurements of aspheric surfaces with low uncertainty. This will be done with an industrial collaborator. 4Q 2006

Collaborations

VNL at Lawrence Livermore National Laboratory, Saša Bajt, EUV Multilayer Development and Coating Team.

Recent Publications

U. Griesmann, Q. Wang, and J. Soons, *"Three-Flat Tests Including Mounting-Induced Distortions,"* Optical Engineering 2007 (in press).

S. Grantham, C. Tarrio, R. E. Vest, and T. B. Lucatorto, *"Metrology for EUVL Sources and Tools, in EUV Sources for Lithography,"* V. Bakshi, ed. (SPIE Press, Bellingham, WA, 2006).

R. E. Vest, Y. Barad, M. L. Furst, S. Grantham, C. Tarrio, and P. S. Shaw, *"NIST VUV Metrology Programs to Support Space-Based Research,"* Advances in Space Research **37**, 283-296 (2006).

R. E. Vest, S. Hill, and S. Grantham, *"Saturation effects in solid-state photodiodes and impact on EUVL pulse energy measurements,"* Metrologia **43**, S84-S88 (2006).

S. M. Owens, J. S. Gum, C. Tarrio, S. Grantham, J. Dvorak, B. Kjornrattanawanich, R. Keski-Kuha, R. J. Thomas, C. C. Kankelborg, *"Narrow-band EUV multilayer coating for the MOSES sounding rocket,"* in Proc. SPIE Vol. 5900, Optics for EUV, X-Ray, and Gamma-Ray Astronomy II, pp. 5-13 (2006).

U. Griesmann, *"Three-Flat Test Solutions Based on Simple Mirror Symmetry,"* Applied Optics 45, 5856-5865 (2006).

N. Machkour-Deshayes, J. Soons, U. Griesmann, R. S. Polvani, J. Stoup, and Z. Q. Lu, *"Form-profiling of optics using the Geometry Measuring Machine and the M-48 CMM at NIST,"* Accepted for publication in J. Res. NIST (2006).

S. Grantham, C. Tarrio, S. B. Hill, and T. B. Lucatorto, *"Optics go to extremes in EUV Lithography,"* Laser Focus World, Vol. **41**, no. 11, pp. 117-122 (2005).

C. Tarrio and S. Grantham, *"A synchrotron beamline for extreme-ultraviolet multilayer mirror endurance testing,"* Rev. Sci. Instrum. **76**, 056101 (2005).

C. Tarrio, S. Grantham, R. E. Vest, and K. Liu, *"A simple transfer-optics system for an extreme-ultraviolet synchrotron beamline,"* Rev. Sci. Instrum. **76**, 046105 (2005).

U. Griesmann, N. Machcour-Deshayes, J. Soons, B. C. Kim, Q. Wang, J. R. Stoup, and L. Assoufid, *"Uncertainties in aspheric profile measurements with the Geometry Measuring Machine at NIST,"* in Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies II; Angela Duparre, Bhanwar Singh, Zu-Han Gu; Eds., Proc. SPIE **5878**, 112-124 (2005).

U. Griesmann, Q. Wang, J. Soons, and R. Carakos, *"A simple ball averager for reference sphere calibrations,"* Optical Manufacturing and Testing VI; H. Philip Stahl; Ed., Proc. SPIE **5869**, 189-196 (2005).

U. Griesmann, J. Soons, and Q. Wang, *"Measuring Form and Radius of Spheres with Interferometry,"* Annals of the CIRP **53**, 451-454 (2004).

W. M. Clift, L. E. Klebanoff, C. Tarrio, S. Grantham, O. R. Wood II, and N.V. Edwards, *"Scaling studies of capping layer oxidation by water exposure with EUV radiation and electrons,"* SPIE vol. 5374, Emerging Lithographic Technologies VIII p. 666 (2004).

Polymer Photoresist Fundamentals for Next-Generation Lithography

Goals

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. This program provides a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 50 nm structures. The unique measurement methods we apply include specular and off-specular X-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), near-edge X-ray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), solid state nuclear magnetic resonance (NMR), atomic force microscopy (AFM), infrared variable angle spectroscopic ellipsometry (IR-VASE), and fluorescence correlation spectroscopy (FCS). Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the photoresist polymer chain architecture and conformation within sub 50 nm structures; (2) the spatial segregation and distribution of critical photoresist components; (3) the transport and kinetics of photoresist components, and the deprotection reaction interface over nanometer distances; (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process; (5) the polymer physics of the developer solution and the dissolution process; and (6) influence of moisture on the thermo-physical properties of interfaces as applicable to immersion lithography. These data are needed to meet the future lithographic requirements of sub 50 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility for development in an aqueous base solution. These reaction-diffusion, and development processes must be understood and controlled at the nanometer length scale to fabricate effectively integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 50 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 50 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm or EUV) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, component distribution, or transport properties. Furthermore, the required resolution for a sub 50 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the updated 2006 International Technology Roadmaps for Semiconductors on page 5, Lithography Section. Table 75 on "Lithography Difficult Challenges" for resist materials at sub- 32 nm indicates three issues (1) Resist and antireflective coating materials composed of alternatives to PFAS compounds, (2) Limits of chemically amplified resist sensitivity for < 32 nm

Technical Contacts:
V. M. Prabhu
E. K. Lin
W. L. Wu

"[This team has] made seminal contributions to the field of lithography in elucidating the effects that contribute to line edge roughness using the unique technical capabilities and know-how of NIST. Their successful cooperation with industry partners and research organizations has been both scientifically outstanding as well as a model of how to implement such joint research efforts."

Ralph Dammel, AZ Electronics

"[This team has] made ground breaking contributions to the fundamental understanding of resist line edge roughness — a technological bottleneck that threatens to derail the continuing miniaturization of the semiconductor devices."

Qinghuang Lin, IBM

"… I just finished a presentation for AMD on your work. Every time I look at it, the framework that has been established seems more and more valuable for future work. … AMD is a huge proponent of what you have done."

Karen Turnquest, AMD, SEMATECH, Lithography

half-pitch due to acid diffusion length, and (3) materials with improved dimensional control and LWR control.

Technical Strategy

In this project, we use model photoresist materials to validate the new measurement methods. Model photoresist materials (248 nm, 193 nm, and EUV) have been used initially to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the deprotection reaction kinetics, and the physics of the development process. These results provide a basis for understanding the material property changes that may affect the development of lithography for sub-50 nm structures using thin photoresist imaging layers. The interaction between model photoresists and BARC materials also requires detailed experimental investigation to optimize the materials factors impacting lithographic performance. Each process step requires an interdisciplinary array of experimental techniques to measure the polymer chemistry and physics in thin films as shown in Fig. 1.

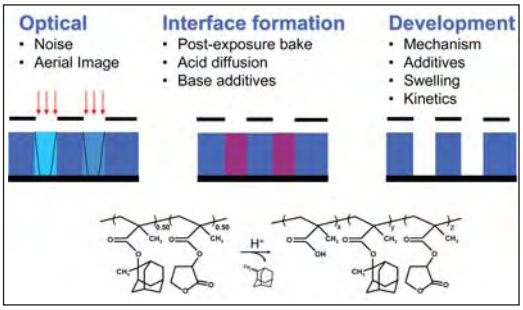

Figure 1. Key lithographic process steps studied for materials fundamentals. A model 193-nm resist under investigation is shown with the acid-catalyzed deprotection reaction.

DELIVERABLES:

- Develop reaction kinetics models to analyze experimental data as a function of dose, PEB time, and component concentration. 1Q 2007
- Measure the *in situ* spatial extent of the residual swelling fraction by neutron reflectivity. 2Q 2007
- Measure the effect of salt valence on the spatial extent of the residual swelling fraction by neutron reflectivity. 3Q 2007
- Develop a method to analyze the depth profiling of deprotection by variable-angle spectroscopic ellipsometry (IR-VASE). 3Q 2007
- Quantify the lateral length evolution in a model line-edge photoresist system by off-specular neutron reflectivity. 3Q 2007
- Assess development effects and influence of PAG loading on LER using the EUV exposure tool at the Advanced Light Source, Lawrence Berkeley National Laboratory. 4Q 2007
- Advance solid state NMR characterization of photoresist/photoacid generator dispersion to thin films using unique substrates. 4Q 2007

Accomplishments

■ EUV photoresist polymers are expected for imaging at the 32 nm node and smaller. Similar to 193 nm the deprotection reaction front profile is a critical factor. However, in particular to EUV photoresists high PAG loading as well as lower EUV doses are expected. We applied neutron reflectivity to understand the effect of dose using model deuterated polymeric resists as shown in Fig. 2. The deprotection fronts exhibit two different length scales; a slow front that initiates high degrees of deprotection near the interface and a fast front that propagates into the resist with reaction-diffusion lengths consistent with those reported in the literature. However, the deprotection level and diffusion-length scale are exposure dose (photoacid concentration) dependent. The origin of the fast-diffusion front dependence on dose was hypothesized due to the increase in copolymer composition polarity as the reaction proceeds thereby limiting the spatial-extent. The evolving copolymer composition appears central in future modeling of latent image profiles. Neutron reflectivity was demonstrated to have sufficient chemical sensitivity and spatial resolution to measure the interfacial structure on sub-nm length scales. This approach can be extended to understand the effects of additives, such as photodegradable bases, as well as different architecture such as the molecular glass photoresists shown in Fig. 2.

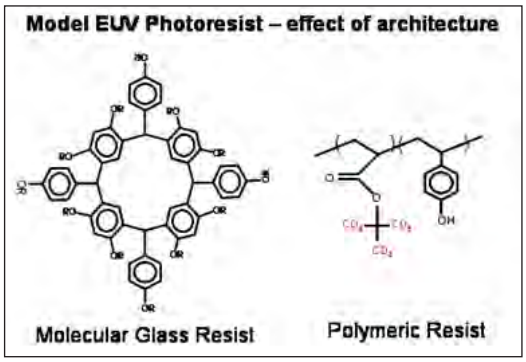

Figure 2. Two contrasting architectures of photoresist materials, but with similar chemistry: molecular glass and polymeric chemically amplified resist.

The effect of architecture or "pixel size" may also play a crucial role to higher fidelity imaging. We develop dissolution fundamentals to help quantify the effects of swelling and dissolution rate on the effect of resist architecture.

■ The molecular origin of dimensional changes within ultrathin films when exposed to developer solutions was measured using neutron reflectivity. A model photoresist material provided needed fundamentals of material sources to line-edge roughness. Quartz crystal microbalance measurements complement these measurements with the added ability to measure the kinetics of swelling, however, the profile and chemical specificity are exclusively obtained with NR.

■ These new measurement methods, applicable to immersion lithography, demonstrate that swelling and aqueous base penetration must be considered to improve dissolution models involving solid-liquid interfaces. The aqueous base profile, shown in Fig. 3, illustrates the penetration of the small deuterium labeled base molecule throughout the thin film as a function of developer strength. The influence of moisture and interfacial energy are also probed using NR, XR, and quartz crystal microbalance techniques, allowing complete equilibrium and kinetics measurement methods.

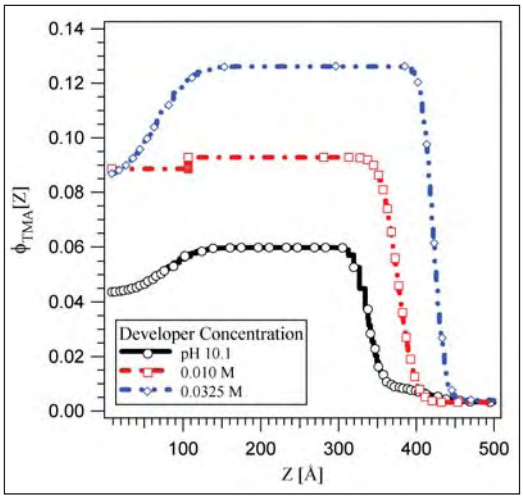

Figure 3. Developer Fundamentals for LER. Direct measure of the base concentration dependence of swelling and deuterated tetramethyl ammonium ion profile throughout the thickness, of a model 157 nm photoresist using liquid immersion neutron reflectivity.

■ Insight into the mechanism of development, rinse, and drying at a gradient line edge was measured by neutron reflectivity with nm resolution. Direct measurements highlight a residual swelling fraction during the development process steps with a lower composition limit for swelling at the model line edge. The final surface roughness is formed by the collapse of this highly associated and surface swollen phase during the drying process. A mechanism of a simple transfer of roughness from the latent image to the developed image is challenged by these data due to the swelling and associating polymer layer. Extending these concepts to previous latent image analysis imply the minimization of the residual fraction provides the lowest surface roughness. This can be achieved through resist and optical design to provide the highest latent image profile slope. However, an ideal collapse and complete elimination of surface roughness was not observed in agreement with lithographic studies. Future simulations and models should include both percolation and penetration of developer and an associative polymer behavior due to the heterogeneity and large chemical mismatch of resist components.

■ The kinetics of an acid-catalyzed deprotection reaction in model photoresist materials was studied as a function of copolymer composition with Fourier transform infrared (FTIR) spectroscopy. Three methacrylate-based terpolymers with varying compositions of acid-labile and non-reactive (lactone) monomers were studied. A mathematical model was developed to analyze the acid catalyzed deprotection kinetics with respect to coupled reaction rate and acid-diffusion processes. The first order reaction rate constant decreases as the non-reactive comonomer content is increased. Additionally, the extent of reaction appears self-limiting as verified by a slowing down necessitating an acid-trapping chemical equation to model the data. An example is shown in Fig. 4. This composition-dependent reaction constant indicates a strong interaction of the acid with the increasing polar resist matrix that

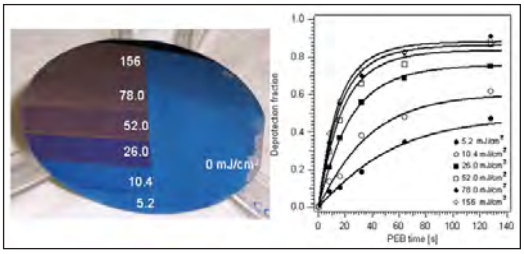

Figure 4. Wafer after exposure to varied DUV dose and fixed baking time the color change represents slight changes in film thickness with extent of reaction. Quantification of the extent of reaction (deprotection fraction) versus post-exposure bake time for model 193 nm resist for varying dose.

drastically reduces the acid transport rate. The reduced acid transport is consistent with hydrogen bonding between photoacid and methacrylic acid product. These results demonstrate a correlation between polymer microstructure and acid catalyzed kinetics. These are necessary measurements for analysis of coupled reaction-diffusion processes. Finally, the models were applied to understand the limiting spatial extent of photoacid diffusion at the model line edge determined by neutron reflectivity.

■ The deprotection reaction front profile was measured with nanometer resolution by combining neutron reflectivity and FTIR on a bilayer structure prepared with model 193 nm photoresists. The upper layer of the structure is loaded with the photoacid generator. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group partially leaves the film, quantified by FTIR, upon reaction. The contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that the reaction front width is dependent upon resist chemistry and PAG size as shown in Fig. 5. These experimental data provide a rational design of next-generation photoresist component from the resist chemistry to the reaction-diffusion process.

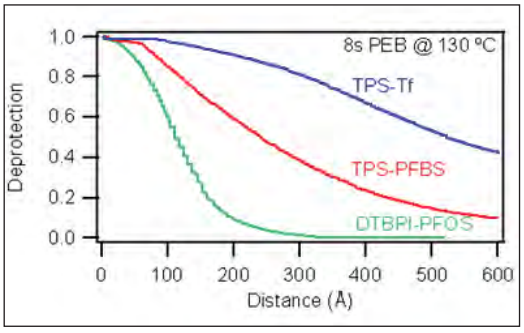

Figure 5. Neutron reflectivity results of the nanometer scale deprotection profile shape dependence on photoacid generator size: TPS-Tf < TPS-PFBS < DTBPI-PFOS. These high-resolution experimental data help verify current advanced reaction-diffusion models.

■ NEXAFS measurements were used to measure the surface concentration and depth profile of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment as shown in Fig. 6. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge X-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer chemistry and PAG size. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport and interactions enable detailed analysis of potential mechanisms leading to loss of profile control. UV exposure, post-exposure bake, and a novel atmosphere controlled chamber have been developed to test environmental stability against model airborne contaminants and influence on *in situ* processing.

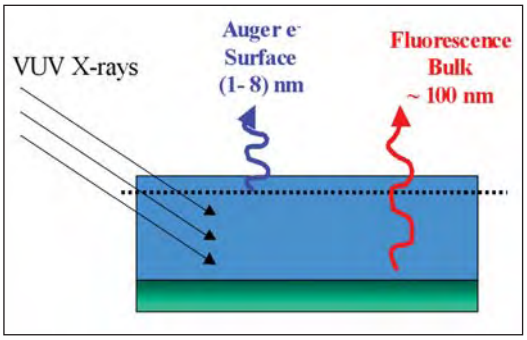

Figure 6. Schematic diagram of the NEXAFS measurement geometry. Spectra are obtained from the film surface and bulk simultaneously.

■ NEXAFS measurements were used to measure the surface concentration and depth profile of photoacid generators for advanced 193 nm photoresist materials for immersion lithography. These measurements quantify the influence of water immersion on the loss of these critical components. NEXAFS on wafer analysis combined

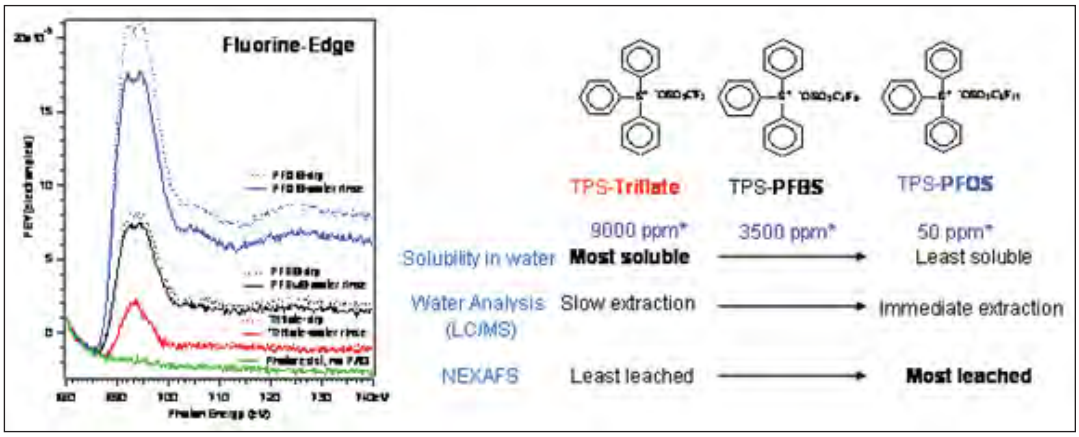

Figure 7. NEXAFS fluorine-edge experimental results quantifying the extent of PAG loss from the surface due to water immersion. The series of PAGs tested for immersion lithography is shown as a function of equilibrium water solubility, extraction from thin films, and NEXAFS surface composition analysis.

with LC/MS demonstrate that equilibrium water solubility of PAGs with varying perfluoroalkyl length does not serve as the appropriate criteria for selecting PAGs for immersion lithography; rather the segregation of PAGs to the top few nanometers provides the majority of leaching as shown in Fig. 7. Additionally, the effects of critical top coats are also investigated to understand the segregation and retention of PAG additives.

■ Characterization of local bulk scale mixing is necessary for understanding future photoresist materials as feature dimensions are reduced to sub-32 nm. The intimacy of mixing of PAG and photoresist was probed by solid state proton NMR methods based on inversion-recovery, solid-echo-spin-diffusion, and chemical-shift-based-spin-diffusion pulse sequences. The effect of resist architecture for EUV lithography has been investigated as a function of different molecular glass core structures (see Fig. 8). The PAG miscibility in several protected and deprotected versions have been discovered with these new classes of resist materials.

■ Current extreme ultraviolet photoresist materials do not yet meet requirements on exposure-dose sensitivity, line-width roughness, and resolution. Fundamental studies are required to quantify the trade-offs in materials properties and processing steps for EUV photoresist-specific problems such as high photoacid generator loadings and the use of very thin films. Furthermore, new processing strategies such as changes in the developer strength and composition may enable increased resolution. In this work, model photoresists (Fig. 7) formulated without base quenchers are used to investigate the influence of photoacid

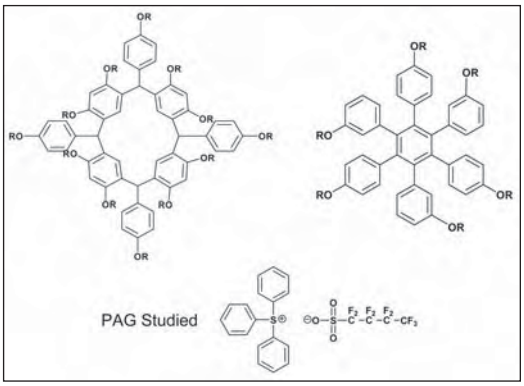

Figure 8. Model molecular glass with two different core architectures and photoacid generator studied for intimacy of mixing by NMR methods.

generator loading and developer strength on EUV lithographically printed images performed at the Advanced Light Source of Lawrence Berkeley National Laboratory. Measurements of LWR and developed line-space patterns highlight a combined PAG loading (Fig. 9) and developer strength dependence that reduce LWR in a non-optimized photoresist.

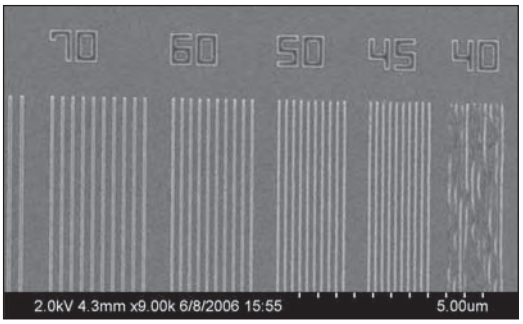

Figure 9. SEM image of EUV patterned model photoresists with nested 1:3 line/space developed in 0.1 mol/L TMAH.

■ The Optical Technology Division is developing chemical force microscopy (CFM) to measure the surface spatial distribution of chemical species in the imaged resist. Using CFM, the homogeneity of the resist can be imaged with chemical contrast using specially prepared probe tips. This information complements the height images obtained with AFM. The distribution of PAG after exposure and deprotected polymer after PEB are of interest. The distribution of deprotected polymer is of particular interest to quantify LER by non-destructive imaging techniques at the nanometer length scale. The latent image measured by CFM in Fig. 10 shows an image of an EUV-exposed model photoresist polymer (Fig. 7) resolved before development for two PAG loadings and varied 1:1 nested line/space.

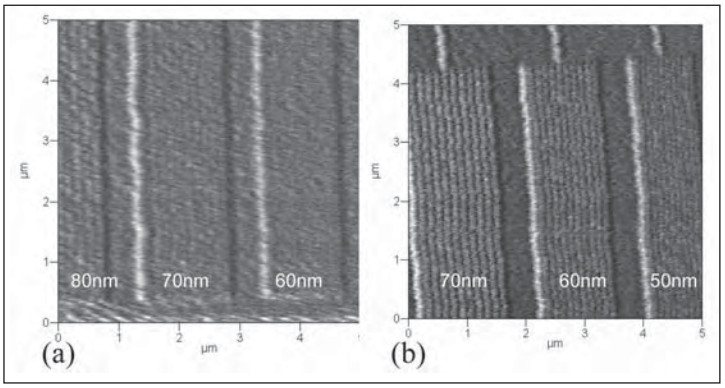

Figure 10. Chemical force microscopy scans of the latent images resolved before TMAH development of 1:1 nested line/space at 5 mJ/cm^2 (a) 3 % and (b) 15 % PAG loading.

Collaborations

Polymers Division, NIST – Shuhui Kang, Kristopher Lavery, David VanderHart

Ceramics Division, NIST – Sharadha Sambasivan, Daniel A. Fischer

Center for Neutron Research, NIST – Sushil K. Satija

Optical Technology Division, NIST – John Woodward, Jeeseong Hwang

Intel – Kwang-Woo Choi (Assignee to NIST), George Thompson

Cornell University – Christopher Ober

SEMATECH – Karen Turnquest

IBM Almaden Research Center – Hiroshi Ito, Robert D. Allen, William D. Hinsberg

AZ Electronics – Ralph Dammel, Frank Houlihan

DuPont Electronic Polymers L.P. – Jim Sounik, Michael T. Sheehan

Intel – CRADA

SEMATECH – Agreement 309841 OF (completed 11/ 06)

Recent Publications

K.-W. Choi, V. M. Prabhu, K. Lavery, E. K. Lin, W.-l. Wu, J. T. Woodward, M. J. Leeson, H. B. Cao, M. Chandhok, G. Thompson, "Effect of photoacid generator concentration and developer strength on the patterning capabilities of a model EUV photoresist" Proc. of SPIE, 6519, 651943 (2007).

V. M. Prabhu, B. D. Vogt, S. Kang, A. Rao, E. K. Lin, S. K. Satija, and K. Turnquest, *"Direct Measurement of the in situ Developed Latent Image: the Residual Swelling Fraction"* Proc. of SPIE, 6519, 651943 (2007).

W.-l. Wu,V. M. Prabhu, E. K. Lin, "Identifying materials limits of chemically amplified photoresists," Proc. of SPIE, 6519, 651902 (2007).

S. Kang, B. D. Vogt, W. Wu, V. M. Prabhu, D. L. VanderHart, A. Rao, E. K. Lin, and K. Turnquest. *"Characterization of compositional heterogeneity in chemically amplified photoresist polymer thin films with infrared spectroscopy."* Macromolecules 40,1497-1503 (2007).

B. D. Vogt, S.Kang, V. M. Prabhu, A. Rao, E. K. Lin, W.-l. Wu, S. K. Satija, and K. Turnquest, *"Influence of base additives on the reaction diffusion front of model chemically amplified photoresists,"* Journal of Vacuum Science and Technology B, 25,175-182 (2007).

K. Lavery, B. D. Vogt, V. M. Prabhu, K.-W. Choi, E. K. Lin, W.-l. Wu, S. Satija, *"Exposure dose effects on the reaction-diffusion process in model EUV photoresists,"* Journal of Vacuum Science and Technology B 24, 3044-3048 (2006).

B. D. Vogt, S. Kang, V. M. Prabhu, E. K. Lin, S. K. Satija, K. Turnquest, and W. Wu, *"Measurements of the reaction-diffusion front of model chemically amplified photoresists with varying photoacid size,"* Macromolecules 39, 8311-8317 (2006).

A. Rao, S. Kang, B. D. Vogt, V. M. Prabhu, E. K. Lin, W. Wu, and M. Muthukumar, *"Effect of Deprotection Extent on Swelling and Dissolution Regimes of Thin Polymer Films,"* Langmuir 22, 10009-10015 (2006).

S. Kang, V. M. Prabhu, B. D. Vogt, E. K. Lin, W.-L. Wu, K. Turnquest, *"Copolymer fraction effect on acid catalyzed deprotection reaction kinetics in model 193 nm photoresists,"* Polymer, 47(18),6293-6302 (2006).

V. M. Prabhu, S. Sambasivan, D. A. Fischer, L. Sundberg, and R. D. Allen, *"Quantitative depth profiling of photoacid generators in photoresist materials by near-edge X-ray absorption fine structure spectroscopy,"* Applied Surface Science 253(2), 1010-1014 (2006).

B. D. Vogt, C. L. Soles, C.-Y. Wang, V. M. Prabhu, P. M. McGuiggan, J. F. Douglas, E. K. Lin, W.-L. Wu, S. K. Satija, D. L. Goldfarb, M. Angelopoulos *"Water immersion of model photoresists: interfacial influences on water concentration and surface morphology,"* Journal of Microlithography, Microfabrication, and Microsystems, 4(1), 013003 (2005).

V. M. Prabhu, B. D. Vogt, W.-L. Wu, E. K. Lin, J. F. Douglas, S. K. Satija, D. L. Goldfarb, and H. Ito, *"Direct measurement of the counterion distribution within swollen polyelectrolyte films,"* Langmuir 74, 6647 (2005).

Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, critical dimension and overlay measurement improvements have barely kept up with lithography capabilities. To maintain cost effectiveness, continued advances need to be made.

Wafer-Level and Mask Critical Dimension Metrology

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason, the project is presented in a number of sub-sections, each focusing on a single technology. These are:

- Model-Based Linewidth Metrology
- Scanning Electron Microscope-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Optical-Based Photomask Dimensional Metrology
- Scatterometry-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Dimensional Metrology with Grazing Incident X-Ray Scattering
- Atom-Based Dimensional Metrology
- Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Model-Based Linewidth Metrology

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth and line edge roughness metrology with uncertainties on the order of 1 nm as required by the industry roadmap.

Customer Needs

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, with projected worldwide sales of $273.8 billion in 2007 [Semiconductor Industry Association projection, Feb. 2, 2007]. As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with linewidth or gate width.

To support present and future semiconductor technologies, industry needs to measure gate electrode widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of less than 2.5 nm and with measurement precision (3 standard deviation repeatability) better than 0.5 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level. In addition to measuring linewidths, the semiconductor industry has needs for measuring linewidth *variation*, that is, linewidth roughness (LWR). LWR in transistor gates has been linked to increased off-state leakage current and to threshold voltage variation. The 2006 ITRS update specifies that LWR, measured as three standard deviations of the CD, must be less than 2 nm in 2007 and be measured with better than 0.4 nm precision.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices. Barriers to accurate LWR measurement include random errors due to noise or sampling and poorly understood measurement artifacts such as measurement bias that comes from treating random edge assignment errors as a component of roughness (a false "noise roughness").

Technical Strategy

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have developed a model-based library method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works by describing edge geometry with a set of parameters (*e.g.*, sidewall angle, corner radius, edge positions). The expected images for a range of parameter choices are calculated using a Monte Carlo algorithm (called MONSEL) that simulates electron trajectories. The resulting actual shape/calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match (Fig. 1, next page). The corresponding line shape is assigned to the unknown. In practice there may be more than two parameters, and the library is interpolated.

Technical Contact:
J. Villarrubia

"Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD SEM measurements."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2005).

"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline."

International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2005).

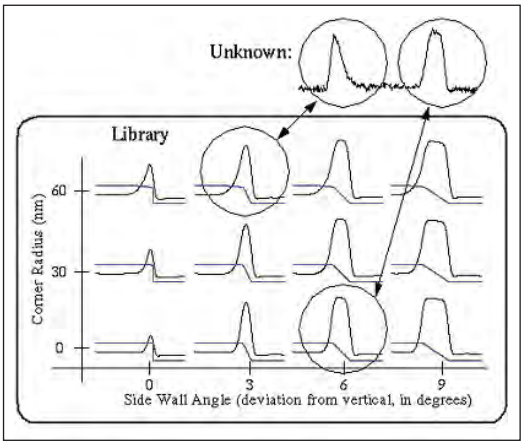

Figure 1. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

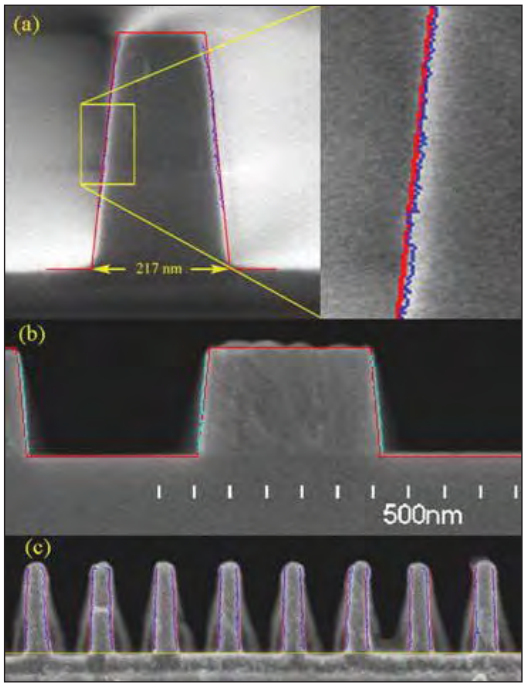

Figure 2. Agreement between MBL and cross-section measurements (a) for isolated polycrystalline ("poly") Si lines in which top-down measurements were performed with a laboratory SEM, (b) for dense poly lines measured with a commercial CD-SEM, and (c) for dense UV resist lines measured with a commercial CD-SEM. In all cases the red lines are the cross sections predicted by the MBL technique based upon top-down measurements, and the blue lines are edges assigned based upon the cross sections.

In recent years we have reported encouraging results for this method. Results for polycrystalline Si are shown in Fig. 2a and Fig. 2b. Measurements like these on poly-Si are industrially relevant after etch, and are also important as a prerequisite for the calibration of wafer linewidth standards. Such standards are likely to be fabricated in Si rather than resist because resist geometry is too unstable for a long-term standard. However, a capability to measure resist would also be industrially useful for pre-etch process control measurements. The effects of contamination, charging, and shrinkage when imaging nonconducting resists may result in poorer accuracy for resist samples than for Si samples. Results for a UV resist are shown in Fig. 2c.

These prior accomplishments establish a direct link between the quality of SEM models and the accuracy of metrology that can be performed using them. In 2007, we are improving the capabilities of the underlying modeling tools used to generate libraries. The existing simulation codes are limited to certain classes of sample shapes, essentially lines uniform along their length and with cross sections characterized by a small number of geometrical parameters, *e.g.*, width, sidewall angle, and corner radius. Improvements to the modeling code will permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, and line footing (see, *e.g.*, Fig. 3). To that end, we are translating the existing FORTRAN version of MONSEL into Java and revising the sample geometrical description. Instead of the previous cross-sectional description, samples will be described as a series of 3-dimensional regions, each of which is specified by primitive shapes (plane-bounded objects, cylinders, spheres, etc.) or combinations of these. Once the 3-D version is compared and agrees with the existing version for shapes in both their repertoires, we will revisit the physics models for SE generation with a view to improving the simulation accuracy. We are encouraging further adoption of this method by CD-SEM suppliers by publication of the method, by making modeling software freely available to CD-SEM manufacturers, and by collaboration with their engineers.

DELIVERABLES:

- Translate existing scattering physics module into Java framework. 4Q 2006
- Complete the merger of existing MONSEL scattering physics into new 3-dimensional code. 1Q 2007

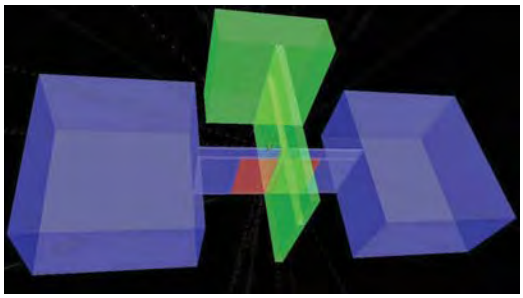

Figure 3. An overview of a FinFET model showing Si source and drain (left and right boxes), a thin connecting Si fin with HfO_2 gate oxide, and a metal (TiN) gate electrode with a crossing fin-like contact. The substrate (not shown, but coincident with the bottom of the pictured structures) is Si.

- Develop alternative SE models (*e.g.*, Gryzinski semi-classical SE generation) for inclusion in the new simulator. 2Q 2007
- Investigate sensitivity of model results to choice of model. 3Q 2007

In Atomic Force Microscopy (AFM) the issues with width determination are similar, and an analogous solution using models of the tip/sample interaction to reconstruct the sample shape is possible. We made considerable progress on this a number of years ago, developing a mathematical morphological description of the sample/probe interaction in terms of dilation, and of sample reconstruction in terms of erosion. These previous developments were limited to samples, images, and tips that could be described by single-valued surfaces (*e.g.*, images in the form of grayscale height maps). Although dilation and erosion similarly described image formation and sample reconstruction for re-entrant surfaces (*e.g.*, undercut lines) we were unable to perform calculations for such surfaces because of limitations in our software implementation. In the summer of 2006 we overcame that limitation by development of a "dexel" (depth element) representation to replace the pixel representation for images of such objects. We continue the development this year with publication of the result and demonstrations of its applicability to samples of interest in semiconductor electronics applications.

DELIVERABLES:

- Complete coauthored paper on 3-D image simulation and surface reconstruction using a dexel representation . Submit to Ultramicroscopy. 4Q 2006
- Paper on applications of Image simulation and surface reconstruction with dexels for SPIE Advanced Lithography meeting. 1Q 2007

Accomplishments

■ The 3-D geometry portions of the new Monte Carlo SEM simulator were completed in 2006. Scattering codes were completed and merged with the geometry parts early this year on schedule according to the milestones listed above. As a result, the planned 3-D simulator is currently working and under test.

■ We have improved our understanding of several physical processes, including work function barrier penetration by electrons, electron transport through dilute gases (relevant to the use of variable pressure SEM, proposed for mask metrology), and the effect of target electron binding energy upon scattering cross sections. This work is in preparation for including this improved physics in future models of SEM performance.

■ In collaboration with Applied Materials, we developed an unbiased linewidth roughness estimator suitable for use in resist measurements, where the resist shrinks during measurement. The results were published in Proceedings of the SPIE Microlithography conference.

■ The work has generated considerable interest in semiconductor and nanotechnology applications areas, leading to an invited presentation at the Micro and Nano Technology Measurement Club meeting, NPL in Teddington, England, a tutorial on "Interconnect-relevant Characterization and Metrology Techniques" at the Advanced Metallization Conference, and a colloquium at the College of Nanoscale Science & Engineering (SUNY Albany).

Collaborations

International SEMATECH, Benjamin Bunday, Michael Bishop.

Hitachi, Ltd., Maki Tanaka.

Applied Materials, R. Katz, C. D. Chase, R. Kris, R. Peltinov

Illinois Institute of Technology, Prof. Xiaoping Qian

Intel Corp

Recent Publications

X. Qian and J. S. Villarrubia, "General Three-Dimensional Image Simulation and Surface Reconstruction in Scanning Probe Microscopy using a Dexel Representation," Ultramicroscopy, in press.

"Monte Carlo modeling of secondary electron imaging in three dimensions," J. S. Villarrubia, N. W. M. Ritchie, and J. R. Lowney, submitted to Proc. SPIE **6518** (February 2007).

"Image Simulation and Surface Reconstruction of Undercut Features in Atomic Force Microscopy," Xiaoping Qian, John Villarrubia, Fenglei Tian, and Ronald Dixson, submitted to Proc. SPIE **6518** (February 2007).

"Line-edge roughness and cross-sectional characterization of sub-50-nm structures using CD-SAXS," R. L. Jones, C. Wang, E. K. Lin, W. Wu, J. S. Villarrubia, K. Choi, J. S. Clarke, and B. D. Bunday, submitted to Proc. SPIE **6518** (February 2007).

R. Katz, C. D. Chase, R. Kris, R. Peltinov, J. Villarrubia, and B. Bunday, "Bias reduction in roughness measurement through SEM noise removal," Proc. SPIE **6152**, 61524L, (2006)

J. S. Villarrubia and B. D. Bunday, *"Unbiased Estimation of Linewidth Roughness,"* Proc. SPIE **5752**, p. 480 (2005).

J. S. Villarrubia, A. E. Vladár, and M. T. Postek, *"Scanning electron microscope dimensional metrology using a model-based library,"* Surf. Interface Anal., 37, p. 951 (2005).

M. Tanaka, J. S. Villarrubia, and A. E. Vladár, *"Influence of Focus Variation on Linewidth Measurements,"* Proc. SPIE **5752**, p. 144 (2005).

J. S. Villarrubia, *"Tip Characterization for Dimensional Nanometrology,"* in Applied Scanning Probe Methods, eds. B. Bhushan, H. Fuchs, and S. Hosaka, p. 147 (Springer-Verlag, Berlin Heidelberg 2004).

Scanning Electron Microscope-Based Dimensional Metrology

Goals

Provide the microelectronics industry with highly accurate scanning electron microscope (SEM) measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron and ion optical system, detection, sample stage, and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors (2005) states that "Scanning Electron Microscopy continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and critical dimension (CD) measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 45 nm generation." The semiconductor industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research of the signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 65 nm or less with a very high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of the minimum feature size, known as CD, are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is key microscopic technique used for this sub-100 nm metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project, a multidimensional project, is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). Conventional optical lithography provides a chance for large amount of good quality samples produced inexpensively. Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm. In order to make this artifact available (while the final certification

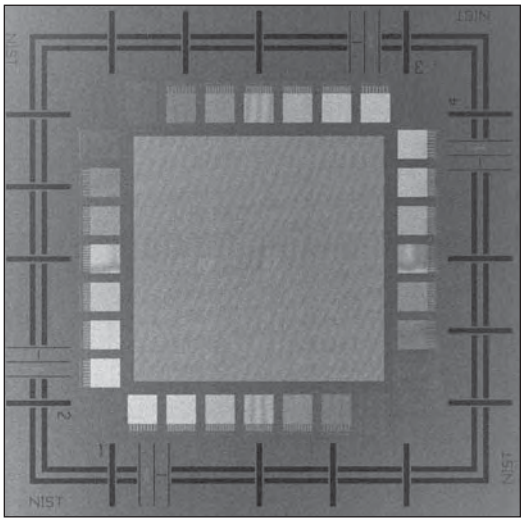

Figure 1. SEM image of the complete RM 8090 Magnification calibration standard reference material.

Technical Contacts:
A. E. Vladar
J. S. Villarrubia
M. T. Postek

"Scanning Electron Microscopy (SEM) – continues to provide at-line and in-line imaging … and CD measurements. Improvements are needed … at or beyond the 45 nm generation … Determination of the real 3-D shape…will require continuing advances in existing microscopy …"

International Technology Roadmap for Semiconductors, 2007

details are being completed) the artifact will be released as Reference Material (RM) 8090A.

DELIVERABLES:

- Development of a new metrology SEM based on a variable pressure instrument. This instrument will be able to work with full size wafers and photomask. 4Q 2007
- Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples. 4Q 2007
- Upon availability of suitable quality samples, quality assessment and delivery of a batch of RM 8120. 4Q 2007
- Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2120 samples. 4Q 2007

2. SEM Performance Measurement Artifacts and Software Solutions: This effort included the development of the Reference Material 8091 (Fig. 2.) and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. Currently we are working with ISO to develop robust software solutions that will allow for resolution performance tracking of SEMs. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. As a part of this effort the NIST SEM Resolution Measurement Reference Image Set was worked out to test the resolution measurement software themselves. This Reference Image Set contains a large number of artificial images that were made by taking onto account the amount and type of de-focusing, noise, vibration and drift and electron landing energies. Suitable samples are being sought to further improve this type of metrology (Fig. 3). Several samples have been purchased by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

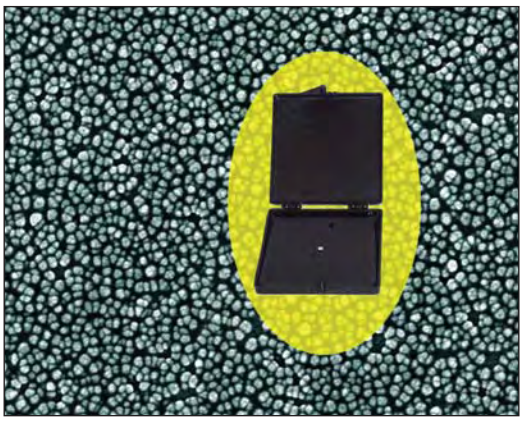

Figure 2. The RM 8091 Sharpness Reference Material.

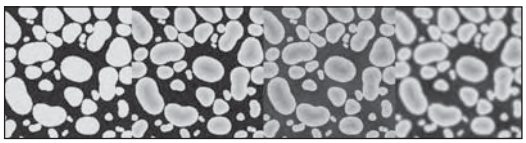

Figure 3. Images that illustrate the image simulation steps for the NIST SEM Resolution Measurement Reference Image Set.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time, the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with a few nm of accuracy. In several publications, NIST demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 1 mm to down to 50 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

A new effort is under way that is aimed at the development of two new Reference SEMs. One with full-size wafer and mask capability is based on an environmental SEM (ESEM), which is very advantageous with charging samples such as quartz masks. The other Reference instrument based on a dual-beam SEM, and will be capable

to work with mask- and smaller size samples. Both microscopes will use the same type of 38 pm resolution laser interferometry, which provides traceability and it allows for the compensation for stage drift and vibration at the nm level.

DELIVERABLES:

- Design and preparation of line width metrology immerse litho artifact suitable for calibration on NIST and external measuring systems for certification of wafer format line width samples. 3Q 2007
- Completion of preliminary measurements on immerse litho samples made by SEMATECH with the new "NISTMAG" metrology mask. 4Q 2007

4. Helium Ion Microscopy – a Promising New Technique for Semiconductor Metrology: The Helium Ion Microscope (HIM) offers a new, potentially disruptive technique for nano-metrology. This methodology presents an approach to measurements for nanotechnology and nano-manufacturing which has several potential advantages over the traditional scanning electron microscope (SEM) currently in use in integrated circuit research and manufacturing facilities across the world. Due to the very small, essentially one atom size, very high brightness source, and the shorter wavelength of the helium ions, it is theoretically possible to focus the ion beam into a smaller probe size relative to that of an electron beam of current SEMs. Hence higher resolution is theoretically achievable. In contrast to the SEM, when the helium ion beam interacts with the sample, it generates significantly smaller excitation volume and thus the image collected is more surface sensitive. Similarly to the SEM, the HIM also produces topographic, material, crystallographic, and potential contrast, and offers ways for investigating new properties of the sample through the use of various detectors. Compared to an SEM, the secondary electron yield is quite high, allowing for imaging at very low beam currents, thus resulting in less sample damage. Additionally, due to their low mass, the helium ions themselves do not significantly alter the sample, which would be common, for example, for gallium ions that are regularly used for ion milling. This development work is at its beginning the first-in-the-world HIM arrived at NIST in May 2007.

DELIVERABLES:

- Installation of the new HIM, design and preparation of measurement plan that addresses all important imaging and metrology parameters of the HIM. 3Q 2007
- Completion of preliminary measurements and quality assessment of the imaging capability of the HIM using amorphous Si immerse litho samples made by SEMATECH. 4Q 2007

ACCOMPLISHMENTS

■ **SEM Magnification Calibration Artifacts –** Samples for Reference Material 8090 have been made in the past successfully, but later several attempts with e-beam lithography yielded no further useful samples. We delivered to NIST Office of Reference Materials 100 pieces of RM 9080A, which were fabricated at International SEMATECH using 193 nm UV light lithography. The finest features are 100 nm wide with a 200 nm pitch. The largest pitch is 1500 μm. There are a large number of 250 nm wide crosses and grids for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from polySi material. These samples give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. The fabrication of the first large batch of samples has been finished in the summer of 2006. With the arrival of the new metrology SEM and its laser interferometer sample stage these will be calibrated.

■ **SEM Performance Measurements –** After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. There have been 75 samples delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is under way to produce more of these samples. These samples are now available to the public, and many of them are already in use.

■ **SEM Linewidth Measurement Artifacts –** For correct linewidth measurements accurate modeling methods are indispensable. The existing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view and using our high-accuracy modeling and fitting

methods, a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of the SEMATECH/NIST mask has been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All of these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2007 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

■ **Development of High Accuracy Laser Interferometer Sample Stage for SEMs –** The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.04 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 4 illustrates the short-term motion of the sample stage, the left side of the figure depicts the location of the stage and the right side is the density distribution of the location of the stage during 1 minute of dwell time. The field-of-views are 2 nm for all images. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality.

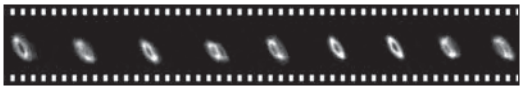

Figure 4. Short-term motion of the SEM sample stage, the stage location (left) and its density distribution during a 1 minute of dwell time, 2 nm field-of-views.

Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and the characterization of various settings and fine tuning of the sample stage, which is critical for high-resolution work.

■ **Development of Line Edge Roughness Metrology for Integrated Circuit Technology –** The measurement of line-edge roughness (LER) has become an important topic in the metrology needed for the semiconductor industry. NIST has successfully developed various LER metrics and methods to make reliable and statically sound LER measurements. The findings have impact on the ITRS as they call for longer lengths for LER evaluation and on LER metrology in general because the new methods offer significantly better metrology than what was available previously. The final report of a year-long study was delivered on time to SEMATECH.

■ **Development of Ultra-High Resolution He ion Microscope –** The HIM technology is not yet as optimized, developed or as mature as the SEM. As a new technique, HIM (Fig. 5) is just beginning to show promise and the plethora of potentially advantageous applications for integrated circuit and nanotechnology have yet to be exploited. Now that commercial instrumentation is available, further work can be done on the fundamental science of helium ion beam generation, helium ion beam-specimen interactions, and the signal generation and contrast mechanisms defining the image.

In addition to these areas of work, modeling needs to be developed to correctly interpret the signal generation mechanisms and to understand the imaging mechanisms. These are indispensable for accurate nanometer-level metrology. HIM and SEM have some overlapping territory, but they remain complementary techniques. Helium ion beam microscopy is forging into new scientific

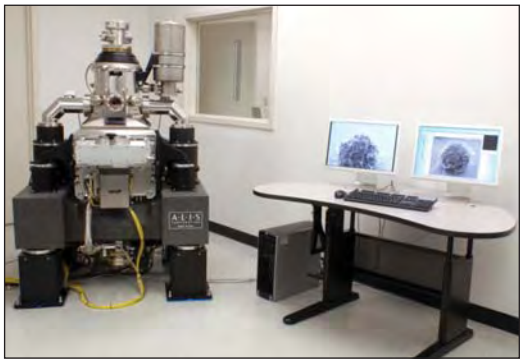

Figure 5. Alis/Zeiss He ion microscope.

and technology territories, and this new and innovative technology will develop new science and contribute to the progress in integrated circuit and nanotechnology. This development work is at its beginning, the first-in-the-world HIM has arrived at NIST in May 2007.

Collaborations

International SEMATECH, Advanced Metrology Advisory Group

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections

Zeiss/ALIS Corp

FEI Co.

ISO

Recent Publications

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A. E. Vladar, Z. Radi, M. T. Postek and D. C. Joy, *"Nanotip Electron Gun for the Scanning Electron Microscope,"* Scanning 2006.

A. E. Vladar, R. Silver, J. Potzick, J. S. Villarrubia and M.T. Postek *"2004 Development of Photomask Artifacts and Metrology Methodology for the 65 nm Device Generation with Extensibility Beyond"* SEMATECH Final Report.

A. E.Vladar, J. S. Villarrubia, R. Dixson., T. Vorburger., N. G. Orji., B. D. Bunday, and M. Bishop, *"Line Edge Roughness Metrology for Integrated Circuit Technology,"* Final Report to International SEMATECH (March 2004).

A. E. Vladar, E. C. Jayewardene, B. N. Damazo, W. J. Keery, and M. T. Postek, *"Laser Sample Stage-based Image Resolution Enhancement Method for SEMs,"* SPIE 2004 5375-181.

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Scanning Probe Microscope-Based Dimensional Metrology

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J. Fu

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in scanning probe microscope-based measurements. *The International Technology Roadmap for Semiconductors (ITRS)* identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2006 update, the goal in 2007 for critical dimension (CD) measurement precision for isolated lines was ± 0.52 nm; this demand tightens to ± 0.29 nm by 2012.

Although most in-line metrology is performed using scanning electron microscope (SEM) and scatterometry, these instruments are not presently capable of first-principles accuracy. That is, they must be calibrated using reference measurements from a tool or combination of tools which is capable of intrinsic accuracy. Such a tool is now referred to as a reference measurement system (RMS), and the 2006 update of the *ITRS* highlights the growing importance of an RMS. The use of atomic force microscope (AFM) and transmission electron microscope (TEM) cross section for this purpose – often in combination – is now a fairly common practice in the industry.

The technical focus of this project, development and implementation of scanned probe microscope instrumentation for traceable dimensional metrology, is thus driven by the anticipated industry needs for reduced measurement uncertainty for in-line metrology tools such as the SEM and scatterometer – since these in turn rely on reduced measurement uncertainty for techniques such as AFM that are often implemented as an RMS.

Customer Needs

The SEM is still the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. Scatterometry or optical critical dimension (OCD) metrology is also rapidly gaining acceptance as an in-line process metrology tool. Scanning probe microscopes (SPMs) possess unique capabilities, which may significantly enhance the performance of SEMs for in-line CD measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, the availability of traceable pitch, height, and width standards in this regime is limited.

Technical Strategy

The SPM dimensional metrology program consists of three inter-related thrusts: The first two thrusts address SPM dimensional metrology with two in-house research instruments at NIST, and the third thrust involves a partnership with SEMATECH to maintain traceability on a commercially available in-line SPM housed in the manufacturing facility at SEMATECH. The two instruments housed at NIST are a calibrated atomic force microscope (C-AFM) for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of line width.

The C-AFM is a custom built instrument that has metrology traceable to the wavelength of light for all three axes of motion, and it has provided calibrated pitch and height measurements for a variety of nano-scale applications. Pitch measurements in the micrometer regime and below can currently be performed with relative standard uncertainties as low as 5×10^{-4}, and step height measurements up to several hundred nanometers can be performed with a relative standard uncertainty approaching 1×10^{-3}. The C-AFM has participated in two international comparisons of sub-micrometer pitch measurements and one comparison of step height measurements.

DELIVERABLES:

- Completed refinement of uncertainties – to reduce by approximately a factor of two - and amended report on two-dimensional pitch measurements using C-AFM as NIST participation in NANO5 – an International Supplementary Key Comparison in Nanometrology. 4Q 2006

- Performed CD-AFM measurements, using the SXM320 at NIST, on trial chips from 200 mm bulk Si (110) wafer to evaluate potential as an alternative starting material for the single crystal critical dimension reference material (SCCDRM) project. 4Q 2006
- Performed CD-AFM measurements, using the SXM320 at NIST, on next generation single crystal critical dimension reference material (SCCDRM) samples for phase 2 of the process optimization (confirmation and refinement) experiment in collaboration with EEEL and ITL. 1Q 2007
- Presented paper describing results of the process optimization experiment for the "next generation" of single crystal critical dimension reference materials (SCCDRM) at SPIE Advanced Lithography Meeting. 2Q 2007
- Presented paper describing a comparison between the calibration of the SCCDRM samples and similar commercially available linewidth standard at SPIE Advanced Lithography Meeting. 2Q 2007
- Presented paper comparing two methods of TEM reference metrology – HRTEM and HAADF-STEM - for CD-AFM tip width calibration at SPIE Advanced Lithography Meeting. 2Q 2007
- Organized, hosted, and ran an evening workshop on the history and future of CD standards at the SPIE Advanced Lithography Meeting. 2Q 2007
- Participate in joint NIST-SEMATECH workshop on OCD standards – in regard to traceability and AFM reference metrology – at SEMICON West. 3Q 2007

The second and third thrusts involve the most commonly used AFM-based method of linewidth metrology in industry: CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. The SXM320 is a prior generation commercially available CD-AFM. Initially, this instrument was used to implement the CD-AFM RMS at SEMATECH during the tenure of Ronald Dixson as the first NIST Guest Scientist there. Now that the instrument is housed at NIST, the uncertainties have been further refined. Currently, pitch measurements can be performed with a relative standard uncertainty of approximately 2×10^{-3}. Step height measurements have a relative standard uncertainty 4×10^{-3}, and linewidth measurements can have standard uncertainties as low as 1 nm. This is a result of the most current release of NIST single crystal critical dimension reference materials (SCCDRM) that was completed in 2005.

The third thrust involves collaboration with SEMATECH to maintain a traceable CD-AFM (RMS) in the manufacturing facility there. This thrust is currently overseen by George Orji who is now the second NIST Guest Scientist at SEMATECH. A current generation CD-AFM, the Veeco Dimension X3D, is now being used to implement the RMS. As is true for the SXM at NIST, the SCCDRM project has resulted in the ability to perform linewidth measurements with a standard uncertainty of 1 nm. The relative uncertainties in pitch and height measurements have been recently reduced to 1×10^{-3} and 2×10^{-3}, respectively.

DELIVERABLES:

- Presented paper comparing two methods of TEM reference metrology – HRTEM and HAADF-STEM - for CD-AFM tip width calibration at SPIE Advanced Lithography Meeting. 2Q 2007
- Publish a joint paper with major semiconductor manufacturer on use of CD-AFM reference metrology to evaluate the performance of in line FIB cross sections at EIPBN conference. 2Q 2007
- Complete a report on the refinements and extensions of the CD-AFM reference measurement system (RMS) for SEMATECH. 3Q 2007

Accomplishments

■ The NIST/SEMATECH partnership in advancing AFM metrology in semiconductor manufacturing continues. George Orji is now in the third year of his tenure as the second NIST Guest Scientist at SEMATECH, following a three year tenure of Ronald Dixson as the first NIST Guest Scientist. George has continued the NIST engagement with SEMATECH by supporting their SEM and scatterometer benchmarking activities with the RMS, and he has overseen the reduction of pitch and height uncertainties by approximately a factor of two.

■ We are collaborating with other NIST researchers and external partners such as SEMATECH, Intel, and IBM to develop linewidth standards and CD reference metrology. A major component of this effort has been the single crystal critical dimension reference materials (SCCDRM) project initiated by NIST researchers in EEEL (Cresswell and Allen). In late 2004, we completed a release of SCCDRMs to SEMATECH and its member companies, and CD-AFM dimensional metrology played a central role. The measurements on the SCCDRM samples were performed by NIST scientist Ronald Dixson using the X3D at SEMATECH which had been implemented as a CD-AFM reference measurement system (RMS) for traceable measurements of pitch, height, and width. High resolution transmission electron

microscopy (HRTEM) was used as an indirect method of tip width calibration for the SCCDRM samples. The AFM and HRTEM results that were used for the tip calibration are shown in Fig. 1. Features on the distributed samples ranged in width from approximately 50 nm to 250 nm with expanded uncertainties of about 2 nm (k = 2) on most features.

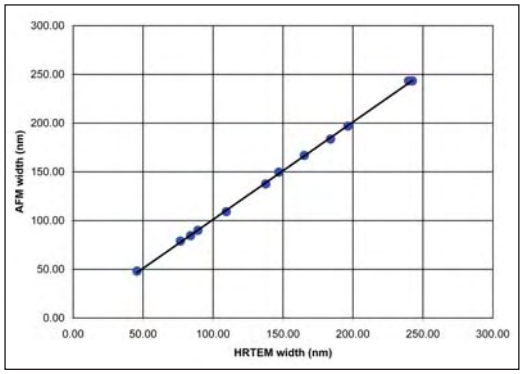

Figure 1. Regression of CD-AFM width values on HRTEM values. The observed slope is consistent with unity – indicating that the two methods have consistent scale calibration. The average offset between the results was used to correct the tip width calibration.

■ As a result of this project, CD-AFM linewidth measurements can now be performed with a 1 nm (k = 1) standard uncertainty. This standard for width calibration is now being used on both the X3D and the SXM at NIST. An image of an SCCDRM taken on the SXM320 is shown in Fig. 2. In 2005, we launched the "next generation" of the SCCDRM project and are currently performing a series of designed experiments to further improve the performance characteristics of the SCCDRMs – including linewidth uniformity.

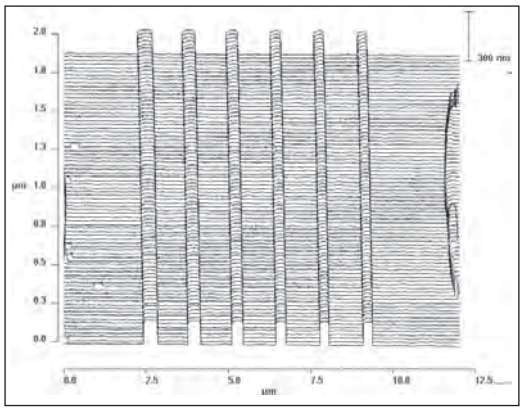

Figure 2. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration. Measurements performed by R. Dixson, sample developed by M. Cresswell and R. Allen.

In the first phase of these experiments, we have observed feature widths as low as 20 nm with uniformity at the 1 nm level.

■ We have used the C-AFM to participate in a series of International Supplementary Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of traceable measurements of dimensional quantities important to the semiconductor industry. We have previously participated in comparisons of step height and one dimensional pitch measurements. The results of these comparisons have now been published under the Mutual Recognition Arrangement (MRA) through which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. During 2005, we participated in a comparison of two dimensional pitch measurements: the C-AFM was used to measure both a 300 nm and 1000 nm grating. An example of a C-AFM image on the 1000 nm grating is shown in Fig. 3. A similar comparison of linewidth measurements is currently being planned and will be led by NIST.

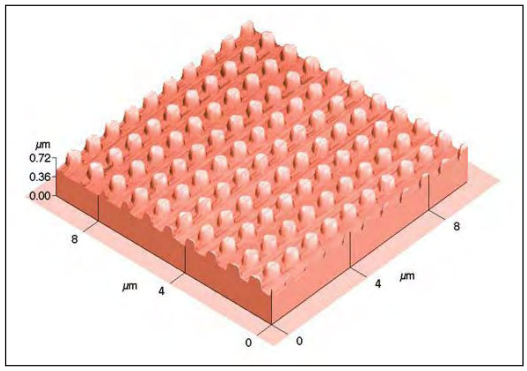

Figure 3. An image of a 1000 nm pitch grating taken using the C-AFM as part of an international comparison of two dimensional pitch measurements.

■ Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2004 we developed a draft standard for AFM z-calibration using the single atom steps for the ASTM Subcommittee E42.14 on STM/AFM. This draft standard is still being revised and undergoing review within the subcommittee.

■ We are also developing a technique for AFM linewidth metrology based on image stitching. This involves the acquisition of paired images using a carbon nanotube probe. The nanotube tip

enables data acquisition at high resolution on one side of the line in each image, and the specimen is rotated 180 degrees between the two measurements. Stitching these two images into a composite offers the potential of accurate linewidth metrology. We have completed two generations of an experiment in which the stitching result is compared with CD-AFM. The composite image used in one of our published comparisons between image stitching and CD-AFM is shown in Fig. 4. Currently, we are assessing the uncertainties and continuing to develop this approach.

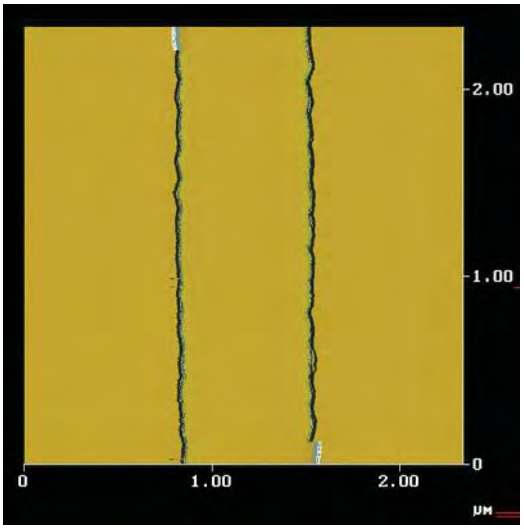

Figure 4. Stitched composite slope image from two images of a linewidth sample taken with a carbon nanotube tip. Measurements performed by J. Fu; sample developed by M. Cresswell and R. Allen; probe developed by C. Nguyen of ELORET/NASA Ames.

■ We continue to refine the CD-AFM RMS at SEMATECH and bring its traceable measurement capabilities to bear on semiconductor manufacturing applications. During the tenure of both NIST Guest Scientists at SEMATECH, we have used this RMS system to provide reference metrology for both SEM and scatterometer benchmarking, measurements of SEM-induced shrinkage of 193 nm photoresist, and to provide reference metrology for evaluation of several new optical methods for measurement of photomasks.

■ In the SEM benchmarking applications, our basic methodology is to perform both CD-AFM and SEM measurements on a series of features on a focus exposure matrix that spans a process window. This approach means that both tools see features that have a range of widths as well as secondary characteristics such as sidewall angle and corner rounding. A regression of the AFM/SEM data allows the SEM to be checked for bias, scale calibration, and linearity of response across the FEM. An example of a SEM/AFM regression using measurements of isolated polysilicon lines is shown in Fig. 5. SEMATECH and its members place high value on SEMATECH's tool benchmarking activities and the support these activities receive from the NIST-supported CD-AFM RMS.

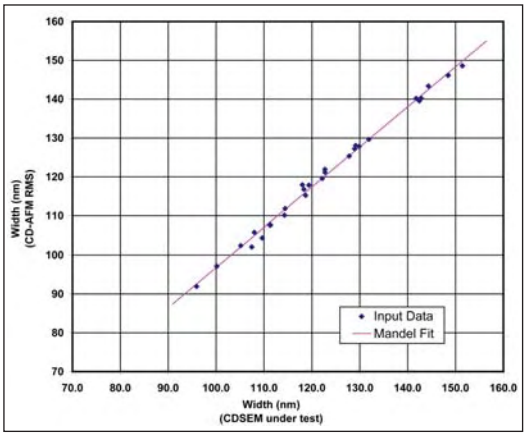

Figure 5. An example of an AFM/SEM regression performed as part of a SEMATECH benchmarking activity during the tenure of Ronald Dixson as the first NIST Guest Scientist at SEMATECH. The measurements were performed on isolated etched polysilicon lines that spanned a wide process window focus exposure matrix. The Mandel regression allows for uncertainty in both variables and is the most appropriate way to compare a tool under test with the reference measurement system. In this example, the SEM performance is very good and exhibits a bias of only 3 nm and linearity within the uncertainties of the comparison.

Collaborations

Intel Mask Operations, Santa Clara, CA

Intel, Hilllsboro, OR

Intel, Santa Clara, CA

SEMATECH, Austin, TX

Veeco Metrology, Santa Barbara, CA

IBM Burlington, VT

IBM Almaden Research Center, San Jose, CA

ELORET Corp./NASA Ames Research Center, Moffett Field, CA

Departments of Mechanical Engineering and Chemistry, University of North Carolina, Charlotte, NC

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China

Recent Publications

N. G. Orji, R. G. Dixson, *"Higher Order Tip Effects in Traceable CD-AFM Based Linewidth Measurements,"* Meas. Sci. and Technol. Vol. 18, 448-455 (2007).

N. G. Orji, R. Dixson, B. D. Bunday, J. A. Allgair, *"TEM Calibration Methods for Critical Dimension Standards,"* SPIE Proceedings Vol. 6518, 651810 (2007).

B. Bunday, J. Allgair, E. Soleck, C. Archie, N. G. Orji, J. Beach, O. Adan, R. Peltinov, M. Bar-zvi, J. Swyers, *"The coming of age of tilt CD-SEM,"* SPIE Proceedings Vol. 6518, 65181S (2007).

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N. G. Orji, M.I. Sanchez, J. Raja, and T. Vorburger, "AFM Characterization of Semiconductor Line Edge Roughness," in *Applied Scanning Probe Methods*, edited by B. Bhushan, H. Fuchs, and S. Hasaka (Springer Verlag, Berlin, 2004) p. 273.

B. D. Bunday, M. Bishop, D. McCormack, J. S. Villarrubia, A. E. Vladar, R. Dixson, T. Vorburger, N. G. Orji, J. A. Allgair, *"Determination of Optimal Parameters for CD-SEM Measurement of Line Edge Roughness,"* SPIE Proceedings Vol.. 5375 (2004).

R. Dixson and A. Guerry, *"Reference Metrology Using a Next generation CD-AFM,"* SPIE Proceedings Vol. 5375, 633-646 (2004).

X. Zhao, J. Fu, W. Chu, C. Nguyen, and T. Vorburger, *"An Image Stitching Method to Eliminate the Distortion of the Sidewall in Linewidth Measurement,"* SPIE Proceedings Vol. 5375, 363 -373 (2004).

Optical-Based Photomask Dimensional Metrology

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements.

Accurate feature size metrology on binary photomasks (constituting 85 % of current mask production) becomes increasingly difficult as critical features shrink and their optical proximity correction cousins proliferate. Phase shift and EUV masks present additional challenges.

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay errors on the wafer and accurately measuring image placement of features on the photomasks. Overlay control is listed in multiple sections of Table 116 of the 2005 SIA ITRS as a difficult challenge for <32 nm processes. Overlay metrology and photomask feature placement metrology have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table 119a shows that there are current image placement and overlay control challenges with no known solutions for photomask image placement metrology beyond the 65 nm node. As shown in Table 119b, the problems are more acute for long term photomask CD metrology where the industry will soon be encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are two main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. NIST's current chrome-on-quartz photomask linewidth standard, SRM 2059, (Fig. 2, next page) contains isolated linewidth and spacewidth features in the range of 0.25 µm

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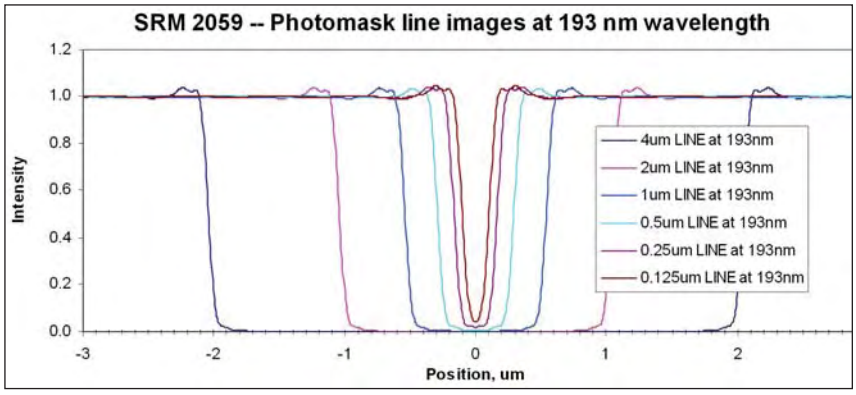

Figure 1. Modeling results for isolated binary photomask lines from 4µm to 0.125µm.

to 32 µm, whose widths have been measured and certified to an uncertainty of ~20 nm at the 95 % confidence level.

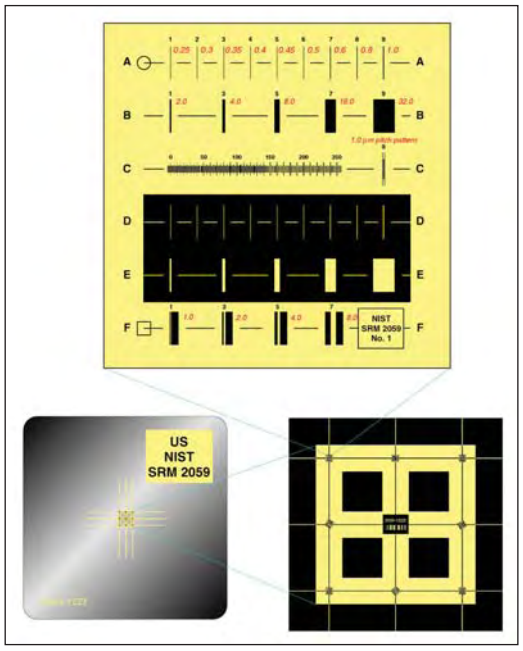

Figure 2. NIST SRM 2059 Photomask Linewidth Standard. Isolated linewidths and spacewidths range form 0.250 um to 312 um.

In response to customers' needs for more accurate photomask feature size measurements, NIST has worked extensively to improve mask metrology through optical image modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. In response to these problems, NIST introduced the Neolithography concept 1997: Modeling the effects of all of the relevant feature properties in both the mask metrology process and the wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes. This concept (at least in part) can be seen today in the design for manufacturing (DFM) sector of the industry.

DELIVERABLES: Compare and improve the accuracy of the NIST optical scattering code with new scattering models developed by Spectel and JCMwave for use in transmission. 4Q 2007

2. The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which is now available as a NIST Standard Reference Material, # 5001. The artifact can be used by the semiconductor industry to standardize 2-D measurements. The SRM 5001 was developed as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements.

A new generation of grid for the SRMs has been fabricated and another round of measurements is in process. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on the new Nikon 5i two-dimensional metrology tool at NIST. The Nikon 5i has been fully characterized and is now a calibration tool for grid calibrations. In response to industry needs, this tool is now under development for use as a wafer calibration tool for large distance position-to-position wafer calibration.

To strengthen the foundation of NIST's linewidth measurement traceability and to support the Bureau International des Poids et Mesures (BIPM) *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES:

- Develop a new set of comparator algorithms to enable the SRM 5001 calibrations to be completed with the Nikon 5i tool in collaboration with the industry Ipro system. Complete the comprehensive analysis capabilities for centerline and edge detection methods with a complete uncertainty statement. 2Q 2007
- Implement the standard scale correction and new mapping software for the Nikon 5I system. Measure the new set of two-dimensional calibration grids with a complete uncertainty. 1Q 2007
- Complete the second round of calibrations of SRM 5001 and complete the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 2Q 2007

ACCOMPLISHMENTS

■ SRM 2800 Microscope Magnification Standard is a standard-size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock has been sold.

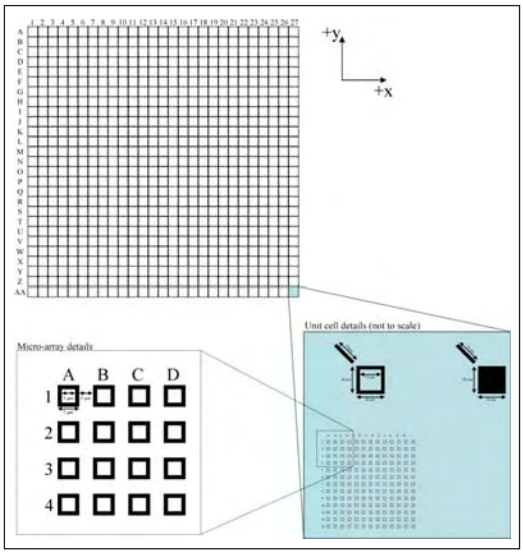

Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

■ The first set of two-dimensional grid artifacts, known as SRM 5001, were delivered to the SRM office and are selling well. These 6-inch photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. A second set of re-designed 6-inch feature placement standards has now been measured and fully calibrated in the close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4). The uncertainty budget for grid measurements and all documentation has been delivered to the SRM office and the second set of calibrated photomask grids will now be made available as a calibrated SRM.

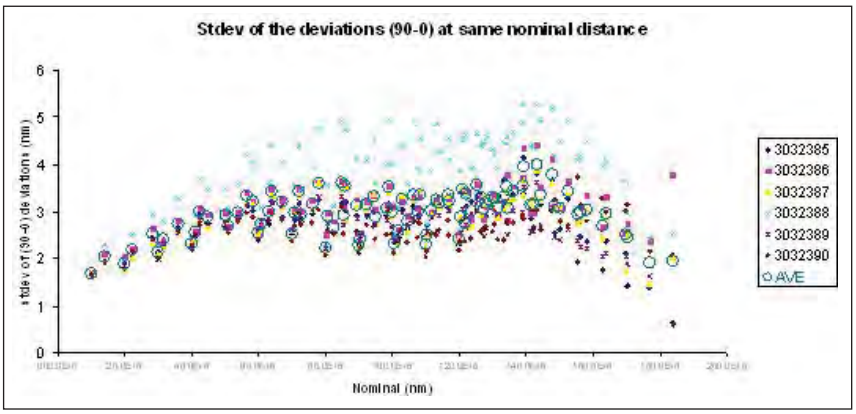

Figure 4 shows tool repeatability and mapping data for the two-dimensional mask calibration procedure.

■ In close collaboration with SEMATECH, we have completed a comprehensive report using optical methods for the calibration of phase shifting photomasks. This includes modeling and measurements in transmission and reflection. This document is available through SEMATECH as a tech transfer document.

■ A comprehensive suite of two dimensional calibration methods for the calibration of optical systems and illumination systems is being developed based on the SRM 5001 grid calibration methodology. Some of these results were recently published at SPIE Microlithography. These methods are enabling a substantially improved optical calibration and alignment sequence as well as improved modeling inputs for more accurate linewidth measurements.

Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

Dr. Mark Davidson, Spectel Research Corp.

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Scatterometry-Based Dimensional Metrology

Technical Contact:
T. Germer

Goals

Our goals are to: (1) increase the effectiveness of scatterometry and other optical critical dimension (OCD) methods by providing industry with new measurement techniques, improved modeling, and standards; (2) provide assessments of accuracy and sensitivity of various OCD methods; and (3) develop facilities to accurately assess OCD targets. Develop improved OCD methods for assessing critical dimension and overlay.

Customer Needs

Scatterometry is increasingly becoming a preferred method for online critical dimension (CD) metrology. The method relies upon measurements of the reflectance or diffraction of small test grating structures as functions of angle, wavelengths, and/or polarization. By comparing measurement results with an extensive library of theoretical simulations or by performing a real-time regression analysis, tools can extract such line profile parameters as critical dimension, sidewall angle, and height, as well as more detailed descriptions of the sidewall shape.

While scatterometry has gained significant acceptance, it is continuing to grow in utility. However, there are many issues that remain that prevent it from having absolute accuracy. For example, the effects of finite illumination, finite target array size, line-edge and line-width roughness, uncertainties in the optical properties of the materials in the structure, neglect of surface oxides or other layers, radiometric accuracy, and the integrity of the theoretical model all contribute to the final measurement uncertainty in ways that are at this time poorly understood.

Ultimately, the industry needs reference artifacts that can test the validity of the results obtained by scatterometry tools. Such an artifact might consist of a set of gratings that have been characterized by a variety of techniques, including scatterometry, scanning electron microscopy (CD-SEM), atomic force microscopy (CD-AFM), and transmission electron microscopy (TEM). Scatterometry provides an independent method compared to the others, and if a comprehensive uncertainty budget were developed for the method, it would substantially improve the overall state of dimensional metrology.

Technical Strategy

There are three major strategies for improving the effectiveness of scatterometry. One strategy is to develop efficient models for the diffraction of light by structures on surfaces, so that NIST has state-of-the-art capabilities to perform scatterometry measurements and analysis as well as to provide standard data for a variety of model structures. The second strategy is to assess the sensitivity and accuracy of scatterometry methods to different structures, in order to provide industry with an understanding of what determines the ultimate sensitivity and accuracy of the methods. Finally, the third strategy is to develop in-house measurement capabilities with the long-term goal to perform scatterometry measurements on reference materials, to perform inter-laboratory comparisons, and to further develop the scatterometry technique.

Specific project elements are defined below:

1. Theoretical Scatterometry Modeling – Rigorous coupled wave (RCW) based theories are the most common methods used to analyze scatterometry data. We have developed in-house capability to perform RCW calculations from arbitrary two-dimensional periodic structures consisting of isotropic materials. These codes are being used to generate libraries for profile extraction as well as test calculations to assess the sensitivity of scatterometry to changes in model parameters or to non-ideal target profiles. Extensions to this capability are required to assess the effects of line-edge and line-width roughness and material anisotropy, as well as to perform RCW calculations on three-dimensional structures, such as contact holes. Building upon the ScatMech library of codes that have been made available on the web for diffuse scattering calculations, we intend to publish these codes.

DELIVERABLES:

- Publication of theory for anisotropic lines. 3Q 2007
- Publication of two-dimensional RCW code in the ScatMech library. 3Q 2007

2. Assessment of Accuracy and Precision of Scatterometry – Scatterometry relies heavily on prior knowledge of the specific structure being examined. For example, optical properties of all incorporated materials are required for the

simulations. Reasonable parameterization of sidewall profiles are required to yield meaningful profiles. Two dimensional structures are assumed to not exhibit line-edge or line-width roughness. In this program element, we are assessing the impact that each model parameter has on the outcome of the measurement. The goal is to establish an independent uncertainty budget that includes all sources of random and systematic uncertainties. Furthermore, we are assessing the sensitivity limits of scatterometry, to determine how far into the future scatterometry tools can provide critical dimension metrology. A report was made to SEMATECH outlining the methods used to determine the sensitivity and applying that methodology to two simple structures.

DELIVERABLES:

- Perform study of the limits of scatterometry precision and accuracy for several process-relevant gratings. 3Q 2007
- Develop method for assessing systematic uncertainties arising in scatterometry. 3Q 2007
- Publish computer program for assessing sensitivity and uncertainty in arbitrary scatterometers. 2Q 2008

3. Scatterometry Measurements – We have recently upgraded our laser-based Goniometric Optical Scatter Instrument (GOSI), Fig. 1, used for diffuse scatter measurements, to perform scatterometry measurements on industry-relevant targets on 300 mm wafers. The measurement capabilities include angle-scanned scatterometry at a number of discrete laser wavelengths. This instrument has the capability to perform conical scatterometry measurements and will be used to perform traditional measurements as well as measurements of higher-order, non-specular diffraction and diffuse scatter. A long term goal is to develop reference scatterometry targets, measure them with this instrument, provide accurate determinations of their dimensions and profiles, and have an uncertainty placed on the results. Another long term goal is to develop novel measurement modalities that improve the utility of scatterometry. One method we have demonstrated is microscope-based scatterometry using back focal plane imaging. This technique enables collection of multiple diffraction order scatterometry signatures in a single image, can be configured for both dense and isolated targets, and allows scatterometry and image-based metrology to be performed on the same tool. Future projects will include the development of spectroscopic scatterometry instruments.

Figure 1. The new Goniometric Optical Scatter Instrument (GOSI) is a reference reflectometer for diffuse and specular scattering measurements having 300 mm sample capability.

DELIVERABLES:

- Perform measurements on potential reference scatterometry target. 1Q 2007
- Construction of a spectroscopic scatterometry capability at NIST. 4Q 2008

ACCOMPLISHMENTS

■ We have developed efficient rigorous coupled wave (RCW) software for two-dimensional periodic structures in the conical geometry. Results of the in-house code have been compared with finite difference time domain, surface integral equation, and other RCW implementations. This software is also configured to run on a large cluster computer, so that library generation is possible.

■ As part of our effort in assessing the precision and accuracy of scatterometry, we have performed a study of the sensitivity of scatterometry to CD and sidewall angle for a large number of different measurement modalities, including angle-scanned and wavelength-scanned reflectometry and ellipsometry, for amorphous silicon gate and gate-resist structures. This study included parameters appropriate from the 45 nm half-pitch node to the 18 nm half-pitch node. The results (see Fig. 2) demonstrated that scatterometry can achieve the necessary sensitivity to measure dense gratings at these nodes. Future work, however, will be necessary to achieve sufficient sensitivity to isolated features.

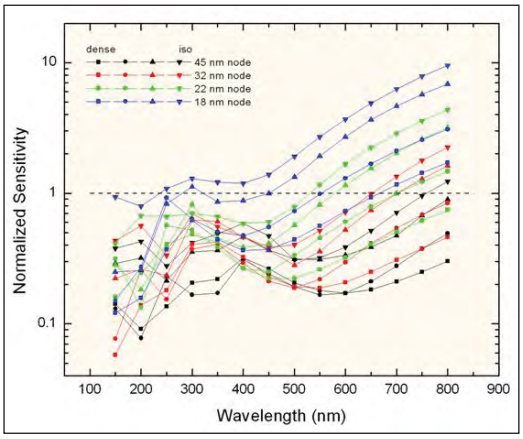

Figure 2. Estimated bottom dimension sensitivity, normalized by the 2 % of bottom dimension specification, calculated for gate gratings measured by angle scans of the reflected Stokes parameters with angles less than 70 degrees.

■ In the area of scatterometry-based optical critical dimension, (OCD) measurement, we have recently measured OCD linewidth of lines in grating targets fabricated using the single-crystal critical dimension reference materials (SCCDRM) process. The SCCDRM implementation, developed by a multi-OU collaboration at NIST, provides lines with known geometries – typically vertical sidewalls – defined by the silicon lattice, and has led to development of a prototype linewidth standard for isolated lines designed for use in AFM calibration. We have shown that the linewidth obtained from the OCD technique for these targets is linearly related to linewidth obtained from SEM, with a slope near unity and zero offset, Fig. 3. Continuing efforts to reduce linewidth roughness of the target, to analyze uncertainties in the OCD measurement, and to evaluate the suitability of these targets for OCD reference materials, are ongoing.

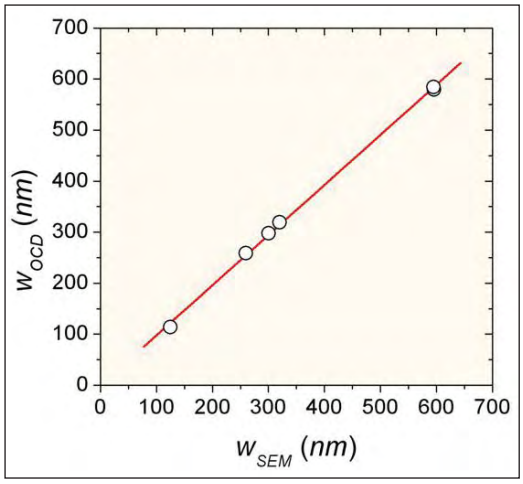

Figure 3. CD linewidth extracted from OCD, w_{OCD}, versus linewidth measured by SEM, w_{SEM}, for six targets on an SCCDRM chip.

■ We have also extracted OCD linewidth from scatterometry signatures of silicon-on-silicon gratings obtained using back-focal-plane imaging in a microscope. We investigated targets with only specular reflectance (grating pitch 300 nm) and those with both specular and higher-order diffraction (grating pitch 600 nm). Linewidths of 131 nm to 140 nm were obtained, with the back-focal-plane signatures demonstrating nanometer-level sensitivity to linewidth, and a linear relationship of linewidth obtained from scatterfield microscopy to linewidth measured by SEM was shown.

Collaborations

International Sematech Manufacturing Initiative, Benjamin Bunday, Limits of Scatterometry Study.

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Small Angle X-Ray Scattering-Based Dimensional Metrology

Technical Contacts:
R. L. Jones
E. K. Lin
W. L. Wu

Goals

To develop a small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, line width fluctuations, and line edge roughness, and statistical deviations across large areas in dense high aspect ratio patterns. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. Further, the wavelengths utilized by SAXS based measurements well complement current metrology tools based on optical scatterometry, SEM, and AFM.

Customer Needs

The drive to reduce feature sizes to sub-50 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the production of standards for current industrial solutions such as CD-SEM.

Technical Strategy

1. Exposure systems capable of sub-50 nm patterning are expected by 2009, requiring control of CD on the level of nanometers and in some cases sub-nanometer precision. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of Angstrom level precision in critical dimension evaluation over large (50 μm x 50 μm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission using a sub-Angstrom wavelength. The high energy of the X-ray source allows the beam to pass through a production quality silicon wafer, and could become amenable to process line characterization. The measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors are sufficient to implement a laboratory scale device capable of high precision measurements. This year, NIST has designed and installed the world's first laboratory scale CD-SAXS device.

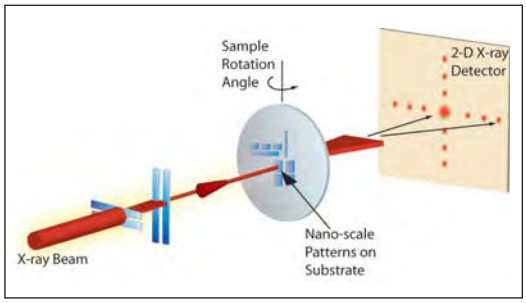

Figure 1. Schematic of the SAXS transmission geometry. Shown is the X-ray beam as it passes through the patterned sample and scattered at an angle 2θ. For a precisely aligned sample with known composition, a 3-d lineshape is obtained in one transmission measurement. Unknown samples can also be characterized through measurements at a variety of sample angles.

DELIVERABLES:

- Publish evaluation results from laboratory scale CD-SAXS instrument. 3Q 2007
- Perform cross-sectional measurements using laboratory scale CD-SAXS instrument on patterns produced with EUV lithography as part of round-robin study with SEMATECH and Intel. 4Q 2007

2. Characterization of pattern quality includes shape factors such as the sidewall angle and curvature. Measurements taken at a series of angles of incidence allows the reconstruction of the line shape. We have performed tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 1 degree. Ongoing analysis and technique refinement will provide additional shape factors, allowing determination of more complex shape information such as sidewall curvature. In addition to a

"high speed," model dependent characterization performed in a single measurement, a second method will be developed based on measurements at multiple sample orientations. This method provides a more precise measurement of the entire pattern cross section in a non-destructive and model independent manner (see Fig. 2). In the current technology node, this measurement can be used to evaluate optical scatterometry models for line shape, while providing a general capability to measure a pattern of arbitrary cross section in future technology nodes.

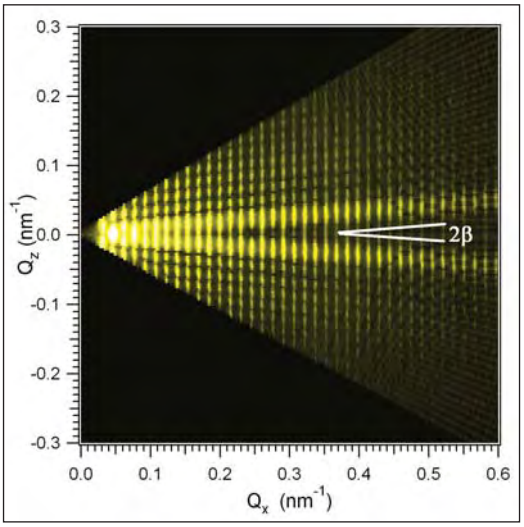

Figure 2. Data from measurements of a polysilicon line grating at varying sample angles. Shown is a contour plot of diffracted intensity as a function of scattering vectors parallel to the substrate, Q_x, and normal to the substrate, Q_z. The sidewall angle, β, is the half angle of the prominent ridges.

DELIVERABLES: Develop and apply refined CD-SAXS models to incorporate the effects of top and sidewall curvature. 2Q 2007

3. Current LER and CD specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. Techniques such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of optical scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. In cooperation with the Advanced Metrology Working Group at SEMATECH, NIST has designed a series of structures to model different types of roughness. CD-SAXS data from these structures will help further develop modeling protocols.

DELIVERABLES:

- Develop and publish refined models of line edge roughness scattering to fit first round of measurements of line edge roughness on model photoresist patterns produced by EUV lithography. 3Q 2007
- Participate in round-robin measurements involving Intel and SEMATECH to compare line edge roughness measurements between CD-SAXS and CD-SEM in oxide line/space patterns created by EUV lithography and pattern transfer, identifying key differences between measurable quantities. 4Q 2007
- Provide CD-SAXS measurements of cross section in round robin study with SEMATECH and Intel to evaluate the potential capability of CD-SAXS as an industrial calibration method. 4Q 2007

Accomplishments

■ We have provided the first measurements of sidewall angle using small angle X-ray scattering (SAXS). Using a series of photoresist gratings produced at the IBM T. J. Watson Research Center (Q. Lin), CD-SAXS was performed using at the Advanced Photon Source (Argonne National Laboratory) to measure photoresist patterns with well-defined sidewall angles. The protocol involves measurements of the sample over 20 degrees of incident angles, and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle (see Fig. 2). The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as a T-topped line, will produce different scattering patterns. The protocol can be adopted for other pattern shapes.

■ Our group has also demonstrated a capability to measure correlated fluctuations in line edge position as a measure of line edge roughness. CD-SAXS measurements of a series of line/space patterns with model LER were produced using 193 nm lithography in collaboration with the Advanced Metrology Advisory Group (AMAG) coordinated by SEMATECH. This initial study provided key data on the sensitivity of CD-SAXS to LER, including the development of models for LER and LWR contributions, in lines possessing periodic sidewall roughness with amplitudes of 3 nm (see Fig. 3). In addition, a methodology and experimental data was published describing a route to use CD-SAXS as a measure of roughness propagating normal to the substrate. Samples of photoresist line/space patterns were provided by the IBM T. J. Watson Research Center

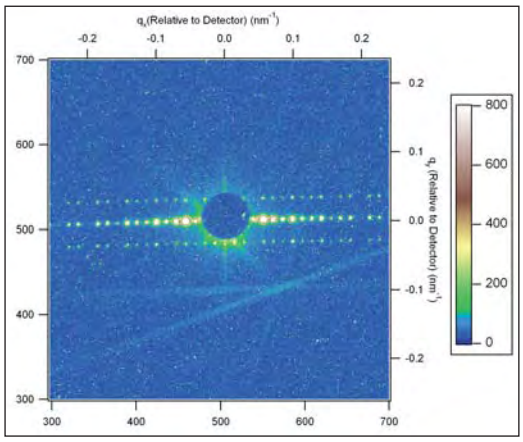

Figure 3. Detector image of etched polysilicon lines with designed line edge roughness. In addition to the typical diffraction spots characterizing pitch and linewidth, satellite peaks of intensity are observed symmetrically above and below the main diffraction axis. The additional peaks are a result of correlated sidewall roughness.

(A. Mahorawala) (see Fig. 4). This type of roughness is commonly observed in photoresists due to imprecise tuning of the underlying anti-reflective coating. Given the ability of CD-SAXS to extract the periodic component of roughness from non-periodic, the technique is capable of quantitatively extracting this component of roughness even when the amplitude is small compared to the random component. These studies are being extended into sub-50 nm dense patterns produced by EUV lithography in collaboration with Intel and SEMATECH.

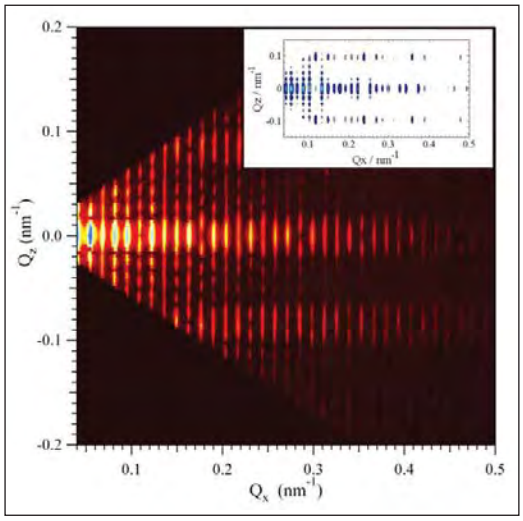

Figure 4. CD-SAXS intensity plotted in the inverse space plane Q_x-Q_z, where Q_x and Q_z are a vectors parallel and normal to the substrate respectively. The main diffraction band in the center results from the line/space pattern, however the parallel intensity bands at Qz = +/- 0.08 result from roughness following a periodic wave normal to the substrate. A simulated model of the roughness provides the capability to extract quantitative information (inset).

■ Initial feasibility studies have demonstrated the potential of CD-SAXS to detect and to estimate the extent of sidewall damage of nanoporous low-κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low-κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ, it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low-κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low-κ material, then backfilled the trenches with the same candidate low-κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays.

■ The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height, and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature (T_G). Heating these patterns below T_G does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above T_G, the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

Collaborations

Polymers Division, MSEL, Chengqing Wang, Derek L. Ho, Christopher L. Soles, Hyunwook Ro, Yifu Ding

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, Melissa Shell, sub-50 nm structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

SEMATECH, Youfan Liu, Metrology of low-κ patterns using CD-SAXS.

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

University of Michigan, Stella Pang, Nanoimprinted polymeric structures.

Molecular Imprints, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

IBM Yorktown Heights, Qinghuan Lin, Development of pattern shape and sidewall angle metrology.

Recent Publications

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, B. J. Rice, K. Choi, G. M. Thompson, S. J. Weigand, D. T. Keane, "Characterization of Correlated Line Edge Roughness of Nanoscale Line Gratings using Small Angle X-Ray Scattering," accepted to J. Appl. Phys. (2007).

E. K. Lin, W.-L. Wu, R. L. Jones, C. Wang, K. Choi, G. M. Thompson, B. J. Rice, "Critical Dimension Metrology with Small Angle X-ray Scattering," accepted to FabTech (2007).

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R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, "Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing," **6**, 1723 (2006).

R. L. Jones, E. K. Lin, W.-L. Wu, Q. Lin, S. J. Weigand, D. T. Keane, J. P. Quintana, "Cross Sectional Metrology of Dense, High Aspect Ratio Patterns using CD-SAXS," Proc. SPIE **5752**, 404 (2005).

H.-J. Lee, C. L. Soles, H. W. Ro, R. L. Jones, E. K. Lin, W.-L. Wu, D. R. Hines, "Nanoimprint pattern transfer quality from specular X-ray reflectivity," Appl. Phys. Lett. **87**, 263111 (2005).

T. Hu., R. L. Jones, E. K. Lin, W.-L. Wu, Q. Lin, D. Keane, S. Weigand, J. Quintana "Small angle X-ray scattering metrology of side wall angle and cross section in nanometer scale gratings," J. Appl. Phys. **96**, 1983 (2004).

R. L. Jones, T. Hu, E. K. Lin, W. L. Wu, R. Kolb, D. M. Casa, P. J. Bolton, and G. G. Barclay, "Small angle X-ray scattering for sub-100 nm pattern characterization," Appl. Phys. Lett., **83**, 4059 (2003).

Dimensional Metrology with Grazing Incident X-Ray Scattering

Technical Contacts:
W. L. Wu
E. K. Lin
C. L. Soles

Goals

To develop a grazing incident X-ray scattering (GIXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on test samples. The focus is to develop a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, line width fluctuations, and line edge roughness, and statistical deviations across large areas in dense high aspect ratio patterns. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes beyond 30 nm nodes.

Customer Needs

The drive to reduce feature sizes to sub-30 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM and optical scatterometry (OS) face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) and sidewall angle as pattern sizes decrease. CD-SAXS measurements do offer an attractive solution for CD metrology but the transmission geometry requires high flux X-ray sources that are not yet available for laboratory or fab line instruments. However, a grazing incidence reflection geometry for X-rays is finding increased use in semiconductor metrology and can utilize current lower flux X-ray sources. In this project, NIST is evaluating the feasibility of grazing incident X-ray scattering as a measurement tool to complement the transmission based CD-SAXS metrology currently under development in NIST.

Technical Strategy

1. We are developing a grazing incident X-ray scattering based method capable of Angstrom level precision in critical dimension evaluation to complement on-going effort of the transmission based CD-SAXS. In comparison GIXS has the following advantage and disadvantages over CD-SAXS;

■ The incident beam intensity can be enhanced by a factor of 4 once the incident angle is set at the critical angle of the substrate which is a silicon wafer for most of the cases. In contrast, there is an over 50 % loss of incident intensity in transmission geometry by going through the substrate. The overall difference is an 8x increase in incident beam intensity. This difference is significant because low beam flux is the major drawback for laboratory scale X-ray systems.

■ For the case of a silicon substrate the critical angle with copper K_α line the incident angle is near 0.2° and this imposes a large footprint on the sample. For example, with an incident beam diameter of 100 μm the footprint on the sample will be near 3 cm along the reflection direction. Such a large footprint is unacceptable for semiconductor applications.

■ To overcome the footprint problem, the beam size at the sample position must be reduced. Current advancements in X-ray optics, however, have enabled the focusing of X-ray beam to 5 μm or less. We will work with industry and university partners to pursue and to evaluate optical components most suitable for CD measurements.

■ The shortcoming of using focused incident X-ray beam is the loss in the angular divergence. The current CD-SAXS system at NIST is designed to have a high resolution such that it can resolve samples with a 400 nm period. However, X-ray based metrology will be needed by the semiconductor industry with the production of 30 nm structures. At these sizes, a lower resolution X-ray instrument will be adequate. Therefore, the current stringent requirements in angular divergence can be relaxed and focusing optics will become a viable route to shrink to beam size at the sample.

DELIVERABLES:

- Evaluate X-ray focusing optics. 3Q 2007
- Acquire X-ray focusing optics. 1Q 2008
- Integrate X-ray focusing optics to the existing CD-SAXS instrument. 3Q 2008
- Evaluate samples with 60 nm or smaller repeat with the GIXS configuration. 4 Q 2008
- Conduct GIXS measurements with model samples for line width, line height, side wall angle and designed sidewall roughness. 2Q 2009

2. The other challenge in the development of GIXS is in the analysis of the experimental data. For transmission based CD-SAXS the structure and the scattering intensity are related through simple Fourier transforms. This simple relation is no longer valid for GIXS data. Considerable efforts have to be devoted in the development of data analysis algorithm.

DELIVERABLES:

- Develop GIXS analysis algorithm and software for line width calculation. 1Q 2008
- Develop GIXS analysis algorithm and software for line height and sidewall angle calculations. 3Q 2008
- Develop GIXS analysis algorithm and software to sidewall roughness calculation. 1Q 2009

We have successfully modified the sample stage of the current CD-SAXS instrument to enable some preliminary GIXS measurements. A recent result from an ordered organic thin film is given in Fig. 1 and the footprint on this sample is over 5 cm. With a successful implementation of focusing optics this footprint can be reduced considerably.

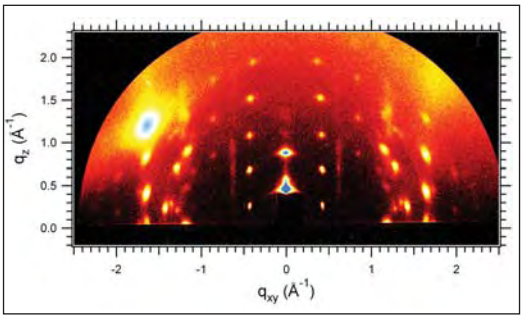


Figure 1. GIXS result from an ordered organic thin film supported on silicon wafer. Data collected on the NIST CD-SAXS instrument using Cu K_α X-ray beam.

Collaborations

Polymers Division, MSEL, R. Joseph Kline, Chengqing Wang, Derek L. Ho, Christopher L. Soles, Hyunwook Ro, Yifu Ding

Intel Corporation, Kwang-Woo Choi, Bryan Rice, sub-50 nm structures.

Recent Publications

M. L. Chabinyc ML, M. F. Toney, R. J. Kline, I. McCulloch, M. Heeney, "*X-ray scattering study of thin films of poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene),*" JACS, **129**, 3226 (2007).

R. L. Jones, C. L. Soles, E. K. Lin, W. Hu, R. M. Reano, S. W. Pang, "*Pattern Fidelity in Nanoimprinted Films using CD-SAXS,*" J. Microlith. Microfab. Microsyst. **05**, 013001 (2006).

R. L. Jones, W.-L. Wu, C. Wang, E. K. Lin, K.-W. Choi, B. J. Rice, G. M. Thompson, S. J. Weigand, D. T. Keane "*Characterization of Line Edge Roughness using CD-SAXS,*" Proc. SPIE **6152**, 215 (2006).

H. W. Ro, Y. Ding, H. J. Lee, D. R. Hines, R. L. Jones, E. K. Lin, A. Karim, W.-L. Wu, C. L. Soles, "*The Role of Stress in Nanoimprint Lithography,*" Proc. SPIE **6151**, 348 (2006).

R. L. Jones, E. K. Lin, W.-L. Wu, Q. Lin, S. J. Weigand, D. T. Keane, J. P. Quintana, "Cross Sectional Metrology of Dense, High Aspect Ratio Patterns using CD-SAXS," Proc. SPIE **5752**, 404 (2005).

H.-J. Lee, C. L. Soles, H. W. Ro, R. L. Jones, E. K. Lin, W.-L. Wu, D. R. Hines, "*Nanoimprint pattern transfer quality from specular X-ray reflectivity,*" Appl. Phys. Lett. **87**, 263111 (2005).

T. Hu., R. L. Jones, E. K. Lin, W.-L. Wu, Q. Lin, D. Keane, S. Weigand, J. Quintana "Small angle X-ray scattering metrology of side wall angle and cross section in nanometer scale gratings," J. Appl. Phys. 96, 1983 (2004).

R. L. Jones, T. Hu, E. K. Lin, W. L. Wu, R. Kolb, D. M. Casa, P. J. Bolton, and G. G. Barclay, "Small angle X-ray scattering for sub-100 nm pattern characterization," Appl. Phys. Lett., 83, 4059 (2003).

W. L. Wu, E. K. Lin, Q. H. Lin, and M. Angelopoulos, "Small Angle Neutron Scattering Measurements of Nanoscale Lithographic Features," J. Appl. Phys., 88, 7298 (2000).

Atom-Based Dimensional Metrology

Technical Contact:
R. Silver

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable and allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

Customer Needs

This project responds to the U.S. industry need for length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer tremendous promise for meeting these future measurement, test artifact, and calibration standards needs of the microelectronics industry. One important application of the high-resolution SPM methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a unique NIST-designed picometer resolution interferometer (Fig. 1).

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of linewidth metrology tools. We are also developing unique high-resolution interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions at the nanometer scale. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

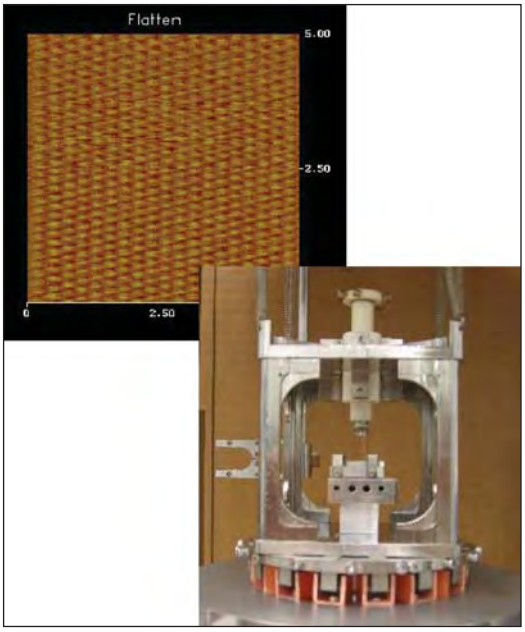


Figure 1. A new STM structure design has been implemented to improve the atomic scale imaging and structural characteristics. This system will provide improved nanometer scale interferometer-based imaging and measurement capabilities.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (see Fig. 2, next page).

As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical CD tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation make the concept of having samples

of known geometry and width essential. This project is developing samples of known geometry and atomic surface structure which yield well defined dimensional measurements. One goal is a measurement which results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the UHV environment and then stabilized and subsequently transferred to other instruments (Fig. 3).

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods

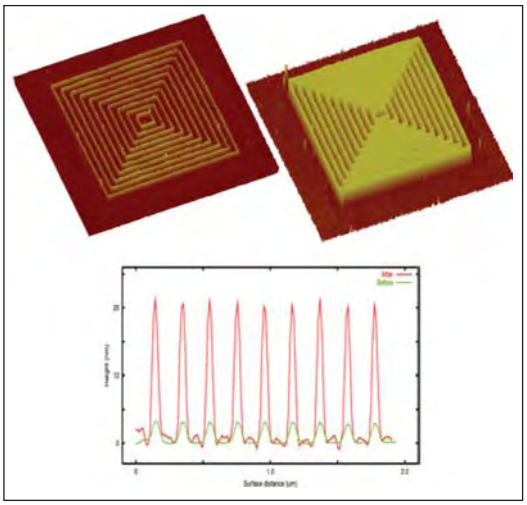
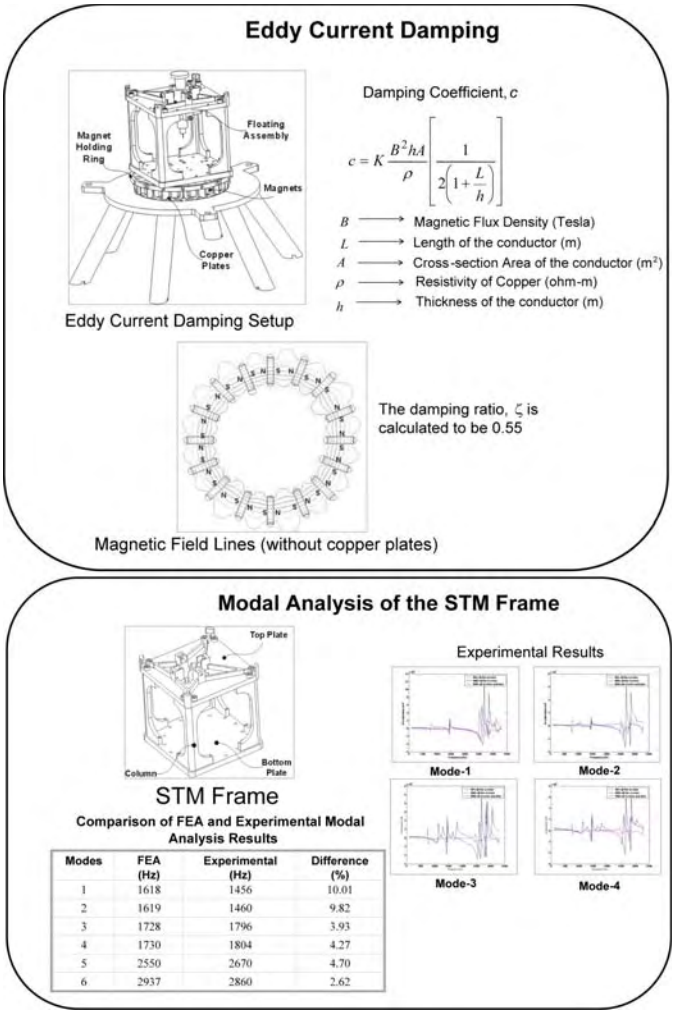


Figure 3. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.



Modes	FEA (Hz)	Experimental (Hz)	Difference (%)
1	1618	1456	10.01
2	1619	1460	9.82
3	1728	1796	3.93
4	1730	1804	4.27
5	2550	2670	4.70
6	2937	2860	2.62

Figure 2. Key design elements for the instrument used to fabricate features with sub-10 nm dimensions. This tool utilizes advanced design tools to optimize vibration sensitivity and enable access to 1 cm x 1 cm of sample area.

that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order which is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES:

- Write features in silicon with critical dimensions smaller than 7 nm. Apply the pattern writing process and etch features for use as optical scatterfield test structures using the new, Scanning Tunneling Microscope (STM). 4Q 2007
- Work with EEEL and ISMT to develop improved methods for etching nanostructures written in silicon. Use RIE etching techniques to etch features with sub-10 nm dimensions in silicon. 4Q 2007

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These

well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES: Develop the rigorous and robust preparation techniques to enable routine atomic resolution using W (111) single crystal tungsten tips. Determine the stability of these W tips for use in STM imaging. 3Q 2007

3. Development of artifacts that can be atom counted and then measured in different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on using new silicon processing methods to reduce the process temperatures required for atomic reconstructions. Fully operational wet chemical processing has been demonstrated on atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing *in situ* processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures (Fig. 4).

DELIVERABLES: Implement UHV sample and tip heating and preparation capability in the Omicron STM system. Enable robust alignment and interface with the system transfer mechanism for sample transfer into the UHV environment. The new STM and UHV preparation facility will allow improved Si sample prep and atomic surface reconstructions. 4Q 2007

4. Develop the new UHV Omicron system and the in-house designed facility for improved robust atomic resolution imaging. The new imaging capabilities are being developed and will next be applied to etched silicon features provided by Sematech on Si (111) wafers when they become available. The intent is to provide atomically resolved and precisely imaged quantitative results on etched silicon substrates. These nano-meter-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples.

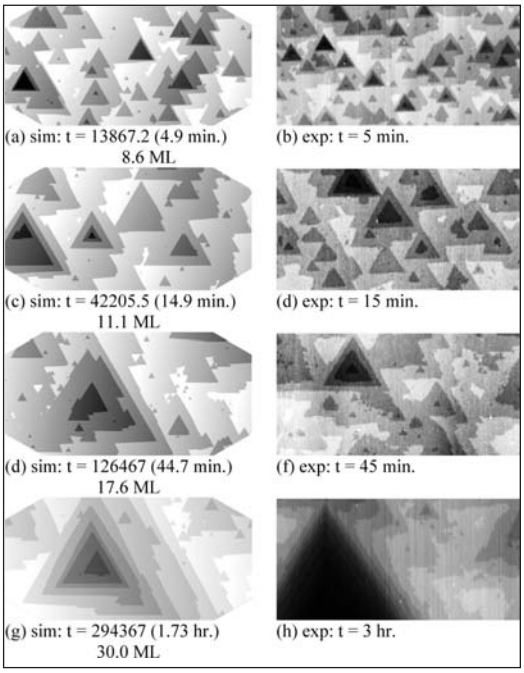


Figure 4. Time resolved KMC simulation for surfaces with 0.02° miscut angle and 60° miscut orientation on the left and compared with experimental data on the right. All images are 4000 × 2000 nm^2.

ACCOMPLISHMENTS

■ The ability to prepare atomically sharp tips in W (111) has been demonstrated. We are now implementing a robust methodology for repeatable UHV tip preparation. This is based on the new tip processing capability in the UHV STM system and will be developed to allow atomic tip preparation without the need for the FIFEM.

■ A workshop from the SPIE Nanotechnology Working Group on nanoimprint technology for semiconductor manufacturing was held at Microlithography 2007. The workshop was organized by Rick Silver, Chris Soles and Mike Postek and included presentations and a panel discussion involving several industry and University leaders. The Nanotechnology Working Group is chaired by Rick Silver and Mike Postek and has served as a forum for developing and applying nanotechnology related manufacturing and fabrication elements which will directly benefit the semiconductor manufacturing community.

■ In the continuing collaboration between the NIST atom-based dimensional metrology project and the Department of Mechanical Engineering at

the George Washington University a presentation was given at the ASPE conference on the dynamic analysis and eddy current damping effects on sensitive tunneling instruments. The work was based on solid model Pro E and Pro Mechanica modeling of structures for use in high resolution imaging tools such as the UHV STM. The actual tool modeled is housed in the AML and the mechanical structure used for this measurement instrument was based directly on the modeling results. The modeling results were further verified using accelerometer measurements to match the theoretical modeling to experiment. The publication focused on this quantitative comparison including a full modal analysis.

■ Collaboration between the NIST atom-based dimensional metrology project and the Department of Mechanical Engineering at the George Washington University the Graduate student Sumanth Chikkamaranahalli has demonstrated the operation of the new STM. This new instrument is expected to make important contributions to the advancement of nanometer and atomic scale standard artifact fabrication and metrology methods capable of sub-nanometer measurement. This new STM has been moved into the previous UHV vacuum facility used by the Burleigh instrument. The new improved metrology tool has replaced the previous instrument which has been the workhorse for several recent publications in Applied Physics Letters and the Journal of Chemical Physics. This project continues to be the basis for substantive successful collaborations with the University of Maryland and the George Washington University.

■ An in depth paper was published in the Journal of Physical Chemistry. The paper is a leading comprehensive set of experimental and theoretical analysis on the preparation of silicon surfaces. This work was carried out in large part by Post Doc Hui Zhou and in collaboration with the University of Maryland, Department of Physics. This paper follows on a paper published in late 2005 in the Journal of Physical Chemistry titled "The Influence of defects on the morphology of Si(111) Etched in NHF". In this new paper we have extended the Kinetic Monte-Carlo simulation method to study the etching dynamics of Si (111) surfaces in NH4F in a time-resolved basis. We have examined the step-flow dynamics of Si(111) etching using various simulation window sizes for variety of miscut angles and miscut orientations as well as those parameters which affect the formation of etch pits. The simulation results have been compared with published experimental data to derive an absolute time scale.

■ We have prepared atomically flat surfaces and obtained atomic order on the wet chemical prepared surfaces. The routine imaging of these surfaces on the atomic scale is expected to be enhanced with the new STM. These results have been recently published in leading chemical physics journals and presentation forums. These results are a substantial step forward in repeatable silicon surface preparation for atomic scale metrology and are now being supported in collaboration with SEMATECH and current industry requirements. The results, seen in Fig. 4, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

■ The silicon etching process has been developed and demonstrated for patterns written on silicon. Patterns with features as small as 10 nm have been written in hydrogen terminated silicon surfaces with subsequent pattern transfer into the silicon substrates. A publication recently appeared on this material. The importance of etching structures in Si (111) is now being supported by SEMATECH and a recent collaboration between NIST and SEMATECH to develop lithography methods and plasma etch method at SEMATECH's fab is now under way.

■ A paper was presented to the ASPE special topics conference by Summanth Chikkamaranahalli, a graduate student from the George Washington University. The paper is an excellent analysis of damping and precision structures for use in STMs and atomic scale imaging. The analysis and modeling have been used in the development of the NIST STM for the atom-based dimensional metrology project. The tool has recently taken very nice high resolution atomic scale images. The scanning tunneling microscope was designed by the NIST team in collaboration with Prof. Vallance at the George Washington University. The FEA static and dynamics analysis using promechanica and preE packages gave the researchers quantitative tools to evaluate and develop the STM imaging head, and larger mechanical structure.

■ We have used the FIM techniques to analyze nanotubes and their structure. The nanotubes were directly characterized for use as SPM tips with dimensional analysis on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology (Fig. 5).

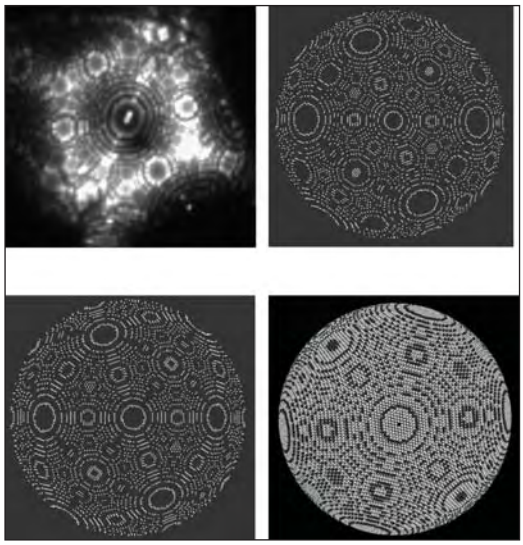


Figure 5. Upper left shows an FIM image of a W (110) tip. On the upper right is a simulation of a FIM image of a W (110) tip with base radius r = 14.9 nm and n = 1.82. The lower panels show simulations of an FIM image of a W (110) tip with base radius r = 14.9 nm and n = 2 and a ball model with same parameters.

Collaborations

Sematech, IBM, University of Maryland, Dept. of Physics, George Washington University, Dept. of Mech. Eng.

Recent Publications

S. Chikkamaranahalli, R. Vallance, B. Damazo, and R. M. Silver, *"Damping Mechanisms for Precision Applications in UHV Environment,"* Proc. ASPE Conf., Pitts. PA (2006).

H. Zhou, J. Fu, and R. M. Silver, *"A Time-resolved Kinetic Monte-carlo Simulation Study on Si (111) Etching,"* Accepted to Journal of Physical Chemistry (2006).

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H. Zhou, *"Study of wet chemically prepared hydrogen terminated Si (111) surfaces and a novel implementation of a high resolution interferometer,"* Thesis, University of Maryland, 2004.

R. M. Silver, S. Gonda, J. Jun, L. Howard, and C. Jensen, *"Atomic Resolution Measurements with a New Tunable Diode Laser-Based Interferometer,"* Optical Engineering, Vol. 43 No. 1 (Jan. 2004).

P. V. M. Rao, C. P. Jensen, and R. M. Silver *"An enhanced model for STM tip geometry measured with FIM,"* JVST B (Mar/Apr 2004).

Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Technical Contact:
M. W. Cresswell

Goals

The goal of this project is to develop test-structure-based reference materials with emphasis on supplying road-map-compliant physical standards for critical-dimension (CD) metrology-tool development and calibration. The specific near-term goal is fabricating a quantity of CD reference-features with nominal CDs in the range 20 nm to 160 nm and having 2σ (expanded uncertainties) of less than 1.5 nm by July 2007. Their application is primarily for AFM-tip calibration. A longer-term goal is to fabricate and calibrate gratings for use in optical critical-dimension metrology that is becoming widely used in advanced semiconductor manufacturing.

Customer Needs

The Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS) 2005 p.36 under "Reference Materials," states that it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials- and process-equipment development. This project is concerned specifically with ensuring a source of such reference materials to satisfy the stated need throughout the near-term years.

Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The roadmap projects the decrease of gate microprocessor unit (MPU) physical gate lengths used in state-of-the-art IC manufacturing from present levels of 28 nm to 13 nm during the near-term years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding specifications for these applications. It is widely believed that the situation can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. The technology that the project has developed for fabricating CD reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation.

Further details of customer needs that have been identified since the SCCDRM distribution to SEMATECH Member Companies in January 2005, and now impact the project's responding technical strategy, are described in the next section.

Technical Strategy

The fundamental SCCDRM technical strategy is to pattern Silicon on Insulator (SOI) device layers with lattice-plane selective etches of the kind used in silicon micro machining, which provides reference features with quasi-atomically-planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if sidewall nano-planarity can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the implementation include starting silicon SOI wafers with the device layer having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micromachining. However, the difficulty of obtaining satisfactory SOI material in larger diameters has driven us towards parallel evaluation of a bulk-wafer starting-material strategy. The roadmap states that measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. The traceability path for dimensional certification of the project's SCCDRMs is responsive to this requirement and originates with measurement of a selection of reference-feature CDs with both Atomic-Force Microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM) imaging. The former technique is highly repeatable and of manageable cost while the latter enables a lattice-plane count that allows expression of the each CD in terms of a traceable distance, which is the periodicity of silicon (111) lattice planes. However, HRTEM is totally destructive and thus is not useful for supplying reference features to end users. The project's traceability strategy thus features state-of-the-art AFM as a transfer metrology to deal with this constraint. Transfer metrology relates CDs extracted by AFM to be traced to SI units through the construction of a so-called calibration curve. An example of such a curve is shown in Fig. 1 (next page). To maintain maximum possible accuracy in the transfer-

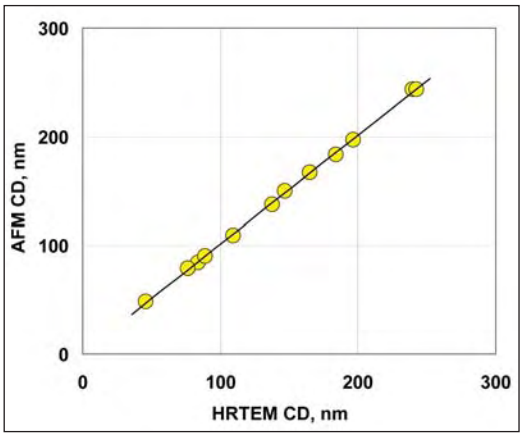

Figure 1. Transfer metrology relates CDs extracted by AFM to be traced to values SI units through the construction of a so-called calibration curve.

metrology operation, an elaborate reference-feature selection protocol has been established to identify reference features that qualify by virtue of their CD-uniformity, as contributors to the construction of the calibration curve, or for delivery to end users. Multiple reference features on a large set of as-patterned test chips are identified initially by high-power optical inspection. This procedure checks primarily for continuity, cosmetics, and apparent uniformity of the narrowest-drawn sets of six features that are incorporated into test structures, which are called HRTEM targets. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to etched CDs of between 50 nm and 300 nm. The "best" 10 % of the AFM targets passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20K magnification to narrow the selection process further. Digitized profiles of the CDs of top-down SEM images are then extracted at 25 nm intervals. The measurements are transferred to a database, which is then interrogated to identify chips, and AFM targets on them, that have more uniform SEM-CD profiles at the narrower CDs — typically less than 150 nm. Candidate AFM targets so identified on each chip are then CD-profiled by AFM. Chips having AFM targets with all six features having superior uniformity are then partitioned into a calibration sub-set and a product subset. All six features of the selected targets on the chips on the *calibration* sub-set are then subjected to HRTEM imaging. These are the chips whose designated AFM targets are to be used as contributors to the calibration curve. The design of all HRTEM targets enables the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation. Since such operations are very costly, this capability is economically advantageous. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve spanning a 150 nm range.

Because 200 mm (110) starting material until recently has been unobtainable at an acceptable cost, this project's technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips. The scheme is shown in Fig. 2. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The Project's technical strategy is now evolving in a way that is addressed in the material that follows below. In summary, it is responding to industry push to implement measures that make the SCCDRMs more compatible with end-user requirements. These measures include:

- replacing the carrier-wafer with a monolithic 200 mm wafer implementation,
- replacing the buried oxide of SOI wafers with a buried boron diffusion having an epitaxial silicon layer deposited over it,
- further reducing the CDs of calibrated features to 20 nm and the uncertainties of the calibrated CD to less than 1.0 nm,
- improving the reference feature's CD uniformity to enable certifying the CD of an extended length,
- improved on-wafer navigation for end-user convenience,

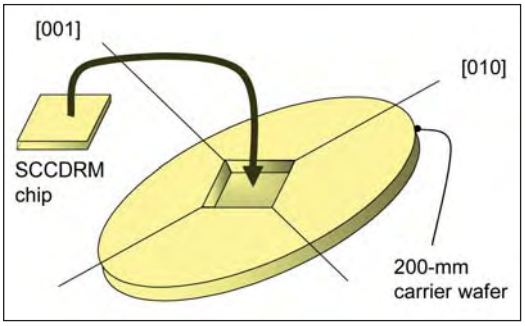

Figure 2. The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

- calibrating a selection of OCD gratings that are replicated at the same time as the isolated lines that have been supplied so far, and
- improved management of the organic residues that sometimes impair the cosmetic appearance of the reference features and their environment on the wafer and to some extent adversely affect the uncertainty values of the delivered product.

Implementing these aggressive measures requires wafer-processing facilities that require innovative teaming with other laboratories. Our strategy takes a page from the roadmap that explicitly states that standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials (ITRS) 2005 p. 36 under "Reference Materials." Likewise, the roadmap states that metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials (ITRS) 2005 p. 36 under "Scope." In response to this mandate, we have developed a unique relationship with the Microelectronics Research Centre (MRC) with the University of Texas in Austin. Our collaboration has resulted in the extraordinary OCD grating section shown in Fig. 3 which exhibits 36-nm lines at 180-nm pitch and having a height of 430 nm. The lithography in this case was done by MRC's JEOL direct-write e-Beam system. In a related collaboration we are working with both MRC and the Scottish Microelectronics Centre (SMC) at the University of Edinburgh to implement a hybrid optical-Ebeam lithography process to diversify our portfolio of reference materials for semiconductor-manufacturing applications.

DELIVERABLES:

- Repeat of the screening experiment to confirm and refine the prior identification of which combinations of six pattern-transfer process factors drive down reference feature CDs and their uncertainties. 4Q 2007
- Demonstrate a hybrid optical-EB-direct-write lithography process to pattern a selection of 200 mm (110) wafers with SCCDRM reference features with CDs at or below the 20 nm level. 1Q 2008
- In collaboration with SEMATECH, apply193 nm lithography to the patterning of a selection of 200 mm bulk-silicon (110) wafers with a SCCDRM test structures having reference-feature CDs at or below the 20 nm level. 2Q 2008

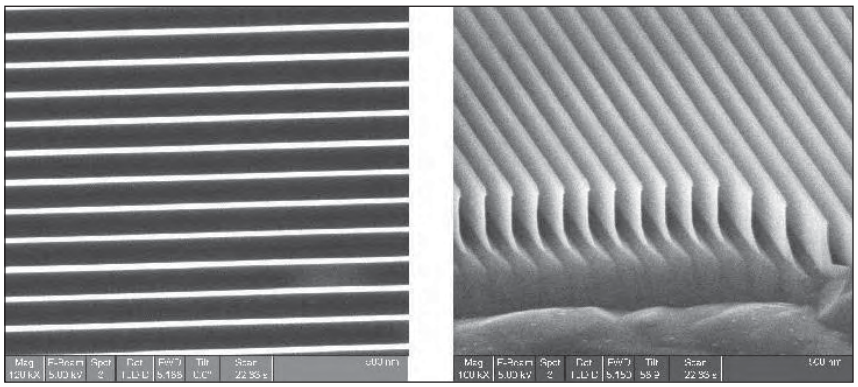

Figure 3. OCD grating section fabricated with SCCDRM technology which exhibits 36-nm lines at 180-nm pitch and having a height of 430 nm. The lithography was performed by collaborating UT-Austin staff using their direct-write e-Beam system.

- Publish measurements and analyses on the application of SEM-CD metrology as a SCCDRM transfer metrology. 3Q 2007
- Fabricate, evaluate, and publish a selection of preliminary measurements made on OCD gratings patterned on SCCDRM wafers to serve as an optical-CD reference material. 2Q 2007
- Implement a plan to fabricate and calibrate a selection of isolated-line CD-SRMs. 4Q 2007

ACCOMPLISHMENTS

■ This project, in collaboration with the NIST Precision Engineering and Statistical Engineering Divisions, has recently designed and implemented a screening experiment to identify which combinations of six pattern-transfer process factors drive down reference feature CDs and their uncertainties. A 2^{6-2} fractional factorial experiment design was implemented to enable an efficient study of this relatively large number of factors and to obtain information on the effects from their interactions. Extensive AFM measurements that have now been made have identified numerous features having CDs at the 20-nm level. The uniformity of individual reference-feature CDs exceeds those of the earlier delivery. As a consequence, it is anticipated that the uncertainties that will be ascribed to them at the completion of the experiment will be well below the prior 1.5 nm to 3 nm range.

■ In preparation for implementing the findings of the process-optimization exercise referenced in the previous paragraph, and responding to the customer needs described earlier, chip layouts have been designed for three new SCCDRM fabrication ventures. Two of them are for 200 mm-wafer monolithic implementations. The first of these is an exercise to evaluate some available 200 mm (110) material, which is difficult to obtain but which we have on hand, to facilitate

running wafer lots on the 193 nm lithography tool at SEMATECH. The evaluation lithography is being accomplished with an i-line tool at the University of Edinburgh. The second is a design that is being incorporated onto a new reticle for lithography by the 193 nm Step-and-Scan tool on line in SEMATECH. The third venture for which new CAD has been designed is a new complex optical/e-beam-direct-write process, which is being applied to 100 mm (110) starting material. The lithographic processing for which the CAD has been designed will be carried out jointly by the Microelectronics Research Center, of the University of Texas at Austin, and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh.

■ One of the main drivers of the customers' need to replace the carrier wafer with a monolithic implementation is that the former is vulnerable to contamination originating during post-assembly cleaning. Ordinarily this is not a leading concern in AFM-tip calibration, although it cannot be dismissed for SCCDRM use in ultra-clean facilities. Otherwise, tip calibration is becoming widely recognized as an application for which the reference materials are well suited.. However, an emerging application of interest in the industry is SEM tool calibration. In this application, regular reference-material cleaning is necessary due to the nature of the metrology. During the current year, a new cleaning procedure was devised and evaluated at the chip level. At the same time, the rate of hydrocarbon deposition during worst-case conditions was assessed. This work was performed to answer anticipated questions on the subject when our 200-mm wafer-based artifacts become available.

■ During the investigations of hydrocarbon contamination by SEM tools, and devising a cleaning procedure to deal with it, we took the opportunity to look at the issue of reference material calibration using HRTEM as the primary metrology and SEM as the transfer metrology. The attractiveness of this approach to calibration is that SEM is a much more readily available facility and is generally faster than AFM even though one can expect uncertainty inflation. The results were technically useful and have been incorporated into a manuscript that has been accepted for publication in an IEEE Transactions journal.

■ The emerging metrology known as optical-CD (OCD) scatterometry translates broadband light, diffracted from an on-wafer grating patterned into the resist or film, into accurate profiles of the grating's features from which key parameters, such as CD, can be extracted. Whereas currently favored metrology tools such as CD scanning electron microscopes and AFMs require a vacuum wafer environment, OCD metrology does not, and is fast and non-invasive. The possibilities of OCD extend to characterizing the sidewall angle and height of critical features. Until physical standards are available, the full promise of OCD control scatterometry may not be met. Since the SCCDRM implementation is well suited to the fabrication of calibrated reference materials for this new application, we have now accomplished the first-ever fabrication and inspection of gratings for this purpose. A paper on the very encouraging first results, which were obtained by collaborating staff in NIST's Physics Laboratory and at SEMATECH have been presented at an international conference in Tokyo, Japan.

■ Recently, the project published a comprehensive full-length report on the fabrication and calibration of SCCDRM Reference Materials entitled RM 8111: Development of Prototype Linewidth Standard in the NIST Journal of Scientific Research. Several other papers on special aspects of the fabrication and calibration, such as test-chip design, AFM metrology, and HRTEM imaging, were presented at the SPIE Spring Symposium of February, 2007, and the IEEE International Conference on Microelectronic Test Structures in March, 2007. A paper on the subject of etch-process optimization for uncertainty management was presented at the International Electron, Ion, and Photon Beam Technology and Nanofabrication Conference in June, 2006. A manuscript on the comparison of SEM-CD measurements and traceable-AFM CD measurements has been accepted for publication in an IEEE Transactions journal in June 2007. An important first description of fabrication of SCCDRMs on 200-mm bulk wafers which was performed in collaboration with the Scottish Microelectronics Centre was presented at the *Frontiers of Characterization and Metrology for Nanoelectronics* in March 2007.

Collaborations

The project is now actively collaborating with the Microelectronics Research Center of the University of Texas at Austin (http://www.mrc.utexas.edu/amrc/publications.html), and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh in Scotland (http://www.see.ed.ac.uk/IMNS/). Both these organizations

operate the advanced wafer processing tools that we will be using to address the customer needs referenced in the sections above. Both institutions have highly skilled staff with both of which we have published recently. We are interacting with the CAD and reticle staff the ISMI Subsidiary of SEMATECH, (http://ismi.sematech.org/) who have invited us to share space on a new reticle for their SVGL 193 nm Step-and-Scan lithography tool to fabricate an advanced generation of SCCDRMs for distribution to the member companies, as well as for possible calibration and distribution from NIST as SRMs.

We also interact regularly and closely with NIST's Physics, MEL and ITL Laboratories (http://www.mel.nist.gov/ and http://www.itl.nist.gov/) with whom we of EEEL share an intramural ATP program award to reduce the certified CDs and uncertainties of SCCDRMs through fabrication refinements.

Standards Committee Participation

Electrical Test Structures Task Force, Co-Chair (Richard A. Allen)

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen)

Recent Publications

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Smith, A. J. Snell, J. M. Stevenson, A. Walton, M. W. Cresswell, R. A. Allen, 'Extraction of Sheet Resistance and Linewidth from All-Copper ECD Test-Structures Fabricated from Silicon Preforms,' 2007 International Conference on Microlectronic Test Structures, pp.14-19 (22-MAR-2007)

R. A. Allen, R. Dixson, M. W. Cresswell, W. Gutherie, B. J. Shulver, A. S. Bunting, J. T. Stevenson, and A. Walton, "CD Reference Materials Fabricated on Monolithic 200 mm Wafers for Automated Metrology Tool Applications," 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, Mar 27-29, 2007, Gaithersburg, MD (01-SEP-2007)

B. Li, L. Shi, P. S. Ho, J. Zhou, R. A. Allen, M. W. Cresswell,'Test Structures for Study of Electron Transport in Nickel Silicide Features with Linewidths between 40 nm and 100 nm,' IEEE ICMTS International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.18-23 (01-APR-2006)

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JEDEC Standard JESD202, "Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress," March 2006. (Written by H. A. Schafft).

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Dixson, R. G., Allen, R. A., Guthrie, W. F., Cresswell, M. W, Traceable Calibration of Critical-dimension Atomic Force Microscope Linewidth Measurements with Nanometer Uncertainty J. Vacuum Sci. Technol. B Vol 23 Issue 6 pp. 3028-3032 November 30, 2005.

Cresswell, M. W., Dixson, R. G., Guthrie, W. F., Allen, R. A., Murabito, C. E., Park, B., Martinez, J. V., Hunt, A. Critical Dimension Reference Features with Sub-Five Nanometer Uncertainty SPIE 30th International Symposium Microlithography Metrology, Inspection, and Process Control San Jose, CA Vol 5752 pp. 288-303 May 30, 2005.

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W. F. Guthrie, R. G. Dixson, R. A. Allen, M. W. Cresswell, C. E. Murabito, B. Park, "Establishing Traceability of Linewidth Reference Materials Using CD-AFM and HRTEM," 2005 International Conference on Characterization and Metrology for ULSI Technology, March 15-18, 2005, University of Texas at Dallas.

R. A. Allen, A. Hunt, C. E. Murabito, B. Park, W. F. Guthrie, and M. W. Cresswell, “Extraction of Critical Dimension Reference Feature CDs from New Test Structure Using HRTEM Imaging,” Proceedings of the 2005 IEEE International Conference on Microelectronic Test Structures, pp. 5-10, March 2005, Leuven, Belgium.

“Report of Investigation of RM 8111: Single-Crystal Critical Dimension Prototype Reference Materials,” National Institute of Standards and Technology, Gaithersburg, Maryland, March 2, 2005.

M. W. Cresswell, R. G. Dixson, W. F. Guthrie, R. A. Allen, C. E. Murabito, B. Park, J. V. Martinez de Pinillos, and A. Hunt “CD Reference Features with Sub-Five Nanometer Uncertainty” published in SPIE Proceedings Vol. 5752 (2005).

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Wafer-Level and Overlay Metrology

Technical Contacts:
R. Silver
T. Doiron

Goals

Provide technological leadership to semiconductor and equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily optical based methods used in overlay metrology and optical, wafer level critical-dimension (CD) metrology.

Customer Needs

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high throughput, lower cost of ownership metrology tools, which enable more dense sampling strategies has lead to a comprehensive program at NIST to both support and advance the optical techniques needed to make these high throughput overlay and photomask/wafer critical dimension measurements (see Fig. 1).

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in multiple sections of Table 116 of the 2005 ITRS as a difficult challenge for both >32 nm and <32 nm processes. Overlay measurements have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table 118a shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 118b, the problems are more acute for long term CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are two main strategic technical components of this project.

1. NIST has developed an overlay metrology tool that has undergone continuous development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is now used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. The technical strategy for overlay metrology is divided into two segments: (a) instrumentation development and the advance of overlay metrology techniques, and (b) the design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will

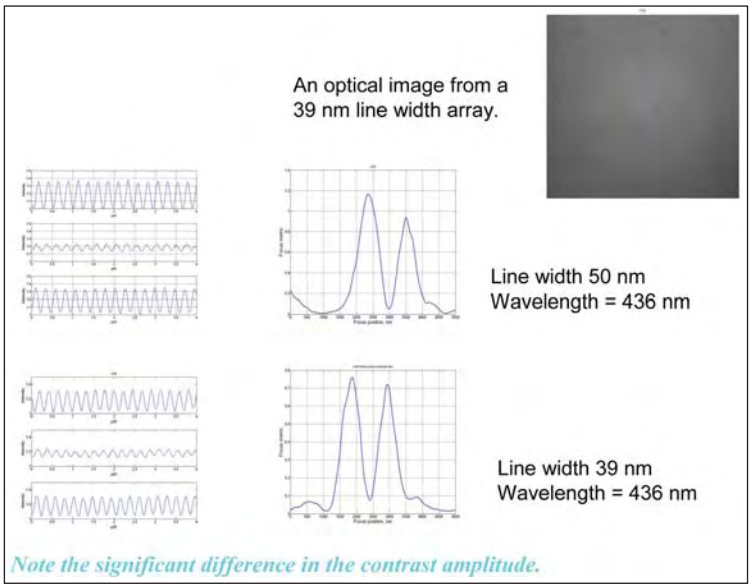

Figure 1. The image is a CCD camera image from an array of 39 nm CD features etched in polysilicon. The panels in the center column each show sets of profiles from the peaks and valleys of the through-focus focus metric curves, seen on the left. The upper two panels are from 50 nm CD linewidth arrays while the lower two are from the 39 nm linewidth array. These data were acquired with 0.4 illumination NA, 0.8 collection NA, and 436 nm wavelength.

translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS) (Fig. 2).

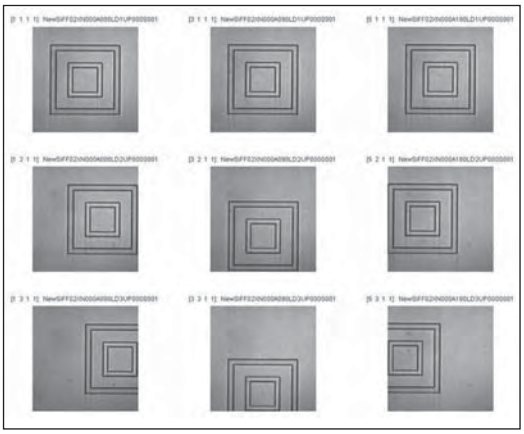

Figure 2. An example of reversal methods applied to determine WIS and the asymmetry of the target itself.

A set of standard artifacts and procedures, developed at NIST and published, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement system used for this component is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high resolution image capture with a full field CCD data acquisition system which has been fully characterized and calibrated. This instrument has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems have been evaluated and improved edge detection and CCD array calibration procedures have been implemented. These same methods for two-dimensional CCD array analysis are now being applied to optical component alignment error and aberration analysis.

Standard overlay artifacts have been fabricated in 200 mm and 300 mm wafers and calibrated for SRM distribution. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for example, Fig. 3.

We have also developed a series of new overlay targets and linewidth targets intended to enable the measurement of overlay and linewidth with device sized features. A variation of these targets allows

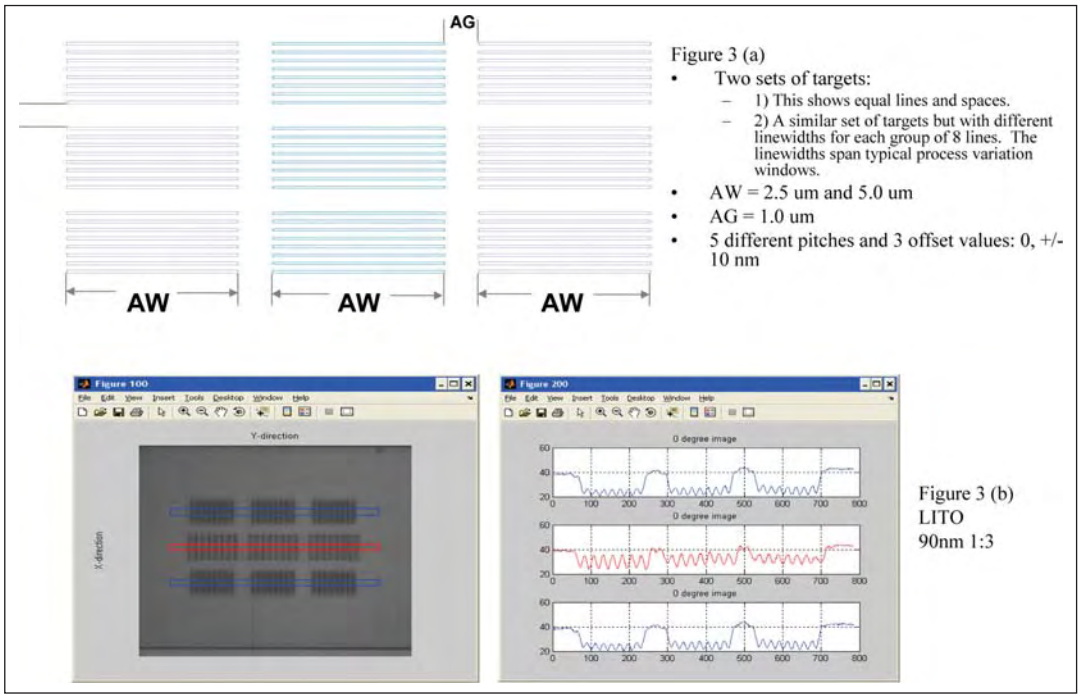

Figure 3. A schematic of the target designs is shown in (a). This is one example of several variations of this design. The lower part of the figure shows an image and a set of profiles for a target which reflects higher-order optical content.

in-chip targets to be placed throughout the active area of a die. These results have been published recently and collaborative work is progressing to develop the commercial applications to measure overlay using device sized features in targets of small overall dimension. There is also a comprehensive effort developing new high resolution overlay targets intended to enable the continued use of optical overlay measurements for the 65 nm node and beyond. An example of the latest high resolution targets is shown in Fig. 4.

DELIVERABLES:

- New alignment techniques and optical characterization tests for the overlay microscope, optics, and the *x-y* metrology stage have been recently published. These new techniques are used to determine the final uncertainties and tabulated combined uncertainty values for the latest set of SRM calibrations. These techniques include the characterization and calibration of complex optical alignment effects and illumination alignment and design errors and their effects on overlay output values. 2Q 2007
- Use the OMAG 4 metrology wafers from the SEMATECH collaboration for an evaluation of overlay calibration targets/wafers. Work with SEMATECH and the Overlay Metrology Advisory Group (OMAG) to develop a new set of calibration structures and techniques for calibration of industry tools. Apply these measurement protocols to optical system alignment, overlay errors, and evaluation of wafer and tool induced measurement errors. 3Q 2007
- Work with SEMI and SEMATECH in the development of new target designs and standards specifications for overlay metrology. This new specification is focused on bringing some standardization back to the overlay target designs and a move away from the growing number of proprietary overlay target designs, for calibration purposes. 4Q 2007

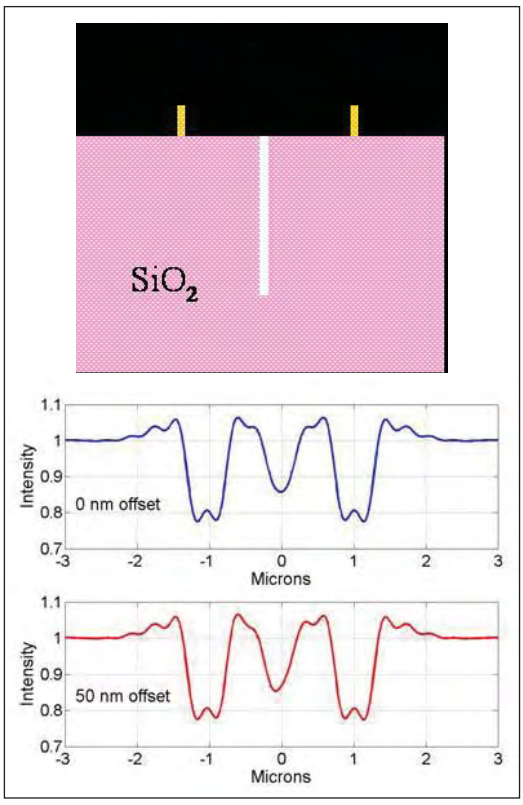

Figure 4. New overlay targets, which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.

Modeling the effects of all of the relevant feature properties encountered in overlay measurements and optical critical dimension measurements using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 5. NIST has a world class effort in optical modeling. This includes the comprehensive comparison of two rigorous coupled wave guide scattering models, a finite difference time domain-based model and the NIST-developed exact integral equation solver method. The latter method has become recognized as the most accurate in existence today.

DELIVERABLES:

- Compare and test the accuracy of new scattering models for line width evaluation. Develop a standard set of simulation values and make them available for comparison and verification by industry users. Publish results for the semiconductor industry. 2Q 2007

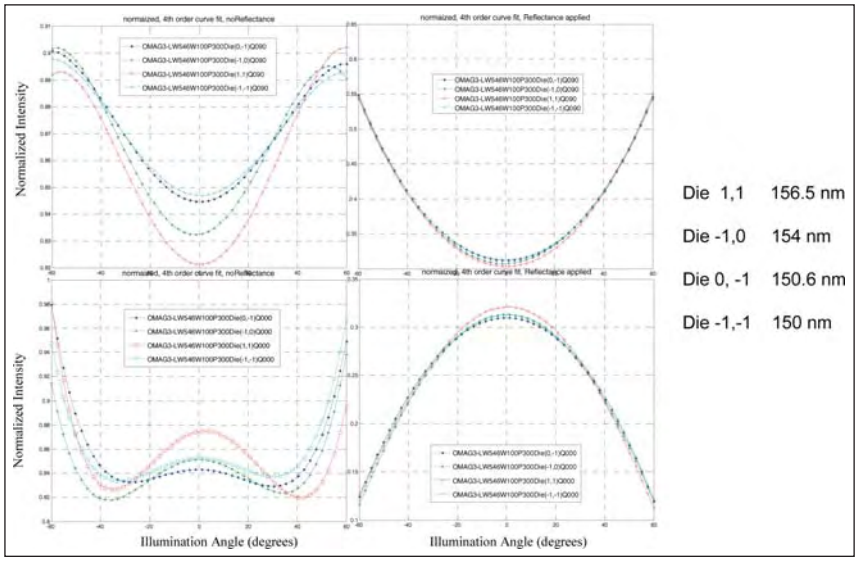

Figure 5. TM polarization is on top and TE is shown on the right. The vertical axes are units of normalized intensity and the horizontal axes are illumination angle in degrees. The data show good sensitivity to nm changes in linewidth. The image has been normalized to the background. A fourth order fit is used to analyze the data. The dynamic range is in part the result of the background normalization.

- Apply the through-focus focus-metric technique to illumination alignment and inhomogeneity. Compare experimental results with modeling results and publish results. 4Q 2007

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This methodology has demonstrated the possibility of using optical methods for line width and overlay metrology with targets composed of features smaller than 40 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. The technique is well suited for high resolution microscopy of metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods which can be suitably applied to device-sized features. Current metrology requirements are demanding higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques have shown promise as potential solutions to these significant metrology challenges. As a part of this project, we have constructed a new optical tool specifically intended to make this type of scatterfield measurement. This effort includes comprehensive optics modeling as well as a new optical configuration designed in-house. The optical design work includes a thorough examination of illumination effects and accurate methods to prepare optical illumination fields.

DELIVERABLES:

- Develop a comprehensive more accurate set of techniques to accurately measure optical illumination fields and publish results. Develop characterization methods to measure the collection optics set of aberrations and to perform optimum optical alignment. 3Q 2007
- Develop the capability to measure dense features which are smaller than 40 nm CD. Demonstrate the sensitivity to 1 nm changes in linewidth for densely positioned silicon structures, and develop modeling techniques for the accurate interpretation of measurements. 4Q 2007

ACCOMPLISHMENTS

■ Researchers from the overlay metrology project have submitted an invention disclosure of a new potential breakthrough in high resolution optical metrology. As a part of this disclosure, a new method has been proposed to measure overlay on targets which are very dense and only reflect zero order optical content. This new, image-based approach is capable of measuring overlay on features as small as 20 nm in dimension with densities to one to two line/space ratio. Sematech has worked jointly on this exciting new technique.

■ Staff from the OMP funded Precision Engineering Division (PED) optical metrology project met with several leading optical metrology tool manufacturers regarding recent advances in the scatterfield microscopy technique. The individual discussions included details about the new high resolution microscopy techniques being developed at NIST and their potential industrial application and implementation. Research in the area of high resolution optical methods is now being pursued at several companies with clear applications in overlay metrology and potential applications in optical based critical dimension metrology. The discussions largely focused on potential technology transfer between the NIST optical projects and development scientists at the optical metrology companies. Details on recent techniques for optical aberration measurements and on methods for evaluating Kohler illumination were covered.

■ NIST electromagnetic scattering code has been compared successfully in new applications of two other industry codes resulting in detailed published comparisons and study of arrayed targets. These model extensions are providing simulations results and guidance in optical tool design and metrology target designs for features currently down to 50 nm. The models are now capable of simulating targets in array formats as well as illumination at a single angle for analysis and development of scatterfield methods.

■ High resolution scatterfield optical techniques continue to be successful. The optics project funded as a competence has proved to be very productive. The cross laboratory proposal has produced several recent results which were published and presented at the recent SPIE Advanced Lithography meeting. The collaboration between the Manufacturing Engineering (MEL) and Physics (PL) laboratories has resulted in several publications this year including a paper in Applied Optics and a very substantial report to Sematech on the Limits of optical Critical Dimension metrology. This collaboration has developed back focal plane imaging and Scatterfield illumination techniques which have now resulted in improved experiment to theory agreement.

■ Significant industry interest in new high-resolution optical overlay target designs developed under the overlay metrology project. Following invited presentations at SEMATECH OMAG and Advanced Metrology Advisory Group (AMAG) metrology workshops, and discussions at SPIE, there was much interest in the new target designs and NIST is working closely with Sematech to implement the new designs on a metrology reticle and new set of test wafers.

■ NIST researchers have made model comparisons between the E. Marx developed optical scattering code, the Spectel company Metrologia metrology modeling package, a recently NIST developed code by T. Germer and the Panaramic Technologies FDTD code. Different material systems were compared as well as detailed material comparisons some of which were published recently. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement based on recent code enhancements and improvements. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results have been presented at SPIE Microlithography.

■ A paper titled "The Limits of Optical Critical Dimension Metrology" was presented by Rick Silver of the PED at the SPIE Advanced Lithography symposium in San Jose. The paper described an in depth study carried out by jointly PED optics researchers and Thom Germer of Physics Lab. The research was a summary of the results written up in an extensive study under contract to Sematech. This paper gave an overview of the optical critical dimension (OCD) limits from a fundamental perspective based on extensive modeling and statistical analysis. This paper was considered a benchmark for the future of OCD and its capabilities. The paper laid the groundwork for future studies on the practical limitations as the fundamental limits are well beyond those limits imposed by the variation of the targets themselves at the nanometer scale. Multiple electromagnetic models were compared and their stability and integrity verified prior to the analysis of the fundamental limits. The study gave measurement uncertainties for the different techniques in their fundamental application and evaluation of sensitivity to changes at the nanometer scale.

■ New scatterfield optical tool operational. The new scatterfield metrology tool has been assembled and is now operational in the Advanced Metrology Laboratories. This tool is specifically designed for performing sophisticated illumination engineering and scanning and has already produced important results. The new tool is fully computer controlled and based on a NIST designed optical column to enable access to a large conjugate back focal plane for illumination engineering. The new tool has been instrumental in investigating recent uncovered polarization dependent transmission effects in the optical train.

■ A paper was presented at SPIE Microlithography on new aspects of optical tool design focused on designing the 193 nm next generation Scatterfield microscope. A key aspect of this paper was a new treatment of the propagation of the electromagnetic scattered intensity profiles through the optical train. This approach is expected to give more accurate evaluation of the optical measurements by including the optical system aberration and its effects directly on them measured profiles. The paper included a further breakdown and analysis of Kohler illumination as used in many bright field microscopes and its application to the new 193 nm optical tool. The analysis has allowed NIST staff to identify key problems in the illumination such as polarization dependent transmission through the optics.

Collaborations

SEMATECH, IBM, Intel, KLA-Tencor, Nanometrics, Applied Materials, Motorola, AMD, and several other leading manufacturers and tool vendors.

Recent Publications

R. M. Silver, B. Barnes, R. Attota, J. Jun, M. Stocker, E. Marx, and H. Patrick, "Scatterfield Microscopy to Extend the Limits of Image-based Optical Metrology," To appear in Applied Optics, (2007).

R. M. Silver, T. Germer, R. Attota, B. Barnes, B. Bunday, J. Allgair, E. Marx, and J. Jun, "Fundamental Limits Optical Critical Dimension Metrology: A Simulation Study," SPIE Proc. Feb. Vol. 6518 (2007).

Y. J. Sohn and R. Silver, *"Kohler Illumination Analysis for High Resolution Optical Metrology using 193 nm Light,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6518, (2007).

Bryan M. Barnes, Lowell P. Howard, Jay Jun, Pete Lipscomb, and Richard M. Silver, "Zero-order imaging of device-sized overlay targets using scatterfield microscopy," *Proc. SPIE* **6518**, 65180F (2007).

R. M. Silver, R. Attota, B. Barnes, and H. Zhou, "A Theoretical and Experimental Evaluation of Scatterfield Microscopy for use in Patterned Defect Inspection," Sematech Tech Transfer Doc, Feb. (2007).

R. Attota and R. M. Silver, “Optical Illumination and Critical Dimension Analysis using the Through-focus Focus-metric Method,” SPIE Vol. 6289, p. 6289OQ, 2006

R. Attota and R. M. Silver, “Optical Illumination and Critical Dimension Analysis using the Through-focus Focus-metric Method,” SPIE Vol. 6289, p. 6289OQ, 2006.

B. Barnes, L. Howard, and R. M. Silver, “Illumination Optimization for Optical Semiconductor Metrology,” SPIE Vol. 6289, p. 6289OP, 2006.

R. M. Silver, B. Barnes, R. Attota, J. Jun, J. Filliben, J. Soto, M. Stocker, P. Lipscomb, E. Marx, H. Patrick, R. Dixson, and R. Larrabee, *“The Limits of Image-based Optical Metrology,”* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520Z (2006).

R . Attota, R. M. Silver, M. Bishop and R. Dixson, *“Optical Critical Dimension Measurement and Illumination Analysis using the Through-focus Focus-metric,”* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520K (2006).

Y. J. Sohn, B. Barnes, L. Howard, R. Silver, R. Attota, and M. Stocker, *“Kohler Illumination in High Resolution Optical Metrology,”* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61523S (2006).

H. Patrick, R. Attota, B. Barnes, T. Germer, M. Stocker, R. M. Silver, and M. Bishop *“Scatterfield Microscopy using back focal plane imaging with an engineered illumination field,”* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520J (2006).

P. Lipscomb, J. Allgair, B. Bunday, M. Bishop, R. Silver, R. Attota, and M. Stocker, *“Calibration Optical Overlay Measurements,”* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 615211 (2006).

D. Kandel, M. Adel, A. Frommer, V. Levinski, A. Rapoport, and R. M. Silver, *“Imaging Simulations of Optimized Overlay Marks with Deep Sub-resolution Features,”* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61522X (2006).

Front-End Processing Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The current gate stacks, currently poly silicon over SiO_2 and SiON dielectrics, are being replaced by high κ – metal gate stacks. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology, and overall reliability metrology.

Wafer and Chuck Flatness Metrology

Goals

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project provides measurement and technology infrastructure to support the measurement of wafer thickness variation of 300 mm silicon wafers, and surface flatness of chucked wafers.

Customer Needs

With the evolution of exposure tools for optical lithography towards larger numerical apertures, the semiconductor industry expects continued demand for improved wafer flatness at the exposure site. The allowable site flatness for 300mm wafers is expected to be less than 45 nm by 2010 and it may be as low as 25 nm by 2015 according to the International Technology Roadmap for Semiconductors (ITRS 2006). This requires wafers with low thickness variation and presents a challenge for both wafer polishing and metrology tools, which must be capable of meeting the specifications. We are addressing the need for standard 300 mm wafers with calibrated thickness variation with the Improved Infrared Interferometer (IR^3) at NIST. The interferometer is used for independent, traceable wafer thickness calibrations, which enable manufacturers of wafers and wafer metrology instruments to certify the performance of their metrology instruments. In addition, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometeR" (XCALIBIR).

Technical Strategy

1. The Improved Infrared Interferometer (IR^3) was developed at NIST for the characterization of the thickness variation of silicon wafers with diameters up to 300 mm. The IR^3 interferometer is an infrared phase-shifting interferometer, operating at a wavelength of 1550 nm which measures the thickness of low-doped silicon wafers up to 300 mm diameter in a single measurement (see Fig. 1 and Fig. 2). The interferometer may be used in several configurations with collimated and spherical test wave-fronts. The collimated wave-front mode is the current focus of the project. In this method, the planar infrared wave-front is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wave-fronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation.

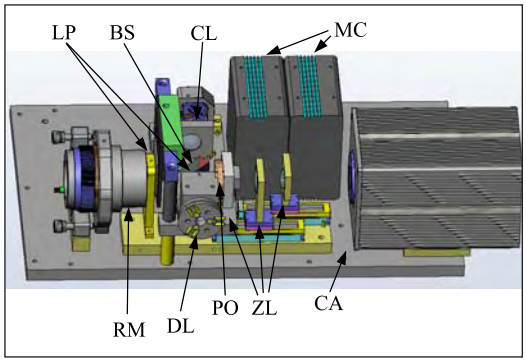

Figure 1. Solid model of NIST's improved infrared interferometer (IR^3). The main components of the interferometer are indicated: collimator lens (CL), polarizing beam splitter (BS), λ/4-plates (LP), reference mirror for the Twyman-Green mode (RM), diverger lens (DL), polarizer (PO), zoom lens (ZL), motion controllers for the zoom lens (MC), and camera (CA). The size of the base plate is approximately 20 cm × 30 cm.

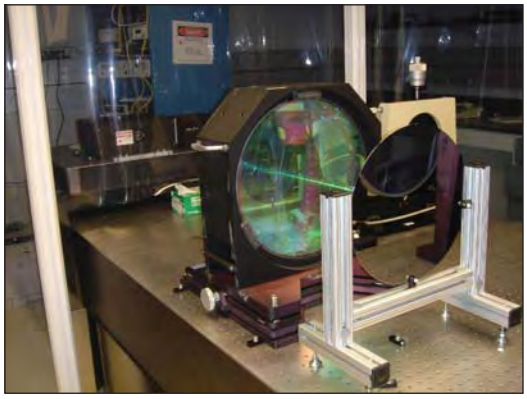

Figure 2. Test arm of the IR^3 interferometer. shown are the collimator lens and the beam expander together with a 300 mm silicon wafer. The insensitivity of the measurement to vibration permits the use of a simple wafer mount.

DELIVERABLES:

- Develop complete uncertainty analysis for thickness and thickness variation measurements. 4Q 2007

Technical Contacts:
U. Griesmann
Q. Wang
J. Soons

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer thickness metrology has led to unprecedented levels of thickness correction on industry standard 300 mm Si wafers, when combined with deterministic finishing technologies such as MRF. The collaboration with NIST has been a significant and crucial component to the success of this effort."

Paul Dumas and Marc Tricard
QED Technologies –
A subsidiary of Cabot
Microelectronics Corp,
Rochester, NY

- Install laser with wide tuning range to enable measurements of very thin wafers. 3Q 2007
- Calibrate the thickness variation of a set of wafers as NIST Standard Reference Materials (SRM), which will be made available for purchase. 4Q 2007

2. Measurements of the flatness of chucked wafers are made with XCALIBIR, a general purpose, 300 mm aperture phase measuring interferometer operating with visible light at 633 nm. The interferometer is housed in a clean room, which eliminates dust particles between chuck and wafer. The results are used to evaluate the influence of wafer-chuck interactions on the chucked wafer flatness.

Accomplishments

IR^3 has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes and the spatial resolution of the detector was doubled to 2 pixels/mm. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty. In addition, a new laser with wide tuning range will make it possible to measure very thin wafers. The optical components in the IR^3 interferometer were improved to reduce the measurement noise. Wavelength phase-shifting has been implemented and a TTV map repeatability of 5 nm peak to valley has been achieved for 300 mm wafers. The IR^3 interferometer is now housed in a clean room, which enables us to make calibration measurements of wafers supplied by industry customers.

The flatness of 200 mm and 300 mm diameter wafers on pin chucks was explored using the XCALIBIR interferometer in a collaboration with Wavefront Sciences Inc., Albuquerque, NM.

IR^3 was used to develop a sub-aperture magneto-rheological polishing process for the finishing of 300 mm wafers with ultra-low thickness variation in collaboration with QED Technologies. Figure 3 shows that a total thickness variation (TTV) of about 40 nm could be achieved. The SFQR resulting from the thickness variation (assuming an ideal chuck) is shown in Fig. 4. These results demonstrate that a suitable sub-aperture finishing process can achieve the exposure site flatness expected by the ITRS for 2015.

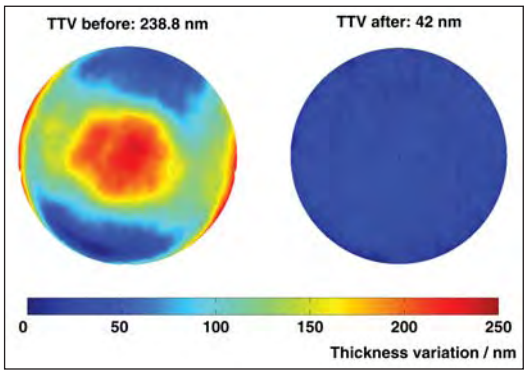

Figure 3. Wafer thickness variation of a 300 mm silicon wafer before and after sub-aperture polishing. The total thickness variation was reduced from 238 nm to 42 nm over a 292 mm aperture (4 mm edge exclusion).

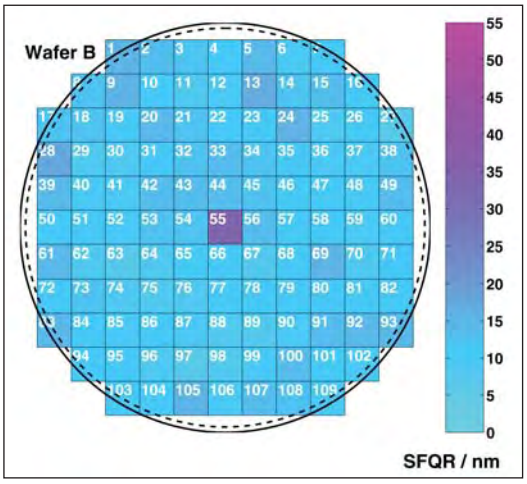

Figure 4. SFQR of the wafer shown in Fig. 3 after sub-aperture finishing for 25 mm x 25 mm sites with the same edge exclusion (4 mm) as in Fig. 3.

Collaborations

During the course of this project, we have interacted with several companies on problems relating to wafer flatness metrology and chucked wafer flatness.

1. WaveFront Sciences: Flatness measurements of free form and chucked wafers for the validation of a metrology tool developed by WaveFront Sciences.
2. MEMC Electronic Materials: Wafer thickness standard development.
3. Siltronic: Wafer thickness standard development.
4. Intel: Development of very thin silicon thickness standards.
5. QED Technologies: Development of ultra-flat 300 mm silicon wafers.

6. Lumetrics: Evaluation of Lumetrics thickness gauging technology for wafer thickness metrology.

Recent Publications

U. Griesmann, Q. Wang, M. Tricard, P. Dumas, and C. Hall, "Manufacture and Metrology of 300 mm Silicon Wafers with Ultra-Low Thickness Variation," *AIP Proceedings of the 2007 Conference on Characterization and Metrology for Nanoelectronics*, Gaithersburg, MD, USA (2007)

Q. Wang, U. Griesmann, and R. S. Polvani, "Interferometric Thickness Calibration of 300 mm Silicon Wafers," *Proceedings of the ASPE Topical Meeting on Precision Interferometric Metrology*, Middletown, CT (2005).

U. Griesmann, Q. Wang, and T. D. Raymond, "Optical Flatness Metrology for 300 mm Silicon Wafers," *AIP Proceedings of the 2005 Conference on Characterization and Metrology for ULSI Technology*, University of Texas, Richardson, TX, USA (2005).

D. R. Neal, P. Pulaski, T. D. Raymond, D. A. Neal, Q. Wang, and U. Griesmann, "Testing highly aberrated large optics with a Shack-Hartmann wavefront sensor," Proc. SPIE 5162, 129-138 (2003).

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Modeling, Measurements, and Standards for Wafer Surface Inspection

Goals

Our goals are: (1) provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces; (2) develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS); and (3) investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, nonmetallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem exist for particles on bare silicon, on non-metallic films, and on wafer backsides, while it is anticipated that no acceptable solutions will exist for metallic films in 2010. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. For new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards *in situ* sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by 13 different Scanning Surface Inspection System (SSIS) indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. The SIA roadmap specifies the need for accurate calibration particles to size critical semiconductor components scaling to 32 nm or smaller by as early as 2008.

By 2010, at the 45 nm node, particles having diameters 22.5 nm must be detectable on bare silicon and nonmetallic films, with 54 nm on metallic films. No known solutions exist at this time. [2006 ITRS, Yield Enhancement, Table 113a]

Technical Strategy

There are two major strategies for improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvements in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for

Technical Contact:
T. A. Germer

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.
VLSI Standards, Inc.

particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) on 300 mm wafers (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLES: Perform measurements of scatter at 266 nm from various films to assess the particle detection limits on those films. 2Q 2007

Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

2. Theoretical Light Scattering Calculations – The focus of our theoretical work is on: (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLES: Publish response curves for a variety of scattering geometries for particles on wafers with blanket films. 3Q 2007

3. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle diameters as small as 50 nm. However, discrepancies have been noticed between PSL measurements using the DMA, and measurements using light scattering on the surface of a wafer. These discrepancies are possibly due to the PSL particles deforming on the bottom as they adhere to the wafer. This problem will be investigated by comparing measurements of the PSL particles to measurements of silica particles, which are less likely to deform when they contact the wafer surface. Measurements will be performed using both the DMA and light scattering instruments.

DELIVERABLES: Compare measurements of silica particles to PSL particles. 4Q 2007

4. Resource on Particle Science – Over the past five years, the particle-related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES: Provide technical support to the SEMI Advanced Wafer Surface Inspection System task force. 4Q 2007

Accomplishments

■ Completed and certified the measurements for new NIST Standard Reference Materials (SRM). Measured and certified SRM 1964, particles with a nominal diameter of 60 nm. Also measured and certified SRM 1963a, with a nominal diameter

of 100 nm, to replace the previous 100 nm SRM 1963, which was corrupted due to agglomeration. SRM 1963a and SRM 1964 are currently available for purchase.

■ Completed initial screening process and preliminary measurements for development of a 30 nm SRM. Identified primary and secondary candidate samples for the 30 nm SRM, based on diameter and distribution measurements. Researched measurement uncertainty for particles smaller than 50 nm and devised strategies for reducing the uncertainty.

■ Developed and improved the NIST Calibration Facility, which uses Differential Mobility Analysis for sizing monodisperse spheres in the size range of 50 nm to 400 nm. Reduced the expanded uncertainty to 1.0 % of the particle size by correlating the slip correction to the measured particle size. Increased resolution and accuracy of measurements through improved equipment and intermediate measurements.

■ Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

■ Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

■ In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

■ Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO_2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

■ Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 4200 copies of the library have been downloaded from the web. The Modeled Integrated Scatter Tool (MIST), a Windows application for calculating integrated scatter, was released in June 2004.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by the uncertainty in the shape of the particle on the surface. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

■ Assisted in revising SEMI M53, a practice for calibrating scanning surface inspection systems, by developing a model-based calibration scheme that matches measured signals from PSL spheres to the predictions of a theoretical model. The accepted model for scattering by the spheres is specified in the standard as that provided by the MIST program. The new method has several advantages over the previous method, including: less sensitivity to changes in availability of specific size standards, improved accuracy, less variability between instruments, and an ability to

extract a quantitative accuracy from the calibration. The expanded uncertainty found by applying the calibration to a commercial instrument was better than 1 % of the diameter, Fig. 2.

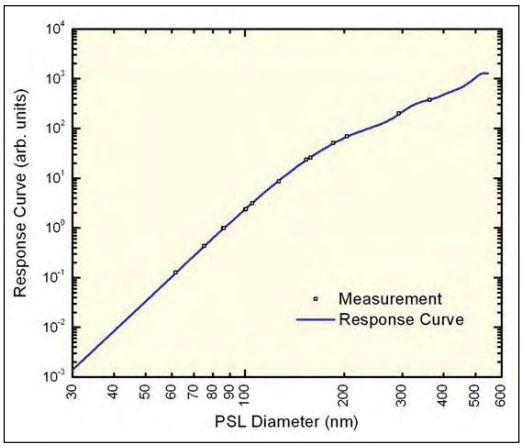

Figure 2. Sample calibration of a commercial wafer scanner using the new SEMI M53 method. The relative expanded uncertainty in particle diameter has been reduced to less than 1 %.

Collaborations

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

Donnelly, M. K., Yang, J. C., "Screening Candidates for 30 nm Spheres," NISTIR 7345, August 2006.

Mulholland, G. W., Donnelly, M. K., Hagwood, C., Kukuck, S. R., and Hackley, V. A., "Measurement of 100 nm and 60 nm Particle Standards by Differential Mobility Analysis," J. Research NIST **111**, 257–312, 2006.

Thomas A. Germer, "Measuring Interfacial Roughness by Polarized Optical Scattering," in *Light Scattering and Nanoscale Light Scattering*, Alexei A. Maradudin, Ed., (Elsevier, New York, 2007) Chapter 10, pp. 259–284.

Thomas A. Germer and George W. Mulholland, "Particle Size Metrology: Comparison Between Aerosol Electrical Mobility and Laser Surface Light Scattering Techniques," in *Characterization and Metrology for ULSI Technology 2005*, D.G. Seiler, A.C. Diebold, R. McDonald, C.R. Ayre, R.P. Khosla, S. Zollner, and E.M. Secula, eds., Proc. AIP **788**, 579–583 (2005).

Jung Hyeun Kim, Sheryl H. Ehrman, George W. Mulholland, and Thomas A. Germer, "Polarized light scattering by dielectric and metallic spheres on oxidized silicon surfaces," Appl. Opt. **43**(3), 585–591 (2004).

J. H. Kim, S. H. Ehrman, and T. A. Germer, "Influence of particle oxide coating on light scattering by submicron metal particles on silicon wafers," Appl. Phys. Lett. **84**(8) 1278-1280 (2004).

J. H. Kim, S. H. Ehrman, and T. A. Germer, "Influence of particle oxide coating on light scattering by submicron metal particles on silicon wafers," Appl. Phys. Lett. **84**(8) 1278-1280 (2004).

Front-End Materials Characterization

Goals

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. Major focus is placed on metrology requirements from the 2005 International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) structural and elemental analysis at the device level, including SIMS and HRTEM, and (2) metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project develops new methods for depth-profiling polymeric materials by Secondary Ion Mass Spectrometry (SIMS), defines optimum procedures for ultra-high depth resolution, develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as, characterizes the accuracy and reliability of existing methods. Materials of interest include high-κ and low-κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. High Resolution Transmission Electron Microscopy (HRTEM) is being developed as a chemical tomography tool for determining 3-D elemental distributions in advanced materials.

(3) Determine the work function, band offset, and interfacial defect structures of high-κ combinatorial metal electrode stacks systems by implementing a combination of techniques including Scanning Kelvin Probe Microscopy (SKPM), internal photoemission (IPE), ellipsometry (SE), backside FTIR, and external photoemission (Soft XPS and Inverse photoemission), and theoretical modeling.

Customer Needs

The Front-End Materials Characterization project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack processes and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2005 International Technology Roadmap for Semiconductors (ITRS) and 2006 Update near-term (through 2009) difficult challenges for front-end processes include: *metrology issues associated with gate dielectrics film thickness and gate stack electrical and materials characterization, introduction of metal gate electrodes with appropriate workfunctions, and metrology issues associated with 2-D dopant profiling. Metrology needs for Thermal/thin films, Doping Technology, SOI, and strained-silicon are discussed in the Metrology section of the 2005 ITRS and 2006 Update*.

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements.

The ITRS identifies structural and elemental analysis at devices dimensions (for example 3-D dopant profiling) as one of the difficult challenges beyond 2009. Offline secondary ion mass spectroscopy has been shown to provide the needed

Technical Contacts:
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D. Simons: SIMS
J. Small: TEM, X-ray detectors
J. Suehle: Electrical Characterization
N. Nguyen: IPE, SE

precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. The ITRS requirements are for at-line dopant profile concentration measurements with precision of 4 % in 2005, decreasing to 2 % precision for the 2010 through 2018 timeframe. The lateral/depth resolutions for 2-D/3-D dopant profiling decrease from 3.5 nm in 2005 to 1.5 nm in 2012. Complete specifications are given for the short term in Table 120a on pages 12-13, and for the long term in Table 120b on pages 14-15 of the 2006 Update to the Metrology section. The need for advances in image and spectral modeling for TEM and STEM applied to 3-D atomic imaging and spectroscopy is discussed under Emerging Research Materials and Devices in the Metrology section of the 2005 ITRS.

Technical Strategy

The 2006 Update to the ITRS expressed as difficult challenges: "starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams," and "measurement of complex material stacks and interfacial properties including physical and electrical properties" (page 2, Table 116, Metrology Section). Our focus areas include development of refined metrology methods and standards for SIMS and TEM, developing improved X-ray detection capabilities for SEMs and electron microprobes, and the characterization of high-κ metal gate interfaces, including band offsets and barrier heights.

Structural and Elemental Analysis at the Device Level, Including SIMS and HRTEM

Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We have organized an international round robin study through ISO committee TC201 to investigate the parameters that must be controlled to make highly repeatable dose measurements of As with SIMS instruments. In addition to improved repeatability for dopants, the ITRS roadmap also requires increased SIMS detection limits for trace metal and organic contamination analysis of semiconductor devices. We are also working on novel methods to enhance detection limits for common metal contaminants by increasing the ionization efficiency during the SIMS sputtering process.

DELIVERABLE: Measure detection limits of selected trace metals on silicon using high transmission/high mass resolution SIMS system. 2Q 2007

Analysis of trace metal and organic contamination on silicon surfaces is a high priority of the ITRS roadmap. To utilize effectively tools such as secondary ion mass spectrometry for trace contamination on silicon surfaces, suitable trace standards must be developed. Over the past 20 years, piezoelectric drop-on-demand ink-jet printing has evolved into a precision microdispensing technology with a diverse range of applications. Examples of applications include desktop color printers, printing and synthesis of DNA arrays and printing of molten solder for use as electrical interconnects on integrated circuits. We are exploring the possibility of using ink-jet technology to print elemental and organic contamination standards on silicon. Piezoelectric printers are capable of printing single microdrops of fluid at the rate of thousands of drops per second. Each drop contains a known concentration of the material of interest. Large concentration ranges are possible simply by varying the number of drops printed. Our first attempts will explore ink-jet printing of organic test dyes on silicon with subsequent characterization by SIMS. Once standard operating procedures are developed for ink-jet printing, it should be feasible to produce standards, (both organic and trace metal) for quality control and calibration of a variety of analytical techniques including SIMS, XPS, AES, EPMA, TXRF and others.

DELIVERABLES: Develop methods for depositing known amounts of organic and inorganic reference materials on silicon surfaces using inkjet printing technology. 2Q 2007

As integrated circuit dimensions shrink to the sub-micrometer regime, there is continued need for accurate and quantitative dopant depth profiling with ultra-high-depth resolution. To probe shallow dopant profiles in Si and other materials, SIMS instruments typically utilize very low en-

ergy primary ion beams to bombard the sample surface. In this case, it is difficult to obtain a well-focused and high current density beam, especially in a magnetic sector SIMS instrument. Recently, there has been growing interest in using molecular ion beams for depth profiling. When a molecular primary ion beam impacts the surface, it dissociates into its constituent atoms with each atom retaining a fraction of the initial energy of the cluster. This process can lead to impact energies on the order of a few 10's of electron volts and a corresponding reduction in the depth of penetration of the primary ion. This process may potentially allow for ultra high resolution depth profiling. In this project, we will utilize C_{60}^+ and Bi_3^+ cluster primary ion beam sources at NIST to sputter depth profile Si, GaAs, SiC, and multiple delta-layers test materials.

Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. In these cases, the achievable depth resolution is limited not by the penetration depth of the primary ion but by the topography induced by the sputtering process itself. We will also explore the use of cluster bombardment SIMS for reduction of sputter induced topography in metal films. This approach will be applied to study depth profiling analysis of gold diffusion in copper and the depth distribution of blanket metals films (copper metallization on silicon).

DELIVERABLES: Evaluate possible applications of a Bi cluster ion source for ultrashallow depth profiling. 2Q 2007

Measurement of the barrier height and determination of the band structure is not straightforward. Recent work by numerous researchers has shown that the measured band offset between a metal gate electrode and high-κ gate dielectric is dependent on numerous factors including composition, structure, and thickness of both the metal gate electrode and the high-κ dielectric. Because of limitations associated with any single technique, we believe that determination of band offsets and work functions requires the use of an array of techniques and the broad expertise available at NIST. We will focus our efforts on the following measurements: standard Capacitance-Voltage (C-V) and tunneling current-voltage (I-V) measurements, internal photoemission, Kelvin probe, and soft X-ray and inverse photoelectron spectroscopy.

DELIVERABLES: Improve efficiency of internal photo emission system and demonstrate performance on metal/high-κ GaAs structure to determine band offsets. 2Q 2007

New technologies being considered when silicon technology can no longer be scaled include alternative high mobility substrates including GaAs and InGaAs. Unfortunately, there is no high quality gate dielectric like silicon dioxide that can be directly grown on the substrate. Research is being conducted to study materials systems using a high-κ gate dielectric material deposited directly on the GaAs or InGaAs substrate. Innovative interfacial chemistry is required to provide a good interface free from defects and trapping states. We are using internal photo emission and spectroscopic ellipsometry to study optically active defects at the interface after various chemical treatments. Electrical test structures are being fabricated to correlate the optical results with electrical characterization.

DELIVERABLES: Prepare GaAs surface and deposit high-κ films by NIST-CSTL ALD processes and conduct optical characterization. 4Q 2007

Accomplishments

Implementation of C_{60}^+ Cluster Ion SIMS Capability

Previous efforts with cluster ion sources used for analyzing both organic and inorganic materials have been very successful. Minimization of beam-induced damage in organic materials has allowed depth profiling of polymers such as photoresists and enhanced ion yields for high-molecular weight fragments. Inorganic material analysis has benefitted in the area of ultra-shallow depth-profiling as well as for analysis of some particularly difficult systems such as metal multi-layers stacks. We have investigated the use of a commercially available C_{60}^+ ion source on the NIST magnetic sector SIMS instrument. We have produced stable ion beams of C_{60}^+ and C_{60}^{2+} with typical currents approaching 20 nA under conditions that allow for several hundred hours of operation. The beam can be focused into a spot size of ~1 μm allowing micrometer spatial scale mapping of patterned wafers. Optimal experimental conditions have been defined to allow for depth profiling analysis of silicon wafer samples, delta doped structures and metal multilayers. One of the critical issues for optimization of this source for analysis of silicon wafer samples is the primary ion impact energy of the C_{60}^+. As shown in Fig. 1 (next page), we have found that at impact energies below ~12 keV,

carbon deposition is the dominant process during bombardment precluding the acquisition of depth profiles from the wafer sample. Successful depth profiles are only achieved at the impact energies exceeding 12 keV. The deposition effect may be useful for lithographic applications as it allows direct ion beam writing of a conductive carbon layer on silicon.

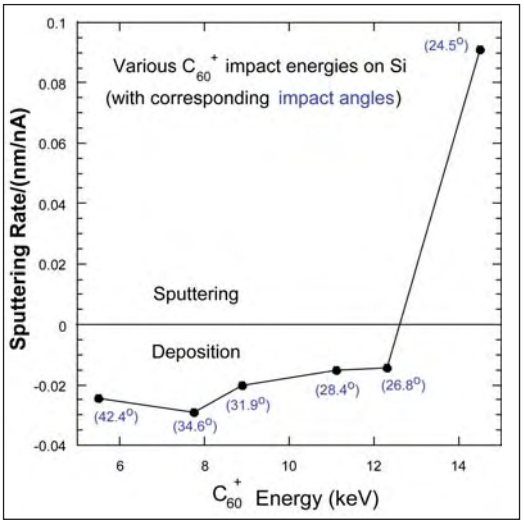

Figure 1. Sputtering or deposition rate for C_{60}^+ on Si as a function of impact energy (angle of incidence in parentheses).

Depth Profiling of Organic Overlayers Using SIMS

Organic photoresists and low-κ dielectric materials are key components for front end semiconductor processing. There is also a growing interest in the use of organic semiconductor materials for organic light emitting diodes and organic thin film transistors. In anticipation of a growing need for metrology tools to characterize these types of materials, we are developing new approaches to characterize the chemical composition and in-depth distribution of organic thin films on silicon. Typically, the use of ion beam sputtering techniques, such as secondary ion mass spectrometry (SIMS), results in extensive chemical degradation of organic thin films such as photoresists or organic light emitting diodes. However, we have found that cluster primary ion bombardment SIMS can minimize this degradation allowing for intact characteristic ions to be obtained throughout the depth of the film. Furthermore, it appears that analyzing these organic materials at cryogenic temperatures provides further reduction in beam-induced damage. In this project, an SF_5^+ polyatomic primary ion source was used to depth-profile poly(methyl methacrylate) (PMMA) photoresist by SIMS at a series of temperatures from -75 °C to 150 °C. The depth profile characteristics (*e.g.*, interface widths, sputter rates, damage cross sections, and overall secondary ion stability) were monitored as a function of temperature for atactic, syndiotactic and isotactic PMMA. At low temperatures it was found that the secondary ion stability increased considerably. In addition, the interfacial widths were significantly smaller. Examples of this increased stability at low temperatures for syndiotactic and isotactic PMMA are illustrated in Fig. 2 for the PMMA fragment at m/z = 69. Corresponding AFM images indicated that there was also decreased sputter-induced topography formation at these lower temperatures as illustrated in Fig. 3. Higher temperatures were typically correlated with increased sputter rates. However the improvements in interfacial widths and overall secondary ion stability were not as prevalent as was observed at low temperatures. The importance of the glass transition temperature (T_g) on the depth profile characteristics was also apparent. The sputter properties of isotactic and syndiotactic PMMA differed greatly. Isotactic

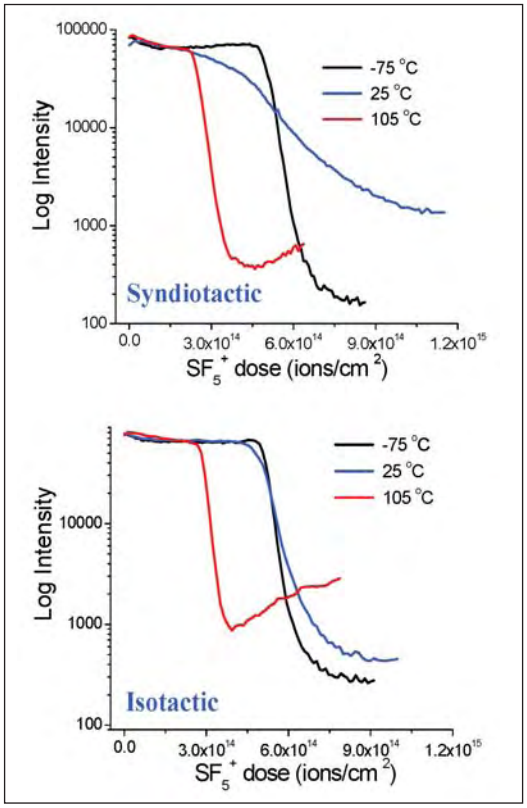

Figure 2. Intensity of m/z = 69 (fragment characteristic of PMMA) as a function of increasing SF_5^+ dose for syndiotactic and isotactic PMMA at three different temperatures.

PMMA showed sharper interface widths and better depth profile characteristics from 0 °C to 65 °C over those observed for syndiotactic or atactic PMMA. The results of this study demonstrate that it is possible to monitor the chemical composition of photoresist thin layers on silicon by analyzing the samples at cryogenic temperatures. This work has resulted in collaborations with International Sematech to prepare thin films of a PMMA photoresist on silicon that will be used as standards for compositional depth profiling.

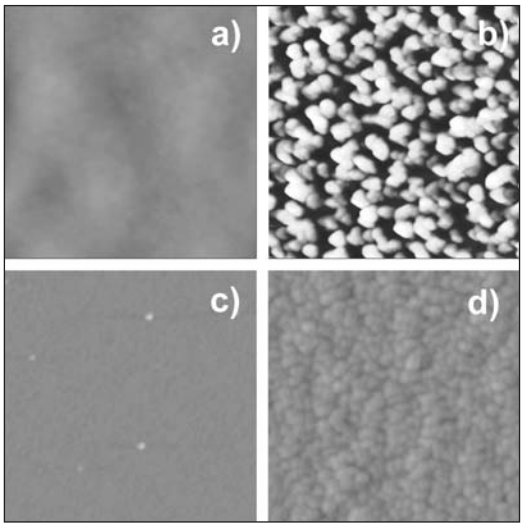

Figure 3. Atomic Force Microscopy (AFM) topography images (1 μm x 1 μm area) of SF_5^+ sputtered crater bottoms at different temperatures: (a) PMMA surface, R_{rms} = ~0.85 nm, (b) 25 °C, R_{rms} = ~11.37 nm, (c) -75 °C, R_{rms} = ~0.274 nm, and (d) 125 °C, R_{rms} = ~1.00 nm.

Round-Robin Study of Arsenic Implant Dose Measurement in Silicon by SIMS

An international round-robin study was undertaken under the auspices of SIMS subcommittee SC 6 of International Organization for Standardization Technical Committee TC 201 on Surface Chemical Analysis. The purpose of the study was to determine the best analytical conditions and the level of interlaboratory agreement for the determination of the implantation dose of arsenic in silicon by SIMS. Motivations for this study were: (a) the relatively poor interlaboratory agreement that was observed in a previous round-robin study before a certified reference material had become available; (b) the observation that the use of Si_3^- as a matrix species combined with AsSi- detection may result in improved measurement repeatability compared with Si_2^-; and (c) the observation that point-by-point normalization can extend the linearity of SIMS response for arsenic in silicon beyond $1x10^{16}/cm^2$.

Fifteen SIMS laboratories participated in this study, as well as two laboratories that performed Low-energy Electron-induced X-Ray Emission Spectrometry (LEXES) and one that made measurements by Instrumental Neutron Activation Analysis (INAA). The labs were asked to determine the implanted arsenic doses in three unknown samples using as a comparator Standard Reference Material 2134, with a certified dose of $7.33x10^{14}$ atoms/cm^2. The use of a common reference material by all laboratories resulted in much better interlaboratory agreement than was seen in the previous round-robin that lacked a common comparator. The relative standard deviation among laboratories was less than 4 % for the medium-dose sample, and somewhat larger for the low- and high-dose samples (see Fig. 4). The high-dose sample showed a significant difference between point-by-point and average matrix normalization because the matrix signal decreased in the vicinity of the implant peak, as previously observed. The average dose from point-by-point normalization was in close agreement with that determined by INAA, indicating that the SIMS relative sensitivity factor approach is valid for arsenic concentrations in silicon as high as 4 atom percent.

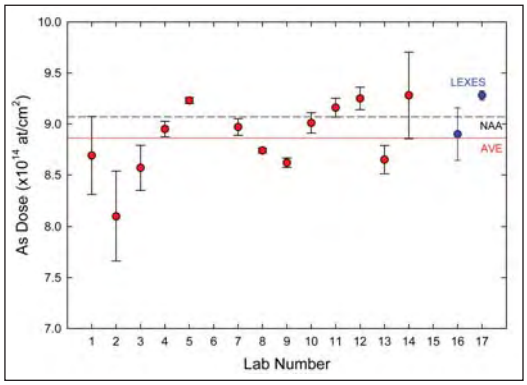

Figure 4. As round robin results for medium dose sample with point-by-point normalization to matrix signal. SIMS lab results shown in red with error bars indicating within-lab repeatability. Relative standard deviation among labs is 3.9 %. Also shown are LEXES results (blue dots), average of SIMS lab results (red line), and NAA result (black dashed line).

Enhanced Performance of Microcalorimeter X-Ray Detector

The NIST transition edge sensor (TES) microcalorimeter X-ray detector is a versatile instrument that combines the high resolution of wavelength-dispersive detectors with the extended range of energy-dispersive detectors. The detector is a small calorimeter operated at a low temperature (70 mK). The temperature change caused by the absorption of single X-ray photons is registered by a current through the transition edge sensor — a thin metal film that undergoes a superconducting-normal transition at the operating point. Our present detector has demonstrated a FWHM resolution of 4.4 eV at 5.9 keV. The technology of microcalorimeters is more complicated than most X-ray detectors, so that a new set of operating considerations has emerged in the process of developing it as an analytical instrument.

We report here the first operation of the NIST TES microcalorimeter X-ray detector to perform quantitative analysis of a sample with an electron probe. The detector element is mounted at the end of a probe projecting from the dewar into the electron microscope. The probe extends horizontally, which requires a sample mounting angle of 45° to optimize the yield with a vertical electron beam. The sample was analyzed using a microbeam probe with a beam current of 7 nA at an energy of 12 keV.

The detector is a microcalorimeter element 400 μm square, located approximately 30 mm from the source of the radiation. Its energy range is 400 eV to 7 keV. Count rates of 50/s to 170/s were registered while taking spectra of the sample and related standards. Spectra were processed using conventional analog pulse amplifiers and pulse-pileup circuitry modified for the relatively long period of the microcalorimeter pulses. The pulses were recorded with a 16K channel multichannel analyzer board with an approximate resolution of 0.5 eV/channel. All spectra were obtained in 1000s live time.

The sample was the K-411 glass which is part of the NIST Standard Reference Material 470, Mineral Glasses for Microanalysis, a standard intended for use with electron probe microanalysis and SIMS. It contains previously analyzed quantities of SiO_2, MgO, FeO, and CaO. Spectra were also taken of reference standards consisting of Fe, SiO_2, MgO, and chloroapatite [$Ca_5(PO_4)_3Cl$]. A spectrum of K-411 glass used in the quantitative analysis is shown in Fig. 5.

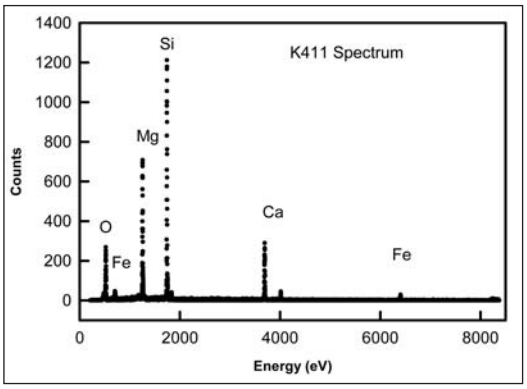

Figure 5. Spectrum of the K-411 Standard Reference Material glass taken with the NIST TES microcalorimeter X-ray detector excited by an electron beam.

Calculations were carried out using a Monte Carlo procedure which varied the composition of the respective elements. The maximum deviation from the concentrations certified in the NIST SRM in the first round of analysis is 2 %. The work demonstrates that the NIST TES microcalorimeter detector has considerable potential for the analysis of X-ray fluorescence lines which would overlap in current energy-dispersive detectors or would be too low in energy for most wavelength-dispersive detectors.

Inkjet Printing for Trace Metal Contamination Standards

The feasibility of using piezoelectric drop-on-demand inkjet printing technology to produce trace metal contamination standards on silicon wafers has been demonstrated. Prototype standards of Fe and Cu contamination with surface concentrations between 10^{13} atoms/cm^2 and 10^{15} atoms/cm^2 have been produced. Figure 6 shows SIMS secondary ion images of prototype standards for iron produced by printing different numbers of drops at a single spot. Concentrations range from approximately 10^{13} atoms/cm^2 for one drop

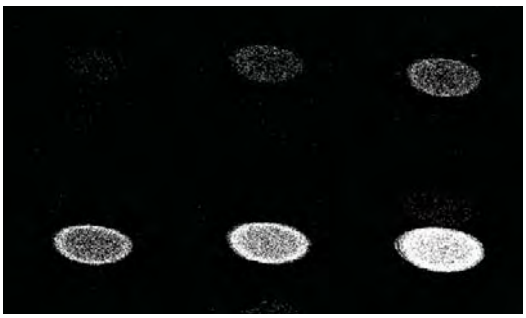

Figure 6. Secondary ion images from 1, 5, 10, 25, 50, and 100 drops of Fe solution in a spot. Scale bar is 250 μm.

per spot to approximately 10^{15} atoms/cm^2 for 100 drops per spot. SIMS measurements show that the secondary ion intensity is linear with respect to concentration over the concentration ranges investigated in this initial study. The success of these preliminary experiments has prompted further work to prepare other elements in addition to Fe and Cu and at concentrations ranging from 10^7 atoms/cm^2 to 10^{15} atoms/cm^2.

LACSBI: A Technique for Removing Unwanted Diffraction Effects from TEM-Based Chemical Images

As front end devices move from the familiar structures of conventional CMOS toward new materials and complex 3-D geometries, there will be an increasing need for flexible metrology solutions at the nanometer length scale. Energy-filtered transmission electron microscopy (EFTEM) provides a method for rapid spectroscopic characterization with nanometer resolution, suitable for both conventional 2-D and tomographic (3-D) chemical imaging. However, the extraction of quantitative chemical images with EFTEM is limited by the susceptibility of all convention transmission electron microscopy (CTEM) to diffraction effects in crystalline specimens: coherent scattering contrast that complicates the interpretation of the [incoherent] chemical contrast.

This effect is illustrated in Fig. 7 with an EFTEM spectral image reconstruction of a FinFET device structure. Here, the distinct colors correspond to amorphous silicon oxide (red), silicon nitride (green) and hafnium oxide (blue) phases, as well as the single-crystal silicon fin (cyan). Only the silicon phase will exhibit diffraction effects. At conventional fixed beam imaging conditions (a), the variation in intensity in the fin from its base (bright) to its tip (dark) is actually the superposition of a <011> diffraction pattern on the chemical image. Effectively, the measured silicon concentration would be high in the bright regions and low in the dark regions, relative to that measured in the amorphous phases. A comparable image with the microscope operated in large angular convergence scanned beam illumination (LACSBI) mode (b), filters out this diffraction contrast. Since all other phases are amorphous, for which no diffraction effects are expected, this application provides a "null" experiment for identification of potential artifacts with LACSBI. No visible loss in spatial resolution is evident in the comparison of Fig. 7 (a), (b), and (c), and a line trace from the LACSBI image (c) shows a spatial resolution of ~2 nm and normalized phase fractions that sum to 99.4 % ± 1.1 % along the line trace.

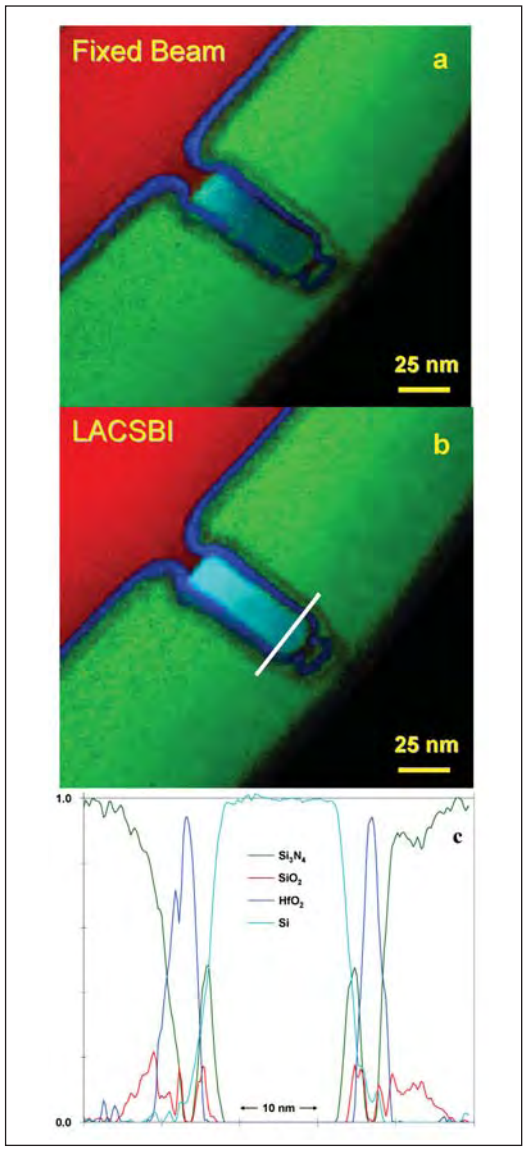

Figure 7. LACSBI with EFTEM imaging of a FinFET. See text for details.

LACSBI mitigates diffraction contrast by averaging the data acquisition over many incident beam orientations, thus providing a largely incoherent image, as required for quantitative analysis. As important as this signal incoherence is for quantitative 2-D imaging and compositional profiles, it is essential for tomographic reconstruction of 3-D chemical images, since the incoherent signal obeys the "projection" requirement for all existing 3-D reconstruction methods from tilt series of images. Thus LACSBI provides a breakthrough

in nm-scale metrology for the complex 3-D architectures that are expected for nonconventional CMOS and post-CMOS devices.

This study is a collaboration with Brendan Foran of Aerospace Corp.

Characterization of the High-κ Metal Gate Barrier Height Using Internal Photo Emission (IPE)

Metal gates on high-κ dielectrics are being actively searched to replace the traditional *poly*-Si gate / SiO_2 / Si (MOS) structure for the next advanced CMOS device generations. In the selection of an appropriate metal gate and high-κ dielectric, one of the most important properties of the selected materials that needs to be considered is the *barrier heights* (Φ) at their interfaces. **I**nternal **P**hoto**e**mission (***IPE***) is a direct method to measure Φ. In addition, ***IPE*** can give insights into other properties of the films such as internal field effects, interface local charges, fixed charge scattering, trappings.

Recently, in a collaboration with SEMATECH, we employed IPE to determine the barrier heights of two ternary metals of great interest for next generation of advanced CMOS: TaSiN and TaN. These metals were deposited on a single dielectric SiO_2 or HfO_2 layer or a stack of SiO_2/HfO_2 with various SiO_2 thicknesses. For the single dielectric layer, it was found that Φ_0 = 3.36 eV and 3.54 eV for TaSiN/SiO_2 and TaN/SiO_2 interfaces, respectively, and Φ_0 = 2.24 eV and 2.47eV for TaSiN/HfO_2 and TaN/HfO_2 interfaces, respectively. It is observed that the difference in the barrier heights of both metals is about 0.2 eV on either of the dielectrics. This indicates that no Fermi pinning is evident at the HfO_2 interfaces. These results are in a very good agreement with the work function determined from electrical CV measurements.

For the more complex structure, TaSiN or TaN on SiO_2/HfO_2 stacks, however, Fermi level pinning is observed when SiO_2 is inserted between HfO_2 and Si substrate. Figure 8 shows a typical photoemission yield for TaN / (HfO_2-SiO_2 stack) structure biased at +3.0 and -3.0 Volt . Clearly, at these biases, the effective barrier heights at TaN / (HfO_2-SiO_2 stack) interface and (HfO_2-SiO_2 stac) / Si interface are 2.49 eV and 3.18 eV, respectively. In addition to the barrier height, IPE yield also provide other optical features such as critical interband transitions, *i.e.*, E_1 and E_2 of Si. The barrier height at zero internal field (Φ_0) is thus

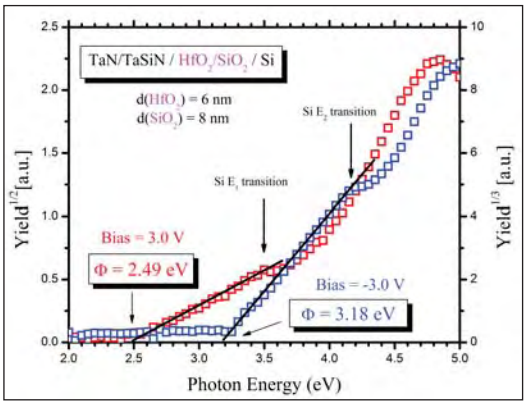

Figure 8. Barrier heights at TaSiN/HfO_2-SiO_2 (red curve) and HfO_2-SiO_2/Si (blue curve) interfaces determined by intertal photoemission at a typical bias of 3.0 V and -3.0 V, respectively.

determined by using Schottky plot of the linear relationship of the barrier height and square-root of internal field ($F^{1/2}$). Figure 9 shows the Shottky plots for various SiO_2 thicknesses. As a result, Φ_0 at the metal gate and HfO_2-SiO_2 stack was found to pin at 2.5 eV for both metals. At the interface of HfO_2-SiO_2 stack and silicon substrate, Φ_0 = 4.5 eV. Furthermore, between both metal gates and the dielectric stack, the barrier heights appear to be insensitive to the applied field strength (see Fig. 9). It's speculated that it could possibly caused by the

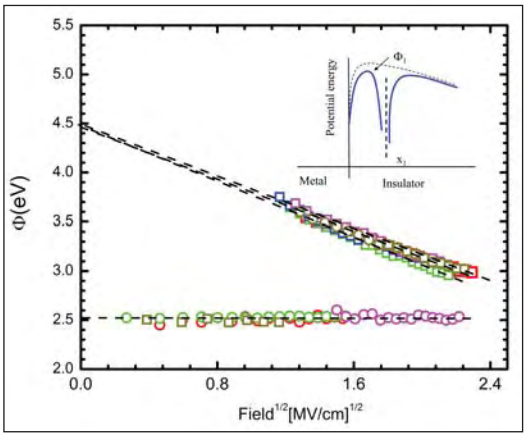

Figure 9. Schottky plots of TaSiN/ HfO_2-SiO_2/Si and TaN/ HfO_2-SiO_2/Si stacks for various SiO_2 thicknesses. Φ_0's at both the TaSiN and TaN gates and HfO_2-SiO_2 interfaces are found to pin at 2.5 eV for both metals, bottom curve. At the interface of HfO_2-SiO_2 stack and silicon substrate, Φ_0 = 4.5 eV, top curve. Between both metal gates and the dielectric stack, the barrier heights appear to be insensitive to the applied field strength. It is possible that a fixed plane charges existing near the interface give rise to a Φ_1 potential which is independent of the external applied field (inset) or it is due to the higher permittivity of the HfO_2 layer.

fixed plane charges near the interface. It's been theoretically simulated that the barrier height could be controlled by the Φ_1 potential of charged plane located at a distance x_1 from the interface (see Fig. 9 inset).

Film Thickness Dependence of Sub-Bandgap Defect States Observed in Polycrystalline Hafnium Oxide

In collaboration with IBM we compare hafnium-based high-κ dielectric films grown by MOCVD and ALD. MOCVD-grown HfO_2 films are mostly monoclinic, while HfSiO films are amorphous. Thin ALD-grown HfO_2 films are amorphous, while thick films are monoclinic, with traces of orthorhombic or tetragonal phases present. We note that sub-bandgap states may be the underlying cause for gate leakage via Frenkel-Poole hopping. The addition of Si to HfO_2 reduces the tendency for crystallization, mitigating such issues. However, such sub-bandgap states likely will not be a limiting factor in high-κ based CMOS technologies, since they line up close to the band edge and are therefore not accessible at the low gate voltages employed.

Collaborations

International SEMATECH, ATDF – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers

Ionoptika – Development of a C_{60}^+ primary ion source for advanced semiconductor technology

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces

Peabody Scientific – Ion source development for Semiconductor SIMS

Micron Semiconductor – trace organic detection

Aerospace Corporation – TEM-based chemical imaging

SEMATECH, Characterization of metal gate/high-κ systems.

University of Maryland, College Park, Ultra-thin gate oxide reliability.

MSEL, Characterization of metal gate/high-κ systems.

IBM, Electrical characterization of high-κ systems.

Intel, Electrical characterization of high-κ systems.

Texas Instruments, Electrical characterization of high-κ systems.

Rutgers University, Characterization of metal gate/high-κ systems.

Micron, Characterization of metal gate/high-κ systems.

Yale University, Electrical characterization of high-κ systems.

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Plasma Process Metrology

Goals

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS, 2006 update) identifies a need for better, more predictive modeling of the impact of equipment on process results (Modeling and Simulation section, pages 6-7, Table 123a). To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, the dependence of these properties on processing equipment, and the effect of these properties on process results, further progress in model development and validation is required. The ITRS also identifies a need for development of robust sensors and process controllers (Metrology section, page 2, Table 116) which are able to convert large quantities of raw data into information useful for improving manufacturability and yield.

Technical Strategy

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors. Our reactors include capacitively coupled cells as well as inductively coupled, high-density plasma reactors, one of which is shown in Fig. 1.

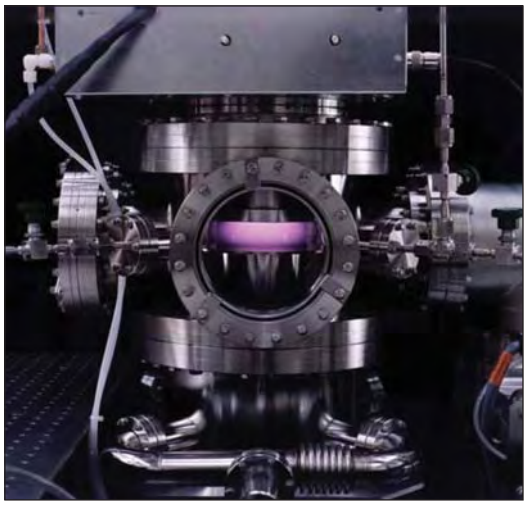

Figure 1. One of the inductive, high-density plasma reactors used in our experimental studies.

Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

1. Our recent efforts have focused on an electrical measurement technique developed at NIST for use in process monitoring and control

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E. Benck

"NIST is one of the leaders in plasma processing related research in the U.S. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools."

Peter Ventzek
TEL, Inc.

"The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries."

Bing Ji,
Air Products and Chemicals, Inc.

applications. This technique relies on noninvasive, nonperturbing measurements of the radio-frequency (rf) current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the flux and energy of the ions that bombard wafers during processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of the plasma and its sheaths. To validate the technique, experiments in an rf-biased, inductively coupled plasma reactor have been performed both with and without silicon wafers loaded in the reactor. Plasma potentials, sheath voltages, total ion flux, and ion energy distributions obtained from the rf measurements have been compared against independent measurements and shown to be in good agreement. The technique has been used to monitor long-term drift in ion energy and total ion flux. We have also monitored the more rapid changes that occur when the pressure, power, and gas flow are perturbed in ways that mimic equipment faults. Small changes in ion energy and total ion flux that occur over the course of a normal oxide etch have also been monitored. Future efforts are directed toward demonstration of the usefulness of the technique in industrial plasma reactors, which may differ from our research reactors in several ways. First, industrial reactors are often equipped with electrostatic chucks, which contain an insulating layer that may have an electrical impedance large enough to significantly affect discharge electrical characteristics. Second, to accommodate 300 mm wafers, industrial reactors require large electrodes, which draw rf currents that are significantly larger than can be handled by our present rf current probes. Third, in many plasma etching applications, industrial inductively coupled plasma sources are not operated in the high-density, purely inductively coupled mode, but are instead operated in a lower-density mode that couples power into the plasma both inductively and capacitively. These issues will be investigated first by experiments performed at NIST, in which we will modify our research reactors to more closely resemble industrial reactors. Additional tests, undertaken in collaboration with industrial partners, will then be performed in actual commercial reactors.

DELIVERABLES:

- Evaluate the validity and utility of rf measurement techniques, electrical models, and analysis techniques in a laboratory reactor equipped with an insulating chuck. 3Q 2007
- Evaluate the accuracy of commercial high-current probes and their use in extending rf-based ion flux and ion energy monitoring to industrial-scale reactors. 1Q 2008
- Perform validation tests of noninvasive, rf-based ion flux and ion energy monitoring in an inductively coupled reactor operated in the low-density, mixed capacitive-inductive mode. 2Q 2008
- Perform validation tests of noninvasive, rf-based ion flux and ion energy monitoring in industrial, inductively coupled plasma reactors. 4Q 2008

2. Dual-frequency, capacitively-coupled plasma reactors are becoming increasingly important in semiconductor manufacturing processes, however, there appear to exist only limited amounts of published data on these systems. Most experimental papers concentrate solely on the etching characteristics, and numerous theory papers on dual-frequency capacitive systems show few comparisons with actual experimental data. Several important fundamental questions about the operation of these systems are not completely understood. How does applying the two rf frequencies to a single electrode compare with applying the frequencies to separate electrodes? How does varying the two frequencies modify the plasma? How independent is the ion energy control and plasma production? These questions will be investigated using a combination of optical measurements (such as time-resolved optical emission spectroscopy), invasive probes (Langmuir probes, wave cutoff probes, and mass spectrometers equipped with ion energy analysis) and noninvasive electrical measurements. Efforts will be directed at obtaining a well-validated, complete model for the physical and electrical behavior of dual frequency discharges. In addition to providing useful insight and fundamental understanding of the operation of such systems, it would also allow more accurate computer simulations of prototype dual-frequency equipment and would enable the noninvasive rf-based process monitoring technique to be used in dual-frequency capacitively coupled plasma reactors.

DELIVERABLES:

- Develop model for ion flux and electrical characteristics of dual-frequency capacitively coupled plasmas and validate by optical and electrical measurements. 2Q 2009
- Develop model for ion energy distributions in dual-frequency capacitively coupled plasmas and validate by mass spectrometer measurements. 4Q 2009.

Accomplishments

■ The NIST-developed, noninvasive, model-based electrical technique for monitoring ion energy and total ion flux has recently been validated in actual etching conditions in CF_4/Ar plasmas (Fig. 2). Unlike previous validations, performed with no wafer present, the recent validations were performed with silicon wafers — oxidized and bare — loaded into the reactor. The wafer, as well as the contact between the wafer and the electrode on which it rests, both contribute an electrical impedance which, if unaccounted for in the model, can cause errors in the ion energy distributions and total ion flux obtained from the noninvasive technique. At low rf bias frequencies < 100 kHz, the contributed impedance was large, resulting in substantial errors in the noninvasive results. Nevertheless, at bias frequencies of 1 MHz or higher, which are more typical of semiconductor manufacturing, the wafer and wafer contact contribute only a few ohms of impedance, resulting in an uncertainty in noninvasive ion energies of only a few electron volts. The speed of the analysis algorithms has also recently been greatly increased, making it possible to monitor changes in ion energy and total ion flux with a time resolution on the order of 1 second. In recent demonstrations, the speeded-up technique has been used to monitor small changes in ion energy and total ion flux that occur over the course of a "normal" oxide etch, as well as larger changes that occur when the pressure, power, and gas flow were perturbed in ways that simulate equipment faults.

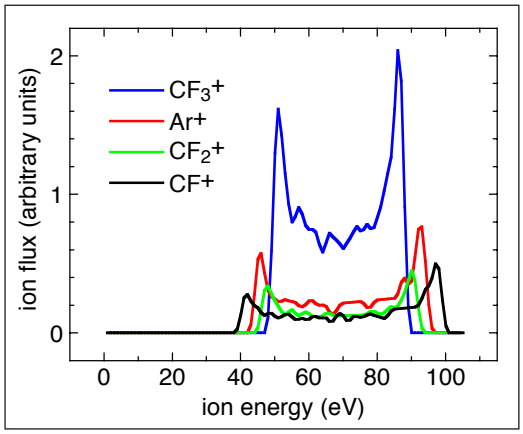

Figure 2. Ion energy distributions from noninvasive electrical measurements, determined in real-time during an oxide etch in an Ar/CF_4 plasma.

■ In a collaboration with KRISS, the Korea Research Institute of Standards and Science, a new method for measuring electron number density in plasmas, the wave cut-off method, has recently been implemented in NIST laboratories. Unlike Langmuir probe measurements, which are commonly used for measuring electron density, cut-off measurements do not suffer from problems with rf compensation or deposition of insulator layers. Comparisons performed in one of our inductively coupled plasma reactors showed good agreement between electron densities measured by the cut-off probe and by a Langmuir probe. The accuracy of the cut-off probe was shown to be greater than the Langmuir probe. The cut-off probe has been used to characterize the spatial variation of the electron density in the inductively coupled reactor and the effect of rf substrate bias on the electron density. Interest in the bias effect has been stimulated by recently proposed, new methods for rf biasing, such as double-frequency bias and nonsinusoidal bias, which may contain Fourier components at frequencies higher than those previously used for biasing. Our measurements showed that even at bias frequencies as high as 30 MHz, the effect of bias on electron density is small, and therefore that nearly independent control of ion energy and ion flux can be maintained even at such high frequencies. Simple analytic models that describe the effect of bias on electron density, which would be useful for estimating such effects under other experimental conditions in other plasma reactors, have been derived and validated by the cut-off measurements. A manuscript describing these results has been written and will appear in print soon.

Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the Web-based NIST "Electron Interactions with Plasma Processing Gases" database. This Web site has experienced tens of thousands of hits throughout its history.

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Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. A major new technology thrust over the past several years is the move to three dimensional integration. Environmental pressures have led to the reduction and elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the stacking of chips with via hole interconnect, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Atomic Layer Deposition – Process Models and Metrology

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W. S. Hurst

Goals

Develop validated, predictive process models and *in situ* metrologies for atomic layer deposition processes.

Customer Needs

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high-κ gate dielectric layers, diffusion barrier layers, and DRAM dielectric layers. However, significant developmental issues remain for many of these applications.

One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the *International Technology Roadmap for Semiconductors (ITRS) 2005 Edition* as *"one of the few enabling methodologies that can reduce development cycle times and costs." [ITRS 2005 Edition, Modeling and Simulation, page 1]* A TCAD topical area identified in the ITRS 2005 Edition is *"Equipment/feature scale modeling—hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings." [ITRS 2005 Edition, Modeling and Simulation, page 1]* A difficult challenge related to this topical area is *"Integrated modeling of equipment, materials, feature scale processes and influence on devices" [ITRS 2006 Update, Modeling and Simulation, Table 122, page 2]* with associated issues including *"Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms, and simplified but physical models for complex chemistry"* and ALD deposition modeling. *[ITRS 2006 Update, Modeling and Simulation, Table 122, page 2]* In addition, the 2005 ITRS notes that *"a key difficult challenge across all modeling areas is that of experimental validation." [ITRS 2005 Edition, Modeling and Simulation, page 1]* Further, with respect to experimental validation, *"One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films." [ITRS 2005 Edition, Modeling and Simulation, page 17]* This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and *in situ* metrologies for ALD processes.

Technical Strategy

This project involves two general directions of investigation: development of *in situ* metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supporting. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that important reaction species will be identified as the understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, this will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetic properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

Various *in situ* diagnostics are being evaluated for use in characterizing gas phase and/or surface processes. Gas phase diagnostic development has focused on metrologies that are sensitive to gas phase chemistry, particularly gas phase chemistry that can be related to film properties. Diagnostics that are sensitive to gas phase chemistry can be used to help optimize gas injection conditions rather than simply monitor precursor delivery. In addition, the results from such diagnostics will be more useful for process model development. ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the gas flow and temperature fields in an ALD reactor. Experimental validation of the overall process model is accomplished by modeling the performance of a

custom-built, research-grade ALD reactor with optimized optical accessibility and benchmarking the numerical results with experimental data. HfO_2 ALD using tetrakis(ethylmethylamino) hafnium (TEMAH) and water has been selected as the chemical system for primary investigation.

1. A number of diagnostics are being evaluated for sensitivity to ALD chemistry and integration into deposition systems. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their proven potential for *in situ* monitoring. While sensors that are sensitive to gas phase species (*e.g.*, mass spectrometry and Fourier-Transform infrared (FTIR) spectroscopy) are easier to integrate into commercial reactors (*e.g.*, in the gas exhaust line), these techniques are only sensitive to volatile species. Hence, it is sometimes difficult to relate the species detected with such techniques to mechanisms of interest on the growth surface. Hence, both gas-phase-sensitive and surface-sensitive techniques are being evaluated to probe ALD chemistry. The suitability of Raman spectroscopy and FTIR spectroscopy for probing ALD surface processes under actual deposition conditions is being investigated. In addition, the suitability of mass spectrometry and FTIR spectroscopy for probing gas phase ALD processes and how best to relate gas phase species to important surface processes is being investigated. A research-grade ALD reactor with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques has been designed and constructed.

DELIVERABLES:

- Complete evaluation of time-resolved, *in situ* FTIR measurements for probing HfO_2 ALD gas phase processes. 3Q 2007
- Complete evaluation of mass spectrometry measurements for probing HfO_2 ALD gas phase processes. 4Q 2007
- Optimize quantum cascade laser system for probing HfO_2 ALD gas phase processes. 4Q 2006

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD and chemical vapor deposition (CVD) is an important aspect of this project and is an ongoing process. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity compiles and evaluates currently available thermochemical and chemical kinetic data for organometallic compounds and related precursors. The second activity supplements available data by using *ab initio* and semi-empirical quantum calculations coupled with transition state calculations to develop detailed chemical kinetic models from computed molecular structures, thermodynamic properties and spectroscopic properties of relevant compounds. The third activity utilizes the experimental and computed thermochemical and chemical kinetic data to develop detailed chemical kinetic models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES:

- Perform high level *ab initio* and Density functional theory (DFT) quantum calculations for ALD and CVD organometallic and metal halide precursors and derivatives containing Al, Hf, Zr, Ga, and Ti atoms. Benchmark heats of formations using correlations with available experimental data in the literature. 2Q 2007
- Develop an ALD mechanism for HfO_2 deposition from TEMAH and water and incorporate the mechanism into a two-dimensional CFD reactor model. 4Q 2007

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of *ex situ* film characterization measurements to reactor conditions as determined by *in situ* measurements and numerical modeling of the temperature and flow fields in the reactor. *In situ* measurement techniques include those techniques being developed for model validation. *Ex situ* measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy (XPS), X-ray diffractometry, atomic force microscopy, ultraviolet Raman spectroscopy, and various electrical measurements. The data provided by these measurements, spatially resolved when possible, include such film characteristics as thickness, stoichiometry, HfO_2 phases present, degree and type of impurity incorporation, leakage current, and dielectric constant.

DELIVERABLES: Investigate the relationship between HfO_2 ALD process parameters, reactor gas flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics. Ongoing

ACCOMPLISHMENTS

■ ALD Reactor Design — An ALD reactor with diagnostic access near the wafer surface that is also capable of growing high-quality, reproducible HfO_2 films was designed and fabricated. Gas flow and temperature profiles in this reactor were simulated using three dimensional CFD modeling, as shown in Fig. 1. Diagnostic access does not significantly perturb gas flow, especially near the wafer surface. Hence, reproducible, high-quality film deposition and *in situ* diagnostics can be performed simultaneously. This reactor is being used to provide data to validate process models and develop metrologies.

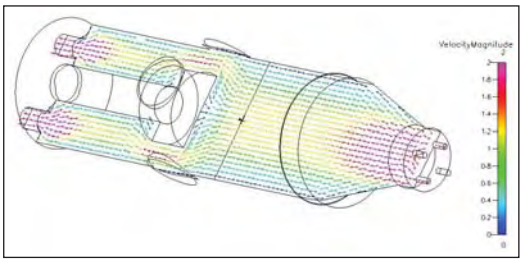


Figure 1. A cross section of the helium carrier gas velocity distribution in the diagnostic-accessible reactor under typical deposition conditions (obtained from a full three dimensional simulation).

■ HfO_2 Film Deposition — ALD HfO_2 films are being deposited under a variety of process conditions using tetrakis(ethylmethylamino) hafnium (TEMAH) and water or tetrakis(dimethylamino) hafnium (TDMAH) and water. Films have been characterized with a number of techniques, including VUV-SE, as shown in Fig. 2, XPS, FTIR, Raman spectroscopy, X-ray diffractometry, atomic force microscopy, and current-voltage measurements.

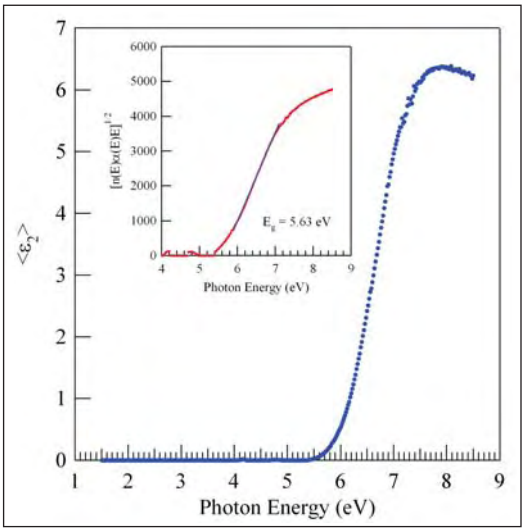


Figure 2. Imaginary part of the complex dielectric function as a function of photon energy for HfO_2 ALD film as determined using VUV-SE. The inset illustrates determination of band gap energy by extrapolation of the expression $[n(E)\bullet\alpha(E)\bullet E]^{1/2}$ to zero (data courtesy of N.V. Nguyen).

■ ALD Reactor Modeling — Three dimensional CFD models for gas flow and temperature fields have been developed for this reactor. In addition, time-resolved precursor distributions have been modeled, as shown in Fig. 3. The results from these models have been used to help optimize reactor designs, especially optical window design, and deposition conditions. Chemical reaction mechanism models for HfO_2 ALD are being developed for use with these three dimensional flow and temperature models to simulate the entire ALD process.

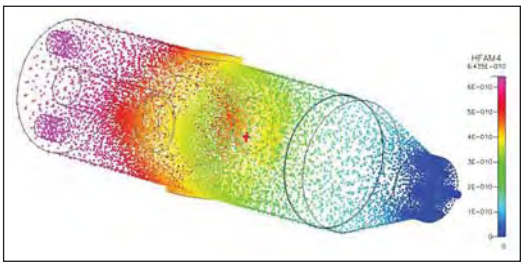


Figure 3. A three dimensional mass fraction profile showing TEMAH mass fraction distribution after 5 sec of helium purge following a 3 sec TEMAH injection into the reactor.

■ *In situ* Measurements — *In situ* gas phase FTIR measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to deposition reactants, TEMAH, and products, N-methylethylamine, as illustrated in Fig. 4. In addition, *in situ* FTIR measurements during TEMAH injection pulses were shown to be sensitive to TEMAH decomposition in the delivery system. A quadrupole mass spectrometric sampling system has been designed and constructed for gas phase sampling near the wafer surface.

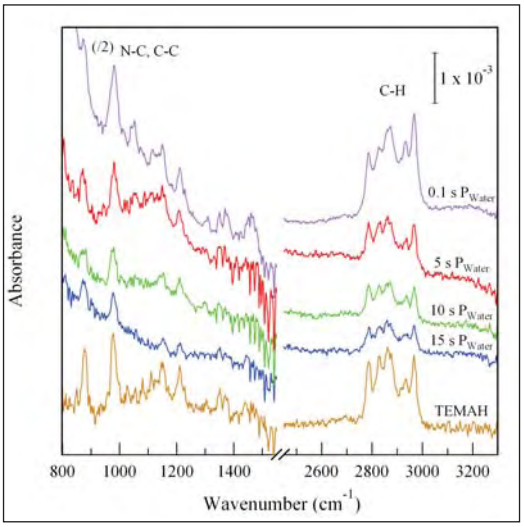


Figure 4. Gas phase FTIR spectra as a function of purge time following a water pulse.

■ Chemical Properties Calculations — Molecular structures and energies for precursors, adsorbates, intermediates, and transition states have been calculated using *ab initio* and density functional theory quantum calculations for ALD of Al_2O_3 from TMA and water and HfO_2 from TEMAH or TDMAH and water. Although the primary focus of this work is on HfO_2 ALD, Al_2O_3 ALD is also being investigated as a model system for two main reasons. First, there has been significant work on Al_2O_3 ALD, and consequently, there are adequate experimental data for use in chemical mechanism validation. Second, aluminum is more amenable to quantum calculations than hafnium, a transition metal. It is expected that lessons learned in developing an ALD model for Al_2O_3 ALD will be useful in development of a HfO_2 ALD model. High level *ab initio* calculations, up to CCSD(T)/aug-cc-pVnZ (n=2-5) have been done for small species to benchmark heats of formation and bond dissociation energies for AlH_nX species (n = 0-2, X = H, F, Cl, OH, NH_2, CH_3). Additional calculations have been also done to provide higher level corrections for core-valence, relativistic, and basis set deficiencies. DFT calculations have been utilized to compute heats of formation for ALD precursors, related molecules, and references molecules. The DFT calculations used the B3LYP method with LANL2DZ+ECP basis sets for the metals and 6-311G(d,p) basis sets for other atoms. Calculations were done on about 130 different organometallic and metal halide species containing aluminum (Al), hafnium, zirconium, gallium, and titanium with alkyl, alkoxy, and amino ligands - $M(R)_n$, $M(OR)_n$, $M(NR_2)_n$ as well as about 50 reference hydrocarbons, oxidized hydrocarbons, and nitrogen-substituted hydrocarbon species. Empirical corrections to the DFT energies will be determined by benchmarking and comparison to reference compounds with available values in the literature. A detailed chemical kinetic model for ALD of HfO_2 from TDMAH and water has been constructed based on these rate expressions. This model is being refined based on further reactor model simulations, comparison with experimental observables, and supplemented with additional quantum calculations, where necessary.

■ Reference Spectra Development — Adequate reference spectra could not be located for TEMAH or N-methyl-ethanamine (MEA), a gas phase product of the TEMAH and water ALD reaction. Hence, infrared and Raman vibrational frequencies were calculated with DFT using B3LYP theory with LANL2DZ basis sets. The calculated frequencies were compared to measured infrared spectra obtained in the ALD reactor and tentatively identified as TEMAH and MEA, as shown in Fig. 5. In the infrared spectra, vibrational modes in the CH wavenumber range were scaled by 0.95 and the modes in the lower wavenumber range were scaled by 0.961.

■ Database Website — A Website http://kinetics.nist.gov/CKMech has been made available. This site contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes, including information pertaining to ALD and CVD of aluminum, Al_2O_3, and other related ALD systems (*e.g.*, Zr, Hf, etc.), as well as a significant amount of information pertaining to hydrocarbon-based reactions.

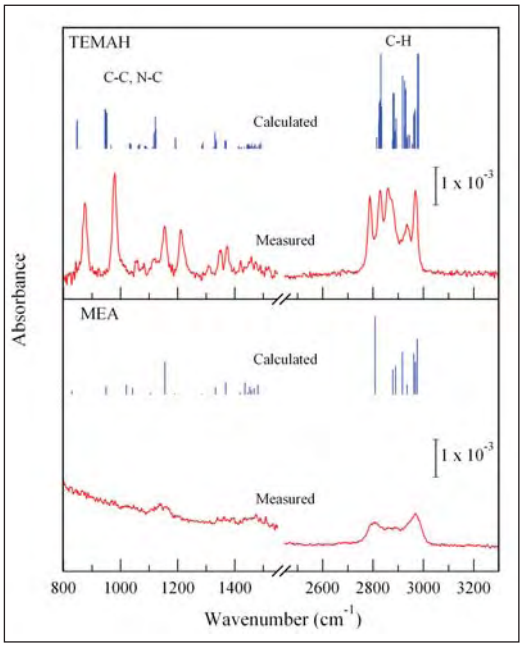


Figure 5. Comparison between calculated and measured spectra of TEMAH and MEA.

Recent Publications

J. E. Maslar, W. S. Hurst, D. R. Burgess, Jr., W. A. Kimes, N.V. Nguyen, and E.F. Moore, "*In Situ* Monitoring of Hafnium Oxide Atomic Layer Deposition," *2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics*, 2007, submitted.

J. E. Maslar, W. S. Hurst, D. R. Burgess, Jr., W. A. Kimes, and N. V. Nguyen, "*In Situ* Characterization Of Gas-Phase Species Present During Hafnium Oxide Atomic Layer Deposition," *ECS Transactions* **2**, 133-143 (2006).

Advanced Nanoscale and Mesoscale Interconnects

Technical Contacts:
T. P. Moffat
D. Josell

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations for both on-chip and chip stack applications, examining the generality of the superconformal filling mechanism and exploring processes utilizing novel barriers and/or seed geometries. This is complemented by surface chemistry studies aimed at understanding and optimizing the feature filling process.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever-smaller dimensions has led to the rise of new challenges, including fabrication of ever-thinner copper seeds, which are required for the copper superfill process, and increased resistivities of the metallizations due to size effects. At the same time the movement towards 3-D integration of integrated circuits is under way. This involves the replacement of long horizontal conductors by short vertical interconnections; in addition to an improved RC response, the new architecture enables integrations of heterogeneous devices. Many challenges to the fabrication through-silicon-vias (TSV) remain that require an understanding of the surface chemistry of copper. To help overcome these hurdles the National Institute of Standards and Technology (NIST) is enhancing existing copper technology through improved understanding of the surface chemistry and metrologies for the superfill process, examining new interconnect materials, and pursuing new fabrication techniques such as seedless processing and atomic layer deposition.

Interconnect metallization issues are discussed in the Interconnect section of the 2006 update of the International Technology Roadmap for Semiconductors.

Technical Strategy

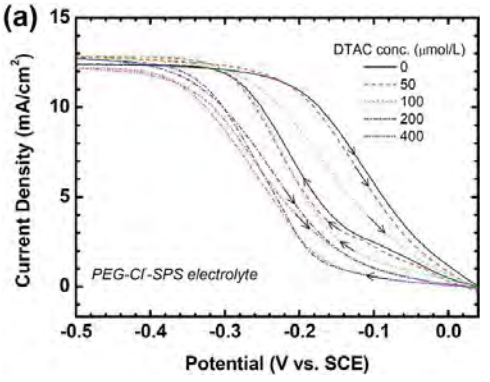
To meet future industrial needs, we have, over the life of this project, developed metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. The derived Curvature Enhanced Accelerator Coverage (CEAC) mechanism has served as a platform for this understanding. An important consequence of bottom-up superfilling is the phenomena of "momentum plating" that can lead to bump formation above filled features. These bumps greatly hamper subsequent planarization processes. However, the overshoot phenomena may be controlled by the addition of certain cationic surfactants to the copper plating baths as shown in Fig. 1 (next page). In the past year, we undertook a variety of electroanalytical and feature filling experiments that help establish suitable strategies to help quantify, understand, and control bump formation. Through this activity the CEAC model was successfully extended to explain and predict the filling behavior during deposition from complex plating baths containing any combination of suppressors, accelerators and levelers.

DELIVERABLES: Publications detailing the experimental demonstration of the use of cationic surfactants to control undesired momentum plating during the superfilling process. Publications detailing the extension of the NIST CEAC superfilling model to quantitatively describe both superconformal feature filling and bump control. 1Q 2007

In parallel with this effort a variety of surface analytical studies, *e.g*. ellipsometry, XPS, and *in situ* STM, are under way to directly probe the competitive adsorption dynamics between multiple additives and the copper surface in order to provide molecular level insight into additive function and design. Particular attention is given to the role of potential-dependent adsorption processes that are central to the performance of the copper pulse plating method used to form TSV.

DELIVERABLES: Publications using surface analytical probes to independently quantify adsorbate coverage's relevant to superconformal feature filling. 1Q 2007, 3Q 2007, and 4Q 2007

The generality of the bottom-up superfilling process to the application of other material systems in ULSI and MEMS remains a subject of great



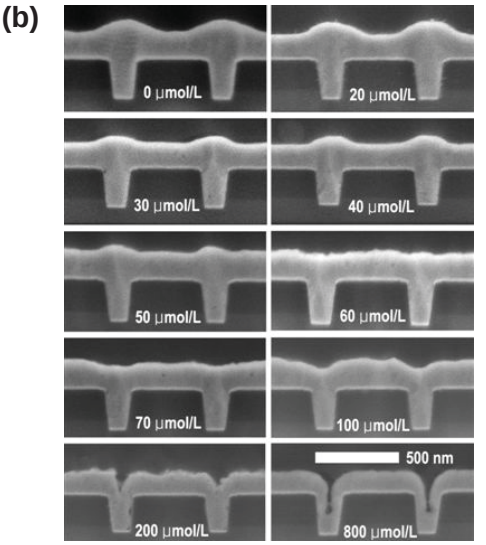


Figure 1a. The effect of the cationic surfactant, DTAC, on the Cu deposition rate in the presence of PEG-Cl-SPS superfilling additives. Note quenching of the hysteretic voltammetric response and increased inhibition with increasing DTAC concentration. Figure 1b. Cross sectional FE-SEM images of Cu deposition on an array of trenches as a function of DTAC concentration. Attenuation of overfill bumping is evident as the DTAC concentration increases to 60 μmol/L, beyond this value DTAC interferes with superfilling.

interest. In addition to silver (the only metal with a higher conductivity than copper) and gold (a metallization for wide-bandgap semiconductors) the prospect for deposition of iron group metals (for magneto-electronic circuitry) has been examined and the preliminary results, as shown in Fig. 2, are encouraging.

DELIVERABLES: Publications detailing the first example of deposition of conducting magnetic materials for Damascene metallization. 3Q 2007 and 4Q 2007

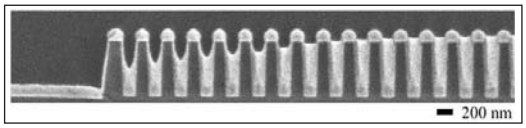


Figure 2. Superconformal Ni deposition from a $NiSO_4$ + $NiCl_2$ +H_3BO_3 electrolyte containing polyethyleneimine. Note the preferential filling of the smallest features and the most densely patterned region.

We've also built upon last year's demonstration of gold superfilling by exploring the impact of catalyst surface diffusion on the feature filling process as detailed in Fig. 3. Likewise, we continue to explore the utility of the CEAC as model as a design tool for alternative processing schemes such as chemical vapor deposition.

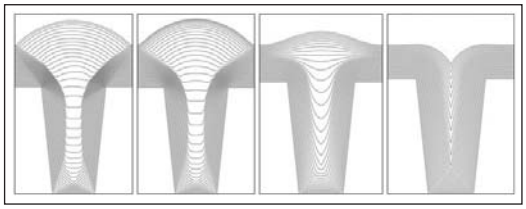


Figure 3. Predicted effect of surface diffusion on Au superfilling of a trench. The dimensionless diffusion coefficient was systematically increased over three orders of magnitude in going from left to right. The smaller values lead to rounding of the corners, while intermediate values cause cusplike filling similar to that often reported for leveling. Filling is nearly conformal for the highest values of catalyst surface diffusion whence the CEAC geometry driven enrichment process is nullified.

DELIVERABLES: Publication exploring the importance of catalyst surface diffusion on shape evolution during superfilling. Including a comparison of observations and CEAC predictions. 1Q 2007

In addition to the electrodeposited copper conductor itself, current metallization technology employs a barrier metal and a PVD copper seed. As feature sizes continue to shrink, the resistive barrier materials negatively impacts electrical performance and deposition of, and on, the PVD seed becomes problematic. These difficulties are driving a search for alternative barrier/wetting layer materials and processes. Ruthenium is one focus because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers, it is immiscible with copper, and copper can be electroplated directly on it, eliminating the need for the PVD copper seed layer and the corrosion problems that come with it. In the past we have demonstrated direct copper superfilling on Ru, Os, and Ir barrier/adhesion

seed layers as well as appropriate metrological aspects required for process control. This work continues with the evaluation of state-of-the-art ALD barrier materials.

DELIVERABLES: Publications detailing seedless superfilling of copper on PVD and ALD layers.
4Q 2007

Accomplishments

- The existing CEAC model of superfilling was extended to include the effect of leveling additives along with the metrology required for assessing the kinetics of the competitive adsorption process. The impact of leveling additives on overfill bump formation during trench filling was demonstrated using prototypical cationic surfactants.

- Bottom-up superfilling of trenches with gold, that might find use in the formation of contacts and metallizations for compound semiconductors, was demonstrated. The importance of catalyst surface diffusion in superfilling processes was revealed and shown to be particularly relevant to the gold system.

- A range of electroanalytical and surface analytical studies are well under way to quantify the competitive and co-adsorption processes associated with copper superfilling additives. In particular, ellipsometry was used to reveal a.) difference in adsorption behavior between rate accelerating thiols versus disulfides, b.) irreversible adsorption of thiols and disulfides versus reversible adsorption of halide and PEG, c.) inhibition of PEG adsorption by a pre-adsorbed sulfonate-terminated thiol or disulfide monolayer film, and d.) displacement of the deposition rate inhibiting PEG layer by adsorption of the sulfonate-terminated thiol or disulfide accelerator.

Collaborations

D. Wheeler, J.E. Bonevich, L.J. Richter, M.L. Walker, P.J. Chen, W.F. Egelhoff: NIST.

Christian Witt: AMD

R. Gordon, Harvard University

T. Aaltonen, M. Leskelä and M. Ritala: University of Helsinki.

Recent Publications

T. P. Moffat, D. Wheeler and D. Josell, *"Superconformal Film Growth,"* pg 96-114 in "Electrocrystallization in Nanotechnology, Ed. G. Staikov, Wiley-VCH (2007).

M. Walker, L. J. Richter, and T. P. Moffat, *"Potential Dependence of Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study,"* Journal of the Electrochemical Society 154(5), D277-D282 (2007).

D. Josell, T. P. Moffat and D. Wheeler, *"Superfilling When Adsorbed Accelerators Are Mobile,"* Journal of the Electrochemical Society, 154(4), D208-D214 (2007).

T. P. Moffat, D. Wheeler, S. K. Kim and D. Josell, *"Curvature Enhanced Adsorbate Coverage Mechanism for bottom-up superfilling and bump control in damascene processing,"* Electrochimica Acta, in press, (2007).

S.-K. Kim, D. Josell and T. P. Moffat, *"Cationic Surfactants for the Control of Overfill Bumps in Cu Superfilling,"* J. Electrochemical Society, 153 (12), C826-C833 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, *"Electrodeposition of Cu in the PEI-PEG-CL-SPS Additive System: Reduction of Overfill Bump Formation During Superfilling,"* J. Electrochemical Society, 153 (9), C616-C622 (2006).

M. Walker, L. J. Richter, and T. P. Moffat, *"Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study,"* Journal of the Electrochemical Society 153(8), C557-C561 (2006).

T. P. Moffat, D. Wheeler, S.-K. Km and D. Josell, *"Curvature Enhanced Adsorbate Coverage Model for Electrodeposition,"* Journal of The Electrochemical Society, 153(2) C127-C132 (2006).

D. Josell, D. Wheeler and T. P. Moffat, *"Gold Superfill in Submicrometer Trenches: Experiment and Prediction,"* Journal of the Electrochemical Society, 153(1) C11-C18 (2006).

Nanoporous Thin-Film Metrology for Low-κ Dielectric Materials

Technical Contact:
C. Soles

Goals

This project addresses critical development and integration issues with the interlayer dielectric (ILD) insulator materials needed for semiconductor interconnect applications by developing measurement methodologies to quantify their porous structures and related properties. This is accomplished by working closely with industry and academia to develop and apply these methods on state-of-the-art materials that are leading candidates for next generation integrated circuit applications. Our unique measurement infrastructure is based on a synergistic and complimentary packaging of specular X-ray reflectivity (SXR), X-ray porosimetry (XRP), small angle scattering using both neutrons and X-rays (SANS and SAXS), and a suite of ion beam scattering techniques including Rutherford backscattering spectroscopy (RBS), grazing angle backscattering (GBS), and forward recoil elastic spectroscopy (FRES). With this measurement platform we can provide high quality data and measurements of the chemical composition, film thickness, density, coefficient of thermal expansion (CTE), moisture uptake, porosity, pore size distribution, wall density within a porous matrix, and even the shape or geometry with which periodically patterned pores are arranged. These measurements can be applied to quantify not only the as-applied, virgin material to aide in materials development, but also after the various ashing, etching, deposition, or chemical mechanical polishing (CMP) processes that tend to alter or damage the final structure of the porous material. This year there is a greater emphasis on the process induced damage over the materials development to reflect the current industrial focus. Integration issues are currently the greatest concern when trying to implement porous ILD materials into functional CMOS devices.

Customer Needs

The continued scaling or shrinking of the integrated circuit (IC) devices require new, more efficient ILD materials to combat the growing problems of a rapidly increasing power density on the chip, greater signal propagation delays due to the RC time constant, and increased cross-talk between the adjacent interconnects that continue to be squeezed closer together. The solution has been to develop low dielectric constant (low-κ or ultralow-κ) materials that incorporate nanometer scale pores to lower their effective dielectric constant. While this recognized approach is effective in meeting the ultralow-κ dielectric constant target, introducing porosity simultaneously compromises many of the other properties that are equally as important such as mechanical strength, thermal conductivity, thermal expansion, and the crucial barrier properties (*i.e.*, resistance to Cu ion migration or moisture uptake) of these highly porous material. Likewise the integration process exposes these materials to harsh conditions, including mechanical stresses under a caustic environment in CMP polishing, ashing and etching induced degradation of the material, and thermally generated stresses resulting from the CTE mismatch of dissimilar materials and the large and rapid temperature changes in the back end of the line processes. All of these processes tend to damage or degrade the porous structures. Developing a material that is optimized to meet all of these conditions has been an enormous challenge. There is still currently no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates have included silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. Irrespective of the candidate materials, there is a strong need for high quality structural data to understand correlations between applied processing conditions and the final physical properties. Only through detailed characterization techniques will materials engineers have the proper feedback to know how a process affects the porous material and to then rationally design new materials that are suitable to withstand the harsh integration processes associated with CMOS fabrication.

Technical Strategy

While the field of porosimetry is broad and generally well-established, the small sample sizes (typically films less than 1 μm thick) and the desire to characterize materials in situ, directly on actual silicon wafers, greatly narrows the number of suitable measurement methods. Therefore a suite of measurement techniques, depicted in Fig. 1 (next page), that are especially sensitive to samples in the thin film geometry have been developed at

NIST. When combined, these techniques can fully characterize the properties that are critical for ILD applications. The measurement techniques include various combinations of our reflectivity techniques (SXR and XRP), small angle scattering (SANS and SAXS), and ion beam scattering methods (RBS, GBS, and FRES) to determine important structural and physical property information in porous films less than 1 μm thick. These measurements are performed directly on films supported on thick silicon substrates, meaning that actual processing effects can be investigated.

The elemental composition of the films are needed to convert the scattering length densities obtained from our X-ray and neutron techniques into a meaningful physical density. For the case of unknown or proprietary ILD materials, we have developed RBS & GBS ion beam techniques to determine the Si, C, and O (or other elements other than H) content of the film while the FRES ion beam technique quantifies the H content. In all of these techniques a beam of high-energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy and angle. We have developed a method to fit the spectra and then compute the absolute ratios of the C, O, Si, and H in the film. From chemical composition, we can convert the scattering length densities into the physical or mass density of the film.

Technique	SXR	SAXS SANS	XRP	ion beam
film thickness	■			
average density	■			■
density profile	■			■
average pore size		■	■	■
pore connectivity		■	■	■
porosity		■	■	■
matrix wall density		■	■	■

Figure 1. A chart indicating which techniques are needed to measure the various critical properties of a porous low-κ material.

SANS and SAXS are transmission scattering techniques well-suited for characterizing critical length scales of the porous networks. Inclusions in the film of a different scattering length density than the matrix lead to small angle scattering when their length scales are on the order of 5 to 500 nm. By modeling the diffracted intensity as a function of the scattering vector, one can determine parameters such as the pores size, the pore size distribution, the inter-pore spacing, and the periodicity with which the pores are distributed. For ordered porous structures this reveals the symmetry or periodic lattice on which the pores are distributed. In the case of SANS, a powerful contrast matching technique can be used by mixing hydrogenated and deuterium substituted organic condensate vapors (such as toluene). At a critical concentration the hydrogenated-deuterated mixture of solvents will have exactly the same scattering length density as the matrix. By controlling the partial pressure of this mixture, the vapor can be selectively condensed inside the pores of a given radius (governed by the critical radius for capillary condensation), thereby rendering the condensed pores "invisible" to the scattering technique. This is an extremely powerful method to specific size dependent information about the population of pores.

High-resolution XR is an established, powerful technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. In addition, changes in the density profile from processing or post-application treatments can be determined. The CTE is determined from measurements of the film thickness at different temperatures. More recently, we have been extending the characterization with XR measurements to the lateral or in-plane dimensions of nanopatterned structures using an effective medium approximation. The density measurements are averaged over lateral length scale larger than the coherence length of the X-ray source. In the limit of periodic patterns, the density profile as a function of height conveys information about the average line to space ratio (or the equivalent patterned volume to unpatterned volume ratio for non-linear structures) as a function of pattern height. When these line-to-space ratios are coupled with a precise measure of pattern pitch or periodicity from a SAXS or SANS measurement, one can characterize the entire pattern cross section as a function of height.

DELIVERABLES: Measure and report on the way in which integration processes impact the porous structure in nanoporous ILD materials. 2Q 2007

■ The number of companies trying to develop ILD candidate materials has significantly

decreased. The industry as a whole is moving closer to integrating nanoporous ILD into next generation devices. The remaining selection of candidate materials can be largely divided by their different deposition processes (*i.e.*, CVD versus spin-on). The major issue now is how these different classes of materials withstand the integration processes. Therefore, we have switched from a large scale materials screening effort to a more focused characterization of how the different integration processes, such as ashing, etching, plasma treatment, and CMP polishing, affect the critical properties of the different classes of porous materials. These integrating processes tend to damage the pore structure and thereby reduce the effect κ (dielectric constant after integration) of the dielectric stack. Measurement techniques are needed to quantify and depth profile the process induce damage to the porous materials.

DELIVERABLES: Extend X-ray porosity characterization techniques from planar films to patterned nanoporous structures. 3Q 2007

■ Our porosity characterization measurements thus far have focused on planar, non-patterned low-κ films. While this has been successful in the early stage evaluation of candidate materials, our techniques are starting to loose traction for the integration issues where patterned low-κ structures are of interest. It is therefore critical to extend our measurements to patterned low-κ materials. Recently, we have shown that the effective medium approximation is valid for the nanoscale periodic patterns of the size scale that are of interest to the semiconductor industry. This means that we can characterize the average density as a function of height through a nanoscale pattern. In periodic linear grating patterns, this average density defines the line-to-space ratio as a function of height. When coupled with an accurate knowledge of the pattern periodicity, we can define the average pattern width as a function of pattern height. Now that we have shown that the average density within the patterned material can be characterized, the next step is to see how the density changes when a probe molecule is condensed inside the pores of the patterned material. This will allow us to determine the porosity and wall density of the patterned material as a function of pattern height, extending the use of XRP from planar to patterned structures.

DELIVERABLES: Characterize the fidelity and porosity of nanoporous material patterned by nanoimprint lithography. 4Q 2007

■ Recently there is a growing interest within the community to directly pattern spin-on organosilicate ILD materials by nanoimprint lithography (NIL). It has been shown that by imprinting the ILD material with a multi-level nanoimprint template to directly fabricate a T-gate type structure, one can greatly reduce the number of lithography, deposition, and etching steps in the back end of the line process. This could *significantly* reduce manufacturing costs. Efforts this year will synergistically couple our expertise in thin film nanoporous X-ray metrology with our simultaneous efforts in NIL metrology development. Specifically, we will adapt our XR shape metrology to quantify the fidelity of the nanoimprint process to evaluate the quality of the patterned ILD materials. We will also adapt our XRP measurements on patterned samples to quantify how the NIL process itself affects the pore structure. These measurement techniques will quantify the feasibility of NIL processes for back end of the line interconnect fabrication schemes. This is a topic that all of the major NIL tool companies are actively engaged in.

Accomplishments

■ We have finally completed our contract work with the SEMATECH (ISMT) Interconnect program. Over the past 7 years, we have evaluated over 180 candidate films for ISMT, provided to them by their member companies. These films have been characterized in terms of their thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density / chemical composition by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and distributed to member companies. Additional measurements were performed on specific samples for further analysis using methods such as additional SANS configurations or X-ray porosimetry. These measurements were critical in helping the industry rationally narrow the wide field of candidate materials for next generation ILD materials.

■ A NIST Recommended Practice Guide, Special Publication 960-13, entitled "Pore Characterization in Low-κ Dielectric Films Using X-ray Reflectivity: X-ray Porosimetry" was released to provide the details and recommendations for the use X-ray porosimetry to characterize nanoporous thin films. This document describes how to build an X-ray Porosimetry Device, how to properly use and align the X-ray optics, how to control the partial pressure of the adsorbate molecules, and how

to interpret the data. Hard copies of this publication (Fig. 2) were mailed to all of our contacts in the low-κ dielectric community and made available for free download through our website: http://polymers.msel.nist.gov/PDF/X-ray_Porosimetry_Recommended_Practice.pdf.

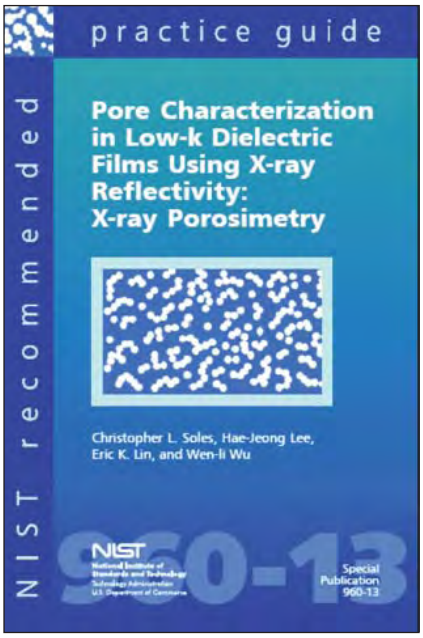


Figure 2. The cover image from our Recommended Practice Guide on characterizing low-κ dielectric films with X-ray porosimetry.

■ The detailed pores structures in a series of highly ordered nanoporous were fully characterized using our measurement techniques. Well controlled, ordered porous structures have the potential to control the degree of interconnectivity through porous network, possibly maximizing the barrier properties of the material. Therefore it is very important to have measurements methods to completely characterize both the size and arrangement of the pores in these ordered systems. Working with our collaborators at the University of Massachusetts, Amherst, a series of organosilicate films with a periodic, self-assembled pore structures were studied in detail. From these measurements we were able to quantify the total porosity, the pore size distribution, the periodicity or spacing of the ordered pores, the degree of interconnectivity between adjacent pores, and the density of the wall material between the pores. Of particular interest we found that the A-B-A triblock copolymer used as the pore generating material lead to a dual distribution of pore sizes. The B block phase segregated into regular spherical pores with a radius of approximately (4 to 5) nm on a cubic lattice of a periodicity of approximately (13 to 15) nm. The second population of pores was much smaller in size and located within the wall material, presumably due to the decomposition of the A blocks which do not phase segregate from the organosilicate marix, between the pores generated by the B blocks. While extremely small, these A block pores accounted for a significant fraction, approximately (30 to 50) % by volume, of the total porosity. This non-trivial fraction of the total porosity has implications on the barrier properties of these materials, suggesting that triblock copolymers may not be the most effective porogen materials for creating isolated, non-interconnected pores.

Collaborations

Polymers Division, NIST – Hae-Jeong Lee, Bryan D. Vogt, Christopher L. Soles, Hyunwook Ro, Da-Wei Liu, Ronald L. Jones, Wen-li Wu, Eric Lin; Center for Neutron Research, NIST – John Barker, Charles J. Glinka, Derek L. Ho

International SEMATECH – Sanjit Daas, Youfan Liu

University of Massachusetts-Amherst – James Watkins

Dow Chemical – Brian Landes, John Lyons, Brandon Kerr, Jason Niu, Tom Kalantar

LG Chemicals – Minjin Ko

IBM T. J. Watson Research Center – Alfred Grill, Qinghuang Lin

Seoul National University – Kookheon Char, Do Yoon

Technion – Michael S. Silverstein, Miche Shach-Caplan

University of Michigan - David Gidley

Axcelis Technologies, Incorporated – Carlo Waldfried

Rohm and Haas Company - Michael Gallagher

Dow Corning – Byung Keun Hwang

Recent Publications

Q. Lin, S. A. Cohen, L. Gignac, B. Herbst, D. Klaus, E. Simonyi, J. Hedrick, J. Warlaumont, H. J. Lee and W. L. Wu, "Low Dielectric Constant Nanocomposite Thin Films Based on Silica Nanoparticle and Organic Thermosets" *J. Polym. Sci B.*, **2007**, *45(12)*, 1482.

H. W. Ro, K. Char, E. C. Jeon, H. J. Kim, D. K., H. J. Lee, J. K. Lee, H. W. Rhee, C. L. Soles, and D. Y. Yoon *Adv. Mater*. **2007**, *19*, 705–710.

H. J. Lee, C. L. Soles, D. W. Liu, B. J. Bauer, E. K. Lin, W. L. Wu, and M. Gallagher, "Structural Characteristics of Methylsilsesquioxane Based Porous Low-κ Thin Films Fabricated with Increasing Crosslinked Particle Porogen Loading" *J. Appl. Phys*., **2006**, *100 (6)*, 064104.

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B. D. Vogt, H. J. Lee, W. L. Wu, and Y. Liu, "Specular X-ray Reflectivity and Small Angle Neutron Scattering for Structure Determination of Ordered Mesoporous Dielectric Films", *J. Phys. Chem. B* **2005**, *109*, 18445.

M. S. Silverstein, M. S. Caplan, B. J. Bauer, R. C. Hedden, H. J. Lee, and B. G. Landes, "Nanopore Formation in a Polyphenylene Low-κ Dielectric" *Macromolecules*, **2005**, *38(10)*, 4301.

B. D. Vogt, R. A. Pai, H. J. Lee, R. C. Hedden, C. L. Soles, W.-l. Wu, E. K. Lin, B. J. Bauer, and J. J. Watkins. "Characterization of Ordered Mesoporous Silica Films Using Small-Angle Neutron Scattering and X-ray Porosimetry." *Chemistry of Materials* **2005**, *17(6)* 1398-1408.

Soles, C. L., Lee, H. J., Lin, E. K., and Wu, W. L., "Pore Characterization in low-κ Dielectric Films using X-ray Reflectivity: X-ray Porosimetry" NIST Special Publication 960-13 (2004).

Interconnect Materials and Reliability Metrology

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in two sub-sections, each focusing on a single aspect. These are:

- Basic Materials Properties
- Test Structures for Interconnect Metrology and Modeling

Basic Materials Properties

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Goals

The objectives of this project are: (1) to develop experimental techniques to measure the material properties that control the reliability of thin conducting and insulating films in interconnects under mechanical, thermal, and electrical stresses; these include basic tensile properties, elastic modulus by both static and dynamic means, residual stresses and strains, fatigue and fracture resistance, and thermomechanical response. (2) to advance the ability to anticipate and meet interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of failure in nanoscale interconnect structures.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 11 thin-film layers now, and will reach 14 layers in the long term *(International Technology Roadmap for Semiconductors, 2006, Interconnect, Tables 80a-b)*. These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low-κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the *Roadmap (2005 Edition), Interconnect, p. 41, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated*. The 2005 iNEMI *(International National Electronics Manufacturing Initiative) Research Priorities* document reports a similar need. The top five research areas listed by iNEMI include *Materials & Reliability* and *Design*. Under *Design*, the top five research priorities include *Mechanical and Reliability Modeling, p. 16*. Appendix C of the document has a detailed section on *Reliability, Mechanical Analysis, and Simulation, p. 44*, which emphasizes the need for material characterization and reliability prediction. Key considerations in this paragraph and elsewhere in the document are effects of temperature and of cyclic loading and effects of size scaling. The iNEMI document specifically calls out the need to *predict and understand failures in MEMS devices, p. 39*. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets, and with the push into exotic nanoscale materials.

Because the films are formed by physical vapor deposition, electrodeposition, or spin-on deposition, their microstructures, and hence, their mechanical properties, are different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results. Industry needs test methods that are efficient and integrable in the fab environment. We see nanoindentation and high-amplitude a.c. measurements as candidates to become routine, or perhaps even on-line, methods. Compared to these, the microtensile test is more laborious, but it provides unambiguous results. We will continue to promote and offer the microtensile test as a reference method, while developing methods to extract needed material property information from the more integrable methods such as nanoindentation and high-amplitude a.c. testing.

We are also working on TEM- and SEM-based techniques for measurement of local strains, to provide detailed information about the nature of deformation and stress-strain response in the

dimensionally-constrained materials that make up microelectronic systems. The techniques are based on electron diffraction measurements of lattice parameters and have spatial resolutions that are compatible with state of the art device dimensions. Electron backscatter diffraction (EBSD) offers a means by which such strains may potentially be mapped with near-20 nm resolution, since the technique is integrated with the scanning action of a SEM. Convergent-beam electron diffraction (CBED) is a TEM technique that can potentially measure strains with better than 5 nm spatial resolution, but requires specimen thinning, and is therefore subject to artifacts. We have efforts under way to advance both approaches.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset, to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology. We held a workshop entitled Reliability Issues in Nanomaterials, 17–19 August 2004, to gauge customer interest in the available tools for characterization of nanomaterials, which, of course, encompasses advanced interconnect structures at both current and foreseen size scales. Microelectronics manufacturers were represented, along with universities, national laboratories, and more general commercial interests. The referenced report gives the details, but two key messages for this research project were the widespread adoption of nanoindentation for material characterization, and the serious consideration given to atomic-scale materials engineering. We are planning the second such workshop, entitled "Materials Characterization for Nanoscale Reliability," to be held in Boulder in August, 2007, to gauge progress in development of reliability metrology applicable to microelectronics and nanomaterials, and to update metrology needs that could be addressed by NIST.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand. We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1). Occasionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry.

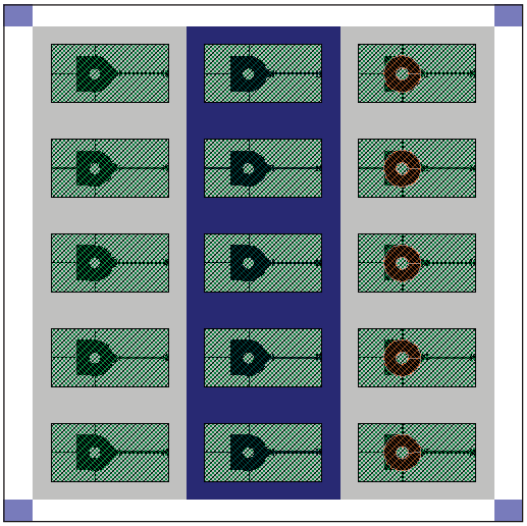

Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. thermomechanical fatigue and micro- and nanoscale characterization of industrially relevant materials. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the SEM. This system has now been used on specimens as small as 2 μm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

We have begun an effort on electrodeposited copper, including specimens from industrial colleagues and produced in-house, to characterize the variability of the mechanical behavior of electrodeposited copper with deposition conditions, film thickness, annealing, and other relevant variables.

DELIVERABLES: A one-day short course consisting of 6 lectures by NIST staff on Interconnect-Relevant Characterization & Metrology was given in conjunction with the 2006 Advanced Metallization Conference. A repeat of this short course at the 2007 conference is under consideration. 4Q 2007

Our measurements involving alternating current stressing of chip-level interconnects are being used to explore the relationships between electrical, thermal, and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in unconstrained lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including EBSD, SEM, and TEM has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This indicates at least the possibility that electrical tests may be exploited to produce information about the mechanical characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because of the experimental convenience of electrical stressing on specimens of a wide range of sizes, including very small.

We have recently presented the first set of experimental data comparing the results of high amplitude a.c. testing and tensile testing on the same material.

DELIVERABLES: Technical publication comparing results of high amplitude a.c. and microtensile testing on e-beam-deposited aluminum, in press. 3Q 2007

The initial ultimate strength value deduced from the a.c. test by extrapolating the results back to one loading cycle, and correcting for the residual stress present in the line-on-substrate specimen, was approximately equal to the value measured in the tensile test. However, physical differences between the tests include: thermomechanical vs mechanical stressing; elevated and variable temperature in the a.c. test; residual stresses in the film on substrate vs none in the free-standing tensile specimen; substrate constraint causing biaxial loading as well as additional strengthening in the a.c. test; and cyclic loading vs monotonic strain to failure. By more realistic treatment of these differences, in measurements on specimens of different materials with different grain sizes and different line widths, we will quantify the uncertainty with which static mechanical properties can be deduced from the a.c. test. By comparison, the rule for obtaining the ultimate tensile strength from a nanoindentation test typically overestimates the microtensile result by a similar amount.

DELIVERABLES: We are planning the 2nd NIST Workshop on Reliability Issues in Nanomaterials. 3Q 2007

We are also developing non-contact optical methods to measure mechanical properties of thin films and interconnects using MEMS test structures that are compatible with the CMOS process. Such non-contact methods may be useful in monitoring the variations of mechanical properties in the production environment. A method has already been developed to measure the residual strain in the passivation and interconnect films using fixed-fixed beams. We are currently developing resonant measurements for cantilever beams to characterize the elastic modulus of each layer (Fig. 2).

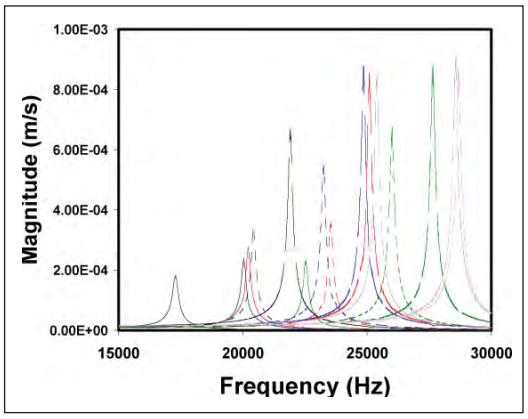

Figure 2. Resonant frequency response of micromachined CMOS cantilever test structures.

The method is based on the fact that the resonant frequency of the cantilevers is related to their elastic modulus, density, and the geometry. They can be fabricated with different combinations of

layers and then comparisons of the resonant frequency can be used to extract the modulus of the individual layer. The cantilever test structures can be fabricated simultaneously with the fixed-fixed beams and measurements of residual strain and strain gradient can be made. With the residual strains, from the fixed-fixed beam method, the elastic constant, from the resonant method, and the strain gradient, from the curvature of cantilevers, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens. 4Q 2007

Accomplishments

■ Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results. Microstructural characterization is critical for defining the applicability of test results for different materials and test techniques. Currently, we are improving our measurements for characterizing the microstructure of electrodeposited copper in order to better understand the influence of microstructure on reliability. Figure 3 shows the grain structure of a commercially produced copper film, as mapped out by electron back scatter diffraction. The colors represent local crystallographic orientation, according to the inset. Regions of constant color are metallographic grains. The long, straight, parallel boundaries are twin boundaries.

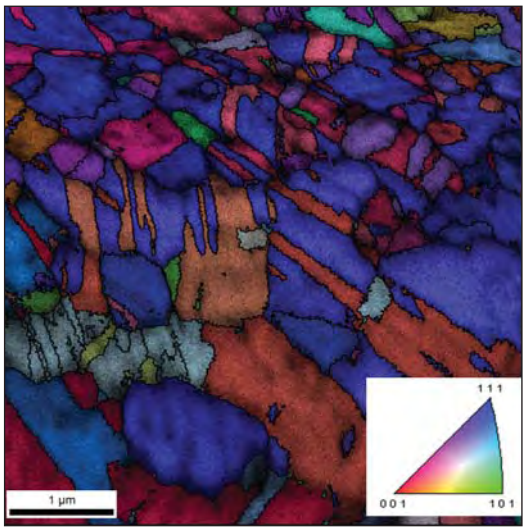

Figure 3. EBSD map of electrodeposited copper film specimen. The colors indicate the surface-normal crystallographic orientation of each pixel, according to the key, inset. Regions of constant color are metallographic grains. The long, straight, parallel boundaries are twin boundaries.

■ Based on input received at the workshop on Reliability Issues in Nanomaterials, discussed above, an international round robin to assess interlaboratory reproducibility of measurements of hardness and elastic modulus by instrumented indentation, on thin film materials typical of those used in interconnect structures in microelectronic devices, has been conducted; a technical publication reporting the results is in review.

DELIVERABLES: Paper reporting round robin has been accepted for an upcoming special issue of *Metallurgical Transactions A*. 3Q 2007

■ A specimen film selected after consultation with a group of experts in the field, consisting of a copper film with a platinum passivation layer, was contributed by Sandia National Laboratory. Open participation was solicited by e-mail to over 100 laboratories. Fragments of the specimen wafer were distributed to approximately 30 laboratories around the world. The goal was to obtain results representative of the experience of a "typical customer" using a testing laboratory. Approximately 25 laboratories conducted tests and contributed reports. The results have been analyzed with assistance from the NIST Statistical Engineering Division. The scatter in modulus and hardness are much larger from laboratory to laboratory than within laboratories; Fig. 4 shows the hardness data.

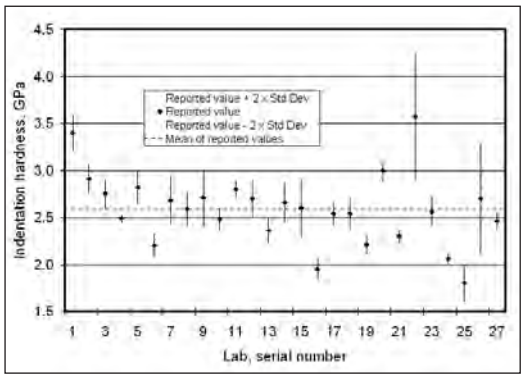

Figure 4. Reported results for indentation hardness of the round robin specimen material, a Cu film on a silicon substrate. The error bars at each data point span a total range of 4 times the standard deviation reported for multiple indentations. The average of the reported hardness values is 2.59 GPa.

This result indicates that comparisons of instrumented indentation results from different laboratories should be treated with caution, and that further investigation is needed to identify the sources of the scatter.

DELIVERABLES: Papers based on two conference presentations on the comparison of electrical and mechanical stress effects have been accepted for the respective technical conference proceedings, to appear in 3Q 2007.

■ We have been working to demonstrate the applicability of our small-scale mechanical testing techniques to materials recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5.

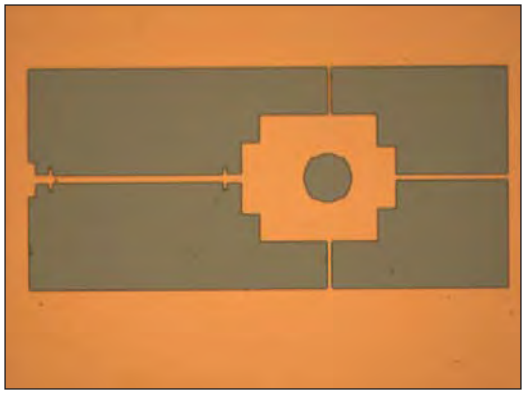

Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 μm to 10 μm, increases the ductility from around 1 % or less to 5 % or more. These data were obtained in microtensile tests of a new variety of electrodeposited copper supplied by an industry collaborator. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 °C. Figure 6 shows recent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

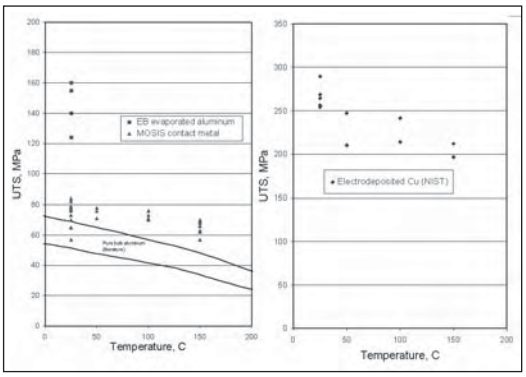

Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

Figure 7a (next page) shows a high-resolution SEM image of the surface of an electrodeposited (ED) copper specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, microstructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic model that simulates the mechanical behavior of this morphology, though at a smaller scale. The atoms shown as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible

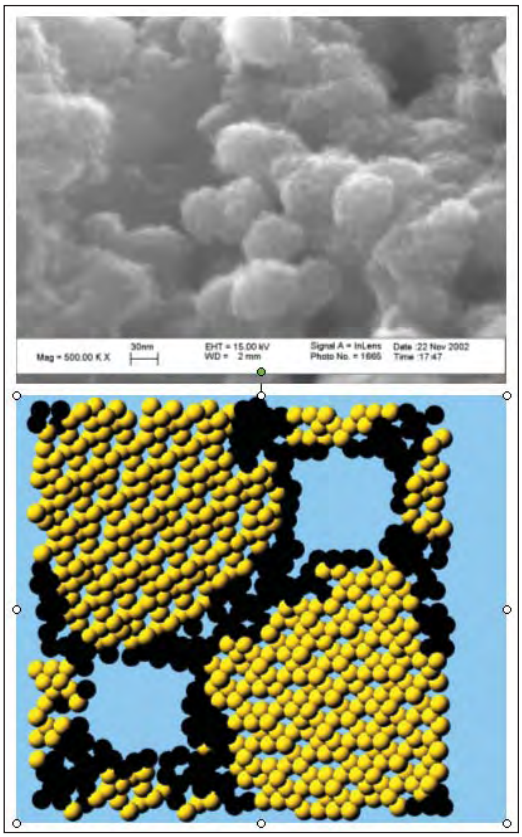

Figure 7. (a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper "balls" are 30–50 nm in diameter. (b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal face-centered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000 atom model simulates a specimen of indefinite size.

explanation for our measured value of the elastic constant of ED copper, which is lower than the bulk value. We have extended our atomistic modeling to the mechanical behavior of quantum dot structures such as germanium in silicon and indium arsenide in gallium arsenide, specifically, the strain in and around the heterogeneous inclusion. Strains surrounding the quantum dot structures play an important role in creating the confined electron states and in providing a driving force for self-assembly of arrays of dots. Our recent paper on GeSi quantum dots, listed below, modeled strains around a quantum dot and predicted surface distortions above buried dots; these might be usable to deduce characteristics of buried dots, such their size and depth beneath the surface, from measurements at the surface.

■ Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. To understand the results, we have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 8).

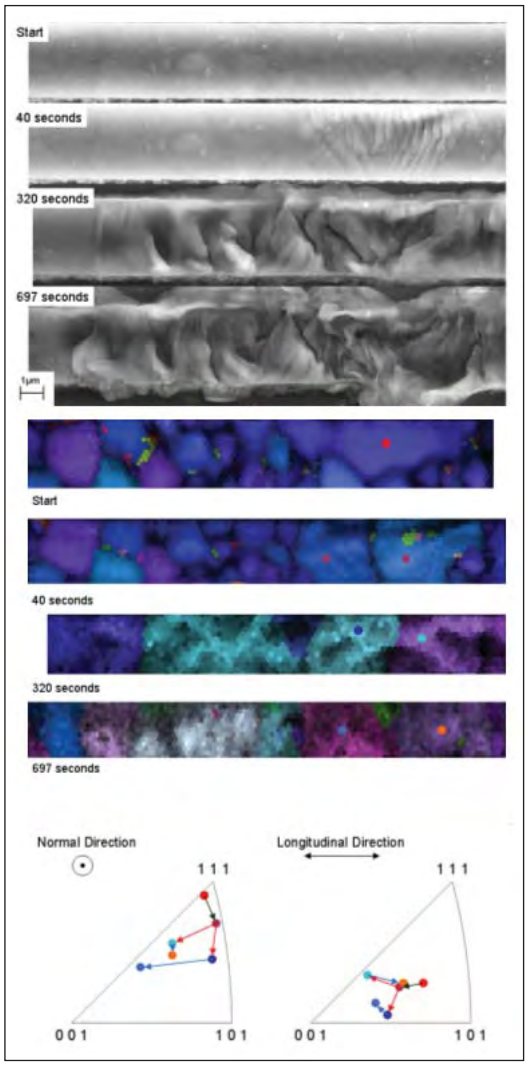

Figure 8. A.C. testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of A.C. cycling at about 12 MA/cm^2. Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect. We are exploring the applicability of the a.c. test to commercial damascene copper structures. In these initial experiments we have plotted the data as lifetime to open circuit *vs* cyclic temperature range in Fig. 9.

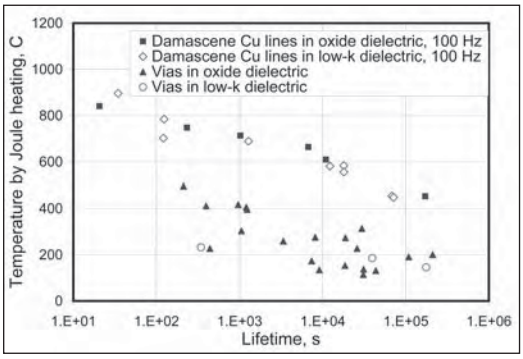

Figure 9. Comparison of lifetimes under high amplitude a.c. of Cu lines and Kelvin vias in damascene structures made with oxide and low-κ dielectric, plotted as cyclic temperature vs lifetime. When plotted in these coordinates, the vias fail at much lower temperatures than the lines in both structures, but the dielectric material does not affect the lifetimes.

On this basis, we found a big difference between vias and lines, but no difference between oxide and low-κ dielectric structures. The preliminary conclusion from these tests is that the combined effects of thermal, electrical, and mechanical stresses need to be accounted for in designing reliable interconnect systems, and that with the a.c. test we can explore material response to all of these stresses.

It is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process. In the Micro- and Nano-Electro-Mechanical Technology (MNT) Metrology Project, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. More information on this effort can be found on that project's report.

Collaborations

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MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

Recent Publications

R. R. Keller, N. Barbosa III,, R. H. Geiss, and D. T. Read, *An Electrical Method for Measuring Fatigue and Tensile Properties of Thin Films on Substrates*, Key Engineering Materials, Vols. 345-346 (2007) pp. 1115-1120 (online at http://www.scientific.net).

D. T. Read and V. K. Tewary, *Multiscale model of near-spherical germanium quantum dots in silicon*, Nanotechnology 18 (10) 105402, 2007.

R. H. Geiss and D. T. Read, *Need for Standardization of EBSD Measurements for Microstructural Characterization of Thin Film Structures*, accepted for publication in Proceedings of the 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, to be published by the American Institute of Physics, 2007.

D. T. Read and R. H. Geiss, *High Amplitude AC Tests of 300-nm Damascene Interconnect Structures*, submitted to Materials Research Society Symposium Proceedings, 2007.

D. T. Read and A. A. Volinsky, *"Thin Films for Microelectronics and Photonics: Physics, Mechanics, Characterization, and Reliability,"* in Micro- and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging, edited by E. Suhir, C.P. Wong, Y.C. Lee, Springer, New York, 2007.

N. Barbosa III, R. R. Keller, D. T. Read, R. H. Geiss, and R. P. Vinci, *"Comparison of Electrical and Microtensile Evaluation of Mechanical Properties of an Aluminum Film,"* submitted to Metallurgical and Materials Transactions April 2006. Paper presented at 2006 TMS Annual Meeting.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* submitted to Metallurgical and Materials Transactions April 2006. Paper presented at 2006 TMS Annual Meeting.

D. T. Read, R. R. Keller, N. Barbosa III, and R. H. Geiss, *"Nanoindentation Round Robin on Thin Film Copper on Silicon,"* submitted to Metallurgical and Materials Transactions April 2006. Paper presented at 2006 TMS Annual Meeting.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, *"Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects,"* Mater. Res. Soc. Symp. Proc. Vol. 863, B9.5.1, (2005).

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R. R. Keller, C. A. Volkert, R. H. Geiss, A. J. Slifka, D. T. Read, N. Barbosa III, and R. Mönig, *"Electrical Methods for Mechanical Characterization of Interconnect Thin Films,"* 2005 Advanced Metallization Conference, p. 643-648.

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Robert R. Keller, David T. Read, and Roop Mahajan, NIST Special Publication 1043, Workshop on Reliability Issues in Nanomaterials, U.S. Department of Commerce, August 2005.

R. R. Keller, and D. T. Read, *"The NIST Workshop on Reliability Issues in Nanomaterials, August 17-19, 2004,"* Proceedings, Government Microcircuit Applications & Critical Technology Conference 2005, Las Vegas, NV, April 4-7, 2005.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, *"Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects,"* Materials, Technology, and Reliability of Advanced Interconnects: MRS Symposium Proceedings, March 28-April 4, 2005, San Francisco, CA.

R. H. Geiss, R. R. Keller, D. T. Read, and Y.-W. Cheng, *"TEM Analysis of Deformation in Thin Films of Aluminum after both A.C. Thermomechanical and Tensile Deformation,"* Thin Films – Stresses and Mechanical Properties XI: MRS Symposium Proceedings, March 28-April 4, 2005, San Francisco, CA.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, "Electric Current Induced Thermomechanical Fatigue Testing of Interconnects," AIP Conference Proceedings 788, Characterization and Metrology for ULSI Technology, pp. 491-495 (2005).

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R. Monig, R. R. Keller, and C. A. Volkert, *"Thermal fatigue testing of thin metal films,"* Review of Scientific Instruments 75 (11): 4997-5004, November 2004.

D. T. Read, Y.-W. Cheng, and R. Geiss, "Morphology, Microstructure, and Mechanical Properties of a Copper Electrodeposit," Microelectronic Engineering, 75 (1): 63-70, July, 2004.

D. Josell, C. Burkhard, Y. Li, Y.-W. Cheng, R. R. Keller, C. A. Witt, D. R. Kelley, J. E. Bonevich, B. C. Baker, B. C., and P. Moffat, "Electrical properties of superfilled sub-micrometer silver metallizations," Journal of Applied Physics, 96 (1): 759-768, July 1, 2004.

Test Structures For Interconnect Metrology and Modeling

Technical Contacts:
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H. Schafft

Goals

The overall goal is to make contributions to a test-structure infrastructure that is relevant to selected state-of-the-art interconnect-system needs as stated by the ITRS *Interconnect* Report 2005 which states that the function of an interconnect system is to distribute clock and other signals and to provide power/ground, to and among, the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of integrated circuits in the face of further scaling of feature sizes.

Test-structure metrology applications can be classified into two categories: (1) optimal selection of materials and processes for developing and maintaining fabrication processes for new interconnect systems that comply with increasing device density and performance needs, and, (2) parameter extraction for modeling and predicting the performance of interconnect systems for particular fabrication architectures. In the first category, the project's test structures for process development target the extraction, by electrical means, of key dimensional parameters such as conductor CD. This is a key unsolved problem for cases in which copper conductors are embedded in barrier metals of different species. Additionally, the adverse interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features, particularly those of the wider upper-level conductors, is a related and as-yet unresolved issue. In the second category, a near-term goal in materials studies is the fabrication of electrically testable, all copper, features having lateral dimensions in the 20- to 100 nm range. This project's unique approach seeks to assess the impact of CD scaling on the fundamental physics of electron transport in features built from single metal species, such as copper, without the metrology complications resulting from having other metal species incorporated into interconnect features. The information is to generate a computational infrastructure to facilitate modeling the performance of features that are replicated with two or more metals and to aid the verification of dimensional parameter extraction for process-control purposes. Among the test structures being implemented for modeling the performance of advanced interconnect implementations are strip lines that are to be rf-tested from d.c. to 10 GHz, consistent with projected clock speeds of integrated circuits over the next half decade.

Customer Needs

Interconnect is becoming the principal factor that determines the maximum performance that can be attained with emerging generations of integrated circuits. The dramatic reversal, from performance which is limited by transistor delay to that which is limited by interconnect delay, challenges the approach of continuing to scale the conventional metal/dielectric system to meet future interconnect requirements. Future advances in IC performance will be governed increasingly by the advances in interconnect technology, at least as much as by advances in active devices. As aluminum is replaced by hybrid copper/barrier-metal conductors, the initial benefits of the higher conductivity are becoming problematic as a result of the predominance of contributions of the barrier metal to the effective conductor resistance. There are two mechanisms. When barrier metal, with its higher resistivity, replaces more highly conducting copper, the proportion of the total CD, which is allocated to copper, is reduced dramatically as CD is scaled. Confounding the phenomenon, higher clock speeds favor conduction by the outer regions of the composite conductor, which render it adversely non-linear. Modeling the generalized binary-metal interconnect conductors at high frequencies is therefore a central issue. This is a very complex task on which no known reports exist in the technical literature. However, we have been able to make a start on providing a tool for dealing with this issue by drawing on NIST resources in other Divisions.

Whereas there is no simple global solution to the challenge of electrical metrology for extracting the CDs of binary-metal interconnect conductors at this time, advances being pursued by this project are likely to play a leading role. Finally, overlay is a metrology challenge that is attributable as much to scaling per se, rather than to the materials selected for interconnect implementation. Overlay metrology is being challenged by exacerbation of the tool- and wafer-induced shifts that are generally manageable for technology generations introduced prior to the present time.

Technical Strategy

The four-part current technical strategy is to build on opportunities afforded by the project's unique SCCDRM experience. The same substrates that have been developed for CD reference-material applications are being applied to the fabrication of single-metal, initially copper-only, test structures with features having lateral dimensions in the 20 nm to 200 nm range. The novel process-flow, which has been reported in a joint paper with the University of Edinburgh at recent conferences, is illustrated in Fig. 1. The approach shown there enables a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the complications resulting from having other metal species that serve as barrier layers. The information so provided enables modeling the performance of features that are replicated with copper-cored binary-metal technology and will aid in the verification of dimensional parameter extraction for process-control purposes.

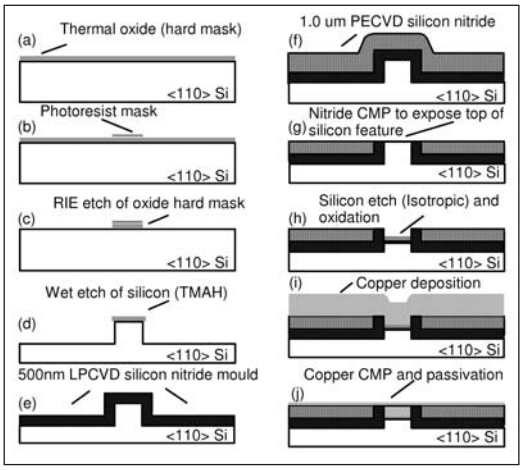

Figure 1. The process flow which was devised for the fabrication of single-metal, copper-only, test structures with features having lateral dimensions in the 20- to 100-nm range.

The project's tool-kit has a test structure that will allow the extraction, by electrical means, of key dimensional parameters for process-control purposes such as copper-cored interconnect-feature CD. This responds to an unsolved problem when copper conductors are embedded in barrier metals. The solution is sought after by companies marketing interconnect-system modeling software tools and their industry clients. Our strategy is based on a test structure we first proposed and published several years ago.

We are continuing a study of the interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features at frequencies that need to be extended to ~100 GHz. This higher upper limit is driven by near-term year clock speeds having rising and falling edge components that substantially exceed 20 GHz. As mentioned above, higher clock speeds favor conduction by the outer regions of the binary-metal interconnect conductor through the so-called "skin effect" phenomenon, which render it adversely non-linear. The technical strategy is to model the parameters of a selection of binary-metal interconnect-conductor architectures using the distributed resistance, inductance, conductance, and capacitance (RLGC) model over the sated range of frequencies using finite-element Maxwell software, which is available at NIST. This approach is quite ambitious and there are no known analytical solutions for generalized binary-metal interconnect conductors. Since there is no report of such analyses in the scientific literature, we have chosen first to verify our Maxwell solutions for a selection of single-metal architectures for which analytical solutions do exist.

A class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. This project has successfully applied for patents on an electrically calibrated test structure to serve as a process- and tool-specific overlay standard that avoids all the limitations of other approaches. The strategy is to reduce the concept to practice by replicating the test structures with a bi-level polysilicon-metal process and conduct parametrical testing. Among the test structures that are being designed for modeling-parameter extraction are strip lines that will be rf-tested from d.c. to 40 GHz, consistent with clock speeds of road-map integrated circuits over the next several years. The strategy is the computation of rf-impedance parameters from S-parameter measurements. An important spin-off from this activity is the application of rf-measurements to validating key dimensional parameters of masks which are patterned for interconnect fabrication, another application which has been sought by the mask-vendor and mask-user industries. This work will be done initially on binary masks but, if successful, will be extended to the examination of opportunities in dimensional metrology for more complex binary-mask applications. Further into the future, the experience gained here may be useful for development of a non-contact electrical-CD metrology, which is understood to be needed by the photo-mask industry.

The ITRS *Interconnect* Report of 2005 relates how both grain-size and feature dimensions affect the effective resistivity of copper in the electrical wiring of integrated circuits. The consequences are of growing concern because new technologies require ever-smaller dimensions that lead to greater resistance and faster operation, which requires smaller resistance. This project strategy is to develop an easy-to-use, versatile effective-resistivity simulation program that is superior to other approaches in use for studying size effects in collaboration with a graduate program at George Washington University. It shows how scattering of electrons by surfaces, grain boundaries, and impurities increases the effective resistivity of copper in thin films and lines as dimensions approach and become shorter than the mean free path of electrons in bulk copper. In related experimental work, copper films are fabricated, their sheet resistances and physical thicknesses are measured, and the predictions of the simulation program are compared to experimental results. Figure 2 shows the various scattering events that are included in the simulation program to simulate size effects in copper that was reported in a recent NIST news release.

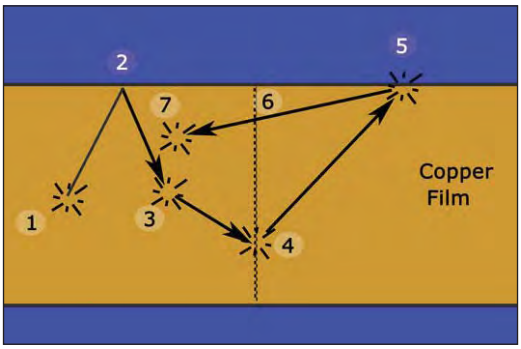

Figure 2. The scattering events that are included in the simulation program to simulate dimensional effects in copper.

The project is also providing technical and related support to the JEDEC Committee JC14.2 on Wafer Level Reliability of the JEDEC Solid State Technology Association to enhance the reliability of in the new copper interconnect technologies. This support is for revising interconnect standards, which were originally written for aluminum interconnects, so that they will be applicable to copper metallization. The primary focus is in writing a new JEDEC standard for constant current and temperature stress testing for electromigration, assisting in revising the JEDEC standard for isothermal stress testing for electromigration, assisting in preparing a new JEDEC stress test for stress voiding, and for preparing JEDEC guidelines for designing stress-voiding test structures.

DELIVERABLES:

- Report results of modeling the distributed resistance values of interconnect conductors that can be simulated by both analytical solutions and a commercial Maxwell solver. 1Q 2007
- Complete analysis of experimental measured increase in effective resistivity of copper films with thicknesses decreasing from approximately 200 nm to 15 nm, and compare measurements with simulation results. 4Q 2006
- Design, and verify by simulation, the performance of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication. 1Q 2007
- Fabricate and test chemically stable test structures having copper-only features and make ECD measurements. 4Q 2007
- Report initial electrical measurements made on second-generation SCCDRM test structures that have been converted to single-crystal nickel-silicide. 1Q 2007
- Design, model, fabricate, and test a selection of co-planar waveguide test structures on chrome-on-glass photo-masks to evaluate the efficacy of developing a non-contact ECD method for sampling printed features. 3Q 2007

Accomplishments

■ As a result of close extended collaboration with the University of Edinburgh, the project has been able to develop and report a unique copper damascene process for the fabrication of a scaled electrical test structure having copper-only features. The purpose is to facilitate studies of electron transport in pure copper without having to correct for the complexities of the interaction of copper with barrier-metal films. This implementation enables the separation of the effects of surface and grain-boundary scattering, as a function of the cross-section dimensions of the conductor by electrical testing. A second joint paper describing the accomplishment was presented at the ICMTS 2007 conference in Tokyo, Japan, on March 8, 2006.

■ In close collaboration with NIST operations in Boulder, Colorado, Maxwell software was applied to the calculation of RGLC parameters of cylindrical copper conductors with diameters ranging from 50 nm to 5000 nm, which were coated with TaN barrier metal of thicknesses typical of

current IC-interconnect applications. At frequencies above 10 GHz, significant increases in resistance were observed. These results have been set aside to allow for verification of the modeling by comparing those of a selection for copper-only wires that were obtained from exact solutions based on Maxwell's equations. Initial results indicate close comparisons for the cases that have so far been compared.

■ A paper that describes a new simulation program and its use to study the effects of surface and grain-boundary scattering on the effective resistivity of copper in thin planar films and small cross-section lines was completed. The paper was accepted for publication in a mid-2006 issue of the Microelectronics Reliability journal.

■ A report was completed that describes a computer program, which simulates the impact of the size on the effective resistivity of line and film conductors. Flow charts and the program code are provided as appendices. This work was published in February 2006 as a NISTIR.

■ In close collaboration with the Laboratory for Interconnect and packaging at the University of Texas at Austin, test structures for the investigation of the effect of linewidth scaling on electron transport in nickel mono-silicide features have been designed and fabricated. The features were patterned on (110) silicon-on-insulator wafers with i-line lithography that replicated test structures from which voltage/current (V/I) measurements could be extracted. Subsequently, the patterning of single-crystal features with direct-write electron-beam lithography has been developed in order to facilitate the future reduction of the linewidths of NiSi features having a highly controlled surface microstructure to linewidths below 40 nm. Figure 3 shows a selection of 40 nm features that were etched in (110) silicon after electron-beam lithography as reported in a joint paper with the University of Texas at Austin at a recent conference.

■ Work has been initiated on a new CD metrology based on coplanar waveguide test structures. Extensive e-m field modeling of characteristic impedance and distributed capacitance, which we have conducted in collaboration with the Department of Electrical & Computer Engineering at George Washington University, indicates that the extraction of these values from S-parameter measurements can be applied to sampling CDs of test-structure features that are printed on photomasks. At this time, the design of a set of thru and de-embedding structures has been designed and a supplier of the substrate has been identified.

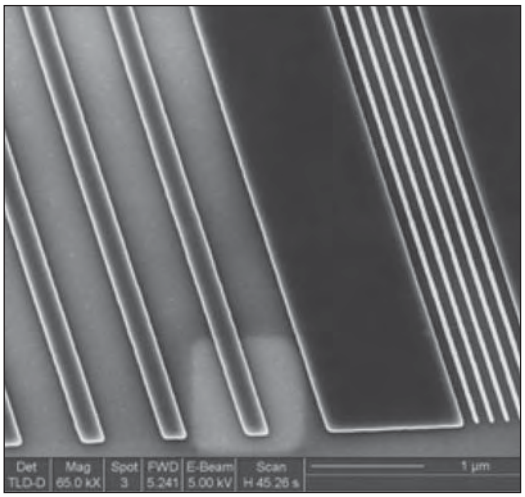

Figure 3. A selection of 40 nm features that were etched in (110) silicon after electron-beam lithography.

■ A poster paper was delivered at the 2005 IEEE International Integrated Reliability Workshop to discuss the details of the model used to simulate size effect on the resistivity of copper, and to describe results of the simulation studies.

■ A new JEDEC standard JESD202 was completed and published in March 2006. The standard describes an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a lognormal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Procedures are provided to analyze complete and singly, right-censored failure-time data.

■ The design and fabrication of a new test chip for the fabrication of test structures that are electrically calibrated to serve as process-specific overlay reference materials for high-density interconnect fabrication has been completed in collaboration with staff at the Scottich Microelectronics Centre of the University of Edinburgh. Preliminary results were presented in a paper at the IEEE ICMTS 2007 conference in Tokyo, Japan, on March 8, 2006.

Collaborations

The leading collaborators are semiconductor processing facilities and laboratories at three major Universities.

The Scottish Microelectronics Centre at the University of Edinburgh (SMC) is now providing a substantial part of the project's wafer fabrication operations. More importantly, the staff there are highly and broadly experienced in interconnect fabrication materials, processes, and issues. Audio teleconferences are exchanged between Project and SMC staff on this and a second project regularly.

The Electrical-Engineering and Computer-Sciences Department at George Washington University has been funding the studies of Ph.D students and a Professor to work on this NIST Project for almost a decade. The present collaboration contributes special skills in rf parameter extraction and the physics of electron transport.

A new collaboration with the Microelectronics Research Center at the University of Texas at Austin has resulted on the transformation of narrow SCCDRM features to silicide material. They are also contributing very desirable ultra-narrow-line lithography for the next-generation SCCDRM fabrication.

This project has always benefited from an active collaboration with Litho-Metrology Operations at SEMATECH. Although this project's focus has only recently shifted away from litho-metrology to interconnect, we are actively pursuing a parallel shift in our collaboration.

Recent Publications

R. A. Allen, R. Dixson, M. W. Cresswell, W. Gutherie, B. J. Shulver, A. S. Bunting, J. T. Stevenson, and A. Walton, "CD Reference Materials Fabricated on Monolithic 200 mm Wafers for Automated Metrology Tool Applications," 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, Mar 27-29, 2007, Gaithersburg, MD (01-SEP-2007).

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Smith, A. J. Snell, J. M. Stevenson, A. Walton, M. W. Cresswell, R. A. Allen, 'Extraction of Sheet Resistance and Linewidth from All-Copper ECD Test-Structures Fabricated from Silicon Preforms', 2007 International Conference on Microlectronic Test Structures, pp.14-19 (22-MAR-2007).

B. Li, L. Shi, P. S. Ho, J. Zhou, R. A. Allen, M. W. Cresswell, 'Test Structures for Study of Electron Transport in Nickel Silicide Features with Linewidths between 40 nm and 100 nm', IEEE ICMTS International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.18-23 (01-APR-2006).

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Snell, J. M. Stevenson, A. Walton, R. A. Allen, M. W. Cresswell, 'Design and Fabrication of a Copper Test Structure as a Electrical Critical Dimension Reference', Proc., IEEE International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.124-129 (01-APR-2006).

C. Nwokoye, M. E. Zaghloul, M. W. Cresswell, R. A. Allen, C. E. Murabito, 'A New Critical Dimension Metrology for Chrome-on-Glass Substrates Based ons-Parameter Measurements Extracted from Coplanar Waveguide Test Structures', SPIE, Bay Area Chrome Users' Symposium, September 18-22, 2006, Monterey, California, 12 pp. (01-OCT-2006).

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JEDEC Standard JESD202, "Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress," March 2006. (Written by H. A. Schafft).

A. Emre Yarimbiyik, Harry A. Schafft, Richard A. Allen, Mona E. Zaghloul, David L. Blackburn: Modeling and simulation of resistivity of nanometer scale copper. Microelectronics Reliability 46(7): 1050-1057 (2006).

W. F. Guthrie, R. G. Dixson, R. A. Allen, M. W. Cresswell, C. E. Murabito, B. Park, "Establishing Traceability of Linewidth Reference Materials Using CD-AFM and HRTEM," 2005 International Conference on Characterization and Metrology for ULSI Technology, March 15-18, 2005, University of Texas at Dallas.

R. A. Allen, A. Hunt, C. E. Murabito, B. Park, W. F. Guthrie, and M. W. Cresswell, "Extraction of Critical Dimension Reference Feature CDs from New Test Structure Using HRTEM Imaging," Proceedings of the 2005 IEEE International Conference on Microelectronic Test Structures, pp. 5- 10, March 2005, Leuven, Belgium.

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Pb-Free Surface Finishes for Electronic Components: Sn Whisker Growth

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M. E. Williams

"NIST provides an invaluable service to the industrial community through unparalleled commitment to understanding the fundamental scientific principles and the basic metrology required to properly investigate a metallurgical problem.."

Dr. Robert Hilty,
Director of Materials Research,
Tyco Electronics
Technology Division
Middletown, PA

Goals

Spurred on by European legislation and the "green movement" of the Pacific Rim countries, the worldwide electronics industry is being compelled to remove lead (Pb) from components. The formation of tin (Sn) whiskers on Pb-free surface finishes is a major reliability issue. Numerous failures due to shorting from whiskers have been reported, especially in the high reliability realm of aerospace, military, and medical device applications. The goal of this project is to provide data and materials measurements of critical importance in order to develop a fundamental understanding of Sn whisker growth and provide industry with information needed for mitigation strategies.

Customer Needs

For many years, electronic component leads and leadframes made of copper (Cu) or Cu alloys were "pretinned" with a protective layer of electrodeposited Sn-Pb prior to use or storage. This protective layer preserves the solderability of the component leads when assembled on circuit boards. Elimination of Pb has been mandated by the European Community (EC) directives on Waste Electrical and Electronic Equipment (WEEE) and the EC Restriction of the Use of Certain Hazardous Substances (RoHS) in Electrical and Electronic Equipment. Both took effect in July 2006. China's version of RoHS was implemented in March 2007. U.S. manufacturers must comply with these requirements in order to compete in the global market.

It is well known that the use of pure Sn protective electrodeposits has serious problems. Sn whiskers (filaments of metal typically 1 μm in diameter and several mm long) can grow from these deposits and cause electrical shorts and failures. Historically, Pb was added to Sn deposits to prevent whisker growth as well as to lower cost. Thus the development of Pb-free Sn alloy deposits to replace Pb-containing Sn deposits is considered important, and tests which ascertain the tendency to form whiskers are critical.

The U.S. microelectronics industry has clearly articulated a need for research and measurement to predict and prevent Sn whiskers in the 2007 International Electronics Manufacturing Initiative (iNEMI), and 2006–2007 IPC technology roadmaps. Specific industrial needs have been identified through NIST participation in the iNEMI technology working groups (TWG) on Sn whiskers. A series of industry and academia sponsored workshops have been held over the past six years to address the problem of Sn whisker growth. In order to prevent or mitigate whisker growth, these workshops have reached a consensus list of concerns: understand the influence of electroplating conditions, grain structure/shape/orientation, compressive stress in the electrodeposits, intermetallic compound (IMC) formation at the SnCu interface, diffusion of Sn, and thermal cycling effects on electroplated components.

Technical Strategy

The current NIST research program has focused on three of industries concerns; viz., plating conditions/grain structure modification, IMC formation, and stress measurements using X-ray diffraction. Many companies are also attacking the list of industry concerns; *e.g.*, Boeing has studied Sn diffusion using Sn isotopes, Agere Systems has lead the way in uncovering thermal cycling effects, and Freescale has examined the relationship between grain orientation and whiskers.

The NIST work is examining the following. Grain size and shape comparison of deposits electroplated at different current densities with and without pulsing and with and without Bismuth (Bi) addition have been conducted. The influence of interfacial IMC growth was eliminated by using a substrate that does not react with the Sn based deposits to form IMC. The use of X-ray diffraction has been employed to measure the stress in electroplated Sn deposits. iNEMI, specifically requested NIST to, ".... take the leadership role in developing the measurement standards and the required degree of process specificity."

DELIVERABLES:

- Determine feasibility of X-ray $\sin^2\psi$ methods for measuring residual stress in Sn electrodeposits. 3Q 2007
- Determine methods to eliminate columnar grain structure in Sn electrodeposits. 3Q 2007
- Complete Manuscript "The influence of pulse pulsing on the grain structure of Sn Electrodeposits." 4Q 2007

Accomplishments

■ Two separate studies involved modifying the Sn grain structure. Varying the electroplating current density through a wide range modified both the grain size and structure of the Sn deposit (see Fig. 1).

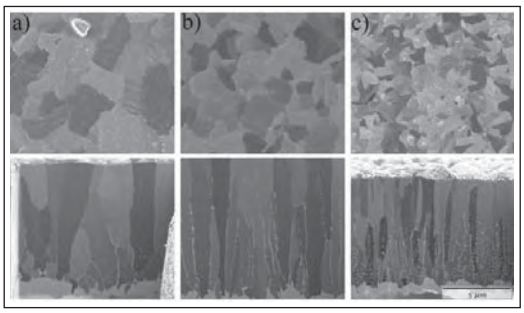

Figure 1. Surface microstructures and cross section FIB microstructures of bright Sn on Cu substrates depending on current density: a) 30 mA/cm2 b) 90 mA/cm2, and c) 200 mA/cm2. As the current density increases, the columnar grain size decreases and the grain shape changes from wavy grain boundaries to facetted grain boundaries.

■ The addition of Bi combined with pulse plating disrupted the columnar structure resulting in equiaxed grains. Under certain values of plating current and levels of Bi solute addition, the filamentary whisker growth was eliminated.

■ Intermetallic compounds (IMC) form at the interface between the Sn deposit and Cu substrates. Bright Sn and a bright Sn-Cu alloy were plated on Tungsten (W), a substrate material that does not form intermetallic compounds with Sn, and stored at room temperature. As with the electrodeposits on Cu, the deposits on W showed hillocks on pure Sn deposits and whiskers on the Sn-Cu alloy. Thus the absence of interfacial IMC had no effect on the formation whiskers. This is important because several authors have claimed that IMC formation is the unique cause of whisker growth.

■ Residual stress in electroplated Sn deposits was measured using the $\sin^2\psi$ X-ray diffraction method. The anisotropic nature of the Sn crystal lattice (bct) and the low stress levels (~ 10 MPa) presented many challenges for this technique. A detailed analysis of errors in the measurement method as it applies to Sn has been performed and a best practice guide is being written.

■ NIST remains a co-chair of the iNEMI Sn Whisker Modeling Group (members include ChipPAC, Cookson, Delphi Delco, Freescale, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics). NIST is also an active participant in the iNEMI Accelerated Sn Whisker Test Group.

Collaborations

International Electronics Manufacturing Initiative (iNEMI); Co-Chair of the Sn Whisker Modeling Group and a member of the Accelerated Sn Whisker Test Group. In an effort to develop a standard X-ray diffraction method to measure stress in Sn electrodeposits we are conducting round robin experiments with Dr. Robert Hilty of Tyco Electronics located in Middletown, PA.

Northrup-Grumman, Linthicum, MD; NIST provided fast growing whisker samples of Sn-Cu electrodeposits on Zn substrates for tests of acrylic conformal coatings. These samples can reduce the evaluation time of the coatings used by industry as a whisker mitigation method to prevent whisker related failures of electronic devices.

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Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Copper is now predominantly the conductor of choice over aluminum because of its intrinsic higher conductivity. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates are required. Additionally, the gate conductor, traditionally polysilicon, is being replaced by metal or metal silicide to eliminate the polysilicon depletion effect. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water and other contaminants at extremely low levels in process gases present serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Atomic layer deposition processes are increasingly being used for high quality thin dielectrics and conductors. Techniques for understanding the deposition mechanisms and characterizing the compounds that are formed are being developed. Theoretical studies elucidating the thermodynamics and quantum mechanical properties of these compounds are being conducted.

Gas Property Data and Flow Standards for Improved Gas Delivery Systems

Goals

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition and the calibration of mass flow controllers (MFCs). As the data are acquired, they will be posted to an online database.

NIST also will develop primary standards for gas flow in the range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry (10^{-6} mol/s ≈1.3 standard cubic centimeters per minute (sccm)).

Customer Needs

The 2005 *International Technology Roadmap for Semiconductors* (ITRS) emphasizes that the grand challenge for front-end processes is "material limited device scaling." The Modeling and Simulations section reinforces this theme: *"Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Databases ... are needed."* Meeting this challenge will require improvements in MFCs for the deposition and etching of diverse new materials. Thermal MFCs meter a wide variety of toxic, flammable, and corrosive gases over a large range of flow rates. Elements necessary for improved MFCs will be accurate models of gas properties and reliable physical standards for gas flow.

Participants at an industry workshop at NIST identified the gases and properties of highest priority, and they recommended publishing the property values in a public, Web-based database. The gases include process gases, "surrogate" calibration gases, and binary mixtures of process and carrier gases. The identified properties and required uncertainties include the following.

heat capacity at constant pressure	±0.1 %
equation of state (gas density)	±0.1 %
viscosity	±0.5 %
thermal conductivity	±0.5 %

The workshop also required the following uncertainties for physical standards for gas flow.

primary standards for gas flow	±0.025 %
transfer standards for gas flow	±0.1 %

Technical Strategy

We are measuring the speed of sound $u(T, p)$ in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have relative standard uncertainties of 0.01 %. Measurement conditions range as high as 425 K and 1500 kPa (or to 80 % of the vapor pressure for condensable gases). Figure 1 shows an example of such data. The speed-of-sound data are used to determine the ideal-gas heat- capacity $C_p^0(T)$ with the targeted uncertainty of 0.1 %. The pressure and temperature-dependences of $u(T, p)$ are correlated with model two-body and three-body intermolecular potentials. These potentials are used to calculate the virial equation of state for the density $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have uncertainties that are less than 0.1 % for density, 10 % for viscosity, and 10 % for thermal conductivity from 200 K to 1000 K.

We also are developing novel acoustic techniques to measure the viscosity and thermal conductivity with uncertainties of less than 0.5 % as specified

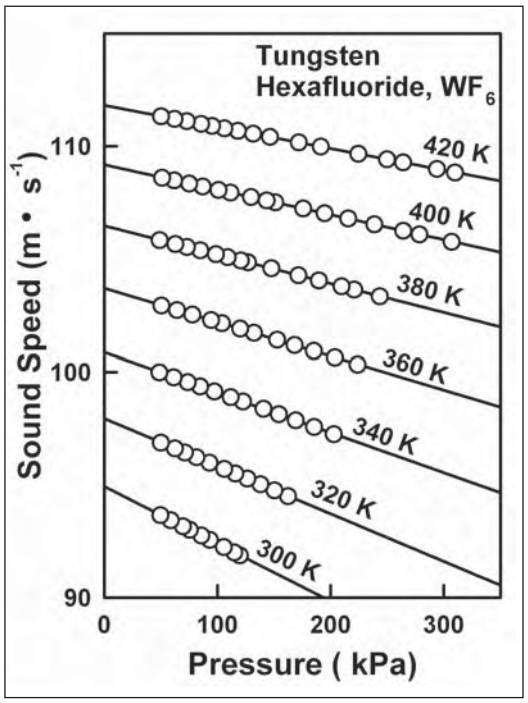

Figure 1. Speed of sound in tungsten hexafluoride as a function of pressure along isotherms.

Technical Contacts:
J. J. Hurly
M. R. Moldover

"I was pleasantly surprised when I came across your database of thermophysical properties of gases used in the semiconductor industry.

It was virtually exactly what I was searching for."

Bob Rathfelder,
Project Engineer,
Parker Hannifin

by the industry workshop. Figure 2 shows a second-generation acoustic viscometer made from Monel. Throughout the project, the results will be made available to industry through publications in professional journals, presentations at professional meetings, and entries in an on-line database at http://properties.nist.gov/semiprop (see Fig. 3).

Figure 2. Second-generation acoustic viscometer made from Monel for use with corrosive gases.

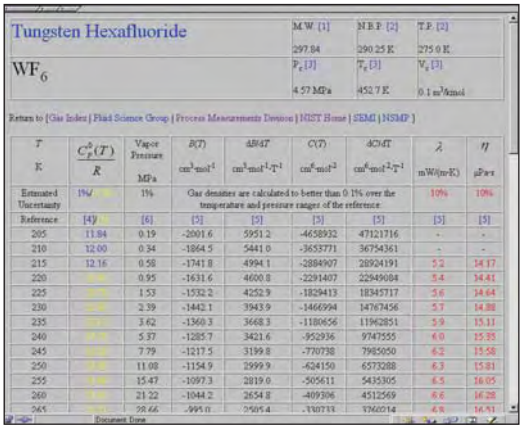

Figure 3. Sample page from on-line database located at http://properties.nist.gov/semiprop/.

We have developed a diverse series of primary standards for gas flow. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10^{-3} mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5–9 atmospheres. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle. The second and third standards have a standard uncertainty of 0.02 %. Figure 4 demonstrates the accuracy of the flow standards.

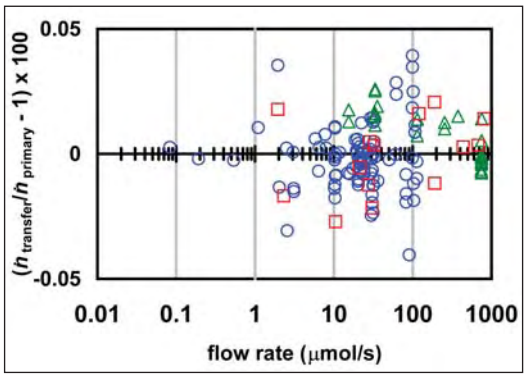

Figure 4. Comparison of three primary flow meters. The transfer standard compared the constant-pressure flow meter (circles) with the gravimetric flow meter (squares) and a constant-volume flow meter (triangles). (1 μmol/s ≈ 1.3 sccm.)

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations, such as MFC manufacturers. Although a flow meter manufacturer often uses its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular cross-section. It was used to perform on-site proficiency tests of industrial flow standards at fabrication facilities and MFC manufacturers. The second-generation transfer standard uses quartz capillaries with a circular cross-section, which are available commercially for gas chromatography. It has been used for comparisons with metrological institutes of other countries as well as manufacturers of flow meters. Its standard uncertainty is 0.03 %. The third-generation standard improves convenience by combining the quartz capillary with commercial instrumentation to measure pressure and temperature.

DELIVERABLES:

- Install new spherical resonator for measuring the speed of sound in the hazardous gases facility. 4Q 2007
- Calibrate resonator. 4Q 2007

A cylindrical resonator was used to study nine process gases, but it must be replaced due to contamination. A spherical resonator has been fabricated and will be installed in the hazardous gas handling facility. The spherical resonator will be capable of producing higher accuracy measurements than the cylindrical resonator.

DELIVERABLES:

- Develop improved model of acoustic viscometer. 2Q 2007
- Develop model of acoustic thermal conductivity resonator. 3Q 2007

The second-generation Greenspan viscometer incorporates lessons learned from the previous device, thereby allowing an improved acoustic model. The model of the thermal conductivity acoustic resonator will need to be tested and further developed from calibration measurements.

DELIVERABLES: Publish in an archival journal the measured viscosity in BCl_3, Cl_2, HBr, C_4F_8, CO, CO_2, NH_3, and SiF_4. 2Q 2007

The acoustic model for the Greenspan viscometer must be applied to each data set to calculate the viscosities of the gases as a function of temperature and pressure.

DELIVERABLES: Update on-line database by with viscosity measurements in BCl_3, Cl_2, HBr, C_4F_8, CO, CO_2, NH_3, and SiF_4. 4Q 2006

The measurements will be disseminated through papers in professional journals, talks given at professional meetings, and the on-line database.

Accomplishments

■ We designed and assembled a second-generation Greenspan viscometer. Its Monel construction allows the study of corrosive process gases.

■ We measured the speed of sound in the process gases Cl_2, NF_3, and N_2O. Typically, the standard uncertainty of the speed of sound was less than 0.01 %. From these data the ideal-gas heat-capacity was determined to within 0.1 %, and an equation of state was developed to predict the gas densities to within 0.1 %. Viscosity was measured in these three gases plus CF_4 and C_2F_6 with an uncertainty of approximately 0.5 %. Viscosity was also measure in the gases BCl_3, Cl_2, HBr, C_4F_8, CO, CO_2, NH_3, and SiF_4. This data set is being prepared for publication and addition to the online database.

■ We continued to provide immediate access to our results by updating the database of gas properties at http://properties.nist.gov/semiprop/.

■ We verified the accuracy of the primary flow meters by comparing the lower and upper ends of their ranges with other, overlapping NIST flow meters. Near both the lower end (0.3 sccm) and the upper end (1000 sccm) the agreement of 0.03 % was within the mutual uncertainty of the comparison.

■ We used the second-generation transfer standard and a prototype of the third-generation transfer standard to make a comparison of gas flows with a manufacturer of mass flow controllers.

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Low Concentration of Humidity Standards

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control — functions that are relevant to minimizing wafer misprocessing.

Customer Needs

Measurement needs and technical challenges for airborne molecular contamination (AMC) in semiconductor wafer processing spanning the next 15 years are given in the 2005 International Technology Roadmap for Semiconductors (ITRS) http://public.itrs.net/. A key measure of technological progress defined in the ITRS is yield enhancement (YE) which is the process of improving baseline yield for a given technology generation from R&D yield level to mature yield. AMC affects YE and constitutes a major impediment to wafer environment contamination control particularly for 300 mm wafer manufacturing processes. An industry expert, G. Dan Hutcheson of VLSI Research Inc., estimates that "a 1 % yield increase equates to $1M per day additional profits for a modern 300 mm fabrication line," *The Chip Insider*®. The ITRS also states "The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation ... to measure AMC at the part per trillion level … low cost, routine monitoring may be required as devices approach molecular dimensions." Target impurity levels relevant to wafer environmental contamination control for a number of AMC including H_2O, THC, CO_2 and other AMCs in various bulk gases are given in ITRS Table 115 and quantify the measurement needs in a variety of wafer production processes. Of these impurities, water vapor is one of the most ubiquitous and difficult to eliminate. Similarly, the Semiconductor Equipment Manufacturers International (SEMI) has standards describing the production and delivery and value assignment of ultra-high purity gases for semiconductor manufacturing http://downloads.semi.org/PUBS/SEMIPUBS.NSF/webstandardsgases. These standards illustrate the stringent requirements for gas purity measurements in semiconductor processes. We also note a new emphasis (beginning with the 2004 ITRS) on epitaxial processes that use gases as source materials, including SiGe and III-V semiconductor requirements for power amplifiers and extension of physical models to III-V semiconductors.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG) (see Fig. 1 and Fig. 2, next page), serves as the project cornerstone and is capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize water vapor measurement and generation systems at the research and development stage as well as commercial devices.

Technical Contacts:
J. T. Hodges
D. Ripple
K. Bertness

"The LFPG is the 'Gold' standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard."

Suhas Ketkar,
Air Products and Chemicals

Figure 1. NIST Low Frost-Point (humidity) Generator.

1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We have constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards. Experience with the system has revealed several limitations of traditional implementations, including deviations of the output from the equation generally used to predict the temperature dependence of the permeation rate.

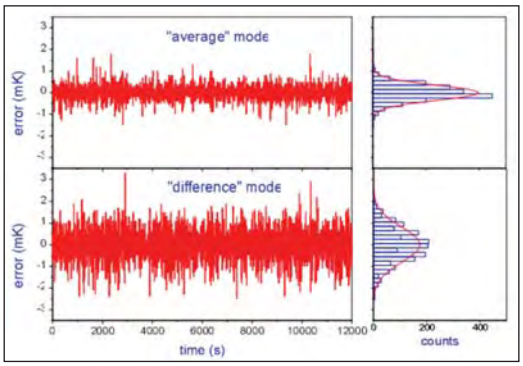

Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

DELIVERABLES:

- Complete uncertainty analysis of permeation-tube calibration system and measure temperature dependence of permeation tubes. 3Q 2006
- Complete documentation of system. 1Q 2007

2. In its standard mode of operation, the LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N_2 based on the minimum achievable temperature of the saturator. We have recently demonstrated a new strategy for pmol mol^{-1}-level humidity generation using dry-gas dilution of the water vapor/gas mixtures produced by the LFPG output stream and have validated the technique with a variety of self-consistency tests. Presently, we are establishing the uncertainties and optimal methodologies for this technique. Development of gas-handling manifolds with ultra-low adsorption/desorption of water will be a key focus of our work in the next year.

DELIVERABLES:

- Perform uncertainty analysis of dilution scheme. 3Q 2006
- Develop improved gas purification scheme for the dry-gas source. 4Q 2006
- Investigate attainable dry-drown rates using coated tubes for gas manifolds. 2Q 2007

4. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct vibrational absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line intensities. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10^{10} molecules cm^{-3}. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in

the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method (Fig. 3). CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequency-stabilized cavity ring-down spectroscopy (FS-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. Taking advantage of the high spectral resolution afforded by FS-CRDS, various line shape effects such as speed-dependent pressure-broadening and collisional narrowing of these transition line shapes by various media can now be quantified.

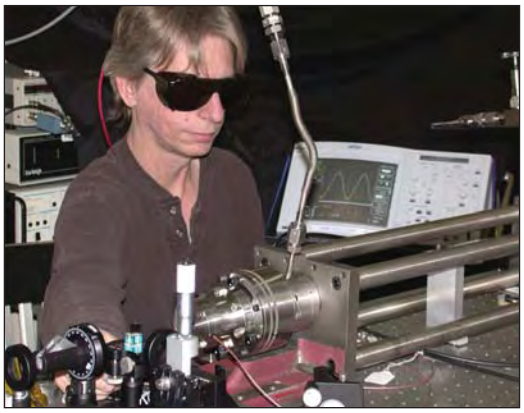

Figure 3. Frequency-stabilized CRDS system.

Using the existing FS-CRDS apparatus and a portable fiber-optics-based FS-CRDS system, we will make multiple independent measurements of H_2O transition line shapes and line intensities in the vicinity of 1380 nm. We will use transfer standards for humidity generation and measurement as well direct measurement of humidified gas samples delivered by the thermodynamic-based LFPG.

DELIVERABLES:

- Assemble and test portable FS-CRDS apparatus based on 1380 nm fiber-optic DFB laser for real-time continuous monitoring of LFPG output. 2Q 2006
- Link H_2O transition line intensities in the 1380 nm spectral region to LFPG for water vapor concentration measurements in the range 1 μmol mol^{-1} to 100 μmol mol^{-1} and measure line shape effects in N_2 and other gases. 4Q 2006
- Optimize the FS-CRDS apparatus for minimum water background, and compare FS-CRDS response to diluted gas streams from the LFPG, at concentrations of 10 nmol mol^{-1}. 1Q 2007

5. Moisture contamination is a serious problem in phosphine, arsine, silane, ammonia, and similar gases used in the epitaxial growth of high-purity semiconductor layers. Gas manufacturers have been lacking adequate instruments to refine their products, and end-users are unable to measure contamination in transferring gases from cylinder to process tool. The critical concentrations of the impurities are not well known; however, it is believed that >10 nmol mol^{-1} oxygen or water in most process gases is undesirable. Optical methods for measuring the moisture impurity concentrations combine high sensitivity and straight-forward traceability through the LFPG absorption line strength measurements. Researchers in the NIST Electronics and Electrical Engineering Laboratory have developed a CRDS system similar to the ones described in the previous sections but linked with a semiconductor crystal growth system to measure H_2O at very low concentrations in semiconductor source gases. The system was rebuilt in 2005-2006 to improve performance, to enable side-by-side tests with commercial instrumentation, and to allow greater flexibility in correlating gas purity with semiconductor growth results. We continue to measure the lineshape, absorption coefficients, and frequency of optical transitions for water, phosphine, arsine, and ammonia in the vicinity of 940 nm and 1380 nm. This information is critical to facilitate the use of high-sensitivity spectroscopy techniques in these gases. The laboratory is equipped to allow safe handling of toxic gases such as phosphine and arsine, enabling collaborative experiments with industry on direct measurements of moisture in those gases. The CRDS capability should ultimately lead to improvements in semiconductor source gas purity, which will allow crystal growers to choose less expensive growth conditions without sacrificing optical emission efficiency and yield in LEDs, semiconductor lasers, and photodetectors.

"[The] trend towards higher gas purities is expected to continue in the future as devices shrink and become more complex, so it is important for Matheson Tri-Gas to stay at the forefront of analytical technology developments. In this regard Matheson Tri-Gas's collaboration with NIST has been most beneficial. Use has been made of NIST's specialized capabilities for handling hazardous electronic specialty gases as well as expertise in the cavity ring-down spectroscopy technique. The work will allow Matheson to potentially offer new grades of phosphine in the future as required by the microelectronics market."

William J. Kroll,
Chairman and CEO,
Matheson Tri-Gas

DELIVERABLES:

- Publish arsine and phosphine spectra with pressure broadening coefficients for line at 943.082 nm. 1Q2008
- Test ammonia spectra in vicinity of 940 nm for possible overload with H_2O transition lines. 4Q 2007
- Correlate water impurity concentrations in ammonia and nitrogen with gallium nitride semiconductor growth results. 4Q 2008

ACCOMPLISHMENTS

■ We have constructed a permeation tube calibration facility (see Fig. 4). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and high-sensitivity quartz crystal microbalance (QCM). The water-containing permeation tubes to be calibrated are placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a precisely controlled stream of purified N_2.

Figure 4. New PTG calibration apparatus.

The diluent gas flow rate is adjusted so that the water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. As seen in Fig. 5, the calibrations derived from this system are repeatable to approximately 1 %, which is significantly superior to traditional gravimetric methods.

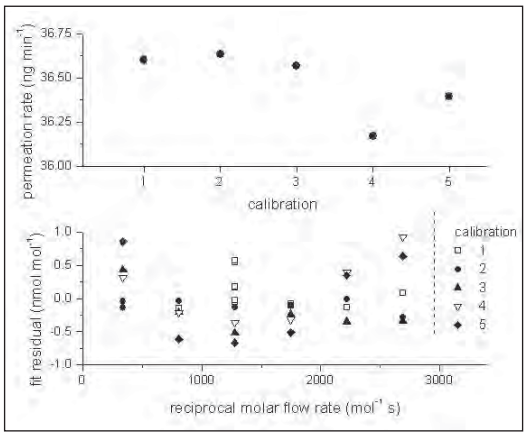

Figure 5. Calibration repeatability (top) and deviations from the fitting function (bottom) of a water-vapor permeation tube in the NIST Permeation Tube Calibration Facility.

■ A new strategy for pmol mol^{-1} (ppt)-level humidity generation has been successfully implemented. The approach, shown in Fig. 6, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above. At mole fractions below 10^{-9}, the uncertainty in water vapor mole fraction is dominated by water vapor background produced by adsorption/desorption of water on internal plumbing surfaces and by water vapor remaining in the diluent after purification. We performed three sets of measurements to validate the method. First, the same nominal output concentration was produced while varying both the water vapor concentration produced by the Low Frost-Point Generator and the level of flow dilution. Deviations from a constant concentration were measured. Second, the calculated water vapor mole fraction of the diluted generator output

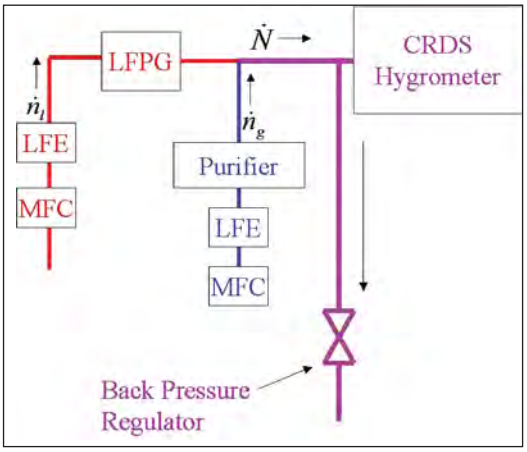

Figure 6. Dilution system for extending the LFPG operating range to pmol mol^{-1} levels.

was compared against the reading of a commercial hygrometer based on cavity ring-down spectroscopy. Third, we measured the water remaining in the diluent gas after purification at various flowrates both with and without an additional cryotrap. An approximate water background of 0.3×10^{-9} was inferred from the data, and the results were consistent within the combined uncertainty of the LFPG output and the water background.

■ The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may affect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results, shown in Fig. 7, indicate that the background contribution to H_2O from system components downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H_2O mole fraction are less than 0.1 nmol/mol.

■ We have successfully developed an FS-CRDS system with automated spectral scanning capability to measure the absorption coefficient of trace quantities of water vapor. In FY 2005 the FS-CRDS method was used to probe H_2O absorption transitions in the 935 nm spectral region, and a spectral resolution of 50 kHz and reproducibility better than 0.25 % were demonstrated. In conjunction with humidity standards for determination of water vapor concentration, these spectroscopic measurements yielded relative uncertainties in line intensities less than 0.5 %. Figure 8 shows measured spectra (symbols) and theoretical spectra (solid lines) for a pair of overlapping water vapor absorption transitions, each case corresponding to a given total gas pressure (with N_2 as the buffer gas). These results illustrate that the spectral resolution and linearity of the FS-CRDS method enable precise quantification of pressure broadening, collisional narrowing and asymmetries of the absorption line shape, thus minimizing systematic errors in the determination of number density and line intensity that typically arise from instrumental line broadening effects. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 940 nm.

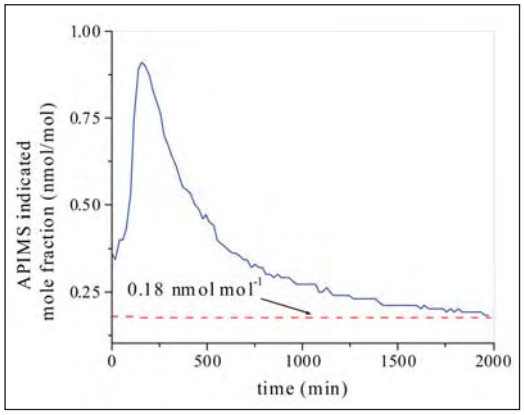

Figure 7. APIMS measurement of LFPG background H_2O concentration showing decay to steady state level.

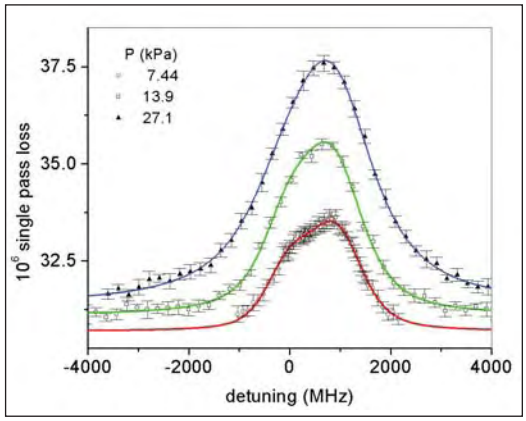

Figure 8. High-resolution FSSM-CRDS spectrum of a pair of pressure-broadened water vapor absorption transitions. Symbols are experimental points, and lines are Voigt fits to the measured profiles.

■ In collaboration with Matheson Tri-Gas and Tiger Optics, we demonstrated sensitivity of less than 10 nmol/mol for H_2O in phosphine using commercially available instrumentation, the first such measurement with this low sensitivity (see Fig. 9, next page). Additional experiments at NIST with arsine indicated that new wavelengths were needed to measure H_2O in arsine to similar sensitivities. We have also used the NIST hazardous gas CRDS system to measure water vapor concentrations in the toxic gases phosphine and arsine in the 940 nm spectral region. Testing of both arsine and phosphine in this spectral region indicated that the least overlap with host gas lines,

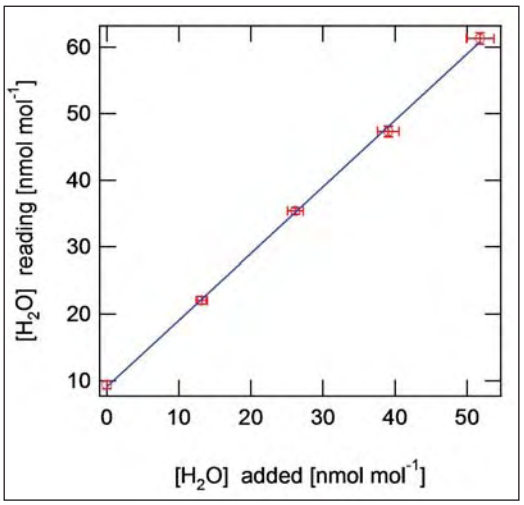

Figure 9. Response curve for commercial instrument measuring H_2O in phosphine with sensitivity of 1.3 nmol mol^{-1} .Zero offset of 9 nmol mol^{-1} is most likely from residual H_2O in phosphine.

and hence the highest sensitivity to water contamination, is present for the H_2O line at 943.082 nm. Future experiments will characterize this line for pressure broadening coefficients and ultimate sensitivity limits. Figure 10 shows a typical H_2O spectrum in arsine.

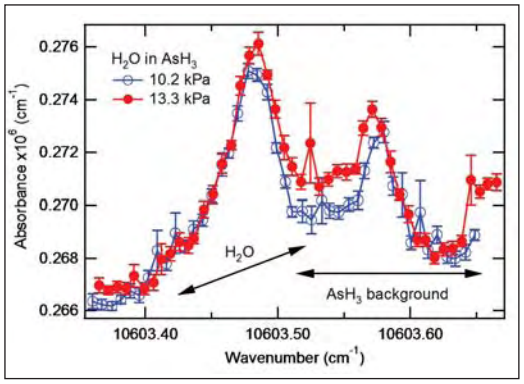

Figure 10. Absorbance spectra for H_2O in arsine near H_2O absorption line at 943.082 nm, showing feasibility of measuring H_2O concentrations on the order of 50 nmol mol^{-1}.

Collaborations

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

Matheson Tri-Gas, Mark Raynor, Jun Feng, and Hans Funke; CRDS measurements of trace moisture in phosphine.

Tiger Optics, Yu Chen; CRDS measurements of trace moisture in phosphine.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers and humidity generators for standards laboratories.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Tiger Optics, Calvin Krusen; evaluation of commercial CRDS technology.

Air Products and Chemicals Inc.; CRDS measurements of trace H_2O in corrosive process gases.

Recent Publications

D. Lisak and J.T. Hodges, "High-resolution cavity ring-down spectroscopy measurements of blended H_2O transitions," Appl. Phys. B (in press).

H. H. Funke, M.W. Raynor, K.A. Bertness, and Y. Chen, "Detection of Trace Water Vapor in High-Purity Phosphine using Cavity Ring-down Spectroscopy," Applied Spectroscopy, 61 (2007): p. 419-423.

G. E. Scace, *"Generating Parts per Trillion Levels of Water Vapor in Nitrogen,"* in Proc. 5th International Symposium on Humidity and Moisture, Rio de Janiero, 2006 (in press).

J.T. Hodges and G.E. Scace, "Developing advanced humidity standards to measure trace water vapor in specialty gases," Micro, **24**, 59 (2006).

D. Lisak, J.T. Hodges and R. Ciurylo *"Comparison of semi-classical line shape models to rovibrational H_2O spectra measured by frequency-stabilized cavity ring-down spectroscopy,"* Phys. Rev. A., 73, 012507 (2006).

V. Vorsa, S. Dheandhanoo, S. Ketkar, and J. T. Hodges, *"Quantitative absorption spectroscopy of residual water vapor in high purity gases: Pressure-broadening of the 1.39253 μm H_2O transition by N_2, HCl, HBr, Cl_2 and O_2,"* Appl. Optics, 44, 611-619 (2005).

J. T. Hodges and R. Ciurylo, *"Automated high-resolution frequency-stabilized cavity ring-down spectrometer,"* Rev. Sci. Instrum., 76, 023112 (2005).

J. G. Cormier, J.T. Hodges, and J.R. Drummond, *"Infrared water vapor continuum absorption at atmospheric temperatures,"* Jour. Chem. Phys., 122, 114309 (2005).

S. Y. Lehmann, K. A. Bertness, and J. T. Hodges, *"Optimal spectral region for real-time monitoring of sub-ppm levels of water in phosphine using cavity ring-down spectroscopy,"* Jour. of Crys. Growth, 261, 225-230 (2004).

J. T. Hodges, *"High-resolution cavity ring-down spectroscopy of $H_2{}^{16}O$ at 10687.36 cm^{-1},"* ISBN 1-55752-765-2, Laser Applications to Chemical and Environmental Analysis, Annapolis, MD, February 9-11 (2004).

J. T. Hodges, H. P. Layer, W. M. Miller, and G. E. Scace, *"Frequency-stabilized single-mode cavity ring-down apparatus for high-resolution absorption spectroscopy,"* Rev. Sci. Instrum. 75, 849-863 (2004).

Temperature Measurements and Standards for Semiconductor Processing

Goals

Our goal is to enable the improved accuracy of temperature measurements in semiconductor wafer processing as prescribed in the International Technology Roadmap for Semiconductor (ITRS).

Our project, initiated in 1997, has resulted in improved calibration wafer technology based on thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers for in-tool radiation thermometer (RT) calibration. We have also developed improved procedures for the calibration of lightpipe radiation thermometers (LPRT) and theoretical models for the relationship between the true wafer temperature and the indicated radiance temperature.

With the completion of this work, we are now focusing on: (1) collaborating with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements, (2) developing new resistance sensors for the range 300–600 °C, and (3) understanding measurement errors when calibration wafers are used in non-isothermal or high heat-flux environments.

Customer Needs

The measurement needs of the semiconductor manufacturing industry, as stated in the ITRS, continue to evolve. Examples of recently identified challenges are:

1. The temperature dependence of present day resists limits the available critical dimension in the Post-Exposure Bake (PEB) process. Improvements will require more stringent temperature measurement and control, or improved resists (Lithography, 2006 ITRS update, p. 7).

2. Fabrication of high-density, non-volatile memory is very sensitive to process temperature (Process Integration, Devices, and Structures, 2006 ITRS update, p. 2).

3. Accurate process models and control algorithms require characterization of the device thermal history during a variety of processing steps (Modeling and Simulation, 2005 ITRS, p. 2).

Current needs include better temperature measurement uncertainty in post exposure bake (PEB) processing of resists, in rapid thermal processing (RTP) of wafers including silicide formation in the temperature range of 300 °C to 600 °C, and in supporting development of instrumented calibration wafers for a variety of other processing steps. Understanding differences of temperature readings between different instrumented wafers is also a high priority.

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation.

Technical Strategy

Our research is focused on two projects that will enable the semiconductor industry to meet the roadmap requirements: (a) develop new, accurate sensors for the 300 °C to 600 °C range, where commercial sensors are inadequate, and (b) investigate effects on measurements of imperfect thermal environments with commercial instrumented-wafer technology.

Industry instrumentation and process developers have also asked us to develop calibrated thin-film resistors for wafer temperature measurement from 300 °C to 600 °C. These measurements are needed for more accurate control of the silicide anneal RTP. We have undertaken the development of precision platinum thin-film resistance thermometers directly on the silicon wafers to improve the uncertainty of *in situ* wafer temperature measurement at these temperatures. We have developed reliable methods for producing durable sensors with good performance. We are presently extending this work to explore rhodium and iridium thin-film thermometers.

DELIVERABLES:

- Publish paper on the fabrication methods, optimization, and attainable uncertainty of thin-film Pt resistor thermometers directly on Si wafers. 2Q 2007
- Explore feasibility of using iridium films as resistance sensors up to 600 °C. 2Q 2007
- Publish results for thin-film Rh and Ir resistor thermometers directly on Si wafers. 3Q 2008

Technical Contact:
D. Ripple

"On behalf of SensArray Corporation, I express our deep gratitude to NIST for significantly contributing to advances in semiconductor lithography process optimization and control. NIST has contributed to improved CD control in lithography processes through the establishment of measurement methods and standards for wafer thermal bake cycle dynamics in resist processing. This support is just in time, as the next area of focus for photo resist processing optimization is bake cycle dynamics. Your work will be of value to every advanced semiconductor factory."

Wayne Renken, President
SensArray Corp.

As a first step in determining the sensitivity of a sensor on an instrumented wafer to a non-isothermal environment, it is necessary to measure the thermal resistance between the sensor and the silicon substrate. We have developed an apparatus in which the temporal response of a sensor to a nearly instantaneous heat pulse is measured. Simple theoretical models can be fit to the data to ascertain the thermal resistance between sensor and wafer. This simple, non-destructive technique is envisioned as a useful quality-assurance tool for manufacturers of instrumented wafers. The same techniques may be extended to study the sensitivity of various sensor designs to high, non-isotropic heat fluxes.

DELIVERABLES:

- Paper on measuring the thermal response time of commercial embedded sensors. 2Q 2007
- Conduct experiments on sensitivity of sensors in instrumented wafers to non-isotropic heat flux. 4Q 2007

Instrumented calibration wafers are now being commercially developed for temperature measurements in a variety of unusual processing environments, such as plasma processing. Modeling of the interaction of the instrumented wafer with its thermal environment is needed to meet constraints on the allowable temperature of the calibration wafers and to assist in interpretation of data obtained with the wafers. We continue to supply instrumentation manufacturers with heat-transfer models that provide physical insight into the measurement errors and thermal management of the instrumented wafers.

DELIVERABLES: Assist manufacturers of instrumented wafers with heat transfer models in vicinity of sensors. 4Q 2007

Accomplishments

Development of Resistance Sensors for 300 °C to 600 °C Applications

■ We have explored the performance of platinum resistance thermometers deposited directly on oxide-coated silicon wafers. Our work has measured the effects of thickness and bond coat (Ti or Zr) of the Pt thin films. We have also measured the effect of ambient atmosphere (air or nitrogen) on the hysteresis and thermal coefficient of resistivity, α. The value of α was not sensitive to the annealing temperature or Ti bond-coat thickness, but did depend on the Pt thickness. Metallurgical analysis has been completed of sensors fabricated both at NIST and by commercial vendors. The optimized Pt sensors have uncertainties of 1 °C in the range 200 °C to 600 °C, limited by thermal hysteresis related to the thermal expansion mismatch between the platinum and the silicon substrate.

Transient Response of Temperature Sensors During the Post Exposure Bake Process

■ Recent studies on dynamic temperature profiling and lithographic performance modeling of the PEB process have demonstrated that the rate of heating and cooling may have an important influence on resist lithographic response. We conducted an experimental and analytical study to compare the transient response of commercial, embedded platinum resistance thermometer (PRT) sensors with surface-deposited TFTCs. A dual instrumented wafer for PEB evaluation is shown in Fig 1. Experiments were performed on a commercial module using wafers instrumented with calibrated type-E TFTCs and commercial PRTs.

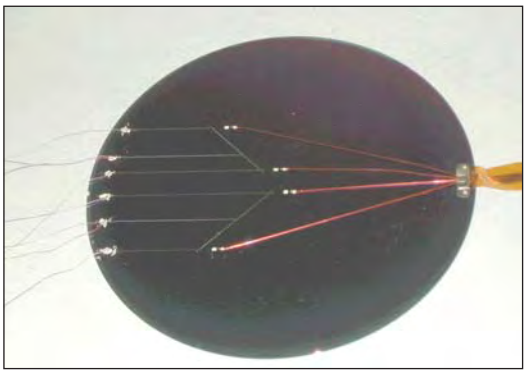

Figure 1. Wafer instrumented with PRTs and type-E thin-film thermocouples.

We measured the temperature of Si wafers in a commercial-type PEB module using both embedded PRTs and TFTCs through a typical thermal cycle from ambient, to 150 °C, and back to ambient. The transient response of the TFTCs led the PRT sensors, indicating a PRT lag (typically) of 2 °C on heating and up to 4 °C on cooling for several seconds. The wafer time constants for response were strongly affected by the air gap distance between the wafer and hot plate as expected. Thermal models were presented that showed estimates for heating time constants in good agreement with experimental data. Lithography simulation results were presented that showed the effects of transient and offset temperature profiles on CD variations.

Calibration of PRT Sensors for Instrumented Wafers

■ Calibration of PRTs that have been imbedded in instrumented wafers presents a challenge for the manufacturer: the wafers are much larger than commonly calibrated thermometers, the calibration process cannot contaminate wafers intended for use in a semiconductor-processing facility, and the uncertainty requirements for PEB applications are fairly demanding (standard uncertainty of approximately 0.01 °C). To validate the methods used in industry, a commercial instrumented wafer was calibrated both by NIST and by the manufacturer in the range 15 °C to 95 °C. The results were well within the stated manufacturing tolerance of the wafer and our expectations for the sensors used on the wafers.

Thermal Resistance of PRT Sensors for Instrumented Wafers

■ We have successfully developed a method for a relatively inexpensive measurement of the thermal resistance between resistance sensors and the underlying silicon substrate of instrumented calibration wafers. The thermal resistance is predominantly determined by the properties of the adhesives and potting compounds used to secure the sensor—a low thermal resistance is needed for the sensor to give a true reading of the substrate temperature independent of the thermal environment of the wafer. The method is nondestructive, and may be performed on used as well as new instrumented wafers to ensure that sensor attachment to the wafer substrate is acceptable for the thermal environment of use. Presently, we are simplifying the method and data analysis to allow ready adoption of the technique by industry.

Recent Publications

W. A. Kimes, K. G. Kreider, D. C. Ripple, and B. K. Tsai, *"In Situ* Calibration of Lightpipe Radiometers in Rapid Thermal Processing Between 300 °C and 700 °C," in *Proceedings of the 12th IEEE International Conference on Advanced Thermal Processing of Semiconductors*, RTP 2004, J. Gelpey, et al., eds., Portland, OR, p. 156-162, Sept. 2004.

B. K. Tsai, D. P. DeWitt, K. G. Kreider, and W. A. Kimes, "Emissivity Compensated Pyrometry for Specular Silicon Surfaces on the NIST RTP Testbed," in *Proceedings of the 12th IEEE International Conference on Advanced Thermal Processing of Semiconductors*, RTP 2004, J. Gelpey, et al., eds., Portland, OR, p. 167-172, Sept. 2004.

K. G. Kreider, D. P. DeWitt, J. B. Fowler, J. E. Proctor, W. A. Kimes, D. C. Ripple and B. K. Tsai, "Comparing the Transient Response of a Resistive-Type Sensor with a Thin-Film Thermocouple during the Post-Exposure Bake Process," *Proceedings of SPIE 29th International Symposium Microlithography*, Vol. 5378, 22-27, Santa Clara, CA, p. 81-92, Feb. 2004.

B. K. Tsai, D. P. DeWitt, E. A. Early, L. M. Hanssen, K. G. Kredier, B. J. Lee, and Z. M. Zhang, "Emissivity Standards for Improved Radiation Thermometry during Thermal Processing of Silicon Materials," *Proceedings of TEMPMEKO 200*4, Dubrovnik, Croatia, (to be published).

K. G. Kreider, D. H. Chen, D. P. DeWitt, W. A. Kimes, and B. K. Tsai, "Effects of Lightpipe Proximity on Si Wafer Temperature in Rapid Thermal Processing Tools," *Characterization and Metrology for ULSI Technology*, D. Seiler et al., eds., AIP, NY, pp. 200-204, March 2003.

K. G. Kreider, D. H. Chen, D. P. DeWitt, W. A. Kimes, and B. K. Tsai, "Lightpipe Proximity Effects on Si Wafer Temperature in Rapid Thermal Processing Tools," *Proceedings of the 11th IEEE International Conference on Advanced Thermal Processing - RTP 2003* Charleston, SC, 125-129, 2003.

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Physical Properties of Liquid Precursors

Technical Contact:
R. Berg

Goals

New materials used in gas phase processes will require new measurements and standards for their efficient delivery to the wafer surface. The National Institute of Standards and Technology (NIST) is supplementing its ongoing project to measure the thermophysical properties of semiconductor gases with a new effort to measure the relevant properties of liquid precursors. Vapor pressure is the most important property because it controls the behavior of vapor delivery devices. Therefore, the project's first goal is to produce accurate vapor pressure data for relevant liquid precursors from room temperature to as high as 200 °C. Such data will improve the modeling of chemical vapor deposition processes and the design and use of bubblers and other devices that deliver precursor vapors. Other goals are to characterize the thermal stability of liquid precursors and to devise a method for measuring vapor pressure that is suitably accurate yet more convenient than existing methods.

Customer Needs

Precursors for chemical vapor deposition are frequently liquid compounds that, until recently, were either rare or nonexistent. Their vapors are delivered to the process chamber either by direct injection (flash evaporation) or by bubbling a carrier gas through the liquid held in a "bubbler." Anecdotes from companies that either sell liquid precursors or sell the associated process equipment suggested an industrial need for improved property data of these specialty chemicals. Designers and users of mass flow controllers, bubblers, and other gas and liquid delivery devices could use such data to optimize the performance of those devices.

Vapor pressure determines the concentration of the precursor-carrier mixture produced by a bubbler, and it sets a lower limit on the wall temperature of the delivery line and process chamber. Although high vapor pressures are preferred, the acceptable range is wide. For example, when heated to 100 °C, the vapor pressure of the widely used liquid TEOS (tetraethyl orthosilicate) is P_V(100 °C) = 12 kPa. In contrast, a candidate precursor might be considered even if its vapor pressure were 100 times lower, say P_V(100 °C) = 0.1 kPa.

Other important properties include liquid viscosity and thermal stability. Viscosity can affect the performance of injection systems. Thermal stability is important because the precursor's decomposition rate may limit the process's upper operating temperature and thereby the vapor pressure.

Technical Strategy

NIST will identify and assess the quality of existing vapor pressure data of compounds such as Hf $[(CH_3)_2N]_4$ (acronym TDMAH). NIST will also fill gaps in the existing data by developing apparatus capable of accurate vapor pressure measurements. The resulting accurate databases will be provided to industry. NIST also will investigate alternate methods to measure vapor pressure.

DELIVERABLES: Develop apparatus to measure the vapor pressures of metal-organic precursors. 1Q 2007

The new apparatus uses pressure gauges that operate at the same temperature as the sample. This direct method was chosen over indirect methods that rely on, for example, thermogravimetric analysis or nuclear magnetic resonance. Challenges include achieving appropriate control of the sample temperature and avoiding systematic errors due to the presence of decomposition products, dissolved gases, and other impurities.

DELIVERABLES: Investigate alternate methods to measure vapor pressure. 2Q 2006

The initial investigation will include an estimate of the method's uncertainty and the identification of sources of systematic error. The leading candidate is speed-of-sound measurements of a mixture comprising the equilibrium vapor plus one atmosphere of an inert gas.

DELIVERABLES: Identify existing vapor pressure data. 3Q 2007

Existing data can be found in journal publications, the NIST Chemistry WebBook, NIST standard reference database 87, and other databases. The applicability of estimation techniques, such as group contribution methods, will be examined.

DELIVERABLES: Develop a system to measure the decomposition rate of metal-organic vapors. 4Q 2007

Some metal-organic precursors are known to decompose at temperatures below 200 °C. The new system will use a mass spectrometer to identify the decomposition products as well as contaminants present in the original sample.

Accomplishments

- NIST organized a SEMI workshop at Semicon West 2006 with the goal of soliciting directions for research on the physical properties of gases and liquid precursors. The 25 participants discussed four questions: (1) Which gases should be measured next? (2) Which liquid precursors should be measured? (3) What properties of liquid precursors are most important? (4) Are the data efficiently available? A report of the workshop is available at http://www.cstl.nist.gov/div836/836.06/.

- Although some precursors, such as TEOS, have been used for many years and have well known properties, others are poorly characterized because they were only recently created or identified. As an example of the resulting diversity, precursors used recently by researchers to make hafnium oxide have included hafnium nitrate, hafnium chloride, tetrakis-dimethylamino hafnium, and tetrakis-diethylamino hafnium. The diversity inherent in research and the proprietary concerns of precursor manufacturers are considerations in selecting a precursor to characterize. Several workshop participants suggested that NIST first measure the example precursors named by the SEMI task force on precursor specifications (Liquid Chemicals committee / Europe). The workshop report lists some of those examples, and a broader range of precursor examples is listed in the supplementary table of precursors attached to the ITRS. The workshop participants pointed out that, in addition to vapor pressure, other important properties include thermal stability, liquid viscosity, and materials compatibility.

- The vapor pressure apparatus, which consists of an oven, a vacuum system, a novel thermoelectric temperature control scheme, and appropriate instrumentation, was assembled. Measurements that compared the readings of pressure gauges inside the oven with other gauges outside the oven were taken between 20 °C and 200 °C. The resulting calibration surface will allow the readings of the hot gauges to be corrected to the required accuracy. Temperature stability within the requirement of 20 mK was demonstrated up to 200 °C. An independent thermometer demonstrated that temperature uncertainty was less than 20 mK up to the independent thermometer's limit of 100 °C.

- Requirements were identified for a 500 amu mass spectrometer, which must include a capillary sampling system suitable for metal-organic vapors at 200 °C.

- Gas flow measurement research at NIST in support of the semiconductor industry created a quartz capillary flow meter with a hydrodynamic model of unprecedented accuracy. A recent spin-off application is use of the model with a ratio viscometer that yielded values of unprecedented accuracy (< 0.1 %) for the viscosities of argon, hydrogen, methane, ethane, and xenon at temperatures from 200 K to 400 K. Another spin-off is a capillary flow meter that provides a 0.1 sccm reference gas flow for calibrating spinning rotor vacuum gauges.

Recent Publications

E. F. May, R. F. Berg, and M. R. Moldover, "Reference viscosities of H_2, CH_4, Ar and Xe at low densities," *International Journal of Thermophysics* (accepted 2007).

Analysis Tools and Techniques Program

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip approaches 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements. Those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling that allows us to bridge those areas where measurements can be done to those where knowledge is needed, but measurements cannot be done is critical. Significant improvements in tools capable of analyzing properties of defect particles in the sub-30 nm size are urgently needed. Global and local stress measurement techniques need to be developed.

Thin-Film X-Ray Metrology for Microelectronics

Technical Contacts:
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D. Windover

Goals

This multi-year collaborative effort between SEMATECH and NIST will provide the semiconductor community with the measurement methodology and calibration capability for accurate thin film characterization using X-ray reflectometry (XRR) and high-resolution X-ray diffraction (HRXRD).

Customer Needs

In recent years, the semiconductor industry has driven scientific advancement towards processing nanometer-scale material coatings with unprecedented uniformity in thickness, composition control, and unique electrical and mechanical properties. Nanotechnology represents the fastest growth area of industry in the United States today. Simultaneous to this rapid advance in thin film processing technologies, the X-ray diffraction user community and instrument manufacturers have collaboratively developed techniques such as XRR and HRXRD that permit the quantitative profiling of thin film characteristics, such as thickness, density profile, composition, roughness, and strain fields. With the XRR method in particular, parameter modeling by conventional methods can be an intractable problem, involving deconvolution of instrument response, data model theory, model selection, and model refinement/fitting, which has prevented the realization of the technique's potential in the characterization of nano-dimensional thin film structures. This effort addresses the mounting industry call for accuracy in thin film characterization (in particular for thickness, density, and roughness determination).

Technical Strategy

This fundamental XRR effort involves two parallel characterization projects being performed on identical, temporally stable, multilayer artifacts supplied by SEMATECH. The NIST project consists of in-house XRR and HRXRD characterization with International System of Units (SI) traceable measurement instrumentation and SI traceable, first principles data modeling including Bayesian analysis providing refinement of instrumental and model parameters as well as structural model selection. In parallel to this NIST measurement project, SEMATECH will measure or have measurements performed using commercial "in-line" XRR instrumentation and NIST will analyze these data with commercial software to study the limitations of commercial instrumentation and software modeling. Combining results from both studies will ultimately allow accuracy traceability and error estimation for commercial instrumentation. This work will also address theoretical XRR modeling limitations and compare software model refinement and model selection approaches. The multi-year collaboration will provide the community with total error budget estimates for a given XRR structural analysis approach and instrumentation. This work will take approximately three years to address the issues discussed [FY 05, 06, and 07]. The progress in FY05 included a comprehensive, first principles development of the XRR theory necessary for traceable modeling of data and a first round of measurements on artifacts by commercial and NIST instrumentation. FY06 work explored the application of an approximate Bayesian model selection method to compare the relative probability of different structural models for measured XRR data. Preliminary results with simulated XRR data have shown success in determining the initial structural model used to generate the simulated data. FY07 deliverables will include the development of an XRR prototype SRM to clarify instrument response issues and provide calibration of instrumentation at SEMATECH.

NIST XRR Study – The NIST standard approach for reducing uncertainty in a measurement technique involves the generation of a Standard Reference Material (SRM). Figure 1 (next page) shows the three parallel research aspects needed for the development of an XRR SRM: (1) the manufacture of a robust thin film calibration artifact with a high degree of temporal stability and contamination and/or oxidation resistance, (2) the development of SI traceable measurement instrumentation, and (3) the creation of an SI traceable, first principles data analysis approach. Figure 2 (next page) shows the current status of steps required to address these aspects for our XRR SRM project.

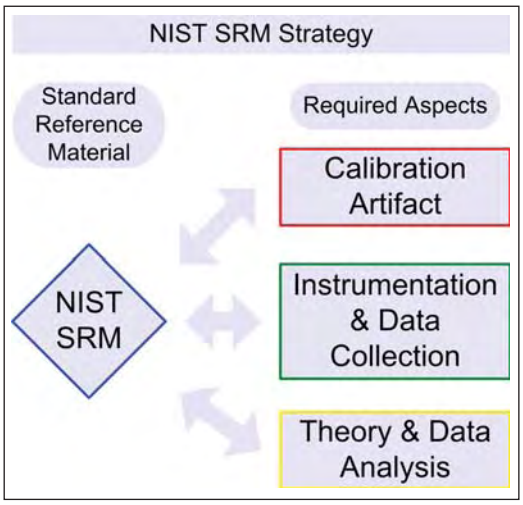

Figure 1. Aspects necessary for a NIST Standard Reference Material. All aspects are essential to provide structural parameter SI traceability.

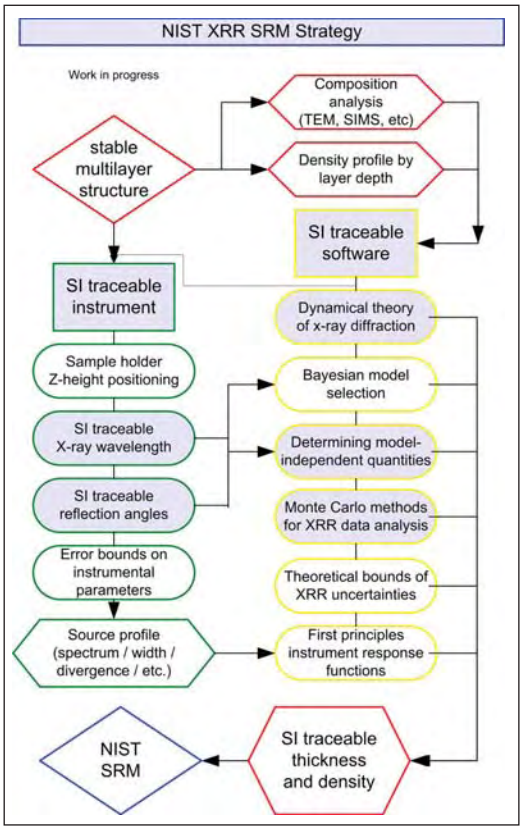

Figure 2. NIST XRR SRM strategy. This flowchart illustrates the key steps in the NIST XRR SRM development project. The light areas indicate work in progress. The outline colors indicate the appropriate aspect of the SRM development process for each step.

This collaborative effort with SEMATECH allows us to examine semiconductor industry relevant structures as potential candidates for an XRR calibration artifact. NIST has also engaged other national metrology institutes (NMIs) in an effort to assess the temporal stability of international NMI pre-standards. Both PTB of Germany and NMIJ/AIST of Japan have provided us with structures for comparative XRR analysis. This cooperative study will help gauge which thin films structures provide stable, well defined, refinement parameters suitable for SI traceable modeling.

NIST has applied considerable resources to developing SI traceable X-ray Reflectometry instrumentation. Over the past seven years, NIST has constructed the Ceramics Division Parallel Beam Diffractometer (CDPBD) for SI traceable measurements of Powder XRD, Epitaxial HRXRD, and thin-film XRR artifacts for the Standard Reference Materials (SRM) program (see Fig. 3). Over a similar timeframe, the Physics Laboratory developed the Physics Laboratory

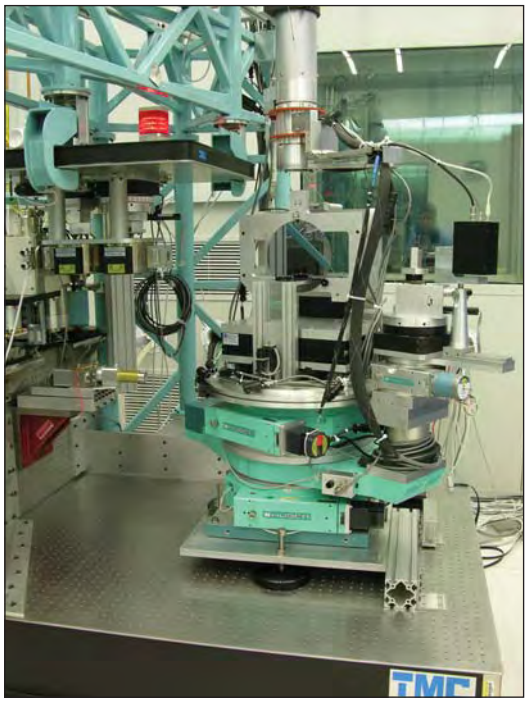

Figure 3. Ceramics Division Parallel Beam Diffractometer (CDPBD). Showing a rotating anode X-ray source (center left), monochromator for generating parallel/monochromatic X-rays (upper center), angle-encoded rotation stages for measuring diffraction angles (lower right) and receiving optics/detector (center right). In order to achieve accuracy in angle measurements and X-ray wavelength stability, numerous design features of varying complexity are present ranging from a "floating" platform holding the X-ray source to a hanging second rotation stage (top center) designed specifically to rotate the cables for the diffraction rotation stages.

X-Ray Reflectometer (PLXRR) specifically for XRR characterization of semiconductor thin-film artifacts. In FY07, we will be working with the Physics Laboratory to integrate the PLXRR into the XRR SRM effort allowing us cross-laboratory measurement comparison in our certification process to move the PLXRR into our temperature controlled laboratory space.

SI traceability in either lattice parameter (XRD) or film thickness (XRR), *d*, requires simultaneous traceability in X-ray wavelength, λ, and diffraction angle, θ, following Bragg's law of diffraction: $2d = n\lambda / \sin(\theta)$. The present NIST instrument development project involves addressing SI traceability aspects for both the diffraction angle and wavelength measurement on the CDPBD. Establishing SI traceability of the diffraction angle requires implementing optical encoding on the two rotation stages used to move the sample and detector. The optical encoder errors are then "mapped" using an external angle reference to generate SI traceability error bounds for each axis. The rotation stages presently have accuracy bounds of ± 2.0 μrads (± 0.4 arc seconds). Calibration experiments and collaboration with encoder manufacturers is currently under way to achieve an approximate one order of magnitude improvement in accuracy by year. Determining SI traceability in wavelength involves constructing a stable, well modeled optics assembly to convert angular and energy divergent radiation from an X-ray source into parallel, monochromatic radiation for use in diffraction. The CDPBD uses a monochromator with Si (220), 2/4-bounce channel-cut crystals to filter the direct source into a source of highly parallel, single energy X-rays. SI traceability in X-ray wavelength from our source will be performed using an SI traceable reference crystal (with measured relative standard uncertainty of 3 in 10^{-8}). The X-ray wavelength for our instrumentation currently has a relative standard uncertainty of ≈1 in 10^{-5} (FY06). The accuracy error bounds and instrument parameters from the wavelength and angle determination studies will provide an overall instrument response function which will be incorporated into NIST XRR profile modeling. The same instrumental parameters will establish guidelines for response profile modeling of commercial instrumentation.

NIST is currently developing first principles, SI traceable XRR software to analyze data and refine model and instrument response parameters. XRR analysis is essentially an "inverse problem" wherein we select input parameters for a "guessed" structural model. This model is then used to simulate data that is compared with measured data and "Goodness of Fit" parameters are determined. This process is repeated until a "best fit" or best "Goodness of Fit" is found and the "best fit" model parameters become the "refined" model parameters used to describe the real structure. Three major questions limit the effectiveness of this current XRR modeling approach: (1) How do we accurately simulate the data using a structural model? (2) How do we know which structural model describes the measured structure? (3) How do we accurately compare simulated and measured data? The NIST software development effort will attempt to answer each of these questions.

To address the model data simulation issue, we have developed XRR theory from Maxwell's equations explaining all approximations and constraints required for the XRR modeling method. This approach will in the future combine XRD, HRXRD and XRR in the same fundamental modeling theory and allow for SI traceability in derived refined parameters (FY08+). To address the question of model accuracy, we are implementing a Bayesian/Maximum Entropy analysis approach to determine the probability that a given structural model correctly describes a given data set. This model selection component is essential to determining the validity of initial structural assumptions in any XRR analysis. Addressing the third question is of considerable interest. Commercial refinement approaches attempt to optimize a solution through a "chi squared" or model/simulation minimization criterion (*e.g.*, genetic algorithms). This approach attains fast solution times most compatible with industrial need, at the loss of statistical data required for parameter uncertainty calculations. NIST, in collaboration with various companies is developing a statistical sampling based refinement using a Markov Chain Monte Carlo (MCMC) formalism to generate SI-traceable uncertainty estimations. The MCMC approach is necessary for developing formal Bayesian model selection methods (FY08+) to compliment existing Approximate Bayesian approach.

NIST/SEMATECH XRR Study – The NIST/SEMATECH project consists of measurements and analysis from commercial instrumentation to allow comparison and calibration transfer from NIST SI traceable measurements and analysis.

The NIST/SEMATECH project combines measurements with commercial "in-line" XRR instrumentation with complimentary compositional analysis results as feedback for comparison with NIST measurements performed in parallel on the same artifacts. The measurement and modeling work at NIST will provide SI traceable XRR measurements and parameter analysis for artifacts and potential candidate SRMs. The collaboration work with SEMATECH allows interface and calibration transfer between NIST SI traceable measurements and "in-line" instrumentation. NIST will then use results from NIST SI traceable measurements, SEMATECH commercial measurements and modeling, and NIST SI traceable XRR modeling, to quantify error bounds and overall error budgets on the accuracy and precision possible from commercial instrumentation and commercial modeling software.

Calibration and accuracy determination of commercial instrumentation are the primary goals of this collaboration. To achieve these goals, we need to develop accurate instrument response functions for commercial instrumentation being calibrated. The instrument response function for commercial instrumentation may be the dominant term in the overall accuracy budget for XRR measurements. To address instrumentation effects on accuracy, work must be performed with different commercial XRR system geometries to discover the mechanical alignment parameters that dominate the error budgets of each system. This will require cooperation from instrument vendors to provide the necessary information or provide detailed instrument response functions directly. The incorporation of instrument response parameters into NIST modeling will allow for comparison between traceable measurements at NIST and measurements on commercial instrumentation in the field. The NIST instrument response function information will be developed through our instrument traceability study discussed earlier. We can then combine specific instrument "corrections" to the accuracy error budget and use a calibration artifact such as a temporally stable thin film structure measured on the commercial instruments and at NIST to provide instrument calibration and stability monitoring (FY07+ deliverable).

Project Deliverables – The final project results available to SEMATECH will include XRR uncertainty estimations based on NIST XRR software and the calibration artifacts necessary for optimizing the performance of commercial "in-line" and laboratory XRR instruments. Theoretical uncertainty estimations provided by NIST software and simulated structural data will determine the limitations of XRR applicability for arbitrary multilayer systems on commercial XRR instrumentation (FY08+). Calibration artifacts measured on NIST SI traceable instrumentation will allow routine system monitoring, alignment calibration, and instrument response function comparisons to ensure commercial instrument precision and stability. These deliverables will dramatically improve the precision and accuracy of conventional XRR characterization of multilayer structures which exhibit well-established composition and uniformity (FY08+ deliverables).

DELIVERABLES:

- NIST analysis of SEMATECH measurements using new XRR modeling approaches. 2Q 2007
- Approximate Bayesian interface selection method. 2Q 2007
- NIST analysis of SEMATECH & NIST measurements (SRM prototype). 4Q 2007

Accomplishments

■ In FY05, the CDPBD moved to equipment space in the Advanced Measurements Laboratory (AML at NIST) which provides instrument temperature stability of ± 0.02 °C. Preliminary calibration of the angle measurement has been assessed for uncertainty determination (accuracy determination has been completed) and improvements using a new compensation approach (being developed through a joint National Metrology Laboratory effort with PTB) will be implemented (FY07). First principles XRR theory development with emphasis on justifying approximations present in commercial XRR software was completed (FY06) and a dynamical scattering based model has been implemented with Monte Carlo Markov Chain (MCMC) methods for structural parameter refinement and formal parameter uncertainty analysis (FY07+). A third/forth round of measurements on SEMATECH artifacts measured by both conventional and NIST traceable XRR systems will be completed this year (FY07).

■ *FY06/7 Technical transfer: Model Independent Structural Information* – In FY06/7, we measured structures from SEMATECH and calibration standards from PTB to test a new approach to discovering structural information using XRR. We try multiple structural models using commercial optimization refinement and compare the "best fits" of each model to discover any model independent, constant parameters across

the analysis set. In Fig. 4, we show this approach for 5 models of a Pulse Laser Deposition Pt layer on optical flat (provided by PTB). The figure shows a cross section mass density profile for the sample. Although the density of the surface layer is difficult to refine, the combined thickness of all the high density layers in every model attempted produces a constant, model independent structural parameter. This approach provides us with a way of locating what information the XRR method is most effective in measuring.

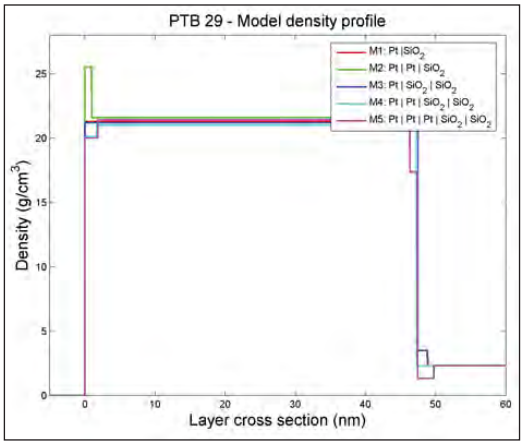

Figure 4. Mass Density Profile of Pt on optical flat. We show Model Independent Structural Information for a 50 nm Pt film on Optical flat. The optimized results from five different XRR models are shown. In each case, the total thickness of the Pt layer(s) is nearly identical providing us with information on the fundamental structure.

■ *FY07 Technical transfer: Preliminary MCMC XRR Modeling* – In FY07, we began testing a sampling based XRR refinement approach for developing SI-traceable uncertainty estimates for model parameters. Figure 5 shows the uncertainty range, or posterior probability density for the total thickness of the Pt on Optical Flat specimen analyzed above. We see a very narrow uncertainty which shows excellent agreement between sampling and optimization approaches to XRR analysis. Figure 6 shows another advantage of the MCMC method; we can test which parameters correlate with each other. In this case, a two-layer model for the same Pt on Optical Flat sample has multiple solution regions, which causes complicated uncertainty evaluations and may cause optimization methods to be trapped in false minima. More work is required on interpretation and implementation of the MCMC method.

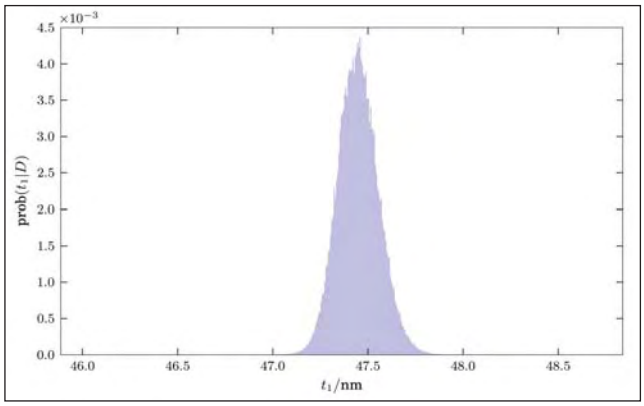

Figure 5. MCMC XRR posterior probability for Pt on optical flat. Showing the total Pt thickness uncertainty estimation or "posterior probability density" for the film used in Figure 4.

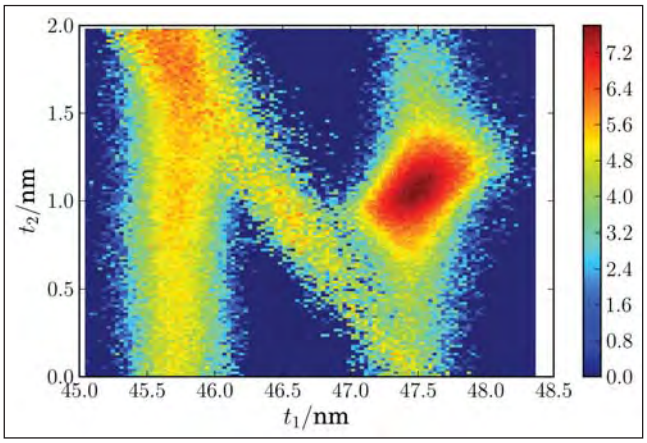

Figure 6. MCMC XRR 2-d histogram for Pt on optical flat. Shows the highly correlated and complex nature of XRR analysis. Here, a two-layer model is being applied to the same sample, and several possible solution regimes appear. The axes are thickness for t_1, the Pt layer and t_2, an interface layer. These multimode cases can often trap optimization based XRR analysis methods.

Collaborations

SEMATECH – PY Hung

PTB, Precision Metrology – Peter Thomsen-Schmidt

LETI – Emmanuel Nolot

NMIJ/AIST – Toshiyuki Fujimoto

Bede Scientific Inc. – Matthew Wormington

Bruker AXS – Assunta Vigliante & Arnt Kern

Coruscavi – David L Gil

Jordan Valley Semiconductors – Dileep Agnihotri

Panalytical – Martijn Fransen

Rigaku MSC – Joe Formica

Technos International – Meredith Beebe

Recent Publications and Presentations

D. Windover, D. L. Gil, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, *"X-ray reflectometry determination of structural information from atomic layer deposition nanometer-scale hafnium oxide thin films"* – oral presentation & conference proceedings at Spring 2007 Materials Research Society, San Francisco, CA (April 2007).

D. L. Gil, D. Windover, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, *"MCMC method for determining structural information using X-ray reflectometry"* – poster presentation at 2007 Frontiers of Characterization and Metrology for Nanoelectronics, Gaithersburg, MD (March 2007).

D. Windover, D. L. Gil, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, B. H. Lee, R. Jammy, A. Diebold, *"NIST method for determining model-independent structural information by X-ray reflectometry"* – poster presentation & conference proceedings at 2007 Frontiers of Characterization and Metrology for Nanoelectronics, Gaithersburg, MD (March 2007).

D. Windover, D. L. Gil, A. Henins, N. Armstrong, J. P. Cline, *"Prototype standards for X-ray reflectometry: an international perspective revisited"* – poster presentation at Spring International Centre for Diffraction Data, Newtown Square, PA, (March, 2007).

P. Xu, D. Windover, N. Armstrong, M. Wormington, A. Henins, J. P. Cline, *"Progress on the NIST High Resolution X-Ray Diffraction Standards"* – poster presentation at Denver X-Ray Conference, Denver, CO, (August, 2006).

D. Windover, N. Armstrong, A. Henins, J. P. Cline, *"NIST X-Ray Reflectometry Metrological Analysis Approach"* – poster presentation at Denver X-Ray Conference, Denver, CO, (August, 2006).

N. Armstrong, D. Windover, A. Henins, J. P. Cline, *"NIST X-Ray Metrology and SRM 1979 for nanocrystallite size broadening"* – invited presentation at CSIRO, Sydney, Australia (November 2005).

D. Windover, N. Armstrong, J. P. Cline, "Prototype Standards for X-Ray Reflectometry: an international perspective" – invited colloquia at PTB, Braunschweig, Germany (September 2005).

D. Windover, N. Armstrong, J. P. Cline, *"Prototype Standards for X-Ray Reflectometry: an international perspective"* – poster presentation at Denver X-Ray Conference, Denver, CO, (August, 2005).

N. Armstrong, J. P. Cline, J. Ritter, and J. Bonevich, *"SRM 1979: The NIST SRM for nanocrystallite size broadening"* – invited presentation at Denver X-Ray Conference, Denver, CO (August 2005).

D. Windover, N. Armstrong, J. P. Cline, P. Y. Hung, A. Diebold, *"Characterization of Atomic Layer Deposition using X-Ray Reflectometry"* – poster presentation & conference proceedings at 2005 International Conference on Characterization and Metrology for ULSI Technology, Dallas, TX (March 2005).

N. Armstrong, W. Kalceff, J. P. Cline, and J. Bonevich, *"A Bayesian/Maximum Entropy method for certification of a nanocrystallite-size NIST Standard Reference Material"* – Ch. 8 in Diffraction analysis of the microstructure of materials, pp. 187-227, Ed. P. Scardi and E.J. Mittemeijer, Springer-Verlag, Berlin, ISBN: 3-540-40519-4 (2004).

N. Armstrong and P. Lynch, *"Determining the dislocation contrast factor for X-ray line profile analysis"* – Ch. 10 in Diffraction analysis of the microstructure of materials, pp. 249-307, Ed. P. Scardi and E.J. Mittemeijer, Springer-Verlag, Berlin, ISBN: 3-540-40519-4 (2004).

N. Armstrong, W. Kalceff, J. P. Cline, J. Bonevich, *"Bayesian inference of nanoparticle-broadened X-ray line profiles"* – J. NIST Research, 108(5), pg 155-178 (2004).

N. Armstrong, M. Leoni, M. Scardi, *"Some concerns regarding the Wilkens' model for dislocation line broadening"* – invited presentation at Size-Strain 4: EPDIC 9, Prague, Czech Republic, (September 2004).

N. Armstrong, J. P. Cline, W. Kalceff, and A. Dowd, *"Status of the NIST Nanocrystalline Size SRM–1979"* – invited presentation at Size-Strain 4: EPDIC 9, Prague, Czech Republic (September 2004).

N. Armstrong, J. P. Cline, W. Kalceff, and A. Dowd, *"Bayesian characterization of nanoparticles from line profile"* – presentation at Denver X-Ray Conference, Denver, CO (August 2004).

N. Armstrong, W. Kalceff, J. P. Cline, J. Bonevich, P. A. Lynch, C. C. Tang, S. A. Thompson, *"X-ray diffraction characterization of nanoparticle size and shape distributions: – Application to bimodal distributions"* – Proceedings of the 28th Annual Condensed Matter & Material Meeting, Wagga, Australia (February 2004).

Electron Microscope Tomography of Electronic Materials

Technical Contacts:
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J. H. Scott

Goals

Enable the use of three-dimensional imaging for thick samples using commercial transmission electron microscopes (TEM) and scanning transmission electron microscopes (STEM). Typical samples include porous low-κ dielectrics, two-layer interconnect samples, and photonic band gap materials.

Customer Needs

The NTRS/ITRS has recognized the need for three-dimensional imaging of interconnects for several years. In this study, our principle objective is to determine the morphology of pores in low-κ dielectric material. Two aspects of the pore distribution are critical: (a) the largest pores may lead to failure of the dielectric (*e.g.*, short circuits), and (b) the connectivity of the pores is important to understand the transport of chemicals during the fabrication of the interconnect.

The potential solutions and major challenges for interconnect are discussed in the 2005 International Technology Roadmap for Semiconductors Update on pages 6 and 7 of the Interconnect Section. Three dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.

Technical Strategy

1. We have various theoretical capabilities in hand, including the ability to perform 3-D Monte Carlo simulations, the ability to perform tomographic reconstructions using an in-house 3-D Bayesian code for tomographic reconstruction which permits an arbitrary transmission-thickness relation, and a unique code which can determine the orientation of the tilt axis on the unit sphere from a tilt series of fiducial reference marks, Fig. 1.

2. In parallel, we will develop theoretical expertise for the effects of coherence on the samples, including understanding when Bragg diffraction is significant for tomography, and to develop simulations of coherent beam illumination, and strategies for beam rocking to reduce said coherence while preserving a sufficiently straight beam for standard tomographic algorithms.

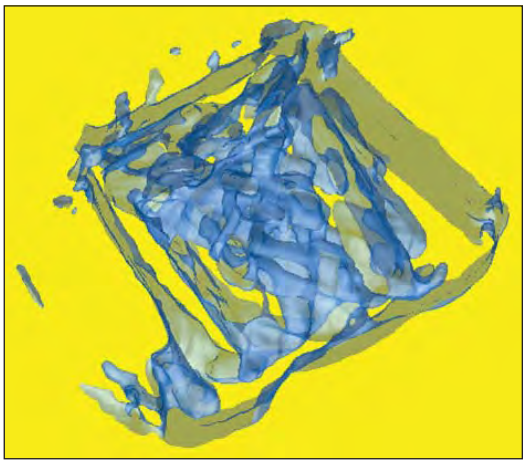

Figure 1. Tomographic reconstruction of a photonic band gap sample. An interconnecting network of material and void is present in the center of the figure. The bands on the outside are from the platinum overlayer added to protect the sample during preparation by a focused ion beam.

DELIVERABLES: Theoretical prediction of Energy Filtered Transmission Electron Microscopy (EFTEM) diffraction patterns of [111], [001], and [110] silicon slabs in the plasmon regime. 2Q 2007

Accomplishments

- Principle accomplishments include: creation of 3-D Bayesian code for tomographic reconstruction; completion of code for identification of rotation axis on the unit sphere and alignment for tomography; further development of 3-D Java Monte Carlo simulation of these complex geometries, allowing understanding of how observed X-ray intensities into composition, Fig. 2 (next page).

Collaborations

International Sematech, Brendan Foran, preparation of low-κ samples, electron microscopy.

Chris Soles and Hae-Jeong Lee, NIST, MSEL, Polymers Division; low-κ samples

Accurel, Inc. Preparation of focused ion beam sections from low-κ samples

Lucent Technologies, Shu Yang; preparation of photonic band gap material.

IBM, Frances Ross; preparation of Si:Au pillar sample.

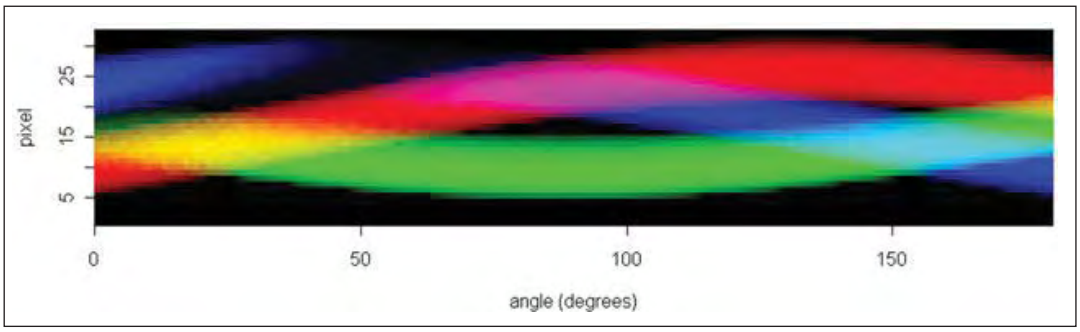

Figure 2. 3-D Java Monte Carlo simulation of interconnect phantoms and observed X-ray emission (Cu=red Al=blue SiO_2=green) from 0 degree to 180 degree tilt.

Recent Publications

Z. H. Levine and R. M. Dunstan, *"Synthetic Incoherence for Electron Microscopy,"* J. Opt. Soc. Am. A, in press (2007).

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Z. H. Levine, *"Synthetic Incoherence Via Scanned Gaussian Beams,"* J. Res. NIST 111, 429 (2006).

Z. H. Levine, A. J. Kearsley, and J. G. Hagedorn, *"Bayesian Tomography for Projections with and Arbitrary Transmission Function with Applications in Electron Microscopys,"* J. Res. NIST 111, 411 (2006).

I. M. Anderson, J. H. J. Scott, and Z. H. Levine, *"3-D Chemical Nanoscale Imaging Via EFTEM Spectral Imaging,"* Proc. Microscopy and Microanalysis (2006).

Z. H. Levine, *"An X-Ray Tomography Primer,"* Electronic Device Failure Analysis 7, 26 (2005).

Z. H. Levine, *"Theory of Bright-Field Scanning Transmission Electron Microscopy,"* J. Appl. Phys. 97, 033101 (2005).

Z. H. Levine, S. Grantham, D. J. Patterson, I. McNulty, I. C. Noyan, and T. M. Levin, *"Imaging material components of an integrated circuit interconnect,"* J. Appl. Phys. 95, 405 (2004).

Z. H. Levine, *"Tomography in the Multiple Scattering Regime of the Scanning Transmission Electron Microscope,"* Appl. Phys. Lett. 82, 3943 (2003).

Z. H. Levine, J. A. Gao, S. Neogi, T. M. Levin, J. H. Scott, and S. Grantham, *"Parallax measurements of an integrated circuit interconnect using a scanning transmission electron microscope,"* J. Appl. Phys. 93, 2193 (2003).

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

Technical Contacts:
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L. R. Vale

Goals

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES)) and an X-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator. We are presently simplifying this refrigerator to reduce system costs and increase the accessibility of microcalorimeter technology.

Customer Needs

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council (ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

"Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating peaks that overlap and cannot be resolved with current generation lithium-drifted-silicon EDS detectors. Such new X-ray detectors will allow resolution of slight chemical shifts in X-ray peaks providing chemical information such as local bonding environments. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. Beta site systems are now beingtested. These detectors can also be implemented in micro XRF systems, using either an electron beam or a micro focus X-ray beam as excitation source. Both are currently in beta phase. XPS (X-ray

photon electron spectroscopy) is also currently being developed as a means to determine thickness and composition of thin (up to 50 nm) films." **2006 International Technology Roadmap for Semiconductors**.

Technical Strategy

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Arrays of X-ray microcalorimeters for increased collection area and count rate have been demonstrated and their energy resolution is comparable to single sensors. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg, Maryland for collaborative use in studying problems of interest to the industry (Fig. 1), and to work with other partners in disseminating the technology.

Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

DELIVERABLES: Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Prepare for the eventual transfer to CSTL of an array microcalorimeter system. Collaborate with CSTL on using the microcalorimeter to study problems of interest to the semiconductor industry. 4Q 2007

2. The adiabatic demagnetization refrigerator that provides 0.1 K operating temperatures is a crucial part of a microcalorimeter system. To date, adiabatic demagnetization refrigerators have been precooled to 4 Kelvin with liquid nitrogen and helium. However, the use of liquid cryogens is an obstacle to potential microcalorimeter users. Consequently, it is desirable to precool the adiabatic demagnetization refrigerator with a push-button mechanical cryocooler whose only consumable is electricity.

DELIVERABLES: Design and build an adiabatic demagnetization refrigerator cooled by a pulse tube mechanical cryocooler. Understand and minimize the electrical and mechanical effects of the cryocooler on microcalorimeter and electron microscope operation. 2Q 2007

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive ^{3}He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES: Demonstrate the cooling of a X-ray microcalorimeter using a tunnel-junction refrigerator that could be coupled to a simple ^{3}He refrigerator. 3Q 2007

4. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated and been used to successfully read out eight microcalorimeters under X-ray illumination. Significant increases in multiplexer bandwidth and pixel-handling capacity are possible based on evolutionary design improvements.

DELIVERABLES: Demonstrate improved SQUID multiplexer and multiplexed operation of up to 128 microcalorimeters under X-ray illumination. Characterize multiplexer performance. 4Q 2007

Accomplishments

■ We designed and built an adiabatic demagnetization refrigerator that is precooled by a mechanical cryocooler. This simple and compact system is operated by the push of a button and requires no liquid cryogens. Because the cryocooler achieves a base temperature of 2.8 Kelvin, lower than that of liquid helium, the operating time of the demagnetization refrigerator below 0.1 K is significantly extended. In addition, we have demonstrated undegraded operation of a high resolution microcalorimeter in the electromagnetic environment of the cryocooler and its control electronics. We have also characterized the effects of the mechanical vibration of the cryocooler on other instruments such as a scanning electron microscope. Through a combination of vibration reduction measures, we have almost completely eliminated distortion of the microscope image due to the cryocooler. A photograph of the pulse tube cooled – demagnetization refrigerator undergoing vibration testing on an electron microscope is shown in Fig. 2.

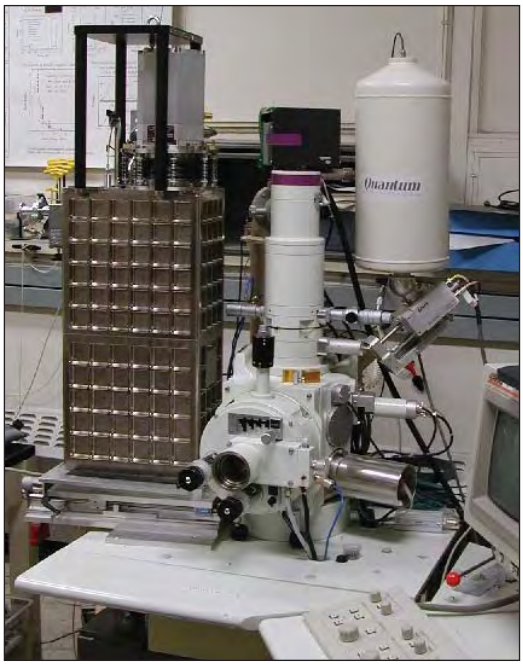

Figure 2. Cryogen-free adiabatic demagnetization refrigerator (left) undergoing vibration testing on a scanning electron microscope.

■ We developed a new generation of microcalorimeters that incorporate additional normal metal regions to suppress internal noise. In addition to being more stable and easier to bias, the energy resolution of these microcalorimeters is significantly improved. We demonstrated an energy resolution of 2.4 eV FWHM at 5.9 keV. We also hold the world record for energy resolution for an EDS X-ray detector of 2.0 eV at 1.5 keV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available.

■ We continue to support the microcalorimeter system installed on a CSTL scanning electron microscope in Gaithersburg, Maryland. As shown in Fig. 3, CSTL staff have demonstrated the ability of the microcalorimeter to do quantitative microanalysis.

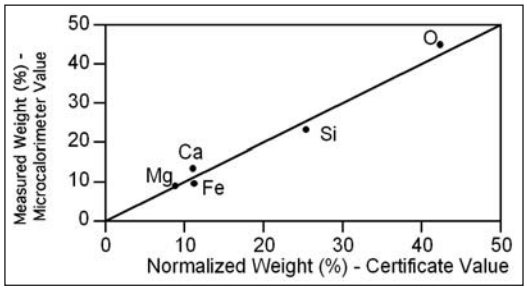

Figure 3. Comparison of elemental weights determined by microcalorimeter with certificate values for NIST K411 standard reference glass. The solid line corresponds to perfect agreement between microcalorimeter and certificate values (data courtesy of Terry Jach).

■ We demonstrated the ability to read out eight TES microcalorimeters in a single multiplexed amplifier channel with 3.8 eV FWHM energy resolution (Fig. 4). The detectors were fast, having a signal decay-time constant of about 150 microseconds. Combining this result with closed-form calculations and a new Monte-Carlo software package that performs a detailed simulation of our SQUID multiplexer, we can reliability predict the future performance of the multiplexer system. In particular, with only evolutionary improvements

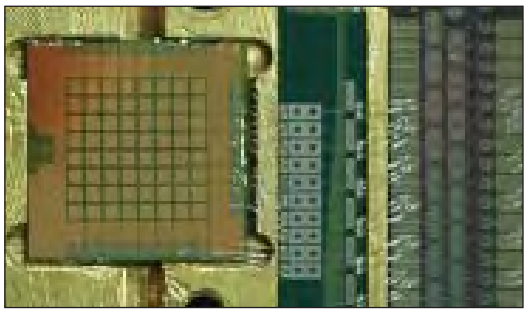

Figure 4. Photograph of an 8x8 array of microcalorimeters. Each microcalorimeter has a 1.5-μm-thick Bi absorber. The middle chip is a filter chip. The chip on the right is a SQUID multiplexer.

to the basic architecture, our time-division SQUID multiplexer will be able to readout 32 detectors per channel with 4 eV resolution or better. Planned improvements include increased open-loop system bandwidth, well-matched pulse rise and fall times, lower SQUID noise, and optimization of the coupling between microcalorimeters and SQUIDs. We have built a test apparatus to house and read out up to 128 microcalorimeter pixels and are preparing to demonstrate multiplexed operation of a 4 x 32 high-resolution microcalorimeter array (Fig. 5).

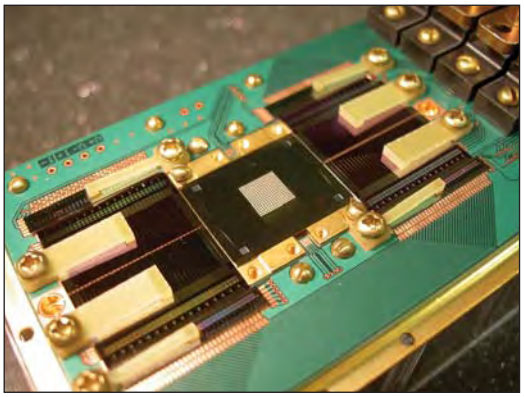

Figure 5. 128 pixel microcalorimeter array and multiplexed readout circuitry.

■ We have continued work on an on-chip solid-state refrigerator to cool X-ray microcalorimeters from 300 mK to 100 mK. If successful, this refrigerator could greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small and inexpensive ^{3}He systems coupled to the solid-state refrigerator. The device is a superconducting analog of a Peltier cooler. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. Recently, we demonstrated refrigerators able to cool bulk material as well as electrically separate pieces of thin-film electronics, such as a X-ray microcalorimeter (Fig. 6). The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. We recently cooled a X-ray microcalorimeter and demonstrated that no additional noise was introduced into the microcalorimeter output. This work has been featured twice on the cover of *Applied Physics Letters* and once on the cover of *Physics Today*.

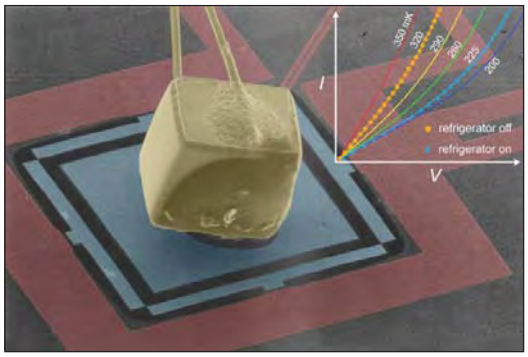

Figure 6. Colorized micrograph of solid-state refrigerator. A cube of germanium (yellow) located on a suspended, micromachined membrane is cooled by four pairs of normal-insulator-superconductor tunnel junctions. The ratio of the volumes of the germanium and the junctions is the same as the ratio of the volumes of the Statue of Liberty and an ordinary person (about 11 000). Macroscopic wires (at upper left) contact the germanium to measure its resistance; these are cooled as well.

■ We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 7). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the data collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.

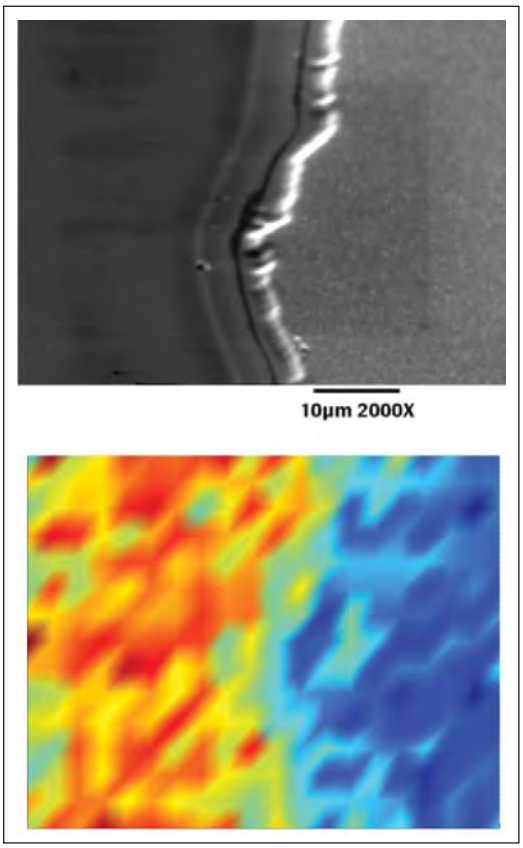

Figure 7. SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al Kα peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ~0.2 eV.

Collaborations

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

Recent Publications

K. D. Irwin, *"Seeing with Superconductors,"* Scientific American, Nov. (2006).

J. N. Ullom, J. A. Beall, W. B. Doriese, W. D. Duncan, L. Ferreira, G. C. Hilton, K. D. Irwin, G. C. O'Neil, C. D. Reintsema, L. R. Vale, B. L. Zink, *"Optimization of TES Microcalorimeters,"* Nuclear Instruments and Methods A 559, 422 (2006).

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Device Design and Characterization Program

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as Multi-Gate FETs (MUGFETs), fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube, spintronic, and phase change and molectronic device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. With all of these changes taking place, NIST has established the Center for Nanoscale Science and Technology (CNST), a multidisciplinary center composed of a research program and the Nanofab, a fee base, shared use user facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.

Device Characterization and Reliability

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M. Green

Goals

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced and emerging CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, physical models for wear-out, and methodologies to determine energy band diagrams and barrier heights for advanced gate dielectric stack systems..

A specific focus is to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (*i.e*, the gate dielectric, SiO_2, and the gate electrode, doped polycrystalline Si), which has served the industry for 35 years, must now be entirely replaced with one having a higher capacitance and lower power dissipation. Gate dielectrics having higher dielectric constants than SiO_2 will replace SiO_2, and metal electrodes will replace polycrystalline silicon. The enormous complexity of selecting the proper combinations of new gate dielectrics and gate metal electrodes can only be attacked using combinatorial materials methodologies. Therefore, we will be implementing this technology.

Customer Needs

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The continual decrease of the gate dielectric film thickness is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) with effective thickness values dropping to 1.0 nm or less by 2010.

Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (*e.g.*, Si_3N_4, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for high-κ/SiO_x stack dielectrics that exhibit polarity dependent defect generation and breakdown characteristics.

Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

Technical Strategy

There are two main focus areas for this project:

- Developing electrical and reliability characterization techniques for ultra-thin SiO_2/oxynitrides and high dielectric constant gate dielectrics.
- Develop combinatorial (fast, local) measurement techniques to measure appropriate electrical properties on gate stacks consisting of new gate dielectric and gate metal electrode materials.

The first focus area is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage, V_t, instability, defect generation rates, spatial and energetic defect profiles, and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics for a variety

of high-κ samples subject to different deposition and gate electrode processes. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization.

DELIVERABLES:

- Study Gate-induced leakage current (GIDL) in metal gate/high-κ gate dielectric MOSFETS. 2Q 2007
- Use ultra-fast current voltage measurements to study fast trapping kinetics in SiC/SiO_2 and metal gate/high-κ systems. 3Q 2007
- Use 1/f noise analysis and charge pumping to profile trap density in high-κ/SiO_2 stacks on Si and III-V substrates. 4Q 2007
- Conduct time-dependent dielectric breakdown study of SiO_2/SiC system. 4Q 2007
- Combinatorial analysis of the work functions as a function of composition in the Ta-Al-N/HfO_2 gate stack. 3Q 2007

Accomplishments

Characterization of Gate-Induced Drain Leakage Current in High-κ gate dielectric MOSFETs

■ Experiments conducted at NIST on transistors with hafium oxide (HfO_2) gate dielectrics have shown that although the gate leakage current is reduced, another leakage current associated with the drain of the device is significantly increased. The NIST research has shown that this leakage current known as gate-induced drain leakage (GIDL) appears to be due to trap-assisted tunneling by defects or traps existing in the HfO_2, Fig. 1. Special ultra-fast measurements were developed to separate leakage components associated with transient electron trapping from traps not associated with the defects responsible for the enhanced GIDL. The results of this work are significant in that they demonstrate how the thickness of the high-κ material affects the increased leakage current and suggests how the dielectric system can be engineered to mitigate it. Details of the study were presented at the 2006 IEEE International Electron Device Meeting in San Francisco CA.

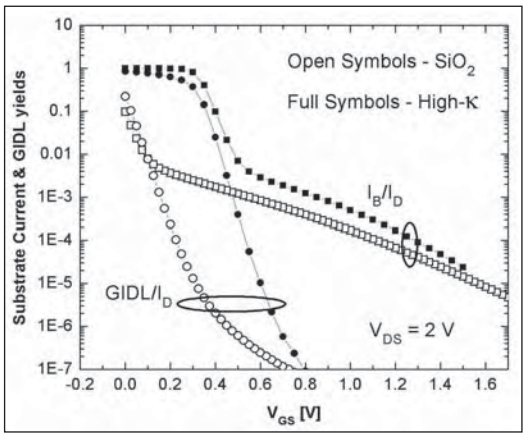

Figure 1. Substrate current yield (I_B/I_D) with GIDL current yield (I_{GIDL}/I_D) as a function of V_{GS} at V_{DS}=2 V of 0.35 μm gate length SiO_2 dielectric and high-κ dielectric n-MOSFETs.

Ultra-Fast Characterization of Transient Gate Oxide Trapping in SiC MOSFETs

■ MOSFET threshold voltage (V_{TH}) and drain current (I_D) instability in state-of-the-art 4H-SiC MOSFETs has been studied using conventional dc and fast *I-V* measurements, Fig. 2. This instability may be explained by trapping of channel electrons in the pre-existing traps at the SiC/SiO_2 interface and at the carbon-rich transition layer extending several nanometers into the oxide. These traps are located in the upper half of the energy band gap. Because of the fast transient behavior of the trapping and de-trapping processes, conventional dc measurement techniques underestimate the sever-

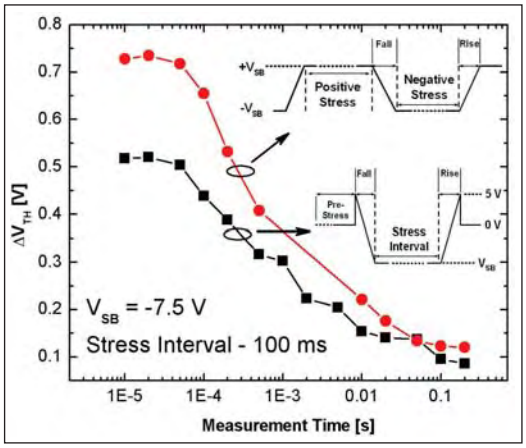

Figure 2. ΔV_{TH} of a SiC MOSFET measured as a function of time for the two different gate stress patterns. The stress bias (V_{SB}) was 7.5 V and stress interval was 100 ms. It is clear that measuring the threshold voltage using a dc sweep (~1 s measurement time) reveals only a fraction of the instability phenomenon.

ity of this phenomenon. Post oxidation annealing in NO passivates the oxide traps and as a result the transient trapping is almost eliminated. A physical model explaining the role of the nitrogen in passivating the oxide defects was proposed.

Spatial Probing of Traps in nMOSFET with ALD HfO_2/SiO_2 Stacks Using Low Frequency Noise Characteristics

■ Low frequency (LF) noise was studied in n-type Metal-Oxide-Semiconductor Field-Effect-Transistors (nMOSFETs) with various HfO_2 or interfacial layer (IL) thicknesses and is found to be dominated by 1/f noise in the frequency range $1\,Hz \leq f \leq 1.6\,kHz$. LF noise magnitude increases with HfO_2 thickness and decreases with IL SiO_2 thickness. Traps at the channel and dielectric interface do not contribute to the 1/f noise or cannot be resolved from thermal noise. The LF noise correlates well with the hysteresis or Vth instability observed during DC measurements. The volume trap density calculated from 1/f noise analysis is more than one order of magnitude higher in 7 nm HfO_2 than in 3 nm HfO_2 devices. Qualitative trap spatial profiles can be obtained from the LF spectra, and the stress induced redistribution of trap distribution can be determined.

Combinatorial Work Function Extraction of $Ta_{1-x}Al_xN_y$ Composition Spreads for the Advanced Gate Stack

■ We have systematically mapped the work functions (Φ_m) of $Al_xTa_{1-x}N_y$ composition spreads on HfO_2 using combinatorial methodology for the first time. A maximum of Al content (x = ~ 0.5) was confirmed to maintain sufficient conductivity for the metal gate application through the capacitance – voltage (C-V) measurement. The EOT maps suggested $Al_xTa_{1-x}N_y$ composition spreads thermally stable. Φ_m and Q_f were extrapolated using V_{fb} vs. EOT. The values of Φ_m, from 5.1 ~ 5.3 eV for the $Al_{0.05}Ta_{0.95}N_x$ alloys to ~ 4.9 eV for the $Al_{0.5}Ta_{0.5}N_x$ alloys, suggested a good replacement for polysilicon in the advanced gate stacks, Fig. 3. The fixed oxide charge density (Q_f) map confirmed the negative polarity induced the increase of Φ_m. Our results strongly suggested the potential of $Al_xTa_{1-x}N_y$ alloys ideal for the p-MOS application.

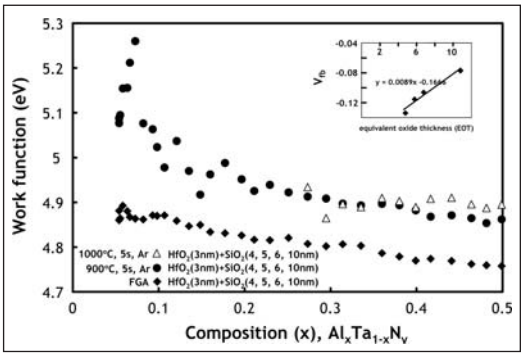

Figure 3. The extracted average work functions (Φ_m) as a function of Al content for the $Al_xTa_{1-x}N_y$ composition spread after FGA, 900°C, and 1000°C. Φ_m was extracted by extrapolating the line in the V_{fb} vs. EOT plot as shown in the inset. An abnormal peak was observed with x < 0.1 after 900° anneal.

Standards Committee Participation

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

Professional Committee Participation

- Technical Program Chair, 2006 IEEE International Reliability Physics Symposium (JSS)
- Technical Program Committee 2006 IEEE International Electron Device Meeting (JSS)
- Chairman of Dielectric Working Group, JEDEC JC14.2 Committee on WLR (JSS)
- Management Committee IEEE Integrated Reliability Workshop (JSS)
- Special Member of Graduate faculty, University of Maryland (JSS)
- Guest editor for Special Issue IEEE Tran. on Device and Materials Reliability (JSS)
- Editor, IEEE Transactions on Electron Devices. (JSS)

Collaborations

IBM, Alternative Gate Dielectrics

Micron, Boise, ID, Characterization of metal gate dielectric systems.

ARL, Characterization of defects and reliability of SiC gate dielectric systems.

GE, Reliability characterization of SiC gate dielectric systems.

Intel, Characterization of high-κ/InGaAs systems

Intel, metal gate/SiO_2 combinatorial systems

IMEC, Ta-Al-N/HfO_2 work functions, combinatorially

Lucent Technologies, Reliability Characterization of ultra-thin gate dielectrics.

SEMATECH Characterization of metal gate high-κ systems.

Rutgers University, Characterization of high-κ gate dielectrics

University of Maryland, College Park, ultrathin gate oxide reliability, combinatorial analysis of advanced gate stacks

U. Texas at Austin, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics

U. Texas at Dallas, high-κ gate dielectric systems..

Recent Talks/Publications

J. J. Kopanski, Book Chapter: "Scanning Capacitance Microscopy for Electrical Characterization of Semiconductors and Dielectrics in Scanning Probe Microscopy: Electrical and Electromechanical Phenomena at the Nanoscale, Springer-Verlag (in press).

M. L. Green, K.-S. Chang, S. DeGendt, T. Schram, J. Hattrick-Simpers, "Application of combinatorial methodologies for work function engineering of metal gate/high-κ advanced gate stacks," Microelectronics Eng., to be published 6/07.

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J. S. Suehle, "Reliability Challenges for Advanced Semiconductor Devices," SEMICON West, San Francisco Ca on July 10, 2006.

J. J. Kopanski, "Scanning Probe Microscopes for the Characterization of Electronic Materials and Devices," INTEL, Hillsboro, Oregon, January 9, 2006. Invited by Mike Gardner, Program Manager of Materials Research, External Programs.

J. J. Kopanski, M. Y. Afridi, S. Jeliazkov, H. Xiong, and T. Walker, "Limitations on the Accuracy and Spatial Resolution of Scanning Kelvin Force Microscopy for Work Function Measurements of Nanostructures," Seeing at the Nanoscale IV: An International Conference Exploring Nanostructure Imaging, Characterization & Modification using SPM & Related Techniques, p. 55, (University of Pennsylvania, Philadelphia, PA, July 17-20, 2006).

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H. D. Xiong, J. S. Suehle, "Spatial probing of traps in nMOSFET with ALD HfO2/SiO2 stacks using low frequency noise characteristics," Proceedings IEEE Integrated Reliability Workshop, Oct. 16-19, 2006.

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S. Sayan, N. V. Nguyen, and J. Ehrstein, J. J. Chambers, M. R. Visokay, M. A. Quevedo-Lopez, L. Colombo, D. Yoder, I. Levin, and D. A. Fischer, M. Paunescu, O. Celik, and E. Garfunkel, "Effect of nitrogen on band alignment in HfSiON gate dielectrics," Appl. Phys. Lett. 87, 212905 (2005). Publication Date: Nov 16, 2005.

Nanoelectronic Device Metrology

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Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable new nanotechnologies (such as Si-based quantum devices, molecular electronics, and carbon nanotubes (CNTs)) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices. Two related goals are the optimization of Si-based single-electron devices for one-electron logic, and the development of ultra-sensitive nanotransistor devices to observe charge reconfigurations in biological systems. Another targeted goal is to develop test structures and methods to measure the electrical properties of small ensembles of molecules reliably (see Fig. 1). A final targeted goal is to develop rapid identification and purification techniques for CNTs.

Customer Needs

Mainstream CMOS, which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is approaching fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) (http://public.itrs.net/) shows no known solutions in the short term for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Two promising beyond-CMOS technologies that each take a very different fabrication approach are molecular electronics and Si-based quantum electronic devices. Molecular electronics is based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

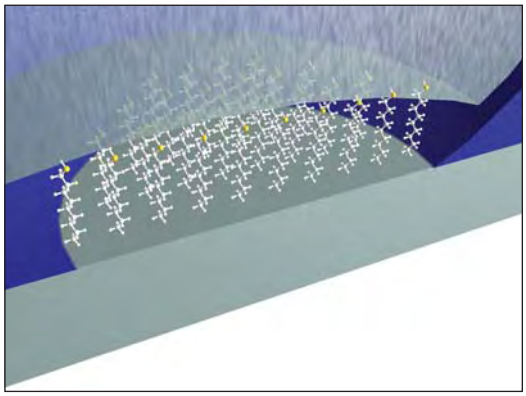

Figure 1. Schematic overview of a suspended Si_xN_y membrane nanopore-based molecular electronic test structure.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (*e.g.*, Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology. Finally, there is a large potential set of customers for ultra-sensitive charge electrometry of biological systems. Many diseases result from changes in protein structure or folding. We will investigate whether such changes can be elucidated through capacitive coupling to nearby nanotransistors.

Before carbon nanotubes (Fig. 2, next page) can fulfill their promise as ultrastrong fibers, electrical wires in molecular devices, or hydrogen storage components for fuel cells, better methods are needed for purifying and identifying raw nanotube materials. We are working towards this goal by developing simple methods of cleaning nanotubes by exposing them to carefully calibrated laser pulses.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Because these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

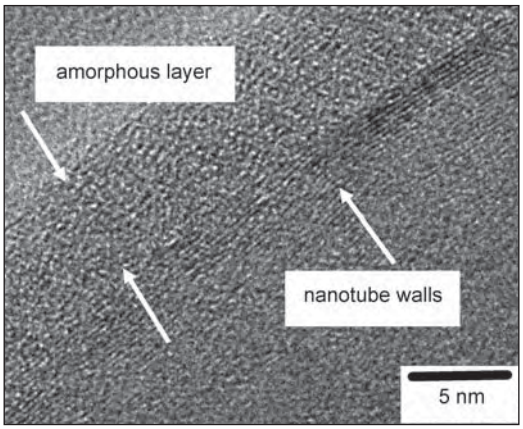

Figure 2. A high-resolution TEM micrograph showing a multi-walled carbon nanotube (MWNT) and the amorphous carbon layer on the outer surface. The parallel nanotube walls correspond to the walls of the MWNT. Photo courtesy of Gurpreet Singh of University of Colorado.

Technical Strategy

Develop the electrical and physical metrology of Si-based nanoelectronics. The focus is on the basic building blocks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

DELIVERABLES:

- Complete development of a simple single nanowire manipulating system (SNMS) to precisely transfer and align individual nanowires into test structures for electrical characterization; prepare and publish manuscript. 1Q 2007
- Experimentally characterize the noise properties of nanowire field effect transistor structures. Prepare and submit manuscript. 1Q 2007
- Design versatile Chemical Vapor Deposition (CVD) reactor capable of fabricating Si and SiGe alloy thin-films and nanostructures 3Q 2007; start assembling CVD system. 4Q 2007
- Complete development of fabrication process for tunable-barrier Si single-electron devices. 4Q 2007
- Assess Coulomb blockade behavior versus small dimensions of tunable-barrier devices – is it possible to achieve both high-temperature operation and reliable, low noise device performance? 2Q 2008

Develop robust molecular test structures (see Fig. 1, for example) in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models. One specific aspect of this research is to develop geometries and architectures that maximize flexibility and operating temperature of single-based single-electron devices.

Figure 3. Curt Richter loads a molecular electronic sample for electrical characterization. Copyright Robert Rathe.

DELIVERABLES:

- Present and publish the first unambiguous experimental evidence of the existence of molecular species in molecular magnetic tunnel junctions – devices that combine features of moletronics and spintronics. 1Q 2007
- Utilize backside FTIR-based technique to determine the chemical origin of the displacement of aliphatic molecules directly attached to silicon after metallization. Prepare and submit manuscript. 2Q 2007
- Systematically utilize IETS (inelastic electron tunneling spectroscopy) measurements to characterize molecules in silicon-base METS. Prepare and submit manuscript describing results. 3Q 2007
- Establish test-structures that enable the integration of molecular electronics with CMOS for the on-chip electrical characterization of hybrid Si/molecular electronic devices. 1Q 2008

Determine the ultra-sensitive charge electrometry capabilities of Si-nanotransistors through measuring the sensitivity and its relationship to device structure. A longer term strategy is to assess how the sensitivity is affected by biological structures in solution.

DELIVERABLES: Assess proof-of-principle by detection of DNA denaturation/renaturation transition using Si nanotransistor. 4Q 2007

Develop rapid, quantitative methods for identifying CNTs. Develop laser purification methods for CNTs.

DELIVERABLE: Determine the limitations and best possible accuracy of the Scanning Kelvin Force Microscopy (SKFM) measurement of surface potential when applied to nanowires. Apply SCM and SKPM to the measurement of the electrical properties of nanostructures, such as dopant concentration, work function, and surface state density. 4Q 2006

Develop laser processing methods for purifying CNTs.

DELIVERABLE: Demonstrate pulsed laser treatment of an individual Multiwall Carbon Nanotube (MWCNT) induced selective exfoliation of amorphous carbon contamination layers. 2Q 2007

ACCOMPLISHMENTS

■ *Spin-polarized Inelastic Electron Tunneling Spectroscopy of a Molecular Spintronic Device Investigated by EEEL Researchers*. Researchers in EEEL have fabricated and characterized molecular-monolayer magnetic tunnel devices. Molecular spintronic systems were fabricated by sandwiching a self-assembled monolayer of octanethiol between two ferromagnetic electrodes in a nanopore (Fig. 1), demonstrating that single molecules can be used as the ultimate building blocks for spintronic devices. By using inelastic electron tunneling spectroscopy (IETS), Wenyong Wang and Curt Richter have obtained the first unambiguous experimental evidence of the existence of molecular species in such magnetic tunnel junctions. Tunneling spectroscopy was also utilized to investigate the spin-polarized inelastic electron tunneling processes in the molecular devices. The measurements revealed that inelastic scattering due to molecular vibrations is likely the main cause of an observed junction magnetoresistance bias-dependence. These results illustrate that such inelastic scattering events must be accounted for when predicting the performance of practical molecular spintronic devices. Molecular electronic devices with spin-dependent tunneling transport behavior offer an innovative and extremely enticing direction towards spin electronics, from both fundamental and technological points of view. Due to the weak spin-orbital and hyperfine interactions in molecules, the spin coherence over time and distance could be preserved much longer in molecular nanosystems than in traditional semiconductors, which makes them a suitable playground for spin manipulations.

■ *Demonstration of homogeneity and uniformity in tunable-barrier Si single-electron devices*. A very common problem in semiconductor-based single-electron devices is the lack of homogeneity in general, and the lack of ability to fabricate devices with uniform device parameters in particular. In a recent study of four nominally identical devices, we showed the enhanced flexibility of these devices, and also the substantial improvement in uniformity. In particular, across these four devices we showed less than a 20 percent spread in a variety of gate capacitance values ranging from a few aF up to a few tens of aF.

■ *Lack of charge offset drift in tunable-barrier Si single-electron devices demonstrated*. We have demonstrated that the recently tested tunable-barrier single-electron devices (similar to the one in Fig. 4) exhibits the same advantage as the previously measured fixed barrier ones: there is no time-dependent drift in the operating characteristics of these devices, in contrast to metal-based single-electron devices. This demonstration allows us to continue working in the tunable-barrier devices, which have both advantages of superior flexibility and stability in time.

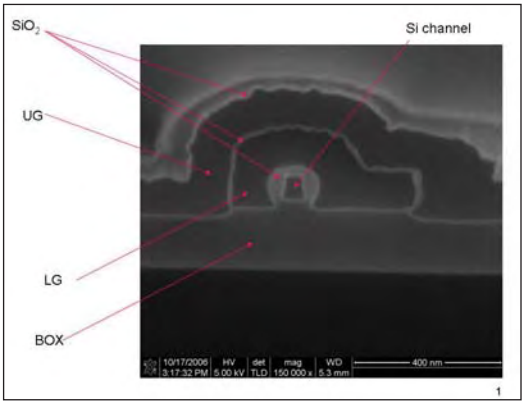

Figure 4. Cross-sectional micrograph of tunable-barrier devices fabricated by our project at the Cornell Nanofabrication Facility.

■ *Investigation of new "barrier" capacitance*. In the tunable-barrier devices, the barriers are produced electrostatically by small "finger" gates; these electrostatically-defined barriers, which are a few tens of nm in size, have not been previously investigated. As a first step in developing the metrology of characterizing such small barriers, we have shown that through Coulomb blockade measurements, it is possible to measure the "barrier" capacitance across these quantum tunneling regions. These capacitances (Fig. 5) range in value down to just a few aF, and such a measurement is only possible with Coulomb blockade studies. We are beginning a collaboration in order to compare our results with simulations; our hope is that this metrology study will allow validation of the simulation models.

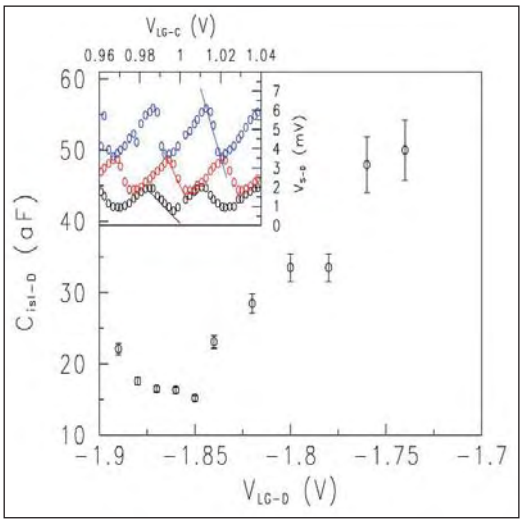

Figure 5. Measurement of "barrier" capacitance produced by electrostatic control from a single lower gate.

■ *System Developed to Precisely Align Single Nanowires*. A system (schematically shown in Fig. 6a) has been devised for manipulating and precisely positioning individual nanowires on semiconductor wafers. This technique, allows the fabrication of sophisticated test structures to explore the properties of nanowires, by using only optical microscopy and conventional photolithographic processing in lieu of advanced (and expensive) tools such as focused ion or electron beams. The smallest-diameter nanowires today are built in a "bottom-up" fashion, assembled atom-by-atom through a chemical growth process such as chemical vapor deposition. This is essentially a bulk process; it produces haystacks of jumbled nanowires of varying lengths and diameters. To control the positioning of nanowires, NIST engineers modified a standard probe station used to test individual components in microelectronic circuits. The station includes a high-resolution optical microscope and a system for precisely positioning work surfaces under a pair of customized titanium probes with tips less than 100 nanometers in diameter. In a two-step process, silicon nanowires suspended in a drop of water are deposited on a special staging wafer patterned with a grid of tiny posts, and dried. Resting on the tops of the posts, selected nanowires can be picked up by the two probe tips, which they cling to by static electricity. The test structure wafer is positioned under the probes, the nanowire is oriented by moving either the probe tips or the wafer, and then placed on the wafer in the desired position. The technique's fine level of control allows the precise placement of single nanowires to create elaborate structures for testing nanowire properties. This capability has been demonstrated by building a multiple-electrical-contact test structure for measuring the resistance of a nanowire independent of contact resistance (Fig. 6b), and a simple electromechanical "switch" suitable for measuring the flexibility of nanowires.

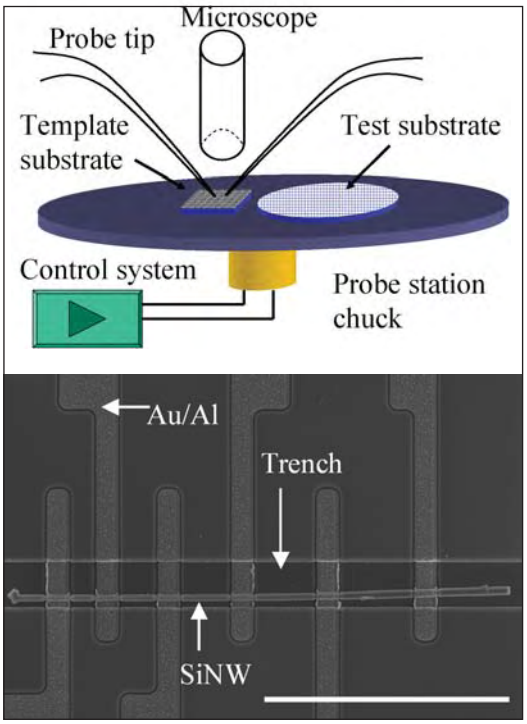

Figure 6. (a) Schematic of NIST single nanowire manipulation system. (b) Scanning electron microscope image shows a single silicon nanowire positioned in an etched trench using NIST's nanowire manipulation technique. The trench helps keep the nanowire in position during the fabrication of the rest of the test structure, which measures metal/nanowire contact resistance. The scale bar is 20 micrometers long.

■ *Interfaces in Molecular-Monolayer/SiO_2 Based Molecular Junctions Characterized*. The results of dc-current-voltage (IV) and ac-capacitance-voltage (CV) measurements have been correlated with vibrational spectroscopy of Au/monolayer/SiO_2/Si structures to establish an improved understanding of the interactions at the buried metal/monolayer and dielectric/silicon interfaces. Towards the goal of observing and characterizing electrical device behavior based upon intrinsic molecular effects, the role of test structures and their interfaces must be understood and eventually effectively controlled. A novel backside-incidence Fourier-transform infrared-spectroscopy technique previously developed by members of the NIST research team was used to characterize buried metal/molecule interface to probe the interaction of the top-metallization with the organic monolayers. Both the spectroscopic and electrical results indicate that Au has a minimal interaction with alkane monolayers deposited on SiO_2 via silane chemistry. An intriguing negative-differential-resistance and hysteresis is observed in the IV measurements of Au/alkane/SiO_2/Si devices. It is unlikely that this behavior is intrinsic to the simple alkane monolayers in these structures. Based on the results of extensive electrical characterization, the observed IV features are attributed to charge trapping and detrapping at both the alkane/SiO_2 and the Si/SiO_2 interfaces. These data illustrate that the dielectrics and other materials used when fabricating molecular devices must be made at the highest level of control to avoid impurities and defects which are likely to lead to spurious device behavior.

■ *Enhanced Inversion Mobility in Silicon Nanowire Field Effect Transistors Demonstrated*. Dr. Sang-Mo Koo and colleagues have demonstrated that silicon nanowire (SiNW) field effect transistors (FETs) fabricated by a standard 'top-down' approach exhibit substantially enhanced transport performance. A systematic study on the inversion electron transport properties of SiNWs with different channel geometries has shown that a SiNW device exhibits enhanced inversion channel current density: the extracted electron inversion mobility of the 20 nm width nanowire channel (1000 cm^2/Vs) is found to be two times higher than that of the reference MOSFET of large dimension (W >1 μm). The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. As the feature sizes of FETs are scaled downward, the semiconductor industry is working to meet the increasing challenges of nanoscale devices that are smaller and yet can be manufactured with minimal deviation from today's standard manufacturing processes. These results strongly suggest that lithographically fabricated SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics, preserving the basic silicon technology infrastructure upon which current industry relies.

■ *Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors*. We have shown that SiNWs with Schottky contacts can be used as enhancement-mode FETs with an excellent on/off current ratio. The process does not require any source and drain doping or silicide formation, thereby allowing for a simple process without thermal annealing. Silicon nanowire field-effect transistors (SiNWFETs) were fabricated with a highly simplified integration scheme to function as Schottky barrier transistors with excellent enhancement-mode characteristics and a high on/off current ratio ~10^7. SiNWFETs show significant improvement in the thermal emission leakage (~6×10^{-13} A/μm) compared to reference FETs with a larger channel width (~7×10^{-10} A/μm). The drain current level depends substantially on the contact metal work function as determined by examining devices with different source-/drain- contacts of Ti (≈4.33 eV) and Cr (≈4.50 eV). The different conduction mechanisms for accumulation- and inversion-mode operation were determined and confirmed by comparison with two-dimensional numerical simulation results. Schottky barrier FETs are of great interest in their own respect as an alternative to traditional doped source and drain device structure, because sub 100 nm range scaling encounters fundamental problems including high leakage current and parasitic resistance. Schottky barrier FETs have a number of advantages including simple and low-temperature processing, good suppression of short-channel effects, and the elimination of doping and subsequent activation steps. These features are particularly desirable for SiNW devices because they can circumvent difficult fabrication issues such as an accurate control of the doping type/level and the formation of reliable ohmic contacts.

■ *Two-dimensional Electrostatics to Enhance Channel Modulation in Dual-gated Silicon Nanowire Devices*. We have experimentally observed enhanced channel modulation in dual-gated silicon nanowire (SiNW) field-effect transistors (FETs). In this work, SiNW FETs were fabricated

using electron-beam lithography to investigate the electrostatic control of current in semiconductor nanowire devices. These novel top- and bottom-gated FETs are based upon simple top-down test structures that rely upon self-aligned Schottky-contacts to enable the electronic properties of SiNWs to be readily studied. Improved device performance is observed for the dual-gated SiNW FETs when compared to simultaneously fabricated large area control FETs. The SiNW devices (with widths down to approximately 60 nm) exhibit an on/off current ratio greater than 10^6, which is more than three orders of magnitude higher than that of control devices prepared simultaneously having a large channel width (5 μm). In addition, the top gate is found to suppress ambipolar conduction effectively, which is one of the factors limiting the use of nanotube or nanowire FETs for complimentary logic applications. Two-dimensional numerical simulations have confirmed an important physical insight illustrated by this work: due to the reduced dimensionality of SiNWs, electrostatic control is enhanced when compared to larger channel width devices.

■ *Comparison of charge offset drift in metal-based and Si-based SET transistors*. We have completed a study comparing the charge offset drift in metal-based and Si-based SET transistors. To date, there has been no reproducible way to eliminate the charge offset drift in metal-based SET devices, while Si-based devices have been characterized that exhibited minimal charge offset drift. The long-term charge offset behavior appears to be correlated with an observation in the short-term noise: two-level fluctuators in the Si-based devices are completely stable with respect to time, thermal cycling, etc.; in contrast, two-level fluctuators in the metal-based devices are notoriously "fragile." We have devised a model that comprehensively explains these results: in the metal-based devices, the defects that produce the drift are interacting strongly, as if they are in a glassy environment. These interactions are the underlying source of the long-term drift, and of the lack of stability in individual two-level fluctuators. This analysis leads us to suggest that a new fabrication process in which the metal films are deposited with low stress will improve the performance of the metal-based devices.

■ *Nano-gap capacitors*. We have succeeded in devising an assembly process and measurement scheme that allows us to measure the electrical breakdown in air with greater accuracy than previously reported. This new capability depends crucially on the ability to accurately measure the gap, which we accomplish by a combination of capacitance measurements and simulations of capacitance versus separation. We have shown the ability to measure over a range of separations between 0.3 microns and 50 microns. These measurements of electrical breakdown in air at small separations are of increasing importance to the MEMS field.

We have also investigated the standard theory for the breakdown at small separations (below about 5 microns). In this regime, the standard theory uses Fowler-Nordheim tunneling in vacuum, along with a surface roughness-induced field enhancement; this field enhancement is typically a factor of about 100. By combining electrical breakdown measurements with AFM measurements of surface roughness, we have for the first time been able to quantitatively test this theory. We find that the roughness in our smooth Au films is much smaller than necessary for the standard theory to be correct. We conclude that the standard theory cannot explain our experiments, and by extension is suspect in most of the measurements done to date.

■ *Joint NIST/HP Research Progresses Toward Critical Molecular Electronics Measurements*. Research at the NEDM and Hewlett Packard (HP) Laboratories is progressing toward reliable methods for measuring the electrical behavior of molecular electronic devices, an emerging nanotechnology eyed for future integrated circuits. By using a crossbar test structure consisting of a molecular monolayer sandwiched between a series of perpendicular metal wires, collaborators at separate facilities recorded nearly identical electrical measurements. This step, along with others taken to eliminate potential sources of error, ensures that the measured behavior is directly attributable to the device and not the experimental setup. Electrical (current-voltage, or IV) measurements of crossbar devices containing eicosanoic acid exhibit a controllable, two-state switching behavior that is due to the presence of the molecular layer. However, the molecular monolayer is not the sole cause. Rather, the switch-like behavior most likely arises from the interaction of the molecules with the electrodes. This example illustrates that the properties of molecular electronic devices are often determined not by the molecule alone, but by the entire device that consists of both the molecules and the attachment electrodes. This two-state behavior was independently measured in two separate laboratories, indicating that it

is not a measurement artifact and illustrating that these devices are robust enough to ship via conventional methods and remain active. In addition to IV measurements, what well may be the first capacitance-voltage (CV) measurements of molecular monolayer-based devices were taken at NIST. These CV curves also show two-state behavior.

■ *Novel approach to investigate buried metal-organic interfaces for molecular electronics*. We have developed and used a novel approach to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique developed at NIST takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of a technologically relevant metal electrode. The samples as prepared encapsulate the organic layer in exactly the same manner as fully fabricated devices. IR and electrical samples were fabricated simultaneously, allowing direct comparison of the spectroscopic results with electrical device performance. Two different chemical processes were utilized to attach nm-thick alkane films to the Si substrates: a conventional silanization process for films on thin oxides and a novel process previously optimized at NIST for direct attachment to silicon. Molecules on silicon are of interest as active electronic layers and for surface engineering. Monolayers bound directly to silicon are expected to have less interfacial capacitance than those on oxides, be more amenable to further processing, and be resistant to degradation die to the nature of the strong covalent bond. Results were presented at the 7th International Molecular Electronics conference and published.

■ *New reactor for growing doped Si, Ge, and SiGe nanowire heterostructures*. A. Davydov and S. Krylyuk have designed a versatile CVD system for fabricating Si and SiGe alloy thin-films and nanostructures. The system includes hot-wall horizontal reactor with 4 independently controlled temperature zones and automated gas delivery system. The reactor is designed to be capable of growing Si and SiGe alloys on round or square 1" substrates at atmospheric or reduced (down to 1.3 Pascals (10 mtorr)) pressure. The system design utilizes SiH_4 gas as a Si source, solid Ge or germanium halides as Ge-sources and solid sources for p (boron-based) and n-type (phosphorus based) doping. To achieve rapid growth process interruption/restoration without exposing system to the outside atmosphere (*e.g.*, for realization of abrupt interfaces in fabricated heterostructures, such as p/n junctions in Si, Ge, and SiGe multi-layers), the reactor design includes adjacent "preservation zone" to be maintained at the growth temperature and pressure in inert atmosphere. All parts of the system have been manufactured and/or purchased and the assembly of the system is in progress. The system is planned to be operational for growing Si nanowires and thin films in 4Q of 2007. Capabilities for growing Ge and SiGe using GeH_4 gas as well as utilizing gaseous sources for n- and p-doping can be added as necessary in FY 2008 (funding permitted). The new CVD system will enhance the NEDM's capability of fabricating Si and SiGe nanostructures with desired structural and electronic properties for nano-metrology needs.

■ *Laser induced exfoliation of amorphous carbon layer on an individual multi-walled CNT (MWCNT)*. By applying a pulsed laser treatment of an individual MWCNT, we selectively induced exfoliation of the amorphous carbon contamination layer. The MWCNT was exposed to a 248 nm excimer laser. After the treatment, transmission electron microscopy (TEM) images (Fig. 7, next page) show that the amorphous layer has expanded and separated from the crystalline MWCNT walls. This interesting observation has implications for laser cleaning and possible thinning of MWCNTs to reduce the radial dimensions.

■ *Rapid and inexpensive identification of bulk carbon nanotubes*. We estimated the volume fraction of metallic and semiconducting carbon single-wall nanotubes (SWNTs) for purified laser vaporization SWNTs, from an effective medium approximation and the measured spectral responsivity of a $LiTaO_3$ pyroelectric detector covered with SWNT "bucky" paper. The detector spectral responsivity from 600 to 2000 nm was proportional to the expected absorption coefficient of the SWNTs, and variations near 700, 950, and 1750 nm correlated with characteristic interband transitions and proportions of SWNTs consistent with 20 % metal and 80 % semiconductor materials.

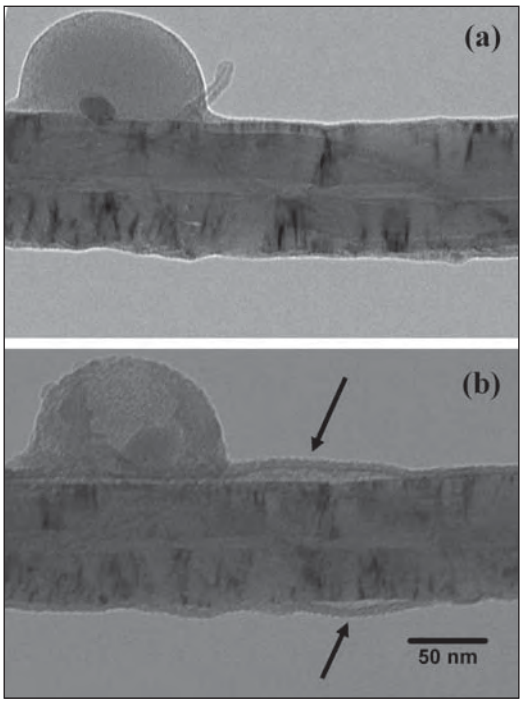

Figure 7. TEM micrographs showing the same region on the MWNT (a) immediately after welding to the TEM grid and (b) after laser treatment. The hemispherical protrusion was an intrinsic feature used to repeatedly locate the same region after treatment. The arrows indicate areas were the amorphous carbon layer separated from the MWNT. Photo courtesy of Gurpreet Singh of University of Colorado.

FY Outputs

Collaborations

Hewlett-Packard, R. Stanley Williams et al., Interface properties of molecular electronic test structures

NTT, Akira Fujiwara, Si-nanowire metrology

National Renewable Energy Laboratory, A. C. Dillon, optical properties of CNT materials.

NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., NIST Molecular Electronics Team

Purdue University, Prof. David Janes, Hybrid Si-molecular devices and test structures

University of Notre Dame, Prof. Greg Snider, Si single-electron device fabrication

Virginia Polytechnic Institute and State University, R. L. Mahajan, laser treatments of CNT materials.

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures

Recent Publications

Li, Q., Zhu, X., Xiong, H. D., Koo, S.-M., Ioannou, D. E., Kopanski, J. J., Suehle, J. S., Richter, C. A., *"Silicon nanowire on oxide/nitride/oxide for memory application."* Nanotechnology 18, 235204 (May 2007).

Li, Q. L., Koo, S. M., Richter, C. A., Edelstein, M. D., Bonevich, J. E., Kopanski, J. J., Suehle, J. S., Vogel, E. M., *"Precise alignment of single nanowires and fabrication of nanoelectromechanical switch and other test structures."* IEEE Transactions on Nanotechnology 6, (2), 256-262, (MARCH 2007).

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Fujiwara, A. F, I. Hiroshi, K. Yamazaki, H. Namatsu, Y. Takahashi, N. M. Zimmerman, S. B. Martin, *"Single electron tunnelling transistor with tunable barriers using silicon nanowire MOSFET,"* Appl. Phys. Lett. 88, 053121 (30-JAN-2006).

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Power Semiconductor Device Metrology

Technical Contact:
A. Hefner

Goals

The goal of the project is to develop electrical and thermal measurement methods, measurement equipment, and theoretical models in support of the development and application of advanced power semiconductor devices.

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient power generation, transmission and distribution. Rapid technical advances are occurring in the development of new power semiconductor materials, fabrication processes, and device designs to address these needs. With the introduction of these new materials and designs come new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC material and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the commercialization of SiC power Schottky diode products in the 400 V to 1200 V range and to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize industry and military power generation, transmission, and distribution by extending the use of switch-mode power conversion technology, with its superior efficiency and control capability, to high voltage applications.

"In 2002, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: "his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in … more efficient/compact power supplies, and higher efficiency power distribution/transmission systems."

Several industry and government programs are currently under way to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is to develop half-bridge power semiconductor modules with 15 kV, 110 A, 20 kHz switching capability. The recently awarded WBST-HPE Phase 3 effort (http://www.darpa.mil/baa/baa06-30.html) anticipates that this semiconductor technology will enable the HV-HF switching required for a Solid State Power Substation (SSPS). The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements, and the Department of Energy has identified HV-HF power devices as an enabling technology for alternative energy sources and energy storage systems, as well as transmission and distribution systems.

Technical Strategy

The strategy of the NIST project is to support the measurement infrastructure of the power semiconductor and energy systems technology industries by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of power semiconductor devices. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters. The NIST project also establishes the theoretical foundation required for development of advanced power semiconductor devices, and develops circuit simulation models for emerging power semiconductor devices to aid in the rapid adoption and effective utilization of new technologies. NIST is taking a lead role in developing the device metrology and performance metrics necessary for industry and government HV-HF semiconductor device development efforts and in the evaluation of potential future impacts power semiconductor technologies requiring future investment.

Metrology High-Voltage High-Frequency Switching Devices

The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements. NIST has recently developed unique world-class laboratory facilities for characterization of HV-HF SiC power switching devices including: a) 25 kV variable-pulse-width curve tracer, b) 15 kV 100 A 50 ns inductive and resistive load switching tester, c) 4 kV, 50 A, 10 ns diode reverse recovery tester, d) pulsed and multi-channel long term diode forward current stress and monitoring systems, e) high-speed high-power Temperature Sensitive Parameter module package measurement system, and f) rapid thermal cycling/shock module package stress system.

Support Programs to Develop HV-HF Semiconductor Devices and Applications

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable Solid State Power Substations (SSPS) for future Navy warships. Conventional distribution approaches being considered for the next generation of aircraft carriers employ a 13.8 kV a.c. power distribution that is stepped down to 465 V a.c. by using large (6 ton and 10 m^3) 2.7 MW transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phase 2 and 3 programs for 2005 through 2008. A new NIST/DOE program was recently established to analyze advanced power electronic component technologies needed for 300 MW Power Conversion Systems (PCS) to enable future Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas. The extremely large PCS is required to convert the 700 V, 1000 A DC power output of one thousand fuel cell modules to the 300 kV AC power transmission level.

DELIVERABLES:

- Participate in planning future government and industry high power generation, transmission, and distribution programs enabled by emergence of HV-HF power semiconductor devices including WBST-HPE Phase 3 and the DOE Fuel Cell Power Plant program. 4Q 2007
- Participate in coordinating the effective utilization of DARPA HPE Phase 2 devices in the SSPS power converter developed by the HPE Phase 3 contractor team. 2Q 2009
- Perform analysis to identify advanced high-megawatt PCS technologies requiring investment to meet the goals of the DOE SECA and FutureGen programs for near-zero emission central station fuel cell power plants. 4Q 2008
- Provide leadership in Chairing an Interagency Task Force and in establishing an industry roadmap for High Megawatt Power Converters. 1Q 2008

Characterize Electrical Performance of DARPA HPE Device Deliverables

NIST continues to serve as the exclusive device deliverable evaluation lab for the DARPA WBST HPE Phase 2 program providing data and analysis critically important to evaluate contractors and plan future programs. NIST evaluates device performance and provides feedback to contractor and DARPA program manager as well as the potential component users in government and industry. The NIST characterization data and analysis has continually identified critical technology advancements required to meet DARPA program goals such as recommendations to improve surface passivation, reducing internal gate resistance, improving PiN power diode (diode made with p-type to intrinsic to n-type semiconductor junctions) speed, transitioning program goal from PiN to Schottky diodes, and specific design parameter targets for MOSFET and IGBT (insulated gate bipolar transistor) designs. The NIST HV-HF characterization results are routinely used in by DARPA in planning documents and by the device developers in publications.

DELIVERABLES: Apply NIST HV-HF power device test systems to evaluate the performance of the 10 kV, 100 A, 50 ns half-bridge power modules produced by the DARPA WBST-HPE program and asses the potential for enabling advanced commercial and military power generation, transmission, and distribution systems. 2Q 2008

SiC Power Device Models for HV-HF Power Converter Simulation

Accurate and robust circuit simulator models for HV-HF semiconductor devices are needed to evaluate the impact of the new semiconductor technology on power converter system performance. NIST develops the generic physics-based models for the SiC power semiconductor devices that are provided in commercial circuit and system simulation software. In addition, NIST also develops model parameter extraction methods needed to measure the physical and structural parameters of specific devices. The NIST model parameter extraction tools have recently been used to characterize SiC power MOSFETs and diodes introduced by the DARPA WBST-HPE Phase 2 program. These models were used as a virtual prototype to perform simulations of a 2.7 MW Solid State Power Substation (SSPS) by the DARPA/ONR/Navsea WBST HPE Government Independent Panel providing the basis for the HPE Phase 3 Broad Area Announcement. The models are also to be used as part of the NIST/DOE advanced PCS technology evaluation.

DELIVERABLES: Develop and apply models of advanced component technologies for high megawatt power conversion systems to determine technologies requiring substantial federal investment to meet the DOE SECA and FutureGen program goals for central station fuel cell power plant PCS requirements. 4Q 2008

Metrology for SiC Device Degradation and Reliability

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for devices with minority carrier injection is the degradation in the electrical characteristics after prolonged forward bias conduction. The degradation occurs from latent material defects such as Basel Plane Dislocations (BPDs) that result in the formation and growth of stacking faults activated by excess-carrier recombination. NIST has recently developed automated stress and degradation monitoring systems to assess degradation of SiC devices. The monitoring methods include forward conduction voltage drop, switching reverse recovery characteristics, and pulsed thermal imaging of current uniformity.

DELIVERABLES: Apply long term application-like 20-kHz switching test system to evaluate HV-HF application reliability and use to evaluate reliability of DARPA WBST-HPE. 4Q 2007

Accomplishments

- *NIST played a key role in planning and coordinating activities of the DARPA HPE program on high voltage SiC power devices including:* Evaluated contractor performance for DARPA WBST HPE Phase 2. Participated in planning and writing Broad Area Announcement (BAA) for DARPA WBST HPE Phase-3 programs and presented status of SiC power devices at the Phase 3 Industry Bidder Briefing day. Also presented the status of the DARPA HPE program at GomacTech in 2005 and 2006, and presented the status of HV-HF semiconductor devices at the IEEE Industry Applications Society Meeting (this paper received the 2006 William M. Portnoy Award). Served as Member of DARPA/ONR Solid State Power Substation (SSPS) Government Independent Design Panel. Participated in planning ONR Mantech SiC Power Device manufacturability program.

- *NIST leading industry and other Federal Agencies in coordinating activities in High Megawatt Power Conversion Systems*. Planed and held the first High Megawatt Converter workshop at NIST with participants from major government and industry programs requiring advanced power converter technologies for high megawatt power conversion systems. Hefner (NIST) appointed as the Chairman of the Interagency Task Force for High Megawatt Power Conversion systems. Served as panel member for DOE Program on SiC-based Inverters in Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas.

- *High voltage clamped inductive and resistive switching test bed developed*. A low parasitic inductance 15 kV switching test system for clamped inductive and resistive SiC MOSFET switching characterization was developed and integrated into the 25 kV safety-interlocked curve-tracer system. A low parasitic capacitance temperature-controlled test fixture with 20 kV voltage isolation and 350° C maximum controllable temperature was also included to enable investigation of HV-HF device characteristics at elevated operating temperature. The hardware is controlled by the NIST virtual curve-tracer instrumentation software.

■ *NIST unique HV-HF device metrology demonstrated unprecedented performance of DARPA WBST-HPE:* The NIST high voltage curve tracer and the NIST high-voltage high-frequency (HVHF) switching test systems were used to demonstrate the unprecedented performance of DARPA WBST-HPE MOSFETs, *e.g.*, 10 kV, 12 A, 50 ns inductive load switching shown in Fig. 1. Typical high voltage silicon devices require several microseconds to switch at 6.5 kV maximum. Significant advances in materials, device design and HV-HF metrology were required for this achievement.

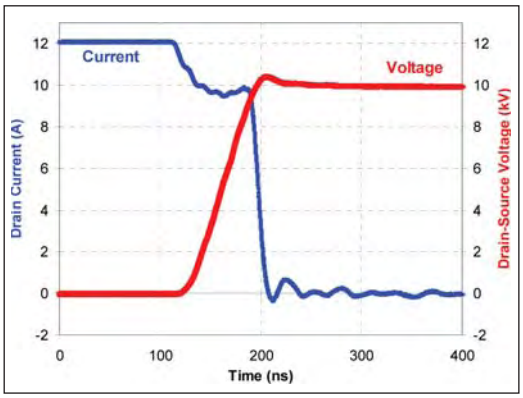

Figure 1. NIST measurement of the unprecedented performance of the SiC power MOSFETs switching at 10 kV, 12 A and 200 °C in less than 75 ns.

■ *NIST contributed to device design required to improve 10 kV SiC rectifier reverse recovery speed:* NIST provided guidance on techniques for improving the reverse recovery time (switching speed) of 10 kV SiC rectifiers developed by the HPE program. The guidance included structure changes to control the plasma distribution during reverse recovery in PiN diodes as well as the recommendation that the program be refocused toward Junction Barrier Schottky (JBS) diodes. NIST characterized the reverse recovery performance of the various diode designs that were produced using the NIST 4 kV, 50 A, 10 ns diode reverse recovery tester. Results indicate that the reverse recovery charge (area under the negative portion of the current waveform in Fig. 2 is reduced using plasma engineering but only the JBS diode is capable of 20 kHz operation.

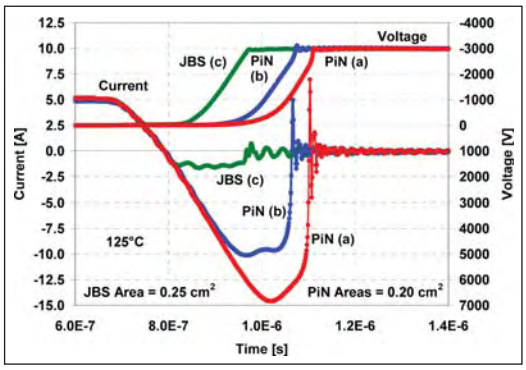

Figure 2. Comparison of reverse recovery time for two different 10 kV SiC PiN diodes, (a) and (b), and a 10 kV JBS SiC diode (c), all at 125 °C.

■ *NIST HV-HF SiC models were used to simulate system performance:* NIST's metrology, device modeling, and parameter extraction tools have resulted in software models for the HV-HF devices that are being produced by the DARPA WBST HPE program. These models are being used by industry and government to simulate the performance of future power distribution and conversion systems enabled by the new HV-HF semiconductor device technology. Figure 3 shows the comparison of the model with measured results.

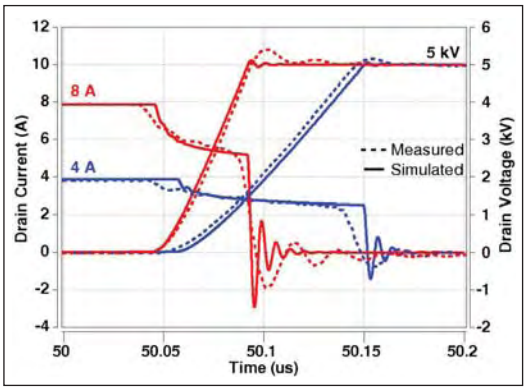

Figure 3. Comparison of measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms for a SiC MOSFET. Both tests were performed at 25 °C with a clamp voltage of 5 kV and drain currents of 4 A (blue) and 8 A (red), respectively.

■ *Extended capabilities of IMPACT parameter extraction software*. The capabilities of the parameter extraction software, IMPACT, were extended to include MOSFETS (in addition to IGBTs) and three prototypes of SiC material (in addition to Si). The parameter extraction hardware was also extended to enable capacitance versus gate- and drain-voltage characterization up to 5 kV.

■ *NIST determined that the SiC PiN diode forward bias degradation due to stacking fault growth is also accompanied by reduced reverse recovery charge and by substantial reduction in device conduction area*. This is significant because it was shown that a factor of ten reduction in conduction area and thus current handling capability occurs for what was previously thought to be a small increase on-state voltage. The conduction area is measured using the unique NIST high-speed pulsed thermal imaging system as shown in Fig. 4. The paper describing this work won the William M. Portnoy Award at the 2005 IEEE Industry Applications Society Meeting 2004.

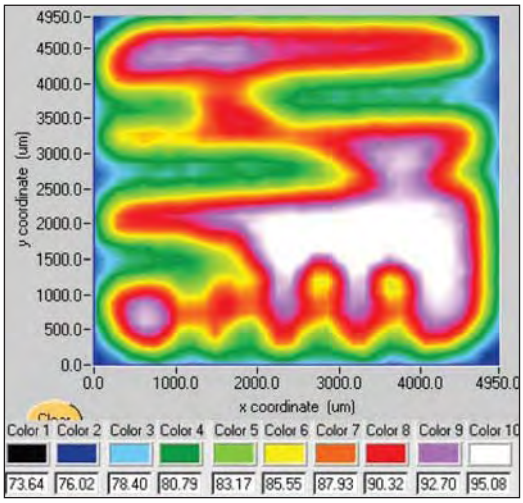

Figure 4. Pulsed thermal image of Low degradation rate SiC PiN diode showing 30 % area reduction after 500 hours of operation.

■ *Demonstrated HV-HF Switch-Mode Power Conversion for the first time*. NIST demonstrated HV-HF Switch-Mode Power Conversion for the first time using DARPA HPE 10 kV, 5 A SiC power devices in a specially designed power converter test system. The demonstration shows that the DARPA HPE SiC MOSFETs are capable of 20 kHz at 5 kV with 2X voltage margin as shown in Fig. 5. By contrast, the fastest high-voltage silicon devices (6.5 kV IGBT) are only capable of less than 300 Hz at 3.2 kV without overheating. The DARPA HPE MOSFET performance meets important industry need and will enable many new HV-HF power conversion systems.

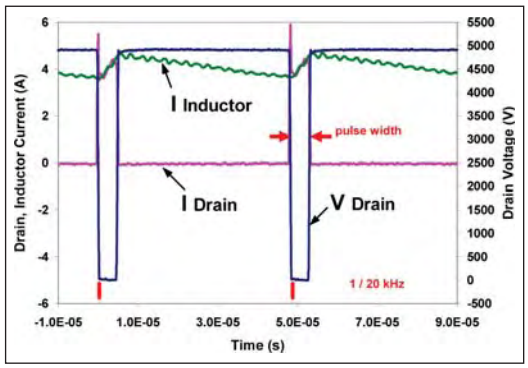

Figure 5. Inductor current, drain current, and drain voltage for as SiC MOSFET operating in a 5 A, 10 kV, 20 kHz switch-mode power converter.

■ *Developed physics-based, transient, electro-thermal simulation capability for high-voltage, high-current SiC bipolar power devices*. A Physics-based TCAD simulations capability has been developed by NIST for high-voltage, high-current SiC power semiconductor devices. This capability has been applied to the electro-thermal study of SiC power thyristors operating under high-current, pulsed-power conditions as shown in Fig. 6. The use of electro-thermal, physics-based device and circuit modeling is fundamental in the study of the operating limits of SiC power devices.

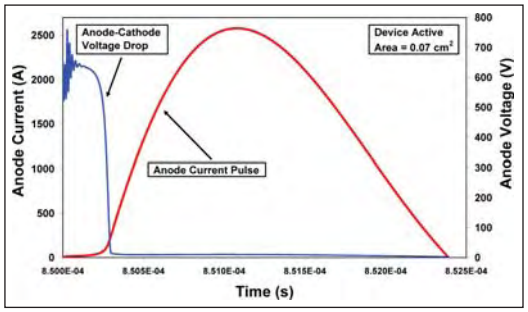

Figure 6. SiC thryristor anode voltage and anode current pulsed-power waveforms.

COLLABORATIONS

Synopsys Inc., SiC power device modeling and parameter extraction for IGBT library component models

CREE, Characterization and application of SiC power devices

Northrop Grumman Corp., Characterization and application of SiC power devices

Virginia Tech., Silicon and SiC power device utilization

Powerex, Power semiconductor device packaging

DARPA/ONR/Navsea, SiC power devices for SSPS and other applications

GE CRD, SiC power devices for robust integrated power electronic systems

University of Puerto Rico Mayagüez, Electro-thermal simulation of power electronic systems

University of Wisconsin Madison, SiC power system simulation

Purdue University/Carnegie Mellon University/Vanderbilt University/Auburn University, Development of process technologies for SiC power devices

Electric Power Research Institute, power semiconductor devices for solid state intelligent universal transformer

Department of Energy, electric vehicle power electronics and power converters for 300 MW fuel cell generation plant

Stanford University, numerical simulation of SiC power semiconductor devices.

Army Research lab, Pulsed power semiconductor devices.

Recent Publications

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Tam H. Duong, David W. Berning, A. R. Hefner, Jr., and Keyue M. Smedley, "Long-Term Stability Test System for High-Voltage, High-Frequency SiC Power Devices," Proceedings of the 2007 IEEE Applied Power Electronics Conference (APEC 2007), February 25–March 1, 2007, Anaheim, CA, pp. 1240-1246.

J. M. Ortiz-Rodríguez, T. Duong, A. Rivera-López, and A. R. Hefner, "High-Voltage, High-Frequency SiC Power MOSFETs Model Validation," to be appearing in 2007 IEEE Power Electronics Specialists Conference (PESC), Orlando, FL.

Madelaine Hernández-Mora, Adwoa Akuffo, Colleen Hood, José M. Ortiz-Rodríguez, and Allen Hefner, "Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability," to be appearing in 2007 IEEE Power Electronics Specialists Conference (PESC), Orlando, FL.

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J. M. Ortiz-Rodriguez, A. R. Hefner, D. Berning, M. Volez-Reyes, M. Hernindez-Mora, G. Gonzalez, *"Lumped-parameter thermal modeling of an IPEM using thermal component models,"* IEEE Proceedings on Computers in Power Electronics Workshop, pp. 43-48 (Aug.2004).

J. Reichl, D. Berning, A. R. Hefner, J.-S. Lai, *"Six-pack IGBT dynamic electro-thermal model: parameter extraction and validation,"* IEEE Applied Power Electronics Conference and Exposition, Volume 1, pp. 246-251 (2004).

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R. Singh, A. R. Hefner, Jr., *"Reliability of SiC MOS Devices,"* Journal of Solid-state Electronics, Vol. 48, No. 10-11, pp. 1717-1720 (24-JUNE-2004).

Organic Electronics Metrology

Technical Contacts:
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D. Gundlach
L. Richter

Goals

Organic electronic devices are increasingly incorporated into commercial prototypes and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need has emerged for new diagnostic probes, tools, and methods to address new technological challenges. Organic electronics adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of measurement methods to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provide the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics.

Customer Needs

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high volume manufacturing, incorporation on flexible substrates, and designed functionality. Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification tags. Market estimates range from $10–30 B globally by 2010–2015, with applications in displays, logic, and lighting. Organic light emitting diodes for displays and lighting form the first generation of products, projected to grow from approximately $0.5 B today to $3 B in 2010. Market expansions to $250 B by 2025 have been estimated should major technology and business barriers be overcome. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. Without this knowledge, guided improvements in materials and processing design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces in organic devices is critical to proper interpretation of carrier transport behavior. Identifying and controlling specific contributions to performance variation requires metrology unavailable to device manufacturers and spanning multiple disciplines that include device physics, chemistry, and materials science.

Technical Strategy

The initial focus of the NIST program is on the organic field effect transistor (OFET) because it is the basic building block of circuitry. The fundamental framework, characteristics, and issues that arise during OFET development are transferable to other organic electronic devices because of commonalities in architecture and interfaces. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics: unique measurements of organic materials and interfaces for both structure and chemistry and electronic properties; and the development of an integrated measurement test platform to correlate device performance with the processing conditions, microstructure, and primary chemical structure of organic semiconductors.

1. Interfacial structure and chemistry fundamentals: The basic OFET consists of thin layers (20 nm to 50 nm thick) of disparate materials including the organic semiconductor, dielectric, electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance.

We are developing a suite of powerful measurement methods including X-ray, neutron, and optical probes to characterize critical organic

interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET device evaluation. Near-edge X-Ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements and measure the orientation of interfacial molecules. Spectroscopic ellipsometry (SE) is a powerful tool to study the electronic state of molecules and evaluate how the transition dipoles of electronic excitations are oriented with respect to film geometry. Polarized infrared absorption (IR) spectroscopy provides both configuration and orientation information for many chemical moieties common to organic electronics materials. Specular and grazing X-ray diffraction (XRD) measurements measure long range positional order to describe unit cell configuration and domain size information. Finally, scanning probe techniques such as atomic force microscopy provide surface morphology information to assess domain shape, size, and spacings.

DELIVERABLES:

- Complete NEXAFS, XRD, and AFM measurements of liquid crystalline semiconducting polymer films as a function of the surface roughness of the substrate and heat treatment. 2Q 2007
- Complete NEXAFS, XRD, polarized IR, SE, and AFM measurements of liquid crystalline small molecule films as a function of the side chain length. 2Q 2007
- Complete measurements of the effect of side chain attachment density on the thin film morphology of liquid crystalline poly(thiophene) materials. 3Q 2007
- Complete measurements of the effect of crystal growth of solution processed small molecule films on charge transport. 4Q 2007

2. *In situ* measurement platform: The highest charge carrier mobilities of semiconducting polymers are obtained only after the film is heated through a mesophase transition. Detailed microstructure analysis of the polymer film during the mesophase transition is critical to determining optimal chemical structures for future generations of polymer semiconductors.

We are developing methods for performing structure measurements described in section 1 on samples while they are heated through a mesophase transition. NEXAFS and polarized IR will monitor the configuration and orientation of the side chains. XRD will measure the thermal expansion of the lattice and the growth and orientation of ordered domains. Polarized optical microscopy will determine the degree of spatial reorganization of the film through changes in the birefringence. NEXAFS and SE will monitor the orientation of the polymer backbone. Transistor measurements will assess the combined effects of thermal disorder, film reorganization, and the thermal activation of charge carriers. The combination of each of these measurements will be used to determine the packing arrangement of the polymer in the mesophase and identify the key structural elements of the molecule responsible for the mesophase, and the mechanism whereby heating to the mesophase increases carrier mobility.

DELIVERABLES:

- Develop instrumentation to incorporate inert atmosphere hot stages on the NEXAFS, SE, and IR instruments and determine the effect of temperature and side chain attachment density on the structure of the side chains and backbone with temperature 2Q 2007
- Complete transistor tests to determine how polymer semiconductor carrier mobility changes with temperature. Assess potential impact of mesophase transitions near room temperature on electrical performance. 3Q 2007
- Complete synchrotron XRD study of the change in diffraction peaks as a function of temperature and side chain attachment density. 3Q 2007
- Obtain a variable temperature polarized optical microscope and determine the change in birefringence as a function of temperature. 3Q 2007

ACCOMPLISHMENTS

■ A strategy was developed to successfully resolve the detailed microstructure of the currently highest-performing polymer semiconductor, poly (2,5-bis(3-tetradecylthiophene-2-yl)thieno[3,2-b]thiophene) (pBTTT-C14) in collaboration with Merck Chemicals. The strategy used a combination of polarized photon absorption spectroscopies NEXAFS, SE, and IR - along with spacing information from XRD and atomic force microscopy (AFM). The combination of these complementary techniques elucidated structure elements not possible by a single technique (Fig. 1). The microstructure model validated theoretical predictions of collaborators at the Palo Alto Research Center (PARC). The strategy was applied to other polymer semiconductors and allowed us to identify a signature structural motif that distinguishes higher-performing polymers from lower-performing. The highest-performing

polymers have interdigitated side chains while others do not. Side chain interdigitation provides a mechanism for three-dimensional ordering and therefore results in larger domain sizes and improved charge transport. A consideration of primary chemical structure variation reveals that interdigitation is controlled by the attachment density of side chains to the polymer backbones. These results establish clear guidelines for side chain attachment in the synthetic design of high performance polymer semiconductors.

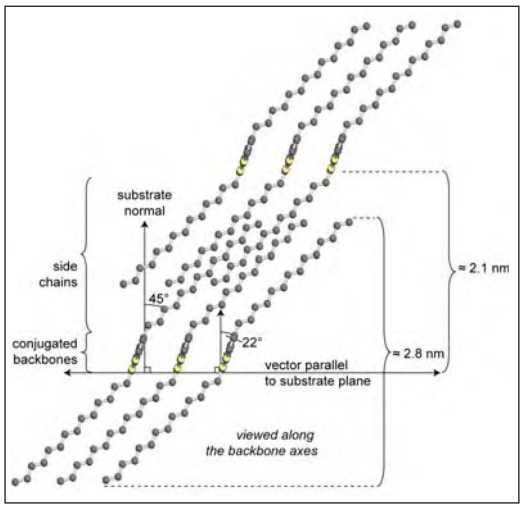

Figure 1. Detailed packing structure of pBTTT.

■ A method was developed to optimize the heat treatment of polymer semiconductors in collaboration with the NIST Combinatorial Methods Center. A thermal gradient stage was used to anneal a substrate covered with polymer transistors over a ~70 °C range about the polymer mesophase transition. After cooling, a programmable probe station was used to map the performance of transistors that had been heated across the gradient. Transition to higher charge carrier mobility occurred just beyond the mesophase transition temperature (Fig. 2). The method provides a general means to optimize the heat treatment of organic semiconductors.

■ Variations in dielectric chemistry were found to impact polymer microstructure. Films deposited on hydrophobic surface preparations, such as octyltrichlorosilane, form large molecular terraces with high charge carrier mobility. Films deposited on bare oxide form much smaller terraces with one decade lower carrier mobility. The results fit a nucleation model where crystals are more likely to nucleate from adhesive surfaces.

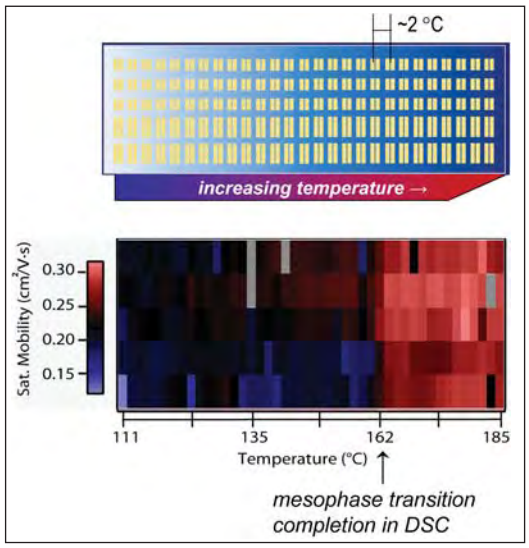

Figure 2. Gradient heat treatment of pBTTT transistors.

■ Systematic evaluation of transistor geometry revealed that polymer semiconductor charge carrier mobility varies with channel length, and the highest mobilities occur in the shortest channels. A detailed analysis of the temperature dependence of the current-voltage characteristics for transistors with different channel lengths showed that the transistor current was not contact limited for temperatures less than 300 K and proved that the mobility was field-dependent, following a Poole-Frenkel-like behavior. The field dependence was strongest for the most ordered films. These results have important implications for channel and dielectric scaling, and may improve the accuracy of organic transistor models for robust circuit design.

Collaborations

Polymers Division, MSEL – Jan Obrzut, Youngsuk Jung, Tatiana Psurek, Leah Lucas, Eric Lin, Joseph Kline

Semiconductor Electronics Division, EEEL – Curt Richter, Oleg Kirillov, Behrang Hamadani, Oana Jurchescu

Ceramics Division, MSEL – Daniel A. Fischer, Joseph Woicik

Surface and Microanalysis Science Division, CSTL – Andrew Moad

University of California, Berkeley – Kanan Puntambekar, Clayton Mauldin, Jean Fréchet, Vivek Subramanian

Stanford University – Mang-mang Ling, Zhenan Bao, Alberto Salleo

Palo Alto Research Center – Michael Chabinyc, John Northrup

Merck Chemicals – Iain McCulloch, Martin Heeney

Stanford Synchrotron Radiation Laboratory – Michael Toney

Corning – Sue Gasper, He Mingqian

Northwestern – Antonio Facchetti, Tobin Marks

University of Kentucky – John Anthony

Penn State University – Tom Jackson

Recent Publications

B. H. Hamadani, R.J. Kline, I. McCulloch, M. Heeney, C. A. Richter, D. J. Gundlach, "Influence of source-drain electric field on mobility and charge transport in organic field-effect transistors," Submitted to J. Appl. Phys.

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Micro- and Nano-Electro-Mechanical Technology Metrology

Technical Contacts:
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Goal

The objective of this project is the development of test structures and test methodologies for the characterization of Micro-Electro-Mechanical and Nano-Electro-Mechanical Technology (MNT) fabrication processes. MNT is the extension of MEMS (Microelectromechanical Technology Systems) to include nanometer-scale technology. Full characterization of an MNT process requires accurate measurement of a large set of material properties, including Young's modulus, residual stress, thermal coefficients, surface roughness, density, and Poisson's ratio; dimensional metrology; and device parameters. Ideally these measurements should be quick, performed in the manufacturing line, with measurements at multiple locations across each wafer to allow characterization of process variation.

Customer Needs

Two NIST U.S. Measurement System (USMS) workshops have been held relating to MNT metrology.

The first USMS Workshop was held in Pittsburgh, PA on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions approximately seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" MEMS. The concept of fabless MEMS is one in which a company can produce devices via a foundry rather than their own, expensive (over $100 million), fabrication facility. This is similar to the foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop was published in the MEMS Industry Group (MIG) 5-year anniversary report [2].

The second USMS Workshop was held on March 15, 2006, during Pittcon, in Orlando, Florida. This meeting was targeted on metrology needs for microfluidics applications. Representatives from seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

Technical Strategy

Overview: The MNT Metrology Project is currently championing MNT standardization efforts in three venues: ASTM, SEMI, and NIST. Highlighting the need for MNT standardization is the number of companies and other organizations participating in these standards activities.

- ASTM: The first four MNT standards (on in-plane lengths, residual strain, strain gradient, and terminology) [3,5-7] originated in the ASTM E08.05.03 Task Group on Structural Films for MEMS and Electronic Applications. Also within this task group, a standard is being developed for determining Young's modulus, ultimate strength, and fatigue for a surface micromachining process.

- SEMI: The MNT standardization efforts being actively pursued in SEMI's North American MEMS Standards Committee include recently-published SEMI Standard MS1-0307 on wafer-to-wafer bonding alignment targets, SEMI MS2-0307 on step height measurements [1], and SEMI MS3-0307 on MEMS terminology. Other SEMI MNT standardization efforts include a draft standard on Young's modulus (Doc 4330), a draft standard for wafer-wafer bond-interface strength (Doc 4419), a proposed guide for the design and materials for ultra high purity microfluidic systems (Doc 4213), specifications for microfluidic interfaces to electronic device packages (Doc 4214), and work on a draft standard for stiction.

An additional activity in SEMI's MNT standardization effort is the identification of standards related to MNT technology. SEMI is attempting to identify these standards and incorporate them into SEMI's "Living Standard." This Living Standard, which will list MNT standards from all standardization bodies and be maintained by the North American MEMS Standards Committee, will serve to guide industry and researchers to existing standards and highlight areas where standards may be needed.

DELIVERABLES: Draft "Living Standard" and easy-to-access SEMI Standards Web page incorporating, for example, a compilation of all MNT standards and pertinent links for purchasing. 4Q 2007

■ NIST: Proposals have been crafted in the MNT Project for the development of two Standard Reference Materials (SRMs); the MNT 5-in-1 SRM and the micro-chevron SRM.

MNT 5-in-1 SRM: The prototype MNT 5-in-1 SRM is expected to double as the step-height and Young's modulus round robin test chip. The five parameters will be in-plane length, residual strain, strain gradient, step-height, and Young's modulus. The first three parameters have been standardized in ASTM as E 2244, E 2245, and E 2246. The fourth parameter recently became the MS2-0307 standard in SEMI. And, the draft standard for the fifth parameter is being balloted in SEMI as Doc 4330.

The five measurements will be taken at NIST on the 5-in-1 SRM and delivered to the customer in order for them to compare their in-house measurements with those taken at NIST.

Customers, including design companies, equipment manufacturers, and fabrication services, have expressed support for this SRM.

This is an interlaboratory effort, involving MSEL and MEL in addition to EEEL.

DELIVERABLES: Design of prototype 5-in-1 SRM complete and ready for fabrication. 4Q 2007

Micro-Chevron SRM: The micro-chevron SRM is proposed for the calibration of wafer bond strength. A micro-chevron test structure (see Fig. 1) would be used in this destructive test.

Wafer-wafer bonding is a mainstay for MEMS design and fabrication. MEMS components, such as acceleration sensors, gyroscopes, micropumps, or microvalves that are increasingly found in smart automotive and navigation control systems or in medical devices typically use wafer bonding technologies. Due to being subjected to mechanical stresses, the industrial applications of these components require both a high mechanical strength and reliability of the wafer-bonded interface. For a knowledge of the strength determining factors (such as fatigue and stress corrosion) of wafer bonding, for quality control, and for the development of new bonding technologies, a method for determining the strength of such bonds is important to producers and users of MEMS devices, of wafer bonding equipment, and of wafer materials.

In the area of dimensional metrology for microfluidics, the MNT Metrology Project has undertaken development of dimensional metrology test structures and techniques. The goal of this work is standard test structures, methods, and analysis techniques such as exist for semiconductor devices.

DELIVERABLES: Prototype test chip for microfluidics dimensional metrology. 4Q 2007

In the area of microrobotics, the MNT metrology project is organizing the initial nanogram demonstration competition at the 2007 RoboCup tournament to be held July 2007 in Atlanta, Georgia. This high-profile activity, involving teams from universities in the U.S. and overseas, will highlight NIST's MEMS activities. The MNT metrology project is also investigating the unique metrology issues associated with micro-robots with the goal of

DELIVERABLES: Organize and hold the demonstration competition for nanogram-scale robotics at the 2007 RoboCup tournament in Atlanta, Georgia. 3Q 2007

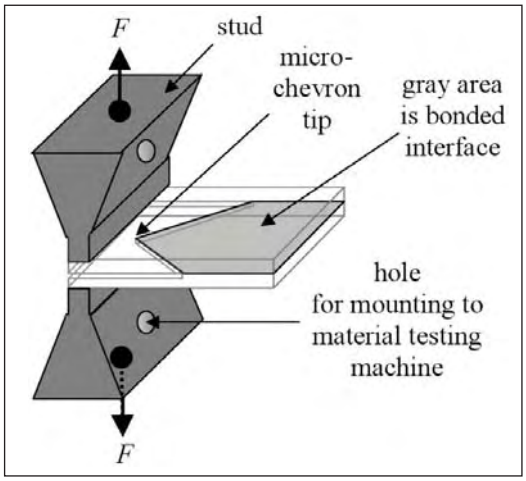

Figure 1. Studs mounted to a micro-chevron test structure.

NIST's role: Activities of the MNT Metrology Project include the following:

1. Keeping tabs on the progress of the various standardization efforts via attending standardization meetings (such as ASTM and SEMI) and maintaining the "Living Standard" for SEMI's N.A. MEMS Standards Committee.

2. Facilitating a collaborative research process between the different parties and acting as a neutral intermediary in shepherding the measurement techniques through the standardization process, if necessary. This could take the form of being the acting technical secretary for a standard.

3. Providing technical assistance to others during the standardization effort, if necessary (and given the appropriate resources).

4. Although the completion of each standard will have its own "character," given NIST's experience with the completion of the four ASTM MEMS standards, guidance can be provided as to what is involved in the completion of a standard test method and lessons learned along the way.

5. Develop standard reference materials, as appropriate.

6. Narrow in on the next material properties to work on at NIST (given the inputs received from the community and the USMS report [2]) and follow through with the work, if appropriate. Currently, the next parameters being considered for standardization are Young's modulus, residual stress, residual stress gradient, and wafer bond strength as described below:

Young's modulus: The draft standard (Doc 4330) being prepared for ballot obtains Young's modulus from resonating cantilevers and fixed-fixed beams oscillating out-of-plane. It applies to films, such as found in MEMS materials, which can be imaged using a non-contact optical vibrometer or comparable instrument.

DELIVERABLES: Young's modulus draft standard (Doc 4330) submitted to ballot. 4Q 2007

Residual stress and its gradient: The draft Young's modulus standard (Doc 4330) also provides for residual stress and stress gradient calculations. These calculations require the Young's modulus value obtained in the standard and values for residual strain (ASTM E 2245) and strain gradient (ASTM E 2246). High values of residual stress lead to failure mechanisms in ICs such as electromigration, stress migration, and delamination. Knowledge of the residual stress values can be used to improve the yield in CMOS fabrication processes.

Wafer bond strength: This draft standard (Doc 4419) uses micro-chevron test structures which consist of two materials, typically two silicon wafers bonded together. The main characteristic of the test structure is the wedge-like structure (which gives it its name) in the bond interface. Studs are glued to either side of the test structure and positioned in the material testing machine where the test structure is pulled apart (see Fig. 1). The maximum load is measured and the critical wafer bond toughness is calculated, which is a measure of the wafer bond strength. This draft standard can be used to determine a preferred bonding technique and it can be used to obtain on-wafer spatial distributions of wafer bond strength.

DELIVERABLES: Wafer bond strength draft standard (Doc 4419) submitted to ballot. 3Q 2007

Accomplishments

■ *MEMS Calculator:* The SED MEMS Calculator Web site [10] includes data sheets on which calculations can be performed that go hand-in-hand with the MEMS standards or standards-related work. Data Sheets K, L, and M are the most recent additions to this web site. Data Sheet K is for step height measurements, Data Sheet L is used to obtain the thicknesses of all the layers in a 1.5 μm CMOS process, and Data Sheet M is used to obtain Young's modulus values.

DELIVERABLES: Data Sheets K and L incorporated on the SED Web site (2Q 2007). Data Sheet M updated on the SED Web site. 3Q 2007

■ *Thickness:* SEMI Standard MS2-0307 on step heights was recently published [1]. Step height measurements are incorporated in an electro-physical technique to find the thicknesses of all the layers in a 1.5 μm commercial CMOS foundry process. Figure 2, next page, shows a test chip design with thickness test structures along the top edge of the chip. A design rendition of a sample thickness test structure is given in Fig. 3a, next page, with its cross-section given in Fig. 3b.) Relatively low values for u_c (between 0.00012 μm and 0.056 μm for a given processing run) have been found. In addition, an earlier version of this technique has been verified via the successful optimization of the Young's modulus values for the various layers in the process.

With this technique, a virtual transition region was found between the physical and the electrical approach, which is based upon the value of u_c. For the presented data set, the transition region is between the u_c values of 0.0073 μm and 0.013 μm, where the electrical approach tended to be used for the smaller values of u_c (which can be viewed as those layers, such as the poly1-to-active area

oxide and the poly1 layers, which tend to be fabricated earlier in the processing sequence) and the physical approach used for the larger values of u_c (which can be viewed as those layers, such as the metal1 and the glass layers, which tend to be fabricated later in the processing sequence).

The electro-physical technique is detailed in a 35-page paper, which is currently being reviewed.

DELIVERABLES: Draft paper entitled "Electro-physical Technique for Post-fabrication Measurements of CMOS Process Layer Thicknesses," receive ERB approval. 4Q 2007

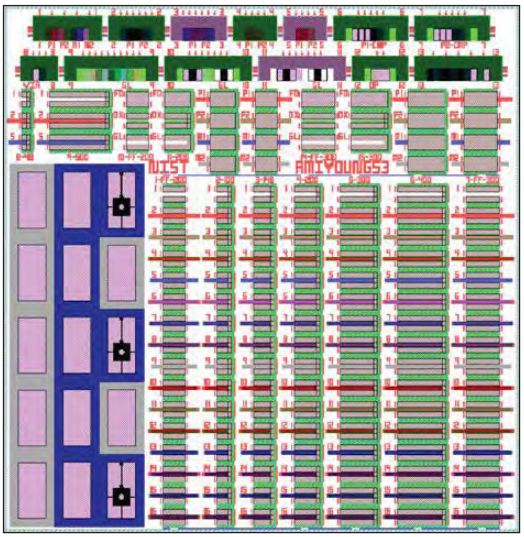

Figure 2. CMOS test chip design incorporating thickness test structures, cantilevers, fixed-fixed beams, and tensile test structures.

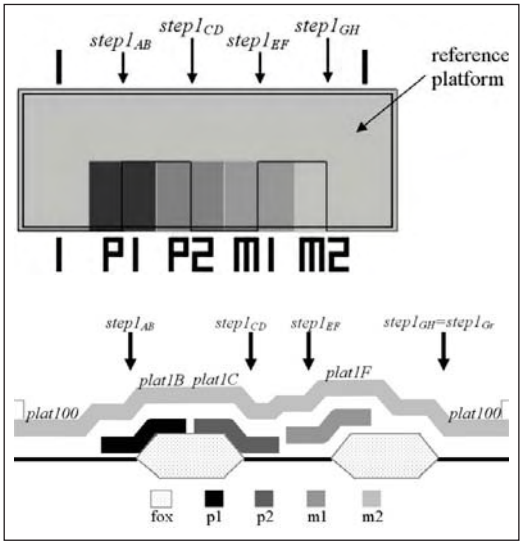

Figure 3. For a thickness test structure: a) a design rendition and b) a cross-section.

■ *Young's modulus:* The test chip design given in Fig. 2 includes cantilevers ranging in length from 100 μm to 400 μm. (A procedure was developed using the optical vibrometer to obtain the resonant frequencies of the shorter length cantilevers.) Plots of Young's modulus versus length for each layer exhibit phenomenal results. *The optimized Young's modulus results are stable as a function of length and within the realm of acceptability!* Figure 4 shows these plots for metal1 and metal2. The data points given at L=500 μm represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds represent values given in the literature. The line represented by '*Eguess*' is the initial value used in the optimization. An initial result from tensile tests done by David Read at NIST-Boulder found an average metal1 and metal2 Young's modulus value of 63 GPa, which falls nicely between the metal1 and metal2 lines in Fig. 4.

The resonant frequency technique for finding the Young's modulus values is presented in an article prepared for Electron Device Letters, which is currently being reviewed.

DELIVERABLES: Draft article entitled "Young's Modulus Measurements in Standard IC CMOS Processes using MEMS Test Structures," receive ERB approval. 4Q 2007

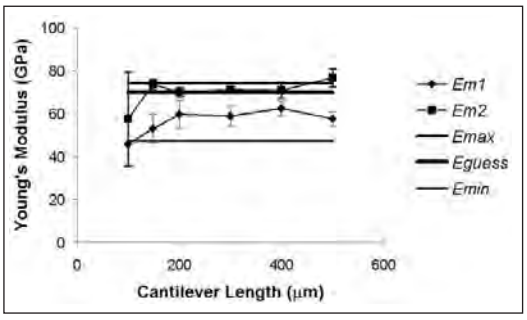

Figure 4. Optimized Young's modulus values for metal1 and metal2 versus length.

Collaborations

BayTech Group, 30 Winsor Way, Weston, MA, Winthrop A. Baylies.

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. P. Thomas Veriner.

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read.

Klaros Corporation, Beallsville, MD Robert I. Scace.

Others (current and/or future): Univ. of Wisconsin, Exponent, Pennsylvania State Univ., Fraunhofer Inst. (Germany), Univ. of Maryland, MEMSCAP, and others not yet identified.

Recent Publications

SEMI MS2-0307, "Test Method for Step-Height Measurements of Thin, Reflecting Films Using an Optical Interferometer," March 2007.

MEMS Industry Group (MIG) 5-Year Anniversary Report, "Standardization and the Study of the U.S. Measurement System for Micro Nano Technologies," September 2006.

ASTM E 2444–05$^{\varepsilon 1}$, "Standard Terminology Relating to Measurements Taken on Thin, Reflecting Films," January 2006.

J. C. Marshall, R. I. Scace, and W. A. Baylies, "MEMS Length and Strain Round Robin Results with Uncertainty Analysis," NISTIR 7291, January 2006.

ASTM E 2244–05, "Standard Test Method for In-Plane Length Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

ASTM E 2245–05, "Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

ASTM E 2246–05, "Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

J. C. Marshall, E. M. Secula, and J. Huang, "Round Robin for Standardization of MEMS Length and Strain Measurements," SEMI Technical Symposium: Innovations in Semiconductor Manufacturing (STS: ISM), SEMICON West 2004, San Francisco, CA, July 12-14, 2004.

J. C. Marshall, "MEMS Length and Strain Measurements Using an Optical Interferometer," NISTIR 6779, August 2001.

SED MEMS Calculator Web site: http://www.eeel.nist.gov/812/test-structures/MEMSCalculator.htm.

NIST's Center for Nanoscale Science and Technology Nanofab

Technical Contacts:
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Goals

The CNST Nanofab is a national, shared access, shared cost, user facility that provides for the measurement and fabrication of nanoscale structures, including, electronic devices, magnetic devices, MEMS, bio-devices, prototypical nanoscale test structures, measurement instruments, and standard reference materials. It provides:

- Access to expensive nanoscale measurement and fabrication tools, technologies, and expertise in a shared-access, shared-cost environment to both NIST and external users.
- A venue to foster collaboration in nanotechnology across NIST's laboratories and with NIST's external partners in industry, academia, and other government agencies.
- A workplace that enables CNST and others to help remove the measurement barriers that are delaying or preventing the implementation of new products based on nanotechnology.

Customer Needs

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in a variety of nanotechnologies in the face of heightened global competition, NIST has established the Center for Nanoscale Science and Technology (CNST). Its mission is to provide science and industry with the necessary measurement methods, standards, and technology to facilitate the development and productive use of nanotechnology from discovery to production. A key component of the CNST is the Nanofab, a national, shared access user facility that provides an economical means to access the expensive tools required to measure and fabricate nanostructures. The CNST Nanofab is located in two of the five buildings (see Fig. 1) in the Advanced Measurement Laboratory (AML) at the Gaithersburg, Maryland campus.

Technical Strategy

The AML location provides the CNST with superior vibration, temperature and humidity control, and air cleanliness. The Nanofab cleanroom has approximately 740 m^2 of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment

Figure 1. Main entrance to the AML showing the CNST Nanofab on the left.

(capable of processing 150 mm wafers) that is now fully operational (Fig. 2). This includes wet chemical wafer cleaning stations, furnaces (two banks of four tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, four reactive ion etchers (SF_6/O_2, Fl Metal, Cl Metal, Deep), one XeF_2 isotropic silicon etcher, five metal deposition tools (three thermal, one e-beam, one sputterer), contact lithography (front- and back-side alignment), critical point dryer, microwave plasma asher, nanoimprint lithography, converted SEM e-beam lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, AFM, etc.). A state-of-the-art e-beam lithography system with mask making capability has been installed and is scheduled for operation in July 2007.

Figure 2. Oxidation and annealing furnace banks.

The Nanofab is operated as a shared access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, are permitted to independently operate the equipment. As of May 1st, 2007, the CNST Nanofab is accessible to users from outside NIST, such

as academia and industry. The tools are operated in a manner such that a wide variety of materials can be processed. Additionally, the CNST Nanofab is unique in that it is located in close proximity to the CNST Research Division, the NIST Laboratories, and the NIST Center for Neutron Research which contain both a wealth of measurement science expertise and a vast array of state-of-the-art and advanced prototype tools. .

DELIVERABLES: E-beam lithography system fully operational by 3Q 2007.

METROLOGY FOR SPINTRONIC DEVICES

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"Imaging and metrology of magnetic structures are at the heart of the systematic development and characterization of magnetoelectronic materials and devices"

WTEC Panel on
SPIN ELECTRONICS
Final Report August 2003 (p.18)

GOALS

The overall goal of the Metrology for Spintronic Devices program is to develop the metrological tools that will enable the development of electronic devices that exploit the electron spin degree of freedom in addition to its charge. Present spintronic devices include magnetic random access memory (MRAM), which has the possibility of becoming a "universal" memory element, hard-disk drive read heads, and other highly-compact magnetic memory devices, such as those based on current induced domain-wall motion in magnetic wires. In addition, spintronic devices also present an avenue towards replacing conventional complementary metal oxide semiconductor (CMOS) technology as device dimensions shrink into the deep nanometer regime, development of entirely new device structures such as nanoscale microwave components for on-chip spectral analysis, nanoscale timing elements, and microwireless communication architectures. In each case, a fundamental understanding of the interactions between a spin-polarized current and ferromagnetic metals and semiconductors is a necessity. The particular goal of this project is to develop the metrology and perform the fundamental measurements to enable the development of these spin-based devices.

An additional goal is to enable the development of magnetoelectronic and spintronic devices by using Scanning Electron Microscopy with Polarization Analysis (SEMPA) to directly image the nanoscale magnetic structure and correlate the magnetic structure with device performance.

CUSTOMER NEEDS

MRAM elements are currently being shipped to customers for incorporation into products which are expected to be commercially available by the end of 2006. The magnetic memory elements are expected to enter the marketplace at the 180 nm lithography node. Although no public roadmap for MRAM exists, companies such as IBM and Freescale Semiconductor expect that the present circuit architecture, which relies on switching (writing) using applied magnetic fields, will not be viable beyond the 65 nm lithography node. These limitations arise because the scaling laws associated with the stability of the magnetic structures used in MRAM devices: As the device dimensions are decreased, the magnetic elements are required to have increased stability against thermal fluctuations. This, in turn, will require larger writing fields, which cannot be supported in the present device architecture. It is expected that a new switching mechanism will be required for scaling MRAM devices below the 65 nm node. One way to circumvent this scaling limitation is to switch the elements through the use of spin-polarized currents flowing through the memory elements to switch (write) them via the spin transfer effect. While this switching mechanism is largely expected to allow continued scaling of MRAM elements, it has been experimentally demonstrated only within the last five years, and the present understanding of the effect remains only qualitative. In order to enable the continued scaling of MRAM devices, the fundamental metrology and measurement of the intrinsic scaling laws associated with the spin transfer effect are a necessity. In particular, methods to definitively relate threshold switching currents to fundamental materials properties need to be developed, materials damping parameters need to be measured as a function of device size, and tunnel junction characteristics need to be understood at the atomic scale.

The performance, and ultimately the commercial viability, of magnetoelectronic devices such as Magnetic Random Access Memories (MRAM) or magnetic field sensors depend on understanding and controlling their magnetic nanostructure. Nanoscale magnetic features such as domains, domain walls, anisotropy dispersion, edge effects, grain structure, and defects critically affect device performance. Imaging these magnetic nanostructures requires techniques with high spatial resolution and high magnetic sensitivity that do not disturb the tiny amount of magnetic material used in a device. SEMPA has 10 nm spatial resolution, 1000 Fe atom sensitivity, and is nondestructive while imaging. Furthermore, SEMPA images the magnetization directly allowing direct comparisons with computer generated micromagnetics simulations of ideal devices.

More generally, many semiconductor devices encounter scaling limitations as the device dimensions shrink into the deep nanometer regime. For instance, present CMOS scaling laws indicate that the devices will encounter both quantum mechanical and fabrication limitations below the 10 nm length-scale. One potential avenue towards circumventing this roadblock is

spin-based devices, which afford the possibility of fast operation, low power-dissipation, and general compatibility with CMOS-based device fabrication. Furthermore, novel effects which occur only at the nanoscale in hybrid ferromagnetic systems can also be exploited to provide new functionality in nanoscale devices. These devices point a way to creating new nanoscale systems such as on-chip spectral analysis, nanoscale microwave generators, as well as nanoscale microwave mixers, phase discriminators, and chip-to-chip wireless communication schemes. However, as with the spin-based memory devices, in order for these spin-enable devices to be commercially realized, the fundamental measurement techniques required to understand the interactions between spin polarized electrons and ferromagnetic materials need to be developed and implemented.

Technical Strategy

The technical strategy is to develop the metrology and perform the fundamental measurements to characterize and understand the effects of spin-polarized currents in spin-based magnetic nanostructures. Particular attention will be paid to the intrinsic scaling laws associated with device switching times in both all-metallic and magnetic tunnel junction MRAM structures, as well as the thermal contributions to the critical current densities. These measurements will help to provide a basis for scaling of MRAM devices below the 65 nm node. Our technical work will also focus on evaluating the potential of nanoscale spintronic devices for replacing/augmenting CMOS in the deep nanometer regime. One potential method to transmit information without charge is through the use of spin waves. Our work will focus on understanding the generation, transmission, and phase control of localized nanoscale spin wave oscillators.

1. Develop methods to measure damping in magnetic nanostructures, particularly as a function of oxidation.

DELIVERABLES:

- Measure damping in NiFe magnetic nanodot *arrays* with sizes ranging from 200 nm to 50 nm. Measurements will be performed on both intentionally oxidized structures and ones capped to prevent oxidation. Compare results with continuous films. Complete measurements in 1Q 2007 and submit results in 2Q 2007.
- Develop metrology to electrically excite and detect FMR resonance in *individual* nanoscale devices made to continuous films and patterned films. Complete measurements in 2Q 2007 and submit results in 3Q 2007.

2. Perform magnetic imaging of tunnel junction device under active bias.

DELIVERABLES: Develop infrastructure and fabrication techniques to allow Lorentz imaging and *simultaneous* electrical characterization of magnetic tunnel junction devices under active bias. Complete measurements in 2Q FY 2007 and submit results in 3Q 2007.

3. Determination of thermal contributions to linewidths of spin transfer oscillators.

DELIVERABLES: Develop infrastructure to measure the linewidth of spin transfer oscillators as a function of temperature (300 K – 10 K) and applied field strength in order to directly determine thermal contributions to oscillator linewidth (phase noise). Complete infrastructure upgrade in 1Q 2007 and complete measurements in 3Q 2007.

SEMPA is already an established tool for imaging magnetic nanostructures in simple ferromagnetic structures. As structures are reduced in size to the nanoscale, the fabrication process can affect the magnetic properties, but to date there has not been a systematic investigation of this. Further, special protocols and instrumentation need to be developed for imaging the magnetization in samples that are operationally as close as possible to commercial magnetoelectronic devices. In particular, sample preparation techniques that expose the ferromagnetic element directly to the SEMPA probe need to be developed for a wide range of samples including insulating ferromagnetic oxides and delicate multilayers. Of course these cleaning procedures must not disturb the magnetic structure under investigation. Finally, since a critical question is the behavior of magnetic nanostructures in a functioning device, our recently developed instrumentation now makes possible magnetic imaging while the device is electrically active *i.e.*, while applying magnetic fields or measuring magnetoresistance.

1. Investigate the effect of fabrication method on magnetic structure of nanoscale magnetic elements.

DELIVERABLES: SEMPA images of arrays of permalloy magnetic elements (lines, squares and ellipses) ranging from 50 nm to 2 micrometer prepared by FIB, dry etching, and liftoff. 3Q 2007

2. Develop new sample cleaning capability to allow SEMPA imaging of a wider range of samples including insulating oxides and very thin film multilayers.

DELIVERABLES: Integrate electron cyclotron plasma source with the SEMPA system to provide an atom source producing thermal energy neutral atoms, a downstream plasma mode providing low energy ions and neutrals, and a broad beam ion source. 4Q 2007

ACCOMPLISHMENTS

■ *High-speed Current Induced Switching for MRAM Devices:* In collaboration with Hitachi Global Storage Technologies (HGST) and Freescale Semiconductors we have demonstrated sub-nanosecond (290 ps) switching of nanoscale MRAM devices is possible via the spin transfer effect. To date this is the shortest switching time that has been reported in the literature. The inverse switching time (*i.e.*, the switching frequency) at room temperature is linearly proportional to the current applied to the device. This finding is in accordance with the behavior expected from theoretical considerations and indicates that the measured room-temperature switching threshold is strongly affected by thermal fluctuations in the nanoscale devices. By extrapolating the measured switching current to zero applied pulse width, the *theoretical* value of the intrinsic device critical current can be determined. However, this theoretical method of determining the intrinsic switching thresholds (*i.e.*, those related to materials properties and device size) from stochastic, thermally activated switching events had not been experimentally verified. By extensively comparing the thresholds for current driven switching at room temperature and 4 K for a range of applied field values, we have been able to verify the extrapolation methods used to infer the intrinsic switching current, identify thermal contributions to the switching threshold, and determine the materials/device parameters that are responsible for setting the intrinsic switching threshold. These measurements will allow for improved device design and reliability for future MRAM at the 65 nm node and beyond.

Damping in Magnetic Nanostructures: One of the critical parameters in determining the threshold switching current in magnetic devices is the magnetic damping parameter; the larger the damping in the system, the larger the current required to switch the device. While the material dependent damping parameters have been routinely measured in macro/microscopic devices, very little is known about how damping is affected when device sizes are decreased to the nanometer length scale. As device dimensions are decreased, the surfaces of devices become increasingly important. This is particularly the case for damping in magnetic nanostructures. Nanomagnetic devices will typically have oxidation of the ferromagnetic materials on at least some of their sides, and ferromagnetic oxides are well known sources of damping. Recently some researchers have shown *indirect* evidence that the magnetic damping in magnetic nanostructures can be increased by more than a factor of ten relative to that of macroscopic devices. We have recently developed the metrology capabilities to *directly* measure the magnetic damping in a variety of magnetic systems over a wide range of device sizes. Our new optical method of measuring damping on arrays of devices has shown that, at room temperature, the oxidation has a negligible effect and shape variations in the nanoscale devices increases the apparent damping by only about a factor of two. We have also developed a new method to electrically measure the damping parameter in *single* devices having dimensions below 100 nm. These measurements, while still being perfected, corroborate those from the large arrays.

■ *Noise and Current Induced Switching in Magnetic Tunnel Junction Devices:* Currently, typical spin transfer based MRAM structures are based on all-metallic structures. These structures have resistances on the order of 5–10 ohms and are poorly impedance matched to standard semiconductor circuitry. While this impedance mismatch will become less severe as device dimensions are decreased, it will likely be necessary to implement magnetic tunnel junction (MTJ) devices. However, in general, there is also an increase in noise, particularly at low frequency, when incorporating tunnel junctions into device structures, which can degrade device performance and read-out fidelity. The low-frequency noise is associated with defects and atomic scale variations in the barrier. We have successfully measured and characterized this excess noise in high-quality aluminum oxide magnetic tunnel junctions with dimensions on the order of several micrometers and used Lorentz transmission electron microscopy (TEM) imaging to investigate the correlation between electronic noise and the structural properties of the barrier. More recently we have upgraded the TEM instrumentation and fabricated devices so that the magnetic devices can now be imaged with Lorentz microscopy under active bias. This

allows us to image directly the magnetic fluctuations in a device while simultaneously measuring its electrical characteristics. Through these simultaneous measurements we can discriminate between intrinsic magnetic fluctuations in the MTJ devices from those associated with electrical defects in the barriers.

■ *Nanoscale Generation of Spin Waves for Communication Architectures:* At present, spintronic devices are being considered as potential replacements for future generation CMOS devices. The basic advantage of the spintronic devices is that they provide the potential to perform both communication and computation through spin instead of charge, and so may be able to perform these operations with comparatively low power dissipation. Several proposed communication and computation architectures are based on the local generation and subsequent propagation of spin waves, Fig. 1. Previously, we have shown that nanoscale magnetic devices are able to generate coherent, gigahertz frequency spin waves. However, the currents required to generate them was relatively high and their propagation away from their source was only theoretical. We have performed the metrology to show directly that in the correct geometry the spin waves can coherently propagate more than 0.5 μm away from their point of generation, putting fairly lenient geometrical constraints on potential device considerations. Furthermore, by incorporating CoFeB materials in these devices we have been able to lower the currents required for the creation of spin waves by roughly a factor of three. This represents a significant advance towards viable device applications.

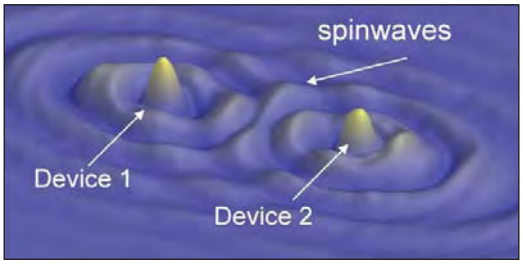

Figure 1. Micromagnetic simulation showing spin wave interactions between two closely spaced nanoscale oscillators.

■ *Nanostructured Magnetic Arrays to Control Motion of Magnetic Flux Quanta:* SEMPA images of a close-packed array of triangular magnetic elements contributed to a multi-institution research effort focused on the control of the vortex motion in superconducting materials. The magnetic elements form an array of asymmetric pinning potentials underlying the superconducting material, which creates a ratchet effect causing a rectified vortex motion (in one direction) when excited by an ac current. This offers interesting possibilities for manipulating flux quanta in fluxonics devices. Fig. 2 (a) shows an array of such triangles in the as grown state. In the lower part of Fig. 2, a higher resolution image of the as-grown magnetization of one of the triangles (b) is compared to the ordered state (c) after applying an in-plane field. The magnetic state of the underlying periodic array of magnetic triangular structures determines the ratchet dynamics of the magnetic flux quanta in the superconductor.

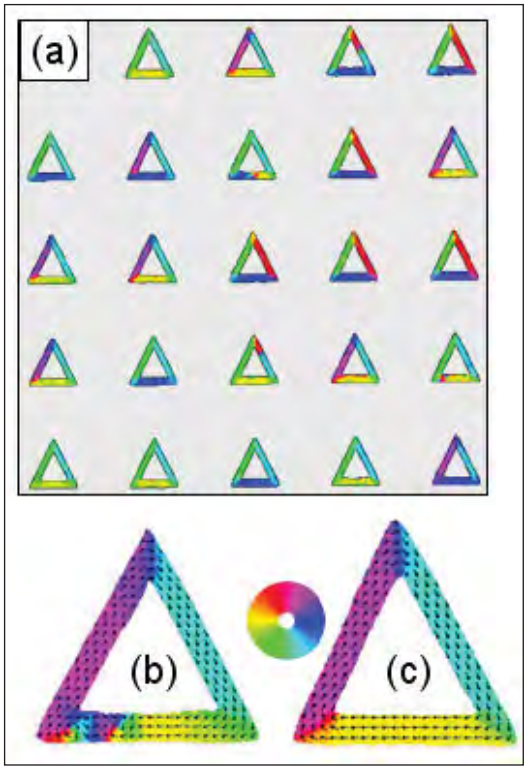

Figure 2. Magnetization (direction given by color wheel) of an array of triangular elements for control of magnetic flux quanta in a superconductor.

■ *Spin Momentum Transfer Switching in Magnetic Nanowires:* Current driven domain wall motion offers the exciting prospect of manipulating magnetization in magnetic devices without applying an external magnetic field. As the spin-polarized electrons of an electron current in a ferromagnet pass through a domain wall, there is a torque on the electrons tending to align their spin magnetic moments with the magnetization direction. Conservation of angular momentum requires a reaction torque, known as the spin trans-

fer torque, from the electrons to the magnetization that displaces the domain wall in the direction of electron flow. We have constructed custom sample holders for SEMPA to allow us to image the magnetization in a nanowire while a current is flowing. SEMPA images showing current induced domain wall motion are shown in Fig 3. In the top two panels, (a) and (b), the vortex wall is "pinned" and there is no change on increasing the current from 0 to 4 mA. In Fig. 3 (c), when 5 mA is applied, the wall is seen to have moved to the left in the direction of electron flow. The wall makes a large jump about 80 % of the way through the image which is scanned from top to bottom. The image (d) taken immediately after (c) shows that the wall has moved to the left to be stopped by the next pinning site. Not much is known about the pinning sites, but it is thought that pinning can be caused by structural defects or chemical inhomogeneities. At present, when pinning sites dominate the domain wall motion, the wall moves from one randomly located pinning site to the next. If the extrinsic defects that cause pinning can be eliminated or controlled such that they can be tailored to do a particular job, current induced domain wall motion could have wide applicability in spintronic devices.

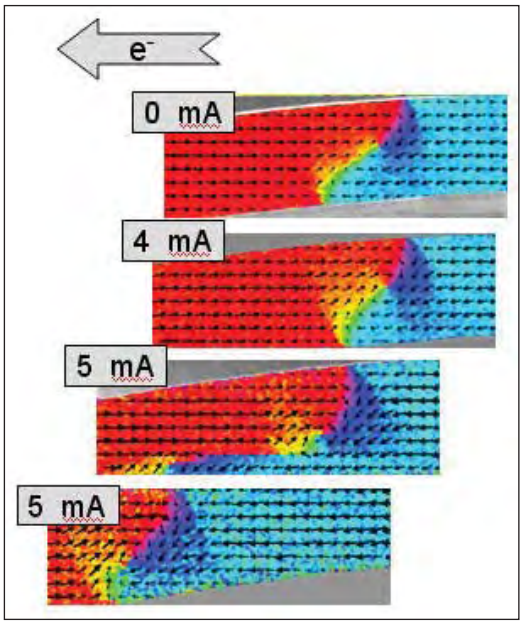

Figure 3. SEMPA images showing the current induced displacement of a vortex domain wall.

Collaborations

IBM, MRAM device imaging and thermal induced noise in tunnel-junction based MRAM devices.

Freescale Semiconductor, MRAM device imaging and incorporating magnetic tunnel junctions into MRAM devices.

Hitachi Global Storage Technologies, high-speed switching in all-metallic MRAM devices.

Seagate Technologies, phase-locking mechanisms in spintronic microwave oscillator arrays.

U. S. Army Research Laboratory, delivery of magnetic nanoscale spin wave oscillators.

U.S. Army Research Laboratory, imaging magnetic sensors.

Future Opportunities

Nanoscale spintronic devices also provide an opportunity for the development of dense non-volatile memory elements as well as new spin-enabled nanoscale microwave devices, such as microwave sources and mixers for timing, communications, and spectral analysis applications. In addition, they also provide one potential avenue towards replacing/augmenting conventional CMOS devices in the deep nanometer regime. As such, we expect that spintronic devices hold the potential to have a great impact on the semiconductor industry, particularly as device dimensions shrink into the nanoscale. The goal of this project is to provide the fundamental metrology and measurements to enable the development of this wide range of devices and applications.

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W. C. Uhlig and J. Unguris, *"Size Dependent Transition from Shape to Exchange Dominated Magnetic Nanostructures in Patterned Zigzags,"* Journal of Applied Physics **99**, 08G302 (2006).

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BioElectronics Metrology

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M. Gaitan

Goals

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal over the next five years is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

Customer Needs

Cell-based assays are a primary tool used by the pharmaceutical industry to measure therapeutic drug efficacy and cytotoxicity. These time-consuming and labor-intensive assays currently involve millions of cells in each culture reservoir. This leads to some inherent measurement biases since the collective response only represents the average for the whole population and, for example, cells at different stages of development will respond differently to stimuli. A true paradigm shift is to utilize micro- and nano-fabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS. Single-cell assays will isolate the parameters affecting cell response and allow the various subpopulations present in bulk cultures to be distinguished. Single-cell assays, when multiplexed, will allow for more rapid identification of drugs and drug targets.

Technical Strategy

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in-vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, in varied buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in-vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We focused our initial research efforts on the study of retinal (neuronal) cells, and currently, we are working with other mammalian cells such as fibroblasts (NIH-3T3), epithelial cells and sperm cells.

DELIVERABLES:

- Develop an array of micro-electrochemical cells and methods to pattern cells on the array for single-cell electrochemical measurements. 4Q 2007
- Develop an array of microelectrodes for impedance-based measurements of cell growth and response. 3Q 2008
- Investigate the feasibility of using microelectrodes for cytotoxicity measurements. 4Q 2008
- Develop an electronic-based method, using microwave heating, for on-chip DNA amplification. 2Q 2008
- Characterize low sensitive field effect transistor (ISFET) -based measurements of pH in a microfluidic network by referencing to a pH determination using a fluorescent dye. 1Q 2008

Accomplishments

■ We developed a method to monitor NIH-3T3 fibroblast cell growth on gold electrodes using impedance spectroscopy. In this measurement technique, individual cells are represented as resistive and capacitive elements, which increase the impedance of the system as the number of cells increase. The two-electrode system was fabricated using photolithographic techniques and is comprised of thin-film gold electrodes with an underlying TiW adhesion layer. The system was then passivated with an oxide layer, which was etched through to define and expose the electrode active areas. Fibroblast cells (NIH-3T3) were able to grow directly onto the gold surface, and as they adhered and multiplied, the impedance of the system increased. Cells preferentially grew on the bare gold surface and not on the oxide. However, the oxide surface can be rendered biocompatible with the use of polyelectrolyte multilayers (PEMs), leading to successful measurements of cell growth with impedance spectroscopy (Fig. 1). Thus, the fabricated cell confluence detector demonstrates the ability to monitor cell adhesion and growth with impedance measurements. Future work will focus on the use of this system to monitor cytotoxic effects, of a variety of chemicals, using impedance spectroscopy to detect cell detachment from the surface.

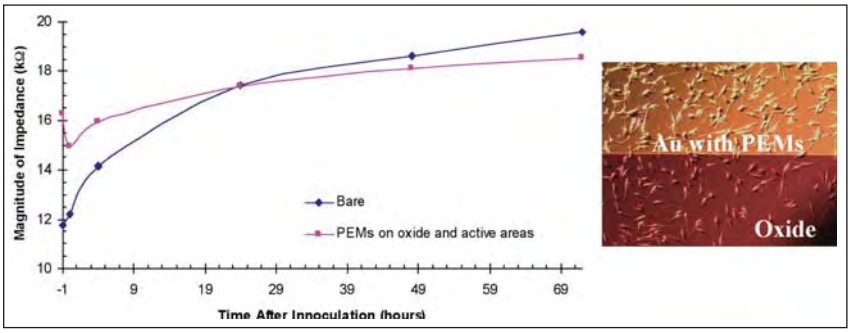

Figure 1. (Left) Graph shows the impedance measurements taken over time as the cells grow on either a bare gold surface or a PEMs-treated surface. (Right panel) NIH-3T3 fibroblast cells growing on a PEMs-modified surface. The polycation used to promote cell adhesion is poly(allylamine hydrochloride).

■ We designed and fabricated a microchip, called mH+, which enables us to study the metrology problems associated with pH determination within planar microfluidic networks, *e.g.* Lab-on-a-Chip (LOC) systems. The work was motivated by the realization that LOC systems might enjoy more widespread commercialization if reliable and accurate electronic chemical sensors are more closely integrated with the microfluidic networks.

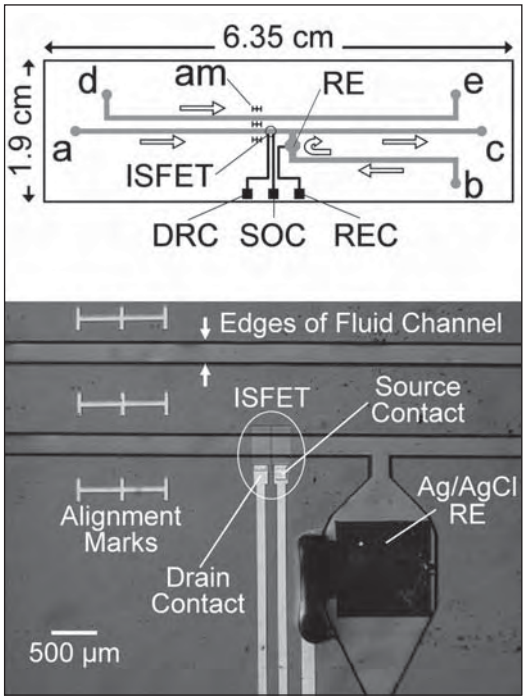

Figure 2. (Top panel) Schematic of mH+ Layout. Overall chip dimensions are as indicated however other features are not shown to scale. The gray lines indicate flow channels molded into PDMS, 280 µm wide by 50 µm high. Arrows indicate the direction of fluid flow. a) test solution inlet, b) reference solution inlet, c) main outlet, d) blank inlet, e) blank outlet, am) alignment mark, RE) on-chip Ag/AgCl quasi-reference electrode, REC) reference electrode contact, DRC) electrical contact to ISFET drain, SOC) electrical contact to ISFET source. (Bottom panel) Photograph of sensing region of the mH+ device, scale as indicated. The ISFET is visible near the center of the figure, while the Ag/AgCl quasi-reference electrode appears in the lower right portion of the figure. Alignment marks and electrical contacts to the ISFET and reference electrode are made of gold.

The mH+ chip comprised 1) an ion-sensitive field-effect transistor (ISFET) fabricated on a silicon substrate, 2) an on-chip Ag/AgCl quasi-reference electrode (RE), and 3) a microfluidic network molded in the transparent elastomer, poly(dimethylsiloxane) (PDMS) (Fig. 2). Thus, both ion-sensitive field-effect transistor (ISFET)-based and fluorescence intensity (FI)-based pH measurements were conducted simultaneously with the mH+ chip. Since two independent pH measurements are used on the same device, the mH+ chip can be used to quantitate the accuracy and precision of microfluidic pH determinations. The utility of the mH+ chip was demonstrated with comparisons of the dynamic range and flow rate dependence of the ISFET-based and FI-based pH measurements. Additionally, ISFET-based measurements clearly resolved step changes in pH as small as 0.26 pH unit in flowing solution. Sample plugs of less than 100 microliters were needed for the measurements.

■ A method for fabricating Ag/AgCl planar microelectrodes for microfluidic applications is presented. Micro-reference electrodes enable accurate potentiometric measurements with miniaturized chemical sensors, but such electrodes often exhibit very limited lifetimes. Our goal is to construct Ag/AgCl microelectrodes reliably with improved potential stability that are compatible with surface mounted microfluidic channels. Electrodes with geometric surface areas greater than or equal to 100 square micrometers were fabricated individually and in an array format by electroplating silver, greater than one micrometer thickness, onto photolithographically patterned thin-film metal electrodes (Fig. 3, left panel). The surface of the electroplated silver was chemically oxidized to silver chloride to form Ag/AgCl microreference electrodes. Characterization results showed that Ag/AgCl microelectrodes produced by this fabrication method exhibit increased stability compared with many devices previously reported. Electrochemical impedance spectroscopy allowed device specific parameters to be extracted from an equivalent circuit model, and these parameters were used to describe the performance of the microelectrodes in a microfluidic channel. Thus, stable Ag/AgCl microelectrodes, fabricated with a combination of photolithographic techniques and electroplating, were demonstrated to have utility for electrochemical analysis within microfluidic systems.

■ Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (μTAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). Our new approach for temperature cycling of microfluidic systems is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel (Fig. 3, right panel). This approach will have application to microwave assisted chemistries, which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibition of more uniform heating profiles. Recently, we have demonstrated, in a different microchip format, the use of microwave heating for the amplification of human DNA (PCR). We are currently working towards the integration

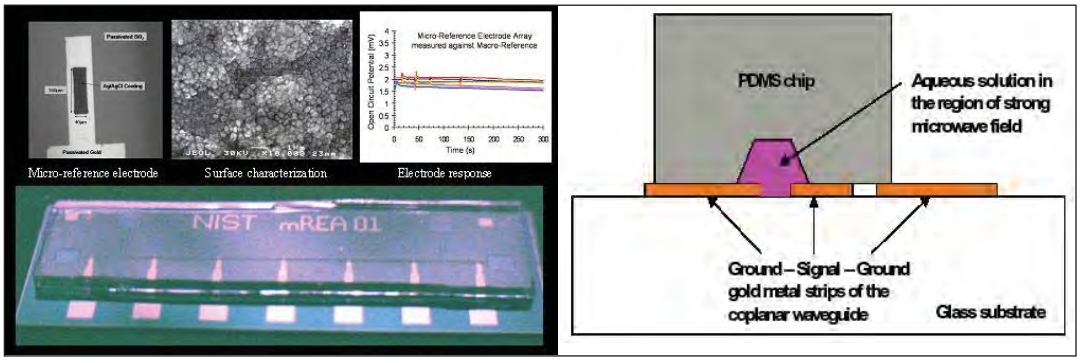

Figure 3. Photographs (left panel) of the NIST micro reference electrode array (mREA) and close-up photo of an Ag/AgCl planar microelectrode, surface, and test. The right panel is a drawing of a fluidic microwave heating assembly showing a gold coplanar transmission line patterned on glass with a poly(dimethylsiloxane) microchannel bonded over it.

of other processes, such as cell lysis and DNA extraction, into a microfluidic system.

■ We have integrated electrodes within microfluidic devices to carry out a.c. dielectrophoresis. In this trapping technique, electric fields polarize cells inducing electrostatic forces, which trap the cells against the electrode edges. We have been able to trap cells suspended from bulk cultures within microchannels when flowed past integrated, energized electrodes. We have observed that more than 85 % of cells passing the electrodes were trapped. On the other hand, when electrodes were deactivated, about 70 % of the cells were subsequently detached by solution flow. Deposition of PEMs on the electrodes renders an adhesion layer to further cell attachment. Trapping experiments carried out after PEMs were deposited over the electrodes showed that all immobilized cells remained adherent after the electrodes were deactivated. We have been using a.c. dielectrophoresis to array cells within a microfluidic channel perpendicular to flow.

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System Design and Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution poses additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing integrated circuit (IC) contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.

METROLOGY FOR SYSTEM-ON-A-CHIP (SOC)

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M. Y. Afridi

GOALS

One of the key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry is the develop-ment of measurement methods and standards for characterizing embedded-sensor (ES) Virtual Components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying embedded-sensor (ES) virtual-components (VCs) compatible with the System-on-a-Chip (SoC) integration methodology used for digital IC design.

This NIST effort will enable ES-VCs to be included in SoC CAD libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated, low-cost, smart homeland security and envi-ronmental sensor systems. One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS-based (MicroElectroMechanical System) VCs into SoCs.

The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, testing standards, verification standards and high-level models of system components. The NIST MEMS-based integrated gas-sensing VC is used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies is used to facilitate the adoption of these MT-VCs into new Home-land Security and industrial applications. Compatibility with the IEEE 1451 set of sensor network standards is supported by the Department of Homeland Security.

CUSTOMER NEEDS

Recent advances in high density CMOS integration and the ability to co-integrate MEMS-based sensor devices enables cost effective complex system designs fabricated on a single chip. The need for standards arises when the system-on-a-chip is designed using IP (Intellectual Property) cores from multiple vendors. These cores must be compatible for design success, thus demanding standards in the area of interoperable interfaces, models and verifica-tion strategies for multi-technology SoC designs.

The SoC design challenges include managing increasing system complexity, achieving system-level verification, and bridging the separate disciplines of system architecture and chip design. These challenges are being overcome with the use of platform-based design approaches that emphasize design reuse, *i.e.* the development of ES-VCs that can be used as cost-effective building blocks for SoC devices, and standards for ES-VC IP interoperability with the SoC design flow.

The direct customers for this infrastructure building will be the makers of system design software, ES-SoC IP de-signers, SoC manufacturers and systems designers. This is generally recognized by the chip designers, manufactur-ers, and EDA tool developers:

"What is the most recent development that promises to truly enable a system on a chip? It is the ability to combine CMOS and MEMS structures into one process flow."

Randy Frank and Dave Zehrbach, Motorola, in *Sensors Online*, 1998

"Definitely, System-on-a-chip is the driving paradigm in our space, and there are some fundamental differences in culture and engineering mentality as well as some new technical skills that need to be developed in engineering. At the highest level, system-on-a-chip implies that you need to think like a system designer but implement like a chip designer, and those traditionally have been different disciplines..."

Shane Robison, Executive Vice President of Engineering, Cadence Design Systems, Inc. EDAcafe.com

TECHNICAL STRATEGY

1. To successfully develop ES-VCs for SoC design methodology, the first step in this multi-step process is to de-velop the ability to make the ES-VC devices via a standard CMOS compatible process. To exercise this capability we have chosen a MEMS microhotplate based embedded gas-sensor, including operational amplifiers, decoders, and an analog-to-digital converter (ADC), and a microcontroller for control and data processing.

"... SoC is the driver for convergence of multiple technologies not only in the same system package but also potentially in the same manufacturing process."

The International Technology Roadmap for Semiconductors, 2003.

"… the trend toward digitisation notwithstanding, the analogue content of SOCs is likely to increase."

Ron Wilson, Electronic Design News (EDN), 2006

2. The second step is to make ES-VCs compatible with the standard digital SoC design methodology. This ap-proach will require ES-VC to incorporate digital interface circuitry and to have the DFT/BIST (Design For Test/ Built-In Self Test) functionality required by SoC standards. To facilitate this approach we will develop methodolo-gies and standards for adding digital shells to ES-VCs and demonstrate them on the gas-sensor VC described above.

DELIVERABLES: Design and fabricate an improved version of the previously fabricated fully digital gas-sensor VC in a standard CMOS 0.5- micron technology to demonstrate a standard digital interface and SoC Design-For-Test functionality. 2Q 2008

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level models (in SystemC/ HDL) exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ES-VCs is at best poorly developed. To address this need, high-level models are being developed for ES-VCs using Analog and Digital Hardware Description Languages and higher-level system description languages such as SystemC. We are also developing methodologies to validate these models. The digital systems industry has standards set by or-ganizations such as OCP-IP, VSIA and OSCI to foster large-scale interchange and interoperability of modular digi-tal IP, and we believe that such standards in ES-VC field are a key factor for the growth of an ES-VC IP industry.

DELIVERABLES: Compare high-level model simulation results for microhotplate-based gas-sensor ES-VCs with measured data from a fully digital ES-VC. 1Q 2009

4. The synthesis process is well defined for the digital SoC design and is well supported by a large number of design libraries. Currently the libraries, methodology, and standards for ES-VC synthesis do not exist. We are developing standards and metrologies for ES-VCs that will be compatible with standard digital synthesis tools.

DELIVERABLES: Develop methodology and standards to allow ES-VC to be syntheses by standard MT-synthesis tools and demonstrate their viability via our microhotplate gas-sensor VC. 2Q 2008

5. Scaling digital circuitry is a key capability used by digital designers to reduce costs and ensure compatibility with different fabrication technologies. Since most systems that would use ES-VCs will be predominantly digital, it is important that there be an equivalent scaling capability for the ES-VCs. To address the need for scaling ES-VCs, we are developing metrologies for digital-compatible scaling processes.

DELIVERABLES: Develop methodologies and standards for an equivalent ES-VC scaling approach and demonstrate its viability via our microhotplate gas-sensor technology. 4Q 2007

6. The testability of ES-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use BIST techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ES-VCs and interface with them via the digital shell.

DELIVERABLES: Develop methodologies for built-in self test of ES-VC devices and demonstrate their viability via our microhotplate gas-sensor technology. 4Q 2007

7. Beside a gas sensor VC, a gas-sensor SoC requires quantification, classification, communication, and control capability. These functional requirements can easily be implemented by an on-chip microcontroller with appropriate algorithms and protocols.

DELIVERABLES: Demonstrate a gas-sensor VC interfaced with an 8051 microcontroller that is IEEE 1451 sensor-network standard compliant. 4Q 2007

NIST is a natural home for this work because NIST has advanced measurement capabilities across the spectrum of sensor technologies.

Accomplishments

- A monolithic micro-gas-sensor system was successfully designed and fabricated in a standard 1.5 μm CMOS process (Fig. 1). The gas-sensor system incorporated an array of four microhotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. Digital decoders selected individual elements of the sensor array and an operational amplifier monitored sensing film conductance. Detection of gas concentra-tions in the 100 parts-per-billion range was achieved. This represented an improvement in sensitivity of two orders of magnitude over existing MEMS-based microhotplate gas-sensors.

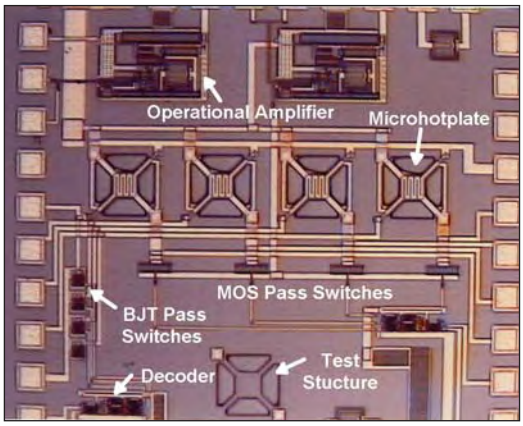

Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

■ Investigated existing and emerging SoC design methodologies, and adapted digital SoC design tool-flow to enable integration of mixed-signal MEMS VCs.

■ A four element gas-sensor VC was successfully designed, fabricated and electrically characterized to demon-strate that the design approach was compatible with SoC design methodology. The performance of the 8-bit ADC exceeded the gas-sensor VC design requirements (Fig. 2).

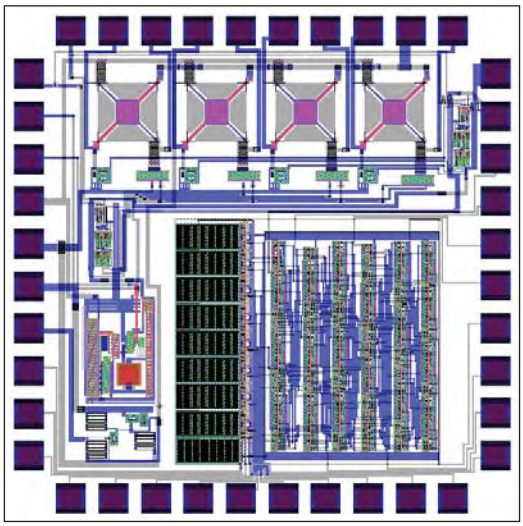

Figure 2. Layout of the four element gas-sensor VC with analog-to-digital control.

■ Electrostatic discharge (ESD) protection structures were added to the gas-sensor and successfully tested These ESD test structures are based on multi-finger thyristor-type devices and are designed to achieve optimum perform-ance and reduced area (Fig. 3).

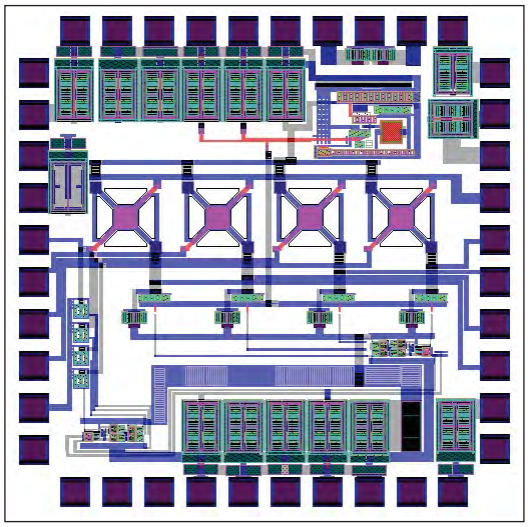

Figure 3. Layout of the four element gas-sensor VC with electrostatic discharge (EDS) protection circuitry.

■ A new post-process etching technique was developed to integrate MEMS devices with standard submicron CMOS processes and a new microhotplate design that scales with standard CMOS structures and voltage levels (Fig. 4). This will enable co-integration of MEMS sensor devices with high density submicron digital systems using cost effective standard CMOS foundries. The submicron gas-sensor test chip was characterized. Characterization data showed the new scalable microhotplate will provide the temperature required for gas-sensor operation at 3.3V.

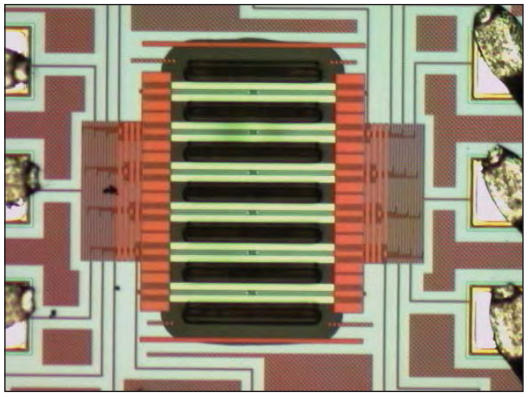

Figure 4. New microhotplate design implemented in standard submicron CMOS technology.

■ Methodologies for designing digital interface shell functionality for ES-VCs were developed and demonstrated by designing the gas sensor SoC architecture.

■ A high-level model of the microhotplate gas sensor ES-VC was developed. A HDL-based microcontroller core was synthesized for a 0.25-micron standard CMOS fabrication process. High-speed SystemC models of the micro-controller and microhotplate were developed to facilitate SoC software design and protocol development. This is the first time a MEMS device has been modeled in systemC and the results demonstrated the importance of including MEMS device models in high level system modeling

■ Microhotplate-based gas-sensor yield was improved by adopting a new chromium etchant.

■ A computer-controlled gas-delivery system was designed, assembled, and tested. The gas delivery protocols for calibrating the micro-hotplate-based gas sensors were designed and implemented.

■ A submicron-microhotplate test-structure chip was designed to compare the performance of different CMOS compatible temperature sensors and to measure the contact resistance between different types of post-processed gas sensor electrodes. This chip also supports the extraction of more accurate microhotplate thermal-model parameters (Fig. 5).

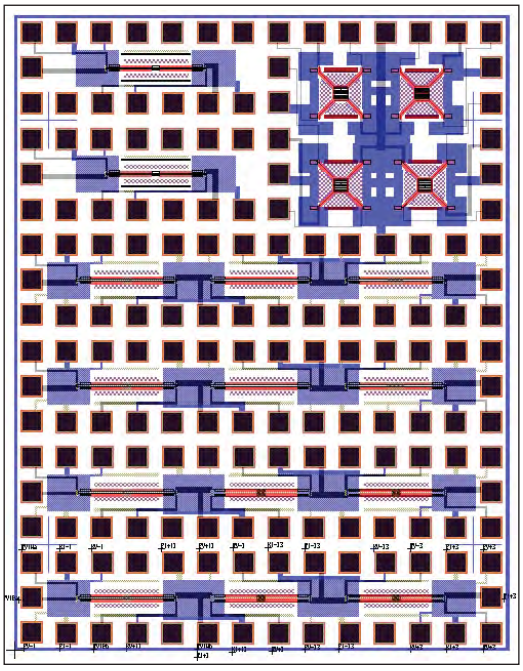

Figure 5. Layout of new microhotplate test-structure chip with different types of temperature sensors and four point electrodes for gas-sensor film contact-resistance studies.

■ An 8051 IP core was synthesized and fabricated in the MOSIS-TSMC 0.25 micron standard CMOS process (Fig. 6). The chip design is compatible with the IEEE1451 sensor network communication standards. Bridge type new microhotplate test structures were also included on the same chip to test the compatibility of our current post process-ing steps with this sub-micron CMOS process.

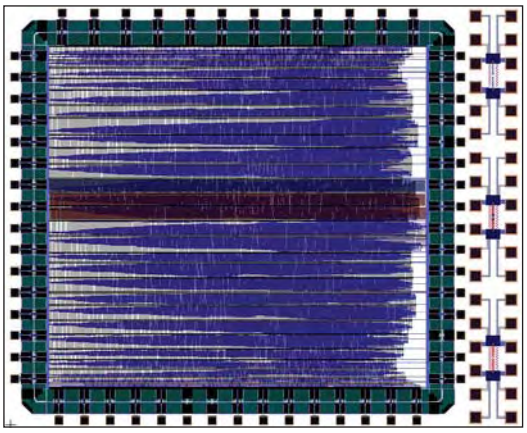

Figure 6. Microcontroller and new microhotplate test-structures Layout.

■ A prototype gas-sensor VC platform was designed and fabricated for the first time in the MOSIS-AMI 0.5 micron standard CMOS process (Fig. 7). The design includes bridge type microhotplate structures, 8-bit DAC, 10-bit ADC, heater drivers, analogue and digital multiplexers, and operational amplifiers. The design has a fully digital interface to control and measure the analogue signals associated with gas sensor, and a complementary analogue interface for debugging.

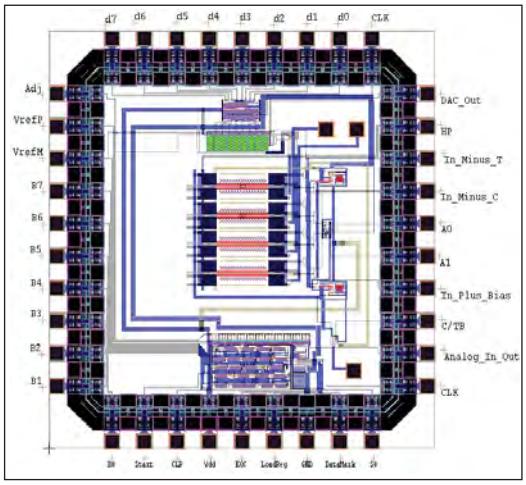

Figure 7. Gas-sensor VC layout for submicron CMOS fabrication.

■ Project personnel collaborated with MEL to incorporate IEEE 1451 network sensor standards compatibility into the gas-sensor SoC. Transducer Electronic Data Sheets (TEDS) were written for the TEDS that are required by the standard. A gas-sensor SoC Transducer Interface Module (TIM) was emulated on a laptop and verified to comply with an essential subset of the IEEE 1451 command set that were issued over an RS232 link to an MEL laptop.

Recognition

2005 George Abraham Outstanding Paper Award:

M. Y. Afridi, A. Hefner, C. Ellenwood, R. Cavicchi, and S. Semancik "Characterization System for Embedded Gas-sensor Systems-on-a-Chip" GOMACTECH 2005, pp. 94-97, 2005.

Recent Publications

A. Varma, M. Y. Afridi, A. Akturk, P. Klein, A. Hefner and B. Jacob, "Modeling Heterogeneous Systems With SystemC: A Digital/MEMS Case Study," in Proceedings of the ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES '06), pp 54-64, Seoul, Korea, October 2006.

J. Geist, M. Y. Afridi, A. Varma and A. Hefner, "Simple Thermal-Efficiency model for CMOS-Microhotplate Design," in Journal of Research at NIST, Vol 111(3), pp. 243, 2006.

M. Y. Afridi, A. Hefner, J. Geist, C. Ellenwood, A. Varma, B. Jacob, "Microhotplate-Based Sensor Platform for Submicron SoC Designs" IEEE International Semiconductor Device Research Symposium (ISDRS), pp. 500-501 2005.

Yaqub Afridi, Allen Hefner, Colleen Ellenwood, Richard Cavicchi, Stephen Semancik "Characterization System for Embedded Gas-sensor Systems-on-a-Chip" GOMACTECH 2005, pp. 94-97, 2005.

Javier A. Salcedo, Juin J. Liou, Muhammad Y. Afridi, Allen R. Hefner, and Ankush Varma "Electrostatic Discharge Protection for Embedded-sensor System-on-a-Chip" (Abs. 2587) 26th meeting of The Electrochemical Society (ECS) October, 2004.

M. Y. Afridi , A. R. Hefner Jr., D. W. Berning, C. H. Ellenwood, A. Varma, B. Jacob, S. Semancik, "MEMS-based embedded sensor virtual components for system-on-a-chip (SoC)," Solid State Electronics, Vol. 48, pp. 1777-1781 (24-JUN-2004).

M. Y. Afridi, A. Hefner, D. Berning, C. Ellenwood, A. Varma, B. Jacob, S. Semancik, "MEMS-Based Embedded Sensor Virtual Components for SoC" IEEE International Semiconductor Device Research Symposium (ISDRS), pp. 500-501 2003.

Muhammad Y. Afridi, John S. Suehle, Mona E. Zaghloul, David W. Berning, Allen R. Hefner, Richard E. Cavicchi, Steven Semancik, Christo-pher B. Montgomery, and Charles J. Taylor, "A Monolithic CMOS Microhotplate-Based Gas Sensor System," IEEE Sensors Journal, vol. 2, no. 6, pp. 644-655, Dec. 2002.

M. Y. Afridi, J. S. Suehle, M. E. Zaghloul, D. W. Berning, A. R. Hefner, S. Semancik, R. E. Cavicchi, "A MONOLITHIC IMPLEMENTATION OF INTERFACE CIRCUITRY FOR CMOS COMPATIBLE GAS_SENSOR SYSTEM" Proceedings of the IEEE Internal Symposium on Circuit and Systems, pp. II 732 – 735, (May 2002).

At-Speed Test of Digital Integrated Circuits

Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes and developing scanning probe microscopes (SPMs) capable of precisely positioning field probes above the surface of the integrated circuit.

Customer Needs

In the device debug and characterization world, a key challenge is the development of diagnostic tools, particularly for timing information. The limitations in the current PICA/time-resolved photoemission detector technology point to the need for radically different methodologies (2005 ITRS Test and Test Equipment Section, page 9). Traditional forms of IC contact probing (fine-pitch probe cards and RF probes) technology require large contact pads incompatible with the operation and economic constraints of modern IC designs (2005 ITRS, Test and Test Equipment Section, page 24). The 2005 ITRS concludes that micro-positioner and atomic-force-microscope-based probing will be required at each roadmap generation to probe minimum sized transistors (2005 ITRS, Test and Test Equipment Section, page 9).

We are developing alternative probing approaches that use high-impedance probes, non-contact probes, and atomic-force microscopes that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit. Figure 1 shows a result of the high-speed metrology we have developed, an on-chip waveform measurement to 200 GHz.

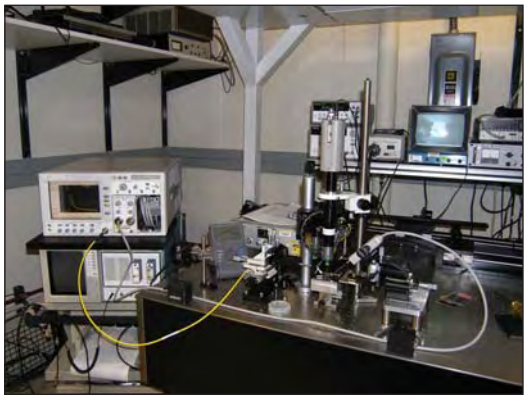

Figure 1. Three on-chip waveform measurements performed with our electro-optic sampling system.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we have constructed a universal SPM test bed for these probes. We are applying our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we plan to tie our metrology back to fully characterized electro-optic sampling measurements.

The 2005 ITRS notes that 10s or 100s of picoseconds of delay are now critical, and that there is no instrument available that simultaneously satisfies the noise floor, analog bandwidth, and test time requirements for high performance interfaces (2005 ITRS, Test and Test Equipment Section, pages 7 and 30). To address this, we are also working on methods for calibrating and correcting imperfections in waveform measurement equipment that cause distorted or blurred measurements. These effects include instrument response, impedance

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J. Moreland
P. Kabos
P. Hale

"As electronic devices shrink into the nanometer size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D.
Intel Corp.

mismatch, multiple reflections, dispersion, timebase distortion, jitter, and drift. After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. Traceability for frequency response is provided to 110 GHz (in coax) and beyond (on wafer) through the NIST electro-optic sampling system. Our calibration strategy is independent of the particular signals being measured and is applicable to digital, RF/microwave, and mixed signal systems, enabling the single platform measurement solutions called for in the 2005 ITRS, Test and Test Equipment Section, page 36.

DELIVERABLES:

- Fabricate and verify functionality to 50 GHz of generator circuits based on photoconductive switches suitable for the construction of portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales. 4Q 2007
- Construct a fiber optic based high speed scanning probe system based on magneto-optic Kerr effect and demonstrate capability of micrometer spatial resolution. 4Q 2007
- Develop a calibration for the time-domain insertion delay of a coaxial cable with sub-picosecond resolution (limited by connector repeatability). 4Q 2007

Accomplishments

■ We have demonstrated a novel frequency-domain method for measuring time-domain delay of dispersive calibration artifacts for differential delay. This frequency-domain approach can also account for pulse shape and source and load impedance effects. We have also demonstrated a method to propagate uncertainty in the NIST Timebase Calibration Software through to various pulse parameters and have demonstrated differential delay calibrations of a dispersive calibration artifact with < 1 ps standard uncertainty.

■ We have developed, fabricated, and tested a noninvasive AFM scanning probe for measuring local microwave power.

■ We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements.

■ We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.

■ We have constructed an SPM universal test bed.

■ We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.

■ We have developed a procedure for testing high-impedance probes directly on our electrooptic sampling system. This system has a calibrated bandwidth of 200 GHz.

■ We have demonstrated a method for correcting oscilloscope timebase jitter, drift, and distortion.

■ We have fabricated fast photoconductive switches and demonstrated a rise time of better than 5 ps, largely exceeding our goal of constructing generator chips useable to 50 GHz. We will use these to construct a portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales, Fig. 2.

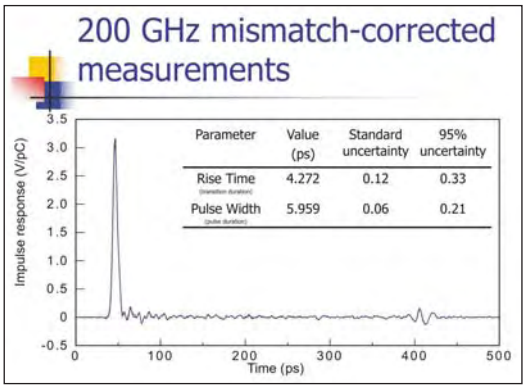

Figure 2. Measurement system used to verify the functionality of our photoconductive switches.

■ We developed the fabrication process for creating the MEMS chips with integrated 45-degree mirrors and trenches for fiber alignment, Fig. 3.

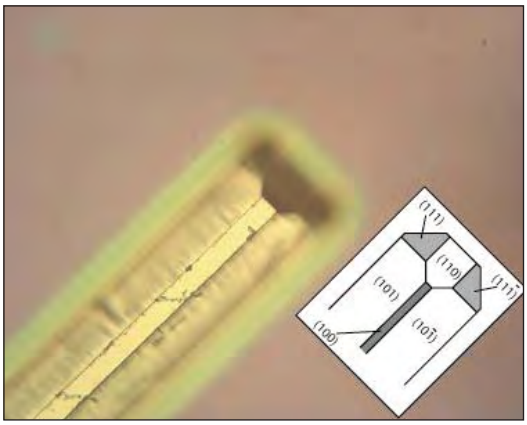

Figure 3. The Fiber-optic trench with integrated 45-degree mirror.

■ We assembled the fiber optic interferometer for the measurement of the deflection of the cantilevers including the thermal feedback control.

Recent Publications

Simone Lee, T. Mitch Wallis, John Moreland, Pavel Kabos, and Y. C. Lee, *"Asymmetric Dielectric Trilayer Cantilever Probe for Calorimetric High-Frequency Field Imaging,"* IEEE JMEMS 16, pp. 78 -86, (2007).

T. S. Clement, P. D. Hale, D. F. Williams, C. M. Wang, A. Dienstfrey, and D. A. Keenan, *"Calibration of sampling oscilloscopes with high-speed diodes,"* accepted for publication in IEEE Trans. Microwave Theory and Tech., 2006.

A. Dienstfrey, P. D. Hale, D. A. Keenan, T. S. Clement, and D. F. Williams, *"Minimum-phase calibration of sampling oscilloscopes,"* accepted for publication in IEEE Trans. Microwave Theory and Tech., 2006.

D. F. Williams, A. Lewandowski, T. S. Clement, C. M. Wang, P. D. Hale, J. M. Morgan, D. A. Keenan, and A. Dienstfrey, *"Covariance-based uncertainty analysis of the NIST electro-optic sampling system,"* IEEE Trans. Microwave Theory and Tech., Jan. 2006.

D. F. Williams, H. Khenissi, F. Ndagijimana, K. A. Remley, J. P. Dunsmore, P. D. Hale, C. M. Wang, and T. S. Clement, *"Sampling-Oscilloscope Measurement of a Microwave Mixer with Single-Digit Phase Accuracy,"* IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 3, March 2006.

P. D. Hale, C. M. Wang, D. F. Williams, K. A. Remley, and J. Wepman, *"Compensation of random and systematic timing errors in sampling Oscilloscopes,"* IEEE Transactions on Instrumentation and Measurement, Vol. 55, No.6, December 2006.

S. Lee, Y. C. Lee, T. M. Wallis, J. Moreland, and P. Kabos, *"Near field imaging of high-frequency fields with calorimetric cantilever probes,"* Journal of Applied Physics, 99, pp. 08H306-1-08H306-3, (2006).

D. F. Williams, P. D. Hale, T. S. Clement, and J. M. Morgan, *"Calibrated 200 GHz Waveform Measurement,"* IEEE Trans. Microwave Theory and Tech., April, 2005.

T. M. Wallis, J. Moreland, W. Riddle, and P. Kabos, *"Microwave power imaging with ferromagnetic calorimeter probes on bimaterial cantilevers,"* Journ. of Mag. and Magn. Mater, vol 286, pp. 320-323 (2005).

Thermal Measurements and Packaging Reliability

Goals

Our goal is to provide the microelectronics industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging and on-chip that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens that present a reliability concern to the manufacturer or end-user, or a model system is fabricated in-house. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal — providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allow us to refine the techniques to make them optimally beneficial to industry, and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, which is essential for technology transfer.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (*e.g.*, SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs) and enables the measurement of transient current constriction failure events in RF and high power devices. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for *in situ* measurement of heat transfer performance degradation after various levels of thermal stress such as power cycling, thermal cycling and thermal shock.

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging and interconnects are many and display a variety of thermal responses that are not always compatible. This makes interconnect lines and interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: (1) predicting reliability or operating life of device, (2) measuring material/device thermal properties *in situ*, (3) confirming or determining the operating limits or thermal performance of a device, and (4) validating thermal models for device, chip, and system performance. Thermal measurements on small, <10 μm, structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to "Moore's Law." Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing

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N. Barbosa
A. J. Slifka
A. R. Hefner

"I am writing to let you know that NIST has been of great assistance to Cenymer Corporation, one of our portfolio companies. This portfolio company has developed a novel material. Dr. Andrew Slifka at NIST was able to provide the company with thermal measurements that are critically important to Cenymer as it approaches potential customers. It is great to have NIST in the community as a resource to companies like Cenymer."

Tim Connor
Sequel Venture Partners

the power dissipation and operating temperature. Equally as clear, we must have accurate and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs. System level power reduction strategies are generally recognized by the ITRS 2005 as necessary for the continual advancement of electronic systems at a rate consistent with "Moore's law."

"As the thermal resistances are made smaller and s*maller for high power devices, thermal metrology with better resolution and capabilities is required. For example there is strong need to establish industry wide transient thermal measurement technique standard." ITRS 2005.*

"Power consumption is now the major technical problem facing the semiconductor industry. As feature sizes shrink below 0.1 micron, static power is posing new low-power design challenges. ITRS predicts a decrease in dynamic power per device over time. However, the doubling of on-chip devices every two years would force an increase of current leakage on a per-chip basis." ITRS 2005.

"New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key." 2006 ITRS Update: one of the five "Difficult Interconnect Challenges" for ≥ 32 mm, ITRS Interconnect, p. 2.

"As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion." 2006 ITRS Update: one of the five "Difficult Interconnect Challenges" for ≥ 32 mm, ITRS Interconnect, p. 2.

Technical Strategy

1. We are developing techniques in scanning thermal microscopy, utilizing the AFM (atomic force microscope), which have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What is the interfacial thermal resistance of an alloy/intermetallic interface." The first was answered using the IR microscope; the second has yet to be answered. Determining temperature and temperature distribution at the micron and submicron size scales and additionally in the time domain will aid in determination of failure mechanisms in packages and interconnects.

DELIVERABLES: Evaluate commercially available Scanning Probe Microscope (SPM) tips for thermal SPM. Determine performance for measuring temperatures at and around on-chip interconnects. 4Q 2007

2. Carbon nanotubes have potential in heat-removal applications for microelectronics. Thermal properties show great promise in this area, if production issues can be addressed. We will continue to cooperate with industry by measuring the thermal conductance achieved by newly-developed thermal compounds that incorporate carbon nanotubes.

DELIVERABLES: Measure interfacial thermal resistance of improved carbon nanotube-covered copper and baseline copper materials. 3Q 2007

3. Stress-voiding, electromigration, thermo-mechanical fatigue and other mechanisms that can cause failures in interconnect lines are all accelerated by temperature. Using scanned- thermal-probe microscopy (SThM), we are measuring temperatures of damaged locations on lines and temperature distribution on and around interconnect lines to elucidate failure mechanisms and predict lifetimes. Our current commercial SThM equipment is marginal for this application. We will determine whether any commercially-available sensors are adequate for the task. If so, we will use the technology in our research on commercial films and lines; if not, we will define the improvements needed in the sensors.

DELIVERABLES: Measure lines both temporally and spatially. Use results in our work on thermomechanical stressing and reliability of interconnect lines. 1Q 2008

4. High speed temperature sensitive parameter (TSP) measurements are required for *in situ* evaluation of the heat transport through the interface

of multi-layer package systems. Recently NIST developed a high speed transient thermal impedance system using a TSP for multi-chip power modules. This enables assessment of die attach and DBC isolation attach degradation after thermal cycling and thermal shock stress. This system also enables validation of electro-thermal device models needed for electrical and thermal system design.

DELIVERABLES: Perform thermal cycling and thermal shock stress on DARPA Wide-Bandgap Semiconductor Technology High Power Electronics program (DARPA HPE) devices and American Competitiveness Institute ManTech devices. Use unique NIST high speed, high current TSP system to evaluate die attach and DBC attach integrity before and after thermal stress. 1Q 2008

5. A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high-speed transient thermal image measurements. NIST has modified a commercial IR system to enable measurement of high speed temperature maps of the chip surface with 1-μs temporal resolution and 15 μm spatial resolutions. The NIST system permits the measurement of the chip heat source distribution before the heat diffuses to surrounding regions and enables the measurement of transient heating events such as reduced power IC FUBs (clock gating, dynamic voltage scaling, and Vdd gating), enables the measurement of transient current constriction failure events in RF and high power devices, and measurement of current uniformity in large area power devices.

DELIVERABLES: Improve the spatial resolution of the NIST high-speed transient thermal imaging system from 15 μm to 3 μm while maintaining the 1-μs time resolution. Begin to transfer the NIST capability to commercial instrument manufacturer. 3Q 2008

6. There is a strong need to establish industry wide transient thermal measurement technique standards as described in the 2005 ITRS roadmap. NIST recently developed and tested a transient thermal calibration test structure with 1-μs temporal resolution using micro hotplates with integrated temperature sensors. The set of calibration test structures is now being expanded to develop a prototype IR transient thermal imaging calibration test chip.

DELIVERABLES: Apply micro hotplate transient thermal calibration test structures to evaluate performance of NIST developed 3 μm, 1 μs high-speed transient thermal imaging system. 4Q 2008

7. Dynamic electro-thermal models of semiconductor packages are needed to evaluate the interaction of the electrical system with the thermal management system. NIST first introduced the concept of package and module thermal network component models in the early 1990's and has since used this methodology to develop models for several specific power module packages. Recently, the program manager and contractors of the DARPA HPE program has requested that NIST provide models for the 10 kV, 100 A SiC power models being developed by the DARPA HPE Phase 2 program (device phase) contractors so that the models can be used to design the thermal management and fault mitigation systems for the prototype future naval aircraft carrier Solid State Power Substation being developed by the DARPA HPE Phase 3 (system phase) contractor.

DELIVERABLES: Provide initial thermal network component models needed by DARPA HPE program to develop the prototype future naval aircraft carrier Solid State Power Substation. 4Q 2007

Accomplishments

■ Since there is no commercially available device for calibration of a thermal atomic-force microscope (AFM) probe tip, we developed 6 different designs and evaluated the electrical performance as a function of temperature. We also chose the best design for use with the AFM in both steady-state and transient thermal modes. Figure 1 shows the device.

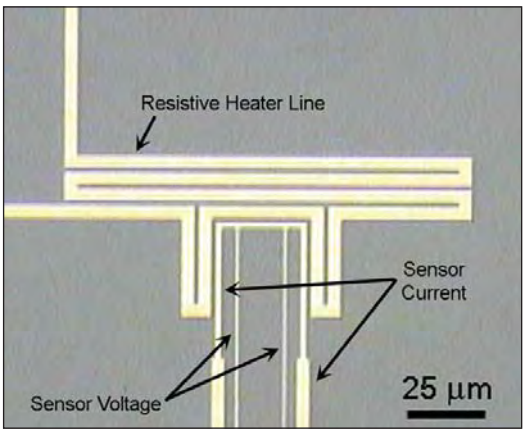

Figure 1. Calibration structure for scanned thermal microscopy. The resistive heater and temperature sensor were fabricated from 300 nm thick aluminum, which allowed for easy fabrication, but limited the maximum operating temperature to several hundred degrees Celsius. The design ensures that the calibration area, located on the sensor structure between the sensor voltage taps, remains at a uniform temperature.

A description of the device has been submitted for publication; the reference is listed below.

The change in resistance as a function of temperature of the sensor can be used to calibrate AFM probe tips. Figure 2 shows the calibration curve for one of the devices.

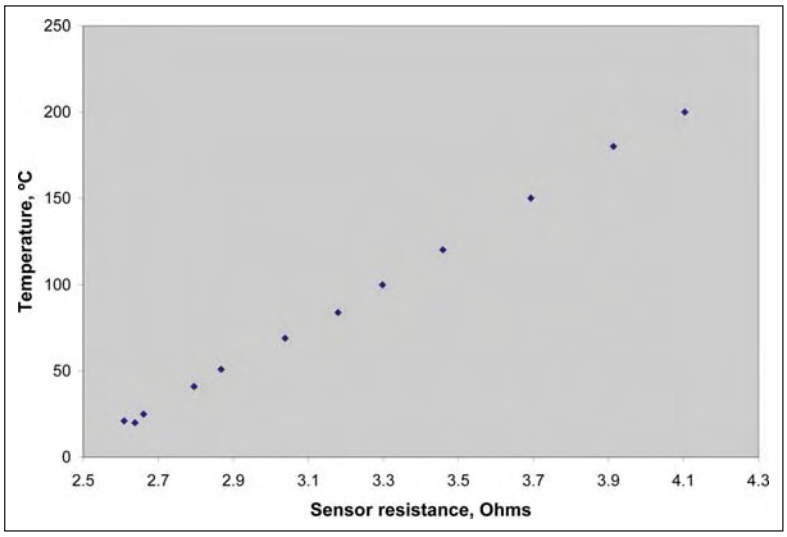

Figure 2. Calibration curve from a NIST microdevice showing device temperature as a function of sensor resistance.

■ Feasibility has been shown of measurements of electronic interconnect lines using the thermal SPM. We have attempted to calibrate the response of the probe tip to temperature, but the measurement is impractical with present equipment.

■ The measurement of thermomechanical fatigue is done in a transient fashion at a rate on the order of 100 Hz. The electronics that control the thermal scanned-probe microscope have specifications from the manufacturer that state that the thermal settling time constant is 350 microseconds due to the thermal mass of the probe tip. Therefore, transient measurements up to 2800 Hz should be possible. To determine feasibility of measuring thermomechanical fatigue, we have made measurements using the thermal probe tip on an interconnect line that was being heated at 100 Hz a.c. Figure 3 shows a plot of data from the thermal microscope in the form of thermal voltage as a function of time.

A calibrated probe tip will allow us to present this data in the form of temperature as a function of time. Two papers were written that include some results: R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, "Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects," presented in April 2006 and accepted for an upcoming issue of *Metallurgical*

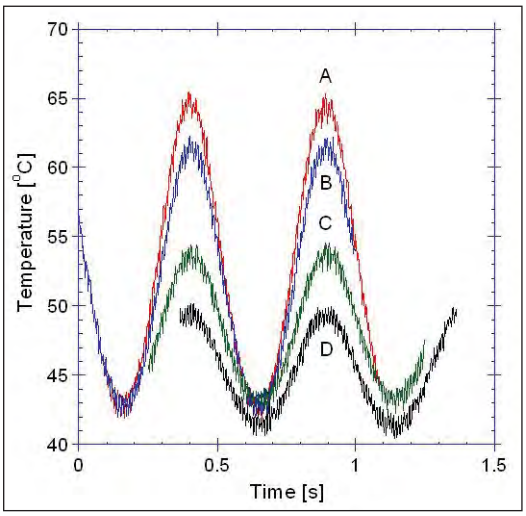

Figure 3. Temperatures obtained at four locations on and near an 8 μm wide line heated by low frequency alternating current. Trace A is at the line center, B is on the line at 2 μm from the center, C is at the line edge, and D is 5 μm away from the line edge.

and Materials Transactions, and R. R. Keller, C. A. Volkert, R. H. Geiss, A. J. Slifka, D. T. Read, N. Barbosa III, and R. Mönig, "Electrical Methods for Mechanical Characterization of Interconnect Thin Films," 2005 Advanced Metallization Conference proceedings.

■ We have been making measurements of carbon nanotube mats grown on copper substrates as a potential replacement for copper-and-thermal-grease heat sinks. Measurements of two copper specimens with thermal grease between all three interfaces was compared with two carbon nanotube (CNT) specimens placed face-to-face, with thermal grease between the measurement plates and copper blank sides at low contact pressure (finger-tight, 555 psi). Figure 4 shows the results. Even at this low contact pressure, before the CNTs

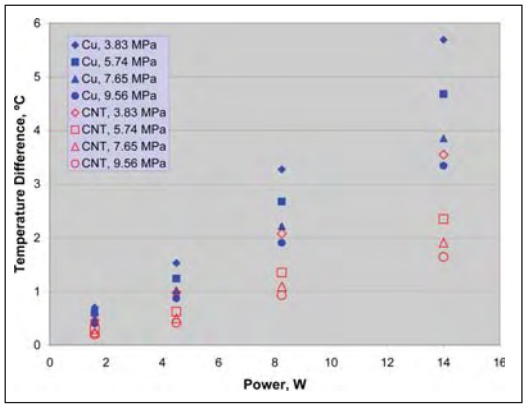

Figure 4. Comparison of temperature differences across thermal-grease-and-copper interfaces and carbon nanotubes.

begin developing large amounts of tube-to-tube contact, the CNT specimens outperform the copper with thermal grease.

■ Development of the high-speed (1 µs) transient thermal imaging system was completed. The acquisition and data analysis capabilities of this system have been extended to include a burst method and to allow frames from different transient movies to be compared more readily. An auto-scaling capability and user definable number of frames have also been added. A thin carbon-black chip coating process was developed to improve sample emissivity without altering the chip surface thermal response time. New thermal microscope hardware has been purchased and installed to enable future upgrade of the high-speed transient thermal imaging system to 3 µm spatial resolution from it's present 15 µm spatial resolution.

■ NIST recently developed and tested a transient thermal calibration test structure with 1 µs temporal resolution using MEMS-based microhotplates with integrated temperature sensors. This specially designed temperature-reference microhotplate structure is calibrated and used to verify the results of the transient IR thermal imaging system. Figure 5 compares the single point IR transient response with the electrically measured transient response of a microhotplate structure for a 20 µs heating pulse.

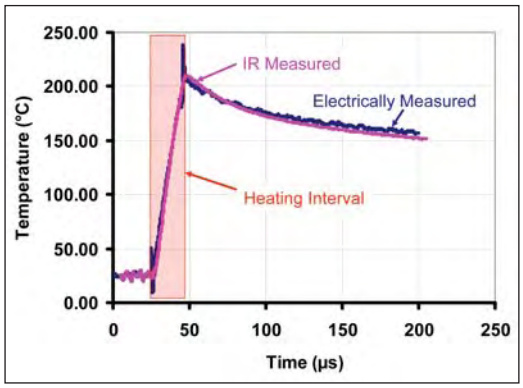

Figure 5. Microhotplate thermal response to a 20 µs heating pulse (as indicated) measured with both IR and electrical methods.

■ As low-degradation rate SiC PiN (power diode made with p-type to intrinsic to n-type semiconductor junctions) diodes are beginning to emerge, the NIST transient thermal imaging system is being used to determine the current uniformity after various levels of stress up to several thousand hours of operation. The pulsed thermal image results show that the current is relatively uniform before degradation and that only 1 % of the chip is conducting all of the current after substantial degradation. Degradation of SiC diodes remains was highly variable as of 2006, as demonstrated in Figs. 6a and 6b. Figures 6a and 6b are current uniformity images of two different SiC 10 kV, 20 A diodes operated at full rated current for 500 hours under forward bias. The diode shown in Fig. 6a demonstrates good current uniformity after 500 hours operation and the diode shown in Fig. 6b demonstrates highly non-uniform current

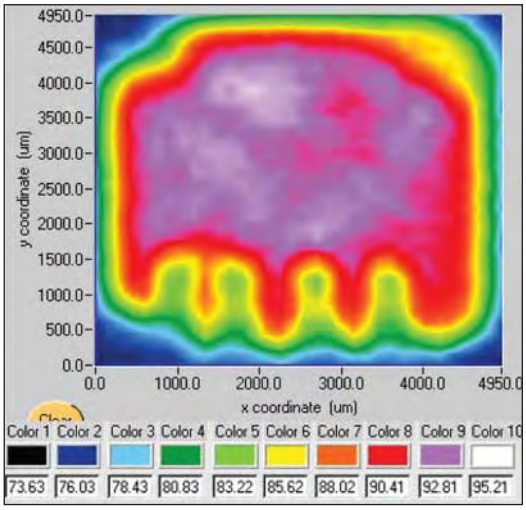

Figure 6a. SiC diode relative temperature uniformity map shows relatively uniform current conduction throughout the chip after 500 hours stress at full current. The four green areas at the lower part of the chip are caused by wire bond shadowing of the thermal radiation.

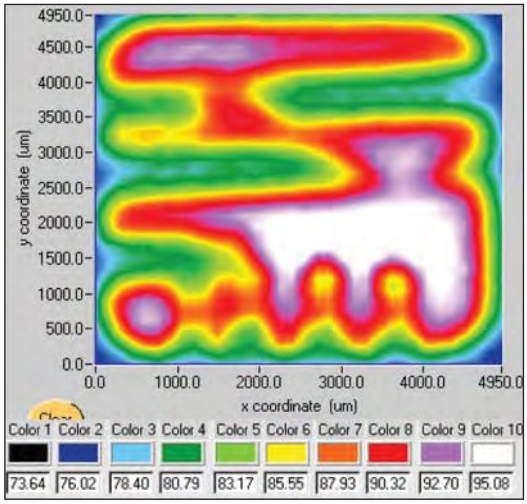

Figure 6b. Relative temperature uniformity map for a similar SiC diode shows highly non uniform current conduction after 500 hours stress at full current. Both of these diodes are mounted on a temperature-controlled heatsink and the background temperature is 75 °C.

conduction after 500 hours operation (only 50 % of device is conducting). NIST has evaluated the current uniformity degradation of numerous SiC PiN diodes samples from 2005 through 2007, providing essential information resulting in the development of "degradation free" SiC power device technology.

- NIST has developed an "*in situ*" method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, V_{GS}, at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter (TSP). This TSP method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module).

- The high-speed TSP method was applied to compare heating response measurements with the thermal models for a commercial high power IGBT half bridge module, a commercial six-pack IGBT module, and a prototype NSF Center for Power Electronic Systems Module. Electro-thermal simulations of a full three-phase inverter have been successfully performed and compared with measured results of the power converter temperature monitors. The NIST high-power, high-speed TSP method has been extended to measure the package cooling performance of 10 kV SiC power MOSFETs being developed by the DARPA HPE program and is being used to aid in the development of packages produced by that program.

- The hardware construction and computer interfacing for the NIST high power rapid thermal cycling/shock test system were completed. This included necessary electronics instruments, flow controllers, high thermal impedance plumbing interfaces, and computer control of air flow rate, water flow rate, and heater power PID temperature controller. The system produces 300 °C thermal cycles with computer programmable temperature rise and fall times (as fast as 10 min rise and fall times are obtained). The rapid thermal cycling/shock test systems are currently being applied to SiC power modules developed by the DARPA HPE program where the NIST high-speed TSP and thermal imaging systems are being used to monitor thermal performance degradation.

Collaborations

University of Nebraska: Kevin Cole

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University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

American Competitiveness Institute (ACI), Navy ManTech center: Barry Thaler

General Electric, Research, Raju, Ravisekhar.

Powerex, Scott Leslie.

Recent Publications

N. Barbosa III and A. J. Slifka, *"Spatially- and Temporally-Resolved Thermal Imaging of Cyclically Heated Interconnects by Use of Scanning Thermal Microscopy (SThM),"* submitted to Microscopy Research and Technique.

Allen R. Hefner and Sharon Beermann-Curtin, *"Status of the DARPA WBST High Power Electronics Program in SiC Device Development and Technology Transition,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2007, March 19-22, 2007

Madelaine Hernández-Mora, Adwoa Akuffo, Colleen Hood, José M. Ortiz-Rodríguez, and Allen Hefner, *"Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability,"* in 2007 IEEE Power Electronics Specialists Conference (PESC), June 2007.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Paper presented at the 2006 TMS Annual Meeting, April 2006. Metallurgical and Materials Transactions (approved publication).

Hefner Jr., A. R., Sei-Hyung, R., Brett, H., Berning, D. W., Hood, C. E., Ortiz-Rodriguez, J. M., Rivera-Lopez, A., Duong, T., Akuffo, A., Hernandez, M., *"Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Devices,"* IEEE Industry Applications Society (IAS) Annual Meeting, October 2006.

R. R. Keller, C. A. Volkert, R. H. Geiss, A. J. Slifka, D. T. Read, N. Barbosa III, and R. Mönig, *"Electrical Methods for Mechanical Characterization of Interconnect Thin Films,"* 2005 Advanced Metallization Conference Proceedings, p. 643-648.

J. R. Reichl, J.-S. Lai, A. R. Hefner, T. R. McNutt, D. Berning, D., *"Inverter Dynamic Electro-Thermal Modeling and Simulation with Experimental Verification,"* IEEE Power Electronics Specialists Conference, pp. 2208-2215 (June 2005).

A. R. Hefner, T. R. McNutt, A. Akuffo, R. Singh, C. Ellenwood, D. Berning, M.K. Das, J. J. Sumakeris, and R. Stahlbush, *"Characterization of SiC PiN Diode Forward Bias Degradation,"* Industry Applications Conference, 2004, pp.1252-1260.

J. Reichl, D. Berning, A. Hefner, and J-S. Lai, *"Six-Pack IGBT Dynamic Electro-Thermal Model; Parameter Extraction and Validation,"* IEEE Applied Power Electronics Conference, February 2004.

Blackburn, D. L., *"Temperature Measurement of Semiconductor Devices – A Review,"* Proceedings of Semiconductor Thermal Measurement and Management Symposium, pp. 70-80 (March 2004).

Manufacturing Support Program

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300 mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with the International Semiconductor Industry Initiative (ISMI, a subsidiary of SEMATECH) to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain," and to provide standards for secure electronic diagnostic data and for coherent time synchronization on the factory floor.

Factory Time Synchronization Standards Development for E-Manufacturing

Technical Contact:
Y. Li

Goals

The project's objective is to facilitate the development of standards and guidelines to achieve reliable clock synchronization and time stamping capabilities for supporting present and future e-Manufacturing needs. The project aims to educate the industry about the requirements, related issues, and potential solutions in regards to distributed precision clock synchronization.

Customer Needs

Increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Advancing next-generation semiconductor manufacturing will require data to be collected and analyzed from a rising confluence of data streams, due to narrowing tolerance windows, new material introduction and novel processing techniques. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

As 300 mm factories mature, the fabrication facilities continue to face difficult challenges in managing the increasing factory complexity, which has resulted in an:

"Explosive growth of data collection/analysis requirements driven by process and modeling needs." 2006 ITRS Update Edition, Factory Integration, p. 2.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data.

"Device and process complexity make the ability to trace functional problems to specific process areas difficult." 2006 ITRS Update Edition, Factory Integration, p. 3.

Quality time stamps ensure the ability to precisely pin-point problems and other types of cause-effect relationships. Accurate time stamps will become a key component in data quality for Advanced Process Control (APC) applications, especially in the realm of Fault Detection Classification (FDC).

With the advent of the Equipment Data Acquisition (EDA) interface where data collection rates can increase to 10,000 data points per second, one millisecond time stamp accuracy will be required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require clock synchronization of all the related local clocks in the manufacturing site including the clocks within the process and metrology tools.

Technical Strategy

Through active participation in the SEMI International Equipment Engineering (IEE) TF, this project will continue to support standards development and legacy standards updates to ensure factory equipment and equipment components can reliably and consistently report time and time-stamp data.

The first approach is to continue to be aware of the latest developments in evolving distributed clock synchronization technologies, specifically in the mainstream protocols such as IEEE 1588, *Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, and NTP, *Network Time Protocol*. The semiconductor industry requirements have been presented to the IEEE 1588 group in order to leverage feedback on recommended practices.

DELIVERABLES: Document time synchronization and time stamping issues in networked control systems to present to the IEEE 1588 committee. 1Q 2007

To expedite integration of time synchronization protocols into the equipment, standards will be necessary to make the tasks as efficient as possible. The SEMI Time Synchronization Working Group has recently developed a new standard for defining a clock object to ensure consistent reporting of time data along with contextual information to allow the user to determine the synchronization accuracy of the time. Additionally, legacy standards need to be updated in order to leverage the new time object. NIST also plans to document recommended methods for implementing the upcoming clock requirements.

DELIVERABLES: Continue to participate in SEMI standards efforts to update relevant time and date information in Information and Control Committee standards to ensure the ability to leverage the new clock definition without conflicts. 3Q 2007

To enable accurate time stamping, it is imperative to have a reliable and accurate clock synchronization methodology. Research on practical application and performance testing of the synchronization protocols would determine the impact of various computing factors (*e.g.*, CPU usage, network traffic, constraints of sensors and embedded systems, etc.) on distributed clock synchronization performance. The Engineering Research Center at University of Michigan has been collaborating with NIST in conducting studies on the accuracies achievable with software-based time synchronization protocols in industrial networks. To fully understand the intricacies, a factory simulation system is currently being developed. The work will have practical benefits in ensuring the potential solutions and new industry standards are feasible and effective in achieving accurate clock synchronization and data time stamping. Additionally, the factory simulation system can be extended to model the impact and cost-benefits of accurate time stamps on factory APC applications.

DELIVERABLES: Create a hybrid factory simulation-sensor network environment with networked computers and embedded sensor and control systems to research the impact of the system on time synchronization and time stamping accuracy. 4Q 2007

Accomplishments

- A NIST internal report (NISTIR 7184) on "Semiconductor Factory and equipment Clock Synchronization for e-Manufacturing" was published in December 2004.
- The presentation on "*Running Out of Time:* Improvements Required in Current Semiconductor and Equipment Clock Synchronization for Supporting Future Real-Time Data Collection" was given at AEC/APC Symposium in September 2004.
- "*Intricacies of Time:* Demystifying Clock Synchronization and Time Stamping for e-Manufacturing" was presented at AEC/APC Symposium in September 2005.
- "*In Search of the Key to the Lock:* Clock Synchronization Requirements in Semiconductor Manufacturing" was presented at the IEEE 1588 Conference in October 2005.
- "Using Network Time Protocol (NTP): Introduction and Recommended Practices" was published as an ISMI Technical Report in February 2006.
- "Legacy Standards Update: SEMI Standards Analysis to Meet Factory Time Synchronization Requirements" was presented at the SEMI Spring IEE TF meeting in March 2006.
- Poster presentation on "New Industry Requirements for Clock Synchronization and Time Stamping" was published at the European AEC/APC Symposium in March 2006.
- "Time Synchronization in Manufacturing Networks" at the Network Performance Workshop (University of Michigan) was presented in April 2006.
- Presented the talk on "Advancing Towards Factory-Wide Data Quality for APC Applications, AEC/APC XVIII Proceedings, Westminster, CO, September 29-October 6, 2006.
- Presented the talk on "Practical Aspects Impacting Time Synchronization Data Quality in Semiconductor Manufacturing," Proceedings of the 2006 IEEE-1588 Conference, Gaithersburg, MD, October 2-4, 2006.
- Published "Factory and Equipment Clock Synchronization and Time-Stamping Guidelines," ISMI Technology Transfer, October 20, 2006.
- Presented "Advancing Towards Factory-Wide Data Quality for APC Applications, AEC/APC Asia Symposium Proceedings, Taipei, Taiwan, November 30-December 1, 2006.

Collaborations

Harvey Wohlwend, Gino Crispieri, International SEMATECH Manufacturing Initiative

James Moyne, Naveen Kalappa, Jonathan Parrott Engineering Research Center, University of Michigan Ann Arbor

Alan Weber, Alan Weber and Associates

Recent Publications

H. Wohlwend, Y. Li, *"New Industry Requirements for Clock Synchronization and Time Stamping,"* European AEC/APC Symposium, Mar 27-31, 2006, Aix En Provence, France.

N. Kalappa, J. Moyne, J. Parrott, Y. Li, *"Practical Aspects Impacting Time Synchronization Data Quality in Semiconductor Manufacturing,"* Proceedings of the 2006 IEEE-1588 Conference, Conference on IEEE-1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, Oct 02-04, 2006, Gaithersburg, Maryland.

J. Moyne, J. Parrott, N. Kalappa, Y. Li, *"Practical Aspects Impacting Time Synchronization Data Quality in Semiconductor Manufacturing,"* AEC/APC Symposium XVIII, Sep 30, 2006 to Oct 05, 2006, Westminster, Colorado.

E. Simmon, Y. Li, J. V. Messina, *"An External Stopwatch for Measuring the Timing of Events in a Computer or Distributed Computing Environment,"* AEC/APC Symposium XVII, Sep 24-29, 2005, Indian Wells, California.

E. Simmon, Y. Li, J. V. Messina, *"Sands of Time: An External Stopwatch for Measuring the Timing of Events in a Computer or Distributed Computing Environment,"* AEC/APC Symposium, Sep 26-29, 2005, Indian Wells, California.

Y. Li, H. Wohlwend, L. Rist, E. Simmon, *"Intricacies of Time: Demystifying Factory Clock Synchronization and Time Stamping for E-Manufacturing,"* AEC/APC Symposium, Sep 26-29, 2005, Indian Wells, California.

Y. Li, *"Using NTP: Introduction and Recommended Practices,"* ISMI Technology Transfer.

E-Diagnostics Security

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Goals

The project strives to employ the latest web services security technologies for mitigating increasing security risks of potential Internet-based application systems, such as e-Diagnostics. As a proof of concept, the project aims to design a web-based framework that leverages available security technologies to ensure proprietary semiconductor process and equipment data would not be compromised.

Customer Needs

Optimizing factory and process capabilities and efficiency will require more data to be shared among disparate partners in the engineering chain. The ability to share data among disparate partners has become a near-term issue in the International Technology Roadmap for Semiconductors (ITRS):

"Manufacturing knowledge and control information need to be shared as required among disparate factories." 2006 ITRS Update, Factory Integration, p. 2.

However, a key concern is the security of the data and the ability to protect intellectual property and other forms of valuable proprietary information. One application where data sharing between the factory and the equipment supplier is necessary to expedite equipment repair is e-Diagnostics. E-Diagnostics enables equipment suppliers to remotely monitor, maintain, diagnose, and repair tools on the factory floor. Enabling a web-based application would provide greater flexibility for equipment engineers to monitor or troubleshoot equipment on the manufacturing floor. With the convenience and economic advantages of being able to diagnose and resolve problems via the Internet come all the security challenges of the digital world. The challenges in managing Internet-based security have been a critical obstacle in using web services for e-Diagnostics. However, the web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security. A web services security framework would provide an initial step towards realizing a web-based e-diagnostics system. A framework infrastructure promotes interoperability and rapid integration of new security technologies to ease the management of dynamic security policies with the proliferation.

Technical Strategy

Companies have expressed the need for methods to manage security risks, but not at the expense of productivity. Therefore simplicity of use and security are the key objectives of this project. The web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security. The eXtensible Markup Language (XML) security suite provides a standard paradigm to manage access control in order to restrict who may and may not control the equipment remotely, encryption and signatures in order to protect the data and ensure against malicious attackers, and key management to ensure the encryption used is safe. These features work with web services transport systems such as Simple Object Access Protocol (SOAP) to further ensure the safety of the data passed in transit. Leveraging the available standards in an effective manner can serve as a potential line of defense. However, employing XML-based standards alone are not sufficient in implementing a secure framework. Security must be managed through careful interaction with factory systems, databases and networks, as well as the users accessing the factory systems.

Robust identity management authentication and access control of legitimate users must be in place. The system should be readily managed to accommodate dynamic security policies. Simplifying security management is a key practice in avoiding security loopholes. Therefore, in facing the proliferation of security threats and system vulnerabilities, the industry can benefit by leveraging mainstream security tools to provide a robust line of defense against potentially costly threats to intellectual property and the continuous operation of factory systems.

Based on the needs of industry, a framework will be designed and implemented that allows for fine-grain access control to restrict unauthorized users from infiltrating the system, while ensuring legitimate users have convenient access to resources necessary to complete their tasks. In order to strengthen the system, we will incorporate the current web-services security technologies available to encrypt messages and secure transportation of all sensitive information. The result of the project would be a prototype to demonstrate a secure web services framework for e-Diagnostics and other web-based applications in the semiconductor industry.

DELIVERABLES: Complete an identity management and access control framework based on Security Assertion Markup Language (SAML), eXtensiblle Access Control Markup Language (XACML) and Lightweight Directory Access Protocol (LDAP). 4Q 2007

Lastly, the security of the system will need to be analyzed and verified. Due to the rapidly evolving nature of security attacks, it is imperative to ensure systems are not only secure against current threats, but also mitigate potential risks in the future. The project will examine the latest types of attacks on identity management and access control, and design methods to evaluate the ability of a system to mitigate such risks.

DELIVERABLES: Evaluate possible threats to the web security framework and research methods to evaluate the security vulnerabilities of a system. 4Q 2007

Accomplishments

- Draft white paper on "Survey of Web Services Security Technologies and Recommended Practices."

- Initial software undergoing development at NIST is available at: *http://e-diagnostics.sourceforge.net/*.

Collaborations

École Supérieure d'Informatique et d'Applications de Lorraine (ESIAL)

Harvey Wohlwend, Gino Crispieri, International SEMATECH Manufacturing Initiative

Engineering Chain Management in the Semiconductor Industry

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Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry's requirements to reduce time, inventory, and therefore costs.

"Manufacturing knowledge and control information need to be shared as required among disparate factories" 2006 Update International Technology Roadmap for Semiconductors Factory Integration (ITRS) 2006 Update, Factory Integration, p.2.

The semiconductor industry is also seeking to control costs and improving semiconductor yields through the development of advanced Factory Information and Control Systems (FICS). Next generation FICS are expected to be able to collect information from equipment that will enable intelligent automated decision-making concerning factory resources. (This will require data quality assurance). Materials will be processed and dispatched to equipment in a way to minimize production equipment idle time thus maximizing factory output. In addition, FICS will allow factories to be more reconfigurable as needed even to the point of being able to modifying wafer processes on a wafer-by-wafer basis. This is even more important with factories expected to use even few total wafers with the expected transition to 450mm. Developing these FICS will require a greater level of interoperability and data exchange within the semiconductor factory.

"Process Control solutions must be able to support the ability to run different process parameters for each wafer, both between and with process runs.. 2005 ITRS Factory Integration, p. 16.

An additional concern for the semiconductor industry is the growing trend towards environmental legislation that seeks to protect the environment from hazardous substances. An example of this new trend is the European Union's Restriction of Hazardous Substances (RoHS) in electronics directive that seeks to reduce or eliminate six substances known to be hazardous to humans and the environment. This will result in a massive shift in the availability of parts as some components are removed from the marketplace while others are redesigned completely to remove the banned substances. In addition to forcing product changes, the only way for companies to comply with such legislation will be to support the exchange of material composition information throughout the entire supply chain. Complying with the new legislations will greatly add to the cost of design and can only be mitigated through the development of appropriate standards.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES: Chair the Product Lifecycle Information Management (PLIM) TWG of the ITRS 2007 Roadmapping Activity. 4Q 2007

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in

leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES: Establish a working arrangement with SEMATECH and SEMI in order to identify top industry IT-standards related needs and develop potential solutions to the current challenges based on cross-industry solutions facing similar issues. 3Q 2007

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Work with industry to create a material declaration standard designed to assist industry in complying with all the forthcoming environmental legislation being passed around the world. 4Q 2007

Accomplishments

- In conjunction with IPC, NIST developed IPC 1752 material declaration standard that supports the exchange of RoHS environmental legislation through the engineering chain.

- Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial has been taught as a class at both NIST and various SEMI standards workshops.

- Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.

- NIST co-led the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Efforts were made to determine the scope and identify the challenges of creating an effective Engineering Chain.

- Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Collaborations

Alan Weber, Alan Weber & Associates

ITRS Factory Integration Technical Working Group

SEMI XML Task Force

SEMATECH

Recent Publications

K. Botsford, J. V. Messina, E. Simmon, *"North American Environmental Compliance Attitudes Towards Electronics,"* Jun 04-06, 2007, Singapore, Singapore.

E. Simmon, *"RoHS Harmonization ? Progress Toward a Single Global Standard?,"* Advanced Forum on Achieving and Maintaining Global RoHS Compliance, Jun 11-12, 2007, San Francisco, California.

H. Wohlwend, G. Crispieri, Y. Li, *"Advancing Factory-Wide Data Quality for APC Applications,"* AEC/APC Symposium-Asia, Nov 30, 2006 to Dec 01, 2006, Taipei, Taiwan.

H. Wohlwend, G. Crispieri, Y. Li, *"Advancing Towards Factory-Wide Data Quality for APC Applications,"* AEC/APC Symposium XVIII, Sep 30, 2006 to Oct 05, 2006, Westminster, Colorado.

A. Griesser, *"Ensuring High Quality Data Transfer Standards,"* AEC/APC Symposium XVI, Sep 18-24, 2004, Westminister, Colorado.

NIST/SEMATECH e-Handbook of Statistical Methods

Goals

The goal of the *NIST/SEMATECH e-Handbook of Statistical Methods* project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the *e-Handbook* readily accessible to its target audiences in industry, including the semiconductor industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH (Fig. 1).

Figure 1. NIST e-Handbook of Statistical Methods team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

DELIVERABLES: Update and maintain the *e-Handbook* on-line, and continue to distribute the *e-Handbook* on CD for off-line use. 4Q 2007

Accomplishments

■ Since release of the final version, work has focused on publicizing the *e-Handbook*, responding to user feedback, and developing a compact disk version for off-line use (Fig. 2). The web version of the e-Handbook averages approximately 1 million hits per month and over 8,500 e-Handbook compact disks have been distributed to industrial, government, and academic users all over the world over the last two years. Publicity on the e-Handbook has appeared in *Science*, *Quality Digest*, *MicroMagazine.com*, *States News Service*, *National Science Digital Library Report for Math, Engineering, and Technology*, and *American Statistician*. In February 2007, a Division workshop was held to discuss additions to the e-Handbook. It was agreed there to seek proposals for additional material to be added to existing chapters, or for new chapters. Several potential topics for new chapters were identified and discussed.

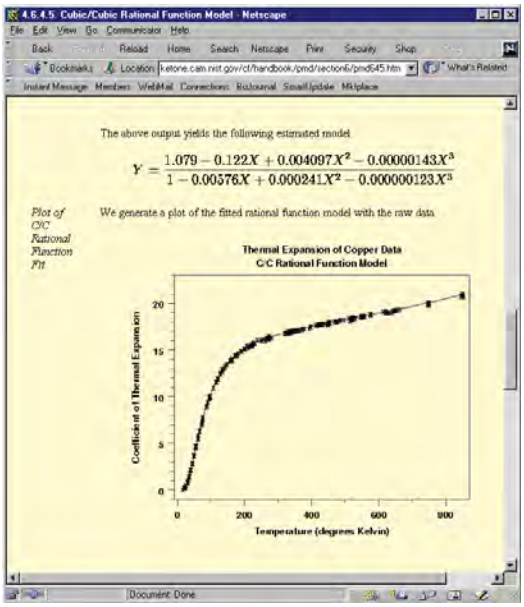

Figure 2. Page from a case study in the process modeling chapter of the Handbook.

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"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc.

Collaborations

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

Recent Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.

Abbreviations and Acronyms

A.C.	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CPU	Central Processing Unit
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
D.C.	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility

Abbreviations and Acronyms (cont'd)

EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal Oxidation Of Silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPU	MicroProcessor Unit
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)

PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RLGC	distributed resistance, inductance, conductance, and capacitance
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-a-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
STM	Scanning Tunneling Microscope
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy
XRR	X-Ray Reflectometry

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