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Shared Virtual Memory (SVM)





Shared Virtual Memory (SVM)





Called Shared Virtual Addressing in Linux Community

Shared Virtual Memory (SVM)





SVM on Intel® VT-d

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- Process Address Space ID (PASID)
 - Identify process address space
- First-level translation
 - DMA requests with PASID
 - For SVM transaction from endpoint device

Second-level translation

- DMA requests without PASID
- For normal DMA transaction from endpoint device

Translation Types

- First-Level translation
- Second-Level translation
- Nested translation
- Pass-Through (address translation bypassed)
- Intel[®] VT-d 3.0 introduced Scalable Mode
 - SVM can be used together with Intel[®] Scalable I/O Virtualization

SVM on Intel[®] VT-d (Cont.)

Nested Translation

- Use both first-level and second-level for address translation
- Enable SVM in virtualization environment
 - First-level: GVA->GPA
 - Second-level: GPA->HPA



 Most vendor supports nested translation for SVM usage in Virtual Machine

Enable SVM in VM

- Need a virtual IOMMU with SVM capability
 - Proper emulation according to IOMMU spec (e.g. Intel[®] VT-d specification)
 - either fully-emulated or virtio-based IOMMU
- Notification for guest translation structure changes
 - Notification mechanism is vendor specific
 - For Intel[®] VT-d
 - "caching-mode": explicit cache invalidation is required for any translation structure change in software
- Enable nested translation on physical IOMMU for given PASID

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Save guest cpu page table pointer to host



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Bind PASID to guest
 CPU page table

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- Bind PASID to guest CPU page table
- Forward guest CPU page table cache invalidation to host

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- Bind PASID to guest
 CPU page table
- Forward guest CPU page table cache invalidation to host
- Page fault reporting and servicing

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Neutral Kernel APIs for both emulated and virtio-based vIOMMUs

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Bind PASID

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• New VFIO IOCTL supporting multiple binding types:

- VFIO_IOMMU_BIND_PROCESS
 - Binding to host CPU page table
- VFIO_IOMMU_BIND_PGTBL
 - Binding to guest CPU page table
- VFIO_IOMMU_BIND_PASID_TBL
 - Binding to guest PASID Table
- New IOMMU API to configure physical IOMMU
 - Need compatibility check of the table format



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Forward Cache Invalidation to Host

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- Invalidation types
 - IOMMU_INV_TYPE_TLB
 - IOTLB and paging structure-caches
- Granularity conversion
 - Supported granularities
 - Domain selective flush
 - PASID selective flush
 - Page selective flush
 - Avoid unnecessary flush
 - Guest global flush -> either domain/pasid selective flush in host
- Use host Identities
 - RID, Domain ID, PASID



Page Fault Handling

PCI Express[®] Address Translation Service

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- PRI: page request interface
- Page Response (PRS)



Page Fault Handling (Cont.)

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- Report PRQ to Guest
 - Page Request Capability in vIOMMU
- Forward guest page response to host



IOMMU Fault Reporting Framework

 Newly defined "struct iommu_fault_param", added to "struct device"

/**

- * struct iommu_fault_param Per device generic IOMMU runtime data
- * @dev_fault_handler: Callback function to handle IOMMU faults at device level
- * @data: handler private data
- * @faults: holds the pending faults which needs response, e.g. page response.
- * @timer: track page request pending time limit
- * @lock: protect pending PRQ event list

```
*/
```

```
struct iommu_fault_param {
```

```
iommu_dev_fault_handler_t handler;
```

```
struct list head faults;
```

```
struct timer list timer;
```

```
struct mutex lock;
```

```
void *data;
```

```
};
```

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IOMMU Fault Reporting Framework

- IOMMU fault handler registration
 - iommu_register_device_fault_handler()
 - iommu_unregister_device_fault_handler()
- In-kernel device driver and vfio driver registers its own fault handler
 - Vfio fault handler should further notify Qemu or other userspace application
- The original idea was brought up by David Woodhouse
 - May refer to more detail <u>https://lwn.net/Articles/608914/</u>

Upstream Status (Kernel)

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- IOMMU/VFIO extension for virtual SVA support (Jacob Pan/Yi Liu, Intel)
 - Earliest RFC patch for vSVA support
 - current kernel API in v5 (<u>https://lkml.org/lkml/2018/5/11/605</u>)
- SVA native enabling on ARM platform (Jean-Philippe Brucker, ARM)
- Shared requirements in the two tracks
 - binding PASID, fault reporting

SVA stands for Shared Virtual Addressing in Linux community

Upstream Status (Qemu)

- Qemu vSVA enabling has two parts (Yi Liu, Intel)
 - vIOMMU emulation
 - Earliest <u>RFC patch for vSVA back to 2017-April</u>
 - Notification framework between vIOMMU emulator and VFIO within Qemu
 - Notifier framework in <u>v3</u>, with community comments addressed



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- Shared Virtual Memory (SVM) enables efficient workload submission by directly programming CPU virtual addresses on the device
- Intel[®] VT-d 3.0 specification extends SVM usage together with Intel[®] Scalable I/O Virtualization
- Holistic enhancements are introduced cross multiple kernel/user space components, to enable SVM virtualization in KVM
- New kernel APIs are kept neutral to support all kinds of virtual IOMMUs (either emulated or para-virtualized)

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Backup

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Intel[®] VT-d ECS (deprecated)





Intel® VT-d Scalable Mode Translation Containercon CONTRIBUTED CONTRIBUTION



Key Difference: PASID is a global ID space shared by all VMs.

ALL page-table pointers moved to PASID Granular table

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