Short Range Pulse Based Inductive Transceiver

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Introduction

The present wireless sensor network scenario is characterized by networks made of tens of nodes spaced by some meters (e.g. fire alarm sensors, anti-intrusion systems and so on). The development of new wireless sensor network applications such as biomedical sensing or wearable-paintable computers requires hundreds of ultra low power nodes communicating over small distances (1-5 cm) at low-to-moderate bit rates [1],[2].

Because the distance between nodes turns to be lower than the wavelength up to many GHz, a near file approach can gives better performance in terms of energy per bit, and will be considered in this work. Moreover, the antenna size for an efficient transmitter must be 1/4 of the wavelength, and this is not feasible for a 1 cm node and for frequencies lower than 7.5 GHz. The above considerations lead to the adoption of a pulse based inductive approach similar to the one presented in [3] for chip-to-chip communications.

In a pulse based communication with low bit rate the information is concentrated in narrow time slots with respect to the pulse repetition period and the average power consumption of the receiver can be strongly reduced by means of duty cycling [4],[5]. However, differently form [4] and [5], a main objective of this work is to exploit the maximum level of integration avoiding the requirements of a precise local oscillator (quartz) on each node for the synchronization and duty cycling. In the proposed architecture the oscillator is replaced with a Phase Locked Loop (PLL) that locks the local time base on the incoming signal. In a strongly connected network the above solution allows to achieve a global synchronization by locking all the nodes to a small set of master nodes providing a common time reference with a reduced set of crystal oscillators.

Chapter 1

Short Range Wireless and Inductors Coupling

Before going through the description of the implementation, this chapter gives an overview of the system starting from the analysis of the inductive coupling between inductors to the inductor design and the architecture definition.
Finally the proposed synchronization scheme for an impulsive radio, based on a local PLL is described an analyzed.

1.1 Coupled inductors

Since the communication is based on coupled inductor, in this section an introduction on the problem is given.
Assuming that the current I_1 flows through an inductor L_1 made of N_1 turns of radius R_1 (each one of area $A_1 = \pi R_1^2$), from a distance greater than 5 times the coil radius the coil can be described as a magnetic dipole MD.

$$MD = N_1 A_1 I_1 = N_1 \pi R_1^2 I_1 \tag{1.1}$$

The electromagnetic filed surrounding a magnetic dipole of magnetic moment MD can be written as [6]

$$E_\phi = \xi \frac{\beta^3}{4\pi} MD \left(\frac{1}{\beta r} - \frac{j}{(\beta r)^2} \right) \sin(\theta) e^{j\beta r} \tag{1.2}$$

$$E_\theta = 0 \tag{1.3}$$

$$E_r = 0 \tag{1.4}$$

$$H_\phi = 0 \tag{1.5}$$

$$H_\theta = -\frac{\beta^3}{4\pi} MD \left(\frac{1}{\beta r} - \frac{i}{(\beta r)^2} - \frac{1}{(\beta r)^3} \right) \sin(\theta) e^{j\beta r} \tag{1.6}$$

$$H_r = \frac{\beta^3}{2\pi} MD \left(\frac{j}{(\beta r)^2} + \frac{1}{(\beta r)^3} \right) \cos(\theta) e^{j\beta r} \tag{1.7}$$

and where r is the observation distance, $\beta = 2\pi\lambda$ and the angles ϕ and θ are illustrated in figure 1.1.
The Poynting vector is defined as

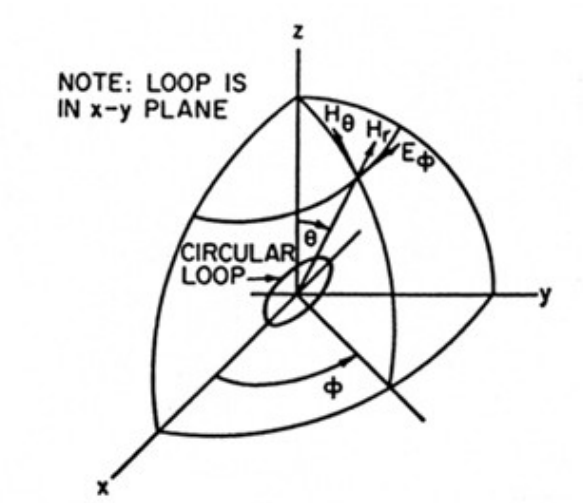

Figure 1.1: *E.M. filed generated by a magnetic dipole*

$$\vec{W} = \vec{E} \times \vec{H}^* \cdot \hat{r} \tag{1.8}$$

that is given by a real part (radiative field) and an imaginary part (reactive field).

$$W = -\frac{E_\phi H_\theta}{2} \frac{\pi}{2} \xi \frac{MD^2}{\lambda^4} \frac{1}{r^2} \sin^2(\theta) \left[1 + j \frac{1}{(\beta r)^2} \right] \tag{1.9}$$

The radiated (active) power is given by the integral of the real part of 1.9 over a surface including the dipole. Assuming a sphere it is

$$P = \int_s W \mathrm{d}s = \int_0^{2\pi} \mathrm{d}\phi \int_0^{\pi} d\theta W r^2 \sin(\theta) \mathrm{d}\theta$$

that is

$$P = \frac{4}{3}\pi^3 \xi \frac{MD^2}{\lambda^4} \tag{1.10}$$

Note that is a lossless space the radiated power does not depend on the sphere radius.

Assuming now that a second inductor L_2 with radius N_2 and number of turns N_2 is put on the same plane of L_1; neglecting the radiated power P, the equation of the system can be written as

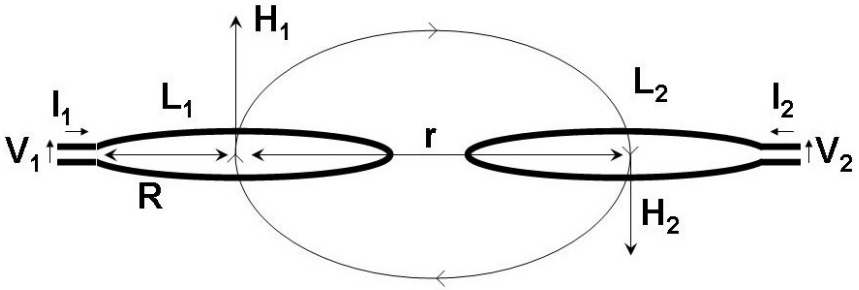

Figure 1.2: *Coupled inductors*

$$V_1 = L_1 \frac{\mathrm{d}I_1}{\mathrm{d}t} + M_{12} \frac{\mathrm{d}I_2}{\mathrm{d}t} \tag{1.11}$$

$$V_2 = M_{12} \frac{\mathrm{d}I_1}{\mathrm{d}t} + L_2 \frac{\mathrm{d}I_2}{\mathrm{d}t} \tag{1.12}$$

$$\tag{1.13}$$

and the coupling factor k is defined as

$$k = \frac{M_{21}}{\sqrt{L_1 L_2}} = \frac{M_{12}}{\sqrt{L_1 L_2}}$$

If the second inductor is open ($I_2 = 0$) and $L_1 = L_2 = L$, equations 1.11 become

$$V_1 = L_1 \frac{\mathrm{d}I_1}{\mathrm{d}t} \tag{1.14}$$

$$V_2 = M_{12} \frac{\mathrm{d}I_1}{\mathrm{d}t} \tag{1.15}$$

and then

$$k = \frac{V_2}{V_1}$$

The coupling factor can therefore be computed as the ratio of the induced voltage V_2 over the voltage V_1.

The concatenated flux with L_2 is given by

$$\Phi_c = \mu H_\theta N_2 A_2 =$$

and if the distance is small with respect to the wavelength (near field approximation)

$$\beta r = \frac{2\pi}{\lambda} r << 1 \quad \Rightarrow \quad \frac{r}{\lambda} << \frac{1}{2\pi}$$

$$\Phi_c = \mu N_2 A_2 M D \frac{16\pi^5}{\lambda^6 r^3}$$

so the induced e.m.f. is

$$V_2 = \frac{\mathrm{d}\Phi_c}{\mathrm{d}t} = \mu N_2 A_2 M D \frac{\mathrm{d}H_\theta}{\mathrm{d}t}$$

and replacing the expression of MD

$$V_2 = \mu A_1 A_2 N_1 N_2 \frac{1}{4\pi r^3} \frac{\mathrm{d}I_1}{\mathrm{d}t}$$

The the mutual inductance is therefore

$$M_{12} = M_{21} = \frac{\mu A_1 A_2 N_1 N_2}{4\pi r^3} = \frac{\mu \pi R_1^2 R_2^2 N_1 N_2}{4 r^3}$$

and the coupling factor k is

$$k = \frac{M_{21}}{L} = \frac{\mu \pi R_1^2 R_2^2 N_1 N_2}{4 L r^3} \tag{1.16}$$

that with the two inductor equals it is

$$k = \frac{\mu\pi R^4 N^2}{4Lr^3} = \frac{V_2}{V_1} \tag{1.17}$$

Note that k is proportional to the squared inductor area and the squared number of turns. It also goes as the distance up to the minus 3 and rapidly decreases as the distance increases; however it does not depends on the frequency (as long as $\beta r << 1/(2\pi)$) but only on the geometry of the system.

1.2 Pulse Based Radio

In this section a brief analysis of the pulse based communication used in this design is given. All the equations and the plots reported in this section refers to the pulse shape chosen for the implementation.

Because the inductor behave like a short circuit for the DC, the voltage pulse forced across the inductor must have a zero average value to avoid useless power dissipation.
For maximum hardware simplicity, in this design a squared signed pulse is considered; the voltage levels are assumed to be ± 1 V, to be compliant with the further implementation in 90 nm CMOS technology.
Applying the voltage pulse $V_t(t)$ (figure 1.3) of duration τ_p to an inductor, the resulting current waveform is shown in figure 1.4.
Since $V_t(t)$ is the superimposition of two pulses, the spectrum can be easily calculated as

$$V_t(\omega) = \frac{V_0\tau_p}{2}\frac{\sin\left(\frac{\omega\tau_p}{4}\right)}{\frac{\omega\tau_p}{4}}e^{\frac{j\omega\tau_p}{4}} - \frac{V_0\tau_p}{2}\frac{\sin\left(\frac{\omega\tau_p}{4}\right)}{\frac{\omega\tau_p}{4}}e^{\frac{-j\omega\tau_p}{4}}$$

and with few algebra

$$V_t(\omega) = -jV_0\tau_p\frac{\sin\left(\frac{\omega\tau_p}{4}\right)^2}{\frac{\omega\tau_p}{4}}$$

The spectrum is shown in figure 1.5.
The energy needed to produce the pulse is given by

$$E = \int_{-\infty}^{+\infty} V_0 I(t)\mathrm{d}t = \frac{V_0 I_M \tau_p}{2}$$

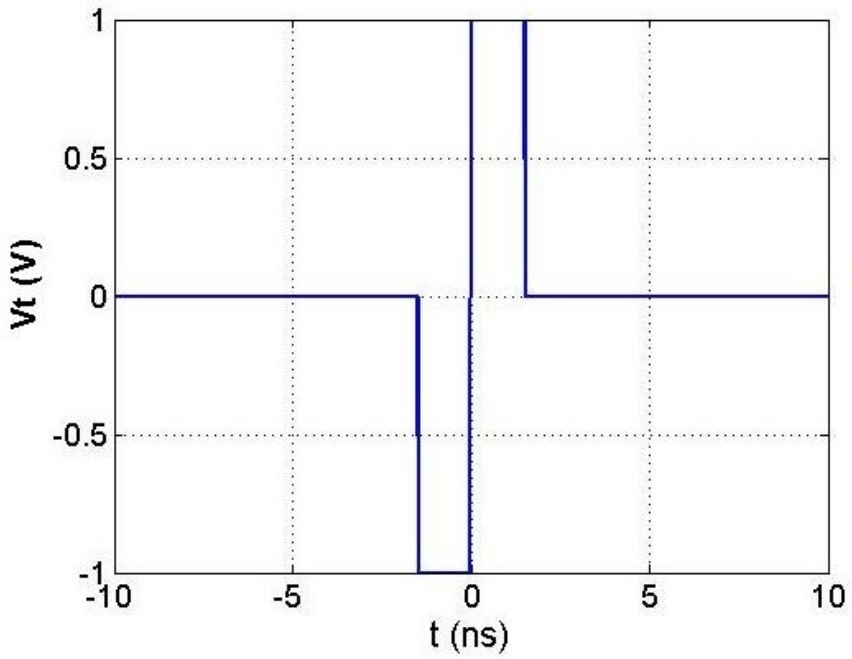

Figure 1.3: *Voltage pulse across the inductor*

and considering the relationship between current and voltage into the inductor L it is

$$E = \frac{V_0^2 \tau_p^2}{2L}$$

while the energy (in V^2) carried by the pulse is

$$E_p = V_0^2 \tau_p^2$$

that, as known by the Parseval's theorem, is equal to

$$E_p = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \|V(\omega)\|^2 \mathrm{d}\omega$$

The maximum of the spectrum is located at $f \simeq 0.742/\tau_p$ and is about $0.725 V_0 \tau_p$. The energy in the first lobe of $V(\omega)$, hence for $f < 2/\tau_p$ is the 85% of the signal energy. Being E_1 the energy of the firts lobe, it is

$$E_1 = \frac{1}{2\pi} \int_{-4\pi/\tau_p}^{+4\pi/\tau_p} \|V(\omega)\|^2 \mathrm{d}\omega = \frac{(V_0 \tau_p)^2}{2\pi} \frac{2}{\pi \tau_p} \int_{-\pi}^{+\pi} \frac{\sin(x)^4}{x^2} \mathrm{d}x$$

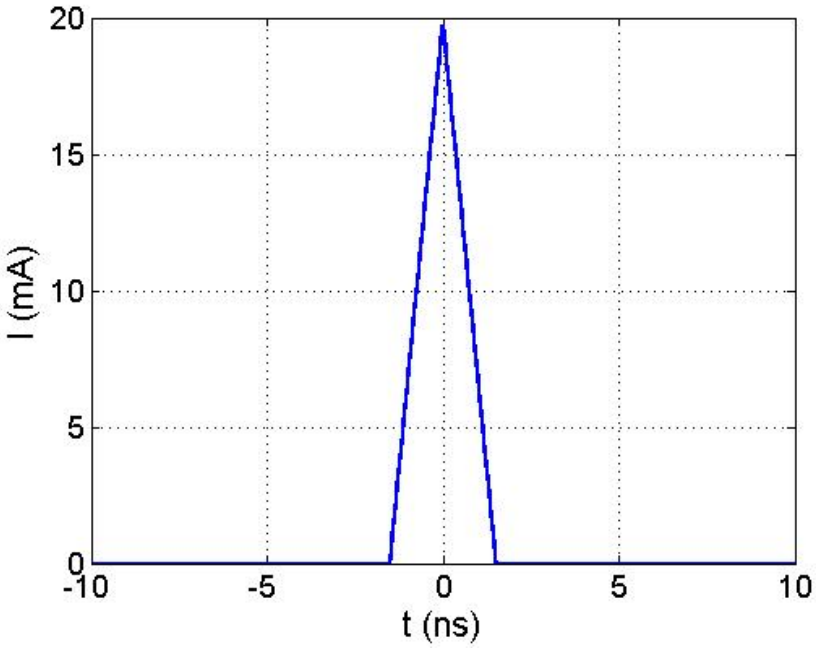

Figure 1.4: *Current pulse through the inductor*

$$\simeq \frac{2}{\pi} V_0^2 \tau_p 1.334 \simeq 0.85 E_p$$

1.3 Inductor design

The inductor to be used as antenna must satisfy certain requirements, due both to technological and functional issues.

- The features must be compatible with a standard low-cost PCB technology (minimum width and spacing greater than 6-7 mils). The substrate must be a standard PCB material, like FR4. No special materials are considered.

- The self resonant frequency must be higher than the maximum frequency of the transmitter bandwidth, otherwise a non negligible amount of the signal energy does not go through the inductor but is shorted by the parasitic capacitance.

- The size of the inductor cannot be as large as one wants. Because of the node size physical limitations and the parasitic capacitance, the area

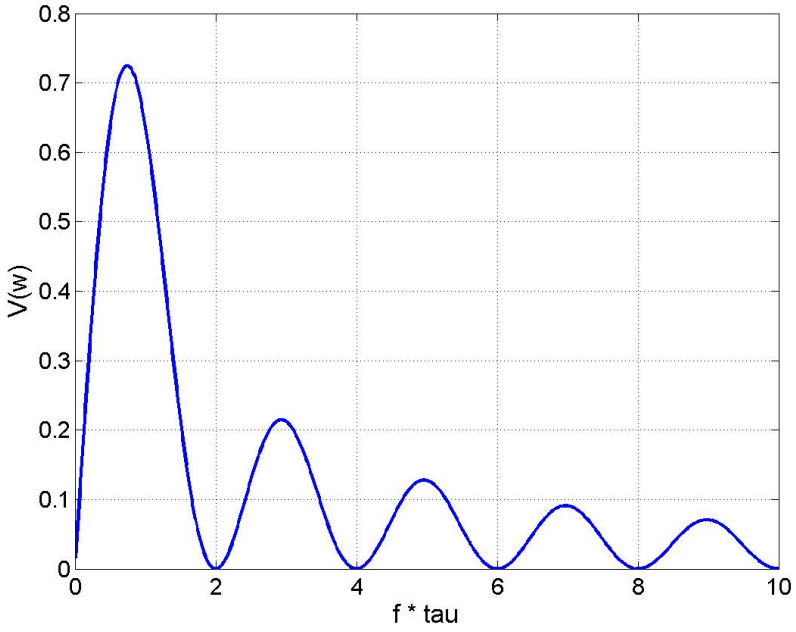

Figure 1.5: *Voltage pulse spectrum*

should be kept lower than 1 cm^2.

- The value of the inductance can not be too small, otherwise high peak currents are required in the transmitter. High transmitter peak currents require a very low transmitter output impedance, together with a power supply able to provide such a peak.

Considering these limitations, a 3 turns, 8.1 mm diameter symmetrical inductor has been designed (figure 1.6) and simulated with Agilent ADS Momentum. A inductance value of 76 nH is found.
Figure 1.7 shows the model extracted from measurements, that are in good agreements with simulations. The self resonate frequency is about 800 MHz.

The coupling factors between two inductors laid out on the same plane as a function of the distance has been measured too. Measurement results are shown in figure 1.8, together with the analytical model based on eq. 1.17.
Since the three turns of the inductor are very different in terms of radius due to the planar implementation, instead of $N\pi R^2$ an "effective area" A_{eff} has

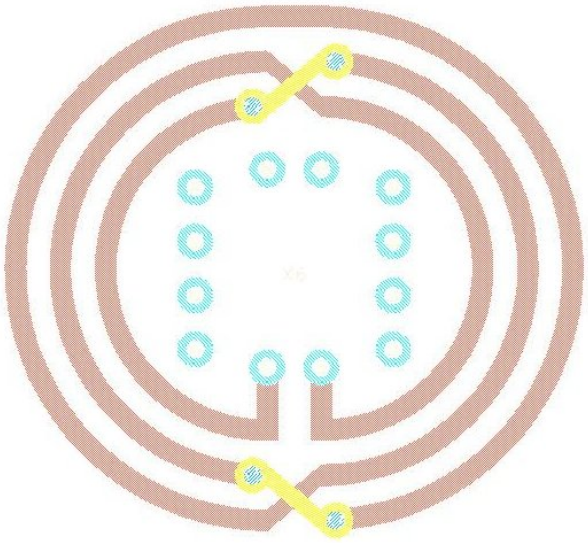

Figure 1.6: *Antenna layout*

been used in eq. 1.17.

$$A_{eff} = \sum_{i=1}^{N_{turns}} \pi R_i^2$$

1.4 SNR and Pulse Duration trade-off

The receiver antenna is sensible to the coupled magnetic filed, but is really poor in term of "radiative field" antenna in the band of interest. In fact if we consider the maximum linear "length" of the antenna, that is the diameter, it is about 1 cm, that is a quarter of the wavelength at 7.5 GHz.
This means that the antenna has a very low efficiency for electromagnetic waves in the range between 0 and 1 GHz, and therefore the performance of the receiver can be assumed to be noise limited (unfortunately further measurements will show that this statement is not true).

Once the spectrum of the pulse is found and the antenna is chosen, a key point in the receiver design is to determine the optimal filter needed on the receiver to maximize the Signal to Noise ratio (SNR). For maximum simplicity and to avoid any external component apart from the inductor, only a capacitor and a resistor are putted in parallel with the inductor to create a parallel

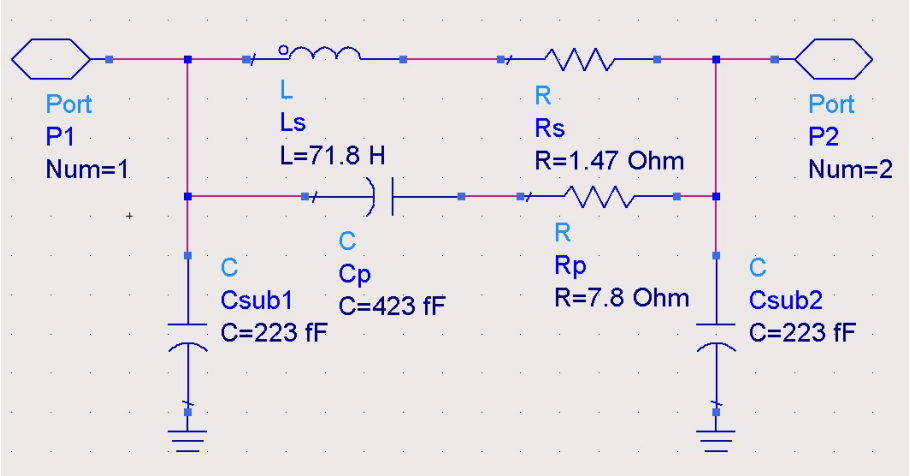

Figure 1.7: *Antenna equivalent model*

resonator, as shown in figure 1.9.
With an LC resonator the pulse can be detected over the noise, that is generated by both the L series resistance and the damp resistor. Assuming a parallel resonator structure, to maintain the signal waveform without ringing, a quality factor lower than 1 must be used. Simulation can be done for a quality factor $Q = 0.8$ to determine the optimal value of the capacitance, hence of the resonance frequency. Since the Q of the resonator is much lower than the Q of the inductor itself, only the resistance R will be considered as a noise source.
The transfer function with respect to the input is low pass and is given by

$$H_s(\omega) = \frac{V_c}{V_r} = \frac{\omega_0^2}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}}$$

with

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad Q = \frac{R}{\omega_0 L}$$

while the output noise PSD is given by

$$P_n = \| \frac{j\omega/C}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}} \|^2 \frac{4KT}{2\pi R}$$

and the squared effective noise is

$$V_n^2 = \int_{-\infty}^{+\infty} P_n \mathrm{d}\omega = \frac{1}{4\omega_0 C^2} Q \frac{4KT}{R}$$

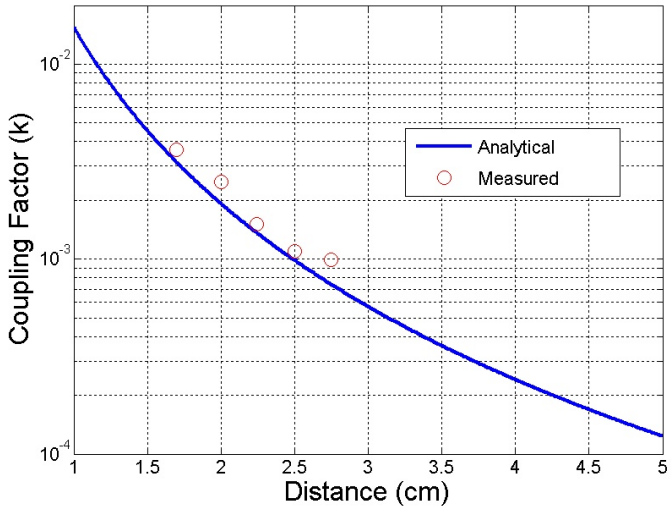

Figure 1.8: *Coupling factor as a function of the distance*

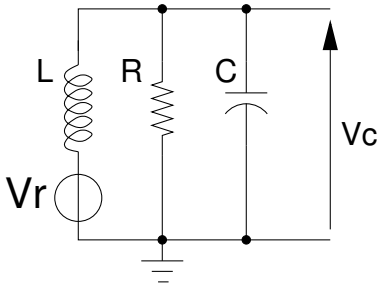

Figure 1.9: *Receiver Filter*

and, being $Q = \omega_0 CR$

$$V_n^2 = \frac{KT}{C}$$

Simulations show that to achieve the best ratio V_p^2/V_n^2, where V_p is the peak of the output pulse, while V_n^2 is the noise power expressed as squared effective value, it must be

$$\omega_0 = 0.612\frac{2\pi}{\tau_p} \tag{1.18}$$

and the (positive) peak of the output signal is

$$V_p = 0.775 V_{r0} = 0.775 k V_0 \tag{1.19}$$

Since the noise only depends on the capacitor value, and the received signal depends on the coupling factor, the SNR of the receiver can easily be calculated as a function of the capacitance C and the coupling factor k.

$$\text{SNR} = \frac{V_p^2}{V_n^2} = \frac{0.775 k V_0 C}{KT} \tag{1.20}$$

Increasing the quality factor at fixed frequency does not change the noise level, that depends only on the tank capacitance, but the response of the filter becomes oscillating (ringing). Considering the peak of the damped sine wave, the signal peak to noise ratio can be increased of a ratio up to about 4 (spectre sim) even if the detection is then more difficult due to the pulse tails.
In this implementation the quality factor has been chosen equal to 0.8, so to avoid any ringing in the circuit and use a pulse polarity detection.

As can be noted from eq. 1.19, if the coupling factor k is small, the received voltage is very small, regardless of the current used into the transmitter (assuming that the transmitter and the receiver inductor have the same characteristics). Even if the signal to noise ratio can be kept greater than 10 dB, the signal bandwidth remains huge. To amplify the signal to a detectable level an amplifier with a high gain, high bandwidth and low noise figure is required (the input referred noise should be in the order of some microvolts).
Nevertheless, increasing the maximum current into the transmitter allows the use of longer pulses, and consequently to reduce the bandwidth according with eq. 1.18 and to increase the SNR, but has no effects, in principle, on the received voltage V_r. However the receiver power consumption can take advantage of the band reduction, payed by a higher one in the transmitter.

Considering the value of the coupling factor previously computed for the inductors, it is possible to find the minimum bandwidth required for the pulse at a desired output SNR (eq 1.20).
At 5 cm distance $k \simeq 1.25 \cdot 10^{-4}$ and with 1 V pulse amplitude in the transmitter the zero-peak received signal is (from eq. 1.19)

$$V_r = 97 \mu V$$

To achieve a SNR of 13 dB on the receiver, that means a 10 dB SNR at the receiver input plus 3 dB margin for the receiver Noise Figure, it is

$$V_n \simeq 22 \mu V$$

and the (minimum) capacitance required on the receiver is

$$C = \frac{KT}{V_n^2} \simeq 8.5\ pF$$

therefore the maximum resonance frequency for the receiver is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \simeq 204MHz$$

and from eq. 1.18, the minimum pulse duration is

$$\tau_p = \frac{0.612}{f_0} \simeq 3.1\ ns$$

$$R = \frac{Q}{2\pi C f_0} \simeq 78\ \Omega$$

When a constant voltage is applied to an inductor, the current grows linearly with time. If the total pulse duration is τ_p, the peak current in the inductor is

$$I_{MAX} = \frac{V\tau_p}{2L} \simeq 20\ mA \tag{1.21}$$

Note that this current, even if it is needed only for a very short time, and therefore the power turns out to be negligible, it must be handled by the transmitter and the power supply. An on-chip decoupling capacitor is necessary to avoid this 20 mA/3 ns pulses to flows over the V_{DD} bond wires and lines and spreading a large amount of di/dt noise. For the chosen number for the inductor and the pulse duration, a reasonable value of the capacitor is found.
The total charge required by the transmitter for a single pulse is given by

$$Q = \frac{I_{MAX}\tau_p}{2} = 30\ pC$$

Assuming to tolerate voltage drop of 100 mV on a "charge tank" capacitance that supplies the transmitter, the minimum value required for this capacitance C_T is given by

$$C_T = \frac{Q}{\Delta V} = 300\ pF$$

that can be integrate in a relatively small area on chip. Moreover this capacitance is not required to be linear and MOS capacitance can be extensively used. Apart from the capacitor, the transmitter driver must be able to drive 20 mA peak current with a voltage drop lower than 100 mV; this fixes a constraint on the transmitter output resistance $R_{out,T}$.

$$R_{out,T} < \frac{\Delta V}{I_{MAX}} = 50\ \Omega$$

1.5 Receiver duty cycling and synchronization issues

The main advantage of a pulse based system with respect to a narrow band one is that the all the information is squeezed in a very small time interval (in this case $\tau_p = 3$ ns) within the pulse period (i.e. $T_p = 50$ μs at 20 kpps pulse rate).
This means that the receiver is really "needed" for only 3 ns over 50 μs, or in other words that the receiver can be hardly duty cycled to dramatically reduce its average power consumption (figure 1.10).
Realistically, the receiver must be turned on some time before the pulse is

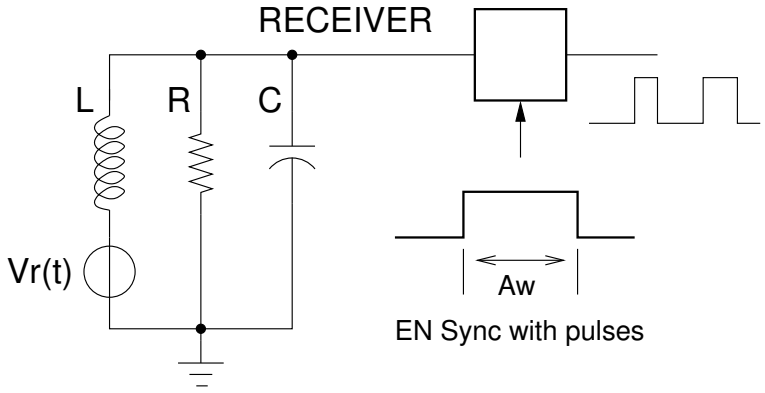

Figure 1.10: *Receiver duty cycling*

coming and can be turned off some time after the pulse. In order to open this "window" for the receiver, and to avoid the use of a wake-up radio, a local time base must be kept in the receiver so the node knows when the next pulse is coming and wake up the receiver.
Of course there is an obvious trade off between the window duration A_w and its accuracy. A longer window will result in a lower receiver duty cycle, but in the same time in a lower power consumption in the local time base, since the required accuracy is lower. On the other hand a window that perfectly fit the pulse leads to the minimum power for the receiver, but requires a very accurate and power hungry time base.

As example, be T_1 and T_2 the period of the local clock of the nodes 1 (transmitter) and 2 (receiver) respectively. The relative accuracy is indicated with α. Assuming a communication scheme based on packets of N bits and an ideal synchronization system that is perfectly locked during the packet

reception, the local time base in the node 2 must keep the time only between one packet and the next one.
At the beginning of the new packet, the time difference between the clock of the two nodes that want to communicate must be lower than half a window ($A_w/2$), otherwise the pulse is missed by the receiver and the communication fails. In a full duplex communication scenario, the minimum separation between packets must be as long ad the packet itself, to allow for a bidirectional communication. In this case

$$NT_1 - NT_2 = \frac{N}{F_1} - \frac{N}{F_2} = \frac{N}{F_1} - \frac{N}{F_1(1+\alpha)} \simeq T_1 N\alpha < \frac{A_w}{2}$$

With packet of $N = 1000$ pulses at 20 kpps pulse rate ($T_1 = 50$ μs) NT_1 must be longer than 50 ms. If $NT_1 = 50$ ms and $A_w = 100$ ns (that is about 30 times the pulse duration) the accuracy must be

$$\alpha < \frac{A_w}{2NT_1} \simeq 1\text{ppm}$$

A so stringent accuracy can only be achieved by providing each node of a crystal oscillator. The requirement of a crystal oscillator leads to an expansive and not fully integrated solution, that is not desired.
The receiver duty cycle achieved in this case is

$$DC = \frac{T_{on}}{T} = \frac{NBA_w}{NBT_1 + NT_1} \simeq 10^{-3}$$

The receiver duty cycle could be further reduced by increasing the interleaving between packets, but this will results in an even higher clock frequency accuracy, or in the needing of a wake-up radio.

An opposite approach is to assume a streamed data flow, that means that 20 kbps are always exchanged between the transmitter and the receiver. Since the pulse is very narrow compared to the bit rate, many communications can be interleaved in a TDMA fashion (figure 1.11). With the previous numbers for bit rates and window duration A_w, and assuming another A_w guard interval between two adjacent windows, up to 250 communications can be established at the same time.
In this case the maximum time without a received pulse is given by the pulse period itself, and the previous equation applies with $N = 1$.

$$\alpha < \frac{A_w}{2T_1} \simeq 1000\text{ppm}$$

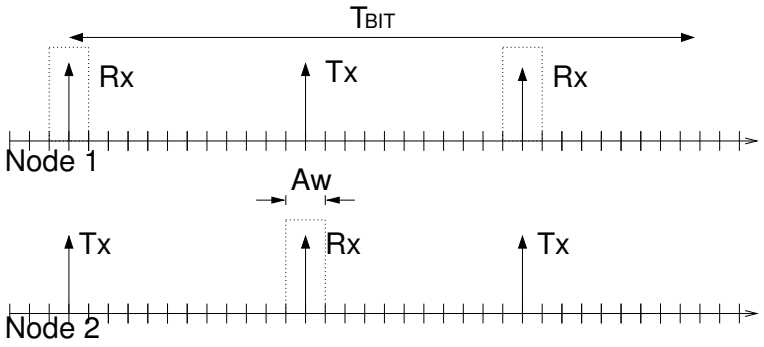

Figure 1.11: *Data stream in TDMA fashion*

The required accuracy in this case is quite relaxed, and it does not need for a reference crystal on the receiver. It can continuously track the received signal by means of local D/PLLs.
The receiver duty cycle turns out to be

$$DC = \frac{T_{on}}{T} = \frac{A_w}{T_1} \simeq 2 \cdot 10^{-3}$$

Note that in the stream communication model, the communication is always sets between nodes, and the synchronization is initialized only once at system start up and not at every packet.
At the network start up, a "master clock" node (provided of a crystal oscillator) starts to transmit pulse so to lock the PLLs of all the neighbor nodes. Once they are locked they can start to transmit pulses to their own neighbors, and in this way the synchronization is propagate to the whole network starting from the "master node" clock.

The main theoretical limitation of this synchronization system remains the locking phase of the PLLs of all the nodes that must be set at (each) power up.
It is well known that the locking time of a PLL is in the order of many hounded of reference periods, and being the reference frequency given by the pulse rate, it is in the order of milliseconds. During this initial interval the receivers cannot be duty cycle.
Further detail on the synchronization scheme will be given in the next chapter or in [7].

Chapter 2

Transceiver Implementation

The proposed architecture has been implemented in 90 nm STMicroelectronics CMOS technology. The power supply is 1 V and only "standard threshold" (svt) transistors have been used both for analog and digital parts. This allows for compatibility of the transceiver with a system which uses either low threshold or high threshold ones.
The process allows for high density MIM caps (Metal Insulator Metal capacitors) and double oxide transistors, that has been extensively used to realize low leakage high capacitance supply bypass. All the digital parts have been realize with standard cells in triple well to reduce interference with the analog parts. Separated supplies are used for analog and digital parts to reduce interference.

It is well known that standard cells are generally designed for high speed-high performance systems, and usually employ transistors that are greater than the minimum size. On the other hand in this application the clock frequency is about 10 MHz, that for a 90 nm technology implies that the leakage power of the gates is dominant with respect to the dynamic power due to the switching activity. As result of that, the power of the digital part is given almost by the leakage, that is excessively high because of the standard cell. This can be dramatically reduced by redesigning the logic cells to operate at a lower frequency applying the techniques adopted for ultra-low-power digital design (high threshold devices, lower W, lover supply voltage, sleeping transistors). However standard cell design has been preferred because of design time constraints and because the optimization of the digital circuits is out of the purposes of this work.
As will be discussed later, the circuit requires about 200 bits for programming the PLL, the transceiver and for the digital calibration of the analog parts.

These bits are provided by a Serial to Parallel Interface (SPI) interface, designed by Nathan Pletcher and Simone Gambini, Graduate Students at EECS, UC Berkeley.

2.1 Transceiver Overview

Figure 2.1 shows the block diagram of the implemented transceiver. The chosen nominal pulse rate is 20 kpps.
The main building blocks, that will be discussed in this chapter, are the transmitter, the receiver and the PLL for the clock recovery/generation. As previously described, the received pulses are used to synchronize a local PLL. The PLL frequency has been chosen equal to 10.24 MHz, that is 512 times the 20 kpps pulse rate. This results in a time resolution on 97.7 ns for the local clock.

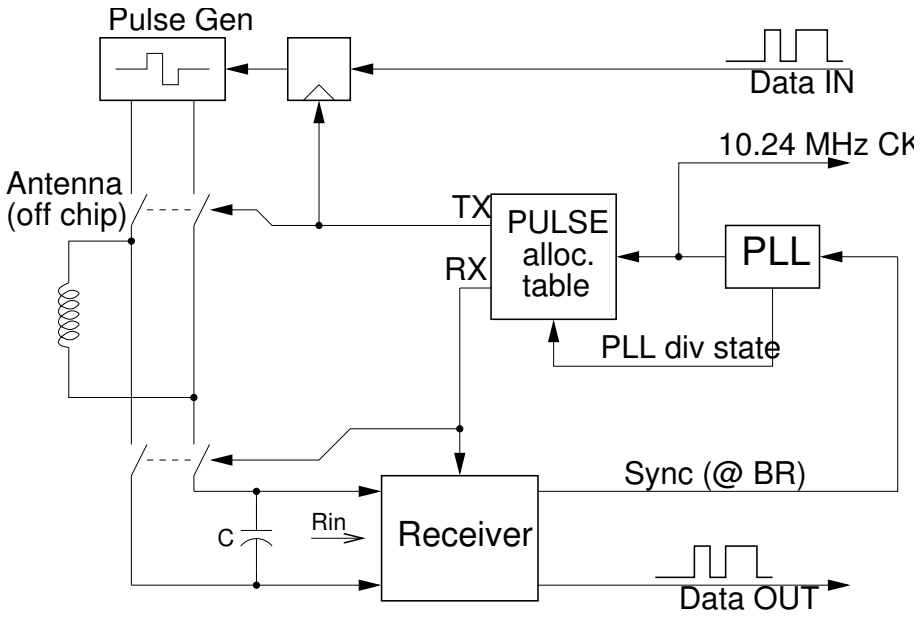

Figure 2.1: *Transceiver block diagram*

2.2 Transmitter

The purpose of the transmitter circuit is to force a square pulse on the antenna.
To achieve the maximum swing of the voltage, a differential bridge topology has been used, as shown in figure 2.2 [3] together with the signals waveform.
In absence of losses due to the MOS transistors and the inductor finite Q, and

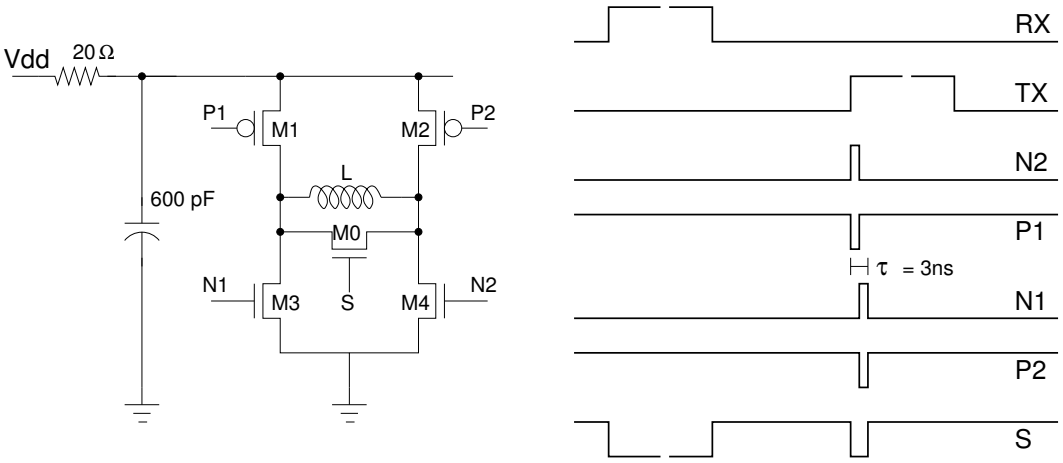

Figure 2.2: *Transmitter and transmitter signals*

considering that the inductor is a very bad antenna and it does not irradiate power, the transmission of the pulses ideally does not cost power. Assuming the transmitted pulse is "1", during the first semi pulse the current flows from Vdd through M1 and M4 down to ground. During the second pulse instead, the current is forced by the inductor through M2 and M3, and again through the power supply. The opposite phases act if the transmitted pulse is "0". If an RC filter with a proper cut-off frequency is used to power the bridge, during the second semi-period the charge is re-injected into the capacitor by the inductor, and (part of) the energy is recovered. Moreover, the capacitor acts as a charge tank and provides the peak current, that can be relatively high, without loading the Vdd line. In this case, with a theoretical 76 nH inductor and a 3 ns pulse, the peak current is 20 mA.
The transistor M0 is switched on at the end of the pulse and shorts the antenna. This operation damps any current still stored in the inductance caused by a not perfect symmetry between the two phases of the pulse. The transistor M0 is then switched off during the reception phase.
Figure 2.3 shows the generation of the transmitter signals, together with the

voltage and current waveforms and spectrum.
When the voltage pulse is applied to the inductor, because of the finite resis-

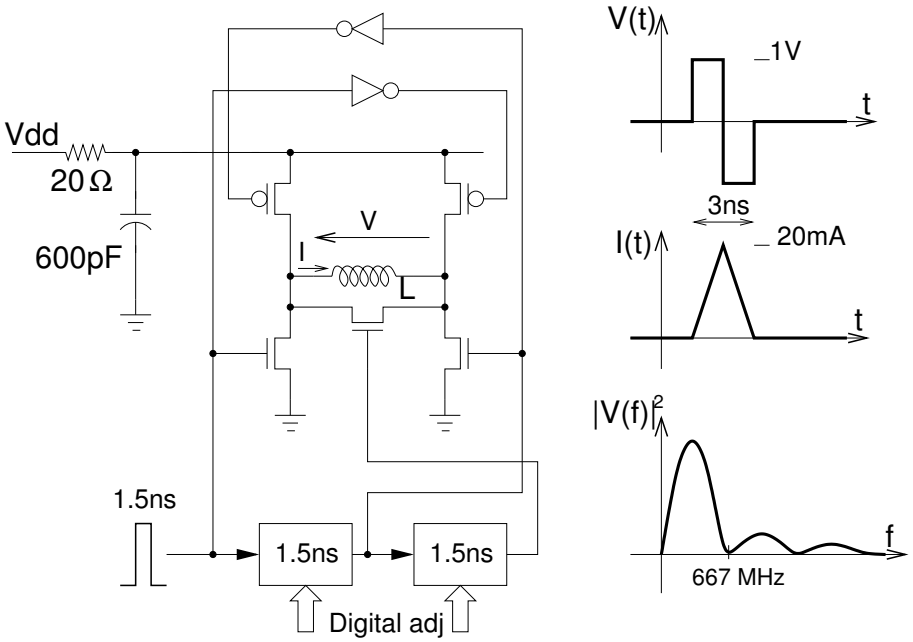

Figure 2.3: *Transmitter delays and signal generation*

tance of the MOS transistors and the current drawn by the inductor, the real voltage signal across the inductor differs from the theoretical one of figure 2.3. Being R_{ON} the ON resistance of the transistor in the bridge, figure 2.4 shows the power spectrum of the voltage applied to the antenna as a function of the MOS resistance. 50 Ω series resistance can be achieved with relatively small transistors and do not degrade the signal in an significant way. Post layout simulation results of the transmitter outputs are shown in figure 2.5.

2.2.1 Transmitter control logic

The 3 ns pulse is generated by means of an analog tunable delay (programmable delay line) and an asynchronous logic network sketched in figure 2.6. The programmable delay line is similar to the ring oscillator described in section 2.6.1 and to save power it is activated only 1 CK period before the transmission. This means that the delay line is active only for two clock period each transmitted pulse; with a bit pulse rate of 20 kpps and a clock at 10.24 MHz, the delay

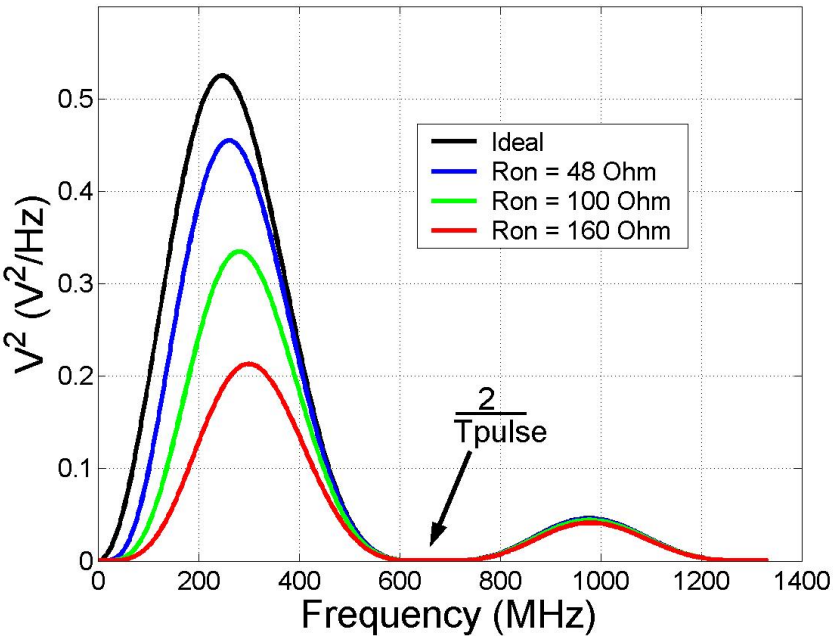

Figure 2.4: *Transmitter voltage spectrum*

line bias current of 57 μ results in the negligible average power of 220 nW. An external signal *TXforce* can be used as trigger to force the transmitter. This input will be used for testing the transceiver up to the maximum operating pulse rate, when the receiver is active all the time and the transmitter pulses are packed one after the other. Simulation shows that the maximum achievable pulse rate should be in the order of 200 Mbps that, however, requires a very high SNR and therefore a reduced distance between the transmitter and the receiver.

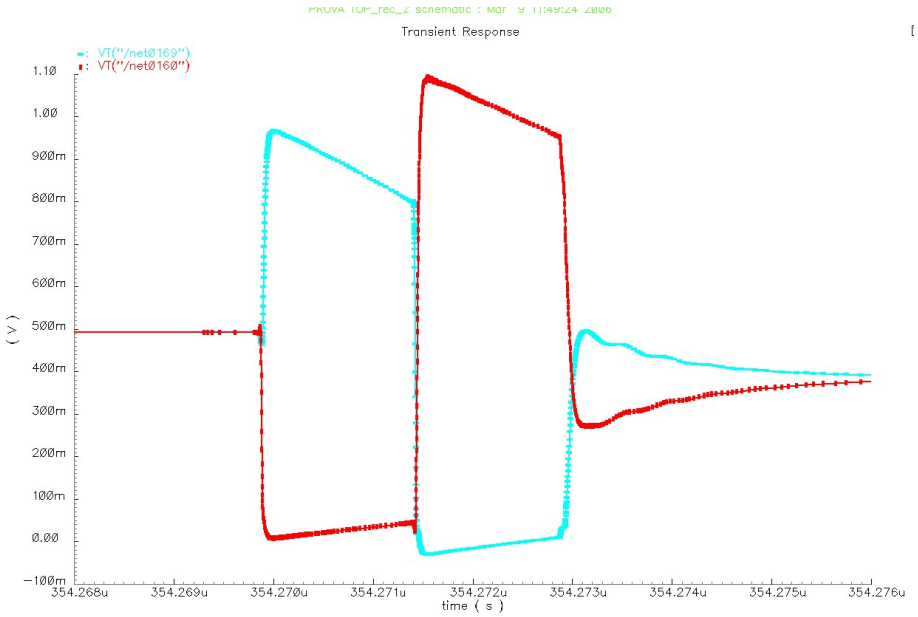

Figure 2.5: *Simulated transmitter output voltage*

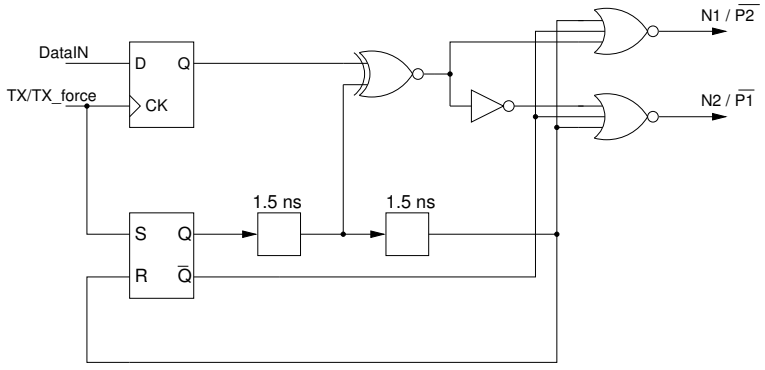

Figure 2.6: *Transmitter Logic*

2.3 Receiver

The receiver should amplify the received signal and detect its polarity so to recognize "1" and "0". The receiver block diagram is shown in figure 2.7.
Since the channel is supposed to be noise limited, only the noise will be con-

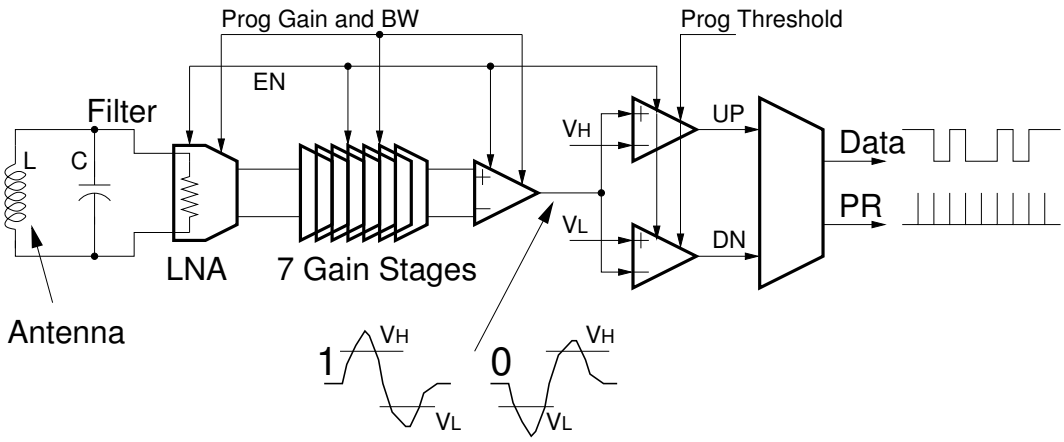

Figure 2.7: *Receiver block diagram*

sidered and the receiver can operate in a pure energy detection mode (asynchronous or incoherent receiver).
In a fully asynchronous implementation, the amplifier stage must completely recover the attenuation due by the channel. The receiver is therefore an amplifier whose gain is equal to the channel attenuation (80dB) and the total bandwidth is equal to the signal bandwidth (in this chapter the signal bandwidth is assumed to be the bandwidth of the first lobe of the transmitted spectrum of figure 1.5).
Similar gain and bandwidth cannot be achieved with a single stage, therefore the receiver has been splitted in 3 main parts:

- LNA: like in every receiver, the first stage provides a high gain with low noise, so that its output signal is relatively strong with respect to the noise of the following stages. To maximize the supply and substrate noise rejection, a fully differential implementation is mandatory.

- Gain Stages: after the LNA a certain number of gain stage is required to amplify the signal up to a level detectable by the comparators.

- Differential to single-ended Converter: because the comparators are realized in a single-ended topology, a differential to single-ended converter

is needed at the end of the amplifier chain. Note that at the input of this last stage the signal level is relatively high and therefore almost insensible to supply and substrate noise.

- Comparators: the comparators compare the received signal with a couple of threshold, so to determine if the received pulse is either a "0" or "1"

- Logic network: the outputs of the comparators feed a logic circuit able to determine the pulse polarity.

Note that for duty cycling the receiver, it must be capable to be switched off and on periodically. If a few ns switch on and off time is required, it means that all the time constants within the amplifier must be lower than 1 ns, that agrees with the amplifier bandwidth to be in the order of 1 GHz.

2.3.1 LNA

In order to minimize the noise figure of the system, an LNA with a real input impedance is used; in this way an ohmic "noisy" resistor is not required to realize the RLC filter since the real part of the LNA input impedance can be used.
Because of the inductive nature of the link, inductively degenerated LNA is not considered to avoid interference between the antenna and the degeneration inductance. Moreover the wide band nature of the signal recommends to use a broad band LNA. Common gate or shunt feedback LNAs seem to be the best choices. However, as shown in [8], combined common gate - shunt feedback LNA achieves the same input impedance using only one quarter of the current. The schematic is shown in figure 2.8, together with the transistor sizing.
The LNA has been designed to achieve the required 78Ω real input impedance that is given by

$$Z_{in} \simeq \frac{1}{4g_m} \tag{2.1}$$

where g_m is the transconductance of the N or P mos.
From the previous equation

$$g_m \simeq \frac{1}{4Z_{in}} = 3.21\mu A/V \tag{2.2}$$

and assuming $g_m/Id = 20$ this results in a (minimum) bias current of 160 μA for each branch. The effective bias current to ensure the proper input impedance

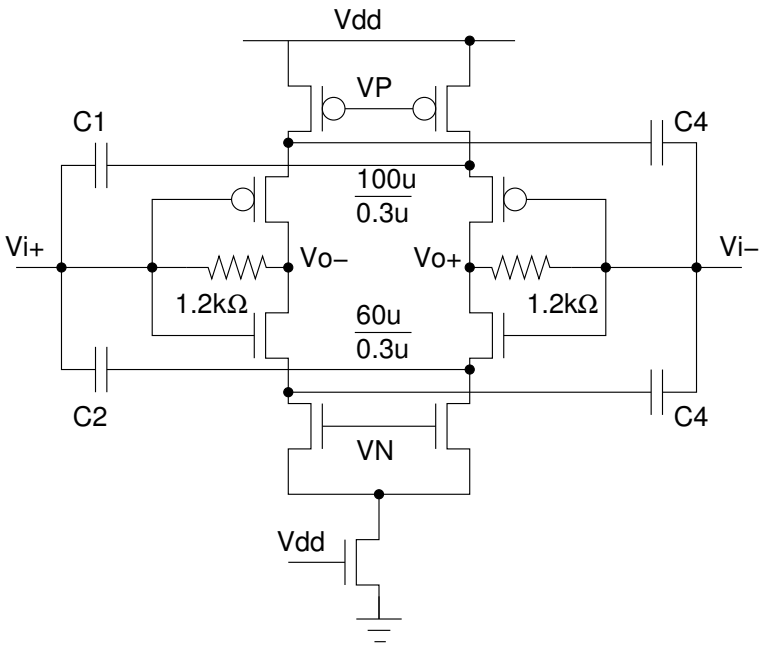

Figure 2.8: *SF-CG LNA*

has been chosen equal to 200 μA.

It should be noted that the input capacitance of this amplifier is not very critical, because it is resonated out by the antenna (some extra capacitance must be added to reach 8 pF of differential capacitance required). This allows one to increase both the W and the L of the transistors, to to achieve a higer transistors output resistance and then a higher gain. On the other side, 4 transistor (plus the dummy switch M0) must be stacked in 1 V and must be carefully designed to avoid triode region operation of the current sources.
The coupling capacitors C1-C4 (20 pF each one) give a high pass behavior in the transfer function, that does not affect the signal since it has very low power spectral density at low frequency (figure 2.4).
Due to the different DC levels, the LNA is AC coupled with the following stage. Coupling capacitors are used for the cancellation of LNA output offset also, in a fashion similar to the one described later for the gain stages.
Because of the input coupling capacitance needed by the LNA, the turning on time of the LNA is relatively long. The capacitances must reach the nominal bias voltage before the LNA get ready to correctly operate. With a bias current of 200 μA for each branch and with 20 pF, 100 ns enables the capacitance to be charged up to 1 V. For this reason in duty cycle mode it is turn on 1 CK

period (97.7 ns) in advance with respect to the following stages.
Simulation shows a differential gain of 21.5 dB and a 3 dB bandwidth from 20 to 950 MHz. The real part of the input admittance ($\mathcal{R}\{Y_{in}\}$) is shown in figure 2.9.

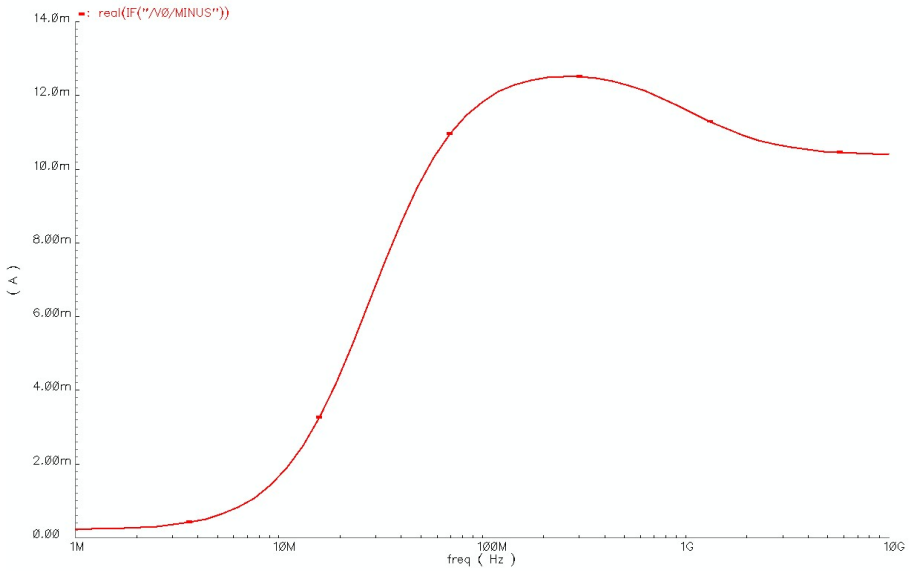

Figure 2.9: *Real part of the LNA input admitance*

2.3.2 Gain Stages

The amplifier is implemented with 7 stage 8 dB differential gain. The schematic of the single stage is shown in figure 2.10.
Because of the broad band nature of the input signal, a broad band stage has been used. A resistive load approach has been preferred to a PMOS saturated load because it does not need a common mode feedback circuitry, and because the higher bandwidth than can be achieved thanks to the very small parasitic capacitances of the poly resistors with respect to the PMOS.

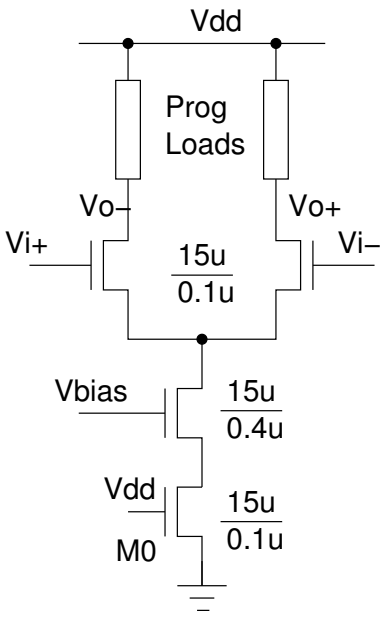

Figure 2.10: *Amplifier Stage*

Design Consideration

The stages have been designed to optimize the ratio between the gain expressed in dB and the bias current, so to achieve the maximum gain for the minimum current over the required bandwidth.
The design optimization has been performed in *MATLAB* starting from simulation data. Some considerations on the design are summarized here.

As mentioned before, the required gain is in the order of 80 dB for the whole chain. In the hypothesis that the LNA has 20 dB gain and the differential to single-ended stage has 10 dB gain, the required gain for the gain stage chain is about 50 dB.
It is well known that achieving high gains with a single stage requires to use non minimal length transistors, because of the limited g_m/g_d ratio (about 10 in 90 nm technology). Moreover the use of resistive loads instead of active ones, limits the maximum available load for the stage to be compliant with the saturation of the transistor.
With a reasonable per-stage gain around 7 dB (2.24), a 50 dB gain can be realized with 7 stages. This means that, with a single pole model for the amplifiers, the bandwidth of each stage must be 7 times the bandwidth required for the whole chain.

Gain	$A_v = 2.24$
Bandwidth	$B = 3.15$ GHz
Load	$C_L = 50$ fF

Table 2.1: Differential stage requirements

In section 1.2 the bandwidth of the input signal has been assumed to be limited at the first lobe (666 MHz). However to get the maximum signal to noise ratio, the received signal must be filtered with a bandpass filter with a center frequency $f_0 = 204$ MHz and a quality factor $Q = 0.8$, as described in section 1.4.
With a 204 MHz center frequency and $Q = 0.8$, the upper bandwidth of the signal is limited at $f_0(1 + 1/(2Q)) = 335$ MHz; a 450 MHz bandwidth for the amplifier chain is reasonably enough to preserve the signal integrity. This constraint results in a 3.15 GHz bandwidth for each stage.
The load is given by the load resistor R_L and the input capacitance of the following stage, plus the interconnection lines. A load capacitance C_L of 50 fF on the last stage has been assumed during optimization, to takes into account for the quite large input capacitance of the differential to single-ended converter. The same total load capacitance, probably overestimated, has been assumed for every stage of the chain.
The requirements for the amplifier are summarized in table 2.3.2.

With a single pole model for the amplifier, and neglecting the transistor output resistance, it is

$$A_v \simeq g_m R_L \tag{2.3}$$

$$B \simeq \frac{1}{2\pi R_L C_L} \tag{2.4}$$

that gives

$$R_L = 1.01\ k\Omega \qquad\qquad g_m = 2.22\ \text{mA/V}$$

Assuming the transistor in sub-threshold operation with $g_m/I_d \simeq 20$, a minimum bias current of 111 μA is required, that gives a minimum bias current of 222 μA for the differential pair.

A more detailed model for the transistors, taking into account the effective $g_m(I_d)$ and $g_d(I_d)$ relationships, has been used for the design. The resulting optimal bias current is 300 μA per stage and the transistor sizing are shown

in figure 2.10. The nominal load resistance turns to be 1200 Ω.
Simulation shows a gain of 8.8 dB with a -3 dB bandwidth of 3 GHz at nominal condition and bias, when the stage is loaded by another stage and 10 fF capacitances to ground that take into account for interconnections. It should be noted that, since the transistors operate in sub-threshold/weak inversion region, the gate source capacitance is proportional to the bias current (like in a bipolar transistor) and usually it is small compared with the overlap capacitance, enhanced by the miller effect, and the interconnection ones.
The bias current is programmable around the nominal value; the loads are programmable as well, in order to compensate for variation of gain and bandwidth due to the current adjustment. The programmable load schematic (just one side) is shown in figure 2.11.

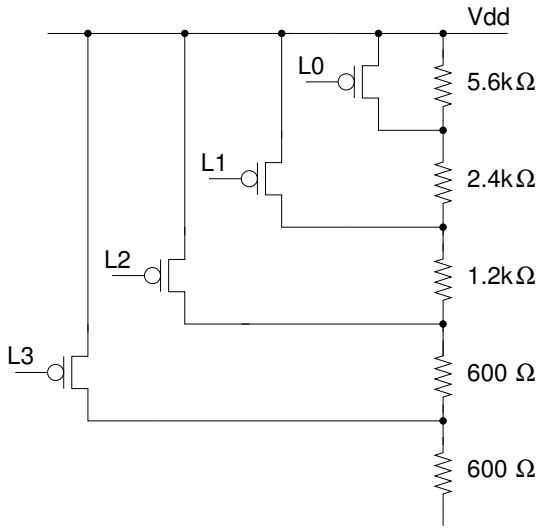

Figure 2.11: *Programmable load of the amplifier stages*

Offset cancellation

Clearly a 50 dB gain amplifier is quite sensible to the input offset, given by process mismatches in the transistors and load resistors; an offset cancellation technique is needed to avoid the saturation of the amplifier because of its own offset.
Because of the small gain of the stage (about 2.5 in linear scale) and the relatively low input offset due to the differential pair mismatch (5 mV), the offset cancellation has been performed once each two stages, by means of coupling

capacitors and switches, as shown in figure 2.12 together with the voltage waveforms.
When the stages are off (EN=0) all the outputs potentials move to V_{DD} and the

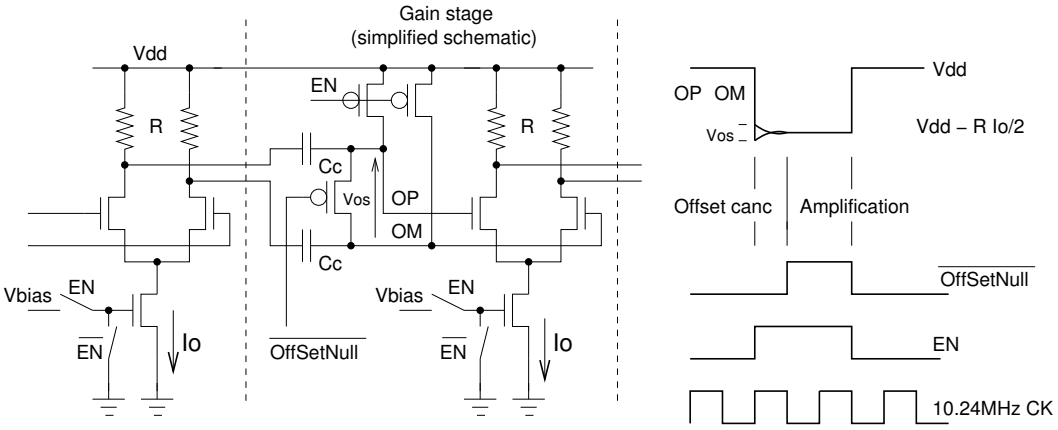

Figure 2.12: *Offset Cancellation*

coupling capacitors C_c are discharged by means of PMOS transistors. When the stages is enabled (EN=1) the outputs moves to the nominal bias voltage (800 mV), and the following stage is biased through the capacitors at the same voltage. To remove the offset propagation, the input of the following stage are shorted for half CK period ($\simeq$ 50 ns) so to equalize the bias voltages on the inputs; when the short is released the inputs remain at the same bias voltage and the transistors are biased at $V_{GD} \simeq 0$.
Note that this "dynamic" bias works only because the amplifier is kept on for short time intervals, during which the capacitors C_c can keep the bias point almost constant.
A branch realized with PMOS transistor in diode configuration and not shown in figure 2.12 is used to static bias the stages when the amplifier is kept on for a long period of time. In this case the coupling capacitors and the bias transistors result in a high pass behavior in the global transfer function of the amplifier; since the signal spectrum has a band pass shape (figure 2.4) this property turns to be useful to remove flicker and low frequency noise without limiting the signal bandwidth.

2.3.3 Differential to single-ended converter

The 7 stages amplifier is followed by a pseudo-differential Differential to Signal-ended converter. This circuit is needed to drive with a rail to rail signal the

comparators.
The differential to single-ended amplifier is shown in figure 2.13. It has been designed to allows for the maximum output swing assuming a 50 fF load.
Because of the different common mode with respect to the output of the pre-

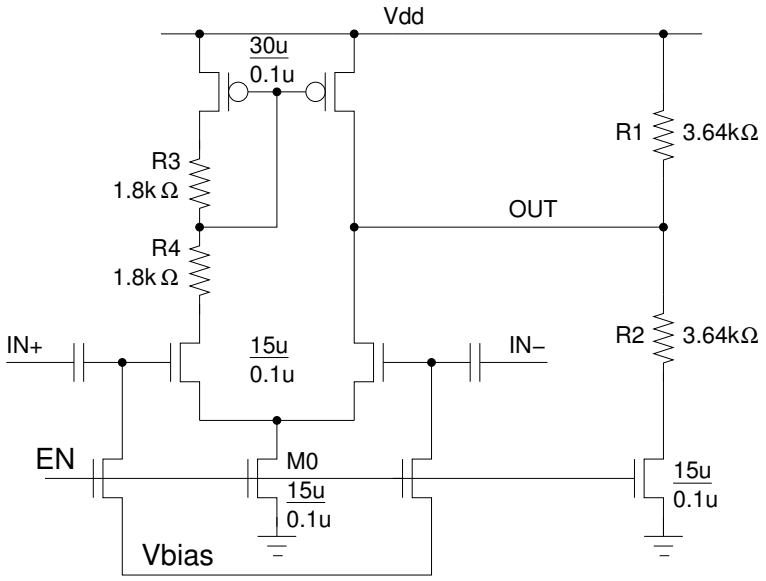

Figure 2.13: *Differential to single-ended amplifier*

vious stage, an AC input coupling is mandatory.
Resistors R_3 and R_4 in figure 2.13 bias the PMOS current mirrored transistor with the same V_{DS} while showing the same (dynamic) load to the differential pairs. Since this stage is pseudo-differential (transistors M0 is only used to switch off the amplifier and it is not a current source) R_3 and R_4 have been designed to minimize the common mode gain. Resistors R_1 and R_2 perform the current to voltage conversion with high linearity.

The simulated gain (differential to single-ended) is 7.1 dB with a -3 dB bandwidth of 1.7 GHz on a 50 fF load. The nominal bias current is 160 μA (plus 137 μA in the resistors R_1 and R_2). The bias current is programmable though 16 levels, as will be described in section 2.4; the load resistance are fixed. Since this amplifier works almost with rail-to-rail single-ended signals, is has been connected to the digital power supply instead of the analog one. This should avoid single-ended feedback to the differential input through the supply line.

2.3.4 Comparators

For maximum simplicity and low power, the comparators have been realized using two inverters whose threshold have been moved by means of source followers, as shown in figure 2.14.
The threshold of the comparators can be varied by adjusting the bias current

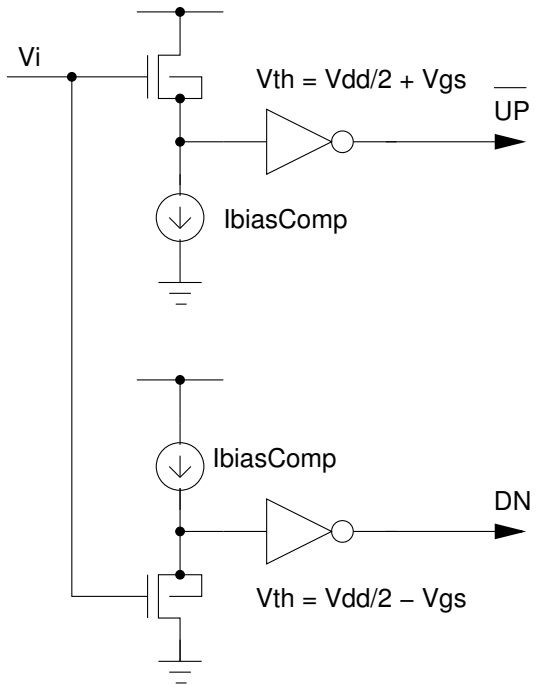

Figure 2.14: *Comparators*

into the followers. The NMOS is realized in triple well in order to have $V_{SB} = 0$ for every value of V_i (such as for the PMOS in N-well).

2.3.5 Data and Clock Recovery

A simplified schematic of the data and clock recovery circuit is sketched in figure 2.15, where UP and DN represent the outputs of the comparators.
The output *bitSync* is activated for each pulse received, while $CKout$ only when a pulse is received during the CK window.

To improve the noise immunity of the system and avoids that a noise spike produces an error in the output signal, a pulse is recognized and detected only when both comparators switch between a time interval that is not greater

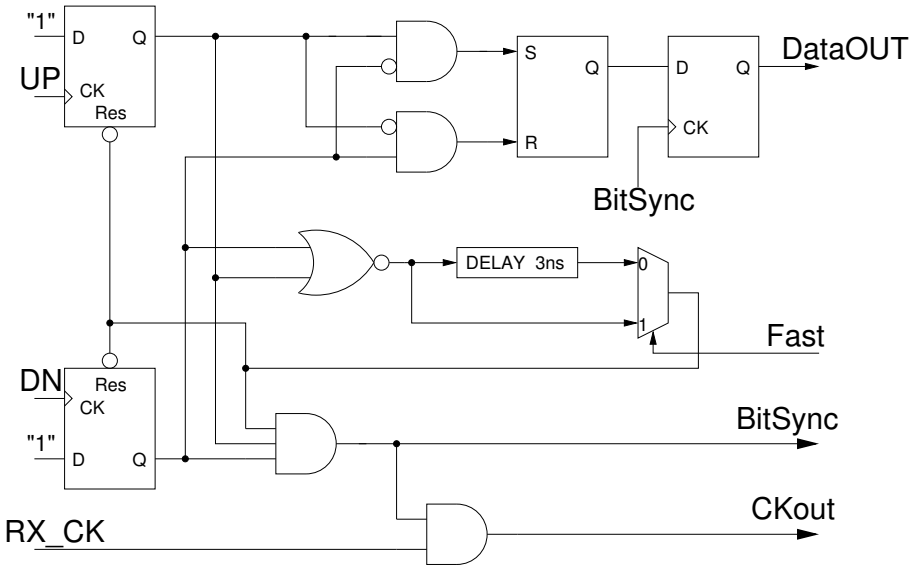

Figure 2.15: *Data and clock recovery circuit*

than the duration of the pulse itself. The second pulse of the opposite polarity should follow the first with a maximum delay, otherwise the pulse is not considered. Since the presence of this delay in the data recovery circuit slows down the maximum achievable pulse rate, this features can be disabled by means of the signal *Fast* to operate at very high pulse rates.

2.3.6 Receiver control logic

For maximum simplicity of design, the control logic is based on a 8 states Gray counters. The outputs are then combined to generate the signals needed to enable the receiver. The Gray counter, instead of a standard binary one, is use to avoid critical races into the logic that generates the signal.
Because of the temporizing required, the counter must be triggered 3 clock period in advance to the clock edge when the pulse is expected. The generation of the trigger signal is described in section 2.7, while the signals are shown in figure 2.16.
At the beginning of the reception phase the LNA is activated 1 CK period before the desired reception window. After half clock period the offset cancellation phase for the LNA is completed (its outputs are unshorted) and at the same time the amplifiers and the differential to single-ended converter are enable. After another half clock period the offset cancellation phase is completed for the amplifier and the comparators are activated. Then the system

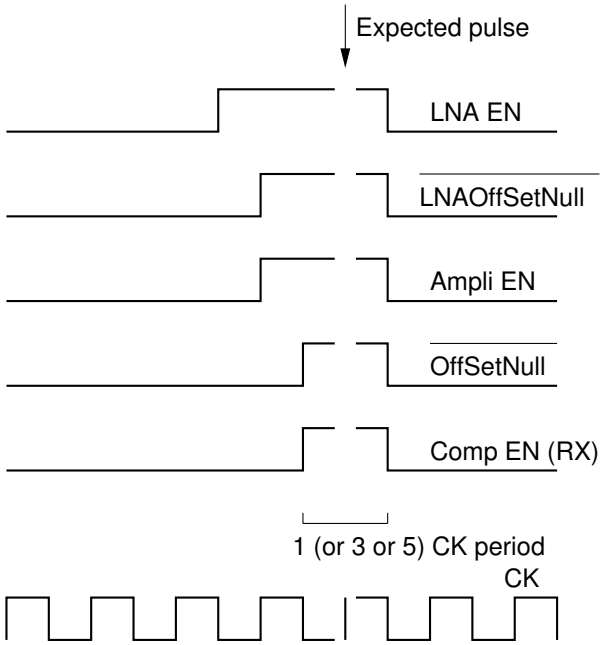

Figure 2.16: *Enabling signals in the receiver*

is kept on (reception window) for a programmable time variable between 1 to 6 ck period, and at the end all is switched off and all the differential outputs are shorted together.

2.4 Bias circuits

All the bias circuits have been implemented according the PTAT circuit (Proportional To Absolute Temperature) of figure 2.17 in order to have a constant g_m over temperature variations [9].
The current is programmable though 4 bits (16 theoretically equal levels) by means of 4 binary sized PMOS operating in deep triode region. The nominal bias current is set with the configuration "1000", in order to have the maximum possible range above and below the nominal bias point. The transistor M0 is used to switch off the bias circuit in stand by mode. Transistor MX and MY are then used to shorted the bias voltage on the cells. The letters a and b in figure 2.17 are referred to the relative ratio of the transistors [9].

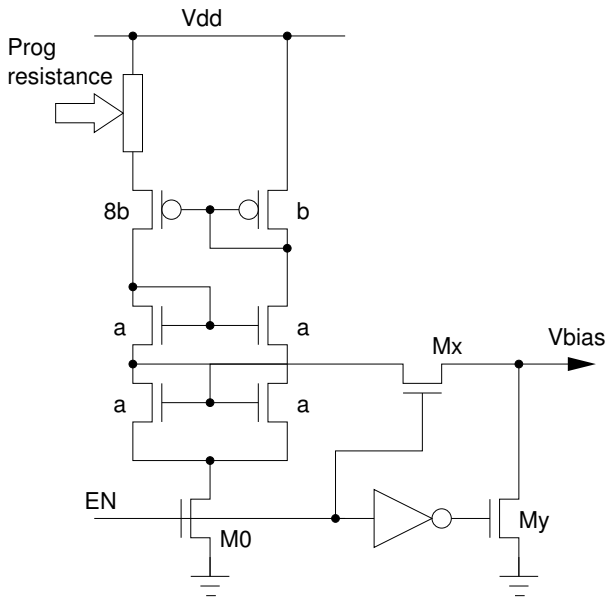

Figure 2.17: *Bias Circuit*

2.5 Amplifier simulations

Figure 2.18 shows the simulated gain of the receiver chain (LNA, 7 differential stages and differential to single-ended converted) in standard bias condition and for TYP-Rtyr-Ctyp, SS-Rmax-Cmax and FF-Rmin-Cmin corners at 27^oC. In TYP condition the gain is 79 dB and the bandpass from 40 to 740 MHz. Only small variation in the in-band gain can be observed through the corners, and can be easily compensated by means of the digital calibration of bias currents and loads. The big difference in the low frequency part of the curves is due to the AC coupling between the stages (the corners are considered for MIM cap also). The total bias current in TYP condition (including the bias circuits and the comparators, is 3.75 mA.

Figure 2.19 shows the voltage at the differential to single-ended output node in duty cycled mode. When the amplifier is off the output is equal to $V_{DD} = 1\ V$. Then the amplifier is activated and the first half clock ($\simeq 50$ ns) is used to switch on the chain and to cancel the offset, as previously discussed. After that the amplifier and the comparators are active for a programmable time from 1 to 5 clock periods. In figure 2.19 the received pulse is exactly in the center of the window (whose duration is one clock period, hence 97.7 ns).

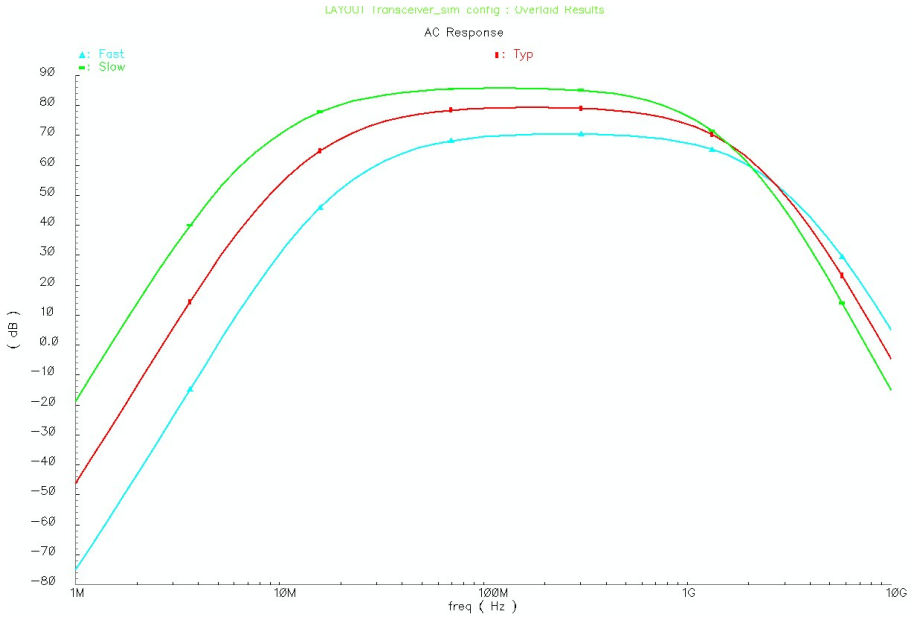

Figure 2.18: *AC gain of the Receiver chain*

Great concerns in this design come from the stability issues of an amplifier with such an high gain and bandwidth. Post layout simulations across corners show a minimum stability factor around 7.

Because of the single-ended nature of the last stage (even if it is supplied by the digital power line), another source of concern is the feedback through the supply and the ground from the output to the input. The amplifier has been simulated considering 1 nH bondwire inductance on every supply and ground lines. Figure 2.20 shows the LNA input sum and difference in correspondence or a received pulse. The common mode has almost the same amplitude of the differential mode and is easily reduced by the high amplifier CMRR. No oscillation is found (in agreement with the stability factor greater than 1).

Finally figure 2.21 shows the output noise power spectral density (V^2/Hz). As expected the maximum of the noise is allocated within the signal bandwidth. The square output effective noise is given by

$$V_{n,eff}^2 = \int \frac{V_n^2}{\Delta f} \mathrm{d}f = 0.0113 V^2$$

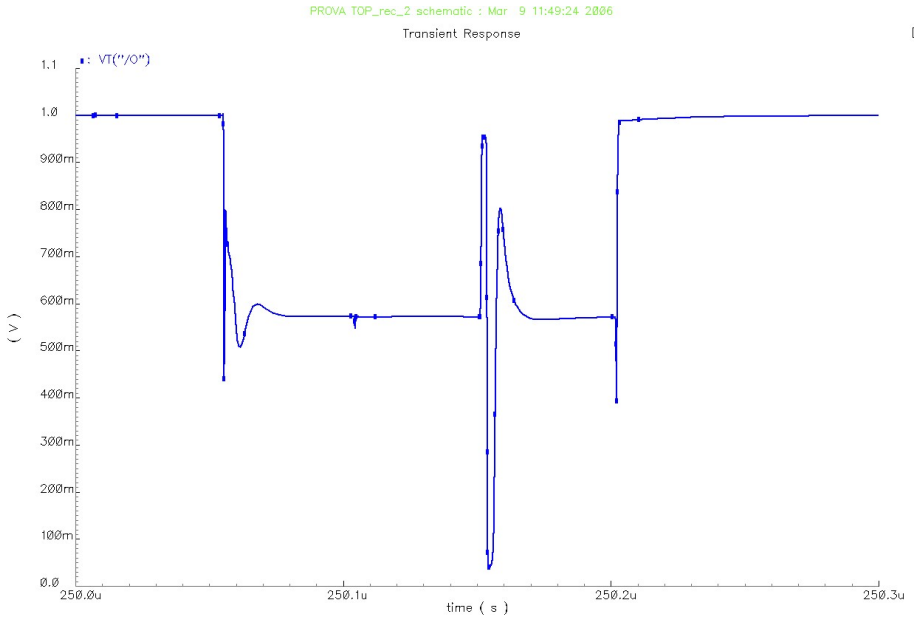

Figure 2.19: *Receiver chain output*

and therefore the effective noise is

$$V_{n,eff} = \sqrt{0.0113} = 0.104\ V$$

Assuming the output signal rail from 0.1 to 0.9 V, the output peak over noise ratio can be written as (equation 1.20)

$$\text{SNR} = \frac{V_p^2}{V_{n,eff}^2} = \frac{(0.9/2)^2}{0.0113} = 15.6 \simeq 12\ dB$$

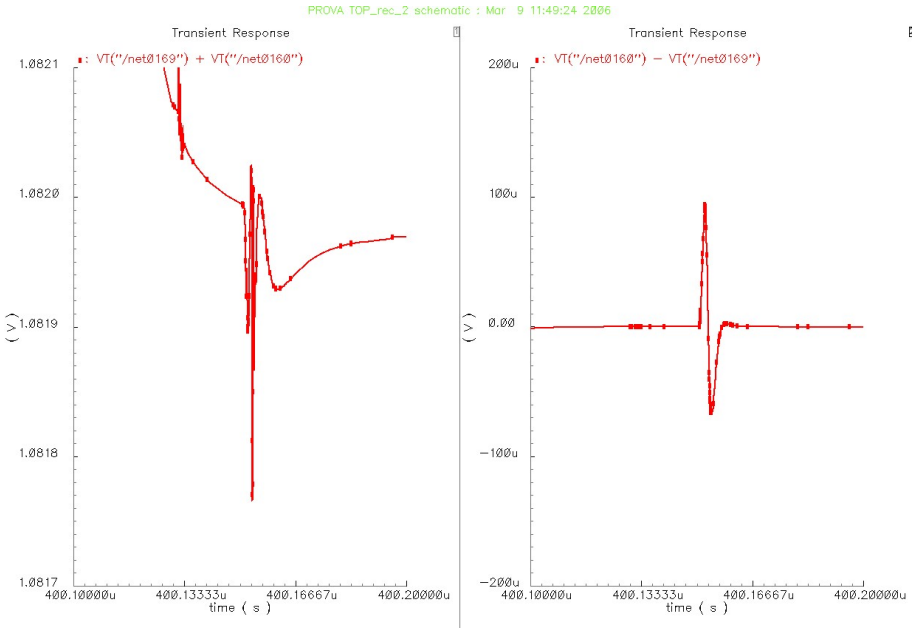

Figure 2.20: *LNA inputs sum and difference*

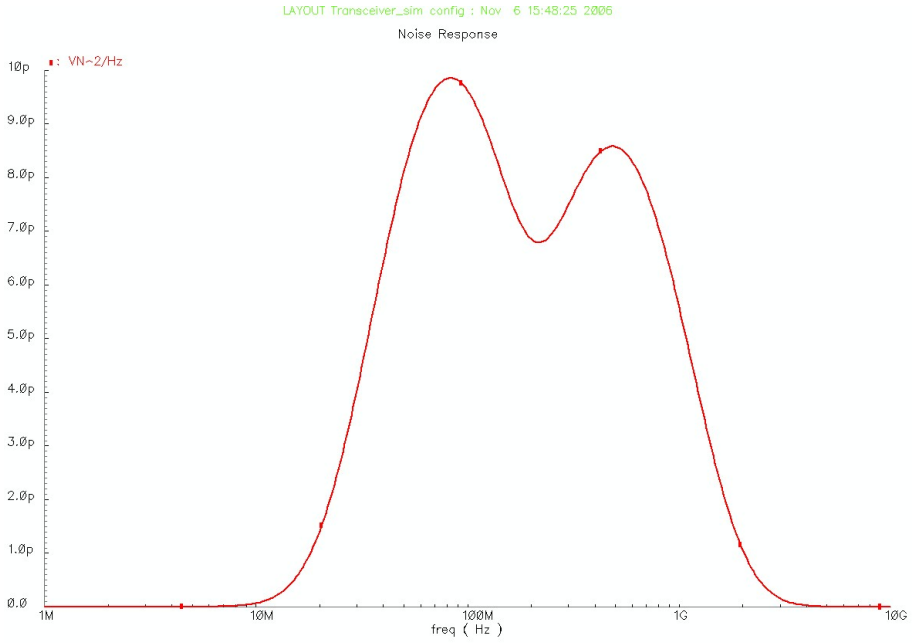

Figure 2.21: *Amplifier output noise*

2.6 PLL and Synchronization scheme

As previously stated, in order to duty cycle the system a local time base is needed on the receiver. Moreover this time base must be synchronous with the transmitter one. Instead of using crystal oscillator to keep the time base, this design exploit a high level of integration and looks for synchronization techniques that do not require for a precise time base on the receiver. As described in section 1.5, the local time base is kept by a Phase Locked Loop that is locked on the incoming data stream, as shown in figure 2.22.
Assuming that the minimum time interval required the circuit is 100 ns, and

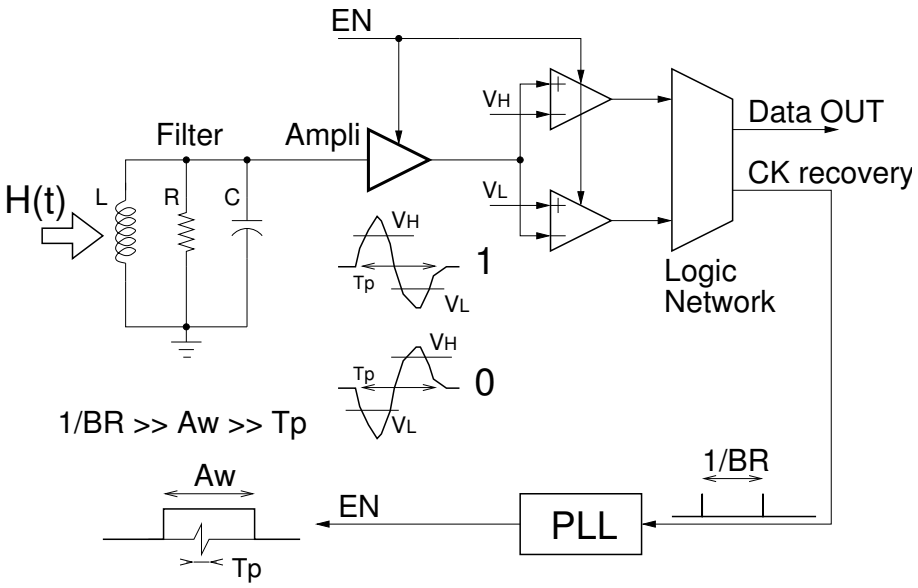

Figure 2.22: *Receiver block diagram*

the nominal pulse rate is 20 kHz, a 10.24 MHz PLL (512×20 kHz corresponds to a 97.65 ns period) has been designed.
This PLL (see figure 2.23 for a block diagram) is used as internal clock for the node and therefore also to drive the transmitter of the same node. This means that the jitter added by the PLL itself degrades the time accuracy of the signal that is propagated to the next nodes. Because of this, there is a maximum number on nodes through which the synchronizatin can be propagate. For a larger numbers of hop the jitter accumulated on the pulse times becomes so high that the receiver does not work anymore (see [7] for further details on the synchronization).

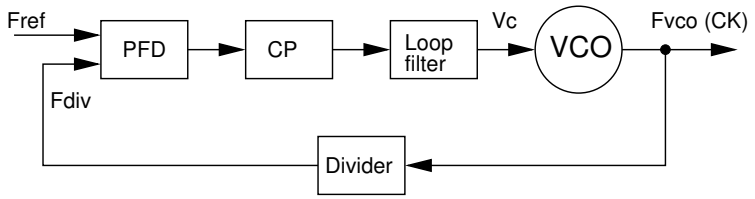

Figure 2.23: *PLL block diagram*

To increase the flexibility of the system, the PLL has been modified in order to accommodate 5 different pulse rates. These pulse rates are 20, 40, 80, 160 and 320 kbps, programmable by changing the division ratio in the frequency divider and adjusting the pole, the zero and the gain of the loop filter. For test purposes, an external clock can be injected into the chip through a proper pin. This can be used to vary the clock frequency over the VCO tuning range or to test the receiver in case of problems with the PLL. Furthermore, the PLL output can be carried out of the chip to test the PLL functionality and phase noise.

In the next paragraph the PLL building blocks are described in details.

2.6.1 VCO

For low frequency and low power controlled oscillators, when external tanks or MEMS are not considered and jitter (or phase noise) specification are not too stringent, ring oscillators are widely used.
The single-ended ring oscillator is realized with 9 current starved inverters (one stage plus the bias circuit is shown in figure 2.6.1). Single-ended implementation has been preferred to a differential one because of the reduced power consumption and the rail-to-rail output signal that can directly drive digital circuits.
Since the control voltage acts on the PMOS, the VCO pulling factor K_{VCO} is negative, and the PLL requires a (180^o) phase inversion in the loop, that is achieved by the active loop filer.
The VCO has been designed to get the maximum V_{gs} over the current starving transistor compliant with the required oscillation frequency over the process variations and temperature, in order to achieve the minimum phase noise [10]. The current consumption of the oscillator is about 15 μA. Actually this current relatively high and can be reduced by reducing the width of the transistors; however this would result in a higher VCO jitter. Since the jitter added by the PLL pollutes the purity of the clock signal from one node to the next, in this

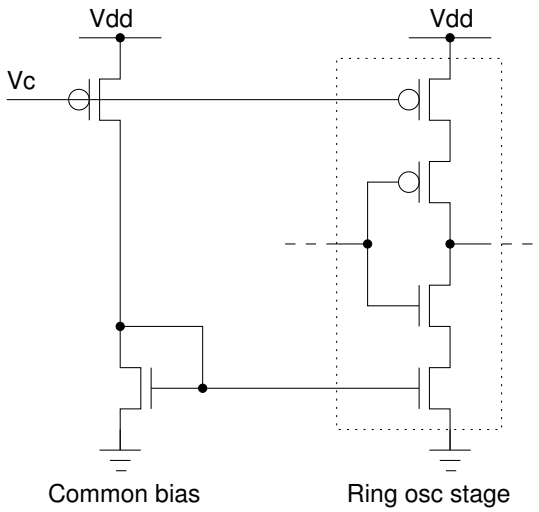

Figure 2.24: *Ring oscillator stage (+ common bias)*

first implementation it was preferred to spend a few more microamp instead of risking a lock failure.

2.6.2 Frequency Divider

The divider has been realized in a synchronous fashion with standard cells (as the rest of the logic blocks of the system). This is perfectly allowed by the fact that 10 MHz is an extremely low frequency for a 90 nm technology. The divider logic diagram is shown in figure 2.25.
Since the state of the PLL divider represents the state of the system for the synchronization mechanism, and the state "0" (when the frequency divider state reaches "0" the divider edge is generated and the reference edge is expected) is the state when the PLL must resynchronized by the incoming pulse, a ripple carry adder is used to force a new initial state in divider, so to change the absolute time position of the "0" state. This adder is also used to increase by one the register content during the count, thus minimizing the divider hardware. The inputs "Speed_UP" are used to reduce the counting modulus (hence the division ratio) from 512 down to 256, 128, 64 and 32.
The divider output is resynchronize with the VCO output (CK) so to minimize the edges delay and jitter.

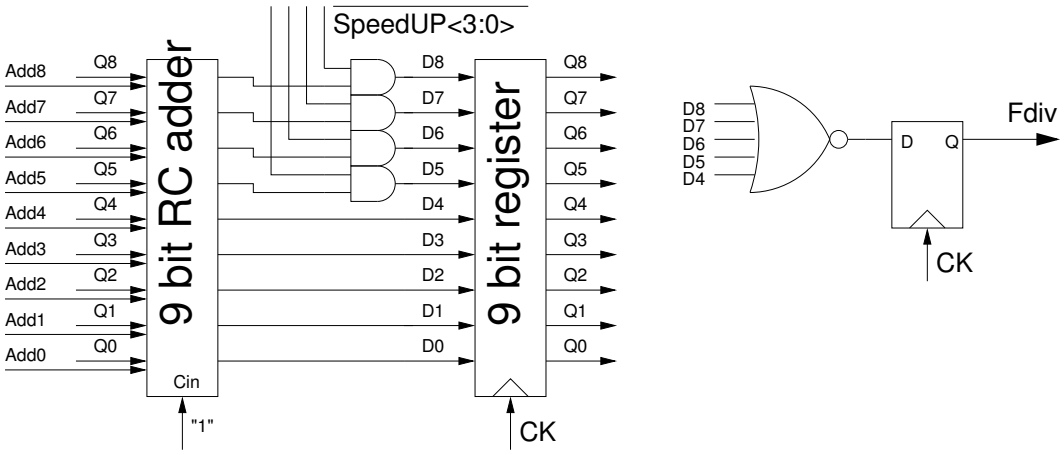

Figure 2.25: *Frequency Divider*

2.6.3 PFD-CP

The Phase and Frequency Detector (PFD) and the Charge Pump (CP) have been realize in an extremely standard way, as shown in figures 2.26 and 2.27 [11]. Because the PLL is integer, charge pump current mismatch and PFD dead zone are not so critical issues as in a fractional one [12]. Moreover the adopted loop filter reduces the sensitivity on the charge pump current mismatch [13]. The charge pump current has been chosen equal to 1 μA.

As will be discussed in the next section, because of the low cut of frequency

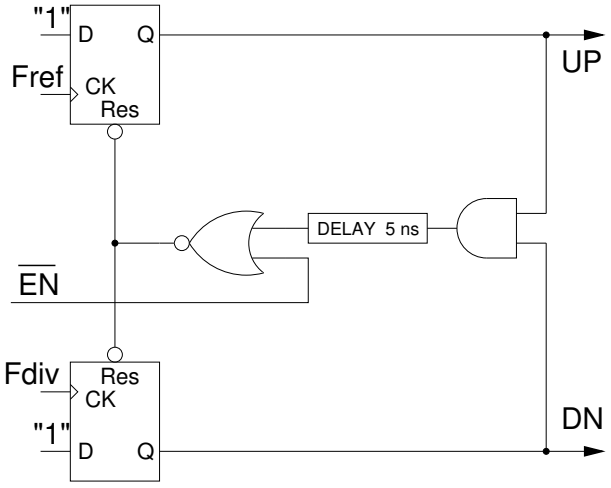

Figure 2.26: *Phase Frequency Detector*

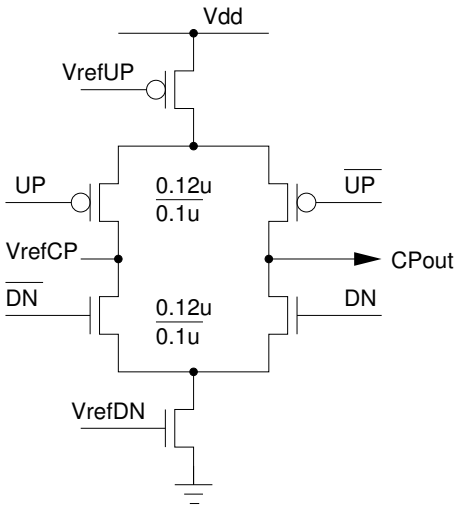

Figure 2.27: *Charge Pump*

of the loop filter, a lower charge pump current would be preferred to keep reasonable values of the filter capacitors and resistor. Anyway, control a current lower than 1 μA can result in high errors because leakage currents cannot be neglected when the charge pump is off. A technique to scale the charge pump injected charge by means of switched capacitors will be discussed in the next section.
The charge pump reference voltage has been integrated by means of a voltage divider. Its bias current is 2.5 μA.

2.6.4 Programmable loop filter

It is well known [14] that the open loop unity frequency of a PLL must be in the order of 1/20 of the reference frequency to get a stable loop.
Assuming a standard lead-lag network for the PLL filter (figure 2.28) the transfer function can be written as

$$F_L(s) = \frac{V_c}{I_{cp}} = \frac{1 + s\tau_z}{s(C_p + C_p)(1 + s\tau_p)}$$

with

$$\tau_p = R_z \frac{C_p C_z}{C_p + C_z} =\simeq R_z C_p \qquad \tau_z = R_z C_z \tag{2.5}$$

and the unity gain frequency turns out to be

$$\omega_c = \frac{I_{CP} R_z K_{VCO}}{N}$$

being I_{CP} the charge pump current, K_{VCO} the VCO pulling factor and N the division ratio.
With a reference frequency of 20 kHz, the required PLL bandwidth should be

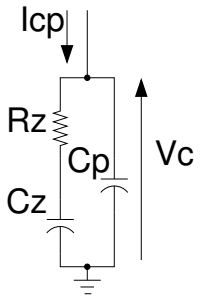

Figure 2.28: *PLL passive loop filter*

in the order of 1 Hz, that results in a very high capacitance and resistance values for the filter components.
For a 60^o phase margin, fixing the capacitance C_z to be 197 pF (about 0.1 mm^2), the components for a passive filter should be

$$C_z = 197\ pF \quad C_p = 8.25\ pF \quad R_z = 3.21\ M\Omega \quad I_{CP} = 62.5\ nA$$

It must be noted that both a 3.21 MΩ and a 62.5 nA current cannot be easily achieved. For this reasons switched capacitors have been strongly used in the filter design. With respect to PLLs made for wireless communication RF synthesize, in this particular application the output phase noise is less critical and the filter design can be relaxed.

The implemented PLL loop filter is shown in figure 2.29.
The switches driven by the non overlapping phases S (Share) and P (Pass), together with the capacitors C_1 and C_2 perform a charge scaling between the charge injected by the charge pump and the charge injected into the active loop filter. During the charge pump comparison $S = 1, P = 0$ and the charge is injected into C_1 and C_2. At the end of the comparison phase, the control logic deactivates S and activates P ($S = 0, P = 1$) and only the charge in C_2 is integrated by the loop filter, while C_1 is shorted.
The "effective" charge pump current is therefore given by

$$I_{CP,eff} = I_{CP}\frac{C_2}{C_1 + C_2} \tag{2.6}$$

With a charge pump current $I_{CP} = 1\mu$A it easy to obtain a 62.5 μA effective current by choosing $C_2 = 15C_1$.

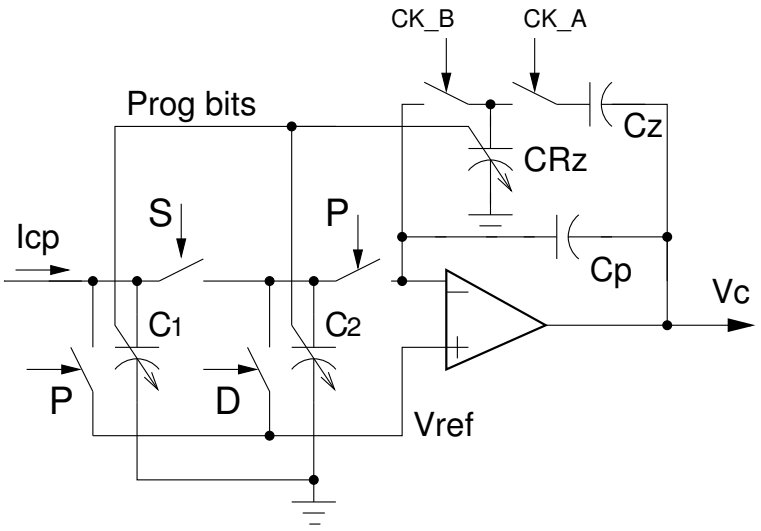

Figure 2.29: *PLL Programmable loop filter*

The switch D is used to dump the charge injected in C_1 if a "false comparison" is detected. In order to achieve the synchronization, the reference frequency of the PLL is given by the incoming pulses; a misdetection would be erroneously interpreted as a PLL unlock state, resulting in a "wrong" charge injected in the filter. For this reason a logic network detects that both the pulses of F_{ref} and F_{div} has been accounted by the PFD (see figure 2.26) during the on window of the receiver. If it does not happen, the comparison is assumed as "wrong" and the charge injected by the pump dumped by D; the total charge in the filter (C_p and C_z) does not change and the VCO frequency remains constant. The resistor R_z is realized by means of switched capacitors. The switching frequency is derived from the frequency divider as the VCO frequency divided by 16 (640 kHz). The corresponding capacitance is therefore 482 fF.

2.6.5 Programmability of the loop filter

As stated in section 2.6, the pulse rate can be changed between 5 different values (20, 40, 80, 160 and 320 kpps). Since the received pulse is also used to lock the PLL, the division ratio of the PLL must be changed through the values 512, 256, 128, 64, 32. Apart from this, the bandwidth of the PLL can be increase to reduce the settling time and keep a constant F_{ref}/ω_c ratio.
In order to do not change the capacitance C_p and C_z, both R_z and $I_{CP,eff}$ must be changed. R_z must be adjusted to move the pole and the zero according to equations 2.5, while $I_{CP,eff}$ to keep the unity gain frequency between the zero

and the pole and ensure the proper phase margin.
Considering that the output frequency is constant, while the unity gain frequency is scaled as $F_{ref}/20$, it is

$$\omega_c = \frac{2\pi F_{ref}}{20} \simeq \frac{I_{CP,eff} R_z K_{VCO}}{N} = \frac{F_{ref} I_{CP,eff} R_z K_{VCO}}{F_{VCO}} \quad \Rightarrow$$

$$I_{CP,eff} \simeq \frac{F_{VCO}}{20 K_{VCO} R_z}$$

While R_z must be decreased for increasing pulse rate, the effective charge pump current must be increased of the same factor.
The reduction of R_z can be achieved increasing the switching frequency of the switch capacitor. However, the two non overlapping phase CK_A and CK_B for the switching capacitor are obtained with a finite state machine driven by the VCO and its output frequency cannot be easily increased. For this reason the capacitance C_{Rz} has been increased instead.
The tuning on the charge pump effective current is easily obtained by changing the ratio between C_1 and C_2, according to equation 2.6.

2.6.6 Operational amplifier design

It is easy to understand that both the finite voltage gain and the operational amplifier (OPAMP) offset will results in a phase difference between the two inputs of the PFD when the PLL is locked, hence in a phase difference between the divider output and the incoming pulse. Because the duty cycling of the receiver is based on the clock, hence the VCO output, any systematic misalignment between the divider output (hence the clock itself) and the incoming pulses must be avoided; it if happens, the amplifier on-window will be not aligned with the pulses causing the failure in both synchronization and reception.
To avoid that, an offset and finite gain compensation technique has been adopted for the OPAMP, as shown in figure 2.30 [15].
Usually the offset compensation is performed by closing the OPAMP in a unity gain feedback loop and storing the offset voltage on the capacitance C_{o1} in series with the "-" input. However, this poor and simple technique results in a residual input voltage given by the OPAMP initial differential voltage (the offset plus the finite differential input) divided by the loop gain. A more accurate offset cancellation can be done by means of the capacitor C_{o2} connected to the output. In this case, during the offset cancellation phase, the

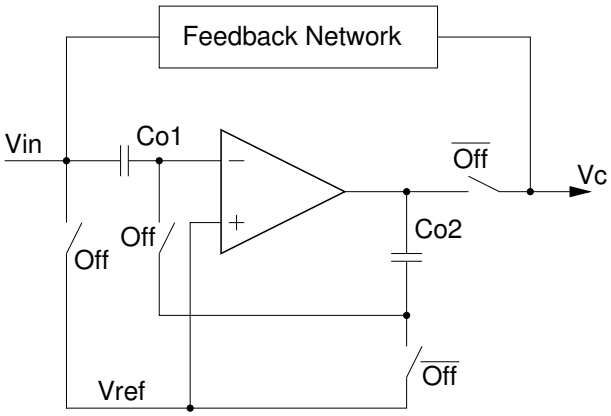

Figure 2.30: *OPAMP offset compensation*

OPAMP output voltage is kept at the same voltage, and the residual differential voltage is given by the original one divided by the square of the gain [15].

In this scheme, however, during the offset cancellation the OPAMP cannot drive the output voltage. During the offset cancellation the output voltage is kept by the feedback network (CRC network) between the input V_{in} (that is connected to V_{ref}) and V_c. To allow that, the OPAMP has been designed to be fast enough to integrate the charge pump charge in only 14 VCO periods (1.37 μs). After that period the charge of C_2 has been completely transfered to the feedback network (Off=0); then there are at least (32 - 14) VCO periods (in the worst case) while the filter output depends only on the charge sharing between C_p and C_z through C_{R_z} (Off=1). Note that since the OPAMP is connected to the output only for a fraction of the reference period, his noise contribution is scaled down, sensibly reducing the PLL output jitter.
These two phases are shown in figure 2.31; on the left the charge is injected in the filter, on the right the offset is canceled.
Thanks to this compensation technique, the gain of the OPAMP is not a critical issue. Upon that, the amplifier has been implemented using a 1 stage OTA for stability reason. The schematic is shown in figure 2.32. The differential pair is realized with PMOS both to reduce flicker noise and because of the output signal is in the range of 300 mV, value that is easily achievable with a PMOS implementation.

It must be noted that when the PLL is locked the charge injected by the charge pump into the loop filter is really small (ideally zero) and the OPAMP

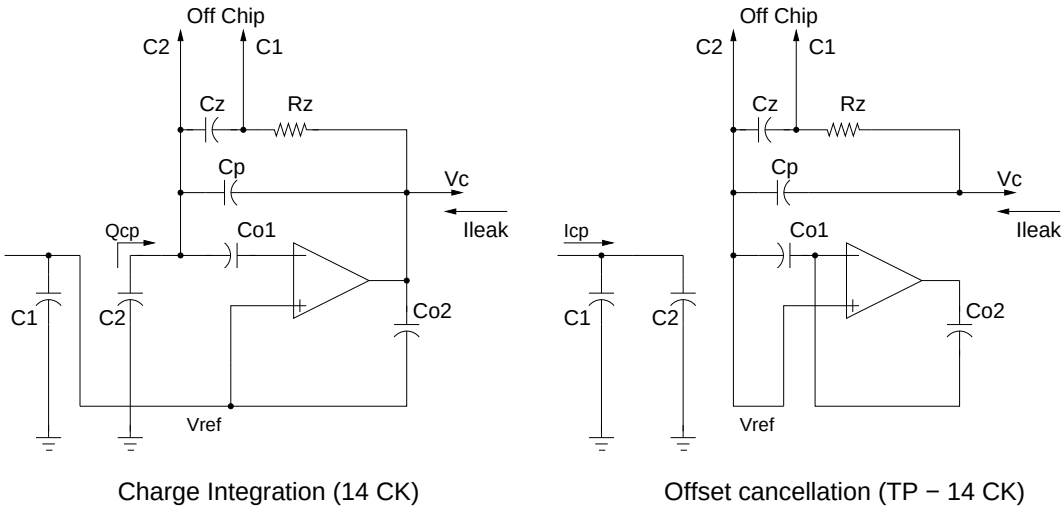

Figure 2.31: *Filter Phases*

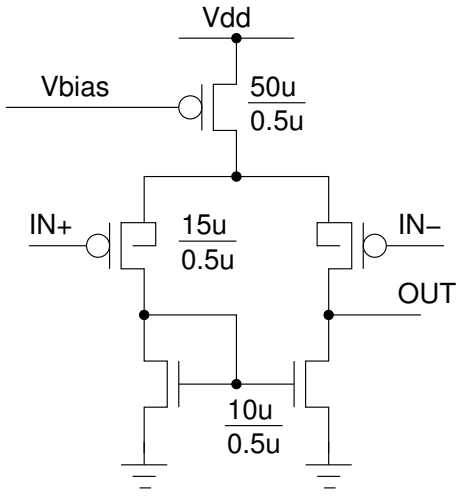

Figure 2.32: *OP AMP schematic*

output is limited by the poles but not by the slew rate. Moreover, thanks to the capacitor C_{o2}, the output voltage of the OPAMP is kept constant during offset cancellation. Slew rate can limit the acquisition time of the PLL, but this is assumed to happen once at the PLL startup, therefore it is not considered in the filter design.

The total load capacitance C_L seen by the OPAMP output is given by C_p (8.2 pF) in parallel with C_{Rz} (16×482 fF in the worst case) and the offset compensation capacitors C_{o2} (2 pF). If the swithced capacitor is synchronous

with the charge pump, as it is, the OPAMP has only $7T_{VCO} = 1683$ ns to settle the output (when C_{R_z} is connected to the output).
The waveform of the loop filter control signal for 160 kpps pulse rate are shown in figure 2.33.

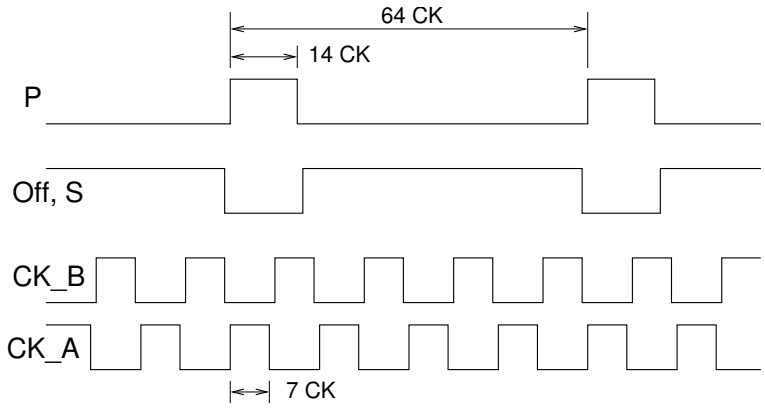

Figure 2.33: *PLL loop filter control signal for 160 kHz reference frequency*

Assuming the time constant τ of the circuit to be 1/5 of the required settling time, the transconductance of the differential pair must be

$$g_m \simeq \frac{C_L}{\tau} =\simeq 133\ \mu A$$

In sub-threshold operation with $g_m/I_d \simeq 20$, the bias current for the differential pair turns to be

$$I_0 = 2\frac{g_m}{20} = 13.2\mu A$$

Periodic AC analysis have been performed, showing that in the worst condition, a minimum current of 20 μA is required to guarantee the correct operation of the filer. All the switches are realized with complementary MOS $1\mu m/0.1\mu m$ and all the non overlapping phases have been generated by means of finite state machine driven by the clock frequency. No optimization of the switch leakage current has been done since at every time, each high impedance node is connected to a low impedance one.
Figure 2.34 shows the comparison of magnitude and phase of the loop filter transfer function with the ideal one. It can be seen that, as one can expect, the finite gain of the amplifier introduces a pole at low frequency. Moreover the switching cap behavior of the filter slightly reduces the phase margin of the system, that however is still enough to maintain a stable PLL operation.

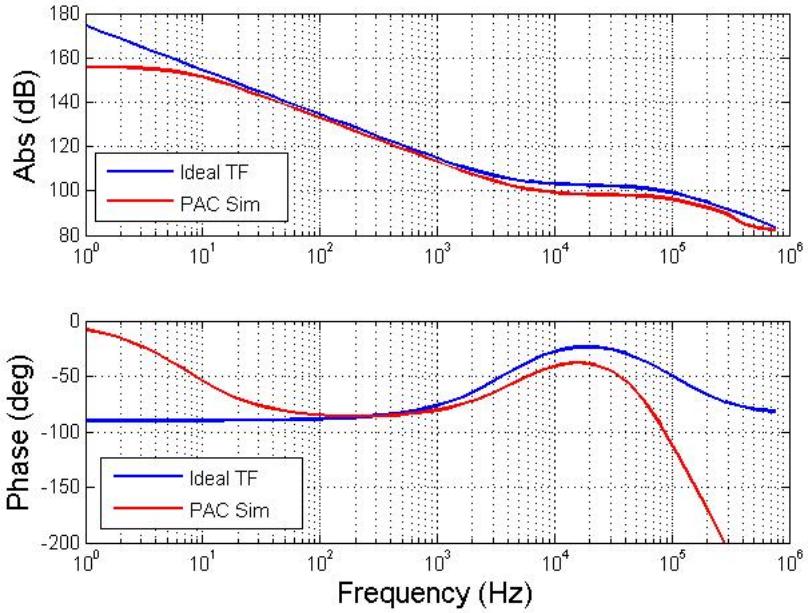

Figure 2.34: *PLL filter simulation*

It is known that the closed loop transfer function of a PLL presents an overshoot due to the presence of a zero-pole couple, where the zero is given by the zero in the loop filter transfer function. To reduce the amplitude of this overshoot, it is necessary to move the zero at a lower frequency, hence increasing the capacitance C_z. For this reason an external capacitance can be added in parallel to C_z in order to reduce the peaking into the PLL transfer function, that, as described in [7], can result in a lock missing of the node.
The reference voltage has been generated on-chip my means of a voltage divider. Because the output impedance of the reference generator is a critical issue, two different impedance of 15 $k\Omega$ and 3 $k\Omega$ (for 6.5 and 30 μA respectively) can be digitally selected.

2.7 Synchronization procedure and related hardware

As previously stated one of the goals of this design is to avid the requirement of a crystal oscillator on each node and to keep the local time base by means of a PLL. The VCO output represents the only time information available on

the node. Each signal in the node is synchronous with the PLL output and the frequency divider state represents the state of the system. In order to determine when the transmitter or the receiver must be activated, the state of the PLL is compared with 9 registers that store the state value corresponding to the transmission and the reception of the data "time slot" (figure 2.35).
The state 0 corresponds by default to the clock reception; when the PLL is

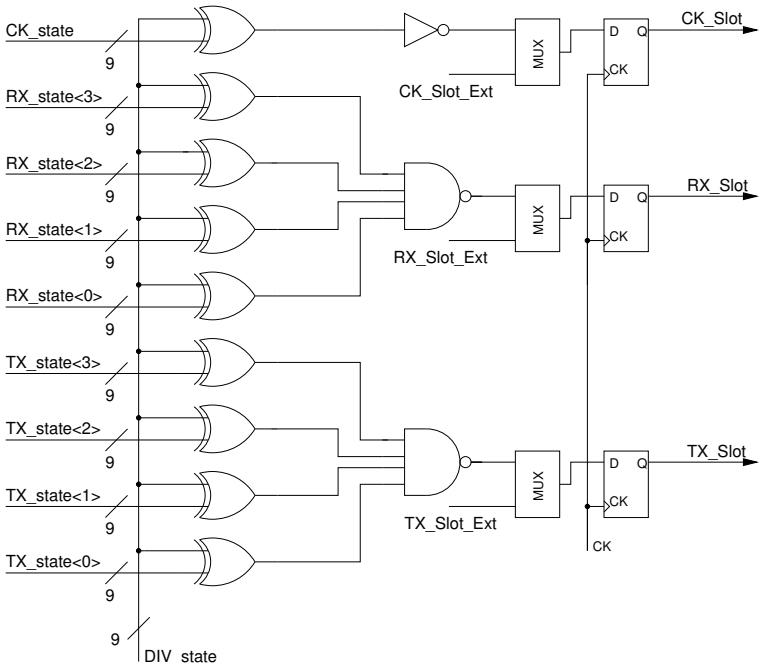

Figure 2.35: *RX_Slot, CK_Slot and TX_Slot generation*

locked and its state is zero the "clock" pulse is expected on the reference input of the PFD, that means that a pulse is respected at the antenna.
Because of the time needed to turn on the amplifier and cancel its offset (figure 2.16), actually the signal CK_Slot must be activated [(2+WinLength+1)/2 clock period in advance with respect to the state 0. If, for example, the frequency divider is dividing by 512 and the window length is chosen 1 clock period, the CK_Slot signal must be activated when the state is 512-3 = 509, that is the number that must be stored in the register CK_state.

For maximum hardware flexibility, it is considered that the bit rate can be increased either increasing the pulse rate or interleaving more pulses into the same reference pulse period, for example to or from different neighbors nodes. This means that more pulses can be received in the same nominal pulse pe-

riod, but only one of them (the one that occurs during the "0" state of the PLL) acts as clock; the others carry only data but not the timing information. In this way the singe node can acquire the clock information from one node and the data from another one, and in the same way can transmit the timing information to a node and data to another one. To allow for that, 4 receiving windows and 4 transmission windows can be "opened" in the same nominal pulse period (hence between one clock pulse and the following one) by means of the comparison of the PLL state with RX_state$< 3:0 >$ and TX_state$< 3:0 >$. As for the clock pulse, due to the time needed to set up the receiver, the registers RX_state$< 3:0 >$ must be loaded with a value that correspond to the desired state minus 3. For the transmitter ones, it must be the desired state minus 2.

For test purposes, the signals CK_Slot, RX_Slot and TX_Slot can be also forced through 3 pins in the chip. To avoid critical races, this signals are synchronized with the internal CK.

The synchronization scheme, that is fully described in [7] works as follows. At the beginning it is assumed that one selected node has on board a crystal oscillator that provides a very stable and precise clock. This node starts to transmit at a fixed and pre-determined pulse rate.
At the same time, all the other nodes are configured to be always on as receiver, and therefore the neighbors start to detect the pulses and their own PLL rapidly converge to the lock condition, that is when the "0" state is aligned with the clock pulse. At this point this node are synchronized and can be duty cycled. Moreover, these nodes are able to transmit in a TDMA fashion, becoming themselves clock source for the other nodes.
In this way the clock is spread around the network starting from a selected "master clock" node. The time required for the full network synchronization depends on the number of step necessary to propagate the clock to the farest node and the PLL settling time.

However this technique cannot be use for network arbitrarily large, as described in [7]. Since the PLL increases the jitter in the synchronization signal, only a limited number of nodes can be synchronized starting from the same "master clock" node because of the accumulated jitter. It is therefore necessary to implement a hierarchical synchronization scheme, as shown in figure 2.36. A few nodes receive an accurate synchronization signal form a precise clock an provide the distribution to the adjacent nodes. In this way the dis-

tance (measured in terms of hops) between each node of the network and the accurate clock can be reduced even with very wide networks. Of course a different way to provide the high level synchronization must be found.

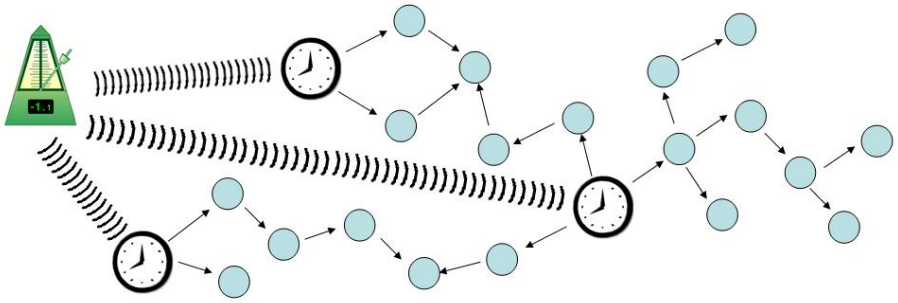

Figure 2.36: *Synchronization hierarchy*

2.7.1 Synchronization simulation

A transmitter, a receiver and the PLL, together with the coupled inductor model, have been simulated for a long time to verify the synchronization scheme between two nodes.
The maximum pulse rate of 320 kpps has been used to save simulation time. All the analog part is described at transistor level, while for the digital circuits a Verilog description have been preferred.
Figure 2.37 shows the received bit, the transmitted bit and synchronization signal generated on the receiver while figure 2.38 the PLL control voltage.
For the first 200 μs the receiver is kept on all the time (not duty cycled) and the PLL adjusts the VCO control voltage to reach the lock condition. After 200 μs the duty cycled operation mode is activated and the amplifier is turned on only when the next pulse is expected. As it can be seen, the system behaves in the same way (the output continues to track the input and the PLL control voltage is constant).

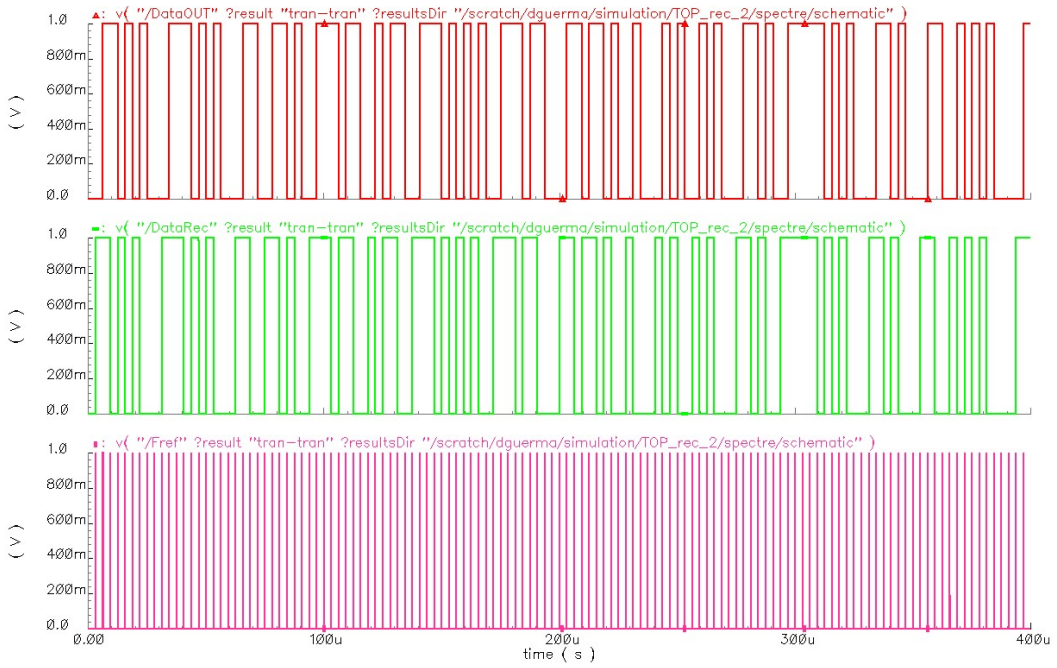

Figure 2.37: *Received bits, transmitted bits, synchronization signal generated by the receiver*

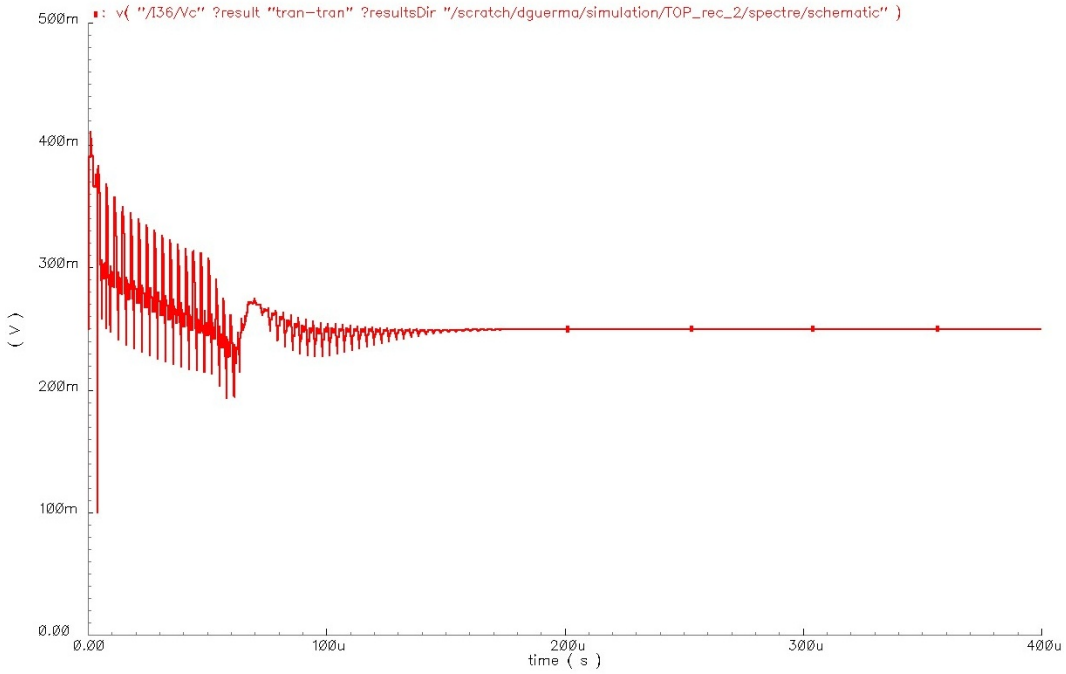

Figure 2.38: *PLL control voltage*

Chapter 3

Test Chip Pin Out

The transceiver has been implemented in a 90 nm 7M-1P CMOS technology provided by STMicrolectronics.
Figure 3.1 shows the layout of the realized chip, that includes a transmitter, a receiver and the synchronization PLL. The die size is 950 μm by 1200 μm; the chip has 32 pads and the area is mainly dominated by the PLL and transmitter capacitors. Underneath the PLL MIM capacitor, MOS capacitor has been used as supply filter on the analog supply.
The receiver has been placed in the center of the die, so to minimize the input connection length. The transmitter is underneath the LNA coupling capacitors to save area.
The big capacitor indicated as TXcap (600 pF) provides the peak current needed by the transmitter; to get the maximum capacitance density it is realized with overlapped MIM cap and MOS cap. Thick oxide transistors have been used to reduce the gate leakage current.
The pad names and functions are indicated in table 3.1. A "X" in the "Enable" column means that the input/output can be enabled or disabled.
Figure 3.2 shows the chip padring, together with the pad labels.

Name	Function	I/O	Enable
CK_SPI	CK SPI	I	
CS_SPI	CS SPI	I	
SI_SPI	DataIN SPI	I	
TX_SlotExt	Force a TX cycle	I	X
RX_SlotExt	Force an RX cycle	I	X
CK_SlotExt	Force a RX CK cycle	I	X
CKExt	External 10.24 MHz CK	I	X
CKOUT	10.24 MHZ CK output	O	X
gnddig	Digital ground	I/O	
gnddig	Digital ground	I/O	
DataOUT	Output Data (received Data)	O	
BitSync	Output Data Sync	O	
vdddig	Digital Vdd (1 V)	I/O	
C2	External Loop Filter Cap (opt)	I/O	X
C1	External Loop Filter Cap (opt)	I/O	X
vdddig	Digital Vdd (1 V)	I/O	
gndpad	Pad ring gnd	I/O	
OOUT	(Squared) Amplifier output	O	X
DataIN	Input Data (Transmitter)	I	X
vddana	Analog Vdd (1 V)	I/O	
vddana	Analog Vdd (1 V)	I/O	
FrefOUT	PLL Reference Frequency Output	O	X
FrefEXT	External PLL Reference Frequency	I	X
vddpad	PadRing Vdd (1 V)	I/O	
FdivOUT	PLL Divider Frequency Output	O	X
gndanalog	Analog gnd (Chip Substrate)	I/O	
DigProbe	Programmable Digital Output	O	X
L2	Inductor Terminal	I/O	
L1	Inductor Terminal	I/O	
TXForce	Force a Transmission Pulse	I	X
gndanalog	Analog gnd (Chip Substrate)	I/O	
vddSPI	SPI Vdd (1 V)	I/O	

Table 3.1: SRW pin out

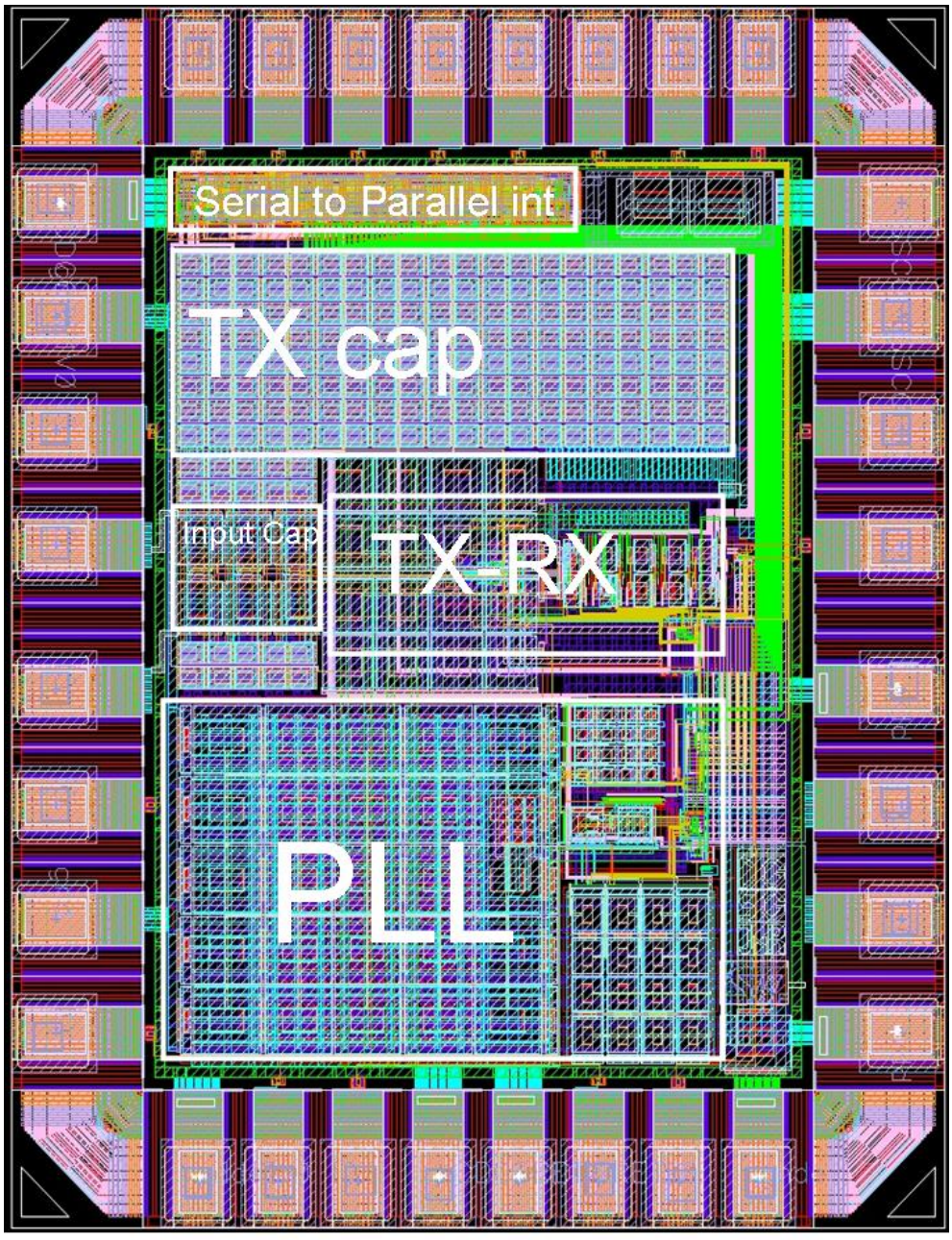

Figure 3.1: *Top Layout*

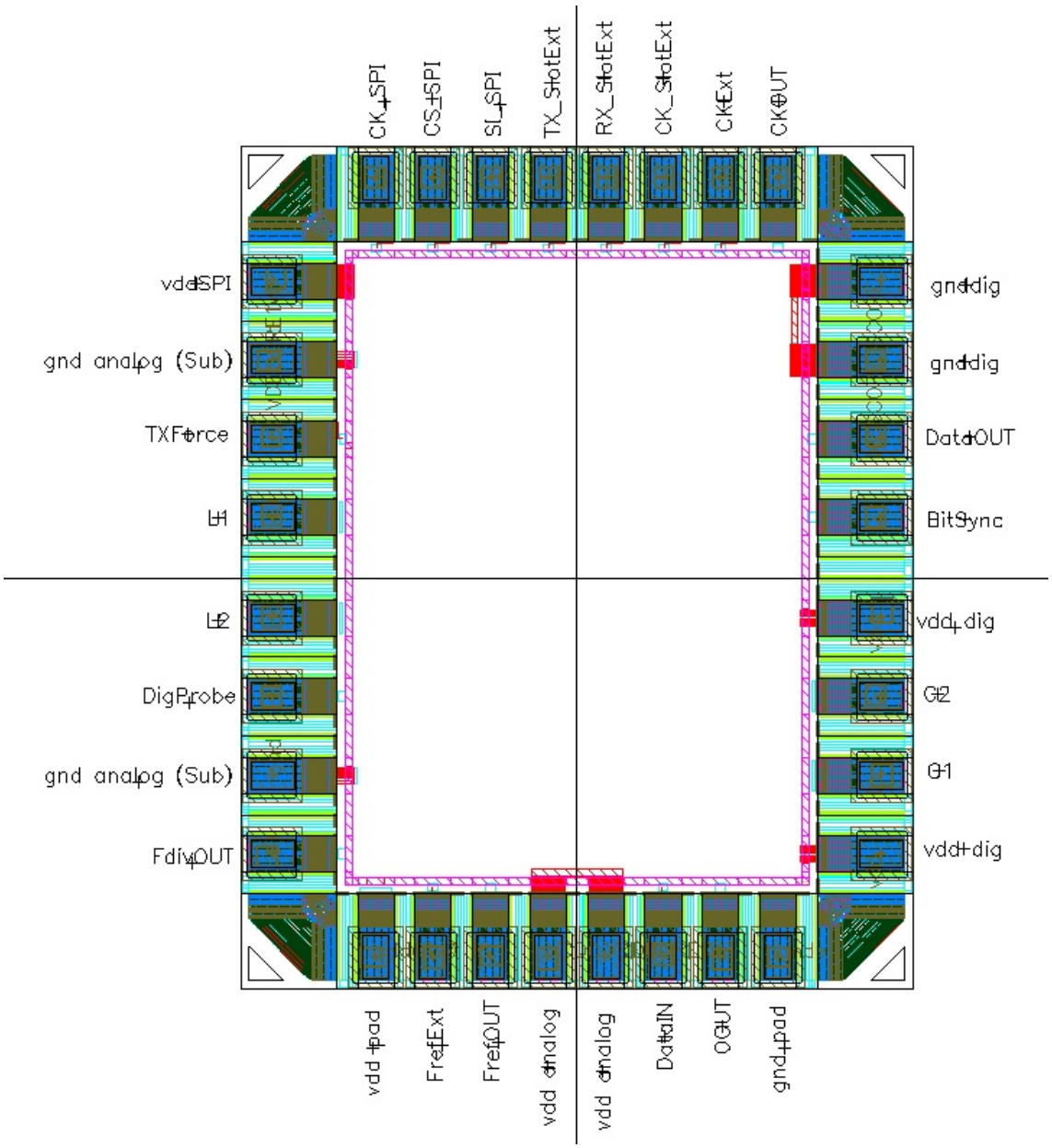

Figure 3.2: *Pad Ring*

Bit< 255 >	Reset_Neg	Reset (=0) of the digital circuits
Bit< 4 >	FilterReset	Reset (=1) of the PLL filter
Bit< 172 >	StartUP	Keep the receiver always on and the PLL in continuous tracking

Table 3.2: General functionality bits

Bit< 174 >	TX_FroceEN	Enable TXForce input
Bit< 55 >	SlotExt_EN	Enable CK_SlotExt, RX_SlotExt and TX_SlotExt inputs
Bit< 13 >	CextEN	Enable the external Loop Filter Cap
Bit< 12 >	CextEN_Neg	
Bit< 209 >	FrefEXTEN	Enable the external reference frequency for the PLL
Bit< 50 >	CKEN	Enable the CKOUT output
Bit< 16 >	FdivEN	Enable the FdivOUT output
Bit< 48 >	CKselect	if 0 the external CK is used if 1 the internal CK (PLL out) is used

Table 3.3: Input Output Enable

3.1 Control Bits

As described in the previous chapter, the chip need tens of configuration bits. These bits are programmed by means of an SPI (Serial to parallel Interface) designed by Simone Gambini ad Nathan Pletcher. Bits are reported in the next tables 3.2, 3.3, 3.4, 3.5, 3.6 and 3.7, divided by functions.
The bits are setted and reseted using a *Python* software and transfered to the chip through an USB/SPI interface [20].
The DigProbe output is the output of a multiplexer (inside the chip) that allows to select 1 out of 8 internal signals and carry it out.

Bit< 56 : 58 >	DigProbe	DigProbe out selection 000 ⇒ EN (Amplifier Enable) 001 ⇒ OffsetNull_Neg (Amplifier) 010 ⇒ RX_CK 011 ⇒ EN_LNA (LNA Enable) 100 ⇒ TX 101 ⇒ RX 110 ⇒ TX_EN 111 ⇒ SPI output

Table 3.4: DigProbge Output Selection

Bit< 34 : 32 >	BCP	Charge Pump Bias 000 = Max current 111 = Zero current
Bit< 37 : 35 >	BopAmp	Op Amp Bias 000 = Max current 111 = Zero current
Bit< 11 : 8 >	SpeedUP	Bit rate selection 0000 = 20 kpps (PLL x 512) 0001 = 40 kpps (PLL x 256) 0011 = 80 kpps (PLL x 128) 0111 = 160 kpps (PLL x 64) 1111 = 320 kpps (PLL x 32)
Bit< 7 : 6 >	VrefBoostEN VrefBoost_Neg	Enable the low impedance PLL filter voltage reference
Bit< 13 : 12 >	CapExt CapExt_Neg	External PLL loop filter capacitance enable
Bit< 17 >	PFDenForce	if = 1 the PLL is sensible to all the edges on the PFD even with StartUP=0

Table 3.5: PLL controls

Bit< 1 : 3 >	Cap	Input capacitance tune 111 = Max Cap 000 = Min Cap
Bit< 183 : 180 >	BLNA	LNA Bias 0000 = Max Current 1111 = Zero Current
Bit< 187 : 184 >	Bampli	Ampli Bias 0000 = Max Current 1111 = Zero Current
Bit< 191 : 188 >	Load	Ampli Load 0000 = 600 Ω 0001 = 1200 Ω 0011 = 2400 Ω 0111 = 4800 Ω 1111 = 10.4 kΩ
Bit< 195 : 192 >	Bfinal	Final Stage Bias 0000 = Max Current 1111 = Min Current
Bit< 199 : 196 >	Bcomp	Comparators Bias 0000 = Min Treshold 1110 = Min Treshold
Bit< 61 : 59 >	Base	ON phase duration 011 = 1 CK 110 = 3 CK 101 = 5 CK
Bit< 179 : 176 >	B_DelTX	TX pulse duration 0001 = Max duration 1111 = Min duration
Bit< 210 >	Fast	Bypass the delay in the CK/Data Recovey circuit

Table 3.6: Transceiver controls

Bit< 160 : 152 >	CKslot
Bit< 151 : 143 >	RXslot0
Bit< 142 : 134 >	RXslot1
Bit< 133 : 125 >	RXslot2
Bit< 124 : 116 >	RXslot3
Bit< 115 : 107 >	TXslot0
Bit< 106 : 98 >	TXslot1
Bit< 98 : 89 >	TXslot2
Bit< 88 : 80 >	TXslot3
Bit< 169 : 161 >	Add
Bit< 49 >	Move CK Slot (+ Add in div state)

Table 3.7: Slots (MAC) controls

Chapter 4

Measurement results

The chip has been mounted on a small board for test purposes. Chip on board technique has been preferred to a package in order to minimize sizes and parasitic inductance of access lines (figure 4.1). The board is 1 by 1 inch and includes the bonding pads for the die, the 8.1 mm inductor and four connectors. It is realized with 4 copper layers and FR4 dielectric material. The board layout is shown in figure 4.2; the left side shows the top two layers, while the right side the lowest two. The inductor is realized in the lowest layers so to keep it as far as possible from the chip and the lines on the top, thus minimizing the parasitic capacitance.
This board is then plugged into another one which provides supplies, inputs and collects the outputs.

4.1 General results and main issues

The testing of the chip required a long time and was extremely complicated; the problems encountered during the chip measurements can be divided in two main categories

- Inductive channel attenuation and interference.
- PLL phase error.

These two issues make the circuit not working as expected, and while the second could be solved in a further implementation, the first one seems to strongly limit the possibility of an inductive based link.
In the following sections every part of the transceiver will be analyzed and the measurements will be described in details.

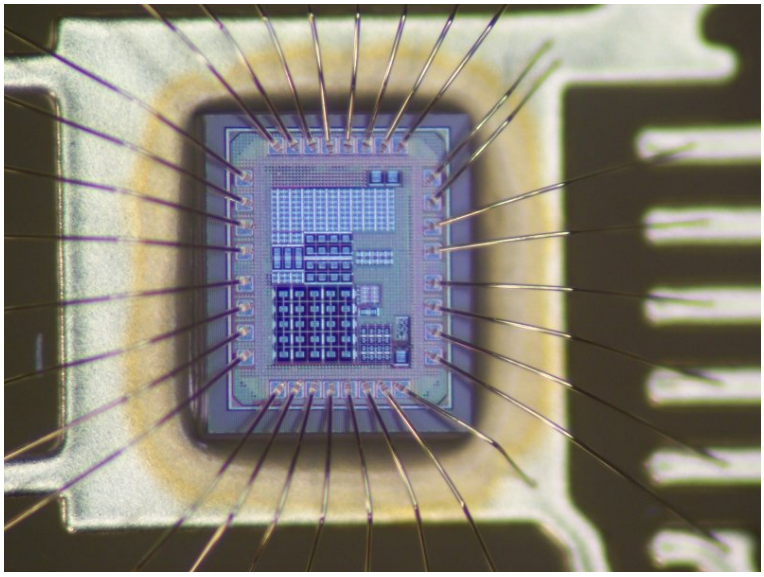

Figure 4.1: *Chip-On-Board assembly*

SpeedUP	PLL Div factor	New PR with 8 MHz VCO	PR with 10.24 MHz VCO
1	512	20 k	–
2	256	40 k	31.25 k
4	128	80 k	62.5 k
8	64	160 k	125 k
16	32	320 k	250 k

Table 4.1: Pulse rates as a function of SpeedUP and the VCO frequency

4.1.1 New pulse rates

As will be explained later, most of the measurements have been taken with the VCO running at 8 MHz instead of 10.24. This VCO frequency, together with the available division ratio in the PLL, leads to new pulse rates for the system, summarized in table 4.1.1.

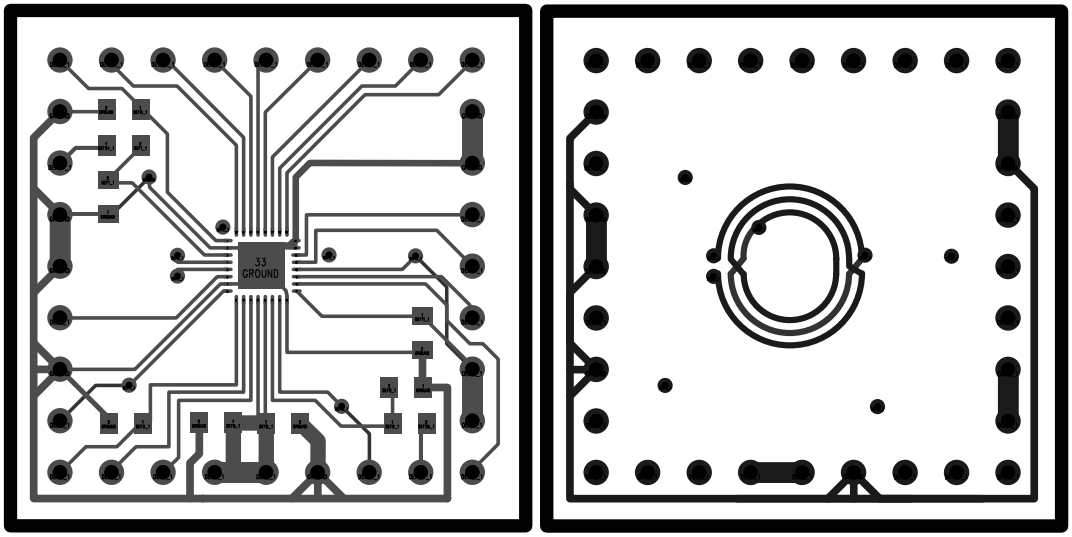

Figure 4.2: *Top (left) and bottom (right) layers of the board*

4.2 Inductor measurements

A photograph of the 8.1 mm diameter, 3 turns on-board inductor is shown in figure 4.3. The die is mounted on the other side of the board in correspondence of the inductor center.
The inductor has been measured by means of an SMA connector mounted on the board side. The connector and the lines from the connectors to the inductor cannot be characterized separately and have been treated like pure delay lines, measuring the physical length and considering a proper dielectric constant for the surrounding materials.
According to this approximation, values of the inductor L and the self resonant frequency can be found. Figure 4.4 shows the measured reflection coefficient (after the de-embedding of the access lines) and the best fit curve assuming a pure parallel LC model for the inductor. This approximation is reasonable being the expected quality factor of the inductor relatively high. The fitting results in a inductance value of 74 nH and a self resonant frequency of 528 MHz (Table 4.2).

The self resonant frequency is lower that the one previously measured for an analog inductor. This is due to the chip access lines on the bottom layer of the board, that increase the parasitic capacitance, and that were not present in the previous prototype. Also minor variation in the inductor vias has been

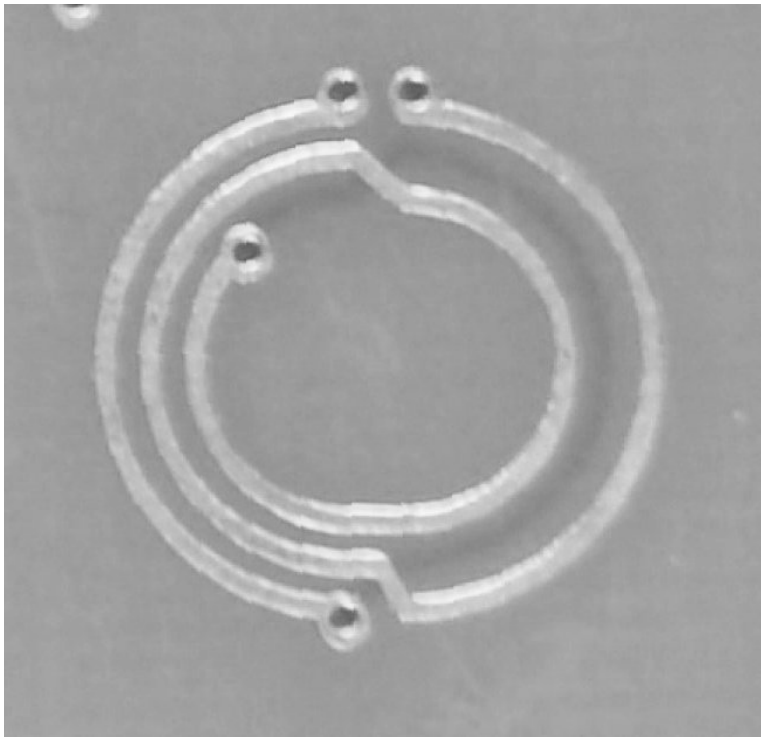

Figure 4.3: *On board inductor*

	Meas	Sim
L	74 nH	76 nH
SRF	528 MHz	¿ 800 MHz

Table 4.2: Inductor value and self resonant frequency (measurements and ADS simulations)

adopted to accommodate the bonding pads. Anyway a self resonant frequency of 528 MHz is still high enough to include almost all the first lobe of the signal spectrum.

4.3 Stand-by currents

For a low power system, a very important parameter is the stand-by current, that is given by the current consumed by the system when any functionality is turned off. When the transceiver is connect to a 1.0 V power supply, with all

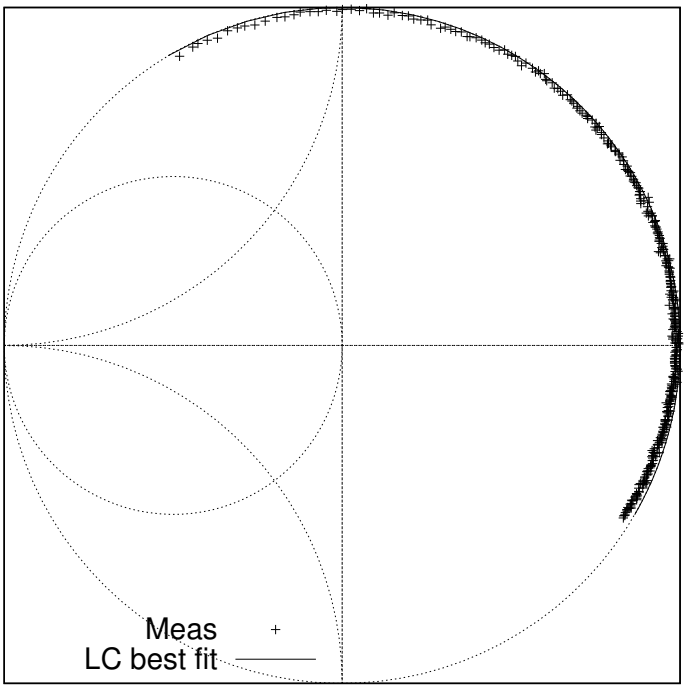

Figure 4.4: *Measured and modeled inductor refection coefficient*

Analog Supply	12.5 μW	12.5 μA
Digital Supply	15.5 μW	15.5 μA
SPI Supply	17 μW	17 μA
Pad ring Supply	5.6 μW	5.6 μA

Table 4.3: Stand by power (and currents) at 1 V supply

the circuitry off, the measured stand-by power and current are summarized in table 4.3.

An analog supply stand-by current of 9 μA was simulated for the voltage references of the charge pump and the PLL loop filter, while the remaining 3.5 μA are due to bias circuits (mainly the charge pump) and leakage in the analog part. The digital stand-by current is in good agreement with simulation (14 μA of leakage current in TT corner); moreover the digital supply also supplies the transmitter, that has a simulated leakage around 500 nA, and the last stage of the receiver. SPI and pad ring stand-by currents have not been

considered in the design.

4.4 Transmitter characterization

In order to test the transmitter performance, it has been forced to generate pulses my means of the pin TXforce.
The pulses are measured across the inductor using two probes of a digital oscilloscope. Figure 4.5 shows a good agreement between the measured pulse and the simulations, the latter taking into account for the probes capacitance (12 pF) and the scope bandwidth (500 MHz). By means of an inductor equal

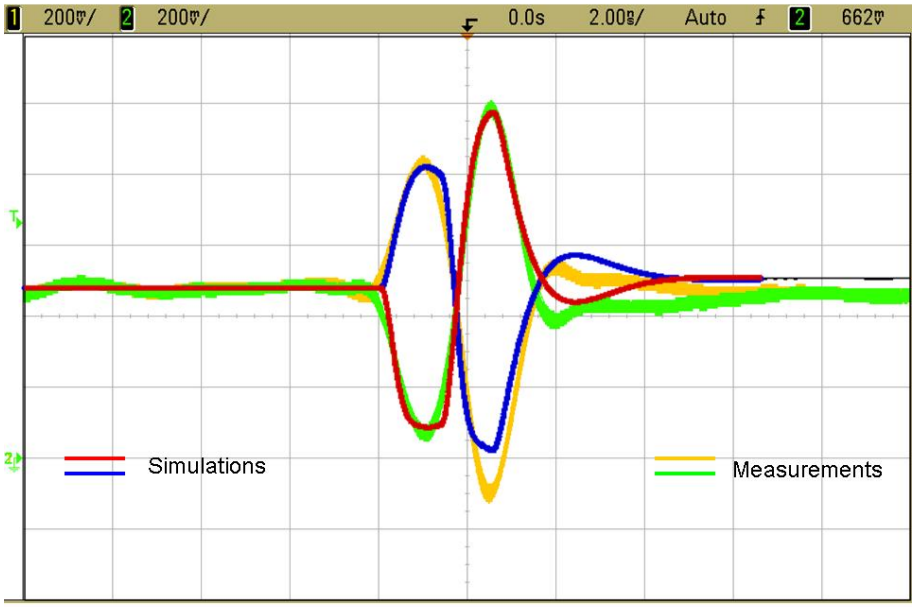

Figure 4.5: *Measured and simulated pulse*

to the transceiver antenna, the pulses can also be collected and shown on an oscilloscope (figure 4.6) or a spectrum analyzer (figure 4.7). Clearly the larges amount of energy is in the first lobe of the spectrum, between 0 and 2 over the pulse duration (about 666 MHz).

The scope used in the measurement of figure 4.6 has an input capacitance (14 pF) and resistance (50 Ω) that are different than the ones of the receiver; furthermore the scope bandwidth is only 500 MHz. The high value of the

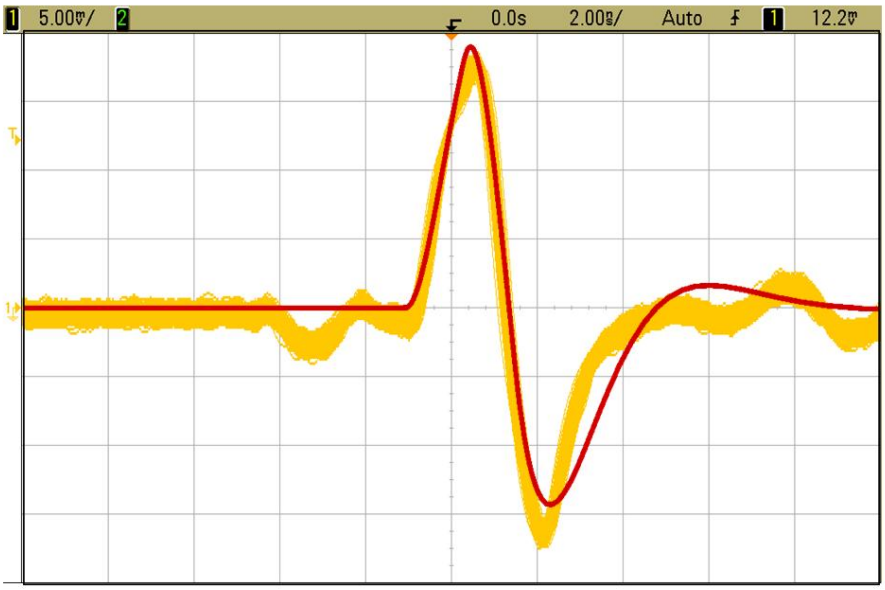

Figure 4.6: *Measured and simulated pulse (k=0.05, C=14 pF, R = 50 Ω)*

capacitance and the limited bandwidth result in a longer pulse, as predicted by simulation with a coupling factor of 0.05.

Transmitter power efficiency and energy per pulse have been characterized as well. Figure 4.8 shows the transmitter power as a function of the pulse rate, when the transmitter delay line used to generate two 1.5 ns pulses is always active. The total measured power is given by the stand-by current of the system (28 μA) plus the delay line bias (52.8 μA) plus the contribution of the pulses. While the first two contribution are constant, the third is proportional to the pulse rate. The best fit curve shows an energy per pulse of 10.86 pJ/pulse for the latter contribution.
When the transmitter is duty cycled, the delay line is activated for two clock periods, and the transmitter power for both 8 and 10.24 MHz clock frequencies is shown in figure 4.9. The energy per bit, apart from the stand-by current of 28 μA, is 21 pJ/pulse with a 10.24 MHz clock and 24 pJ/pulse with a 8 MHz clock, as summarized in table 4.4.

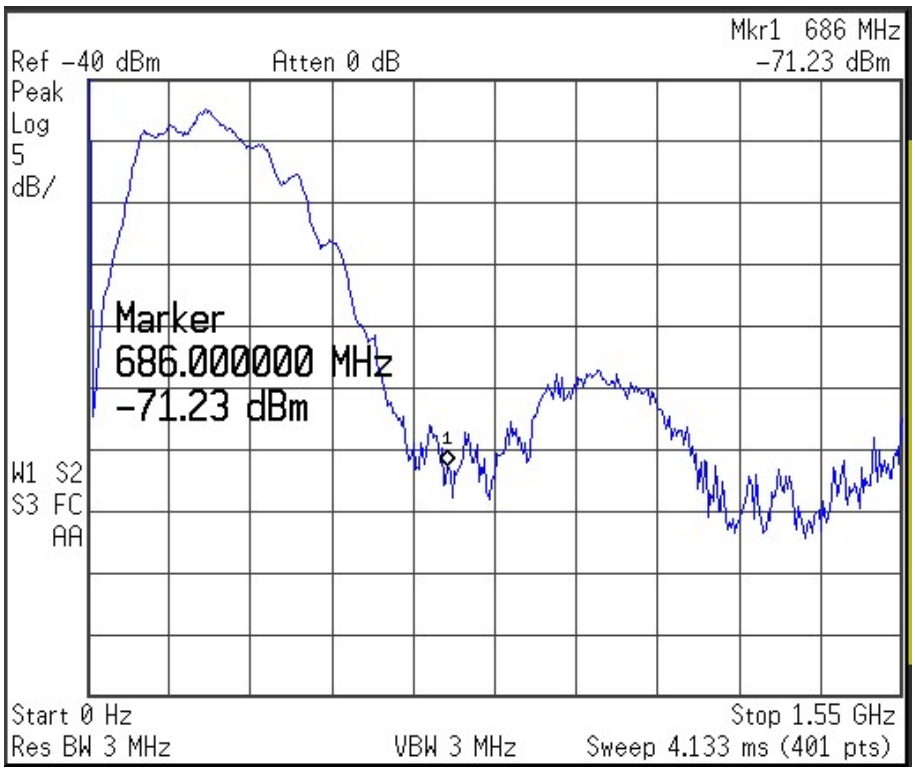

Figure 4.7: *Measured Spectrum at 1 mm distance*

Delay Line Bias	52.8 μW
Epulse (w/o bias)	10.24 pJ/pulse
Epulse 10.24 MHz CK	21 pJ/pulse
Epulse 8 MHz CK	24 pJ/pulse

Table 4.4: TX power consumption and energy per pulse at 1 V supply

4.5 Inductive channel characterization

As previously anticipated, the inductive channel does not behave as expected. First of all, and this is still unexplained, no sensible coupling has been detected with the inductors laid out on the same plane, even at then minimum distance allowed by the boards (2.54 cm). This is probably due to the large amount of wires in the boards needed to connect the 32 chip pins; those can couple with the transmitter antenna and shield the receiver one.
Anyway, stacking the inductors on on top of the other with no wires in be-

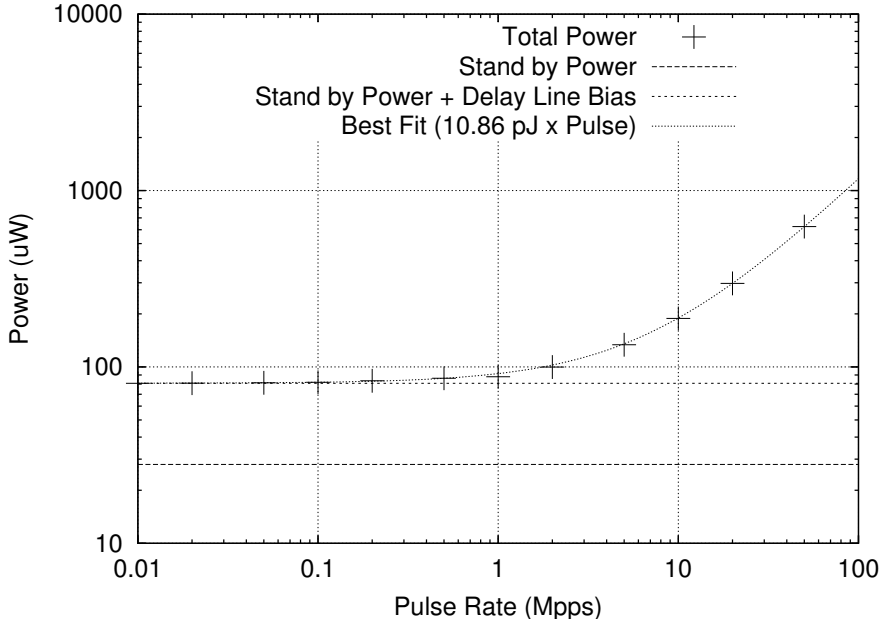

Figure 4.8: *Measured power of the transmitter, not duty cycled*

tween, a coupling factor not so far from the expected one is found. Figure 4.10 shows the analytical coupling factor together with the one extracted from the measurements. The analytical model considers the inductor as an infinitesimally small magnetic dipole, and for that reason it is not valid at really short distances; if computed with this simplify model it would result infinity, that of course is non sense. The measured coupling factor has been extracted starting from peak-to-peak detected voltage and taking into account both the impedance and bandwidth of the scope and the real transmitted pulse shape.

The second problem, definitely underestimate during the system design, is the coupling between the receiver inductor and any source of magnetic field apart from the transmitter. While, on one hand, the inductor is a really bad antenna for an electromagnetic plane wave, on the other hand it is really sensible to a variable magnetic field generated by any current that flows close to it.
Of course in a "real application" it is not expected to have such a current; all the functionality of the system are within the chip and no lines surround the inductor apart from the supply. Unfortunately this does not apply for the testing set up of the transceiver, because digital lines feed the transmitter and

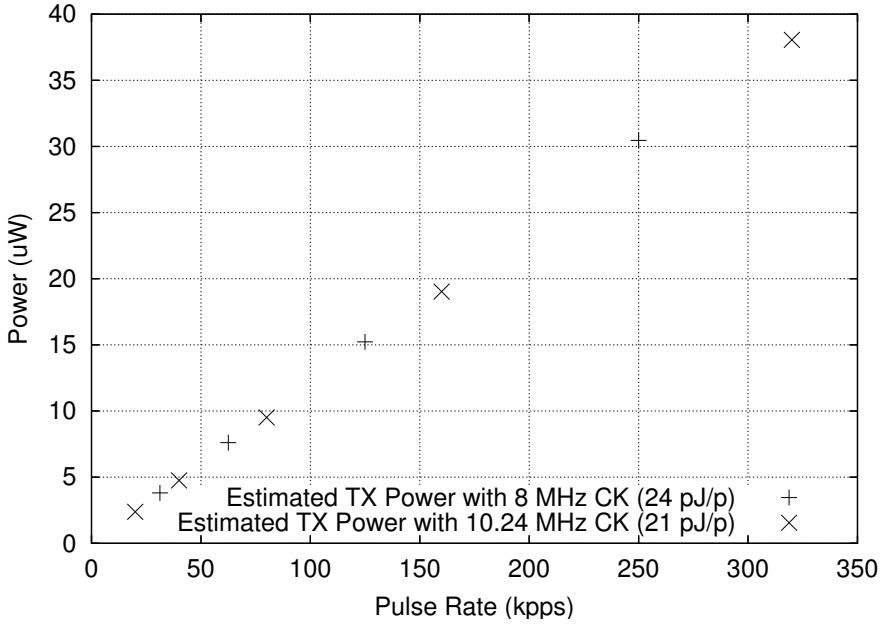

Figure 4.9: *Estimated power of the transmitter in duty cycled operation mode*

collect data from the receiver. These lines go extremely close to the receiver antenna (just on the other side of the board for the receiver lines, and at the same distance of the transmitter for the transmitter ones) and any signal transition on them generates a variable magnetic field that is detected and amplified by the receiver.

This behavior is exacerbate by monitoring of the signals by means of a scope, that increases the currents and hence the magnetic fields generated by those lines. Moreover, the 14 pF probe load also gives high switching currents that result in high supply noise (a greater number of supply and ground pad would be required to reduce the impact of digital switching).

The lack of coupling for the inductor on the same plane, together with the high sensitivity of the receiver to interference, limit the viable communication range to a very short distance (lower than 1 cm) and with the inductor stacked one over the other. So doing the signal induced by the transmitter in the receiver inductor is strong enough to overwhelm the interferences, and the communication can be established.

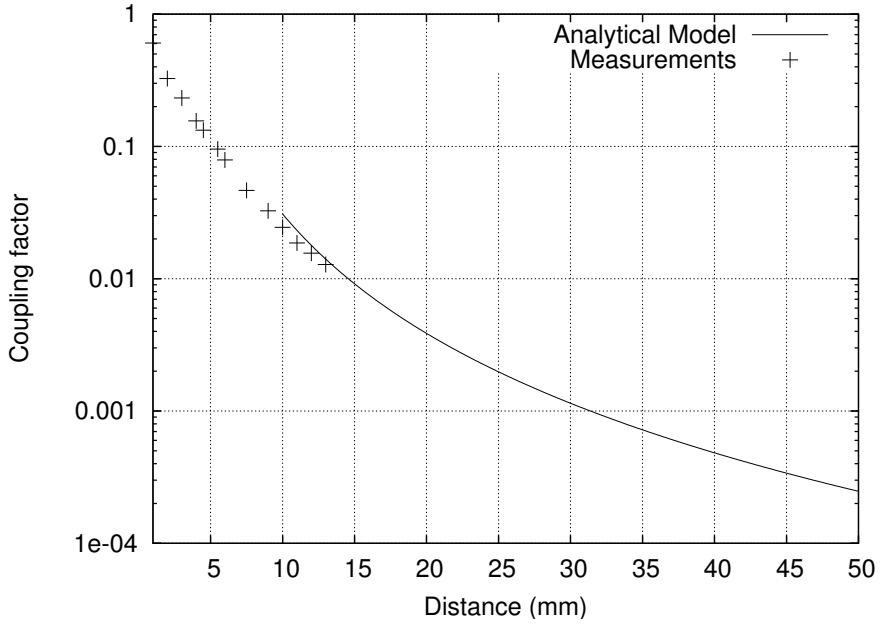

Figure 4.10: *Analytical and (indirectly) measured coupling factor for the stacked inductors*

The communication over 5 cm cannot be verified. Up to now it is still unclear if, even with autonomous nodes without any access line and boards including only the inductor, a inductive coupling base communication can be established in the range of 5 cm.

4.6 Receiver and data link characterization

With respect to many other receivers, that can be tested by plugging a signal source at the LNA input, it is not possible to test a stand-alone receiver because no instrumentation is available to produce the pulse with the required shape, duration and repetition period.
This force to use a transmitter as signal source and to establish a link between the transmitter and the receiver. Because of the previously discussed limitation of the channel, transmitter and receiver must be stacked one over the other at a very short distance.
Unfortunately this is a sub-optimal operating condition for the receiver, that has been designed for a very high gain. A small gain can be achieved by means of a bias current reduction, but this leads to a strong bandwidth reduction that produces pulse spreading and ringing, giving false commutations of the comparators. To avoid this, minimum load resistors must be selected and paradoxically a high current is still necessary even for a moderate or even low gain.
Measurements in this conditions are shown in figure 4.11 for a 9 mm distance; the transmitted (and received) sequence is 0011.

4.6.1 Loopback measurement

Another way adopted to test the receiver is to drive independently both the transmitter and the receiver on the same chip, so to avoid any kind of interference from the inductors, the boards, or any external source. To introduce the maximum (possible) attenuation, the inductor terminals have been shorted on the boar and the received voltage is given by the drop on the bond wires and lead frames inductance and resistance. Despite this setup seems to give a huge attenuation, considering 1 nH for each bond wire and 50 Ω output impedance for the transmitter, the attenuation at 300 MHz is only 22.5 dB. However, this also results in a different pulse shaping, and the lowes inductance value push the energy of the pulses at higher frequencies.
In these conditions both transmission and synchronization has been achieved, with a clock frequency of 8 MHz, as will be discussed in the next section. The maximum measured pulse rate is 50 Moos, and it is limited by the I/O rather than the transceiver.
Figure 4.12 shows the total power contribution for different window size in the duty cycle operation mode. This power includes both the transmitter and the

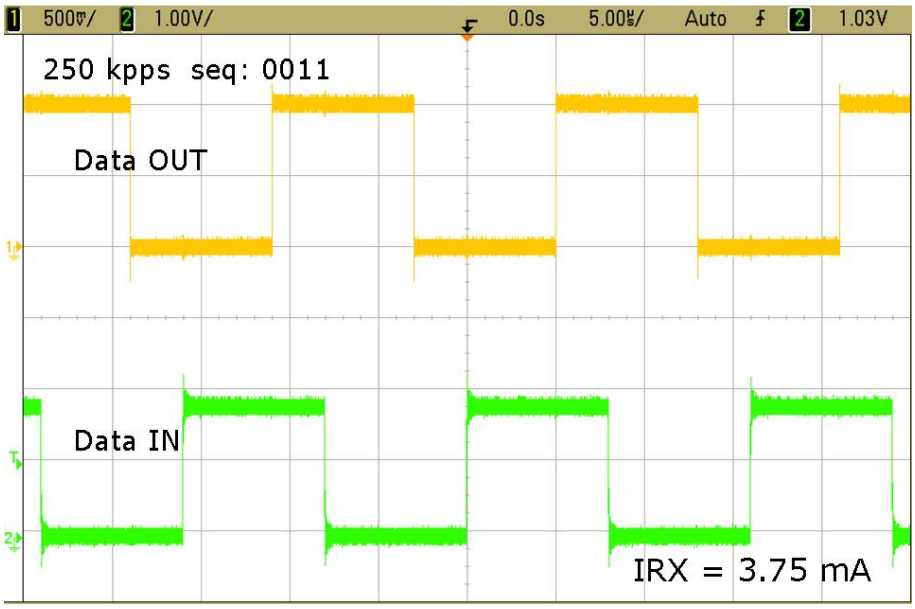

Figure 4.11: *Transmitted and received sequence for 9 mm distance*

receiver contributions. The crosses represent the measured values while the lines the respected power computed considering the biases and the duty cycle factor. Some comments are necessary to figure 4.12.

- Total power curves are plotted for decreasing pulse rates (see table 4.1.1 for 8 MHz clock) from the top to the bottom. The lowest one is for 31.25 kpps and in that condition only the synchronization is achieved while the bit error rate becomes intolerably high (in duty cycled mode). For a window of 1 clock period neither the synchronization is achieved because a high jitter affects the window that cannot fit the received pulses. As will be explained in the next session, the PLL control voltage must be adjusted by means of an external current source, that modifies the PLL loop bandwidth and introduces noise, increasing the jitter of the window. Spectrum measurements shows that the PLL jitter is lower when this external current is not used.

- The measured power for the transmitter is not the actual one in the effective system (and reported in section 4.4). First of all because the transmitter delay line is not duty cycled, and on top of that the transmit-

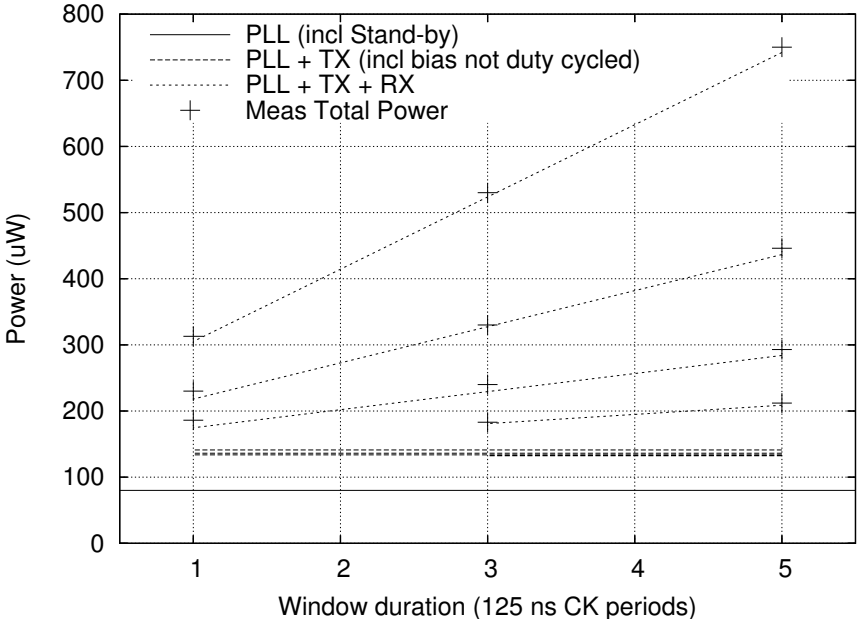

Figure 4.12: *Transceiver power consumption*

ter energy per pulse is higer because its output are practically shorted on board and the load impedance is significantly lower that the antenna's one. Anyway for pulse rates lower than 1 Mpps the power of the transmitter not duty cycle is mainly given by the delay line bias, as shown in figure 4.8.

Assuming that the attenuation introduced by the short over the inductor is similar to the one of a real channel and that the synchronization would be achieved in all the conditions if the external PLL current would not be needed, the power consumption and energy per pulse shown in table 4.6.1 are achieved by the receiver.

The power consumed by the receiver in the above conditions is about 3.5 mW and the maximum measured pulse rate without duty cycle is 50 Mpps. Actually the transmitter has been measured up to 100 Mpps and the limitation of the receiver is partially related to its output buffer. Anyway, power and energy per pulse can be computed for the transceiver working at 50 Mpps without duty cycle. The results are summarized in table 4.6.1.

Note the different behavior with respect to table 4.4 and 4.6.1. The transmitter power is given by the delay line bias plus a contribution proportional

Pulse Rate kpps	Window CK peridos	Power RX μW	Epulse RX nJ/pulse
250	5	600	2.40
250	3	382	1.53
250	1	164	0.66
125	5	300	2.40
125	3	191	1.53
125	1	80	0.64
62.5	5	150	2.40
62.5	3	96	1.54
62.5	1	41	0.66
31.25	5	75	2.40
31.25	3	48	1.54
31.25	1	20	0.64

Table 4.5: Estimated RX power consumption and energy per pulse at 1 V supply

TX power	565 μW
RX power	3500 μW
TX Epulse	11.3 pJ/pulse
RX Epulse	70 pJ/pulse

Table 4.6: Estimated TX and RX power consumption and energy per pulse at 1 V supply for 50 Mpps

to the pulse rate; at high pulse rate the contribution of the delay line is spread over a wide number of pulses per second and this results in an almost constant energy per pulse for the transmitter. Differently the receiver has almost a constant bias current for every pulse rate, and its energy per pulse decreases as the pulse rate increases.

4.6.2 LNA input impedance

The input impedance of the receiver has been measured in with the same technique described in section 4.2. Actually the measured impedance includes the inductor, so to verify the input resonance and impedance at the desired frequency for the system.
Figure 4.13 shows the measured input impedance (including the inductor) for different values of the LNA input capacitance at nominal bias current. Increasing the capacitance the resonant frequency decreases as expected.

Figure 4.14 shows the same plot for a fixed input capacitance and a variable current. At the resonance frequency, the input impedance decreases as the bias current increases. This is also shown in figure 4.15 for the impedance modulus.

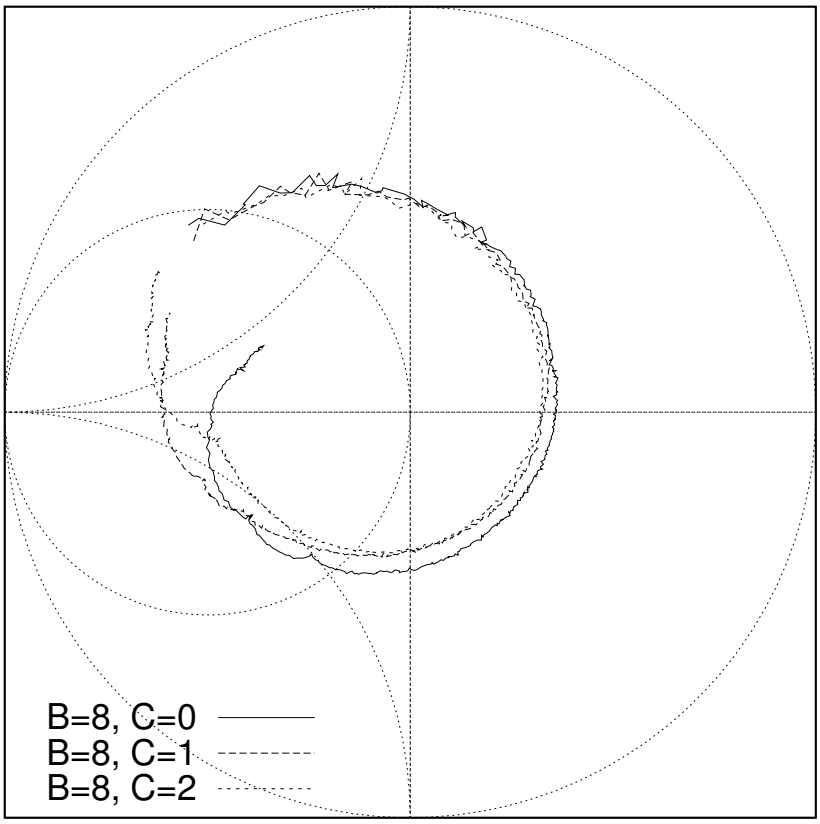

Figure 4.13: *Input reflection coefficient for different input capacitance*

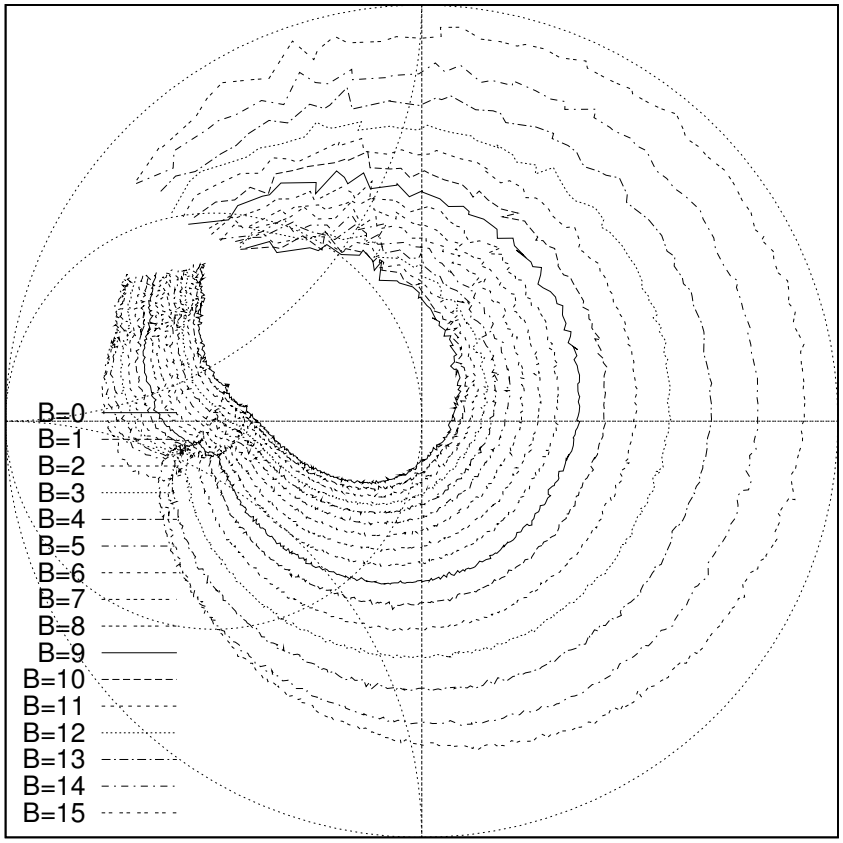

Figure 4.14: *Input reflection coefficient for different LNA bias currents*

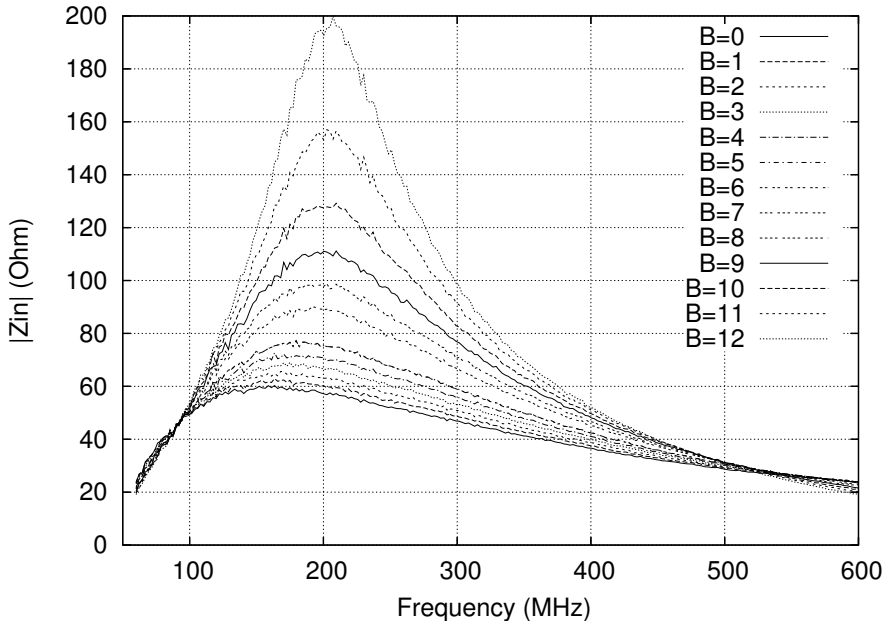

Figure 4.15: *Input impedance moduli for different LNA bias currents*

CP reference	2.5 μW
CP bias	2 μW
Loop filter reference	6.5 μW
Total Analog Stand-by	12.5 μW
Digital Leakage	15.5 μW
Loop Filter	24.4 μW
Charge pump	1 μW
VCO 10.24 MHz	23.2 μW
VCO 8 MHz	17.2 μW
Meas Total Power 10.24 MHz	76.6 μW
Meas Total Power 8 MHz	70.6 μW

Table 4.7: PLL power consumption at 1 V supply

4.7 PLL and Synchronization

The PLL is the main responsible of the analog stand-by current because of the charge pump and loop filter references. The measured PLL power consumption is 76.6 μW at 10.24 MHz VCO frequency with 320 kHz reference. At 8 MHz VCO frequency with 250 kHz reference the power is 70.6 μW. Both from simulations and measurements the PLL power budget of table 4.7 can be done.

The PLL has been measured without the high current loop filter reference (VrefBoost = 0) that would consume 19.2 μA if turned on. The Loop filter bias current can actually be reduces down to 6.8 μA without degrading substantially the PLL stability. The measured frequency vs. control voltage characteristic of the VCI is shown in figure 4.16.

PLL measurement, however, show a phase delay between the edges at the PFD inputs (figure 4.17) that causes problems in the synchronization procedure.
Due to the gate leakage phenomena, the control input of the VCO leaks from V_{DD} a current of about 200 nA at nominal VCO frequency. Because of this leakage, the charge pump should be opened for a while every cycle, to cancel the average current injected by the gate leakage. This requires a misalignment between the reference and the divider output edges at the input of the PFD, resulting in a frequency locking with a phase mismatch, hence a time delay, that depends on the VCO frequency and the reference frequency.

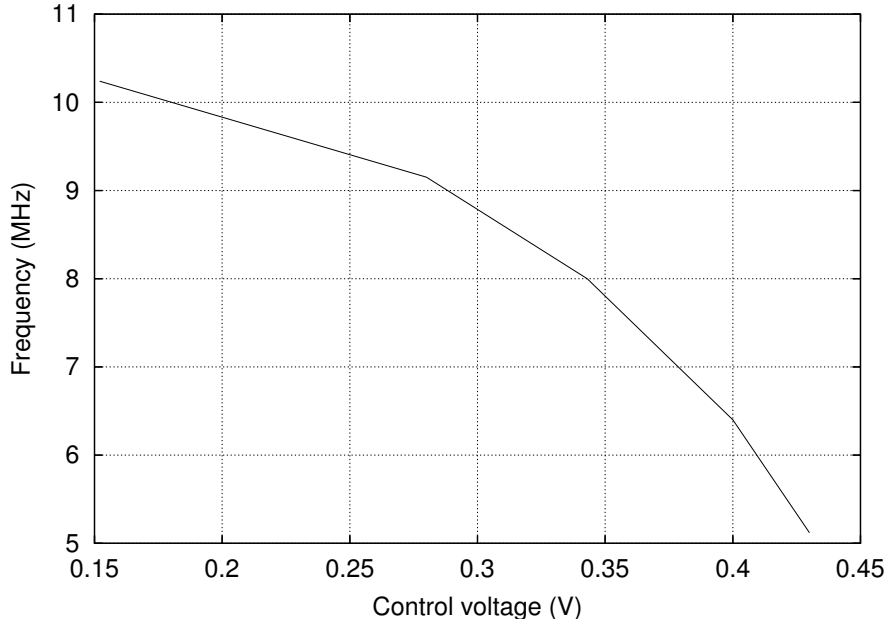

Figure 4.16: *VCO frequency versus control voltage*

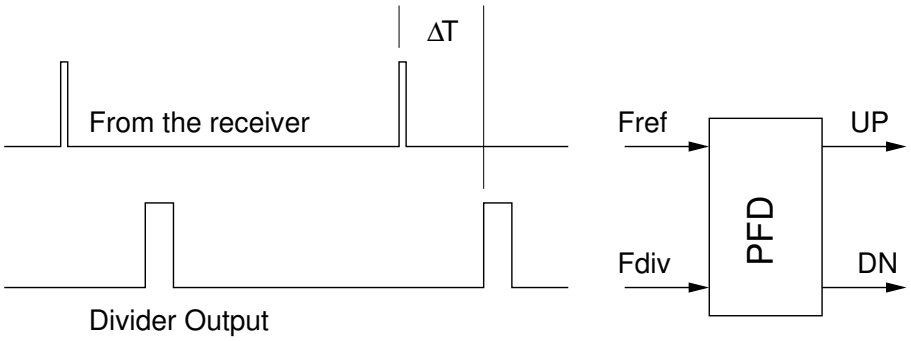

Figure 4.17: *PFD inputs in lock condition*

4.7.1 Leakage effects

Apparently the PLL uses an active filter and a small current drawn from the filter's output should not be a problem as long as the operational amplifier operates in high gain region. Actually the loop filter is not connected to the VCO for the 100% of the reference period, because a large fraction of this time is used for OPAMP offset cancellation and the loop filter operates in a "passive" way.
The "active" operation mode is shown in figure 4.18 (left side), while the

passive one (when the OPAMP is connected in unity gain feedback to cancel the offset) in figure 4.18 (right side). TP is the pulse repetition period. While

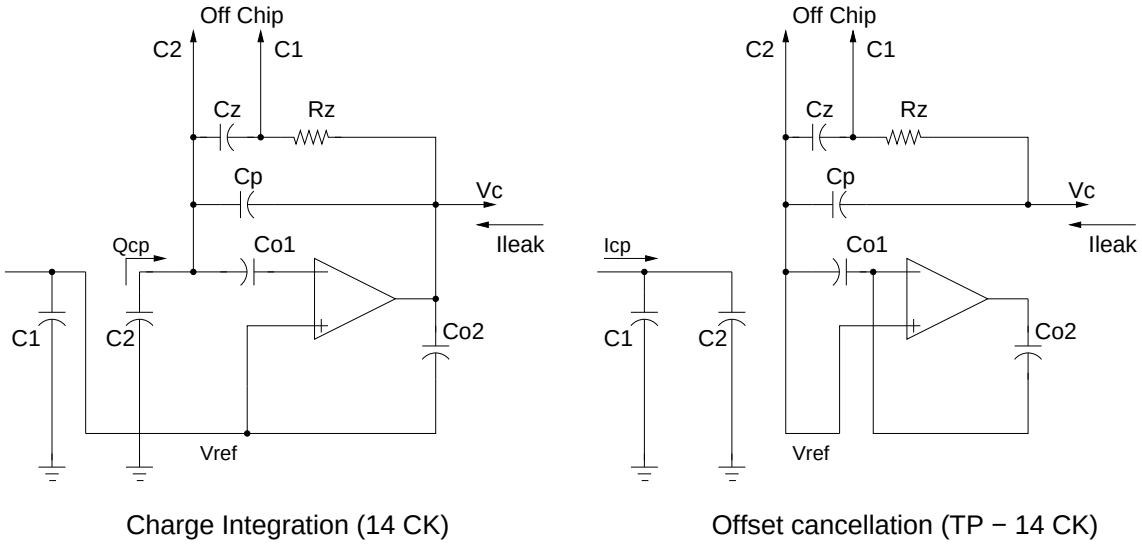

Figure 4.18: *Detailed PLL filter operations*

in the first phase the control voltage of the VCO is fixed by the OPAMP output, in the second phase the voltage must be kept by the capacitors C_P and C_Z, while the OPAMP is disconnected from the output. A current leakage through the VCO caused an average current that must be canceled every reference period to keep the control voltage with a constant average. This current can only be provided with a charge pump pulse, and therefore a finite difference in the PFD input phases occurs. This difference is function of the charge pump current, the leakage current, hence the VCO control voltage, and the amount of time while the OPAMP is not connected to the output. At the smallest reference frequency (20 kHz) the PLL cannot neither lock because the effective charge pump current (65 nA) is lower than the leakage current. This current can theoretically be canceled by subtracting the same current from the VCO control node, that is not accessible outside the chip. Practically this is obtained putting an external high value resistor between the resistor R_z (through pin C1) and an "ad-hoc" potential, function of the VCO frequency. Leakage current reduction can be also achieved by reducing the VCO frequency down to 8 MHz, thus reducing the V_{gs} on the VCO PMOS (see figure 2.24). In order to have a perfect charge balance at the VCO control node

$$Q_{leak} = I_{leak} \cdot T_{leak} = Q_{CP} = I_{eff,CP} \cdot \Delta T \tag{4.1}$$

where ΔT is the delay between the edges at the PFD input and T_{leak} the time interval when the loop filter output is not connected to the OPAMP.
From the design of the loop filter control logic, it turns out that the OPAMP is connected to the VCO for 14 periods, and therefore

$$T_{leak} = T_{VCO} \cdot (512/SpeedUP - 14) \tag{4.2}$$

The effective charge pump current given by (see 2.6.4)

$$I_{eff,CP} = I_{CP} \cdot SpeedUP/16 \tag{4.3}$$

where

$$SpeedUP = 512F_{ref} \cdot T_{VCO} = \frac{512}{N} \tag{4.4}$$

being N the modulus of the PLL counter (frequency division ratio).
With these substitutions, 4.1 leads to

$$\Delta T = T_{VCO}\frac{I_{leak}}{I_{CP}}\frac{512/SpeedUP - 14}{SpeedUP/16} \tag{4.5}$$

Form equation 4.5 and measurements of the delay ΔT at different VCO frequencies, together with the measurements of the VCO control voltage V_C, a best-fid model for the leakage current as a function of the VCO control voltage V_c can be found. A parabolic function has been assumed for $I_{leak}(V_c)$.

Figure 4.19 shows the delay between the reference edge and the divider edge as a function of the charge pump current for different control voltage, hence the VCO frequencies (10.24, 9.152, 8, 6.4 and 5.1 MHz from the top to the bottom respectively), together with the delay obtained by equation 4.5 with the best fit function for $I_{leak}(V_C)$.

Figure 4.20 shows the fitted dependency of I_{leak} on the control voltage, together with the simulated curves. Even if they are not exactly the same (gate leakage is hardly modeled and strongly depends on the process corner) a relationship can be clearly shown.
Unfortunately, gate leakage simulation was not available at the time of the circuit design, while it is now with a new and improved design kit.

Figure 4.21 finally shows the measured and predicted value of the delay ΔT as a function of the charge pump current and for different division ratio with the VCO running at 10.24 MHz (128, 64 and 32 from the top to the

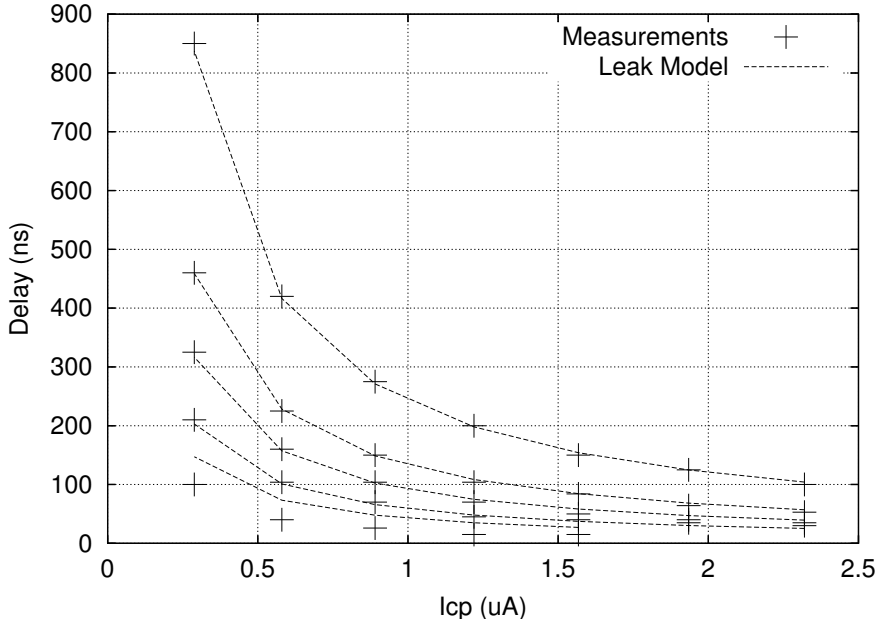

Figure 4.19: *PFD edges delay ΔT as a function of the charge pump current I_{CP} for different VCO control voltages*

bottom). Once again, good agreement between measurements and the model can be shown.

4.7.2 Synchronization on duty cycled operation

Both reducing the VCO frequency down to 8 MHz and subtracting a proper current from the pin C1 by means of an external resistance, the synchronization can be achieve.
To perform this measurement, the same chip has been used both as transmitter and receiver, as discussed in the receiver measurements section.
Figure 4.22 shows the clock windows of 125 ns duration together with the BitSync output, that produces a pulse for every detected pulse. Figure 4.23 reports the same situation with a lower time resolution, and 3 RX_CK pulses are shown with a 250 kpps pulse rate.
Figure 4.24 and 4.25 show the received data and the clock and data windows (RX_CK and RX respectively) when multiple data are received between two clock pulses in a TDMA fashion. In this particular case 3 bits are equally

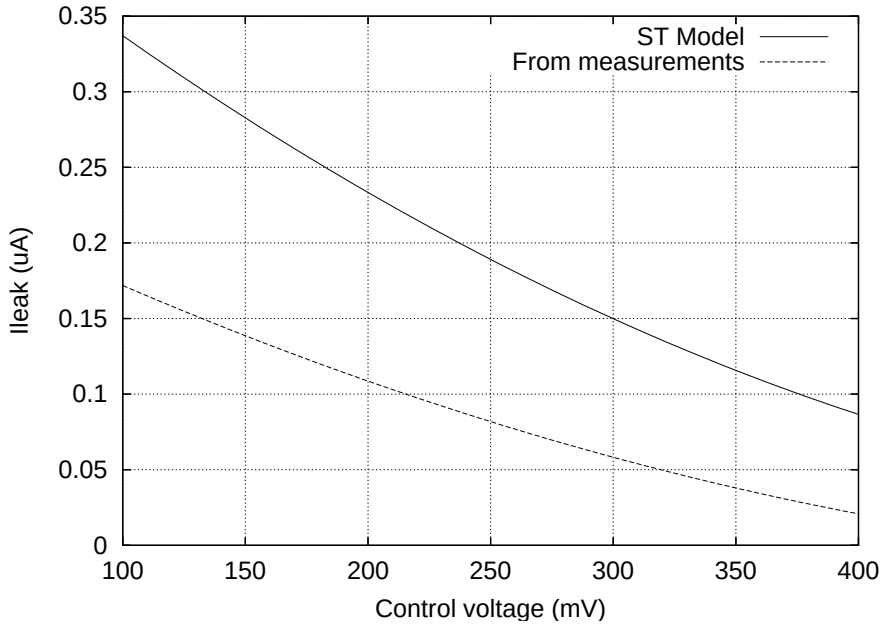

Figure 4.20: *VCO leakage current I_{leak} as a function of the control voltage - ST model and curve extracted from measurements*

spaced between two clock pulses at 250 kpps.

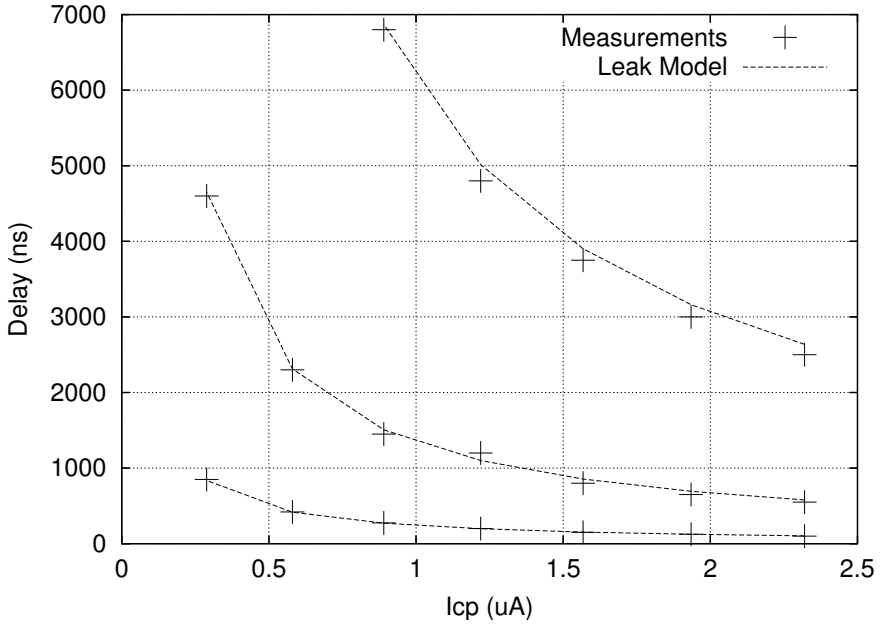

Figure 4.21: *PFD edges delay ΔT as a function of the charge pump current I_{CP} for different division ratio at 10.24 MHz VCO frequency*

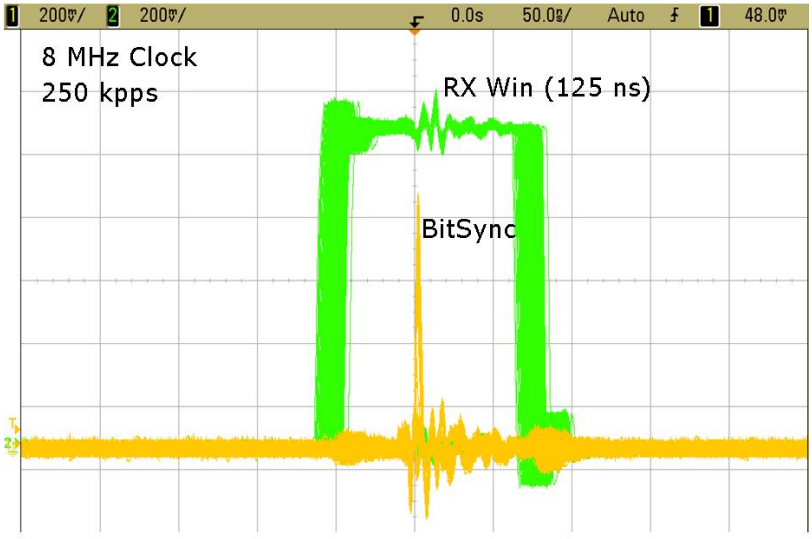

Figure 4.22: *Received pulse fitted by the clock receiving window*

Figure 4.23: *3 received pulses at 250 kpps fitted by the clock receiving windows of 125 ns*

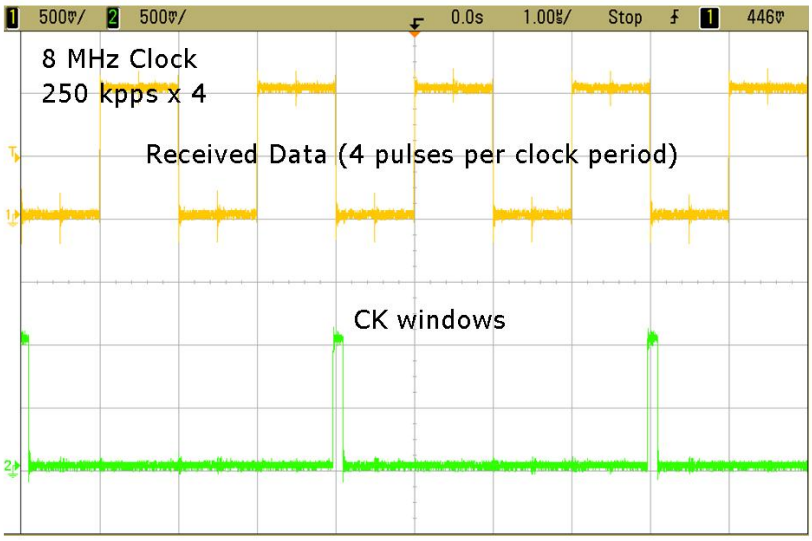

Figure 4.24: *Received multiple data and clock windows*

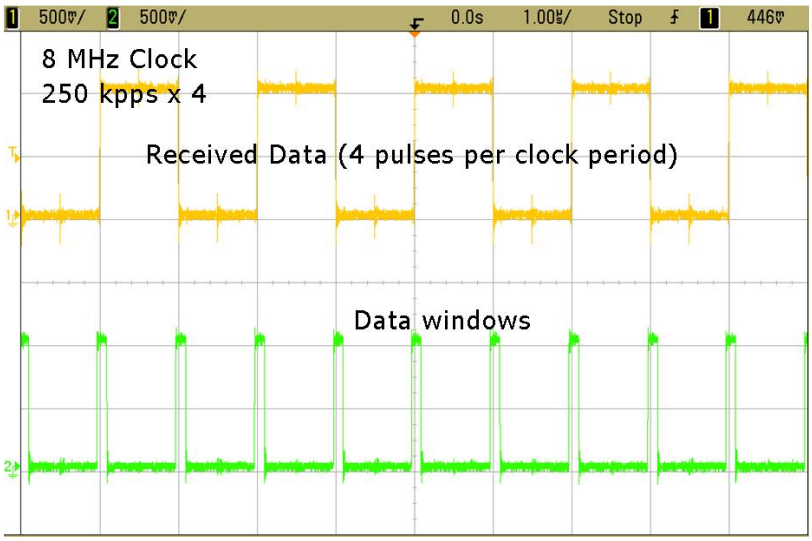

Figure 4.25: *Received multiple data and data windows*

Conclusions

A wireless transceiver based on inductive coupling has been designed, fabricated and tested. The communication is achieved by means of the transmission of signed pulse at low bit rate, and power saving can be achieved in the receiver by means of duty cycle. The receiver is synchronized on the incoming data flow through a phase lock loop (PLL), that is used to duty cycle the system. In this way the synchronization does not require of a local crystal oscillator and a high degree of integration can be achieved.

Despite many problems encountered during the measurements, some interesting data have been collected and reported. Three main problems that limit the performance of the system have been identified:

- The coupling factor between a transmitter inductor and a receiver inductor laid out on the same plane is dramatically lower than expected. The only way to get a communication is to stack the two inductors one on top of the other at a distance lower than 1 cm. Even if this difference with the previous channel measurements is still unclear, it is possibly due to the lines needed to connect the die and the other components that surround the inductors. These can have a shield effect on the magnetic filed reducing dramatically the coupling factor. Inductors stacked one on top of the other, without any line in between, show a coupling factor not so far from the expected one.

- The switching of digital lines close to the receiver antenna, such as the transmitter inputs and especially the receiver outputs, generate a magnetic field that is detected by the receiver antenna. These interferences, especially the lattr, make the receiver unstable if the "wanted" signal level is below the interference. The receiver can work only at a very short distance from the transmitter, when the received signal overwhelms the self coupled noise. At long distance the receiver is mainly unstable due to the feedback between its digital outputs and the antenna.

- A gate leakage current in the VCO produces a phase error in the PLL lock state. This phase error is traduced in a misalignment between the real pulse position and the expected one, and of course it makes the synchronization not possible on the chip as it is. However by reducing the VCO frequency and using an external current generator, the synchronization mechanism has been proved.

Apart from these problems, a loopback test (using the transmitter to directly feed a receiver on the same chip) is able to proof the concept of the pulse based radio and the proposed synchronization scheme.

Further revision of the system, anyway, would require major revision of the design. Some of them are quite easy to achieve and have immediate impact on the perform ace, while for some of them is not clear if they can lead to a real advantage

- Reduction the gate leakage in the VCO, i.e. by means of another current mirror in the bias circuit or with a new loop filter design.

- Choose a different topology for the digital outputs, to avoid coupling with the antenna. Low drop differential output can be useful to reduce interference, or the received bit can be temporarily stored in a on-chip memory and read off-line.

- Minimization of the board size (if possible) and chip I/O, to reduce the lines surrounding the inductor, possible responsible of the reduced coupling factor.

- Memorization of the transmitted test sequence in a memory on chip, avoiding to feed the transmitter with data. The the transmitter clock line still remains, since the system assumes that at least one node is provided with an (external) crystal oscillator. Low drop differential input can be used to alleviate the problem.

- The single ended comparators show a very high sensitivity to the supply variation. A differential implementation can reduce that sensitivity.

- A redesign of the pulse-polarity detection scheme (clock and data recovery circuit) that is insensible to the output ringing (e.g. only detect the first positive-negative or negative-positive transition) will reduce the sensitivity of the receiver to the gain-bandwidth configuration.

- The digital I/O buffers seems to be too strong. A reduction of their size, together with an increasing of the ground and supply pads, will reduce output ringing and will increase the SPI reliability.

- The receiver should be improved to allow for operation at lower gain with the same bandwidth (or even hugher). Particularly the possibility of having lower gain at the nominal bandwidth must be implemented. At the moment low gains without band reduction can be achieved only halving the load resistors; a more "continuous" load resistor scaling is desirable".

The conclusion that one can drawn from this project are still unclear. The chip itself seems to work quite close to simulation, apart from well identified problems. However two points suggest that this cannot be the right way for a reliable short range wireless system.

- The "apparent" lack of coupling between inductors laid out on the same plane must be investigated. It can be due to an excess of lines around then, that actually should not be present in a real node. However simulation and measurements in the possible environment for the node must be done before further continue in this direction.

- The excess of coupling with the interferences suggest that a pure energy detection scheme is probably not the best choice for this kind of application. Correlation and other selective techniques must be used to reject interference and detect only the wanted signals.

Appendix: Super-Regenerative Receiver

Before studying the pulse based radio, a super-regenerative approach was considered [21]. Analysis showed that this was not the most efficient way to implement the transceiver described in this report. In this chapter a simple analysis of the super-regenerative receiver is summarized, followed by some considerations and comparison with the pulse based one.

Super regenerative operating principle

A super-regenerative receiver is mainly an oscillator that is kept as close as possible to the Barkhausen's condition; the active part is periodically tuned to be (infinitesimally) larger than the one needed to exactly cancel the losses of the tank. It can be shown that the start-up time of the oscillator depends on the amplitude and the frequency of the signal injected into the tank. Usually this signal is given by the thermal noise of the tank parallel resistance and the active part of the circuit used to generate the negative impedance.
In this case an induced voltage V_i is assumed on the inductor of an LC tank, given by the coupling with another oscillator, as shown in figure 4.26.
The equation of the system are given by

$$V = -L\frac{\mathrm{d}I_L}{\mathrm{d}t} + V_i \tag{4.6}$$

$$I_L = C\frac{\mathrm{d}V}{\mathrm{d}t} + (g_L - g_m)V \tag{4.7}$$

$$\tag{4.8}$$

hence

$$V = -LC\frac{\mathrm{d}^2V}{\mathrm{d}t} + L(g_L - g_m)\frac{\mathrm{d}V}{\mathrm{d}t} + V = V_i$$

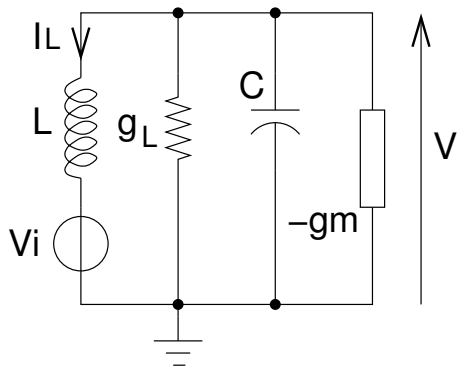

Figure 4.26: *LC tank including losses and negative gm*

$$\frac{\mathrm{d}^2V}{\mathrm{d}t}\frac{g_L - g_m}{C}\frac{\mathrm{d}V}{\mathrm{d}t} + V = V_i$$

In the $\mathcal{L}$-trasf domain, as well known, it is

$$V = H(s)V_i \tag{4.9}$$

with

$$H(s) = \frac{\omega_0^2}{s^2 + s\frac{2}{\tau} + \omega_0^2} \tag{4.10}$$

and

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad \tau = \frac{2C}{g_L - g_m}$$

The oscillation condition is satisfied if

$$g_m > g_L \quad \longrightarrow \quad \tau < 0$$

and then

$$H(s) \simeq \frac{\omega_0^2}{(s - 1/\tau)^2 + \omega_0^2} = \frac{\omega_0^2}{(s - p_1)(s - p_2)} = \frac{\omega_0^2}{s^2 - s(p_1 + p_2) + p_1 p_2} \tag{4.11}$$

If $-\tau^{-1} << \omega_0$ the poles can be written as

$$p_{1,2} = \frac{g_L - g_m}{C} \pm j\omega_0 \tag{4.12}$$

Since the poles have a positive real part the system is unstable. Assuming a cosine wave of amplitude A and angular frequency ω_i for the input, it is

$$V_i = \frac{As}{s^2 + \omega_i^2}$$

and

$$V = \frac{\omega_0^2}{s^2 + s\frac{2}{\tau} + \omega_0^2} \frac{As}{s^2 + \omega_i^2}$$

that can be written as

$$V = \frac{\alpha s + \beta}{s^2 + \omega_i^2} + \frac{\gamma s + \delta}{(s + 1/\tau)^2 + \omega_0^2} \tag{4.13}$$

by satisfying the equation system

$$s^3(\alpha + \gamma) = 0 \tag{4.14}$$
$$s^2(\beta + 2\alpha/\tau + \delta) = 0 \tag{4.15}$$
$$s(\alpha\omega_0^2 + 2\beta/\tau + \gamma\omega_i^2) = sA\omega_0^2 \tag{4.16}$$
$$1(\beta\omega_0^2 + \delta\omega_i^2) = 0 \tag{4.17}$$

that gives

$$\gamma = -\alpha \tag{4.18}$$
$$\delta = -\beta\frac{\omega_0^2}{\omega_i^2} \tag{4.19}$$

The first part of equation 4.13 is easily recognized as the forced response of the system at the input V_i. Then

$$\alpha = \mathcal{R}\{H(\omega_i)\}$$

$$\beta = \omega_i\mathcal{I}\{H(\omega_i)\}$$

and therefore

$$\gamma = -\alpha = -\mathcal{R}\{H(\omega_i)\}$$

$$\delta = -\beta\frac{\omega_0^2}{\omega_i^2} = -\omega_i\mathcal{I}\{H(\omega_i)\}\frac{\omega_0^2}{\omega_i^2}$$

Being

$$\mathcal{L}^{-1}\left\{\frac{\gamma s + \delta}{(s + 1/\tau)^2 + \omega^2}\right\} = e^{-t/\tau}\left[\gamma\cos(\omega t) + \left(\frac{\delta - \gamma/\tau}{\omega}\right)\sin(\omega t)\right]$$

the response of the system in the time domain can be written as

$$V(t) = A\mathcal{R}\{H(\omega_i)\}\cos(\omega_i t) + A\mathcal{I}\{H(s)\}\cos(\omega_i t) +$$

$$-A\mathcal{R}\{H(\omega_i)\}e^{-t/\tau}\cos(\omega_0 t) + \frac{-\omega_i\mathcal{I}\{H(\omega_i)\}\frac{\omega_0^2}{\omega_i^2} + \mathcal{R}\{H(\omega_i)\}/\tau}{\omega_0}e^{-t/\tau}\sin(\omega_0 t) \tag{4.20}$$

and if ω_i is close to ω_0 it is

$$V(t) \simeq \|H(\omega_i)\|\cos(\omega_i t + \angle H(\omega_i)) - \|H(\omega_i)\|e^{-t/\tau}\cos(\omega_0 t + \angle H(\omega_i))$$

The system clearly is unstable having complex conjugate poles with positive real part. The first part of the response depends only on the input signal (forced response), while the second part is due to the instability of the system. Once the oscillation is injected, the envelope can be written as

$$V_{env} \simeq A\|H(\omega_i)\|e^{-t/\tau} \simeq A\frac{\omega_0\tau}{2}e^{-t/\tau} \tag{4.21}$$

However, since the system is unstable, even if no input signal V_i is applied it starts to oscillate injected by noise, such as commonly happen in LC oscillators. Considering a current noise source i_n in parallel with the conductances g_L and g_m of power spectral density

$$\frac{i_n}{\Delta f} = 4KTg_L(1+F)$$

where $4KTg_L$ is the noise power spectral density of the tank parallel resistor while $F(>0)$ takes into account for the noise of the active transconductor g_m. In time domain it is

$$\frac{\mathrm{d}^2V}{\mathrm{d}t}\frac{g_L - g_m}{C}\frac{\mathrm{d}V}{\mathrm{d}t} + V = -\frac{1}{C}\frac{\mathrm{d}i_n}{\mathrm{d}t}$$

and in the $\mathcal{L}$-trasf domain it is

$$s^2V + \frac{g_L - g_m}{C}sV + \omega_0 = -\frac{1}{C}si_n$$

The noise transfer function can therefore be written as

$$H_n(s) = \frac{-\frac{s}{C}}{s^2 + \frac{2}{\tau}s + \omega_0} \tag{4.22}$$

and if $\tau << 1/\omega_0$ it can be approximated as

$$H_n(s) \simeq \frac{-\frac{s+1/\tau}{C}}{(s+1/\tau)^2 + \omega_0}$$

In the same way the time domain impulse response can be approximated with

$$h_n(t) = -\frac{1}{C} e^{-t/\tau} \cos(\omega_0 t)$$

The output voltage is therefore

$$V(t) \simeq -\frac{1}{C} \int_o^{+\infty} i_n(\xi) e^{-(t-\xi)/\tau} \cos(\omega_0 (t-\xi)) \mathrm{d}\xi =$$

$$= -\frac{e^{-t/\tau}}{C} \int_o^{+\infty} i_n(\xi) e^{\xi/\tau} \cos(\omega_0 t - \omega_0 \xi)) \mathrm{d}\xi =$$

$$= -\frac{e^{-t/\tau}}{C} \cos(\omega_0 t) \int_o^{+\infty} i_n(\xi) e^{\xi/\tau} \cos(\omega_0 \xi) \mathrm{d}\xi - \frac{e^{-t/\tau}}{C} \sin(\omega_0 t) \int_o^{+\infty} i_n(\xi) e^{\xi)/\tau} \sin(\omega_0 \xi) \mathrm{d}\xi$$

Hence, defining $V_{n,cos}$ and $V_{n,sin}$ it is

$$V(t) = -V_{n,cos} e^{-t/\tau} \cos(\omega_0 t) - V_{n,sin} e^{-t/\tau} \sin(\omega_0 t)$$

with

$$V_{n,cos} = \frac{1}{C} \int_o^{+\infty} i_n(\xi) e^{\xi/\tau} \cos(\omega_0 \xi) \mathrm{d}\xi$$

$$V_{n,sin} = \frac{1}{C} \int_o^{+\infty} i_n(\xi) e^{\xi/\tau} \cos(\omega_0 \xi) \mathrm{d}\xi$$

Describing the noise as a random Gaussian process the statistical properties does not depend on time, and therefore

$$V_{n,cos} = \frac{1}{C} \int_o^{+\infty} i_n(t-\xi) e^{\xi/\tau} \cos(\omega_0 \xi) \mathrm{d}\xi$$

$$V_{n,sin} = \frac{1}{C} \int_o^{+\infty} i_n(t-\xi) e^{\xi/\tau} \sin(\omega_0 \xi) \mathrm{d}\xi$$

and $V_{n,cos}$ and $V_{n,sin}$ can be approximated as the responses H_r of the (stable) resonator to the input noise i_n.

$$H_r = \frac{s/C}{s^2 + s\frac{\omega 0}{Q} + \omega_0}$$

with

$$Q = -\frac{\omega_0 \tau}{2} \qquad (Q > 0)$$

The effective voltage of $V_{n,cos}$ and $V_{n,sin}$ can now be computed as

$$V^2_{n,cos,eff} = V^2_{n,sin,eff} = \int_0^\infty \|H_r(\omega)\|^2 \frac{i_n^2}{2\pi\Delta f} \mathrm{d}\omega =$$

$$= \frac{1}{2\pi}\frac{i_n^2}{\Delta f}\int_0^\infty \|H_r(\omega)\|^2 \mathrm{d}\omega =$$

and being

$$x = \frac{\omega}{\omega_0}$$

$$V^2_{n,cos,eff} = \frac{1}{2\pi}\frac{i_n^2}{\Delta f}\frac{1}{(\omega_0 C)^2}\int_{-\infty}^\infty \frac{x^2}{(1-x^2)^2 + \frac{x^2}{Q^2}}\omega_0 \mathrm{d}x$$

Under the hypothesis that Q is real the integral can be approximated as

$$\omega_0 \int_0^\infty \frac{x^2}{(1-x^2)^2 + \frac{x^2}{Q^2}}\mathrm{d}x \simeq \frac{\pi}{2}\omega_0 Q$$

and

$$V^2_{n,cos,eff} \simeq \frac{1}{2\pi}\frac{i_n^2}{\Delta f}\frac{1}{(\omega_0 C)^2}\frac{\pi}{2}\omega_0 Q = \frac{\tau}{8C^2}\frac{i_n^2}{\Delta f}$$

Assuming that $V_{n,cos} = V_{n,sin}$, the effective noise voltage can be written as

$$V^2_{n,eff} \simeq V^2_{n,cos,eff} + V^2_{n,sin,eff} = \frac{-\tau}{4C^2}\frac{i_n^2}{\Delta f}$$

A "signal to noise" ratio of the super-regenerative can be written as

$$SNR_{SR} = \frac{V_{env}}{V_{n,env}} = \frac{A\|H(\omega_i)\|}{V_{n,eff}}$$

that gives a measure of the sensitivity of the system.
If SNR_{SR} is lower than 1, the rise time is almost independent on the input signal. The larger SNR_{SR} is, the greatest the difference in the envelope rise time between the presence or the absence of signal.

Considering a threshold level V_{th} for the envelope signal, the time necessary to reach this threshold with an input amplitude A is

$$T_{th,A} = -\tau \ln\left(\frac{V_{th}}{A\|H(\omega_i)\|}\right)$$

while the time needed without any input signal (apart from the noise) is

$$T_{th,n} = -\tau \ln\left(\frac{V_{th}}{V_{n,eff}}\right)$$

thus resulting in a time difference

$$\Delta t = -\tau \ln\left(\frac{A\|H(\omega_i)\|}{V_{n,eff}}\right)$$

Implementation wise, it is easier to sample the output of the envelope detector at a fixed time (e.g. at the end of the quench pulse) and chose τ so to maximize the voltage difference ΔV between the envelope when injected by the signal and the one when injected by the noise, as shown in figure 4.27.
Assuming a linear model for the oscillator start up it seems that this voltage

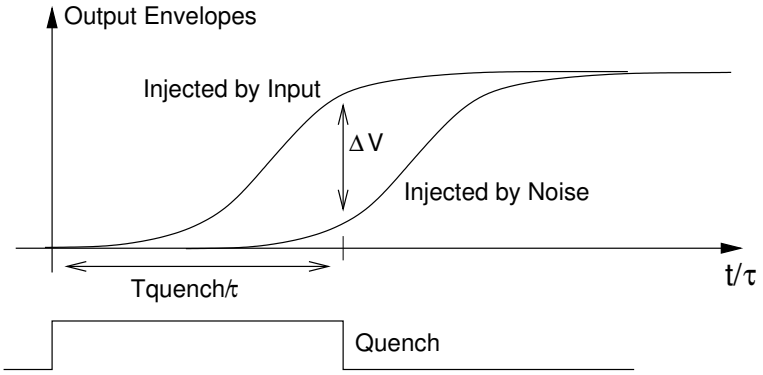

Figure 4.27: *Start up envelope of a VCO in presence and absence of induced signal on the inductor*

difference is going to increase indefinitely with time

$$\Delta V(t) = (A\|H(\omega_i)\| - V_{n,eff})\, e^{-t/\tau}$$

However, in a real oscillator, the amplitude of the oscillation cannot increases forever but is limited by the saturation of the active stage or the power supply (figure 4.27). Clearly an optimal T_{quench}/τ that maximizes ΔV can be found. Since

$$\tau = \frac{2C}{g_L - g_m}$$

and the inductor is assumed to be fixed, once the frequency (hence C) and the tank losses (hence g_L) are given, the optimal can be reached by tuning the oscillator g_m through its bias current.

Initially proposed super-regenerative receiver

The first idea, considered at the beginning of this project for the data link, is sketched in figure 4.28 (and is quite similar to [22], even if it was outlined before).
The transmitter is simply realized by means of an oscillator that is OOK

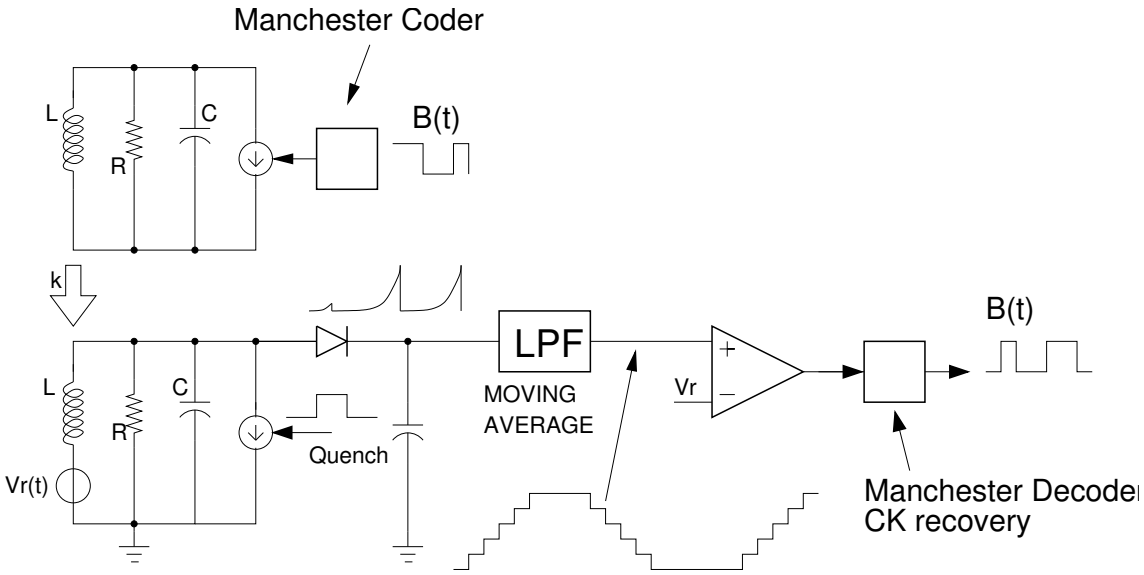

Figure 4.28: *VCO and super-regenerative receiver*

modulated by the digital data. The tank of the VCO is given by an integrated capacitance and the on board inductor previously discussed. A Manchester code must be used to avoid long 0 or 1 sequences; these would make hard the synchronization of the receiver with an OOK modulation.
As receiver the same oscillator can be used, but its bias is "quenched" and the start up time is measured. A proper feedback loop is needed to set the proper VCO bias current so to keep if as close as possible to the Barkhausen's conditions. The quench frequency must be chosen high enough to account many quench periods for each bit, and a moving average filter is used for the bit detection. Synchronization can be extracted from the received sequence thanks to the Manchester coding.
A possible transceiver architecture is shown in figure 4.29.

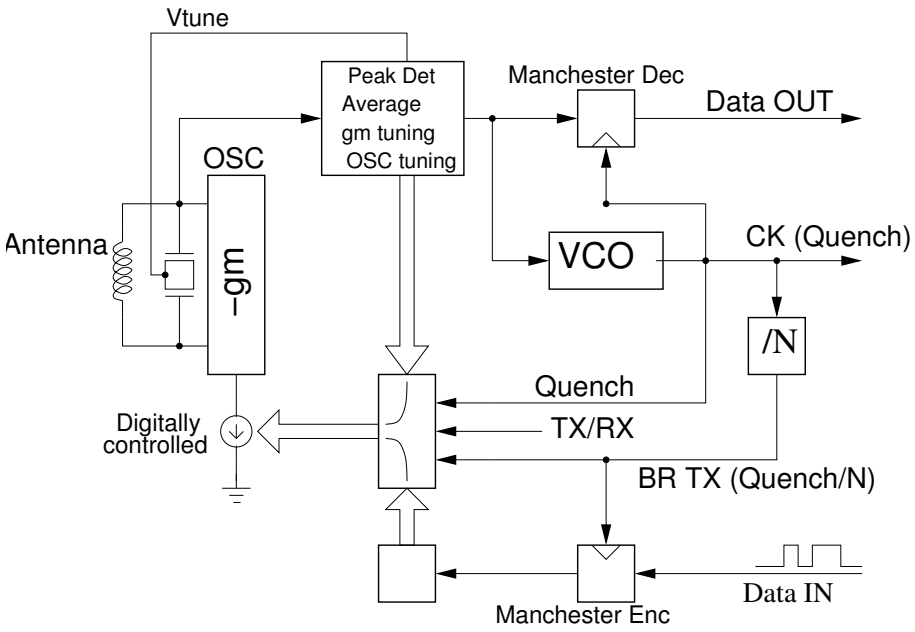

Figure 4.29: *Possible transceiver based on a super-regenerative principle*

Comparison with a pulse based transceiver

Without going through too many details, for this particular application a super-regenerative approach turns out to be not convenient in terms of power efficiency with respect to a pulse based one for small bit rate. Moreover, some drawbacks emerge considering the proposed super-regenerative transceiver architecture.

- Power consumption: Using a super-regenerative receiver, the only allowed transmitter is an OOK modulated oscillator. It is easily observed that the energy required by the transmitter is greater by far than in the case of the pulse based one. Assuming that it is not possible to do a VCO with less than 100 μW, because of the finite tank resistance that can be achieved, and a 50% OOK modulation, the transmitter power consumption is in the order of 50 μW.

- Selectivity: the selectivity of the super-regenerative receiver depends on the quality factor of the tank, that is limited by technological issues (i.e. inductor on board versus FBAR resonators). A high Q tank results in a high selectivity for the receiver as is amenable, but on the other side

only a low frequency offset is tolerated between the transmitter and the receiver. While this is easily achieved by FBAR resonators [21] this does not apply for on board inductors and integrated capacitance.

- Multichannel: being a narrow band system, a frequency division multiplexing is necessary. This requires tuning capability for the VCO and probably and RF PLL to set the oscillation frequency to the desired value.

- Synchronization issues: the synchronization of the receiver must be done extracting the bit rate from the received sequence. This can probably be achieved together with the data recovery, by digitalizing the peak detector output. However this is going to add complexity to the system.

- Re-radiation: once the super-regenerative receiver is injected it effectively behaves like an oscillator and can inject its close nodes resulting in an information "leakage" through the nodes. Of course this does not happen in a pulse based radio.

These considerations lead to the design of a pulse based transceiver instead of a narrow band - super-regenerative one. However they must not be taken like "absolute true". They only means that the particular application and the design constraints subject of this work are better suited for a pulse based radio. The availability of high Q resonator, like in [21], can radically change the previous consideration.

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