SiC Power Devices and Modules
Application Note
Rev.003

Note:
The evaluation data and other information described in this application note are the results of evaluation by ROHM under identical conditions and presented as references.
We do not guarantee the characteristics described herein.

Contents

1. SiC semiconductor

1.1 Physical properties and features of SiC

SiC (silicon carbide) is a compound semiconductor material composed of silicon (Si) and carbon (C). Table 1-1 shows the electrical characteristics of each semiconductor material. SiC has an excellent dielectric breakdown field intensity (breakdown field) and bandgap (energy gap), which are 10 times and 3 times greater than Si, respectively. Furthermore, control over the p- and n-types necessary for device manufacturing can be achieved in a wide range. Consequently, SiC is considered as a promising material for power devices that can exceed the limit of Si. SiC has various polytypes (crystal polymorphism), and each polytype shows different physical properties. For power devices, 4H-SiC is considered to be ideal and its monocrystalline wafers between 4 inches and 6 inches are currently mass produced.

Table 1-1. Electrical characteristics of semiconductor materials

Properties	Si	4H-SiC	GaAs	GaN
Crystal Structure	Diamond	Hexagonal	Zincblende	Hexagonal
Energy Gap : E_G (eV)	1.12	3.26	1.43	3.5
Electron Mobility : μ_n (cm^2/Vs)	1400	900	8500	1250
Hole Mobility : μ_p (cm^2/Vs)	600	100	400	200
Breakdown Field : E_B (V/cm) X10^6	0.3	3	0.4	3
Thermal Conductivity (W/cm℃)	1.5	4.9	0.5	1.3
Saturation Drift Velocity : v_s (cm/s) X10^7	1	2.7	2	2.7
Relative Dielectric Constamt : ε_S	11.8	9.7	12.8	9.5
p, n Control	○	○	○	△
Thermal Oxide	○	○	×	×

1.2 Features as power devices

Due to the high dielectric breakdown field intensity of SiC, which is approximately 10 times higher than that of Si, high breakdown voltage power devices from 600 V to several thousand V can be manufactured with a drift layer having a higher impurity concentration and a thinner thickness compared with Si devices. Most of the resistance component of high breakdown voltage power devices is the resistance of this drift layer. Therefore, SiC can realize high breakdown voltage devices with a very low on-resistance per unit area. Compared with Si, the drift layer resistance per area can theoretically be reduced to 1/300 at the same breakdown voltage. With Si, minority carrier devices (bipolar devices) including IGBTs (insulated gate bipolar transistors) have been mainly used to address the increase in the on-resistance associated with a higher breakdown voltage. However, they suffer from a large switching-loss and high frequency drive is limited due to the heat generated as a result of the switching-loss. In contrast, using SiC, a high breakdown voltage can be achieved with majority carrier devices (Schottky barrier diodes and MOSFET), which are high speed device structures. Therefore, all three features, namely “high breakdown voltage”, “low on-resistance”, and “high speed”, can be simultaneously realized.

Furthermore, its bandgap is approximately 3 times wider than that of Si, enabling power devices that can be operated at a higher temperature (although the guaranteed temperature is presently around 150°C to 175°C due to restriction from the heat resistance reliability of packages, a guaranteed temperature above 200°C can be realized with progress in the package technology in the future).

2. Features of SiC SBD

2.1 Device structure and features

With SiC, high breakdown voltage diodes above 1,200 V can be realized using the Schottky barrier diode (SBD) structure (up to approximately 200 V with Si-based SBD).

As a result, as shown in Figure 2-1, the recovery loss can be significantly reduced by replacing currently prevailing high speed PN junction diodes (FRD: fast recovery diode) with SBD. This contributes to improvement in the power supply efficiency, downsizing of passive components including coils by high frequency drive, and noise reduction. Their applications are mainly power factor correction (PFC) circuits and secondary side rectifying bridges, and extending to onboard chargers for EV, power conditioners for solar power generation, power supplies for servers, air conditioners, and so on.

Currently, SBD with breakdown voltages of 650 V, 1,200 V, and 1,700 V are listed in ROHM's lineup.

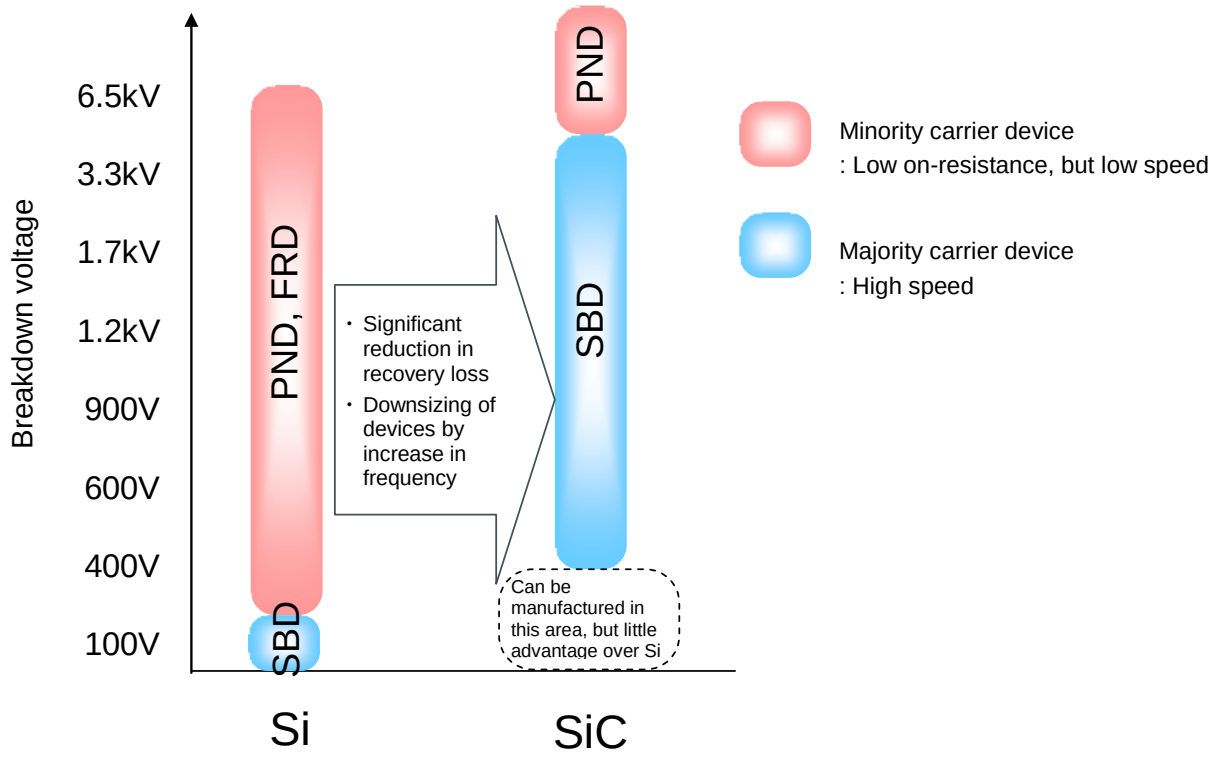
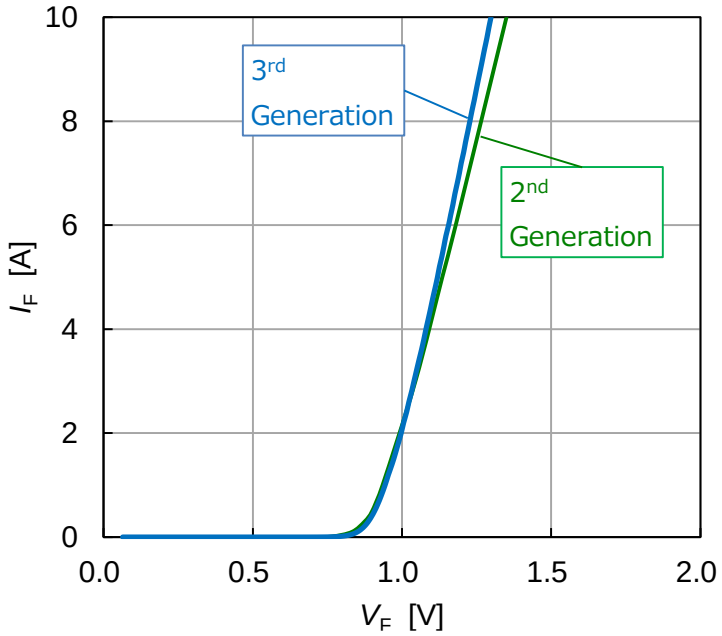


Figure 2-1. Rated voltage ranges for Si and SiC (diodes)

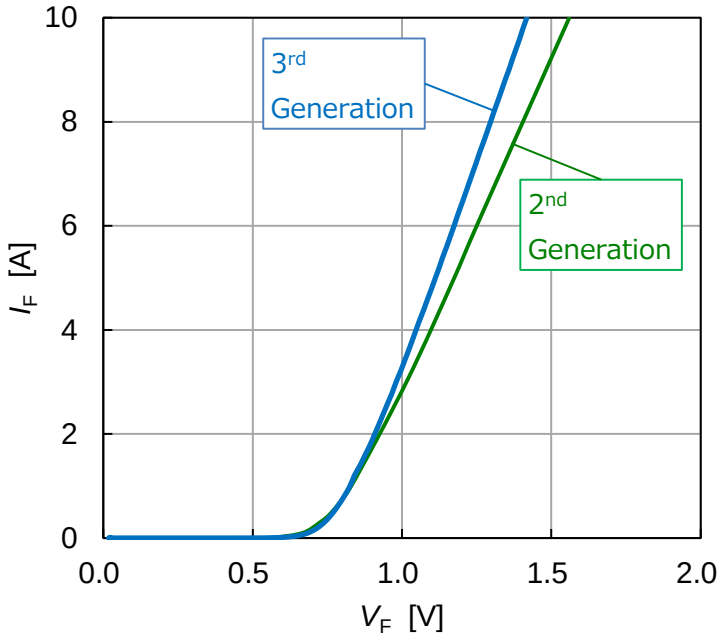
2.2 Forward characteristics of SiC SBD

The rising voltage of SiC SBD is a little less than 1 V, similar to Si FRD. The rising voltage is determined by the height of the Schottky barrier and can usually be reduced by designing a lower barrier height. However, there is a trade-off relation between the rising voltage and the leakage current in a reverse bias condition, which increases as the barrier height decreases. In the second generation of ROHM's SBD, innovations in processes successfully reduced the rising voltage by approximately 0.15 V while maintaining the leakage current and the recovery performance at the same level as conventional products. Furthermore, in the third generation SBD, V_F and the leakage current are further reduced by combining the JBS (junction barrier Schottky) structure and the low V_F process for the second generation SBD. In particular, V_F is significantly reduced at high temperature.

The temperature dependence differs from that of Si FRD, showing increase in V_F due to increase in the operating resistance as temperature increases. They can be safely used in parallel connections because a thermal runaway is unlikely to occur. Figure 2-2 shows typical V_F-I_F characteristics.



(a) Tj=25℃



(b) Tj=150℃

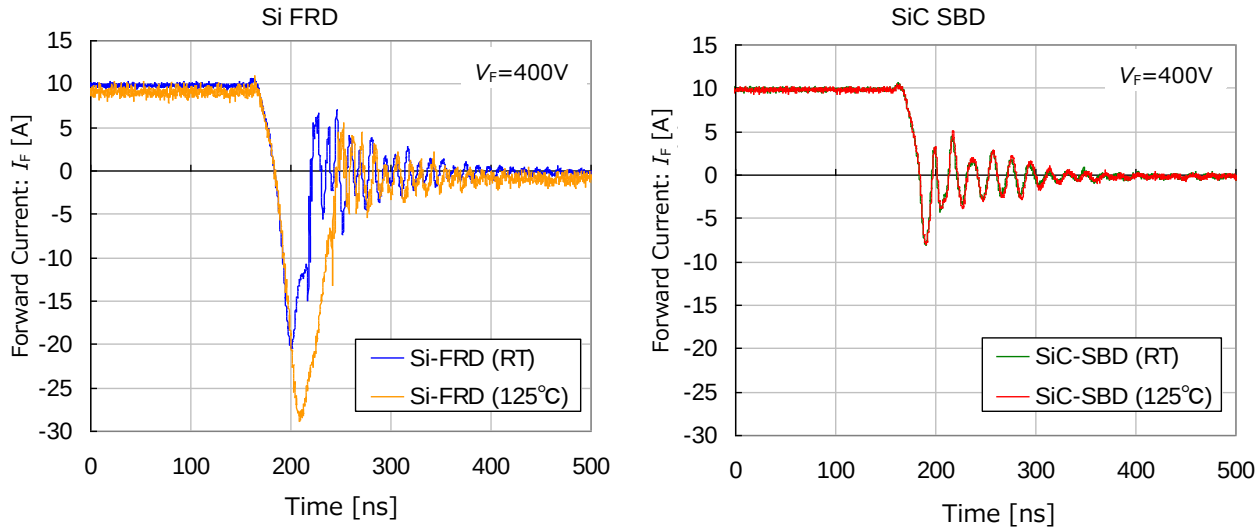
Figure 2-2. Forward characteristics of SiC SBD (650 V, 10 A class)

2.3 Recovery characteristics of SiC SBD

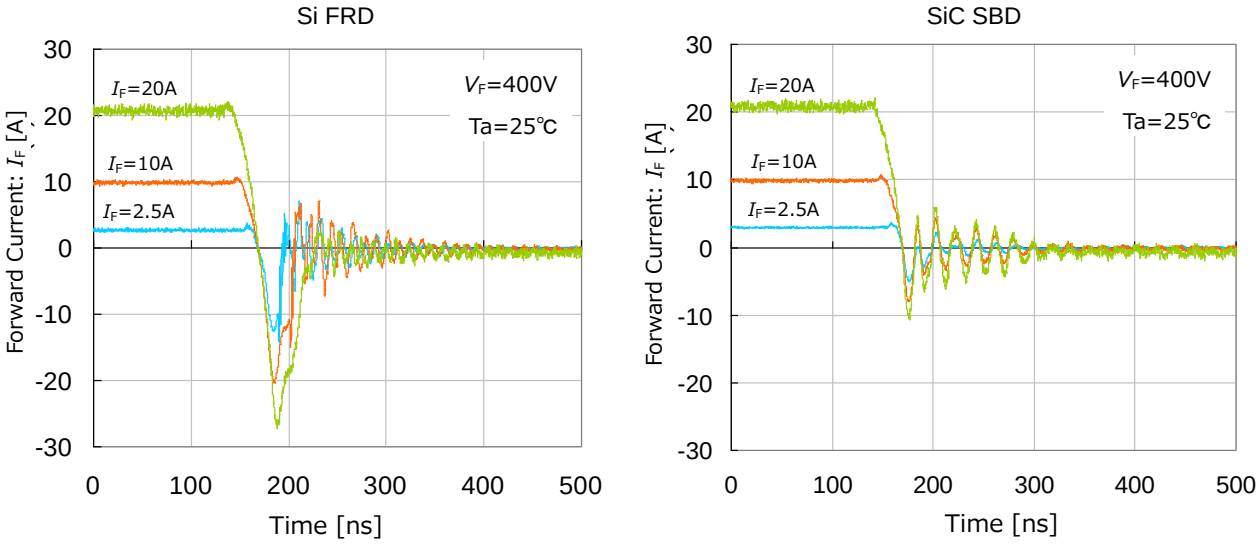
In Si-based high speed PN diodes (FRD: fast recovery diode), a large transient current flows momentarily when the direction switches from forward to backward, causing a large loss due to transition to the reverse bias state during this period. This is attributed to a contribution to electrical conduction by minority carriers that have been stored within the drift layer during a forward conduction until they disappear (storage time). The larger the forward current and the higher the temperature, the longer the recovery time and the larger the recovery current, resulting in a significant loss.

In contrast, since SiC SBD are majority carrier devices (unipolar devices), which do not use minority carriers for electrical conduction, no accumulation of minority carriers occurs in principle. Only a small current flows that is sufficient to discharge the junction capacitance, and the loss can be significantly reduced compared with Si FRD. Since this transient current is mostly independent of the temperature and the forward current, a stable and high speed recovery can be achieved in any environment. In addition, noise generated due to the recovery current is expected to be reduced.

Figure 2-3 shows the measurement results of the recovery characteristics of SiC SBD and Si FRD. It can be seen that the recovery current is significantly reduced with SiC, irrespective of the operating temperature and the flowing current.



(a) Temperature dependence



(b) Forward current dependence

Figure 2-3. Comparison of recovery characteristics (650 V, 10 A class)

2.4 Forward surge characteristics of SiC SBD

In the second generation SBD, a simple structure has been employed where Schottky metal is only attached to the drift layer, referred to as the pure Schottky structure. However, since the resistance value of the drift layer increases at a higher temperature, self-heating limits the current when the forward surge current flows, resulting in a trend that makes the peak surge current I_{FSM} smaller compared with Si FRD. In the PFC circuits without a bypass diode, the inrush current during startup and other situations may damage SBD.

Therefore, the JBS structure is employed in the third generation SBD, improving the I_{FSM} characteristics by approximately 2 times from the second generation. Since micro PN junction diodes are fabricated on the Schottky interface in the JBS structure, holes are injected via the PN junctions when a large current flows, reducing the increase in the resistance of the drift layer. Due to their high tolerance against the inrush current, they can be safely used in the PFC circuits without a bypass diode.

Figure 2-4 shows the structural difference between the second and third generations, and Table 2-1 shows the comparison of their typical electrical characteristics.

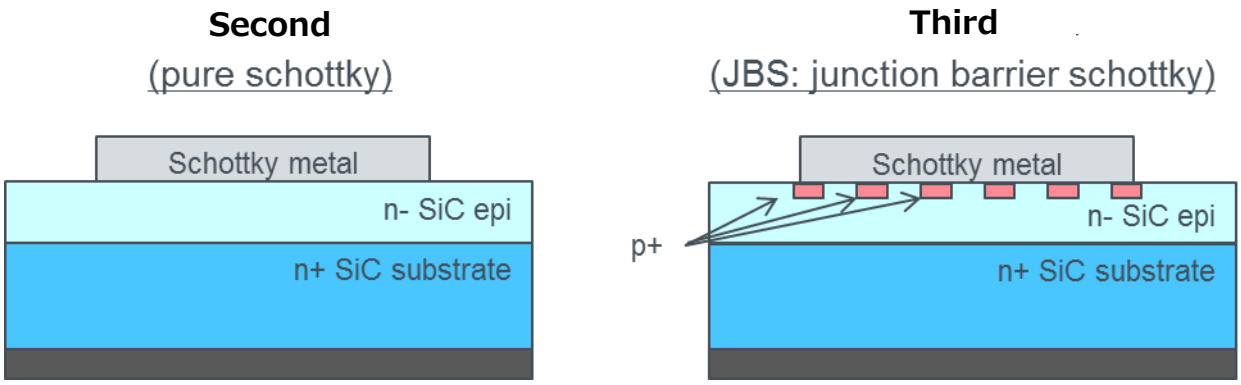


Figure 2-4. Structural comparison between the second and third generation SiC SBD

Table 2-1. Comparison of major electrical characteristics between the second and third generations

Item	Second generation SCS210AG	Third generation SCS310AH
V_F@10A (25C) typ.	1.35V	1.35V
V_F@10A (150C) typ.	1.55V	1.44V
I_R (25C) typ.	2μA@600V	0.03μA@650V
I_{FSM} 50Hz, 1 pulse	38A	82A

2.5 Precautions for using SiC SBD in series or parallel

When selecting power devices, there may not be a device with your desired rating depending on the voltage and current conditions. In such cases, multiple devices may be used. However, since there is always a variation in the characteristics among the devices, special care must be taken.

2.5.1 Series connection

If it is necessary to block voltage above the breakdown voltage of a device, multiple SBD might be connected in series. To equalize the voltage applied to each element, a balance resistor is generally connected in parallel between the anode and the cathode. However, for SBD, using a balance resistor as a countermeasure is not practical because the leak current IR in a reverse bias condition as well as its variation is large, as shown in Figure 2-5 (a).

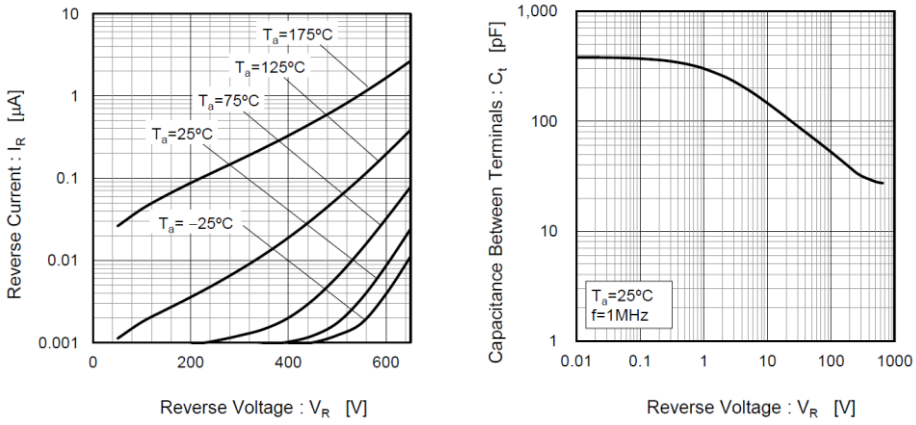
In addition, the terminal capacitance C_t shown in Figure 2-5 (b) varies significantly depending on the applied voltage. Therefore, in the transient state immediately after a reverse bias is applied, the voltage is unbalanced and may exceed the rating in some cases.

Based on the above, we basically do not recommend using multiple SBD connected in series.

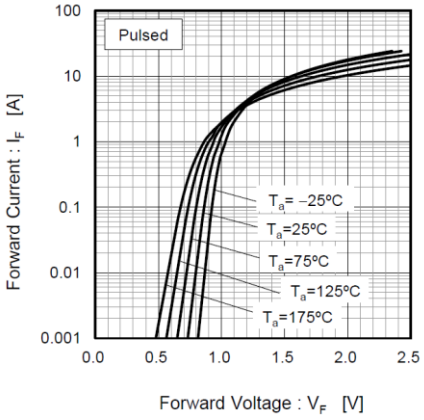
2.5.2 Parallel connection

If current to be passed through SBD exceeds the rating of a device, multiple SBD might be used in parallel. For SiC SBD, when the current increases, V_F increases as the device temperature increases as shown in Figure 2-5 (c). Therefore, the current is equilibrated rather than concentrated in a certain device.

Consequently, no additional circuit is required when multiple SBD are used in parallel. However, precautions must be taken, such as using devices from an identical lot and equalizing the wire inductance as much as possible.



(a) V_R-I_R characteristics (b) V_R-C_t characteristics



(c) V_F-I_F characteristics

Figure 2-5. Graphs of SCS306AM electrical characteristics (selected)

3. Features of SiC MOSFET

3.1 Device structure and features

With Si, the on-resistance per unit area increases with the breakdown voltage of a device (the on-resistance increases with the 2nd to 2.5th power of the breakdown voltage approximately). Therefore, IGBT (insulated gate bipolar transistors) are mainly used for a voltage of 600 V and higher. Compared with MOSFET, the on-resistance of the IGBT is reduced with conductivity modulation, in which holes (minority carriers) are injected into the drift layer. However, accumulation of the minority carriers generates a tail current at turn-off, resulting in a significant switching loss.

Since the resistance of the drift layer is lower for SiC compared with the Si devices, it is unnecessary to utilize the conductivity modulation. Therefore, a high breakdown voltage and low resistance can be simultaneously achieved in the MOSFET, which has a high speed device structure. In principle, the tail current will not be generated in the MOSFET. Therefore, replacing the IGBT with the MOSFET can significantly reduce the switching loss and downsize cooling structures such as a heat sink. The high frequency drive by the MOSFET can also contribute to downsizing of passive components, which is impossible with the IGBT. Furthermore, the SiC MOSFET also have advantages over the Si MOSFET in the range between 600 V and 900 V, such as smaller chip area (enabling mounting on smaller packages) and a very small recovery loss of the body diode.

Currently, the planar and trench type MOSFET with breakdown voltages of 650 V, 1,200 V, and 1,700 V are listed in ROHM's lineup. Their applications extend to various uses, including onboard chargers, power supplies for industrial equipment, and inverter and converter sections of high efficiency power conditioners.

Figure 3-1 shows a comparison between Si and SiC for the rated voltage ranges of the MOSFET and IGBT.

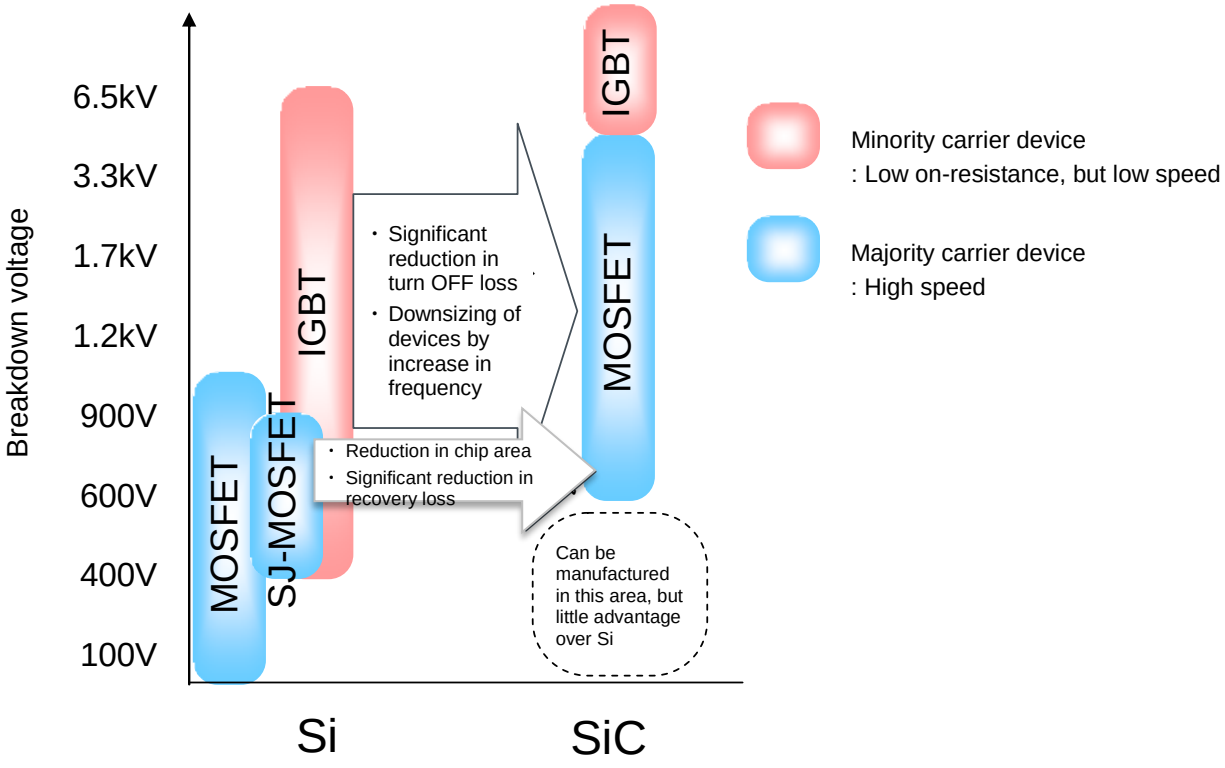


Figure 3-1. Rated voltage range for Si and SiC (MOSFET and IGBT)

3.2 Standardized on-resistance (RonA)

Since the dielectric breakdown field strength of SiC is approximately 10 times higher than that of Si, high breakdown voltage can be achieved with a drift layer having a low specific resistance and a thin film thickness. Therefore, compared at the same breakdown voltage, a device with a smaller standardized on-resistance (RonA: on-resistance per unit area) can be manufactured. As shown in Figure 3-2, when compared at the breakdown voltage of 900 V, for example, the SiC MOSFET can realize the same on-resistance with a chip size approximately 1/100 and 1/10 of that of the Si MOSFET and the super junction (SJ) MOSFET, respectively. This enables a reduction of the on-resistance with a smaller package as well as the gate charge Qg and the capacitance.

For the super junction MOSFET, the breakdown voltage of existing products is only up to 900 V currently. For the SiC MOSFET, however, a breakdown voltage over 1,700 V can be achieved with a low on-resistance. Since the bipolar device structure (having a low on-resistance, but a slow switching) like the IGBT is unnecessary, a device that has a low on-resistance, high breakdown voltage, and high speed switching simultaneously can be realized with the SiC MOSFET.

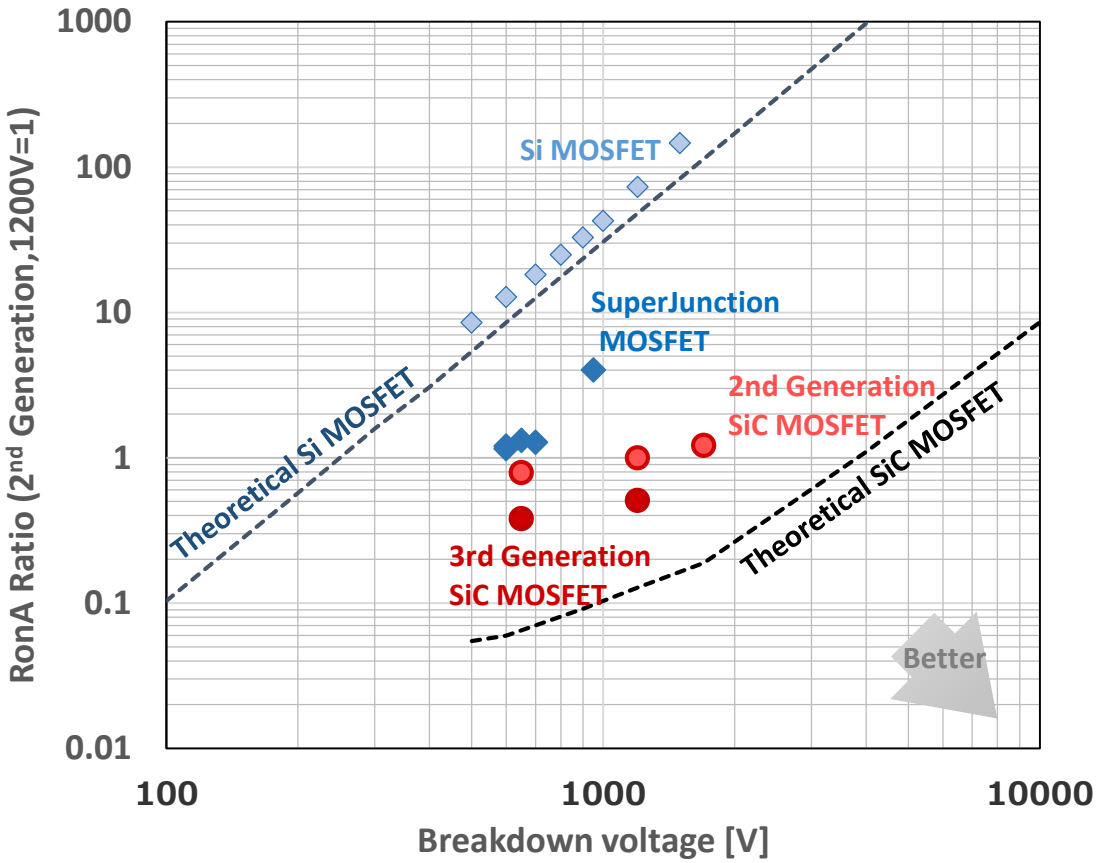
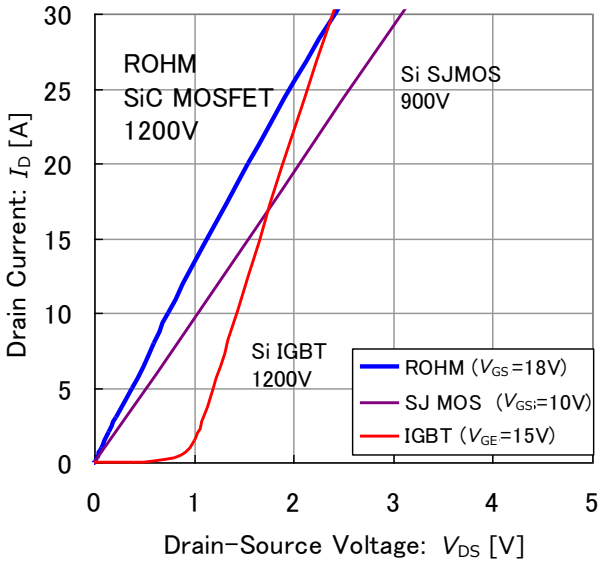


Figure 3-2. Comparison of RonA

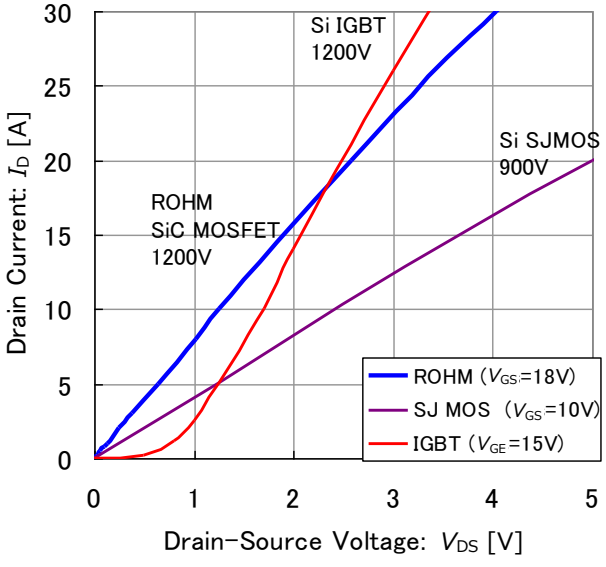
3.3 V_{DS}-I_D characteristics

Since there is no rising voltage like the IGBT, the SiC MOSFET can realize a low conduction loss in a wide current region from small to large current.

Furthermore, although the on-resistance of the Si MOSFET is increased by two times or more at 150°C from room temperature, a relatively low increase rate makes thermal design easier with the SiC MOSFET, and a low on-resistance can be realized even at high temperature. Figure 3-3 shows the V_{DS}-I_D characteristics of each device at ordinary and high temperatures.



(a) Ta=25℃



(b) Ta=150℃

Figure 3-3. V_{DS}-I_D characteristics

3.4 Driving gate voltage and on-resistance

The drift layer resistance of the SiC MOSFET is lower than that of the Si MOSFET. However, since the mobility in the MOS channel part is limited by the current level of technology, the resistance in the channel part is higher compared with the Si devices. Therefore, a lower on-resistance can be obtained with a higher gate voltage (gradually saturated over V_{GS} = 20 V).

As can be seen from the V_{GS}-$R_{DS(on)}$ characteristics in Figure 3-4, the SiC MOSFET cannot exhibit the original performance regarding the low on-resistance if the driving voltage V_{GS} = 10 to 15 V, which is the range used for the general IGBT and Si MOSFET. Therefore, we recommend driving the SiC MOSFET around V_{GS} = 18 V in order to obtain a sufficiently low on-resistance.

In addition, the on-resistance tends to decrease at higher temperature if V_{GS} = 13 V or less. When the SiC MOSFET are connected in parallel, it is possible that the current is concentrated in a single element and causes thermal runaway. Therefore, be careful not to drive the SiC MOSFET with V_{GS} = 13 V or less.

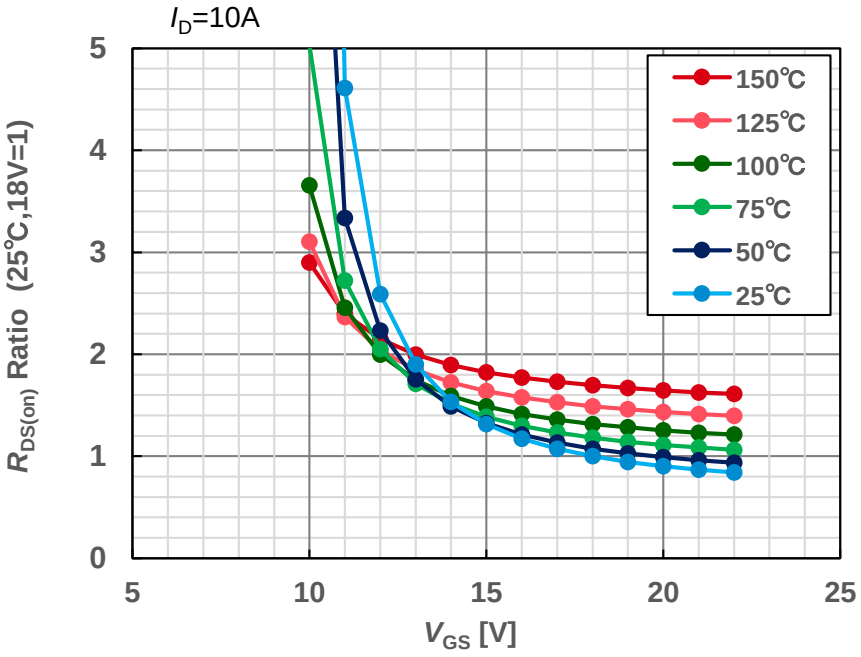


Figure 3-4. V_{GS}-$R_{DS(on)}$ characteristics

3.5 Temperature coefficient of on-resistance

The on-resistance of the general Si high breakdown voltage MOSFET significantly increases at high temperature. The reason for this increase is as follows: the resistance of the drift layer (R_{EPI}), which accounts for 90% or more of the on-resistance of a device, tends to increase by approximately two times when temperature is increased by 100°C.

As with the trend for Si, the resistance of the drift layer for SiC also increases approximately two times when temperature is increased by 100°C. However, the increase rate of the on-resistance of a whole device is lower compared with the Si MOSFET (Figure 3-5). This is because the drift layer accounts for a small proportion of the on-resistance of the SiC device and many other resistance components are contained in the on-resistance. The channel resistance R_{CH} slightly decreases at high temperature, while the resistance of the n+ board R_{SUB} shows almost no temperature dependence.

Furthermore, among the SiC MOSFET, the temperature coefficient of the on-resistance depends on the breakdown voltage and the device design. In the 650 V products, the temperature coefficient is very small because the resistance component of the drift layer is small. In the 1,200 V products, however, the temperature coefficient is larger because the drift layer is thick and its resistance component is large. Even among SiC products with the same breakdown voltage, the actual value of the breakdown voltage and the reliability is higher in the products with a thicker drift layer, while the temperature coefficient of the on-resistance is larger (Figure 3-6).

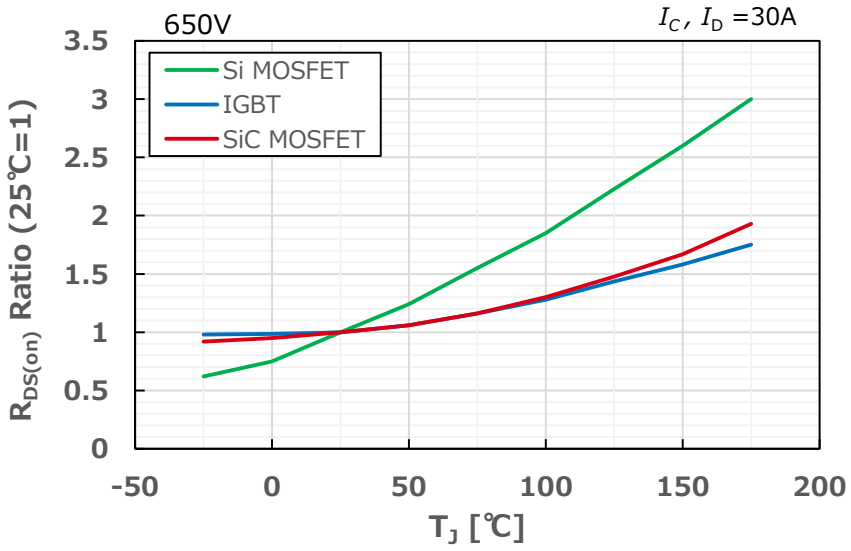


Figure 3-5. Temperature characteristics of standardized $R_{DS(on)}$ of 650 V SiC MOSFET, Si MOSFET, and Si IGBT

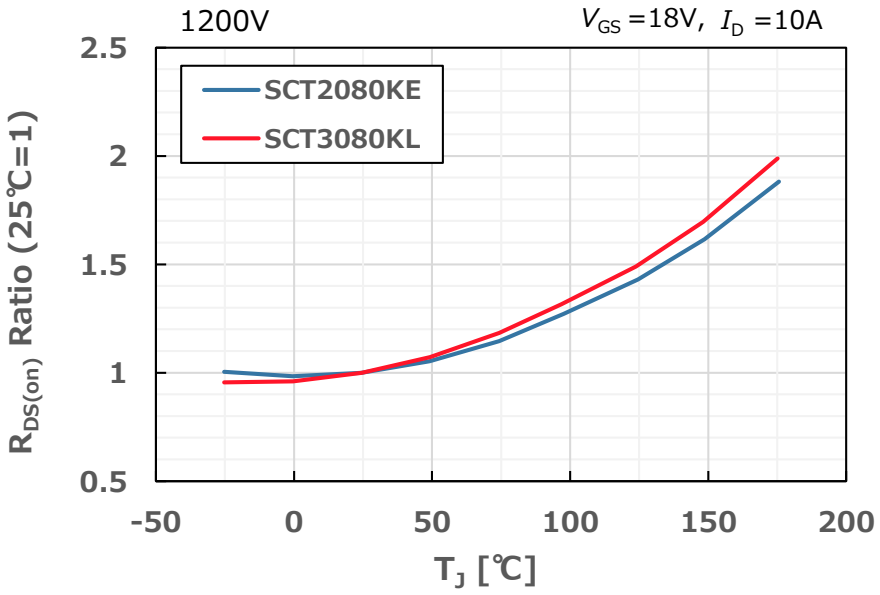


Figure 3-6. Temperature characteristics of standardized $R_{DS(on)}$ of 1,200 V SiC MOSFET (second and third generations)

3.6 V_{GS}-I_D characteristics

Figure 3-7 shows the V_{GS}-I_D characteristics. The left and right graphs show the same data plotted with the vertical axes in the logarithmic and linear scales, respectively. When defined at a few mA, the threshold voltage for the SiC MOSFET is similar to that of the Si MOSFET, approximately 3 V at room temperature (normally OFF). However, since the gate voltage required to pass a few ampere is approximately 8 V or greater at room temperature, the tolerance against self-turn-on can be considered equivalent to that of the IGBT. The threshold voltage tends to decrease at higher temperature. As can be seen from the graphs, even at Ta = 150°C, a current of 5 A or greater will not flow until V_{GS} = 6 V or higher.

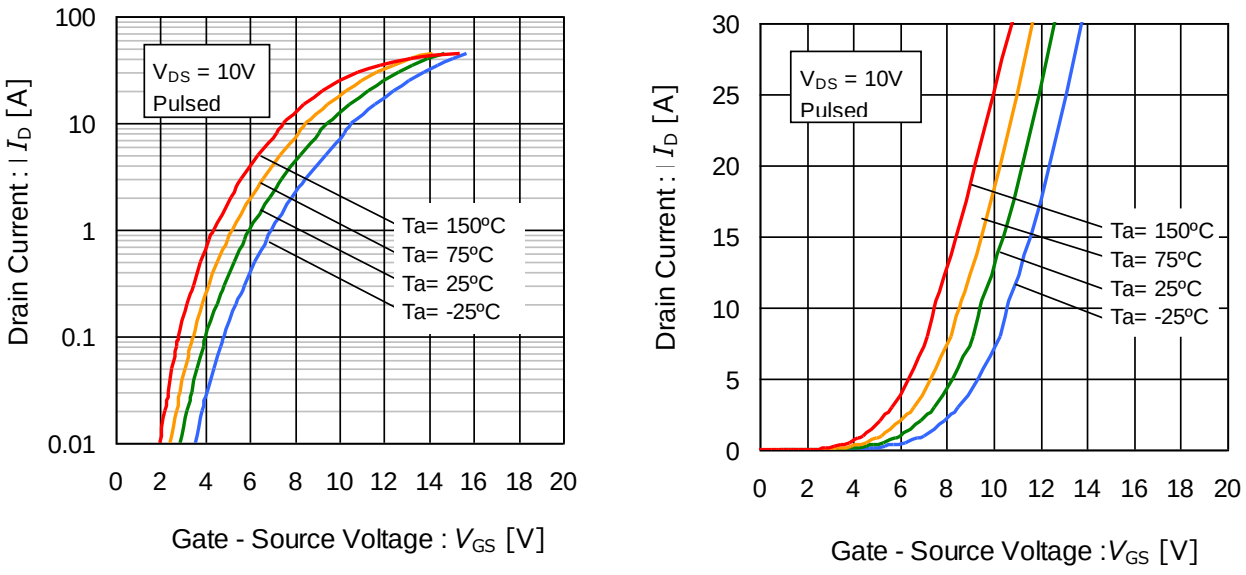


Figure 3-7. V_{GS}-I_D characteristics (SCT2080KE)

Figure 3-8 shows a comparison of V_{GS}(V_{GE})-I_D(I_C) characteristics of the SiC MOSFET and IGBT. It can be seen that although $V_{GS(th)}$ of the SiC MOSFET is lower at I_D(I_C) = 10 mA, it exceeds that of the IGBT at 5 A or greater.

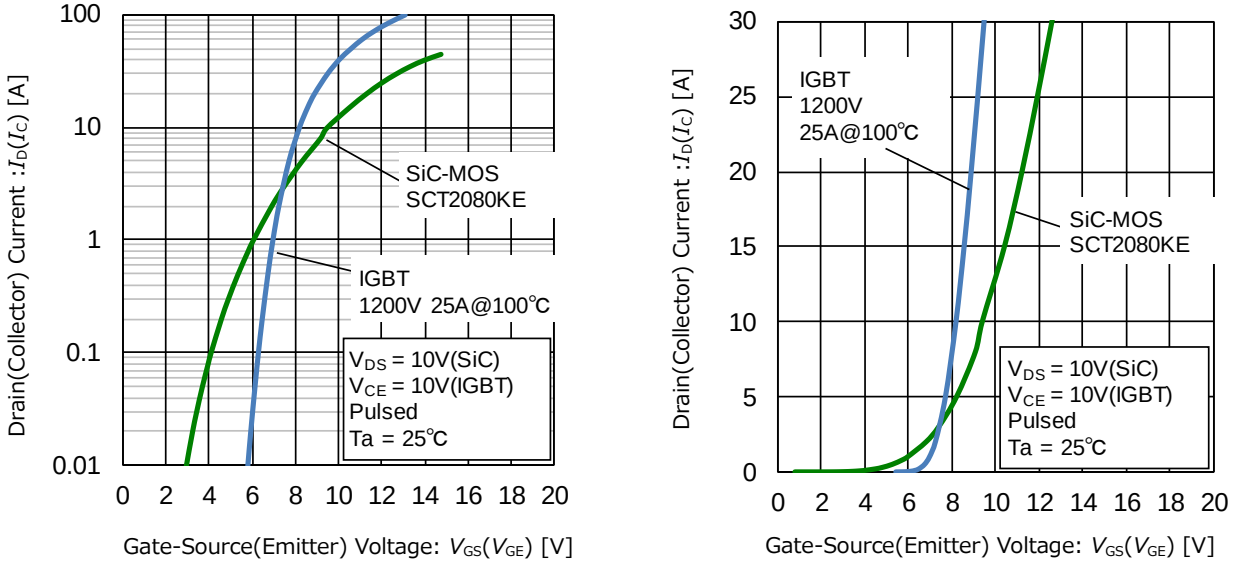


Figure 3-8. V_{GS}(V_{GE})-I_D(I_C) characteristics (SiC MOSFET vs. IGBT)

3.7 Turn ON characteristics

SCH2080KE, where the SiC-MOSFET and SiC-SBD are mounted on the same package, and a product where the Si-IGBT and Si-FRD of equivalent classes are mounted on the same package are used to configure each half bridge circuit. Then, the switching waveforms are compared using the inductive load double pulse test (DPT). Figure 3-9 shows the test circuit.

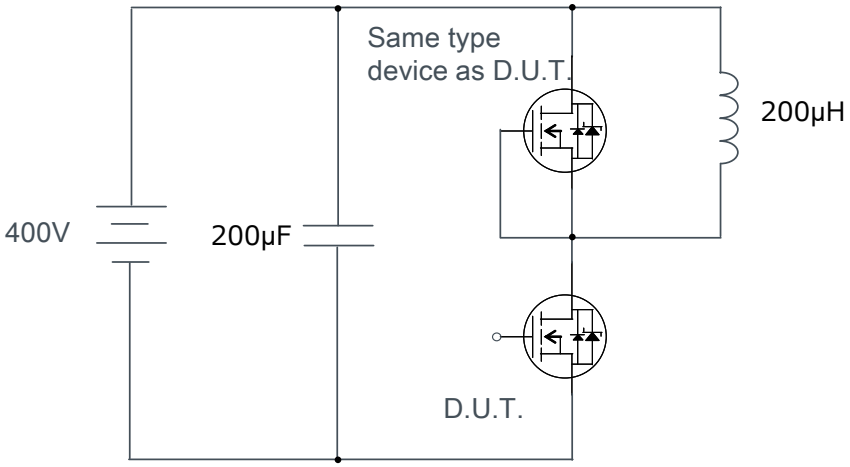


Figure 3-9. Double pulse test circuit

The turn ON speed of the SiC MOSFET is several tens of nanoseconds, similar to the Si IGBT and Si MOSFET. However, in the case of inductive load switching, a recovery current generated due to commutation to the diode of the upper arm penetrates and flows to the lower arm as well. Therefore, a significant loss is added depending on the performance of the diode. (Figure 3-10)

The body diode of the Si FRD or the Si MOSFET generally has a very large recovery current and generates a significant loss. In addition, this loss tends to increase further at high temperature. In contrast, high speed recovery is possible with the SiC SBD independently of temperature. The body diode of the SiC MOSFET also shows a high speed performance similar to the SiC SBD, although V_F is high. Such high speed recovery performance can reduce the turn ON loss (Eon) by several tens of percent.

The switching speed depends strongly on the external gate resistance R_{G_EXT}. To achieve high speed operation, a low gate resistance around a few ohms is recommended. Select an appropriate gate resistance with consideration for the surge voltage.

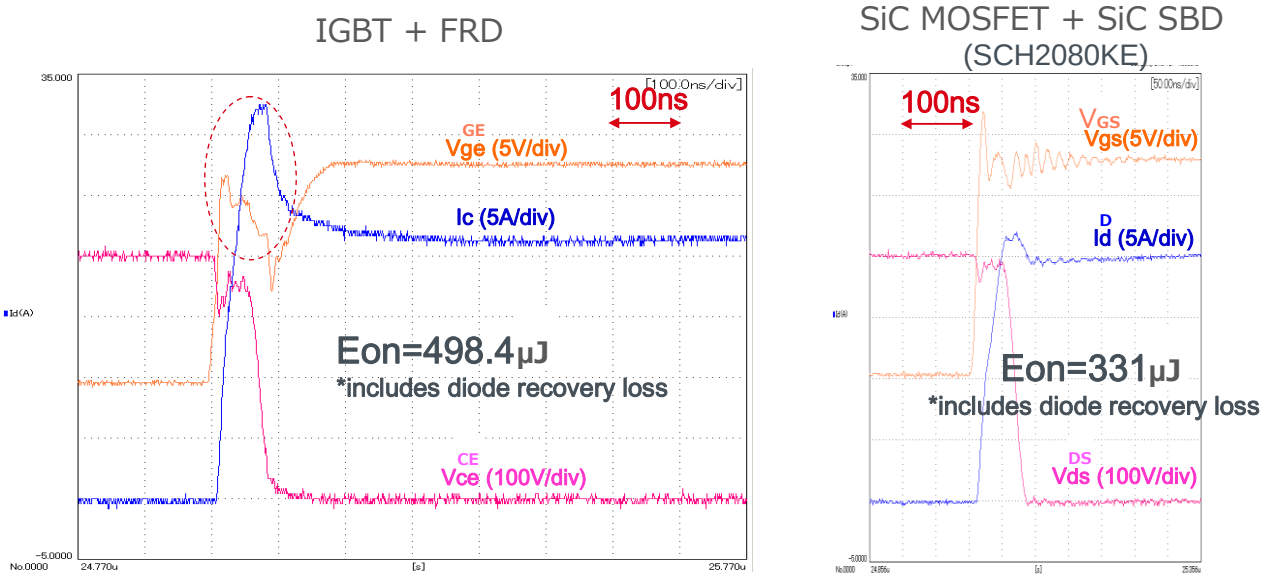


Figure 3-10. DPT turn ON waveforms

3.8 Turn OFF characteristics

The most notable feature of the SiC MOSFET is that the tail current, which is observed in the IGBT, is not generated in principle. With SiC, the high speed MOSFET structure can be manufactured even at a breakdown voltage of 1,200 V or greater. Therefore, reduction in the turn OFF loss (Eoff) by approximately 90% compared with the IGBT (Figure 3-11) can be achieved, contributing to energy conservation of the circuit as well as simplification and downsizing of the cooling mechanism. While the tail current in the IGBT increases at higher temperature, almost no temperature dependence exists in the MOSFET.

Furthermore, the IGBT cannot usually be used at a high frequency region above 20 kHz because the junction temperature (Tj) exceeds the rating due to heat generated with a large switching loss. However, since Eoff is small, the SiC MOSFET can perform high speed switching operation at 50 kHz or higher. Operating at higher frequency enables downsizing of passive components including transformers and filters. (Figure 3-12)

The switching speed depends strongly on the external gate resistance R_{G_EXT}. To achieve high speed operation, a low gate resistance around a few ohms is recommended. Select an appropriate gate resistance with consideration for the surge voltage.

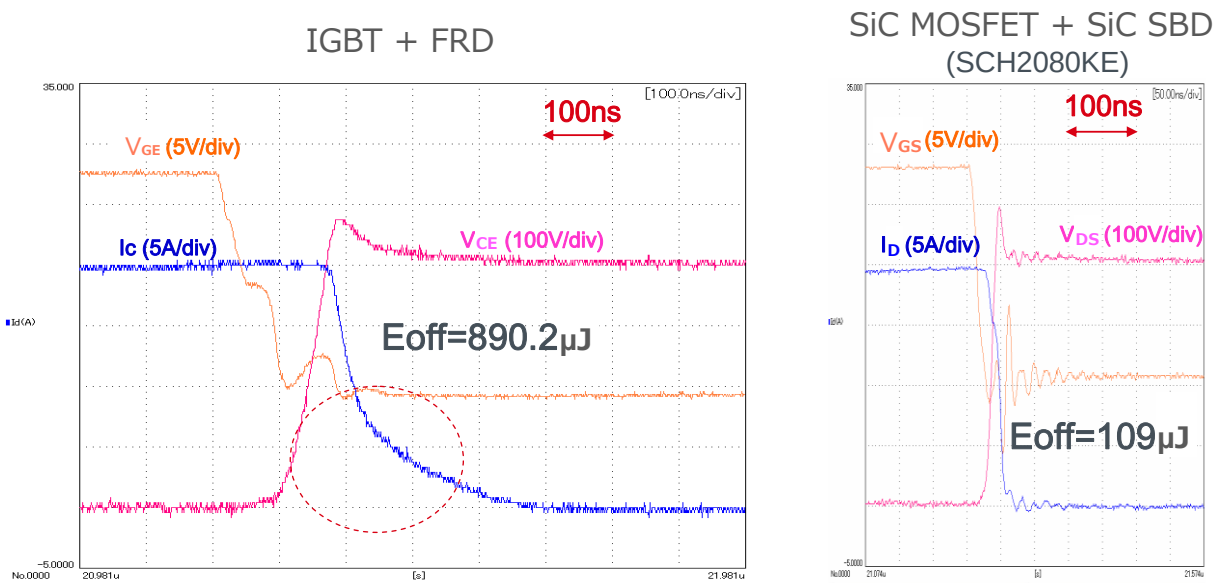
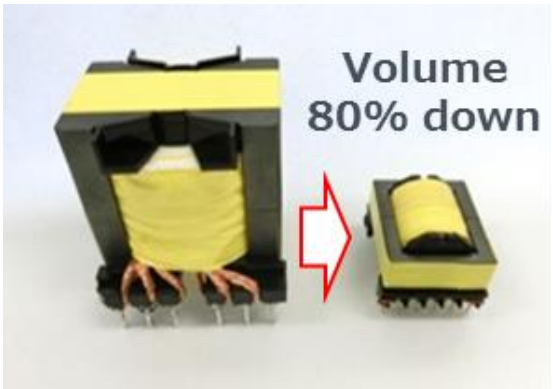


Figure 3-11. DPT turn OFF waveform



(a) 20 kHz (b) 160 kHz

Figure 3-12. Example of downsizing of transformer with high frequency operation

3.9 Internal gate resistance

The chip internal gate resistance depends on the sheet resistance of the gate electrode material and the chip size. If the design is common, the gate resistance is inversely proportional to the chip size: the smaller the chip, the higher the gate resistance. The chip size of a SiC MOSFET is smaller compared with the Si devices. This makes the capacity smaller, while making the gate resistance higher. The internal gate resistance is 6.3Ω and 12Ω for the 1,200 V 80mΩ products in the second and third generations, respectively.

The switching time depends strongly on the external gate resistance. Figure 3-13 shows the relation between the external gate resistance and the switching loss. Since the loss increases if the gate resistance is increased, in order to achieve high speed switching, use an external gate resistance as low as possible around a few ohms while checking the surge condition.

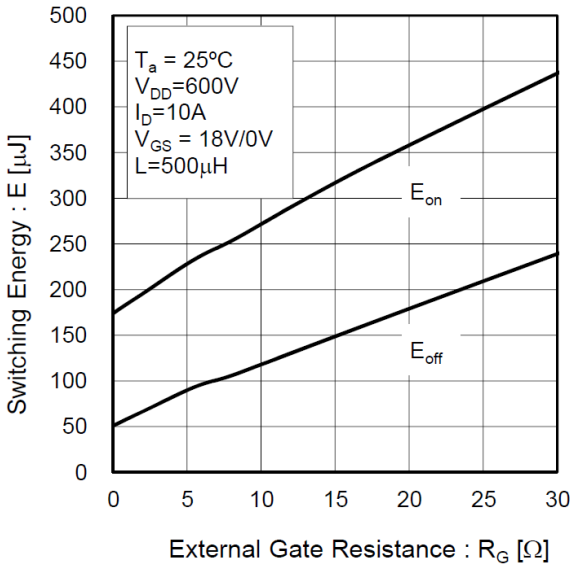


Figure 3-13. Dependence of switching loss on external gate resistance

3.10 Recovery characteristics of body diode

Although the body diode of the SiC MOSFET is a pn diode, the storage effect of minority carriers is scarcely observed due to a short lifetime for the minority carriers, and a very high speed recovery performance (several tens of nanoseconds) similar to the SBD is obtained. As a result, the recovery loss can be reduced to a fraction or several tenths of that of the body diode of the Si MOSFET or the external FRD of the IGBT.

As is the case with the SBD, the recovery time of the body diode is independent of the forward injection current I_F. In addition, as shown in Figure 3-14, comparison between the body diode of the SiC MOSFET (SCT2080KE) and the SiC SBD (SCH2080KE) indicates no difference in the recovery current if d*I*/d*t* is constant. In bridge applications including inverters, a bridge circuit configured only with the MOSFET can achieve a very small recovery loss. At the same time, the risk of failure and noise generated due to the recovery current can be expected to be reduced.

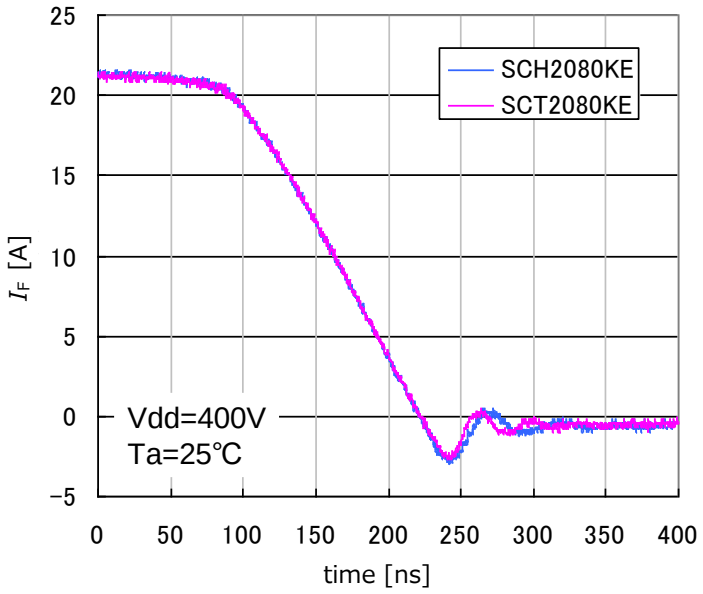


Figure 3-14. Reverse recovery characteristics

(a) SCH2080KE: SiC SBD combined type, (b) SCT2080KE: SiC MOSFET only (body diode)

3.11 Temperature dependence of BV (breakdown voltage)

BV of the SiC MOSFET also increases with temperature as in the case with the Si MOSFET. If the device is used at low temperature, the BV value decreases compared with room temperature. However, since ROHM's SiC MOSFET are designed with a sufficient margin, the BV value will not fall below the rated voltage even at low temperature.

Figure 3-15 shows general temperature dependent characteristics of BV.

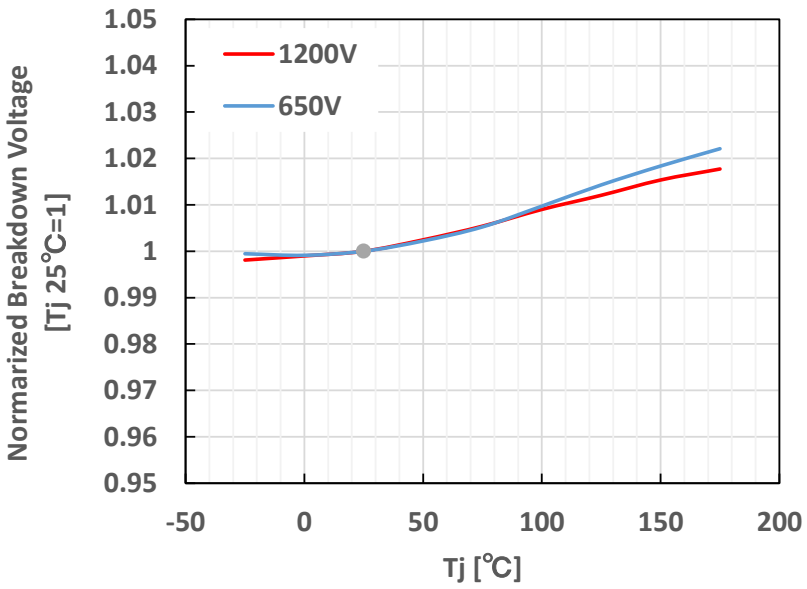


Figure 3-15. Temperature dependent characteristics of BV

3.12 1700 V SiC MOSFET for flyback

As shown in Figure 3-16, the SiC MOSFET with the breakdown voltage of 1,700 V can gain a significant advantage in performance over the Si MOSFET: RonA is 1/200 of that of the Si MOSFET. Therefore, a low on-resistance 1/10 of that of the Si MOSFET can be achieved with a chip size of less than 1/10. By replacing the 1,500 V Si MOSFET (around 10Ω) commonly used for auxiliary power supplies (flyback converters) for industrial equipment with the AC input of 200 to 400 V with a low on-resistance SiC MOSFET (around 1Ω), the heatsink can be eliminated with reduced heat generation and the mounting can be automated with surface mounting devices, realizing downsizing, reduced heat generation, and simplification of the mounting process without increasing the total cost. ROHM also proposes flyback controller IC dedicated for SiC as well as combined products of the SiC MOSFET and controller IC.

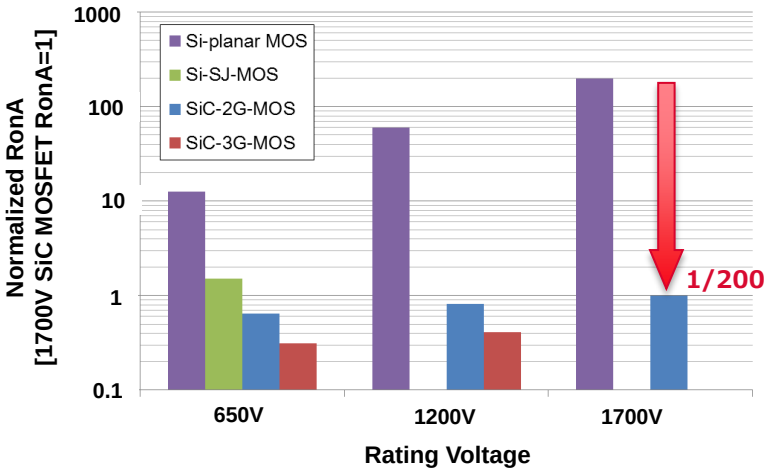


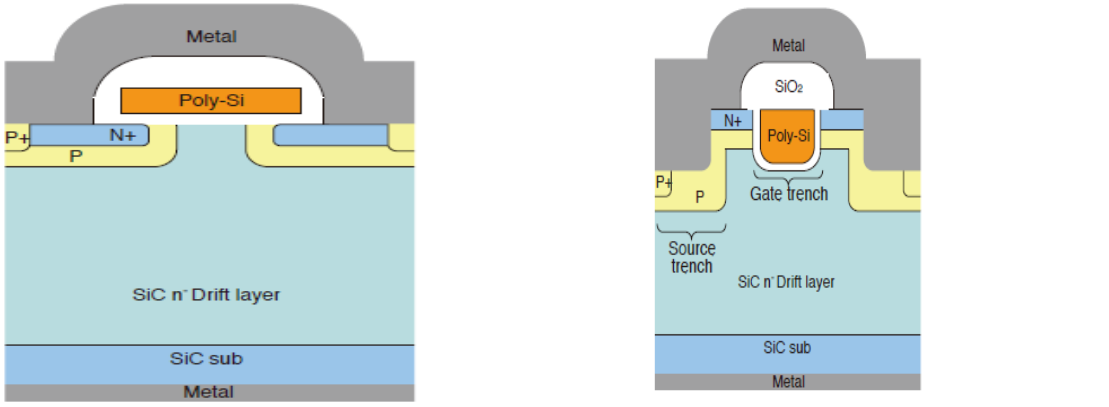
Figure 3-16. Comparison of RonA at each breakdown voltage

3.13 Third generation trench gate SiC MOSFET

The third generation SiC MOSFET employ the trench gate structure (Figure 3-17). The cell pitch has been decreased to reduce the channel resistance. In addition, a resistance component due to narrowness of the current path between p-well (referred to as the JFET resistance) is also eliminated. These measures have successfully reduced RonA by half compared with the second generation. Table 3-1 shows a list of comparisons of the main characteristics between the second and third generation MOSFET. Since the same on-resistance is obtained with a smaller chip area, the cost can be reduced.

With a general SiC trench gate MOSFET structure, it is difficult to ensure the long term reliability because the gate oxide film at the bottom of the gate trench is exposed to a high electric field when the device is turned OFF. However, ROHM has solved this issue by employing a unique double-trench structure. By constructing another trench structure in the source part and forming the p-type layer at the bottom, the field strength applied to the gate oxide film when the device is turned OFF has been successfully reduced by 35% and the long term reliability can be achieved.

Since the rating of the gate voltage is narrow in the third generation MOSFET, refer to countermeasures against gate surge in Chapter 5 and use the device within the rating.



(a) Planar type (second generation) (b) Trench type (third generation)

Figure 3-17. Structures of second and third generation devices

Table 3-1. Comparison of various characteristics between second and third generation devices (selected from data sheet)

Device		**Second** SCT2080KE	**Third** SCT3040KL	
Package		TO247	TO247	
Tjmax		175°C	175°C	
Pd Tc=25°C		262W	262W	
Id Tc=25°C		40A	55A	
Vgs		-6 ~ 22V	-4 ~ 22V	
Ron	Tj=25°C	80 mΩ	40 mΩ	Ron ↓50%
	Tj=125°C	125 mΩ	62 mΩ	
Eon	Vdd=800V Id=20A	760uJ	550uJ	Esw ↓30%
Eoff		120uJ	90uJ	
Ciss/Coss/Crss		2080 / 77 / 16 (pF)	1337 / 76 / 27 (pF)	Ciss ↓35%
Qg		106 nC	107 nC	
Rg		6.3Ω	7Ω	

3.14 Temperature dependence of switching characteristics

While the switching speed depends strongly on the parasitic capacitance of the device, the parasitic capacitance of the SiC MOSFET shows little change against temperature and the temperature characteristics of the switching loss are extremely stable. As shown in Figure 3-18, the characteristics of the switching loss are nearly flat from 25°C to 175°C. Figure 3-19 shows the temperature characteristics of SCT3040KL (a) Ciss, (b) Crss, and (c) Coss. It can be seen that every component is stable against temperature.

V_{DS}= 600V , I_D= 20A , R_{G_EXT}= 0Ω

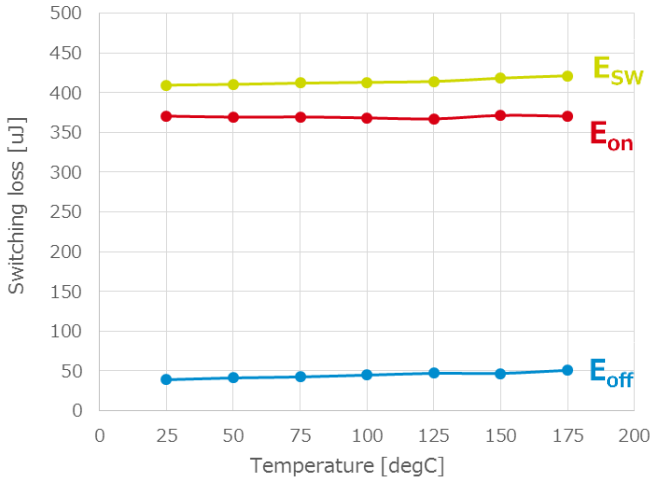
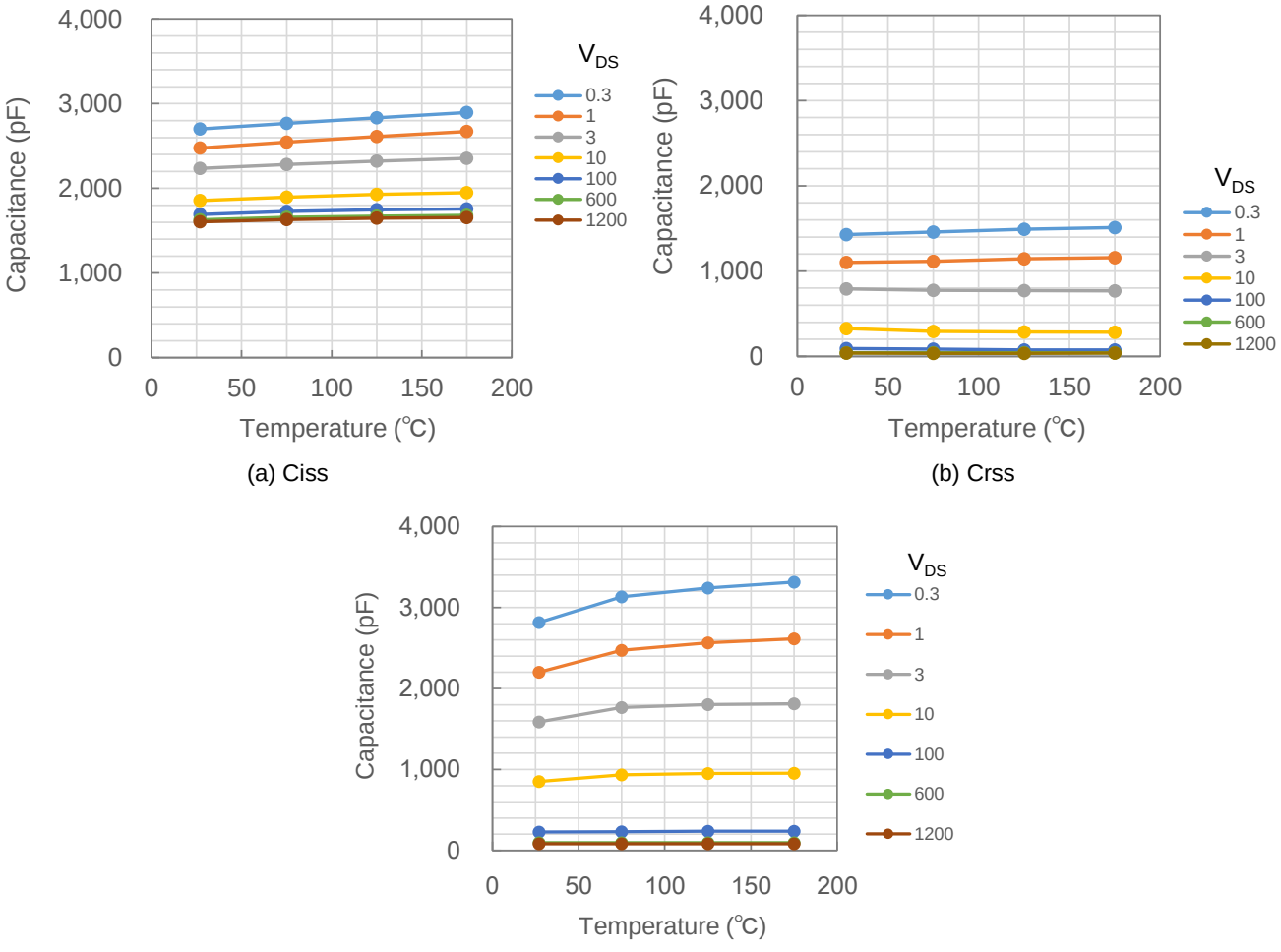


Figure 3-18. Temperature dependence of switching loss (SCT3040KL)



(a) Ciss

(b) Crss

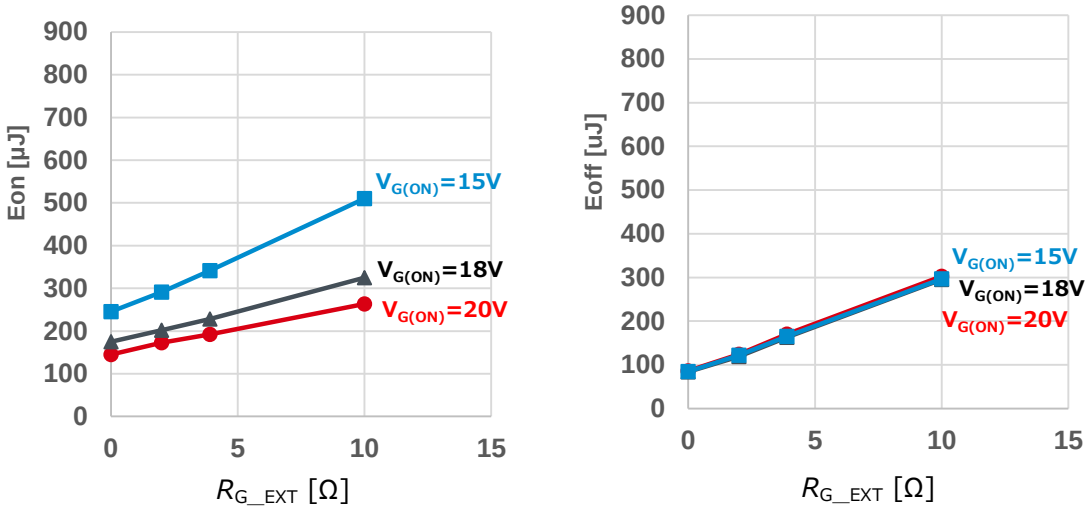
(c) Coss

Figure 3-19. Temperature dependence of Ciss, Crss, and Coss (SCT3040KL)

3.15 Gate voltage dependence of switching characteristics

Figure 3-20 shows the difference in the switching loss due to the gate drive voltage. The switching loss when the device is turned ON (Eon) decreases as the driving supply voltage $V_{G(ON)}$ increases. Eon at 18 V is reduced by 1.5 times compared with 15 V. This is because the gate current increases as the potential difference between $V_{G(ON)}$ and the plateau voltage increases, accelerating the discharge of Crss, i.e., the decline of the drain voltage.

In contrast, the switching loss when the device is turned OFF (Eoff) shows little variation with $V_{G(ON)}$. When the device is turned OFF, since the gate current charging Crss is determined by the potential difference between the plateau voltage and the gate OFF voltage (0 V in this case), $V_{G(ON)}$ is basically unrelated to Eoff.

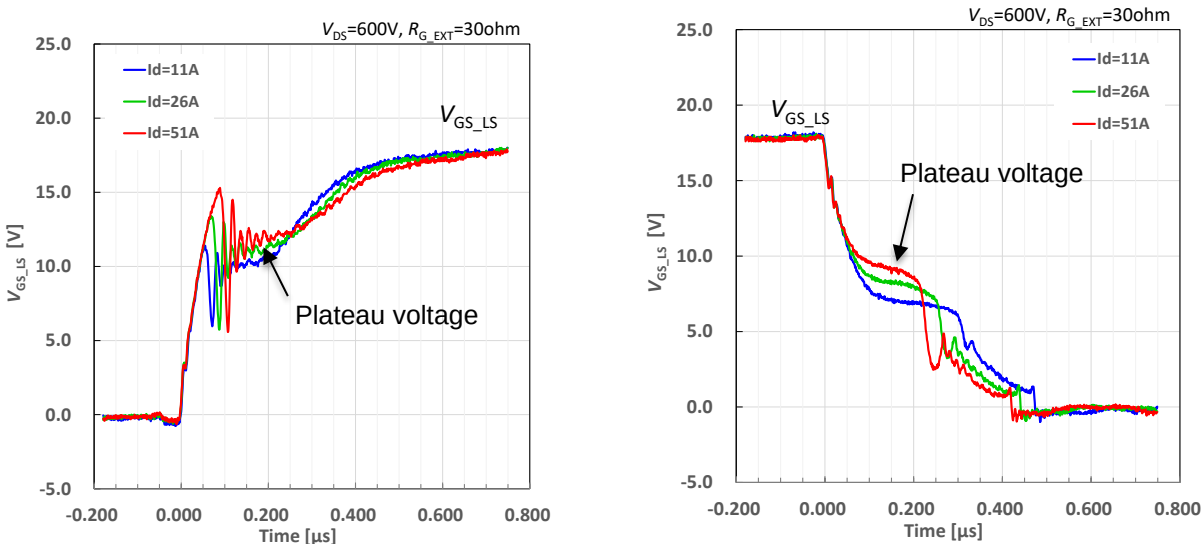


(a) Eon (b) Eoff

Figure 3-20. $V_{G(ON)}$ dependence of switching loss

3.16 Drain current dependence of switching speed

Figure 3-21 shows the behavior of the gate-source voltage V_{GS} with different drain current I_D. Whether the device is turned ON or OFF, the plateau voltage tends to increase as I_D increases. Therefore, when I_D increases, the turn ON speed decreases and the turn OFF speed increases.

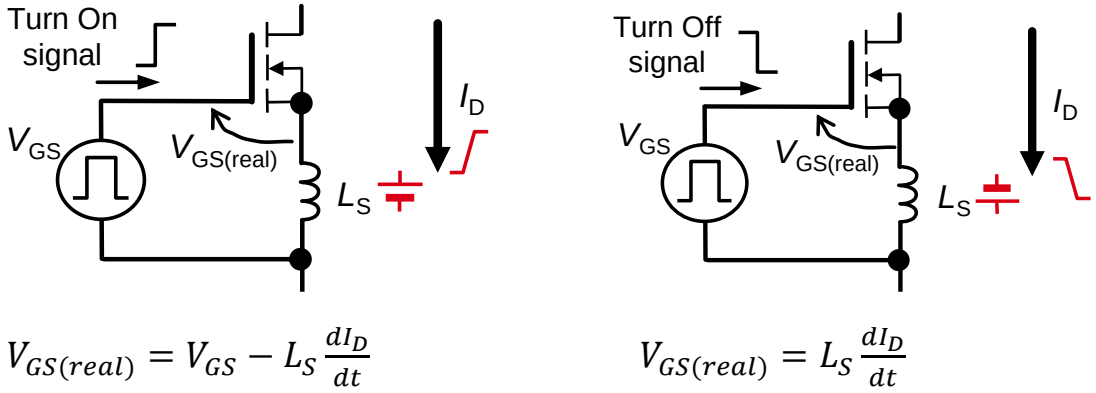


(a) Turn on (b) Turn off

Figure 3-21. Comparison of gate-source voltage for each I_D

3.17 Effect of parasitic inductance on switching characteristics

The 3-pin type packages such as TO-247N use a common source terminal for the gate drive circuit and the main circuit where the drain current flows. Therefore, the parasitic inductance caused by the source terminal (Ls) generates induced voltage due to variation in I_D during switching, adversely affecting the gate drive circuit. Figure 3-22 shows this mechanism. When the device is turned ON, the drain current I_D increases. The voltage generated due to this dI_D/dt ($L_S \cdot dI_D/dt$) reduces the effective voltage applied across G-S ($V_{GS(real)}$), reducing the switching speed. Since I_D decreases when the device is turned OFF, a voltage with reversed polarity relative to the polarity during the turn ON is generated in L_S, preventing the turn OFF operation.



$$V_{GS(real)} = V_{GS} - L_S \frac{dI_D}{dt}$$

(a) During turn ON, I_D increases

$$V_{GS(real)} = L_S \frac{dI_D}{dt}$$

(b) During turn OFF, I_D decreases

Figure 3-22. V_{GS} due to effect of source inductance

The common inductance for the source (Ls) can be generated not only in the source terminal of the 3-pin package and the internal wire bonding, but also in the wiring layout on the PCB.

Figure 3-23 shows an example of the adverse effect when the return line is shared between the main and drive circuits on the PCB. While the return line is partially shared with the main circuit in layout A, it is completely separated from the soldering part of the terminal in layout B. It is found that the rise of V_{GS} is smaller and the rise rate of I_D is slower in layout A. It is important to draw the return line of the drive circuit in such a way that the return line is separated from the main circuit starting from the lead terminal part of the MOSFET.

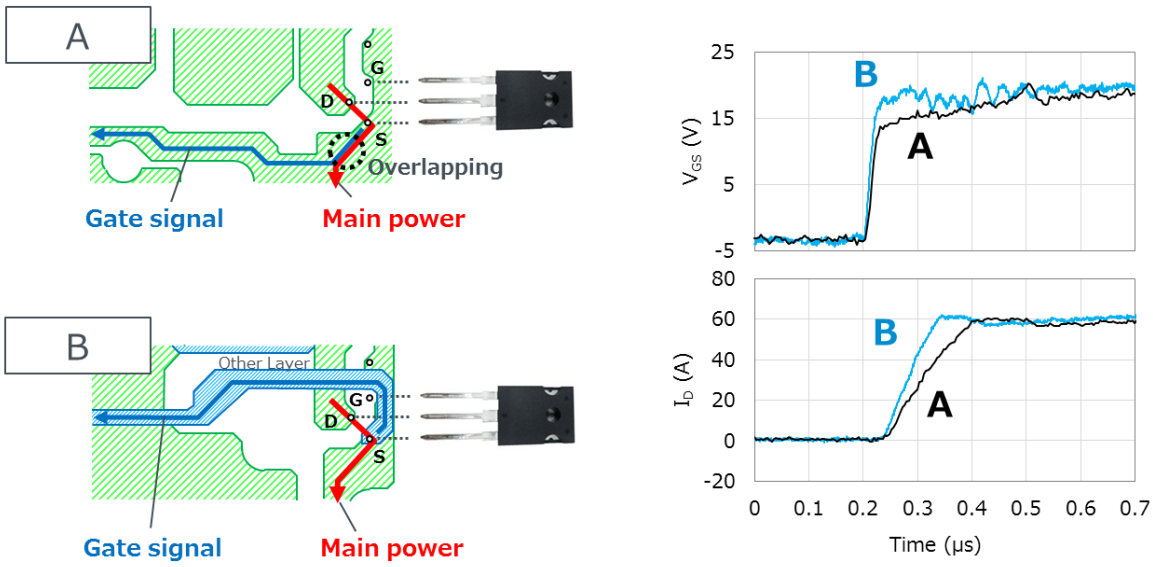


Figure 3-23. Effect of layout of gate drive circuit on switching waveforms

(A) Shared return, (B) Separated return

3.18 Kelvin source package

To eliminate the effect of the induced voltage generated in the source terminal on the switching speed as described in Section 3.17, packages equipped with the Kelvin source (driver source) terminal have been developed. At ROHM, the TO-247-4L (4-lead) package has been productized. Its external view and internal equivalent circuit are shown in Figures 3-24 and 3-25, respectively.

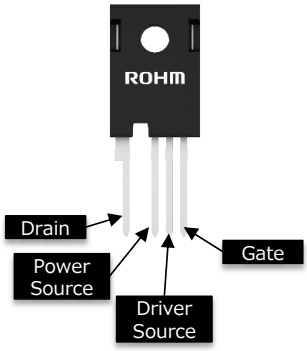


Figure 3-24. External view of package equipped with Kelvin source terminal

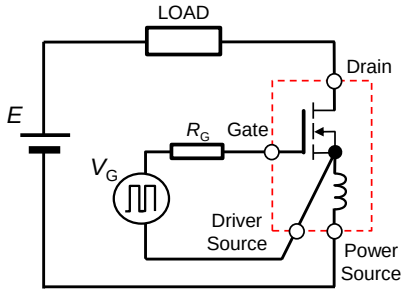
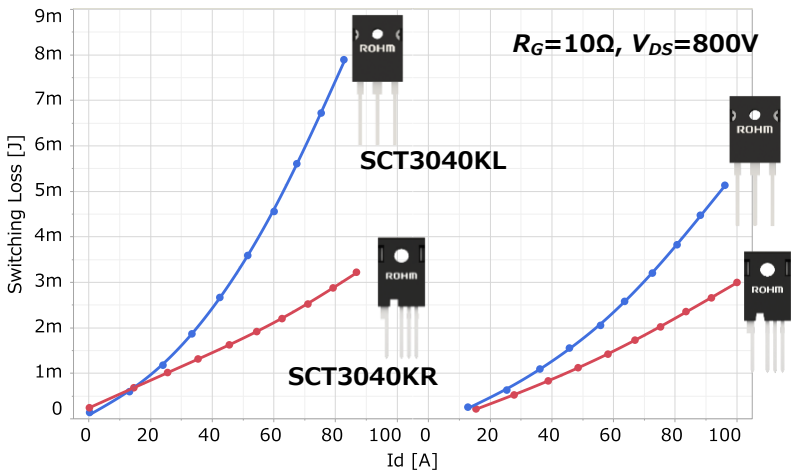


Figure 3-25. Drive circuit using Kelvin connection

In this package, a driver source terminal is provided that is connected with the surface electrode of the MOSFET chip using a separate wire from the main circuit source. As a result, the drive circuit will not be affected even if the parasitic inductance of the main circuit generates induced voltage due to the current variation. Therefore, the switching loss can be significantly improved. Figure 3-26 shows the result of DPT comparing the switching losses between TO-247N (3-lead) and TO-247-4L (4-lead). They differ only the packages and the same chip is used for both of them. It is found that the presence of the driver source terminal improves both the turn ON and turn OFF losses further as I_D is larger.



(a) Eon (b) Eoff

Figure 3-26. Comparison of switching losses (TO-247N vs. TO-247-4L)

4. Evaluation board for discrete SiC MOSFET

4.1 Evaluation board for SiC MOSFET (discrete)

Table 4-1 shows a list of evaluation boards released by ROHM for the SiC MOSFET (discrete). The half bridge structure is employed to evaluate the switching characteristics. Evaluations of the buck and boost topologies, including the double pulse test, can be performed with the minimum number of external components. The switching speed can be adjusted and the driving voltage can be changed. The gate surge protection circuit is also installed.

For more detailed information, refer to the SiC support page on ROHM's website (https://www.rohm.co.jp/power-device-support).

Table 4-1. List of evaluation boards for SiC MOSFET (discrete)

Device under evaluation	External design	Product name
TO-247N/TO-247-4L For third generation SCT3xxxxxxx series		P02SCT3040KR-EVK-001
TO-263-7L For third generation SCT3xxxxxW7 series		P03SCT3030AW7-EVK-001 P03SCT3040KW7-EVK-001
TO-247N For second generation SCT2XXX series		P01SCT2080KE-EVK-001

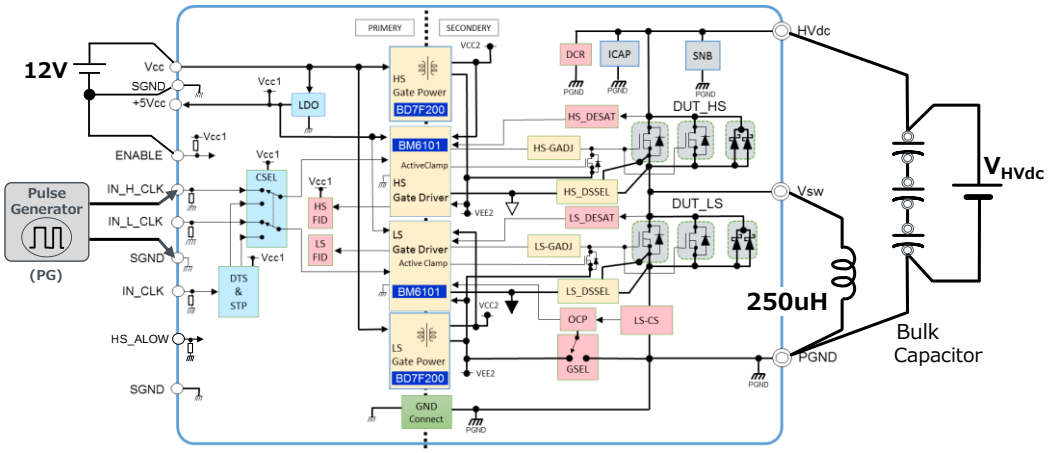
4.2 Case example of evaluation

This section explains an example of implementation of the double pulse test using the evaluation board, P02SCT3040KR-EVK-001. The devices under test are SCT3040KR and SCT3040KL (1,200 V, 40mΩ). Figure 4-1 shows (a) the test circuit, (b) the measurement scene, and (c) the gate drive circuit of the MOSFET.

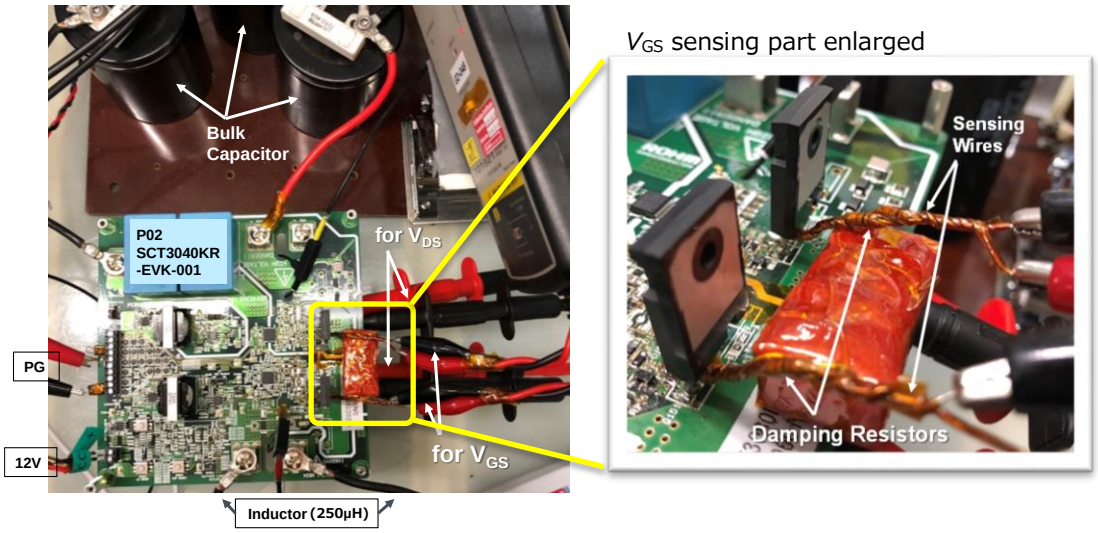
The measurement instruments required for the test are the control power supply (12 V), pulse generator (PG), load inductor (250 µH), and high voltage load power supply (V_{HVdc}) only, as shown in (a). Since V_{HVdc} is located at a distance from the evaluation board, a bulk capacitor is connected in this case. A bulk capacitor is basically unnecessary because a 10 µF film capacitor is also mounted on the evaluation board. However, we recommend connecting a bulk capacitor according to the operating conditions.

The method for sensing V_{GS} during the measurement is explained in (b). An isolated probe is usually used to measure the waveforms of the high-side (HS) MOSFET. However, the end of a high breakdown voltage isolated probe is too large to be attached to the terminal of the MOSFET directly. Therefore, in this measurement, a sensing copper wire of approximately 10 cm in length is soldered to the gate-source terminal of the MOSFET, and the probe is attached to the end of the copper wire. Furthermore, to suppress the waveform ringing due to the inductance of the additional sensing wire, a 100Ω damping resistor is inserted. In addition, the parts indicated in red in (c) are the protection circuit to remove the surge generated between the gate and source of the MOSFET. The effect of this protection circuit is also verified.

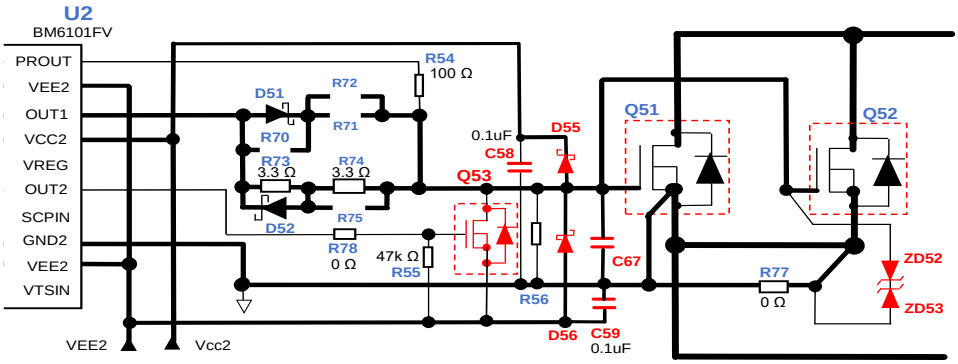
In this case, the HS MOSFET is operated as the switching device, and a body diode is used on the low-side (LS) for commutation. The pulse width is adjusted so that V_{HVdc} is 800 V and I_D is 55 A to 60 A approximately, and the switching operation is observed when the device is turned ON and OFF. The waveforms are shown in Figures 4-2 and 4-3.



(a) Block diagram of measurement circuit



(b) Measurement scene

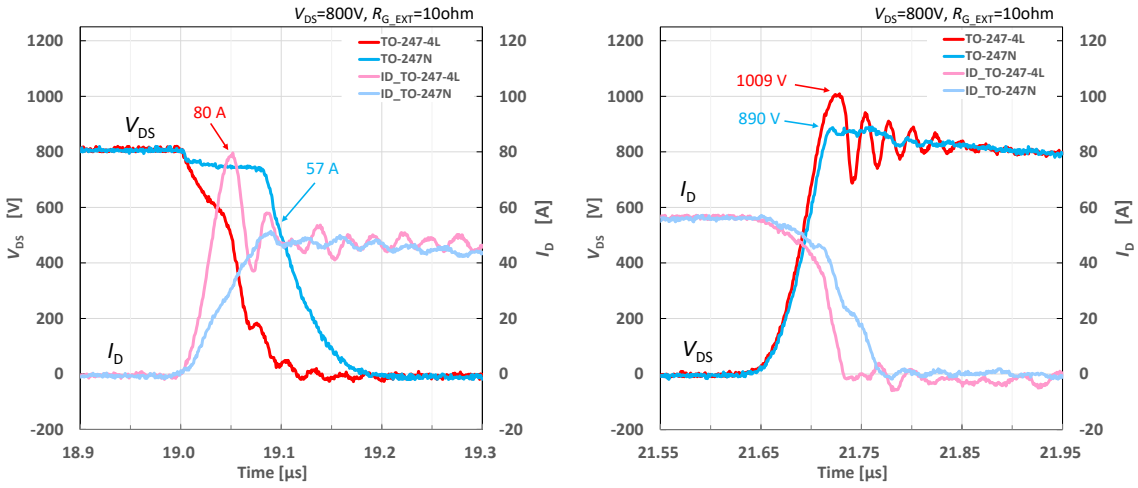


(c) Gate drive circuit

Figure 4-1. P02SCT3040KR-EVK-001 measurement circuit

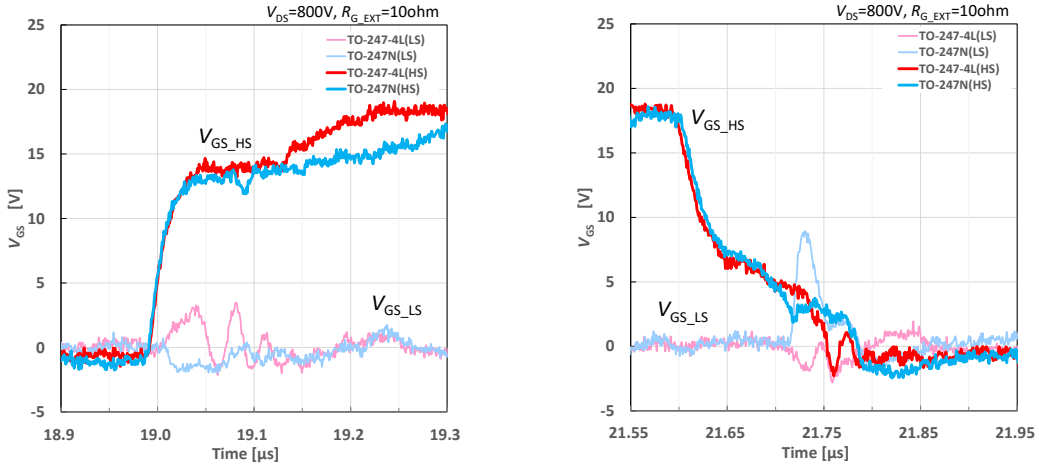
Figure 4-2 (a) and (b) show the waveforms of V_{DS} and I_D while (c) and (d) show the waveforms of V_{GS}, where SCT3040KL (TO-247N) and SCT3040RK (TO-247-4L) are compared. Although the V_{GS_HS} waveforms on the switching side in (c) and (d) are nearly identical, the I_D waveform of TO-247-4L is much faster in (a) whether the device is turned ON or OFF. This is the effect of the driver source terminal described in Section 3.18. For more details, refer to Application Note “Improvement of switching loss by driver source”*4.

Meanwhile, as the protection circuit shown in Figure 4-1 (c) removes the positive and negative surges described in Application Note “Gate-source voltage behavior in a bridge configuration”*1, the gate-source voltage V_{GS_LS} on the non-switching side (LS) MOSFET is shown to satisfy the narrow gate voltage rating unique to SiC MOSFET.



(a) V_{DS} and I_D during turn ON

(b) V_{DS} and I_D during turn OFF



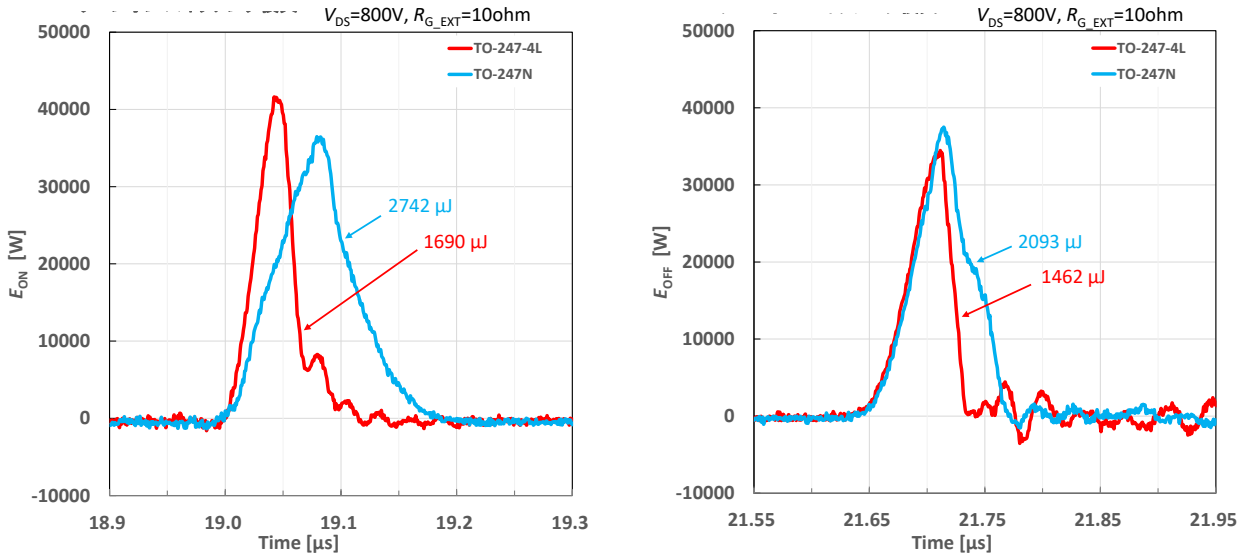
(c) V_{GS} during turn ON

(d) V_{GS} during turn OFF

Figure 4-2. Comparison of switching waveforms between TO-247-4L (SCT3040KR) and TO-247N (SCT3040KL)

Furthermore, Figure 4-3 shows the waveforms of the switching losses Eon and Eoff.

In TO-247-4L, the problem of delayed switching speed due to induced voltage generated in the source terminal is resolved, reducing the total switching loss by approximately 35%.



(a) During turn ON

(b) During turn OFF

Figure 4-3. Comparison of switching losses between TO-247-4L (SCT3040KR) and TO-247N (SCT3040KL)

5. Gate drive

The SiC MOSFET is a switching element of the normally OFF and voltage driven type that is easy to drive with less drive power. The basic driving method is similar to that of the IGBT or the Si MOSFET. The recommended driving gate voltage is around +18 V and 0 V for the ON and OFF sides, respectively. However, if a higher noise tolerance or a faster switching is required, negative voltage can be applied within the gate voltage rating.

In this chapter, we explain cautions for designing related to the gate drive and the recommended driving conditions among other points.

5 .1 Cautions for circuit systems

5.1.1 Driving with pulse transformer

When driving with a pulse transformer, the same voltage is output to the positive and negative polarities. Since the range of the V_{GS} rating of the SiC MOSFET is narrower on the negative side compared with the positive side, pulse transformers, which output the same voltage to the positive and negative sides, cannot be used for the SiC MOSFET.

5.1.2 High-side driving with bootstrap system

If the upper and lower MOSFET are connected in series in a bridge structure, the gate drive on the high-side (HS) is required to employ a floating system. The bootstrap system is one of such systems. Since a great number of references are available regarding the operation, the explanation is omitted here. When the HS MOSFET is OFF, the load current normally flows as described with a solid line arrow in Figure 5-1. At that time, the body diode is energized if the LS MOSFET is OFF. Therefore, the voltage of Vsw is $-V_F$ and the boot capacitor is charged with (V_G + V_F). However, since V_F of the body diode of the SiC MOSFET is higher than that of the Si MOSFET, care must be taken so that the gate voltage rating of the gate driving IC or MOSFET will not be exceeded.

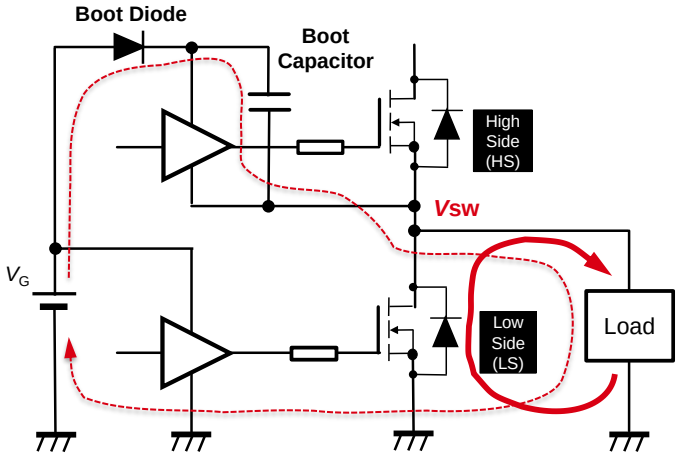


Figure 5-1. Bootstrap circuit

5.1.3 High-side driving with isolated power supply

If an isolated power supply with an isolated transformer is used as the power supply for driving the HS MOSFET, care must be taken regarding the coupling capacitance that exists between the primary and secondary sides of the transformer. This is because the fast variation at the rate of d*v*/d*t* on the secondary side (MOSFET side) of the transformer leads to superimposition of voltage noise on GND1 on the primary side through the coupling capacitance of the transformer, causing a malfunction in the driver IC in the worst case, as shown in Figure 5-2. Therefore, considering the condition of d*v*/d*t* for the *V*sw voltage, use a transformer with the smallest coupling capacitance possible.

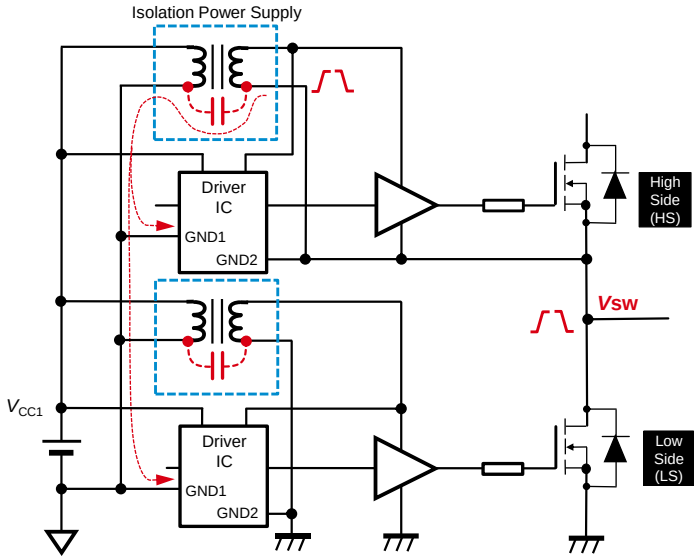
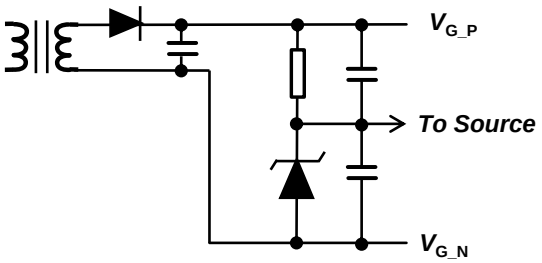


Figure 5-2. Problem with noise in transformer for isolated power supply

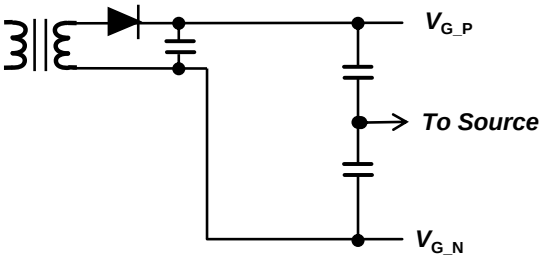
5.1.4 Negative bias generation circuit

An example of circuits generating negative bias is presented in Figure 5-3. Each circuit has advantages and disadvantages in the cost, mounting space, voltage precision, and so on. Therefore, carefully consider the operating conditions of the MOSFET and the system requirements to select a circuit.

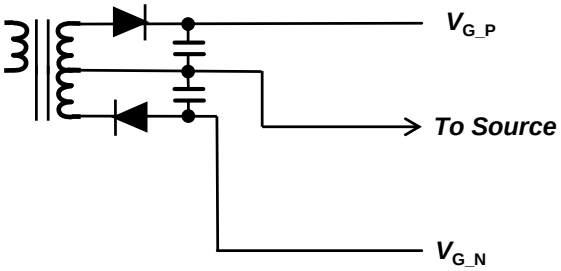
In addition, a driver IC that does not support negative bias can be used by connecting negative bias V_{G_N} to the GND level of the driver IC. However, it should be noted that the monitoring level of the driving voltage of the MOSFET is decreased by the negative bias if the driving voltage of the MOSFET is monitored in the driver IC (UVLO2). For more details, refer to Section 5.3.



(a) Zener diode system



(b) Capacitor voltage dividing system



(c) Positive and negative output transformer system

Figure 5-3. Example of circuit generating negative bias

5.2 Buffer circuit

Although driver ICs are used to drive MOSFET, not a few of them simultaneously feature protection functions against abnormalities. Since the driver ICs equipped with functions required for the system design are generally selected with the priority given to the functions, their driving ability may not be sufficient. In addition, if more than one MOSFET is connected in parallel, for example, in a power module, or if a MOSFET with a large chip size is used, the driving ability of a single drive IC may not be sufficient as well.

In these cases, it is effective to provide a buffer circuit that can complement the driving ability between the driver IC and MOSFET. In Figure 5-4, a push-pull type buffer circuit with a bipolar transistor is shown using ROHM's driver IC (BM61S41RFV-C) as an example.

The buffer circuit is the part enclosed with red dotted lines in Figure 5-4. The drive signal output from the OUT terminal is connected to the base of Q1 and Q2. Q1 and Q2 are turned ON when the level is Hi and Lo, respectively. Although the driving ability of the driver IC is the maximum rating of 4 A, it can be increased up to approximately 10 A (peak) by using ROHM's 2SRC542 and 2SRA542 for Q1 and Q2.

In addition, the buffer circuit can be expected to play a role in dispersing heat generation. The heat generation in the driver IC can be an issue if you want to increase the switching frequency. However, high frequencies can be supported by adding a buffer circuit to disperse the heat generation in the entire drive circuit.

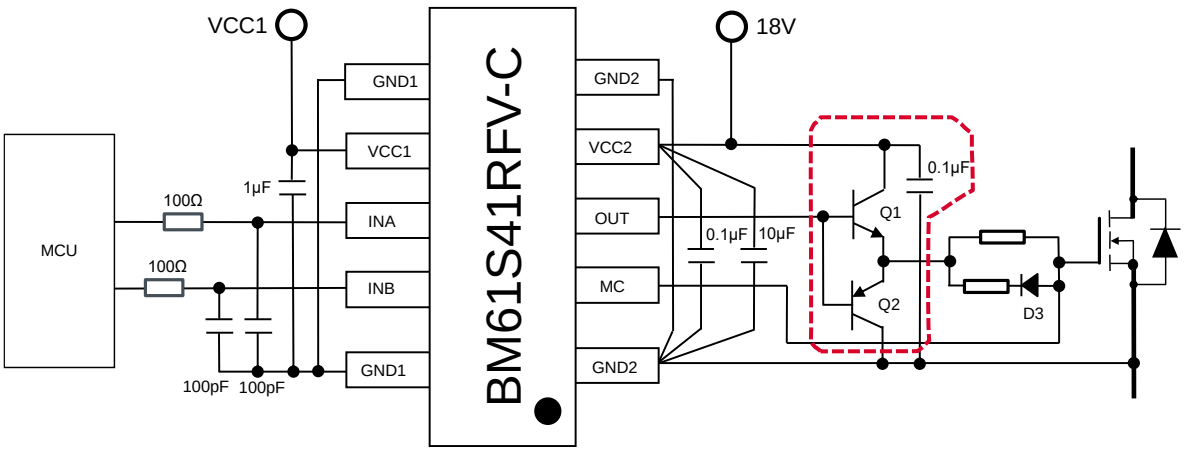


Figure 5-4. Example of buffer circuit (using BM61S41RFV-C)

5.3 UVLO (under voltage lock out: function to prevent malfunction at low voltage)

In Section 3.4 (Figure 3-4), we explained that the resistance during ON ($R_{DS(on)}$) increases as the driving voltage decreases in the SiC MOSFET. For this reason, the driver ICs usually have an additional function to monitor the drop in the driving voltage.

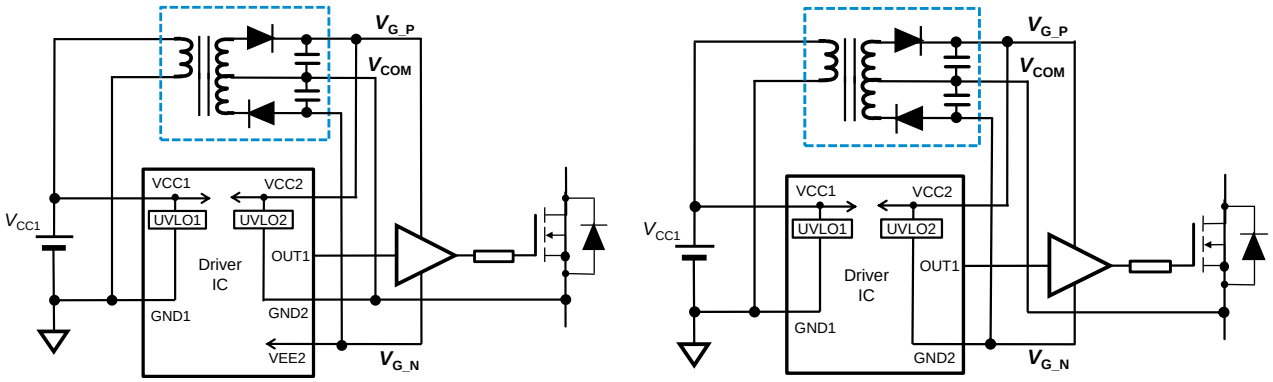
Table 5-1 shows the monitoring level for the driving voltage V_{UVLO2} in ROHM's driver IC (BM61xxxxx series). Since the driving voltage of the SiC MOSFET is higher than that of the Si MOSFET or IGBT, UVLO2 is set to a high level in the BM61S series, which is developed for the SiC MOSFET.

Table 5-1. BM61xxxxx series VCC2 monitoring level

Item	Package	Isolation [kVrms]	Output Current [A]	V_{UVLO2} [V]	V_{OVP} [V]
BM61S40RFV	SSOP-B10W	3750	4	14.5	21.5
BM61S41RFV				14.5	NA
BM61M41RFV				7.4	NA

As also explained in Section 5.1.4, care must be taken regarding cases where a driver IC that does not support negative bias (VEE2) is used in the drive circuit using negative bias. Figure 5-5 shows methods for providing power supply in a general drive circuit. While (a) shows the case of using a driver IC supporting negative bias, (b) shows the case of using a driver IC not supporting negative bias. The power supply for the gate drive uses the V_{G_P} and V_{G_N} power supplies during ON and OFF, respectively, and its GND is set as V_{COM}. Since V_{UVLO2} of a driver IC is generally referenced for GND2 of the IC, GND2 is constant irrespective of the presence or absence of VEE2 and V_{G_P} is monitored at the same level in (a). In the case of (b), however, the monitoring level of the driving voltage of the MOSFET (V_{MOS_UVLO2}) is reduced by negative bias V_{G_N} as described in Equation (1). To use negative bias, select a driver IC that supports negative bias wherever possible.

$$V_{MOS\_UVLO2} = V_{UVLO2} - V_{G\_N} \quad (1)$$



(a) With negative bias function (b) Without negative bias function

Figure 5-5. Example of drive circuit connection according to presence or absence of negative bias function

5.4 Gate driver IC for SiC MOSFET

When selecting a gate driver IC for the SiC MOSFET, the following points must be particularly considered.

- Driving voltage (e.g., the maximum rating)
- Driving ability (e.g., output peak current and switching frequency)
- Propagation delay time (e.g., between the primary and secondary sides)
- Protection function (e.g., Miller Clamp, DESAT, OCP, and UVLO)
- Tolerance to the common mode transient voltage (CMTI: Common Mode Transient Immunity)

In addition, driver ICs are roughly categorized into two types: single function (Simple) and multifunction (Complex) types. The Simple type features the drive signal only, and is productized as small packages including SOP-8 and SSOP-10. In contrast, the Complex type supports negative bias and features various protection functions, the temperature monitoring function, isolated power supply, and so on. Many of these products are available as a large package of SOP-20 and greater.

Many products that provide various required functions are included in the lineup. Please visit ROHM's website (https://www.rohm.co.jp) or contact our sales representative.

5.5 Recommended gate voltage (V_{GS})

The driving voltage is particularly important among the driving conditions for the SiC MOSFET. As explained in Section 3.4, a higher driving voltage is required for the SiC MOSFET compared with the Si MOSFET in order to obtain a sufficiently low on-resistance. Meanwhile, the gate voltage rating of the SiC MOSFET is narrower than that of the Si MOSFET.

Figure 5-6 shows a comparison of the driving voltages between ROHM's SiC MOSFET (SCT3040KL) and super junction MOSFET (R6047KNZ4). Since the recommended driving voltage for SCT3040KL is from 0 V to +18 V, it is necessary to increase the amplitude of the driving voltage compared with that of R6047KNZ4, of which the recommended driving voltage is from 0 V to +10 V.

Meanwhile, compared with the gate voltage rating of R6047KNZ4 from -30 V to +30 V, that of SCT3040KL is narrower, ranging from -4 V to +26 V. Therefore, particular attention should be paid to the negative bias side. Furthermore, the positive and negative surges can be superimposed on the gate-source voltage during switching, and such positive and negative surges must be contained within the gate voltage rating as well.

Since the gate voltage rating of ROHM's SiC MOSFET varies for each generation, a list of comparisons is shown in Table 5-2. In addition, for the gate voltage rating of the SiC MOSFET, refer to Section 8.2 "Reliability of SiC MOSFET".

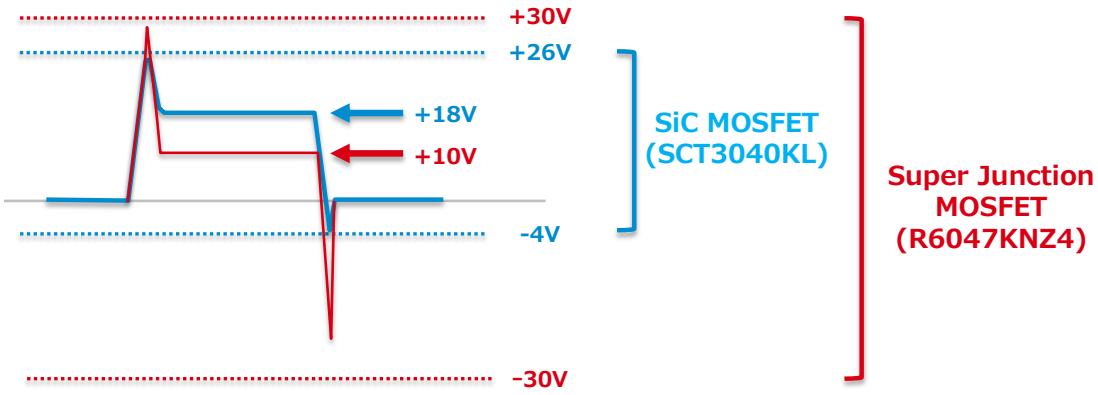


Figure 5-6. Comparison of gate voltage rating between the SiC MOSFET and Si MOSFET

Table 5-2. Comparison of gate-source voltage

Parameter		2nd Generation SCT2xxxx	3rd Generation SCT3xxxx
Gate-Source Voltage		-6 V ~ +22 V	-4 V ~ +22 V
Gate-Source Surge Voltage		-10 V ~ +26 V	-4 V ~ +26 V
Recommended Drive voltage	Positive	+18 V ~ +20 V	+18 V ~ +20 V
	Negative	-4 V ~ 0 V	0 V

5.6 Recommended external gate resistance (R_{G_EXT})

An important factor determining the switching performance of the MOSFET is the external gate resistance (R_{G_EXT}). As described in Equation (2), the peak current during gate driving is determined by the total value of the output source resistance of the driver IC (R_{ONH}), R_{G_EXT}, and the internal gate resistance (R_{G_INT}). As explained in Section 3.9, the internal gate resistance of the SiC MOSFET generally tends to be higher than that of the Si MOSFET. Therefore, it is necessary to decrease the external gate resistance R_{G_EXT} and increase the gate current in order to operate the high speed switching. In addition, since the positive and negative surges between the gate-to-source terminals described in Section 5.5 also increase as R_{G_EXT} increases, the surges can be reduced by selecting the smallest value possible for R_{G_EXT}.

$$I_{PEAK} = \frac{V_{G\_P}}{(R_{ONH}+R_{G\_EXT}+R_{G\_INT})} \quad (2)$$

However, accelerating the switching increases the voltage surge that is generated between the drain and source. Therefore, select R_{G_EXT} so that the surge is contained within the rating, or add a surge absorption circuit such as a snubber circuit to absorb the surge.

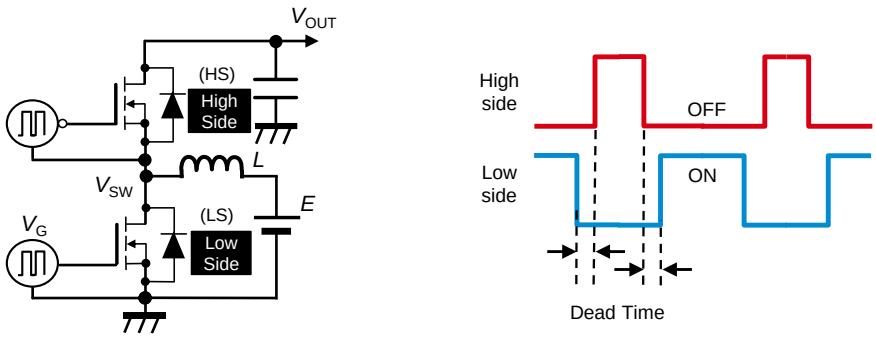
5.7 Recommended dead time (t_{DT})

For the MOSFET used with the bridge structure, dead times are usually provided so that the upper and lower sides will not be turned ON simultaneously. Figure 5-7 (a) shows a case example of the dead time control in a boost circuit. The low-side (LS) and high-side (HS) MOSFET operate for switching and synchronous rectification, respectively. As shown in (b), dead times are provided before LS is turned ON and after LS is turned OFF to prevent HS and LS from turning ON simultaneously. During the dead times, the current of inductor *L* flows through the body diode of the MOSFET. Since the forward voltage V_F of the body diode of the SiC MOSFET is higher than that of the Si devices, it is considered desirable to shorten the dead times as much as possible.

However, if the current of inductor *L* during turn OFF ($I_{L(OFF)}$) decreases, the charge/discharge current to Coss of the upper and lower MOSFET also decreases. As a result, the charge/discharge of Coss, i.e., the variation in V_{DS}, cannot be completed within the dead times. In this case, the switching loss, which should not occur originally, is generated in the synchronous rectification MOSFET, and issues with reduced efficiency or increased heat generation emerge. Therefore, it is necessary to estimate the minimum value of the dead time according to the operation condition of $I_{L(OFF)}$.

The minimum dead time shown in Equation (3) is calculated with a constant Coss for the sake of simplification. However, actual Coss varies with the drain-source voltage V_{DS}. In many cases, Coss described in the data sheet is generally a representative value at a certain V_{DS} and not necessarily the worst condition. By using the V_{DS}-C characteristics shown in Figure 5-8 and calculating Coss with V_{DS} <1 V where Coss is maximized, the dead time can be designed with a margin (the part inside the dotted square). Actual electric charge required for the charge/discharge corresponds to the area of the part enclosed with solid lines in the figure. Therefore, t_{DT} can also be calculated more accurately by using this area part for the numerator in Equation (3). The capacitance graphs such as Figure 5-8 are almost always presented in the data sheet.

$$t_{DT} > \frac{(C_{OSS\_HS}+C_{OSS\_LS})\times V_{OUT}}{I_{L(off)}} \quad (3)$$



(a) Boost circuit (b) PWM pulse timing

Figure 5-7. Dead time control in boost circuit

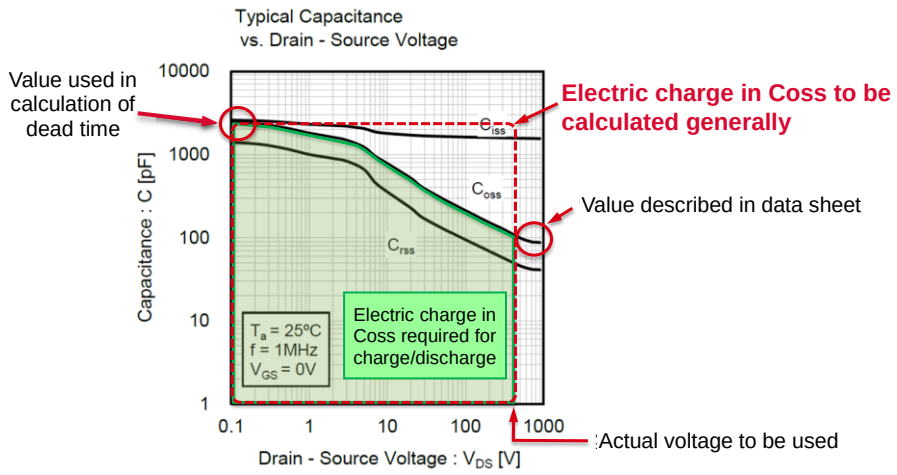
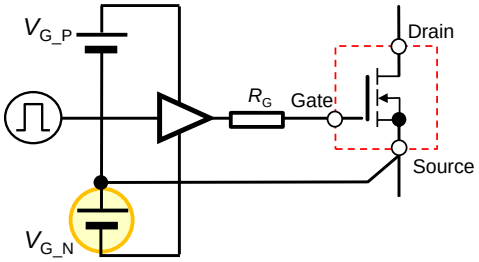


Figure 5-8. V_{DS} dependence of parasitic capacitance (SCT3040KL)

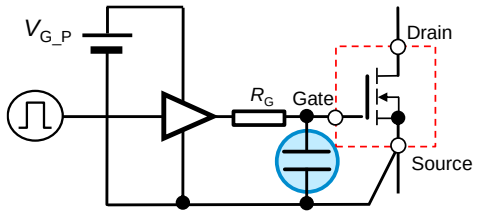
5.8 Countermeasures against self-turn-on

If MOSFET are used in bridge structures, such as inverters and full bridge circuits, the MOSFET on either or both of the upper and lower arms are supposed to be turned OFF. However, due to variation in V_{DS} or I_D on the non-switching side (commutation side) responding to the operation of the switching side MOSFET, they can be accidentally turned ON even when the OFF command has arrived at the gate terminal. This is referred to as self-turn-on. When this phenomenon occurs, not only is the efficiency reduced, but the MOSFET may also be damaged in the worst case.

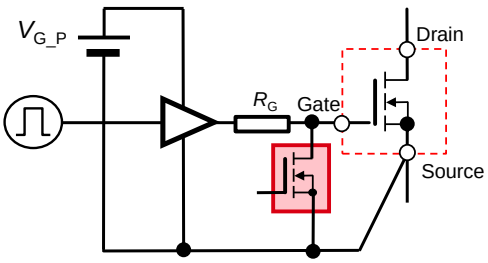
Figure 5-9 shows examples of circuits for countermeasures. In (a), by making the turn OFF voltage a negative voltage (V_{G_N}), the gate voltage is prevented from exceeding $V_{GS(th)}$ even when a rise of the gate voltage occurs that can trigger the self-turn-on. However, this method cannot be used for the third generation SiC MOSFET, for which the V_{GS} rating on the negative side is narrow. In (b), by connecting a capacitor of 1 nF up to 5 nF between the gate and source of the MOSFET, an instantaneous rise of the gate voltage is prevented. In (c), by using an active miller clamp MOSFET that is turned ON below a certain value of the gate-source voltage, a rise of the gate-source voltage is prevented. For (b) and (c), since these effects are diminished if the parasitic inductance exists, it is important to install the parts for countermeasures as proximate as possible to the gate and source terminals. It is also recommended to select parts in a small package with a small parasitic inductance.



(a) Negative bias



(b) Capacitor connected between gate and source



(c) Active miller clamp MOSFET

Figure 5-9. Example of countermeasures against self-turn-on in bridge structure

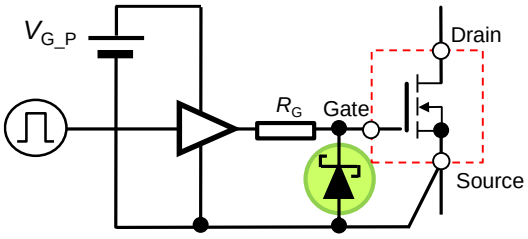
Each system has advantages and disadvantages, and may not be applicable depending on the functions of the driver IC to be used. Please understand the generation mechanism of self-turn-on correctly and make selection.

The generation mechanism of self-turn-on is detailed in Application Note “Gate-source voltage behavior in a bridge configuration”*1. In addition, various circuits for countermeasures are presented in Application Note “Gate-Source Voltage Surge Suppression Methods”*2. Please refer to this Application Note as well.

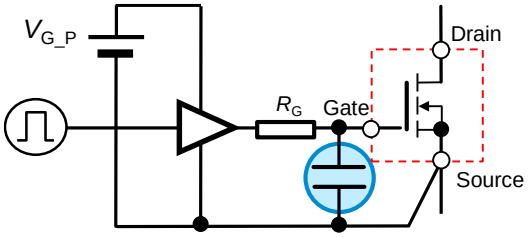
5.9 Countermeasures against negative surge

As explained in Section 5.5, the gate voltage rating of the SiC MOSFET is very narrow. In particular, the margin for the voltage during actual use is only a few V regarding the negative bias. Therefore, it is very important to include countermeasures against the gate negative surge from the design phase.

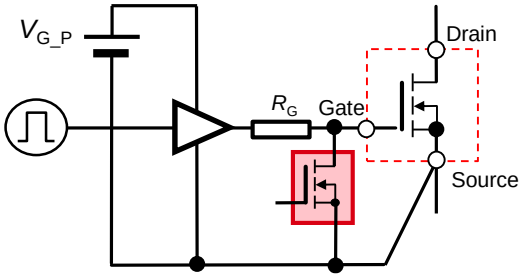
Figure 5-10 shows the circuits for countermeasures against the negative surge. In (a), a diode to clamp the negative bias is connected between the gate and the source. In (b), by connecting a capacitor of 1 nF up to 5 nF between the gate and source of the MOSFET, an instantaneous drop of the gate voltage is prevented. In (c), by using an active miller clamp MOSFET that is turned ON below a certain value of the gate-source voltage, a drop of the gate-source voltage is prevented. The countermeasures in (b) and (c) are identical to the countermeasures against self-turn-on described in Section 5.8 and these countermeasures can be shared. In addition, similar to the countermeasures against self-turn-on, it is important to install the parts for countermeasures proximate to the gate and source terminals and select parts with the smallest parasitic inductance possible.



(a) SBD connected between gate and source



(b) Capacitor connected between gate and source



(c) Active miller clamp MOSFET

Figure 5-10. Countermeasures against negative surge in bridge structure

However, the negative surge is not necessarily caused by a single factor, but caused by multiple factors closely connected with the timing of variations in V_{DS} and I_D. Effective countermeasures depend on the timing of occurrence of the negative surge. Therefore, it is necessary at first to accurately understand the factors causing the negative surge. It is important to take the best countermeasures according to the circumstances, such as the presence or absence of the negative bias and the board layout conditions, based on this understanding.

The generation mechanism of negative surge is detailed in Application Note “Gate-source voltage behavior in a bridge configuration”*1. In addition, various circuits for countermeasures are presented in Application Note “Gate-Source Voltage Surge Suppression Methods”*2. Please refer to this Application Note as well.

5.10 Short-circuit protection

There are several methods of short-circuit protection for MOSFET. In this section, representative methods are explained.

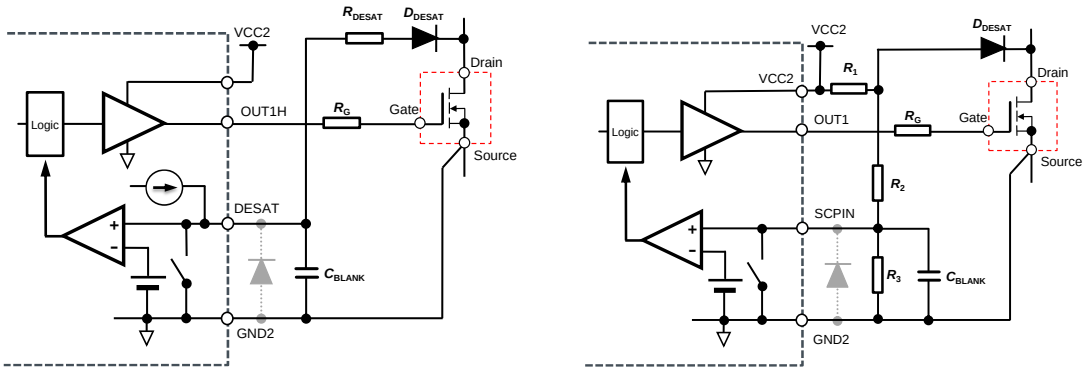
5.10.1 DESAT

DESAT (desaturation fault detection) is widely used as the simplest short-circuit protection and incorporated in most of the products of the Complex type of driver IC.

Figure 5-11 shows examples of the DESAT circuit using ROHM's driver IC: (a) BM60052AFV-C and (b) BM6101FV-C. The external components include the DESAT resistor R_{DESAT}, R_1, R_2, R_3, the DESAT diode D_{DESAT}, and the blanking capacitor C_{BLANK}, which are used to adjust the detection level, detection time, and so on. For D_{DESAT}, select the high speed recovery type because the applied voltage varies at dv/dt in proportion to the switching speed of the MOSFET. In addition, the drain terminal voltage is also applied to R_{DESAT} and R_1 during the recovery period of D_{DESAT}. Therefore, it should be noted that a resistor with an excessively low rated voltage is not appropriate.

The detection level and the detection time for the short-circuit current should be set based on an understanding of the current tolerance and the short-circuit rating of the MOSFET to be used. In addition, depending on the circuit structure of the MOSFET, the voltage of the drain terminal may drop to less than that of the source terminal, lowering the DESAT terminal of the driver IC below GND2. It should be noted that protection of the DESAT terminal by connecting a clamp circuit with diodes and the like is also required.

For more details including the operations and the setting method of the short-circuit current level, refer to the data sheet for the driver IC to be used and Application Notes.



(a) Using driver IC BM60052AFV-C (b) Using driver IC BM6101FV-C

Figure 5-11. DESAT circuit

5.10.2 Short-circuit protection in MOSFET equipped with current sense terminal

The current detection circuit for the MOSFET and IGBT equipped with the current sense terminal is shown in Figure 5-12. The current flowing through the current sense resistor (R_{SENSE}) is reduced in proportion to the number of cells, for example, by 1/1000 of the current flowing between the drain and the source. Therefore, even with a large current, the power loss in the current detection circuit can be limited. However, since noise components such as the recovery current in the bridge structure are detected together, it may be necessary to remove the noise with an RC filter and the like, depending on the circuit operating conditions.

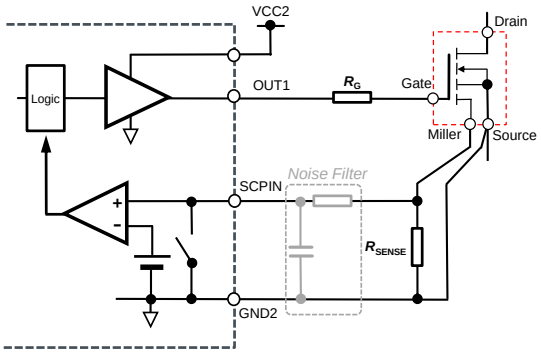


Figure 5-12. Over current protection circuit using driver IC BM6101FV-C

5.11 Recommended layout

We have explained the following functions of the gate drive circuits.

- Gate resistance (adjusting the switching speed)
- Buffer circuit (increasing the gate driving ability)
- Gate surge protection (MOSFET gate protection)
- MOSFET short-circuit protection (preventing damage during over current)
- Gate driving power supply.

All of these required circuit parts must be mounted on the printed board. Ideally, all functions should be mounted near the MOSFET. However, it is necessary to set priorities on the board layout.

In addition, the degree of occurrence of the gate surge and the priorities of countermeasures also depend on the characteristics and circuit topology of the device to be used. Therefore, when considering the layout of a circuit around the MOSFET, careful examination is required regarding the pattern inductance of which function should be reduced.

To categorize the circuit topologies, they can be distinguished based on the MOSFET structure and the switching operation. Namely, they can be roughly distinguished into the structure using a single MOSFET (single) and the structure using the upper and the lower MOSFET connected in series (half bridge), and further categorized into the hard switching system (hard switching) and the soft switching system (soft switching) as the switching operation of the MOSFET.

In the half bridge structure, the non-switching side is affected by the operation on the switching side. In contrast, since a single MOSFET is used in the single structure, it is sufficient to consider its own switching operation only.

Furthermore, the required functions are distinguished for each device generation. The reason is that the switching characteristics and the gate voltage rating vary with the generations.

Table 5-3 shows the required functions and the layout guide for each device generation and circuit structure. By determining the layout priorities of the parts for countermeasures in the following order, operations within the rating and a high efficiency should be achieved simultaneously.

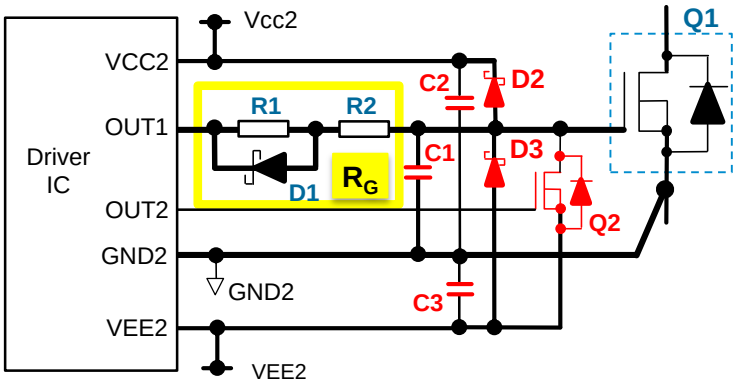
Table 5-3. Required functions in gate drive circuit

Topology		Second generation SiC MOSFET	Third generation SiC MOSFET
Single End	Hard Switching Soft Switching	1) Gate resistance	1) Negative surge clamp SBD 2) Gate resistance
Half Bridge	Hard Switching	1) External capacitor between G-S 2) Gate resistance	1) Active miller clamp MOSFET 2) Negative surge clamp SBD 3) External capacitor between G-S 4) Gate resistance
	Soft Switching	1) Gate resistance	1) Negative surge clamp SBD 2) External capacitor between G-S 3) Gate resistance

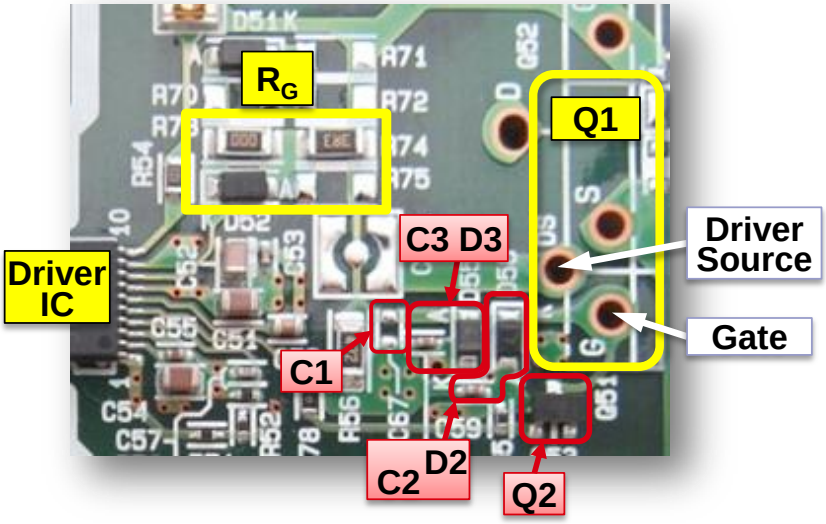
Figure 5-13 shows a layout example for the half bridge evaluation board for the SiC MOSFET (P02SCT3040KR-EVK-001): (a) drive circuit diagram, (b) picture of the mounted board, and (c) and (d) layout of the board pattern.

Since this board is used to evaluate the third generation SiC MOSFET with the hard switching operation, the countermeasures against gate surges are the most important. Since the driver IC being used (BM6101FV-C) features the control signal for the active clamp MOSFET, place the MOSFET (Q2) most proximate to the SiC MOSFET, and then place the diode for absorbing the negative surge (D3) and its bypass capacitor (C3). Next, the diode for absorbing the positive surge (D2) and its bypass capacitor (C2) are laid out. Since the positive surge is generated due to the inductance caused by the pattern length from the driver IC to the MOSFET, whether or not the mounting is possible is judged according to the layout situation. Finally, the capacitor for countermeasures against self-turn-on (C1) is placed between the gate and the source.

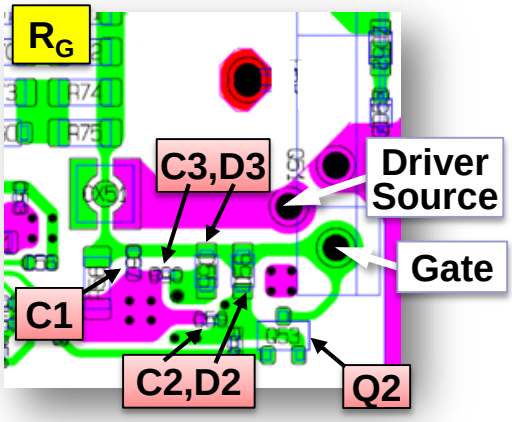
The effect of the surge absorption parts is diminished as the distance from the MOSFET increases. Therefore, it is recommended to place the parts within 2 cm from the MOSFET as shown in (c). In addition, it is important to lay out the return line from the driver source terminal to the driver IC directly under all the driver circuit parts, as in pattern (d) covering the entire surface, so that the effect of external noise on the drive signal and the surge protection circuit can be reduced as much as possible.



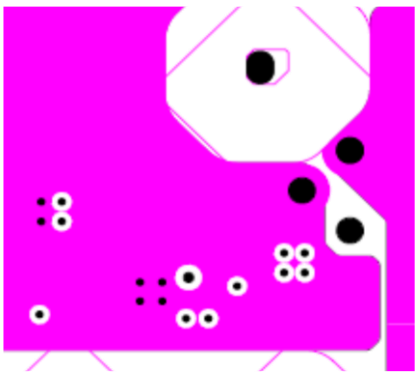
(a) Example of gate surge protection circuit



(b) Example of gate surge protection circuit mounted on PCB (P02SCT3040KR-EVK-001)



(c) Parts mounted surface



(d) Second layer

Figure 5-13. Layout example of gate surge protection circuit (P02SCT3040KR-EVK-001)

5.12 Precautions for using MOSFET in series or parallel

If multiple MOSFET are simultaneously operated in series or parallel, it is nearly impossible to operate each of them on the completely same timing, because variation in the characteristics always exists in each device. Therefore, the precautions that must be observed are different from those where a single device is used.

Although general precautions are explained in this section, it does not mean we recommend using multiple MOSFET. Before use, confirm that they can be operated safely.

5.12.1 Series connection

If the voltage applied to the device (V_{IN}) exceeds the rating of the device to be used, two devices may be connected in series (Figure 5-14) in order to reduce the voltage applied to each device by half. However, care must be taken because disequilibrium of the voltages applied to the devices may occur due to variation in the characteristics of the devices, the inductance of the board wiring, and so on.

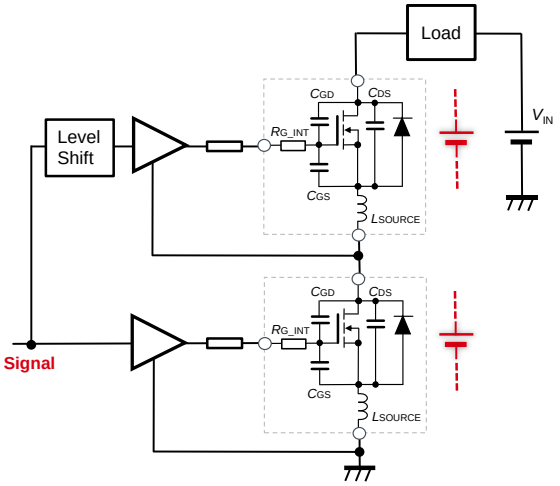


Figure 5-14. MOSFET series connection

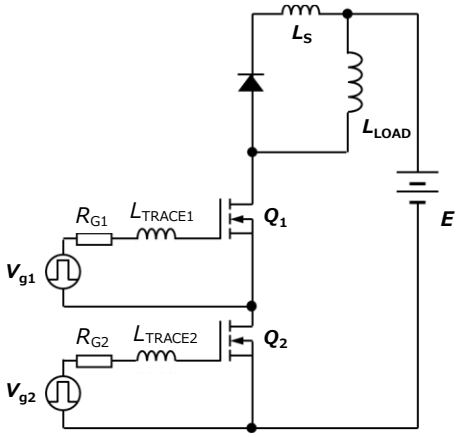
In the initial state when the power is turned ON (before any switching operation is performed), the voltage applied to each device corresponds to the ratio of Coss. However, once the switching operation is started, disequilibrium of the voltages applied to the devices becomes obvious due to variation in the switching speed during turn OFF. The following variations can be considered as the factors of the variation in the switching speed.

- $V_{GS(th)}$ of MOSFET
- Capability of the drive circuit (external gate resistance, wire inductance)
- Delay in the drive circuit
- Ciss, Crss, Coss, and the internal gate resistance of MOSFET

Figure 5-15 shows the simulation result of the V_{DS} waveforms during turn OFF: (a) the simulation circuit and the conditions, (b) variation in $V_{GS(th)}$, (c) variation in external R_G, (d) difference in the pattern inductance of the gate drive circuit, (e) variation in delay of the drive circuit, (f) variation in C_{GD}, and (g) variation in C_{GS}. The effect of each factor on the V_{DS} waveforms of MOSFET Q1 and Q2 is shown. The disequilibrium of V_{DS} due to the variations in the slight delay of 5 ns in the gate drive circuit as shown in (e) and C_{GD} of the MOSFET in (f) is pronounced. However, the effects of other factors including $V_{GS(th)}$ and the pattern inductance of the drive circuit cannot be ignored, either.

As seen above, any variation can strongly affect the switching speed of the MOSFET. If the switching operation is performed with an imbalance between the devices, not only does the switching loss become unbalanced, but V_{DS}

higher than the rating is also applied as a result, leading to deterioration of the reliability, and the devices may be damaged in the worst case. Verify the variations carefully before performing the operation.



Simulated condition

Q1,Q2 : SCT3160KL

E=1500V

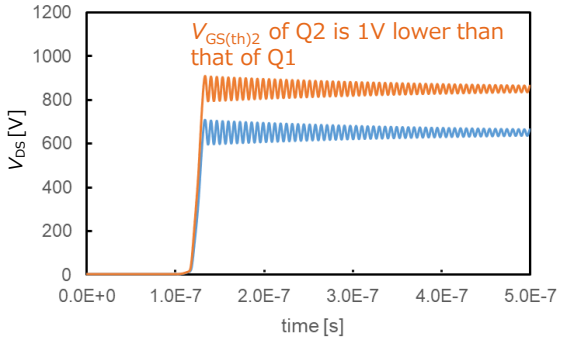
I=20A

L_S=50nH

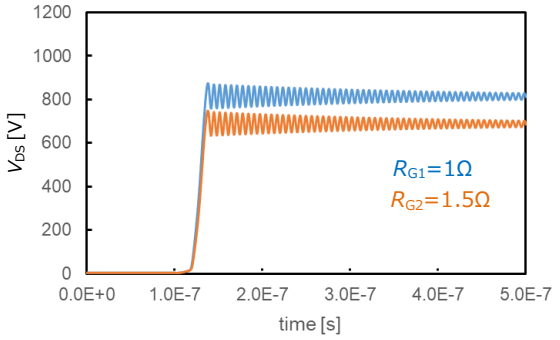
L_{TRACE1}=L_{TRACE2}=20nH

R_{G1}=R_{G2}=1Ω

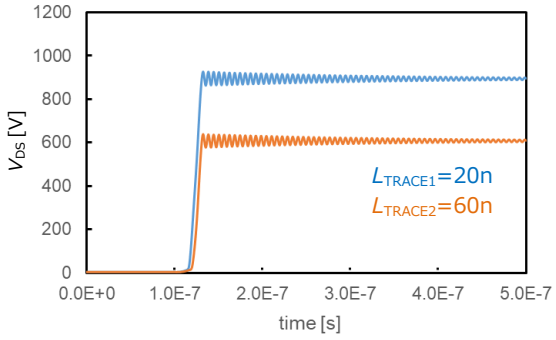
(a) Simulation circuit and operating conditions for MOSFET connected in series



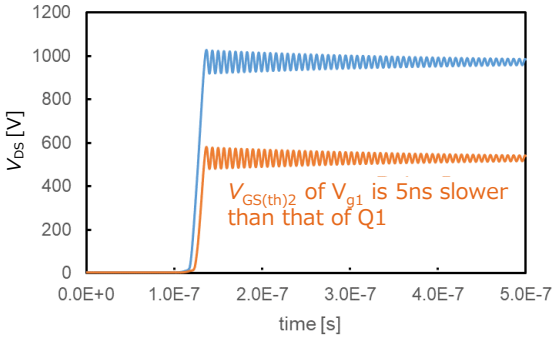
(b) Variation in $V_{GS(th)}$



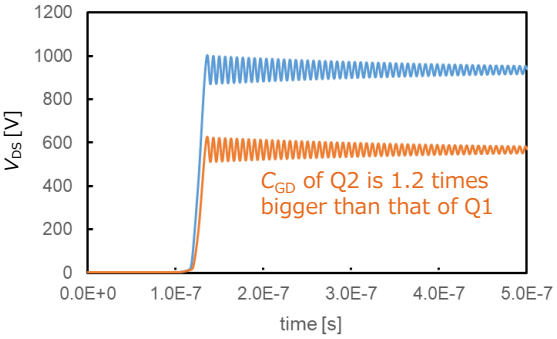
(c) Variation in external R_G



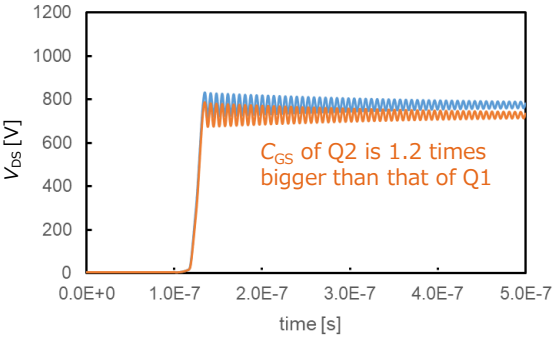
(d) Difference in pattern inductance of gate drive circuit



(e) Variation in propagation delay of gate drive circuit



(f) Variation in C_{GD}



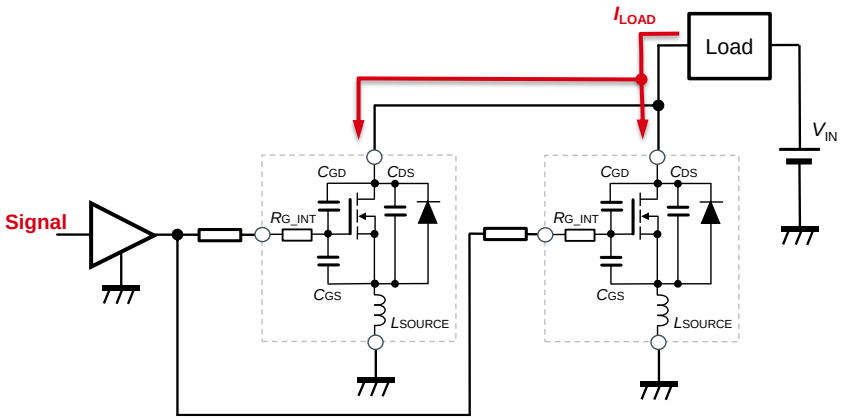
(g) Variation in C_{GS}

Figure 5-15. Simulation waveforms for MOSFET connected in series

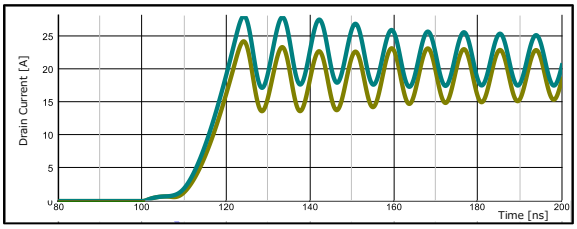
5.12.2 Parallel connection

If the current flowing through the device (I_{LOAD}) is larger than the rating for the device to be used, two devices may be connected in parallel in order to reduce the current flowing through each device (I_D) by half.

Figure 5-16 (a) shows an example of such a connection. To reduce the variation in the switching operation between the devices, an external gate resistor is individually connected to each MOSFET. If the MOSFET is directly driven without connecting the external gate resistor, the current disequilibrium can easily occur in the transient state during turn ON or turn OFF due to the variation in the characteristics of the MOSFET and the drive circuit. [Figure 5-16(b)]



(a) Drive circuit for parallel connection



(b) Simulated disequilibrium of drain current during turn ON (without external gate resistor)

Figure 5-16. MOSFET connected in parallel

However, even when the external gate resistors are connected, the current imbalance can still occur due to the variation in the devices and the disequilibrium in the drive circuit. The following variations can be considered as the factors of the current imbalance.

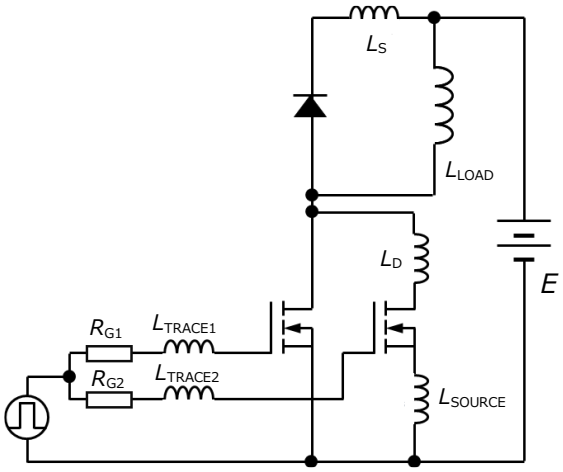
- $V_{GS(th)}$ of MOSFET
- Capability of the drive circuit (external gate resistance, internal gate resistance, wire inductance)
- Wire inductance in the main circuit of MOSFET
- Ciss, Crss, and Coss of MOSFET
- Cooling condition of MOSFET (attached to different heatsinks)

Figure 5-17 shows the simulation result of the I_D waveforms during turn ON: (a) the simulation circuit and the conditions, (b) variation in $V_{GS(th)}$, (c) variation in external R_G, (d) difference in the pattern inductance of the gate drive circuit, (e) variation in the inductance of the MOSFET main circuit, (f) variation in C_{GD}, (g) variation in C_{GS}, and (h) difference in the source inductance included in the drive circuit. The effect of each factor on the I_D waveforms of MOSFET Q1 and Q2 is shown.

As is obvious from (b) and (h), the larger the difference in $V_{GS(th)}$ and the difference in the source inductance, the more pronounced the I_D disequilibrium during turn ON. In addition, the I_D disequilibrium also tends to increase if (e) difference in the inductance of the main circuit or (f) variation in C_{GD} of the MOSFET is larger.

As seen above, the switching operation with an imbalance between the devices connected in parallel causes a transiently excessive I_D to flow instantaneously, increasing the switching loss. As a result, not only is the reliability deteriorated due to the increase in heat generation of the device itself, but the device may also be damaged in the worst case. In particular, verify the variations carefully before performing the operation under the condition where the carrier frequency is high and the switching loss increases relatively.

In the steady state, since the on-resistance of the MOSFET ($R_{DS(on)}$) tends to increase as the temperature increases (see Section 3.5), the currents applied to the individual devices (I_D) are balanced spontaneously.



Simulated Condition

Q1,Q2 : SCT3022KL

E=800V

I=150A

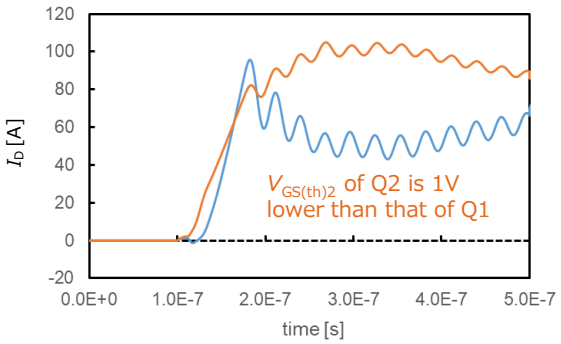
L_S=50nH

L_{TRACE1}=L_{TRACE2}=20nH

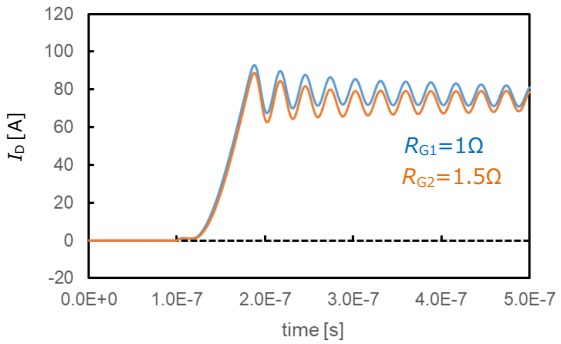
R_{G1}=R_{G2}=1Ω

L_{SOURCE}=0nH

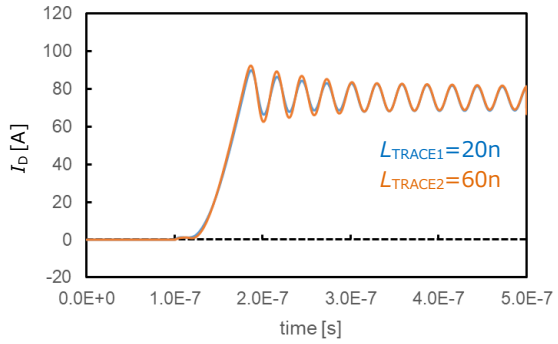
(a) Simulation circuit and operating conditions for MOSFET connected in parallel



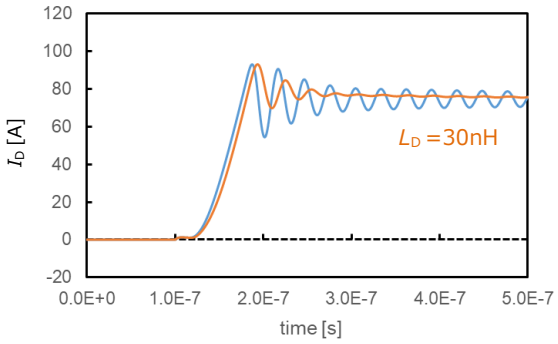
(b) Variation in $V_{GS(th)}$



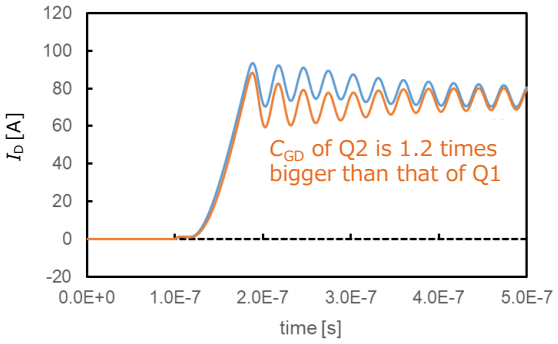
(c) Variation in external R_G



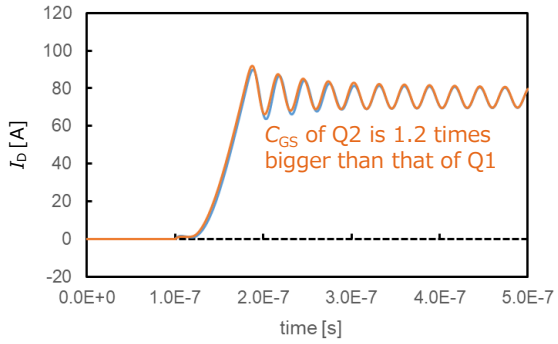
(d) Difference in pattern inductance of gate drive circuit



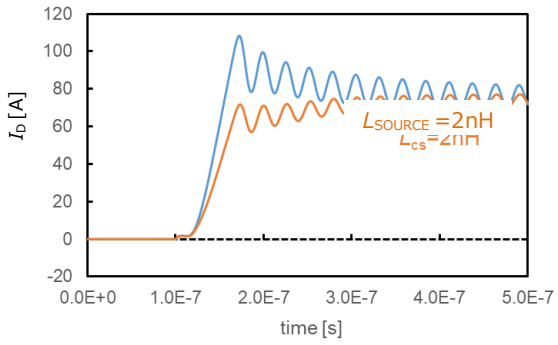
(e) Difference in drain pattern inductance



(f) Variation in C_{GD}



(g) Variation in C_{GS}



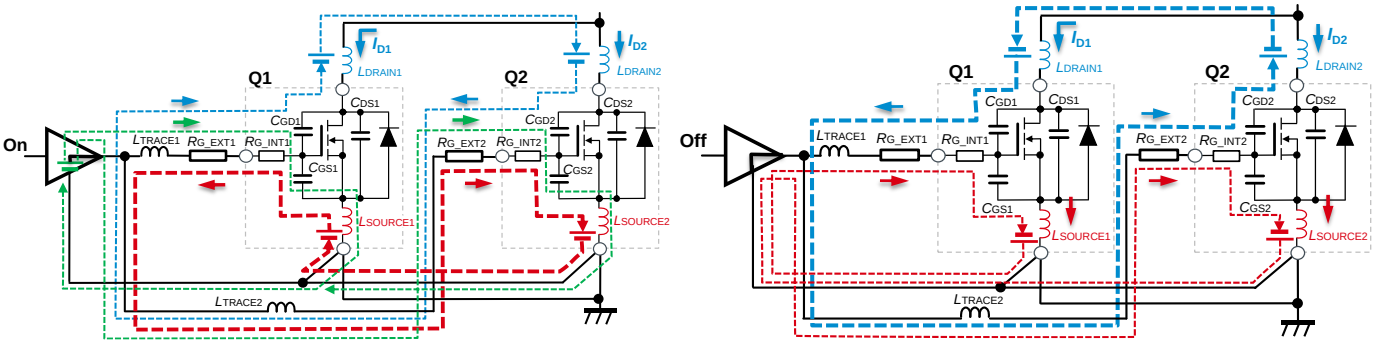
(h) Variation in L_{SOURCE}

Figure 5-17. Simulation waveforms for MOSFET connected in parallel

In addition, in rare cases, the gate-source voltage (V_{GS}) can oscillate with the parallel connection. This oscillation phenomenon can occur in both of the turn ON and turn OFF timings. As shown in Figure 5-18, this oscillation is caused by the formation of RLC resonance circuits between Q1 and Q2 due to the gate resistance between the MOSFET (Q1, Q2) (R_{G_EXT} + R_{G_INT}), the inductance of the board pattern of the drive circuit (L_{TRACE}), and the capacitance between the gate and drain (C_{GD}) or the capacitance between the gate and source (C_{GS}) of the MOSFET. If there is no variation in the MOSFET and the drive circuits are completely the same, the devices connected in parallel and the drive circuit would perform the identical operation. Therefore, no energy would be exchanged between the devices and the resonance would not occur. However, difference exists in both of them actually, and the imbalance in the drain current (I_D) causes difference in the induced voltage generated with L_{SOURCE}. The difference in the generated induced voltage results in the energy exchange in the closed circuit between the devices connected in parallel, causing the oscillation.

In the parallel connection shown in Figure 5-18, if the variation in the MOSFET or the difference in the drive circuit causes I_D of MOSFET Q1 to start ON or OFF slightly earlier than that of Q2, the resonance currents flow in the direction of the arrows between the MOSFET immediately after ON or OFF is started. During turn ON (a), in addition to the current charging C_{GS} (green), the resonance currents are generated with L_{DRAIN1} and $L_{SOURCE1}$ (red and blue). As R_{G_EXT} decreases (dI_D/dt increases), the resonance currents due to the imbalance and other factors are increased and more likely to cause the oscillation.

In contrast, in the resonance circuit during turn OFF (b), the drive circuit side is connected to GND. Therefore, the resonance circuits containing L_{SOURCE} do not affect each other, and only the resonance circuits due to the induced voltage generated with L_{DRAIN} affect the V_{GS} oscillation.



(a) V_{GS} oscillation operation during turn ON

(b) V_{GS} oscillation operation during turn OFF

Figure 5-18. V_{GS} oscillation due to parallel connection of MOSFET

These V_{GS} oscillations can be reduced by increasing R_{G_EXT} or inserting a ferrite bead proximate to the gate terminal. This is also obvious from the fact that the condition of the damping resistance in the oscillation of an RLC circuit is generally expressed with Equation (4).

$$R > 2 * \sqrt{\frac{L}{C}} \quad (4)$$

6. Features of SiC power module

6.1 Features of SiC module

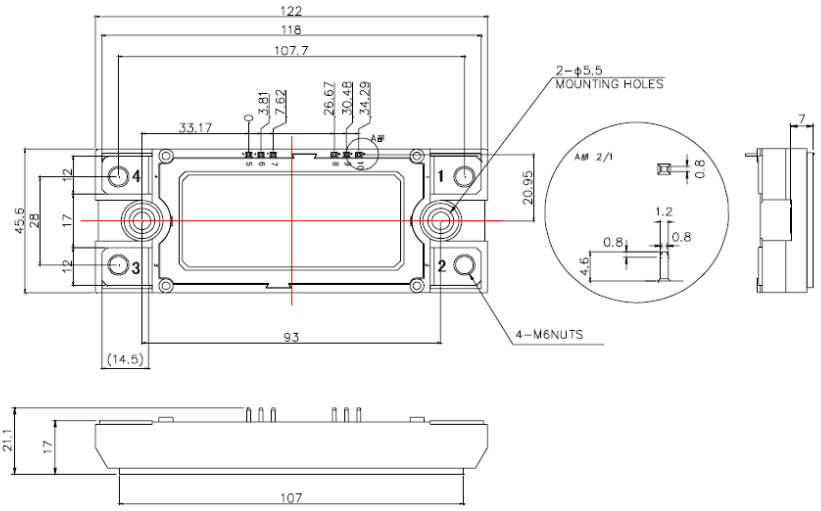
Currently, IGBT modules that combine the Si IGBT and FRD are widely used for power modules that can handle a large current. ROHM leads the world in mass production of the power modules equipped with the SiC MOSFET and the SiC SBD. Since a large switching loss caused by the tail current of the IGBT and the recovery current of the FRD can be significantly reduced with SiC modules, the following effects can be obtained among others.

1. Improvement in the power supply efficiency and simplification of the cooling structure due to reduction in the switching loss
   (example: downsizing of heatsink, replacement of water cooling/forced air cooling with natural air cooling)
2. Downsizing of peripheral parts due to increase in the operation frequency
   (example: downsizing of reactors, capacitors, etc.)

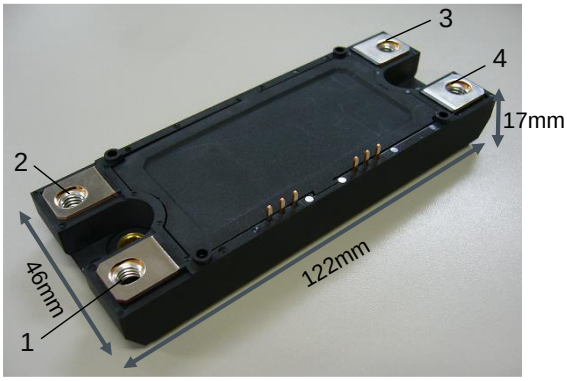
Their applications extend to various uses, including power supplies for industrial equipment and power conditioners for solar power generation.

6.2 Circuit configuration

The current products of the SiC power module are available in the 2 in 1 type that can configure half bridge circuits and the chopper type that can configure chopper circuits. For the 2 in 1 type, the SiC MOSFET + SiC SBD type and the type configured with the SiC MOSFET only can be selected according to the applications. Figure 6-1 shows the external view of the C-type module, and Figure 6-2 shows the internal circuit diagram.

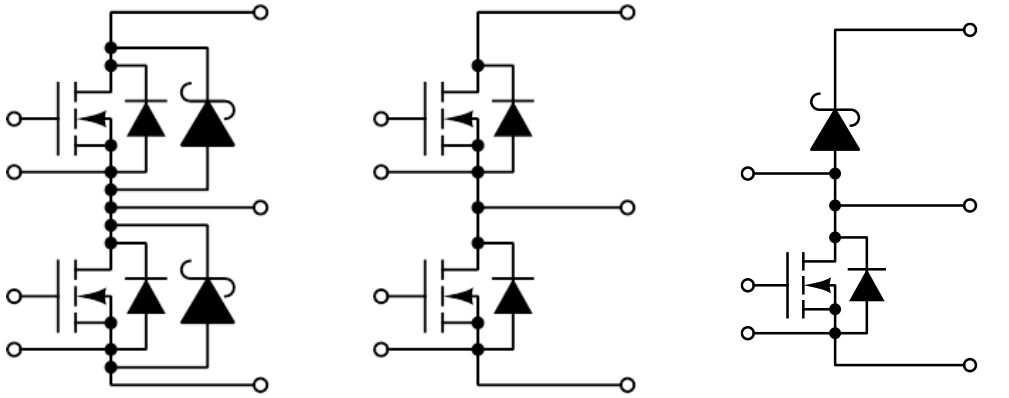


(a) Outline drawing



(b) Picture of external view

Figure 6-1. Shape of C-type power module



(a) 2 in 1
(SiC MOSFET with SiC SBD)

(b) 2 in 1
(SiC MOSFET)

(c) Chopper
(SiC MOSFET and SiC SBD)

Figure 6-2. Circuit diagram of SiC power module

6.3 NTC thermistor

When the module product is equipped with a thermistor, the temperature inside the module case can be monitored. The resistance value at 25°C and the B constant (temperature coefficient) of a thermistor are specified in its product specifications. The resistance value of a thermistor at temperature T_1 [$R_{th}(T_1)$] is derived from Equation (5).

$$R_{th}(T_1) = R_{th}(T_0) * \exp\left\{B_{T_0/T_1} * \left(\frac{1}{T_1} - \frac{1}{T_0}\right)\right\} \quad (5)$$

$R_{th}(T_1)$： Resistance value of the thermistor at the prescribed temperature

T_0： Reference temperature for calculating the resistance of the thermistor
Generally specified to 25°C for ROHM products

T_1： Temperature of the thermistor being detected

$R_{th}(T_0)$： Resistance value at the reference temperature

$B_{T0/T1}$： Constant specified for the thermistor (B constant)

The B constant present in this equation has the temperature characteristics, and is not strictly constant. Since the B constant is specified at 25°C/50°C for ROHM's SiC power module, the error is increased as the thermistor temperature moves away from 50°C.

If the resistance value adjusted to the operating temperature is necessary, a rough estimation can be calculated by referring to Figure 6-3. If detailed data for the temperature and resistance values are necessary, contact our representative.

However, pay attention to the following points if you use the thermistor mounted inside the module.

- The thermistor is mounted on the isolation substrate and is not located on the heat radiation path. (A certain thermal resistance exists between the thermistor and the semiconductor junction.)
- The relation between Tj and the thermistor temperature depends on the external cooling condition. (Same as above.)
- The temperature cannot be measured in the transient state.

A reference circuit for the temperature detection is shown in Figure 6-4.

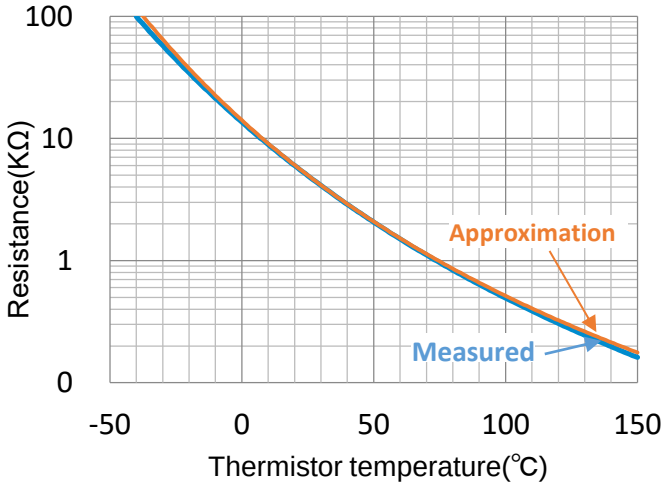


Figure 6-3. Thermistor temperature characteristics

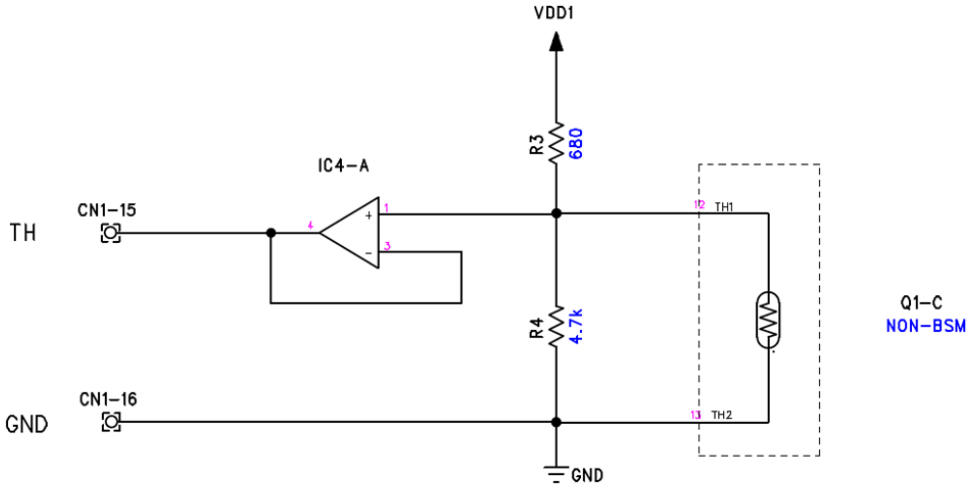


Figure 6-4. Example of temperature monitoring circuit

6.4 Installation method for power module

6.4.1 Installation of heatsink

The power module is equipped with a heatsink for cooling. Its structure is designed so that the module can be tightened at a constant torque with the installation screws. Figure 6-5 shows the cross section of the structure of the power module. Since the solder, wiring pattern, isolation substrate, and so on, are present between the chip of the SiC MOSFET and the base plate, it is extremely important to install the heatsink to on the base plate correctly.

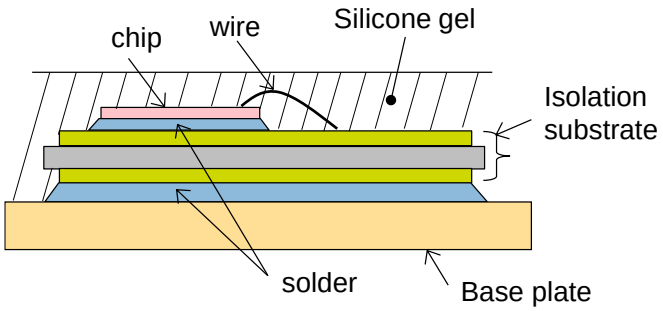


Figure 6-5. Structure of base plate of power module (cross section)

When installing the heatsink, caution must be taken regarding the contact between the base plate and the heatsink and its evenness. Although the base plate of the power module appears even, it is actually warped due to the stress generated during the assembly of the power module. Figure 6-6 shows the warped shape of the base plate. The power module is warped by approximately 38 μm at maximum in the cross section along the long side direction, having a complex and irregular shape. Therefore, when tightening the power module to the heatsink, a gap always occurs between the heatsink and the base plate. Furthermore, even when the shape of the base plate is a simple convex, a gap occurs similarly if the installation surface of the module or the heatsink is scratched. This gap hinders the heat radiation from the power module to the heatsink, leading to heat generation exceeding the temperature expected in the heat radiation design.

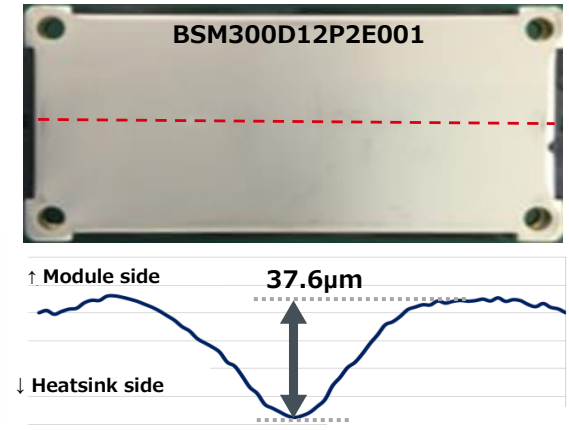


Figure 6-6. Warping of base plate

Although thermal sheets and thermal grease are used to fill this gap, there are several points that should be noted.

On one hand, the thermal sheet is easy to handle due to its solid form. On the other hand, however, its application requires significant caution because the torque strength required for assembly is large (e.g., 8 N·m) and it exceeds the rating for the power module (3.5 N·m). In contrast, since the thermal grease is fluid, it can be used at a torque strength within the rating for the power module. However, it is difficult to control the thickness and the grease may flow due to temperature change (pump-out phenomenon), resulting in a void or gap. Therefore, the materials should be selected carefully.

For more details on the assembly method using the thermal grease and the effect of heat radiation, refer to Application Note “Optimized heat sink assembly method for effective heat dissipation”*5.

6.4.2 Installation of signal wires

To have the power module perform the switching operation or to sense the internal temperature, it is necessary to connect the control signal wires to the signal terminals of the power module (Figure 6-7).

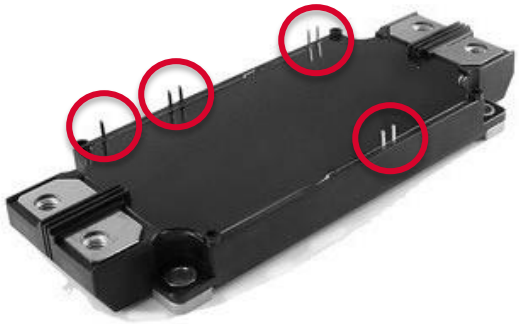
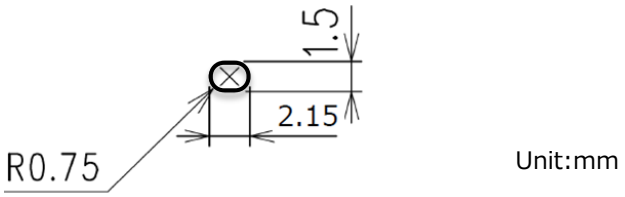


Figure 6-7. Signal terminals of power module

The methods for connecting the signal wires to these signal terminals include solder connection with a PCB and fitting connection via a contact. However, when a signal terminal is soldered, the through-hole prepared on the PCB side must have the finished diameter indicated in Figure 6-8 (a).

In addition, when a signal terminal is connected via a contact, evaluation can be performed using the contact indicated in Figure 6-8 (b). However, these parts are intended to be used for evaluation of the functions of the power module, and the reliability regarding the number of times of insertion and removal or vibration is not evaluated. If these parts are used in the customer's final products, be sure to evaluate the reliability under the conditions corresponding to each application and judge whether or not they can be used.



(a) Example of through-hole for signal terminal on drive board

(b) Example of contact (Hirose Electric HIF3 series)

Figure 6-8. Connection method of signal terminal

The solder connection must be manually performed with a soldering iron under the following conditions. In addition, the soldering should not be performed with reflow.

- Soldering iron tip temperature: 400°C or less
- Soldering time: 5 seconds or less

6.5 Switching characteristics

The switching characteristics of a SiC power module (BSM120D12P2C005, 1,200 V and 120 A, C-type package) were evaluated with the double pulse test at the inductance load indicated in Figure 6-9. The parasitic inductance inside the module is approximately 25 nH, and the parasitic inductance of the circuit is approximately 15 nH.

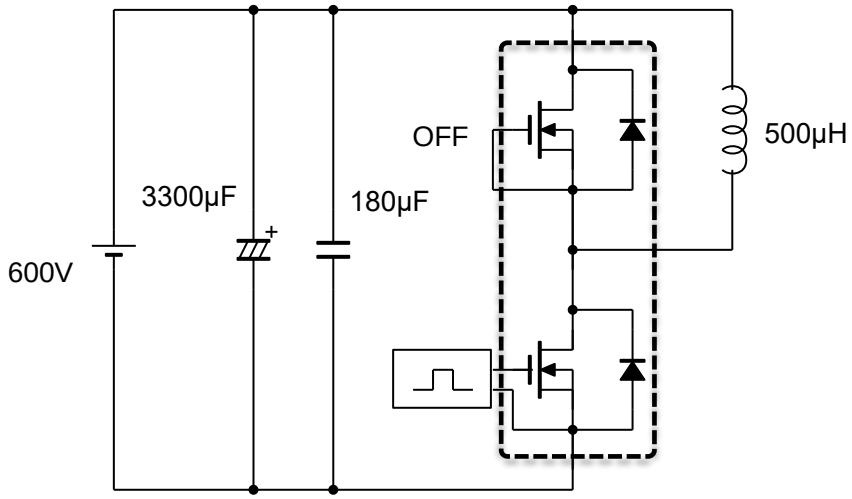
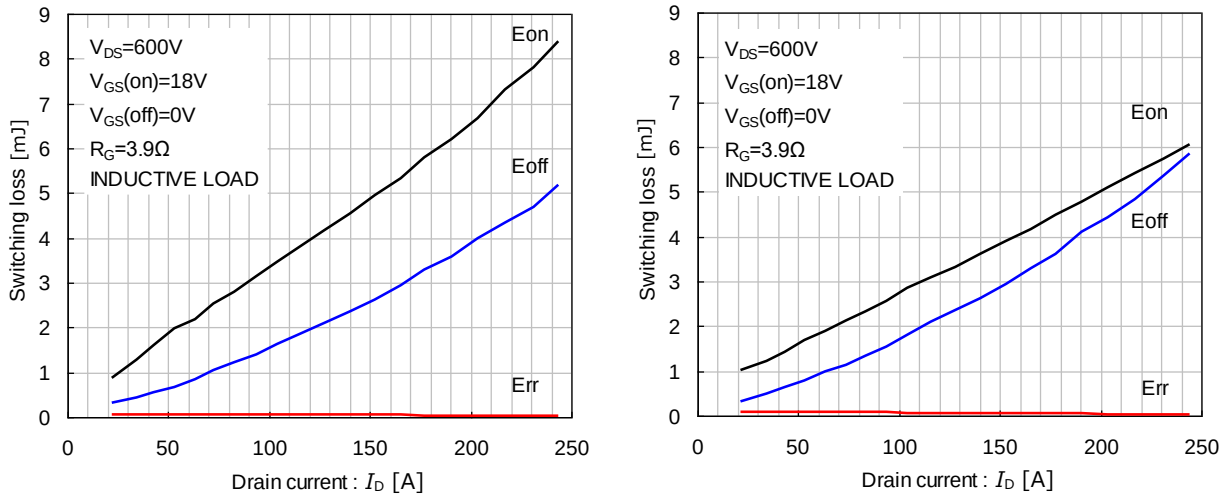


Figure 6-9. Double pulse test circuit

6.5.1 Drain current dependence and temperature dependence

In the SiC power modules, the recovery loss (Err) is nearly zero thanks to the high speed recovery performance of the SBD (or the body diode of the MOSFET). In addition, since there is no tail current in the MOSFET, the SiC power module features a very small Eoff compared with the IGBT. Eon and Eoff tend to increase almost in proportion to the current (the trend of increase depends on the external R_G). While the recovery current in the Si FRD and the tail current in the IGBT increase at higher temperature, change in the losses with temperature is very small in the SiC module, which is configured with the majority carrier devices. Since the threshold decreases at higher temperature, Eon tends to decrease and Eoff tends to slightly increase. (Figure 6-10)



(a) Tj = 25°C

Tj = 125°C

Figure 6-10. Drain current dependence of switching loss

6.5.2 Gate resistance dependence

If the external gate resistance is high, the charge/discharge current to the gate decreases and the switching is decelerated. Accordingly, Eon and Eoff increase and the original performance may not be realized. Select the smallest gate resistance possible. (Figure 6-11)

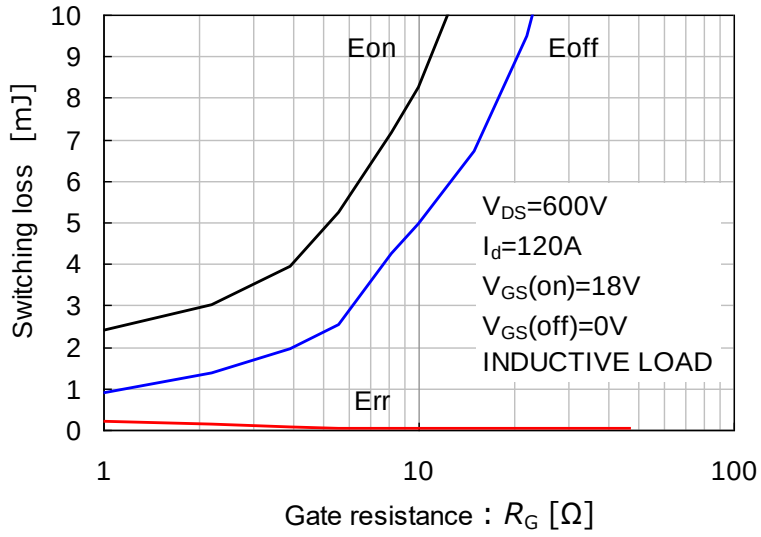


Figure 6-11. Gate resistance dependence of switching loss (Tj = 25°C)

The dependence of d*V*/d*t* and d*I*/d*t* on the external gate resistance is as shown in Figures 6-12 and 6-13. By reducing the external gate resistance, both d*V*/d*t* and d*I*/d*t* are increased. Although ROHM's SiC power modules are tested under various conditions, no mode of d*V*/d*t* failure or d*I*/d*t* failure has been confirmed in the investigations so far.

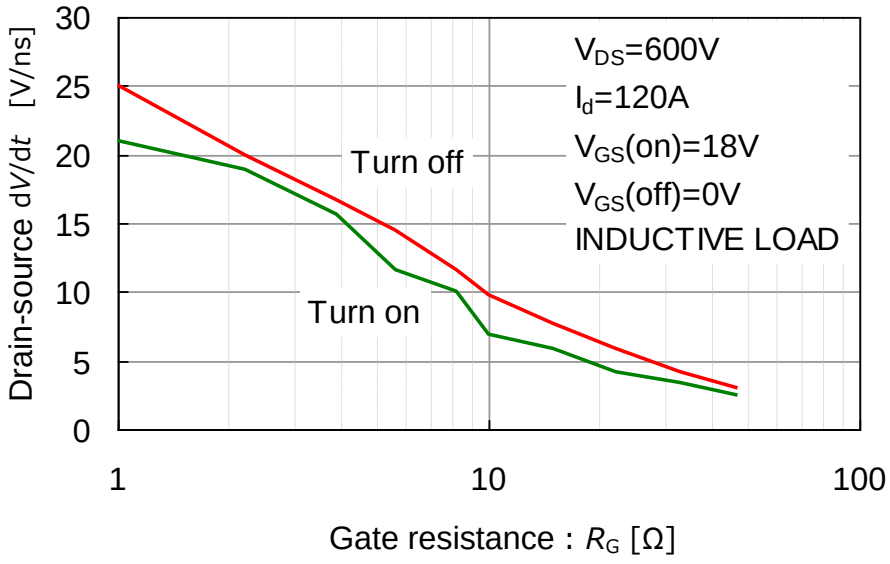


Figure 6-12. d*V*/d*t* vs. gate resistance (Tj = 25°C)

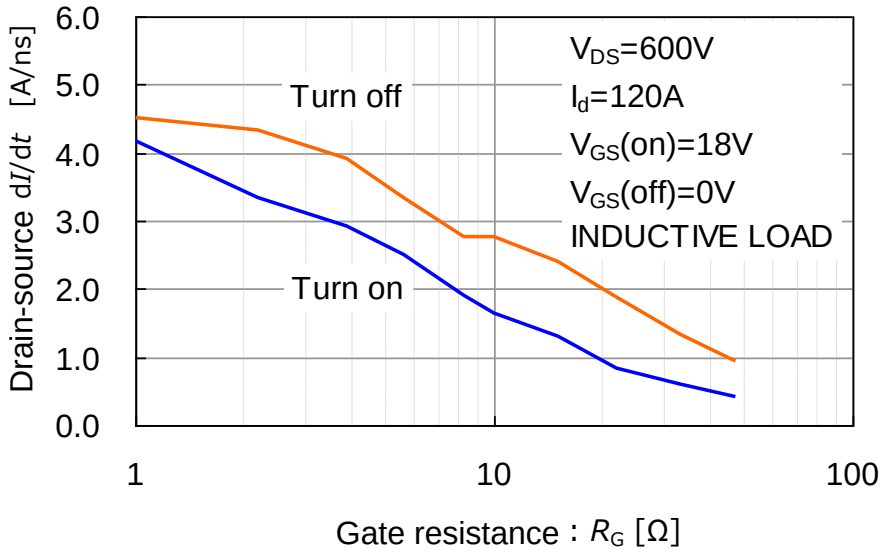


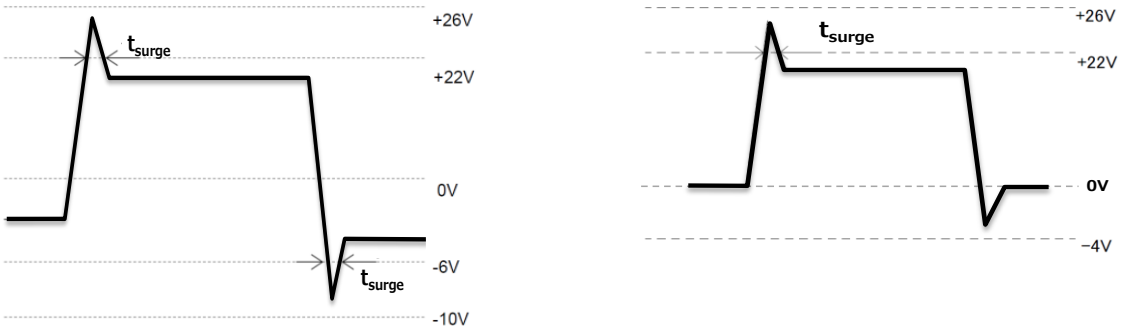
Figure 6-13. d*I*/d*t* vs. gate resistance (Tj = 25°C)

6.5.3 Gate bias dependence

The V_{GS} rating for modules using the second generation SiC MOSFET ranges from -6 to +22 V. The V_{GS} rating includes the surge rating that is specified with the pulse width (t_{surge}) of 300 ns or less and ranges from -10 to +26 V [Figure 6-14 (a)]. The recommended driving conditions are $V_{GS(on)}$ = 18 V and $V_{GS(off)}$ = 0 V or up to -5 V when the negative bias is used. However, as the absolute values of $V_{GS(on)}$ and $V_{GS(off)}$ increase, the charge/discharge of the gate is accelerated and Eon and Eoff tend to decrease.

In contrast, the V_{GS} rating of modules using the third generation SiC MOSFET ranges from -4 to +22 V, and the surge rating ranges from -4 V to +26 V [Figure 6-14 (b)]. The recommended driving conditions are $V_{GS(on)}$ = 18 V and $V_{GS(off)}$ = 0 V.

Both of the second and third generation modules cannot be guaranteed against surges exceeding the rating. Use the modules within the rated range.



(a) Second generation module (b) Third generation module

Figure 6-14. V_{GS} surge rating

6.6 Comparison of switching loss with IGBT module

The results of comparing the switching performances of the IGBT modules (products available from three different companies, 1,200 V and 100 A class, 2 in 1 configuration) and the SiC power modules are shown in this section.

6.6.1 Comparison of total switching loss

If the gate resistance is selected appropriately, the total switching loss (Eon + Eoff + Err) in the SiC power module can be reduced by 85% compared with the IGBT module having the smallest loss (Figure 6-15). This enables driving at 50 kHz and higher, which cannot be achieved in the IGBT modules conventionally. As a result, the passive components such as reactors can be downsized. In addition, the IGBT modules usually have a problem with heat generation due to the switching loss and can be used with a current only around a half of the rated current. However, the SiC modules having a small switching loss can be used without derating the current significantly even when being driven at high frequency. In other words, the SiC modules can replace the IGBT modules with a larger current rating.

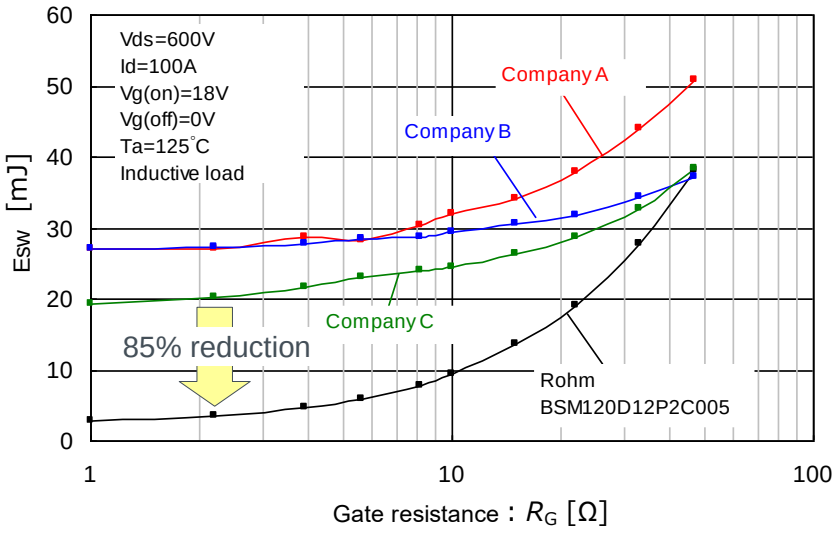


Figure 6-15. Comparison of total switching loss

6.6.2 Comparison of recovery loss (Err)

In the IGBT modules, a large loss occurs due to a large reverse recovery peak current (*I*rr) and a long reverse recovery time (*t*rr) of the FRD. In contrast, *I*rr and *t*rr of the SiC SBD are very small and the loss is negligible (Figure 6-16).

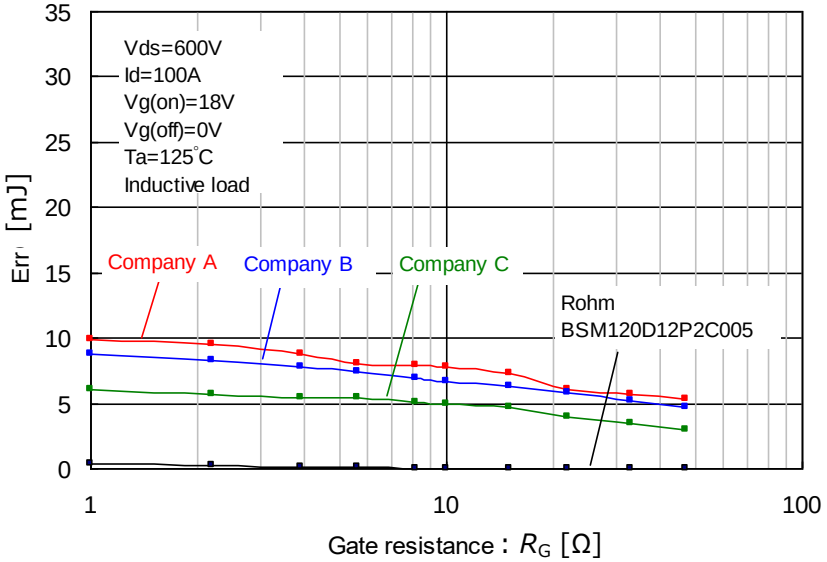


Figure 6-16. Comparison of recovery loss

6.6.3 Comparison of turn ON loss (Eon)

The recovery current generated on the commutation side arm side penetrates into the opposite side arm side, increasing the turn ON loss in the switching device. As in the case of the recovery loss, the turn ON loss is reduced in the SiC power modules in which the recovery of the diode is fast. The lower the external gate resistance, the smaller the loss (Figure 6-17).

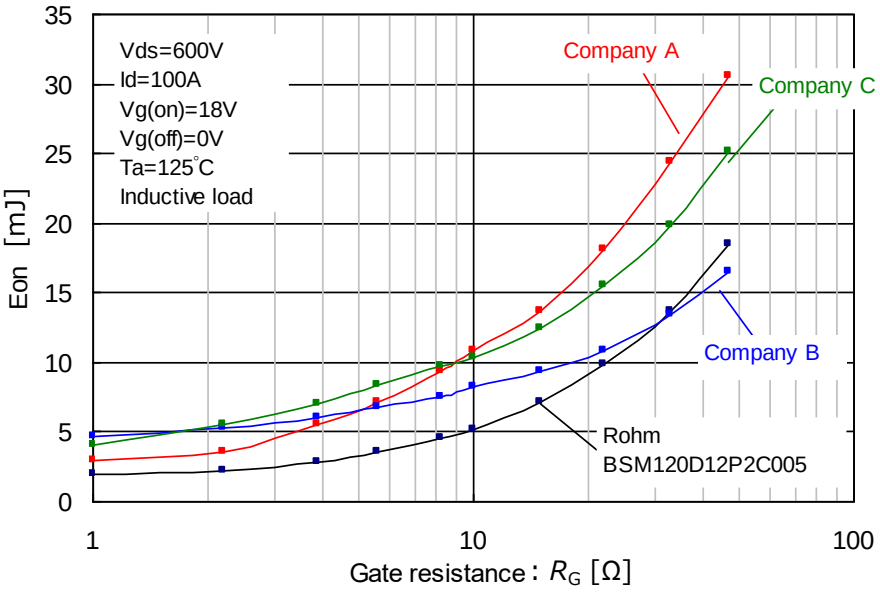


Figure 6-17. Comparison of turn ON loss

6.6.4 Comparison of turn OFF loss (Eoff)

Since the turn OFF loss in the IGBT is caused by the tail current, the gate resistance dependence doesn't appear noticeable, always having a large value. In contrast, since no tail current exists in the SiC MOSFET in principle, a very fast and low loss switching can be realized. The lower the external gate resistance, the smaller the loss (Figure 6-18).

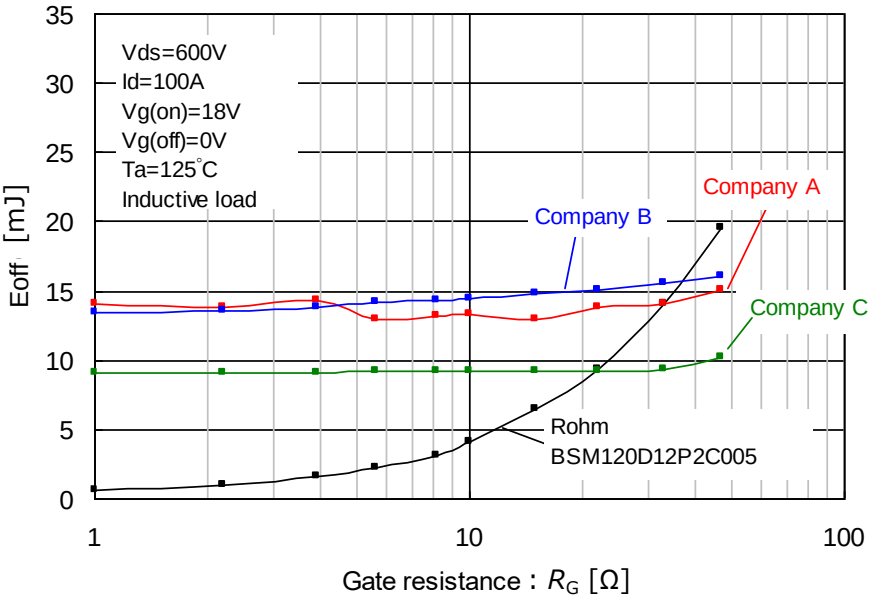


Figure 6-18. Comparison of turn OFF loss

6.7 Countermeasure against self-turn-on

In half bridge structures, when the MOSFET (M1) on the upper arm is turned ON, the reverse recovery of the forward current that has flowed through the commutation diode (external SBD or body diode) of the MOSFET (M2) on the lower arm occurs, and the potential between the drain and source of M2 increases simultaneously. dV_{DS}/dt generated at this point causes a transient gate current via the reverse transfer capacitance (Crss) of M2 (I_G = Crss × dV_{DS}/dt). As this current flows into the gate resistance, the gate voltage of M2 is increased (Figure 6-19). If this voltage significantly exceeds the gate threshold voltage ($V_{GS(th)}$), the self-turn-on of the MOSFET (M2) occurs, causing short-circuit of the upper and lower arms.

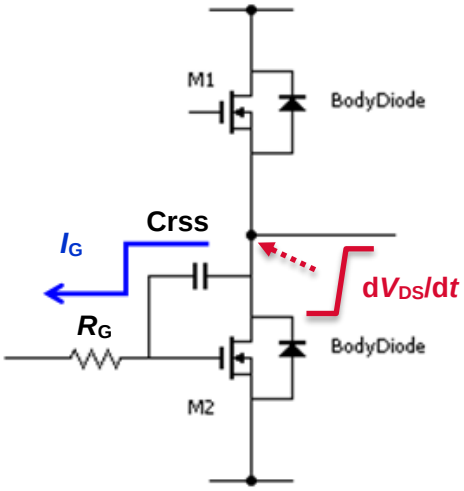


Figure 6-19. Generation mechanism of self-turn-on

In the SiC MOSFET, $V_{GS(th)}$ is low around 3 V because it is defined by I_D equaling a few mA. However, the gate voltage required to pass a large current is high over 8 V, and the tolerance against self-turn-on is not significantly different from the IGBT. However, if self-turn-on is possible in the operating condition, the following countermeasures are recommended similar to the Si power module. Since these countermeasures may affect the switching, make adjustments while checking the waveforms. For the countermeasures against self-turn-on using the active miller clamp, also refer to Application Note “Self-turn-on countermeasure by using active miller clamp”*6, which provides more information.

- Increase the negative bias during OFF (possible for the second generation MOSFET only)
- Add capacitance between the gate and the source
- Add a transistor between the gate and the source (clamp between gate and source using the active miller clamp MOSFET)
- Increase the gate resistance to decelerate the switching

6.8 RBSOA (reverse bias safe operating area)

The RBSOA (reverse bias safe operating area) of the SiC power modules covers the entire range that 200% of the rated current multiplied by the rated voltage, similar to the IGBT modules (Figure 6-20).

The drain-source voltage indicated here is the value in the immediate vicinity of the chip (V_{DS_INT}), but not the terminal voltage (V_{DS}). From the parasitic inductance (Ls) specified for each power module and dI_D/dt of the actual waveform, calculate V_{DS_INT} indicated in Equation (5).

$$V_{DS\_INT} = V_{DS} + L_S * \frac{dI_D}{dt} \quad (5)$$

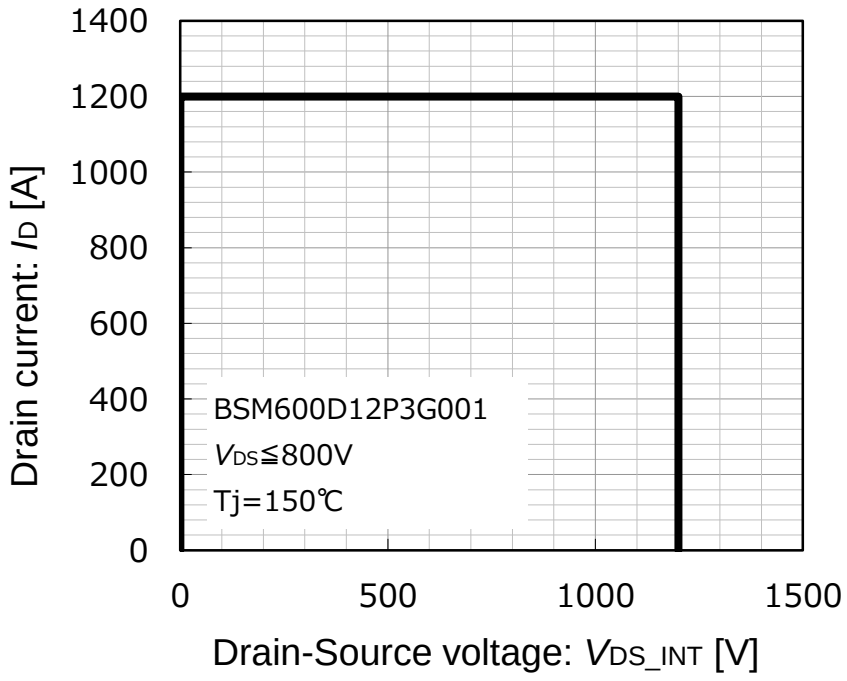
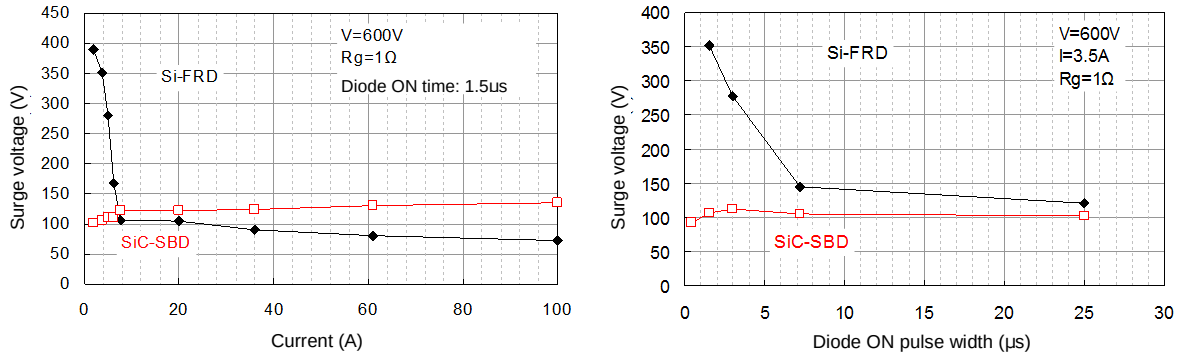


Figure 6-20. RBSOA of 1,200 V and 600 A product

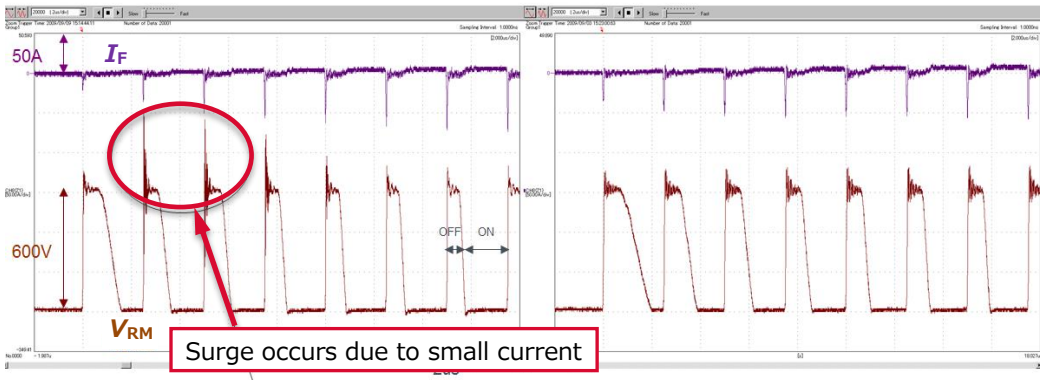
6.9 V_{DS} surge of diode conducting narrow pulse of small current

In the Si FRD, the minority carriers stored in the drift layer decrease when the electrical conduction time is short and the current is small. As a result, d*i*/d*t* of the return of recovery is increased, generating a high surge voltage as indicated with black lines in Figure 6-21 (a) and (b). The surge voltage of the diode is increased as the turn ON of the MOSFET is accelerated, possibly damaging the elements and causing noise. Therefore, it is necessary to limit and slow down the turn ON. In contrast, since the minority carriers are not used and the recovery current is very small in the SiC SBD, a high surge voltage will not occur even under the small current and short pulse conditions as indicated with red lines in (a) and (b). Since it is unnecessary to limit the turn ON speed of the MOSFET, the switching loss can be reduced. A comparison of the V_{DS} surge waveforms when the short pulse operation of diodes is performed is shown in Figure 6-22.



(a) I_F VS. Surge Voltage (b) I_F pulse width VS. Surge Voltage

Figure 6-21. V_{RM} surge characteristics



(a) Si IGBT + Si FRD (b) SiC MOSFET + SiC SBD

Figure 6-22. Comparison of voltage surge due to recovery current under small current and short pulse

6.10 G-type power module

In general, power modules have a large parasitic inductance due to their large size and internal structure. Since the inductance of wiring and the like can cause a surge voltage through the high dI_D/dt of the switching current, it is desirable to reduce the inductance as much as possible.

ROHM has developed the G-type power module, in which the internal inductance is reduced as much as possible. In addition, the thermal resistance (R_{th}) of the module has also been improved, doubling the allowable current by improving the heat radiation ability. Figure 6-23 shows the external views and rough estimations of the internal inductance.

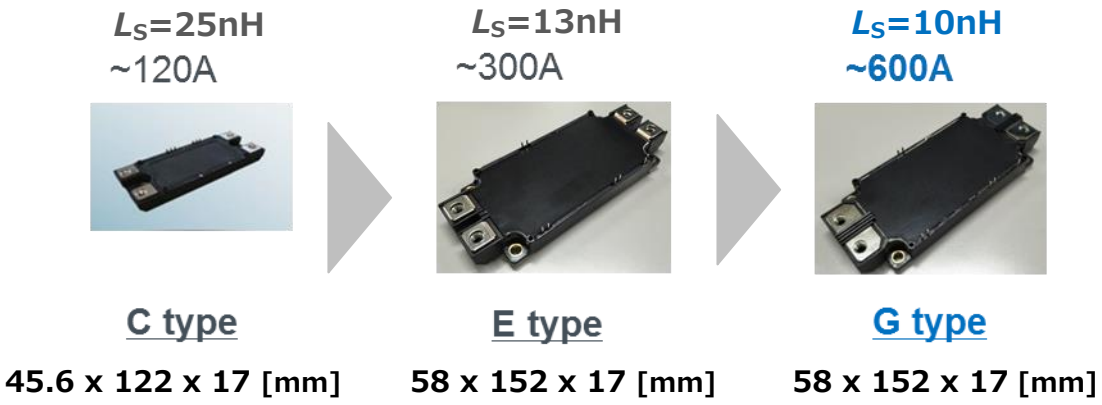
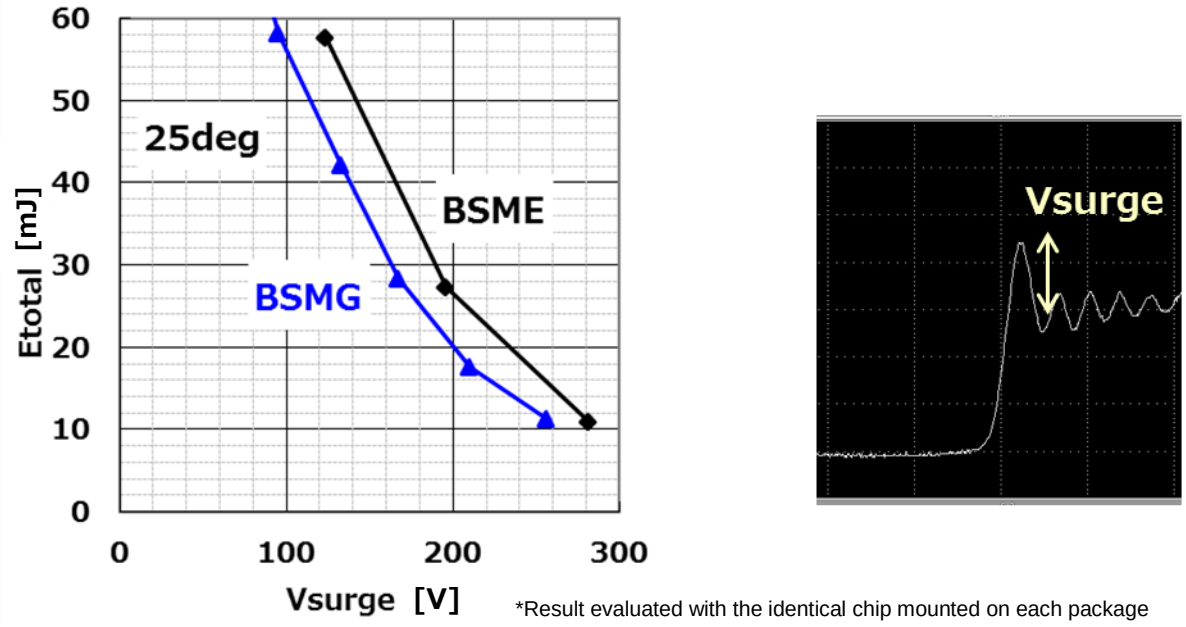


Figure 6-23. Case type of power module

Figure 6-24 shows the result of the comparison for the V_{DS} surge during turn OFF between the G- and E-types. Since the internal inductance is reduced in the G-type, the occurrence of a surge voltage can be limited under the same driving condition. From a different point of view, if the power modules are operated under the switching conditions that result in the same surge voltage (reducing the external gate resistance of the G-type), the loss can be reduced by approximately 25% compared with the E-type.



*Result evaluated with the identical chip mounted on each package

Figure 6-24. Comparison of V_{DS} surge and switching loss between G- and E-types

7. Evaluation board for module

7.1 Drive board for SiC power module

A list of the drive boards for SiC power modules released by ROHM is shown in Table 7-1. These drive boards are equipped with the basic functions for driving the power modules, isolated power supply for driving, over current protection circuit, and so on, as standard features. Therefore, they can be used to drive the power modules by only preparing a single power supply for control.

For more detailed information, refer to the SiC support page on ROHM's website (https://www.rohm.co.jp/power-device-support).

Table 7-1. List of drive boards for SiC power modules

Device under evaluation	External design	Product name
BSM series For second generation 1200 V E-/G-type		BSMGD2G12D24-EVK001
BSM series For third generation 1200 V E-/G-type		BSMGD3G12D24-EVK001
BSM series For second and third generations 1200 V C-type		BSMGD3C12D24-EVK001
BSM series For second generation 1700 V E-type		BSMGD2G17D24-EVK001

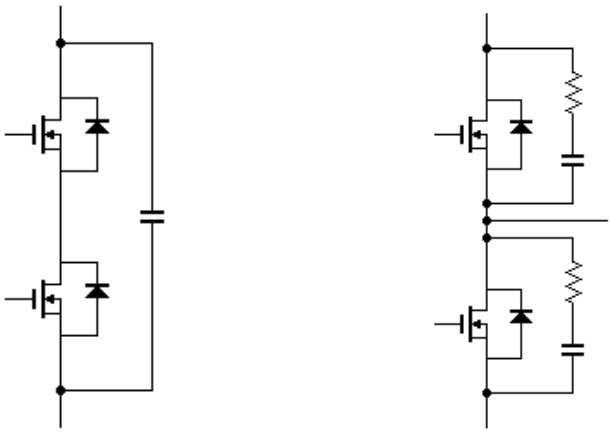
Since these drive boards have been developed for evaluations over a short period, no guarantee of their reliability is provided and no adequate creepage distance, and so on, is ensured. If the circuit diagrams and the board layouts of these drive boards are transferred to your boards, be sure to verify the reliability yourself.

7.2 Countermeasures against surge voltage

The SiC modules have a fast switching speed and handle a large current. Therefore, the wire inductance inside the module or in its surrounding (L_{LINE}) may cause the surge voltage ($V_{SURGE} = -L_{LINE} \times dI_D/dt$), which can exceed the rated voltage.

To suppress such surges, the following countermeasures are recommended similar to the Si power modules. However, since these countermeasures may affect the switching characteristics, make adjustments with an actual circuit while checking the waveforms.

- Design the wiring of the main circuit (and snubber circuit) as thick and short as possible to reduce the wire inductance.
- Place the mounting position of the smoothing capacitor close to the MOSFET to reduce the wire inductance.
- Add a snubber circuit.
- Increase the gate resistance to reduce dI_D/dt.



(a) C snubber circuit (b) RC snubber circuit

Figure 7-1. Snubber circuit for power module

Figure 7-2 shows the difference in the V_{DS} waveforms due to the presence or absence of the C snubber and the types of the capacitor. By installing an appropriate ceramic capacitor, the surge voltage and the ringing can be reduced. ROHM provides the snubber boards ideal for evaluations of high speed SiC modules, as shown in Figure 7-3. For more details, refer to the information on the SiC support page on ROHM's website (https://www.rohm.co.jp/power-device-support).

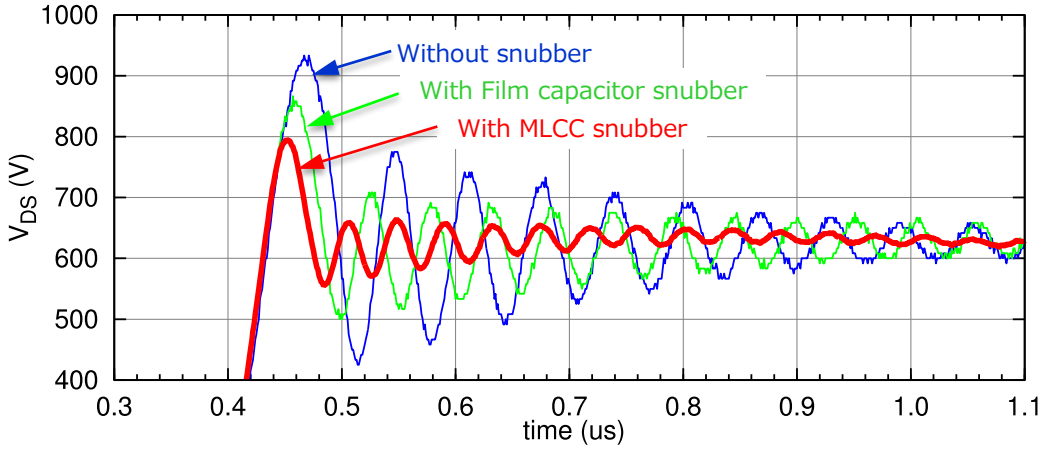
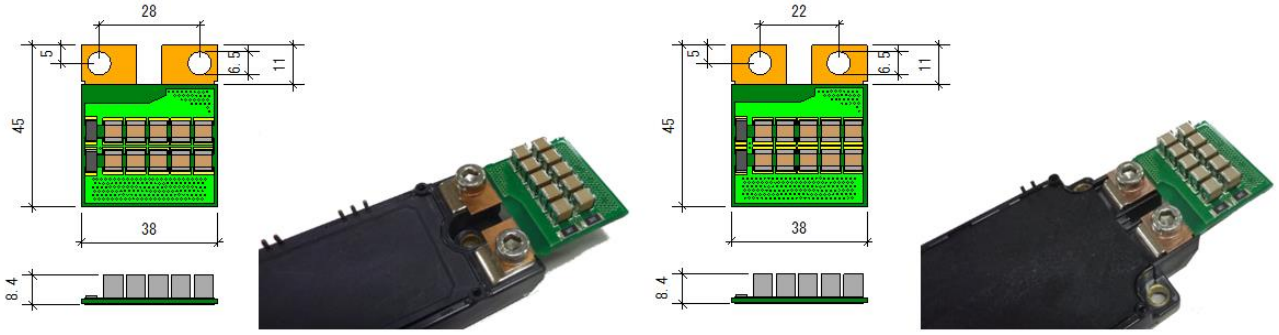
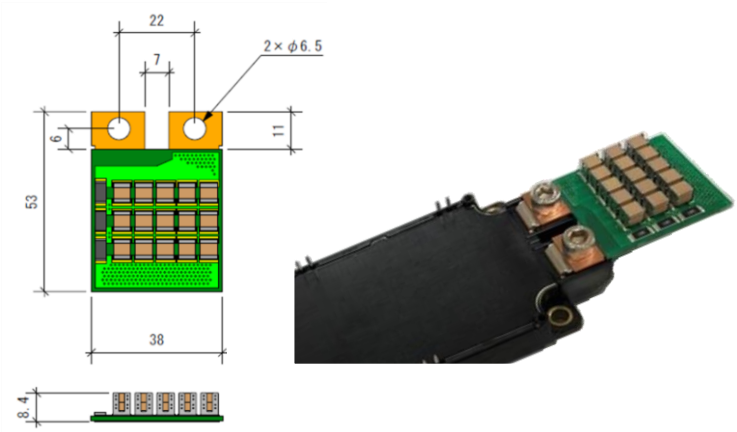


Figure 7-2. Comparison of turn OFF surge waveforms due to presence or absence of snubber circuit



(a) EVSM1D72J2-145MH26 for C-type (b) EVSM1D72J2-145MH16 for E-type



(c) EVSM1D72J3-934MH93 for 1,700 V

Figure 7-3. Snubber board for SiC power module

8. Reliability

Since the SiC power devices are used for industrial equipment with a generally long product life, the device performance should be maintained over a long period. Furthermore, since they are often used in an environment subjected to very large thermal and electrical stress, they must be evaluated under various conditions and the required period for maintaining the performance must be secured (life design).

Ideally, the reliability should be evaluated under the stress conditions to which the devices will be subjected in the operating environments. However, since the products with a product life over 10 years cannot be evaluated under the exact same conditions, alternative testing methods, such as the accelerated test, are generally used. In this case, it is important to understand the operating environments correctly and set the conditions including the acceleration accordingly.

This chapter explains the reliability items that must be particularly noted for each device. For general items of the reliability test, “JEITA Standard ED-4701” and “JEDEC Standard JESD22-A102” are complied with and implemented.

8.1 Reliability of SiC SBD

8.1.1 d*V*/d*t* failure and d*I*/d*t* failure

In conventional products, a mode has been confirmed in which the peripheral structure of the SiC SBD is damaged if a large d*V*/d*t* is applied. In ROHM’s SBD, however, this failure mode has not been confirmed in the investigations so far even with the operation around 50 kV/μs.

Furthermore, in the Si FRD, there is a mode in which the recovery current (Irr) is increased if d*I*/d*t* is large, damaging the device through the current concentration. In contrast, since the recovery current in the SiC SBD is very small, this mode can be considered unlikely.

8.1.2 Result of reliability test for SiC SBD

Tables 8-1 and 8-2 show the results of the reliability tests for the through-hole type and the SMD type, respectively.

Table 8-1. Result of reliability test for through-hole type

(a) Life test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
High Temperature Reverse Bias	$T_a = T_{jmax}$, $V_R = V_{Rmax} \times 0.8$ JEITA ED-4701/100A-101A	1000 h	22	0
Temperature humidity bias	T_a= 85℃, RH = 85%, V_R= 100 V JEITA ED-4701/100A-102A	1000 h	22	0
Temperature cycle	T_a = -55℃ (30 min) ～ T_a = 150℃ (30 min) JEITA ED-4701/100A-105A	100 cycles	22	0
Pressure cooker	T_a = 121℃, 203 kPa [2 atm], RH = 100% JESD22-A102C	48 h	22	0
High Temperature storage	T_a = 175℃ JEITA ED-4701/200A-201A	1000 h	22	0
Low Temperature storage	T_a = -55℃ JEITA ED-4701/200A-202A	1000 h	22	0

(b) Stress test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
Resistance to solder heat 1	Dipping leads into solder bath at 260 ±5℃. JEITA ED-4701/301-302A	10 s	22	0
Resistance to solder heat 2	Dipping leads into solder bath at 350 ±10℃. JEITA ED-4701/301-302A	3.5 s	22	0
Solderability	Dipping into solder bath at 245 ±5℃. JEITA ED-4701/301-303A	5 s	22	0
Thermal shock	$0\ ^{+5}_{-0}$ (5 min) ～ $100\ ^{+0}_{-5}$ (5 min) JEITA ED-4701/302-307B	100 cycle	22	0
Terminal strength (Pull)	Pull force = 20 N JEITA ED-4701/400A-401A	10 s	22	0
Terminal strength (Bending)	Bending Load = 10 N JEITA ED-4701/400A-401A	2 times	22	0

• Failure criteria :
According to the electrical characteristics specified by the specification. Regarding solderability test, failure criteria is 95% or more area covered with solder.
・Sample standard:
[Reliability level: 90%][Failure reliability level(λ1): 10%][C=0 And the number of samples is being made 22 in accordance with single sampling inspection plan with exponential distribution type based on MIL-STD-19500.

Table 8-2. Result of reliability test for SMD type

1. Life Test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
High Temperature Reverse Bias	$T_a = T_{jmax}$, $V_R = V_{Rmax} \times 0.8$ JEITA ED-4701/100A-101A	1000 h	22	0
Temperature humidity bias	T_a= 85℃, RH= 85%, V_R= 100 V JEITA ED-4701/100A-102A	1000 h	22	0
Temperature cycle	T_a = -55℃ (30 min) ～ T_a = 150℃ (30 min) JEITA ED-4701/100A-105A	100 cycles	22	0
Pressure cooker	T_a = 121℃, 203 kPa [2 atm], RH= 100% JESD22-A102C	48 h	22	0
High Temperature storage	T_a = 175℃ JEITA ED-4701/200A-201A	1000 h	22	0
Low Temperature storage	T_a = -55℃ JEITA ED-4701/200A-202A	1000 h	22	0

2. Stress Test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
Resistance to solder heat 1	Reflow at 260 ±5℃(peak temperature). JEITA ED-4701/301-301C	2 times	22	0
Resistance to solder heat 2	Dipping into solder bath at 260 ±5℃. JEITA ED-4701/301-301C	10 s	22	0
Resistance to solder heat 3	Dipping leads into solder bath at 350 ±10℃. JEITA ED-4701/301-301C	3.5 s	22	0
Solderability	Dipping into solder bath at 245 ±5℃. JEITA ED-4701/301-303A	5 s	22	0
Thermal shock	$0\ ^{+5}_{-0}$ (5 min) ～ $100\ ^{+0}_{-5}$ (5 min) JEITA ED-4701/302-307B	100 cycle	22	0
Terminal strength (Pull)	Pull force = 20 N JEITA ED-4701/400A-401A	10 s	22	0

• Failure criteria :
According to the electrical characteristics specified by the specification. Regarding solderability test, failure criteria is 95% or more area covered with solder.

・Sample standard:
[Reliability level: 90%][Failure reliability level(λ1): 10%][C=0 And the number of samples is being made 22 in accordance with single sampling inspection plan with exponential distribution type based on MIL-STD-19500.

8.2 Reliability of SiC MOSFET

Since the chip structure of the SiC MOSFET is more complex than that of the SBD, the reliability test must be performed in anticipation of various types of external stress including thermal, electrical, and mechanical ones. In addition, since the factor is often compounded under the actual operating conditions, it is important to evaluate the reliability under the closest conditions possible to the actual use.

This chapter compares the reliability of the SiC MOSFET with that of the Si MOSFET, which has already been refined through many years of market application, and explains the potential of the SiC MOSFET.

8.2.1 Gate oxide film

The reliability of the gate insulating film formed on SiC had been questioned over many years. However, through the development of the gate oxide film formation process and the optimization of the device structure, ROHM has achieved quality equivalent to the widely used current Si MOSFET and IGBT.

Figure 8.1 shows the result of the CCS TDDB (constant current stress time dependent dielectric breakdown) test. In the CCS TDDB test, the tunnel current is forcibly passed through the gate oxide film and the amount of electric charge per unit area that has been passed through the film before a failure occurs is judged. As an indicator of the quality of the gate oxide film, Q_{BD} is 15 to 20 C/cm^2. Therefore, strength equivalent to the Si MOSFET is obtained.

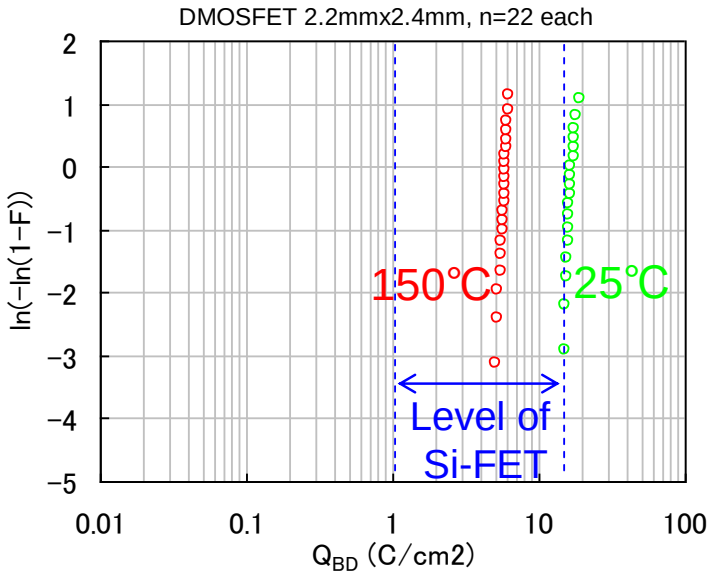


Figure 8-1. CCS TDDB (24mA/cm^2)

Even with the high quality of the gate insulating film, many crystal defects remain in SiC crystals, and there were concerns about initial failures due to these crystal defects. ROHM is making an effort to prevent product with initial failures from being delivered to the market by employing a unique screening technology.

Based on the result of the HTGB (high temperature gate bias) test (+22 V, 150°C/175°C), it has been confirmed with a total of more than 3,000 devices that 1,000 hours have passed without a failure or variation in the characteristics. In addition, it has also been confirmed with more than 600 devices that 3,000 hours have passed without a problem.

8.2.2 Threshold stability (gate positive bias)

With the current level of technology, traps are formed on the interface of the gate insulating film formed on SiC. If the gate positive bias is applied with DC for a long time, electrons are captured in the traps and the threshold is increased. However, this shift in the threshold is very small around 0.2 to 0.3 V with V_{GS} = +22 V and 150°C after 1,000 hours. This is the lowest level in the industry. Since most of the traps are completely filled within several tens of hours after the stress is initially applied, the threshold remains stable without variation after that. Figure 8-2 shows the test result with V_{GS} = 22 V for the second generation SiC MOSFET.

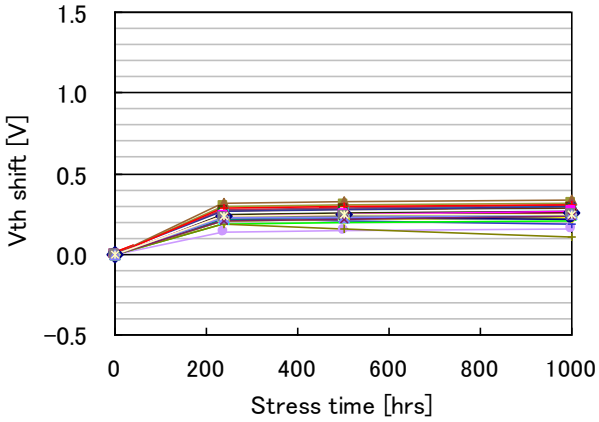


Figure 8-2. HTGB (V_{GS}=+22V, 150℃)

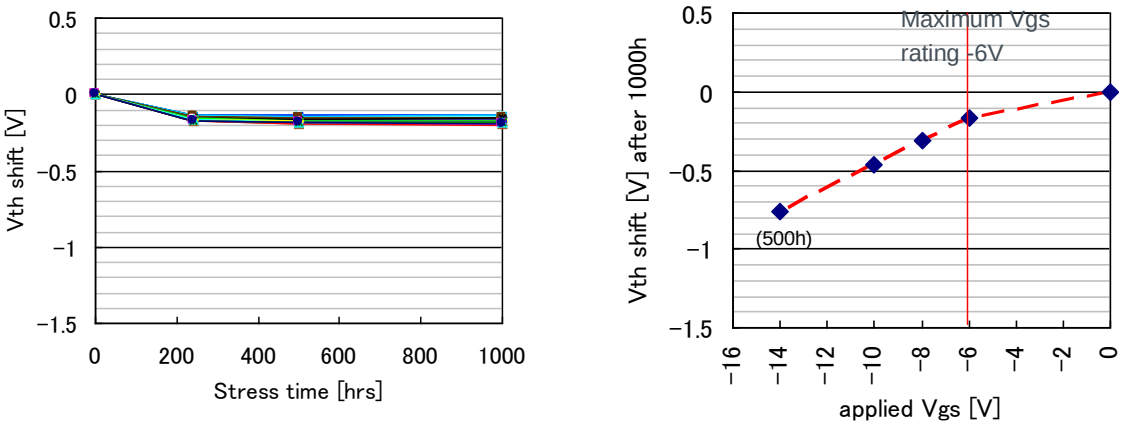
8.2.3 Threshold stability (gate negative bias)

If the negative bias is applied with DC for a long time, holes are also trapped and the threshold is decreased. In the case of the second generation SiC MOSFET, the amount of change in the threshold is larger compared with the case of the positive bias. Since the threshold is decreased by 0.5 V or greater if V_{GS} is -10 V or greater, the guaranteed voltage for the gate negative bias is set to -6 V. Do not use a negative bias larger than the guaranteed voltage, because the threshold will be decreased significantly.

Figure 8-3 shows the result of the reliability test for $V_{GS(th)}$ of the second generation SiC MOSFET. It can be seen that the variation is minimized if V_{GS} is within the guaranteed voltage of -6 V.

Since charging and discharging to the traps are repeated with an AC bias across the positive and negative values, the effect on the threshold shift is known to be small.

In contrast, since the trench gate is employed in the third generation SiC MOSFET, the tolerance against the DC negative bias is improved and the threshold is scarcely decreased even with -10 V DC. However, it should be noted that a new limitation occurs against the AC gate bias as described in the next section.



(a) HTGB (V_{GS}=-6V, 150℃) (b) $V_{GS(th)}$ shift after 1000 hours vs. V_{GS}

Figure 8-3. Result of reliability test for $V_{GS(th)}$ of second generation SiC MOSFET (gate negative bias applied)

8.2.4 Threshold stability (third generation MOSFET)

As described in Section 5.5, the gate rating of the third generation SiC MOSFET is narrower than that of the second generation. If the gate AC drive is performed while the negative bias is larger than the rated voltage (-4 V), a phenomenon appears in which the threshold ($V_{GS(th)}$) gradually increases. Under the conditions in which V_{G_P} = 22 V and V_{G_N} = -4 V to -10 V, the pulses are applied at 300 kHz (duty: 50%). As a result, no problem occurs with the negative bias voltage of -4 V, while $V_{GS(th)}$ is found to suddenly increase with the negative voltage from -6 V to -10 V. Whether or not the threshold will vary is little affected by the duty or the magnitude of the positive voltage, but is determined only by the magnitude of the negative bias (whether or not it exceeds -4 V). Under the condition that allows the threshold to vary (-6 V to -10 V), the speed of the variation depends on the number of the positive and negative biases. Therefore, the characteristics vary earlier as the switching is performed at a higher frequency.

If the increase in the threshold is considerable, $R_{DS(on)}$ is known to increase as well. In addition, regarding the switching loss, Eon tends to increase and Eoff tends to decrease. Although the total switching loss does not change significantly, care must be taken because the ratio of the on and off losses changes. If the change spreads to the conduction loss or the switching loss, the increase in heat generation may be appeared or the device may be damaged in the worst case as a result. Therefore, it is strongly recommended to always use the device within the rating including surges. For the countermeasures for this purpose, refer to Section 5.9 and Application Note “Gate-Source Voltage Surge Suppression Methods”*2.

8.2.5 Short-circuit rating

The SiC MOSFET is a device with a smaller chip area and a higher current density compared with the Si device. Therefore, the tolerance against short-circuit, which is a thermal failure mode, tends to be lower compared with the Si device. The 1,200 V second generation MOSFET of the TO247 package has a sufficient tolerance with V_{DD} = 700 V and the short-circuit endurance time of 10 µs or longer at V_{GS} = 18 V. Since the saturation current decreases with a lower gate voltage, the quantity of generated heat decreases and the endurance time increases. If the supply voltage is low, the endurance time also increases due to reduction in heat generation. Therefore, the 650 V products have a longer endurance time compared with the 1,200 V products.

In the third generation MOSFET, the short-circuit time is further decreased because RonA as FOM is much smaller. However, the short-circuit rating of 5 µs or longer (typical value) is secured for both of the 1,200 V and 650 V products. However, absolute guarantee using measurements and other measures is not performed for the short-circuit rating of the discrete SiC MOSFET.

ROHM’s gate drive ICs with a built-in insulating element can block in approximately 2 µs after over current is detected, and are equipped with functions including the soft turn OFF (for more details, check the data sheet for each model). Since the time required for turning OFF the SiC MOSFET is extremely short, if the speed of blocking V_{GS} is fast, a sudden d*I*/d*t* may cause a high surge voltage. Use functions such as the soft turn OFF, which can decrease the gate voltage gradually, in order to block with a condition where over voltage will not be applied.

8.2.6 d*V*/d*t* failure

For the Si MOSFET, there is a mode in which the transient current is passed through capacitance C_{DS} due to the high d*V*/d*t* and the parasitic bipolar transistor operates causing damage to the device.

For the SiC MOSFET, it is thought that the current amplification should not occur due to the small amplification factor of the parasitic bipolar transistor (h_{FE}). This failure mode has not been confirmed in the investigations so far even with the operation around 50 kV/µs.

In addition, during the recovery of the body diode, d*I*/d*t* during the recovery is small due to a very small recovery current in the SiC MOSFET. Consequently, since d*V*/d*t* will not be increased, this failure mode is considered unlikely.

8.2.7 Cosmic ray neutron-induced single-event effects

Damage caused by a collision of a cosmic ray neutron or heavy ion that falls on the Earth's surface in rare cases (SEB: single event burnout) is considered to be the main reason for chance failures in the high breakdown voltage power device. At a high altitude, this is especially a problem because the neutron density can be higher by 10 times or greater than that at sea level. In addition, if multiple large chips, such as power modules, are used, the chance failure rate of the entire set tends to increase. Therefore, it is necessary to select elements with the lowest failure rate possible.

For the 1,200 V third generation SiC MOSFET and the general Si IGBT, Figure 8-4 shows the result of a test irradiating neutrons of which the spectrum simulates the spectrum in the atmosphere while varying the applied V_{DS} (approximately n = 10 for each plotted point). Since the failure rate depends strongly on the applied voltage, derating by around 60% (720 V) of the rated breakdown voltage (1,200 V) was necessary to operate the IGBT at a low failure rate. In contrast, the failure rate of the SiC MOSFET is lower than that of the Si IGBT by more than 4 orders of magnitude, and the failure rate is 1 FIT or less even with V_{DS} = 1,200 V (100% of the rated breakdown voltage). This is attributed to the low probability of colliding with neutrons due to the smaller size of the SiC chip compared with the Si devices and the actual value of the breakdown voltage being high with a sufficient margin, among other reasons. Thus, when the device is used at a high altitude or multiple devices are used as a set, SiC can limitlessly reduce the risk of chance failures induced by cosmic ray without a significant voltage derating.

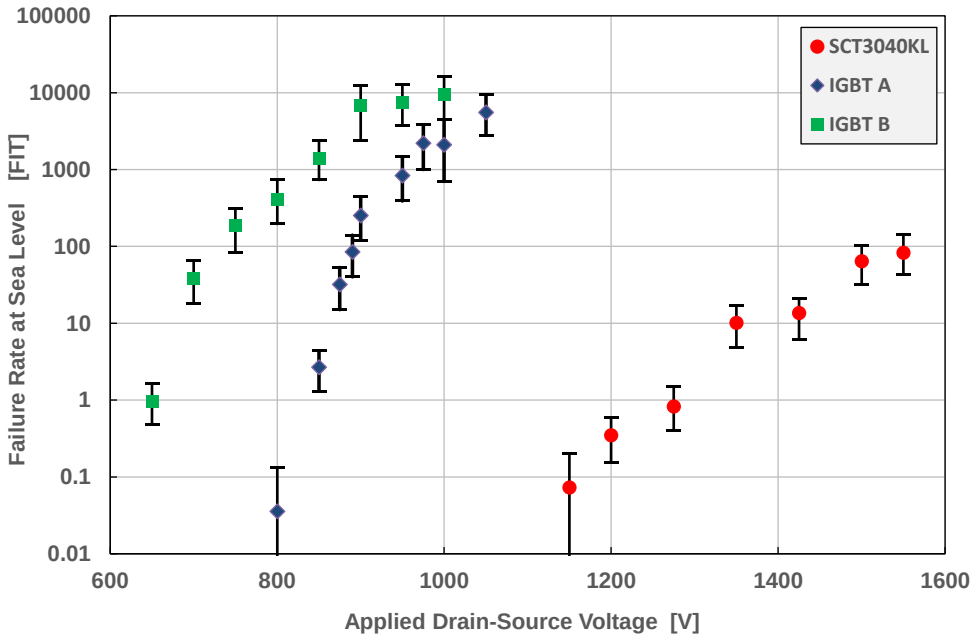


Figure 8-4. Comparison of failure rate due to cosmic ray between the SiC MOSFET (third generation) and IGBT

8.2.8 Electrostatic discharge rating

It is a feature of the SiC MOSFET that the chip can be downsized compared with the Si products. However, the electrostatic discharge rating is decreased. Take ample countermeasures against static electricity and handle the devices with care.

Example of countermeasures against static electricity

- Removal of static electricity from human bodies, devices, and working environments using an ionizer (recommended)
- Removal of static electricity from human bodies and working environments using a wrist band and grounding
  (without other measures, it is insufficient because this measure has no effect against charging in devices)

8.2.9 Cautions for power cycle

If the operation of the MOSFET is switched ON and OFF within a few ms to a few seconds, the junction temperature of the internal chip (Tj) may be varied by a certain width (ΔTj), even when the case temperature (Tc) appears to be constant. ΔTj generated in such a short period causes thermal stress on the bonding surface through difference in the linear expansion coefficient of the source wire and the SiC chip. Then, if the number of ΔTj cycles exceeds a certain value, the interface is cracked and the bonding strength is reduced as shown in Figure 8-5. Finally, separation of the source wire or increase in the contact resistance of the bonding surface can cause $R_{DS(on)}$ to increase, leading to damage to the power device through increase in heat generation.

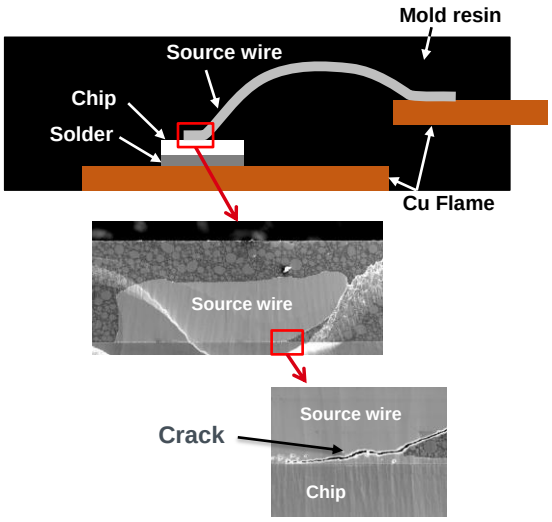


Figure 8-5. Failure mode due to ΔTj power cycle

For the power cycle rating of the source wire, the life tends to shorten exponentially as ΔTj increases. To secure a product life of 10 years or longer, it is necessary to attempt to decrease ΔTj sufficiently (i.e., by adjusting the driving conditions, selecting elements with low $R_{DS(on)}$) as well as the cooling design during the design phase.

Among the general items of the reliability test, the temperature cycle (TCY) and the intermittent conduction (IOL) can cause the solder mainly on the back of the SiC chip to crack due to the swing of the case temperature (ΔTc) for a few minutes to a few hours. These should be distinguished as other failure modes from the power cycle (PCY) due to ΔTj, in which the wire separation occurs.

8.2.10 Result of reliability test for SiC MOSFET

Table 8-3 shows the result of the reliability test.

Table 8-3. Result of reliability test for through-hole type

1. Life Test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
High Temperature Reverse Bias	$T_a = T_{jmax}$, $V_{DS} = V_{DSmax}$ JEITA ED-4701/100A-101A	1000 h	22	0
High Temperature Gate Bias	$T_a = T_{jmax}$, $V_{GS} = V_{GSmax}$ JEITA ED-4701/100A-101A	1000 h	22	0
High Temperature Gate Bias	$T_a = T_{jmax}$, $V_{GS} = V_{GSmin}$ JEITA ED-4701/100A-101A	1000 h	22	0
Temperature humidity bias	T_a= 85℃, RH = 85%, V_{DS} = 100V JEITA ED-4701/100A-102A	1000 h	22	0
Temperature cycle	T_a = -55℃ (30 min) ～ T_a = 150℃ (30 min) JEITA ED-4701/100A-105A	100 cycles	22	0
Pressure cooker	T_a = 121℃, 203kPa [2 atm], RH = 100% JESD22-A102C	48 h	22	0
High Temperature storage	T_a = 175℃ JEITA ED-4701/200A-201A	1000 h	22	0
Low Temperature storage	T_a = -55℃ JEITA ED-4701/200A-202A	1000 h	22	0

2. Stress Test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
Resistance to solder heat 1	Dipping leads into solder bath at 260 ±5℃. JEITA ED-4701/301-302A	10 s	22	0
Resistance to solder heat 2	Dipping leads into solder bath at 350 ±10℃. JEITA ED-4701/301-302A	3.5 s	22	0
Solderability	Dipping into solder bath at 245 ±5℃. JEITA ED-4701/301-303A	5 s	22	0
Thermal shock	0^{+5}_{-0} (5 min) ～ 100^{+0}_{-5} (5 min) JEITA ED-4701/302-307B	100 cycle	22	0
Terminal strength (Pull)	Pull force = 20 N JEITA ED-4701/400A-401A	10 s	22	0
Terminal strength (Bending)	Bending Load = 10 N JEITA ED-4701/400A-401A	2 times	22	0

• Failure criteria :
According to the electrical characteristics specified by the specification. Regarding solderability test, failure criteria is 95% or more area covered with solder.

・Sample standard:
[Reliability level: 90%][Failure reliability level(λ1): 10%][C=0 And the number of samples is being made 22 in accordance with single sampling inspection plan with exponential distribution type based on MIL-STD-19500.

8.3 Reliability of SiC power module

The SiC power modules handle a larger power and their outer dimensions are larger compared with the discrete products. Therefore, in addition to thermal stress and electrical stress, the SiC power modules are susceptible to mechanical stress as well. The reliability design is particularly important in order to judge whether or not the required performance can be maintained throughout the expected life of devices.

The wear-out failure modes of power modules include the following modes, and it is common to confirm their capability with comprehensive evaluation of the power cycle and other items.

- Solder crack on the base plate
- Solder crack on the chip
- Separation of the bonding wire (lift off, heel crack)
- Degradation of the chip metallization, etc.

8.3.1 Power cycle

In a general power module structure, if the chip temperature varies during the operation, stress generated due to difference in the linear expansion coefficient of the aluminum wire and the SiC chip causes a crack on the wire bonding surface. If this crack advances, a failure finally occurs in the separation mode.

During the operation in actual applications, while the case temperature (Tc) of the module varies relatively moderately with a longer period, variation in the junction temperature (Tj) can be steep with a shorter time cycle, as shown in Figure 8-6. The main reasons for the short time cycle include the acceleration and deceleration operations of the device. The cycle is also generated constantly as the operation of the circuit topology. In contrast, the long time cycle is caused by the starting and stopping times of the device, among other factors.

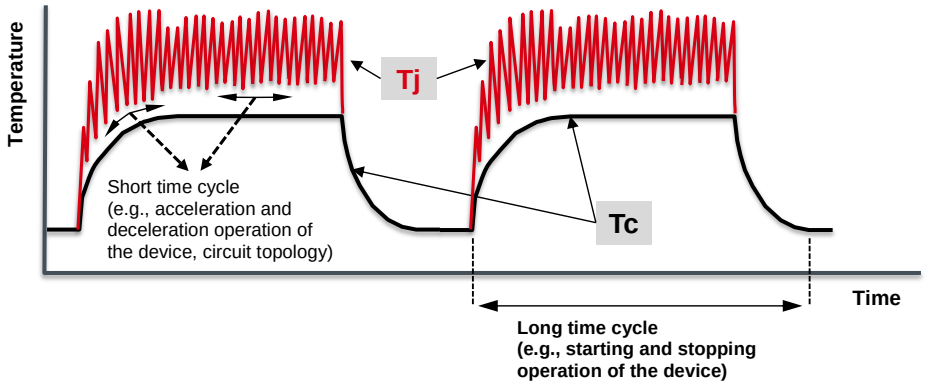


Figure 8-6. Power cycle operation mode

It is necessary to carefully consider these power cycle lives from the system design phase. Special care must be taken regarding the short time cycle generated due to the circuit topology, because the number of cycles can rapidly increase.

Figure 8-7 shows a general power cycle life curve. In this figure, the number of cycles at which the failure rate reaches 1% with the averaged Tj of 100°C is plotted. As ΔTj increases, the power cycle life is reduced exponentially.

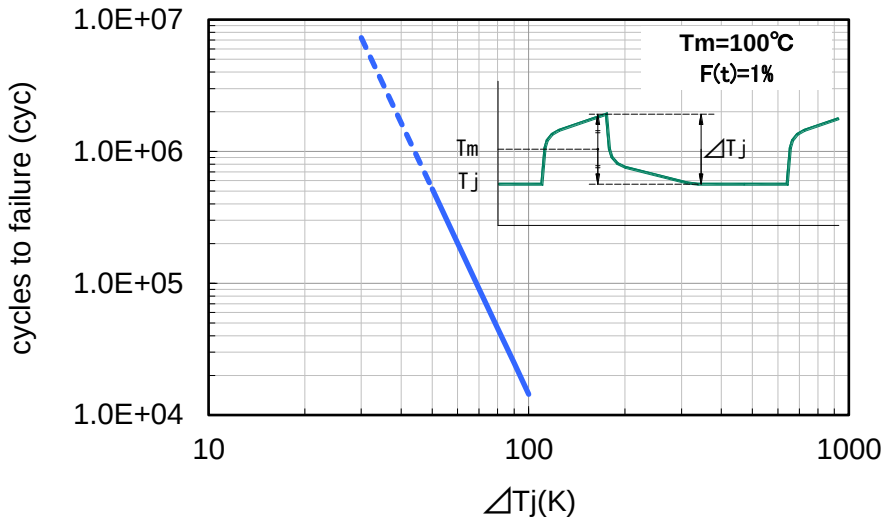


Figure 8-7 Power cycle life time curve

8.3.2 HV-H3TRB (High Voltage High Humidity High Temperature Reverse Bias)

HV-H3TRB (high temperature high humidity bias test) is a test for evaluating the durability of power devices if they are used in a high temperature and high humidity environment, providing one of the indicators to determine whether the devices can endure for a long period in a harsh environment, such as outdoor use in a high temperature and high humidity region. Inside a general case type power module, hygroscopic silicone gel is used as the insulating material for the chip. If the gel absorbs moisture, the chip can no longer tolerate high voltage, increasing the leakage current and causing a failure such as dielectric breakdown.

For ROHM's 1,700 V breakdown voltage SiC module, a new coating material and a new processing method are introduced as the measures to protect the chip from moisture, and HV-H3TRB has been passed. In the high temperature high humidity bias test where V_{DS} = 1,360 V is applied in a high temperature and high humidity environment (85°C/85%), dielectric breakdown occurred in the IGBT module within 200 hours. In contrast, no failure occurred in the SiC module (BSM250D17P2E004) over 1,000 hours and longer, demonstrating its high reliability. (Figure 8-8)

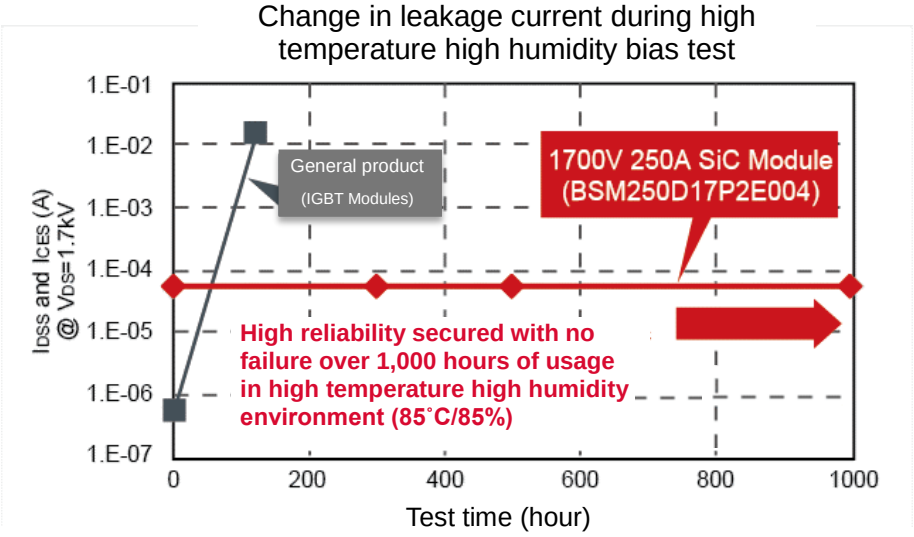


Figure 8-8. Result of HV-H3TRB test

8.3.3 Result of reliability test for SiC power module

Table 8-4 shows the result of the reliability test for the SiC power module.

Table 8-4. Result of reliability test for SiC power module

試験項目 Test Item	試験方法／準拠規格 Test Method/Standard	試験時間 Test Condition	サンプル数 n(pcs)	不良数 pn
ΔTjパワーサイクル Δ Tj power cycle	Δ Tj=100℃±5℃、Tj≦150℃、Ta=25±5℃ EIAJ ED-4701/100-106	15000cyc	5	0
ΔTcパワーサイクル Δ Tc power cycle	ΔTc=50℃±5℃、Tj≦150℃、Ta=25±5℃ EIAJ ED-4701/100-106	5000cyc	5	0
温度サイクル Temperature cycle	-40℃(60min)～RT(30min)～ 125℃(60min)～RT(30min) EIAJ ED-4701/100-105	100cyc	5	0
耐湿試験 Temperature humidity storage	85℃/85% EIAJ ED-4701/100-103	1000h	5	0
高温保存 High Temperature storage	Ta=150℃ EIAJ ED-4701/100-201	1000h	5	0
低温保存 Low Temperature storage	Ta=-40℃ EIAJ ED-4701/100-202	1000h	5	0
高温ゲートバイアス(+) High temperature gate bias(+)	Vgs=22V、Ta=150℃ JESD22-A108	1000h	5	0
高温ゲートバイアス(−) High temperature gate bias(-)	Vgs=-6V、Ta=150℃ JESD22-A108	1000h	5	0
高温逆バイアス High temperature reverse bias	Vds=960V、Vgs=0V、Ta=150℃ EIAJ ED-4701/100	1000h	5	0

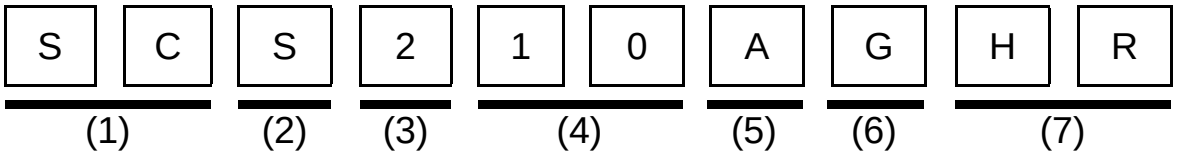
(b) 強度試験 (Stress Test)

試験項目 Test Item	試験方法／準拠規格 Test Method/Standard	試験時間 Test Condition	サンプル数 n(pcs)	不良数 pn
振動 Vibration	10～500Hz/15min 100m/s^2 Each X,Y,Z axis, EIAJ ED-4701/400-403 condition code B	6h (2h / direction)	5	0
衝撃 Shock	5000m/s2 pulse width 1msec Each X,Y,Z axis, EIAJ ED-4701/400-404 condition code B	3times / direction	5	0
熱衝撃 Thermal shock	0 $^{+5}_{-0}$(5min) ～ 100 $^{+0}_{-5}$(5min) EIAJ ED-4701/300-307 condition code A	10cyc	5	0
端子強度（引張り） Terminal strength (Pull)	Pull force ; 40N(main terminal), 20N(signal terminal) EIAJ ED-4701/401-Ⅰ	10sec	5	0
締め付けトルク強度 Mounting strength	3.5N・m(M5) EIAJ ED-4701/402-Ⅱ	10sec	5	0

※ 故障判定項目は仕様書に記載されている電気的特性にて行っています。
Failure criteria : According to the electrical characteristics specified by the specification.

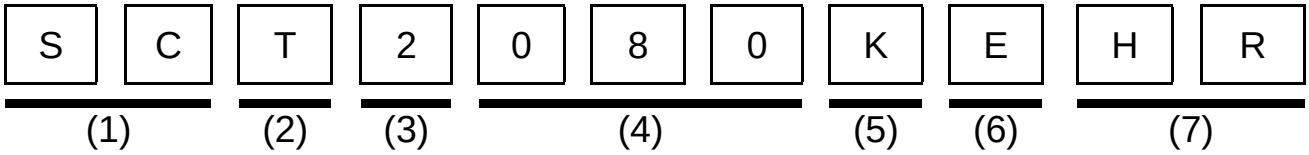
9. Construction of model name

9.1 SiC SBD (discrete product)



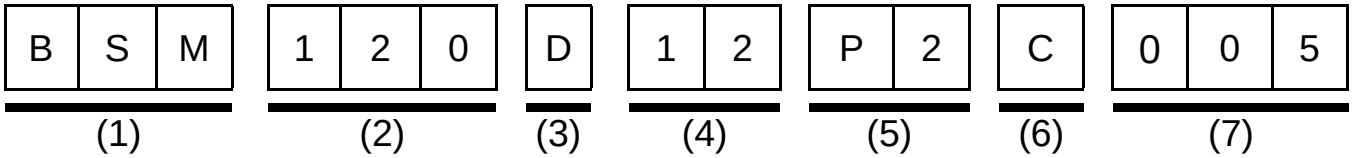
(1)	Indicates SiC		
(2)	Indicates SBD		
(3)	Indicates the generation		
(4)	Current (in ampere)	05 ➔ 5A , 20 ➔ 20A	
(5)	Voltage	A ➔ 600V, 650V	
		K ➔ 1200V	
(6)	Package	D ➔ TO-252-2DL	
		E ➔ TO-247	E2 ➔ TO-247 (including 2 elements)
		L ➔ TO-247N	L2 ➔ TO-247N (including 2 elements)
		G ➔ TO-220AC-2L	H ➔ TO-220ACP (halogen free)
		P ➔ TO-220ACP	J ➔ TO-263AB (LPTL)
		M ➔ TO-220MF-2L	Y ➔ TO268-2L
		Z ➔ TO-220FM	Z2 ➔ TO-220FM (including 2 elements)
(7)	Automotive compatible	Blank ➔ Standard product	
		HR ➔ Product compatible with AEC-Q101	

9.2 SiC MOSFET (discrete product)



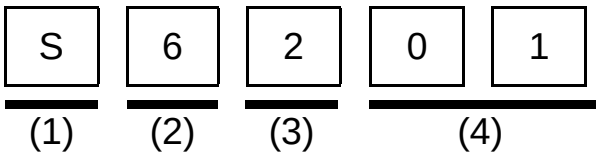
(1)	Indicates SiC		
(2)	Indicates the type	T ➔ MOSFET	
		H ➔ MOSFET + SBD combined	
(3)	Indicates the generation		
(4)	On-resistance value (in mΩ)	080 ➔ typ. 80mΩ , 160 ➔ typ. 160mΩ	
(5)	Voltage	A ➔ 600V, 650V	
		K ➔ 1200V	
		N ➔ 1700V	
(6)	Package	E ➔ TO-247	L ➔ TO-247N
		R ➔ TO-247-4L	Y ➔ TO-268-2L
		F ➔ TO-220AB	Z ➔ TO-3PFM
		W ➔ TO-263-7L	X ➔ TO-220FM
(7)	Automotive compatible	Blank ➔ Standard product	
		HR ➔ Product compatible with AEC-Q101	

9.3 SiC power module



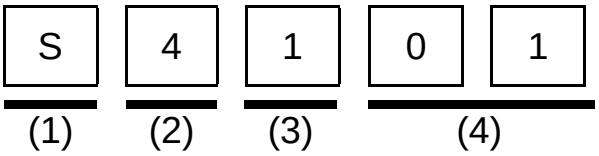
(1)	Indicates the SiC power module	
(2)	Current (in ampere)	T ➔ MOSFET H ➔ MOSFET + SBD combined
(3)	Circuit configuration	D ➔ 2 in 1 (Half bridge) C ➔ Chopper
(4)	Voltage	12 ➔ 1200V 17 ➔ 1700V
(5)	Device type	P2 ➔ Second generation P3 ➔ Third generation
(6)	Case type	C ➔ C-Type G ➔ G-Type E ➔ E-Type
(7)	Serial number	

9.4 SiC SBD (chip product)



(1)	Indicates SiC	
(2)	Indicates SBD	
(3)	Indicates the generation and the breakdown voltage	2 ➔ Second generation 600V/650V 3 ➔ Second generation 1200V 4 ➔ Second generation 1700V 5 ➔ Third generation 650V/1200V
(4)	Serial number	

9.5 SiC MOSFET (chip product)



(1) Indicates SiC

(2) Indicates MOSFET and the generation
- 2 ➔ Second generation
- 4 ➔ Third generation, fourth generation

(3) Indicates the breakdown voltage
- 2 ➔ Second generation 650 V
- 3 ➔ Second generation 1200V
- 4 ➔ Second generation 1700V
- 0 ➔ Third generation 650V
- 1 ➔ Third generation 1200V
- 5 ➔ Fourth generation 750V
- 6 ➔ Fourth generation 1200V

(4) Serial number

10. Example of application circuit

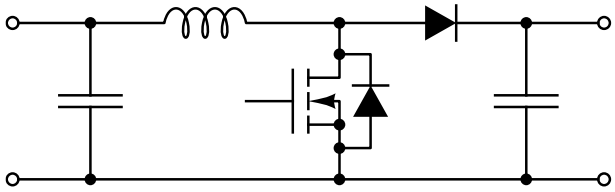
10.1 Power factor correction (PFC) circuit, boost chopper

• Correction of the efficiency by reduction in the recovery current, noise reduction

• Driving at high frequency by reduction in Err of the diode and Eon on the switch side

→ downsizing of the passive components

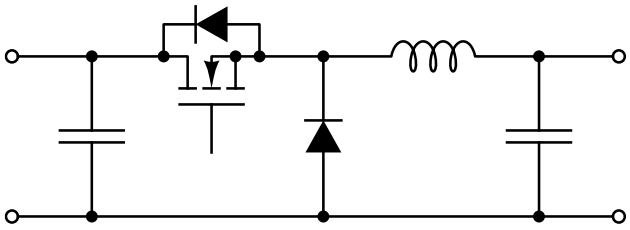
* Since the recovery does not affect the loss in the critical mode PFC, a large effect cannot be expected.



10.2 Buck chopper

• Correction of the efficiency by reduction in Eoff, simplification of the cooling structure

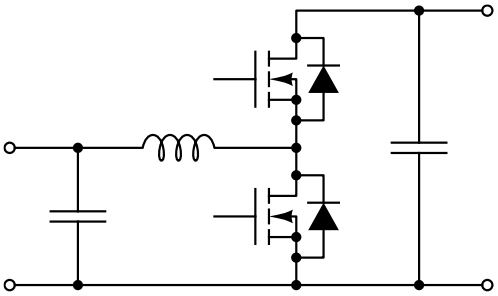
• Downsizing of the passive components by using high frequency drive



10.3 Buck-boost chopper

• Correction of the efficiency by reduction in Eon and Err, simplification of the cooling structure

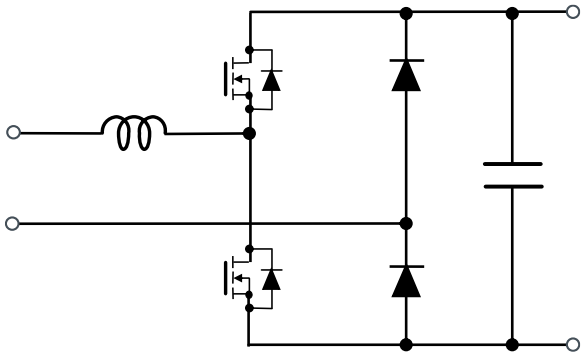
• Downsizing of the passive components by using high frequency drive



10.4 Totem pole PFC

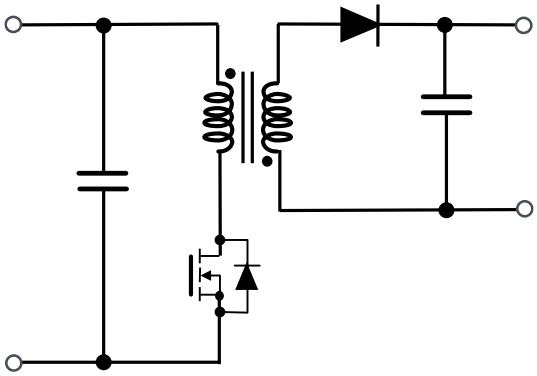
• Correction of the efficiency by reduction in Err and Eon

• Downsizing of the passive components by using high frequency drive



10.5 Flyback converter

• Correction of the efficiency by reduction in the conduction loss, simplification of the cooling structure

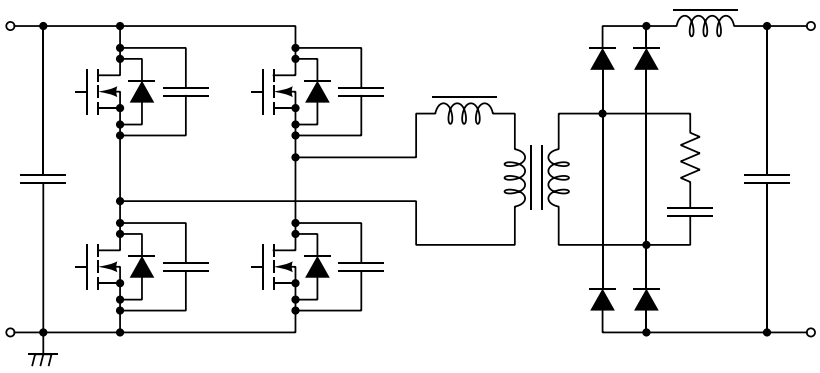


10.6 DC/DC converter (soft switching type)

• Correction of the efficiency by reduction in Eoff, simplification of the cooling structure

• High frequency drive by reduction in Eoff → downsizing of the transformer

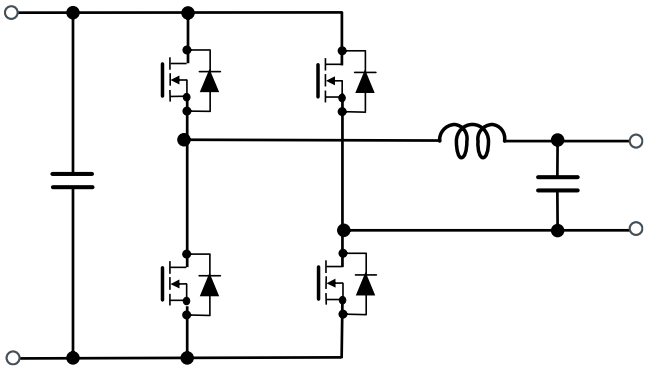
• Protection in the resonance type from damage during the off resonance operation



10.7 Inverter for power conditioner

• Correction of the efficiency by reduction in Eoff, Err, Eon, and the conduction loss as well as reduction in the conduction loss under a light load (increase in the electric power to be sold)

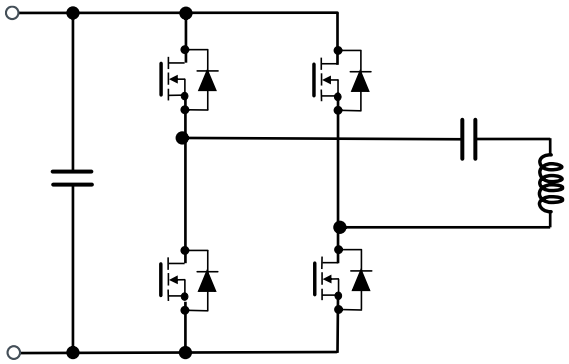
• Simplification and downsizing of the cooling structure



10.8 Inverter for IH

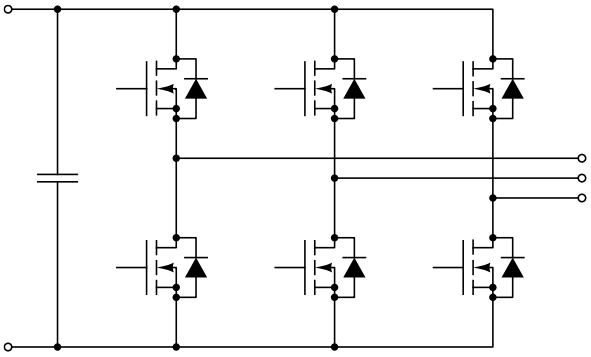
• Expansion of the process target range by increase in frequency

• Correction of the efficiency by reduction in Eoff and Err, simplification of the cooling structure



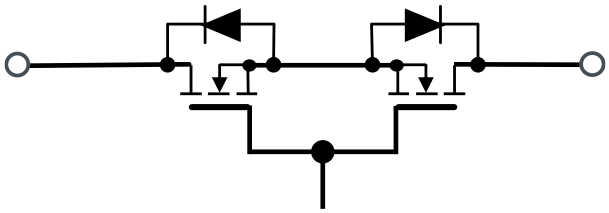
10.9 Motor drive

• Correction of the efficiency by reduction in Eoff, Err, Eon, and the conduction loss under a light load, simplification of the cooling structure



10.10 Relay

- Reduction in the on-resistance, small sized mounting
- Improvement in the reliability relative to the mechanical relay



References:

*1 “Gate-source voltage behavior in a bridge configuration”
Application Note (No. 60AN135E Rev.002) ROHM Co., Ltd., April 2020
*2 “Gate-Source Voltage Surge Suppression Methods”
Application Note (No. 62AN010E Rev.002) ROHM Co., Ltd., April 2020
*3 “Snubber circuit design methods”
Application Note (No. 62AN037E Rev.002) ROHM Co., Ltd., April 2020
*4 “Improvement of switching loss by driver source”
Application Note (No. 62AN040E Rev.002) ROHM Co., Ltd., April 2020
*5 “Optimized heat sink assembly method for effective heat dissipation”
Application Note (No. 62AN126J Rev.001) ROHM Co., Ltd., December 2019
*6 “Self-turn-on countermeasure by using active miller clamp”
Application Note (No. 63AN041J Rev.001) ROHM Co., Ltd., July 2020

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